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A novel CMOS photosensor with a gate-body tied NMOSFET structure

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ABSTRACT

A novel CMOS photosensor with a gate-body tied NMOSFET structure realized in the triple well is presented. The photocurrent is amplified by the lateral and vertical BJT action, which results in two different output photocurrents, which can be used for different applications within a pixel. The lateral action results in the drain current with higher sensitivity at low light intensity. And the vertical action results in the collector current with uniform responsivity over wider range of the light intensity. The proposed photosensor is compatible with CMOS circuits.

Keywords: Gate-body tied NMOSFET, triple well, lateral BJT, vertical BJT, photosensor

1. INTRODUCTION

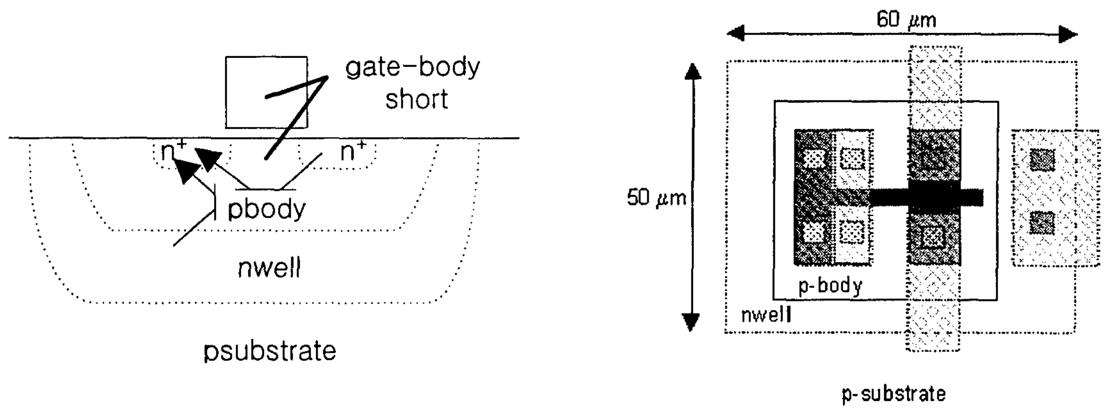
There has been much interest on the miniaturization of assay for the use of detection of biological species or specific DNA sequences, which makes various experiments to be done quickly with low cost [1,2]. The conventional detection method is to use of fluorescence label and high performance CCD camera. But this CCD-based detection system is very expensive and relatively large compared with micro-scale assay. So, there is a strong need for an integrated detection chip compatible with the micro-scale assay. The detection chip contains photosensors such as phototransistor [3] or photodiode [4] fabricated with CMOS process. As the array density increases, the detection chip has complex circuits and high performance photosensors are needed. And light source is needed for fluorescence activation and but this light source itself makes the detection of emitted fluorescence light confused. So, a novel photosensor suitable for the detection of fluorescence light is greatly needed.

On the other hand, great attention has been paid to CMOS image sensor [5,6,7] since it has many advantages such as low power, price, and CMOS circuit compatibility compared to the conventional CCD image sensor. CCD image sensor is fabricated with the highly optimized process for charge transferring [5] and all the output charges are transformed to the voltage signal by a high sensitive amplifier. But CMOS image sensor is fabricated with the standard CMOS process and the output voltage (or current) of each sensor is directly accessed with a in-pixel amplifier or buffer. As a result, CMOS image sensor can be easily integrated with CMOS circuits and is useful for various applications. Widely used CCD concepts such as pixels, charge transferring and amplifiers have been developed over many years and the process has optimized to CCD and it became different with CMOS process. Consequently, simple implementation of CCD concept with CMOS process is not satisfying and a novel CMOS photosensor is needed to achieve high quality image [7].

The gate-body tied MOSFET structure has been recently used as a CMOS photosensor. It uses high current gain caused by the lateral BJT action [8,9] and useful compared to widely used n+ p-type substrate. But in the proposed photosensor [9], some of the injected holes are wasted by the vertical diffusion and also this can cause the latch-up. In this work, we show that the quantity of vertically injected holes can be comparable with that of laterally injected ones. And a novel photosensor is proposed. It is a gate-body tied NMOSFET in the triple well. Using this photosensor, two photocurrents are available by the lateral and vertical actions of the BJT. And it will be shown from the experiments that two currents have different characteristics. Some scaling properties of the device will be also discussed.

2. DEVICE STRUCTURE AND FABRICATION

The proposed photosensor is a gate-body tied NMOSFET realized in the triple well as shown in Fig.1. It is fabricated with 1.5μm CMOS process and some modifications are made to implement triple well. In this photosensor, pbody and source regions correspond to the base and emitter, respectively, of both lateral and vertical BJT's and nwell region is the collector of vertical BJT. The base widths of lateral and vertical BJT's are defined by the effective gate length (~0.67μm in this work) and difference of the junction depth between pbody and nwell (~0.80μm in this work), respectively. Photogeneration takes place at drain-pbody junction and nwell-pbody junction. These junctions are placed at different depths from the silicon surface and have different light absorption length. So, the drain current and nwell current have different spectral responses, which may be used to distinguish the light source for fluorescence activation and emitted fluorescence light. The gate oxide thickness is 250 Å and gate material is N^+ polysilicon. A channel implantation with boron ions was performed followed by an arsenic implantation to form the single source/drain. Gate and pbody contacts are shorted with the metal later.



(a) (b)

Fig.1. Structures of a proposed photosensor (a) schematic cross section (b) top view.

Fig.2 shows the simulated doping profile under the source region. Nwell is implemented with a phosphorous implantation and 20-hour drive-in at 1100°C. And the p-type body (pbody) is implemented with a boron implantation and 150-minite drive-in at 1050°C. In implementing triple well, much care is done to set the threshold voltage of PMOSFET to –0.7V.

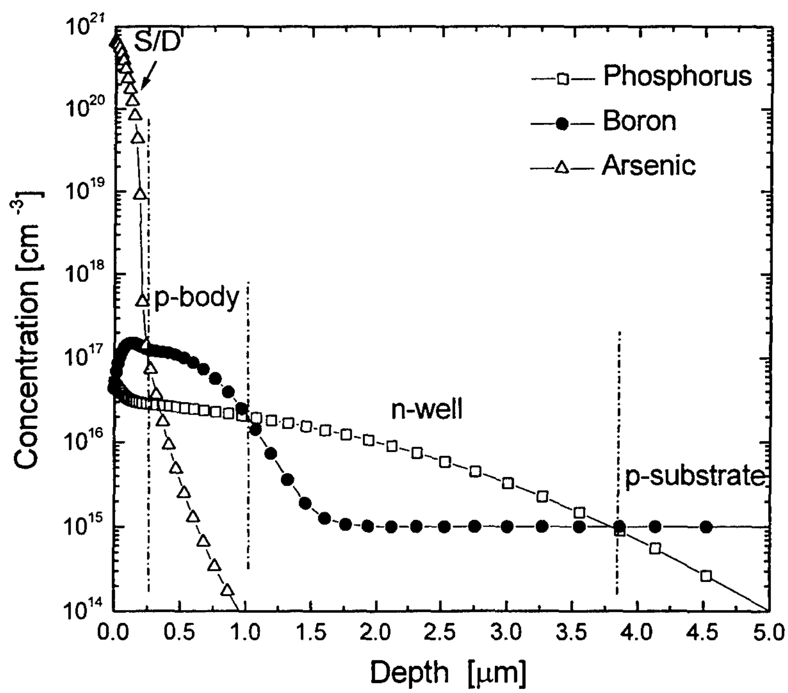


Fig.2. Doping profile under the source area

3. EXPERIMENTAL RESULT AND DISCUSSIONS

Fig. 3 shows the drain and collector(nwell) current characteristics of the fabricated device with the gate and pbody tied and floated. The peak current gains of the drain and collector currents are about 3730 and about 257, respectively. Until the surface channel is formed, the drain current is mostly composed of the diffusion of electrons injected from the source into the silicon surface. When the gate voltage reaches the threshold voltage(with the pbody voltage fixed to the gate voltage), the drain current is mostly due to the surface channel current and the contribution from the BJT action is minimal since the surface potential is nearly fixed. On the other hand, the collector current is mostly composed of the electron diffusion for all gate and pbody bias conditions. As a result, the drain current is higher than the collector current at low gate and pbody voltage but the difference becomes smaller as the voltage increases. And drain current is lower than the collector current after the channel is formed.

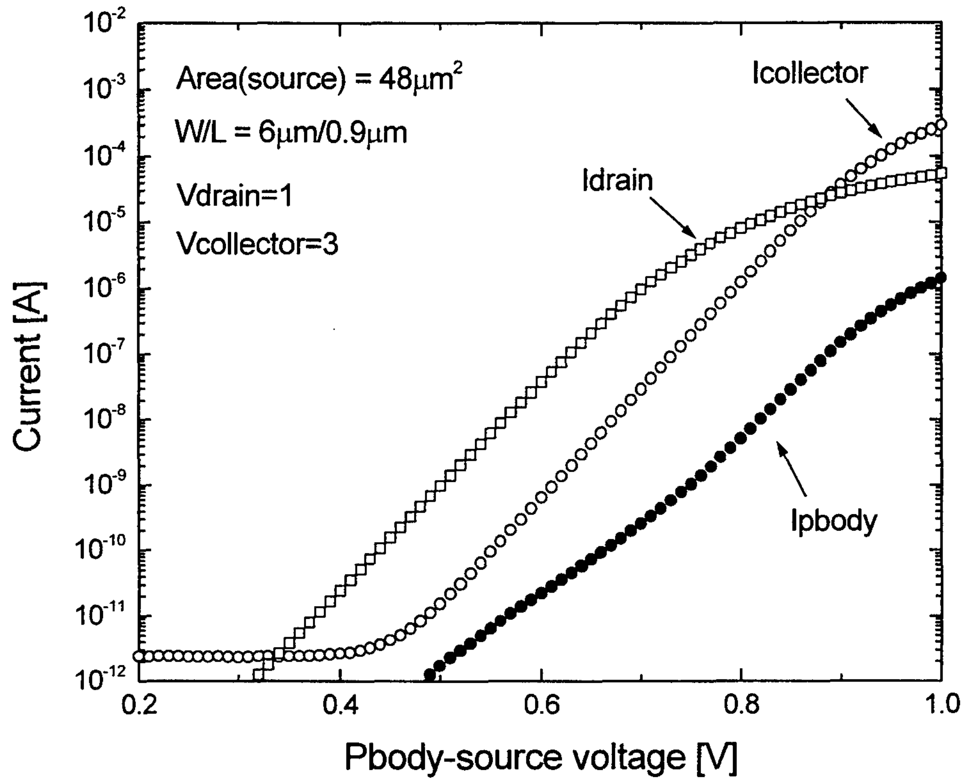


Fig. 3. Gummel plot for gate-body tied NMOSFET with W/L=6μm/0.9μm. $V_{collector}$=3V, V_{drain}=1V and V_{source}=$V_{psubstrate}$=0V. Open square and circle marks are drain and collector currents, respectively. And Filled circle mark is pbody current. The inset shows the device structure.

Fig. 4 shows the measured photocurrents and photogains of the proposed photosensor. The photogain is defined to be the ratio of the collector (drain) current due to BJT action to the collector-pbody (drain-pbody) diode current. The photodiodes currents are measured for the diodes in pbody-drain and pbody-nwell junctions with the gate floated. The photogains of the collector and drain are above 1000 and 50000, respectively. Drain photocurrent is higher than the collector photocurrent at low light intensity, but the difference becomes smaller as the light intensity increases and collector photocurrent is higher at high light intensity. It is because the accumulated holes raise the pbody voltage and channel is formed. Drain photocurrent shows the much higher photogain especially low light intensity and collector photocurrent shows the more linear response over wide range of the light intensity.

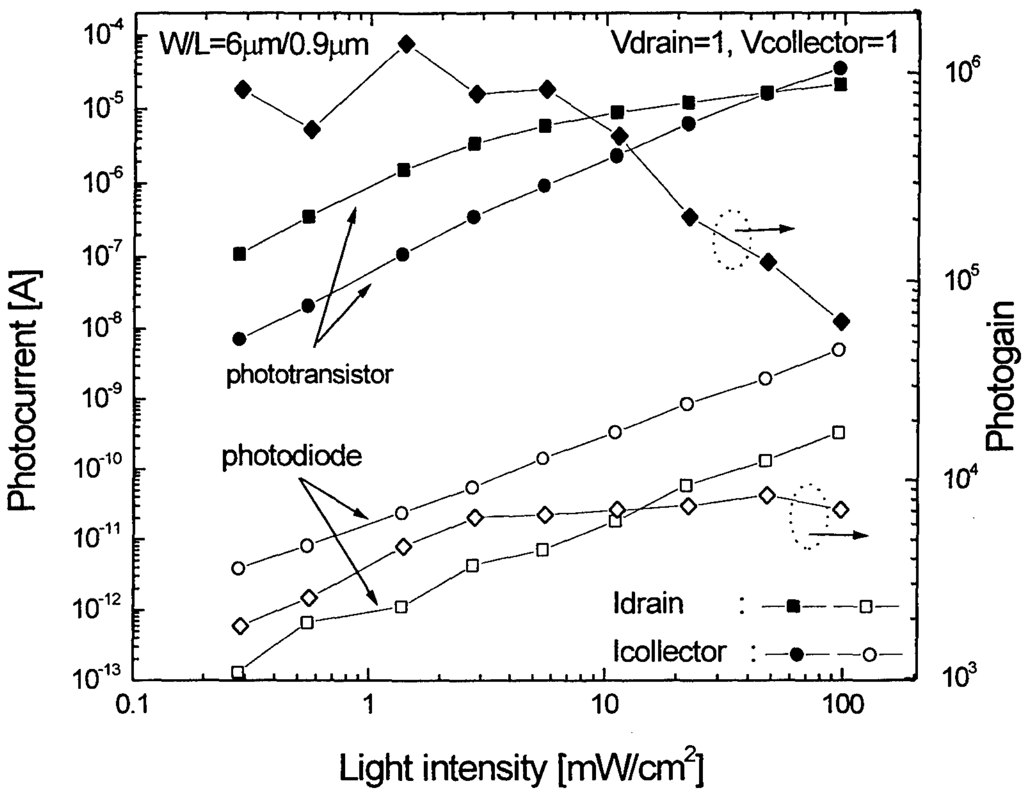


Fig. 4. Photocurrents and photogain of drain and collector with W/L=6μm/0.9μm. $V_{collector}=V_{drain}=1V$ and $V_{source}=V_{psubstrate}=0V$. Filled and open marks are the currents of phototransistor and photodiode, respectively. Square and circle marks are the currents of drain and collector, respectively. Diamond marks are the photogain defined as the ratio of phototransistor current to photodiode current.

Fig. 5 shows the photocurrents measured at the drain and collector terminals with dark and light conditions as a function of drain voltage. The photocurrents show the linear or logarithmic increase with the light intensity as shown in Fig. 4 below the breakdown voltage. Drain dark current is higher than collector dark current due to the lateral BJT action, but it is lower than 10pA at room temperature. The breakdown voltage is about 2.9V in the dark condition, and it decreases to about 2.0V under the light, which is mainly due to the photogeneration induced avalanche breakdown. Between the photo-triggered breakdown and the dark breakdown voltage, the photocurrents increase rapidly by the photo-triggered avalanche, which may be used as a high sensitive photodetector at very low light intensity.

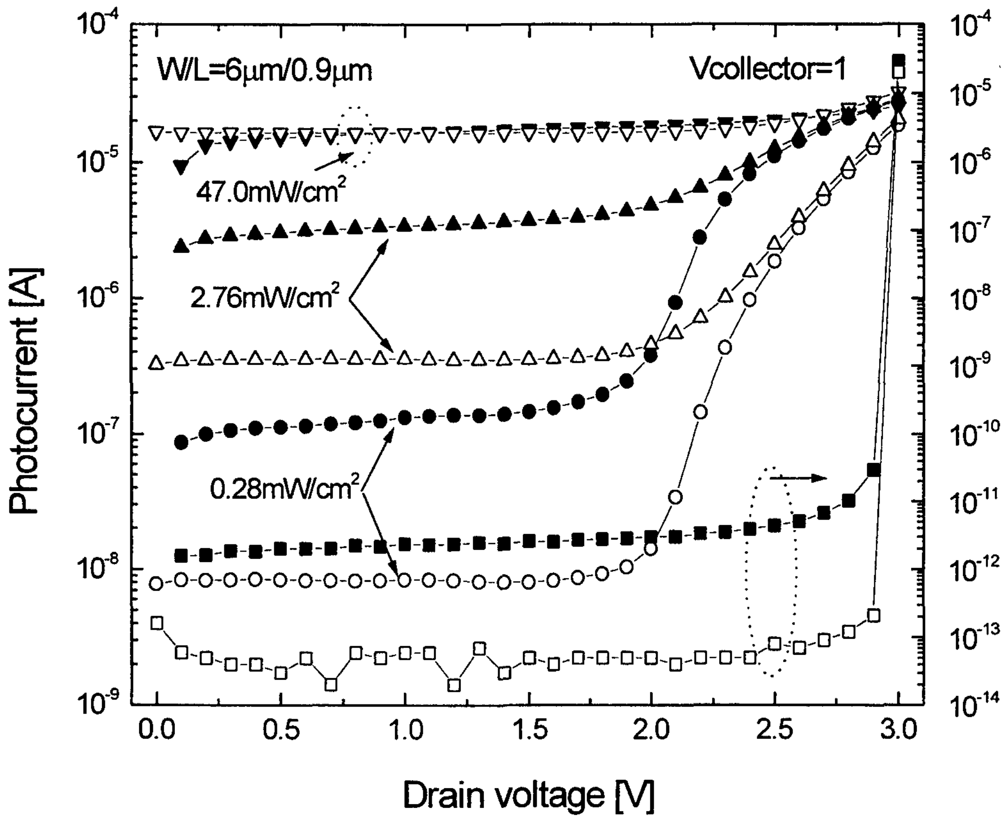


Fig. 5 Photocurrents of drain and collector versus drain voltage. W/L=6µm/0.9µm. $V_{collector}$=1V, and V_{source}=$V_{psubstrate}$=0V. Filled and open marks are drain and collector photocurrents, respectively.

In the following, some scaling properties and associated design considerations will be explained. Fig. 6 shows that the drain photocurrent, and dark current (I_d) increase as the gate length scales down while the collector photocurrent and dark current (I_c) remain constant.

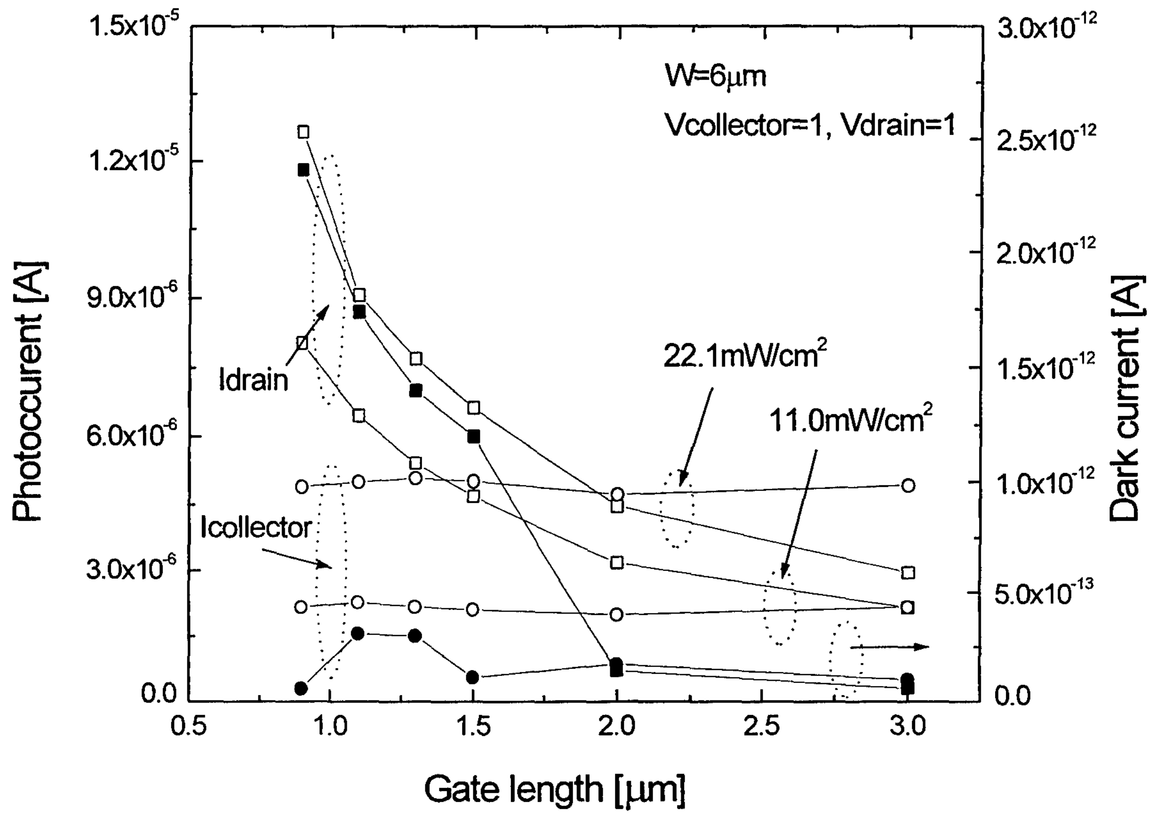


Fig. 6. Photocurrents for the various gate lengths. W=6μm. $V_{collector}=V_{drain}=1V$, and $V_{source}=V_{psubstrate}=0V$. Filled marks are the dark currents. Square and circle marks are the photocurrents of drain and collector, respectively.

In the pbody at steady state, the magnitude of in-flux of the generated holes and out-flux to source is same and can be expressed as,

$$q\eta\Phi A_{gen} = I_0 \exp(V_{BE} / nV_t) \tag{1}$$

where η, Φ, V_t, I_0, A_{gen}, and n are the quantum efficiency, photon flux, and thermal voltage, saturation current and area where photogeneration occurs, and non-ideal factor, respectively. After solving (1), pbody voltage is expressed as,

$$V_{BE} = nV_t \ln(q\eta\Phi A_{gen} / I_o)\,. \tag{2}$$

The dependency of drain and collector photocurrent on the pbody voltage can be expressed as,

$$I_c \propto I_o \exp(V_{BE} / nV_t) = q\eta\Phi A_{gen} \tag{3}$$

$$I_{d,\,subthreshold} \propto W \exp(V_{BE} / nV_t) = q\eta\Phi A_{gen} W / I_o \tag{4a}$$

$$I_{d,\,above\ threshold} \propto W(V_{BE} - V_{TH})^{\alpha} \tag{4b}$$

where W is gate width, V_{BE} is same V_{GS}, and I_0 is dependent on the source area. (2) and (3) show that I_c/A_{gen} is independent of the source area while (2) and (4) show that I_d/W decreases as the source area increases for a fixed A_{gen}.

Fig. 7 shows the relation of photocurrents with source area. It verifies this relation that I_c/A_{gen} is independent of the source area while $I_d/(W{\cdot}A_{gen})$ decreases as the source area increases.

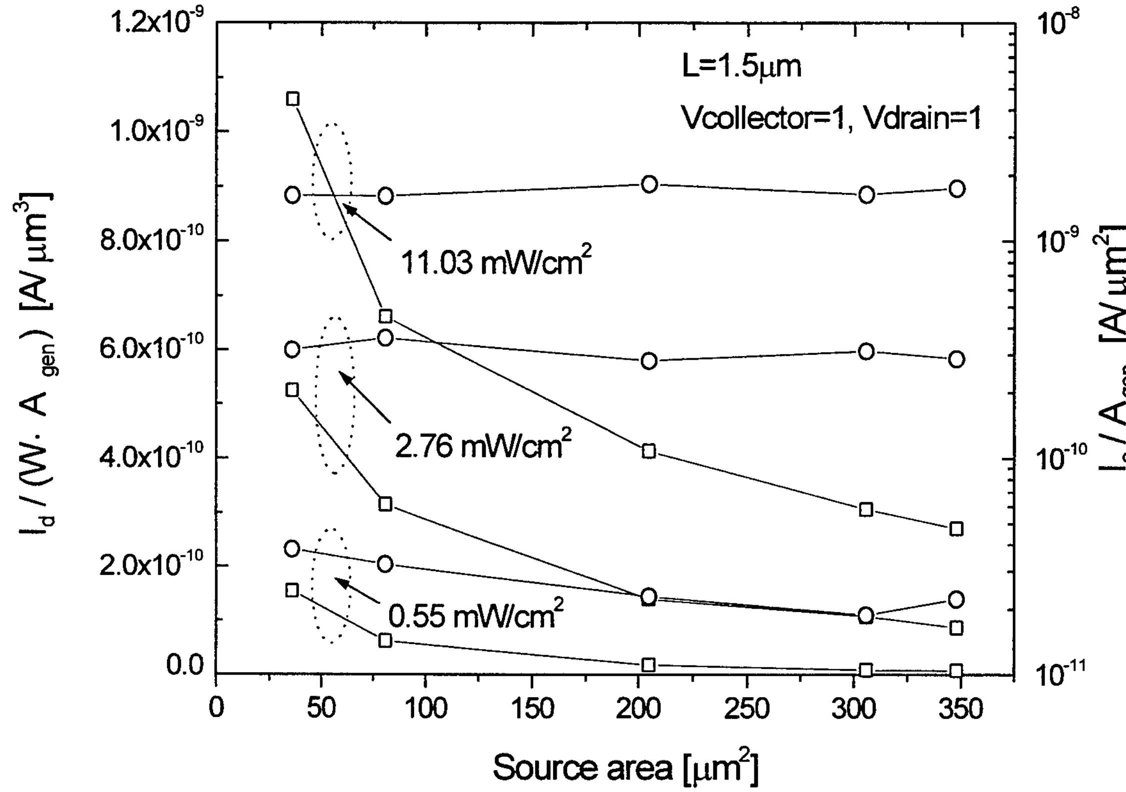


Fig. 7. Photocurrents for the various source areas. L=1.5μm. $V_{collector}=V_{drain}=1V$, and $V_{source}=V_{psubstrate}=0V$. Square marks are the drain photocurrents per unit gate width and unit photogeneration area. Circle marks are the collector photocurrents per unit photogeneration area.

As a result, the maximum drain photocurrent can be achieved with the ring gate structure for a given pixel size, since effectively large gate width with the small source area in the ring gate and the large drain area can be realized to obtain the high pbody voltage and large photogeneration area.

4. CONCLUSION

A novel photosensor is proposed and fabricated. Two output photocurrents are obtained through the drain and collector with different magnitudes, dark currents, and responsivities to the light intensity. The drain photocurrent has higher magnitude at low light intensity and higher photogain, while the collector photocurrent has lower dark current, higher magnitude at high light intensity and uniform responsivity over wide range of the light intensity. And the drain photocurrent was shown to increase with the scaled gate length and source area while the collector photocurrent is independent of the gate length and source area for a fixed photogeneration area. A ring gate structure was proposed to obtain large gate width, small source area and large drain area for a given pixel size.

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