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APPARATUS AND METHOD FOR CALIBRATING VOLTAGE SPIKE WAVEFORMS

TO ALL WHOM IT MAY CONCERN:

BE IT KNOWN THAT (1) JOSEPH M. MUHITCH employee of the United States Government and citizen of the United States of America, (2) EDWARD W. WILBUR, JR., citizen of the United States of America, residents (1) Exeter, County of Washington, State of Rhode Island and (2) Bristol, County of Bristol, State of Rhode Island, have invented certain new and useful improvements entitled as set forth above of which the following is a specification:

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1 Attorney Docket No. 83343

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3 APPARATUS AND METHOD FOR CALIBRATING VOLTAGE SPIKE WAVEFORMS

4

5 STATEMENT OF GOVERNMENT INTEREST

6 The invention described herein may be manufactured and
7 used by or for the Government of the United States of
8 America for governmental purposes without the payment of any
9 royalties thereon or therefor.

10

11 CROSS-REFERENCE TO RELATED PATENT APPLICATIONS

12 This patent application is co-pending with one related
13 patent applications entitled APPARATUS AND METHOD FOR
14 CALIBRATING VOLTAGE SPIKE WAVEFORMS FOR THREE-PHASE
15 ELECTRICAL DEVICES AND SYSTEMS (Attorney Docket No. 83342),
16 by the same inventor as this application.

17

18 BACKGROUND OF THE INVENTION

19 (1) Field of the Invention

20 The present invention generally relates to an apparatus
21 and method for calibrating voltage spike waveforms that are
22 used to test survivability and compatibility of an
23 electrical device.

1 2. Description of the Prior Art

2 Many electrical devices, both military and commercial-
3 off-the-shelf ("COTS"), have specifications that are
4 incomplete with regard to compatibility and survivability.
5 This problem is exacerbated when COTS devices are integrated
6 with devices configured in accordance with military
7 specifications such as onboard electronics of a submarine or
8 other naval vessel. Vendors typically do not perform tests
9 or evaluations on the compatibility and survivability
10 characteristics of electrical devices.

11 What is needed is a technique for efficiently and
12 inexpensively testing the compatibility and survivability of
13 electrical devices.

14 Prior art systems and techniques for testing electrical
15 devices with voltage spike waveforms and voltage spike
16 suppression devices are disclosed in U.S. Patent Nos.
17 4,307,342, 5,463,315, 5,525,926, 5,623,215 and 6,088,209.
18 However, such prior art systems and techniques do not
19 address the aforementioned problem or meet the
20 aforementioned need.

21

22 SUMMARY OF THE INVENTION

23 It is therefore an object of the present invention to
24 provide an apparatus and method for calibrating voltage
25 spike waveforms that are used to test the survivability and

1 compatibility characteristics of electrical equipment
2 including military and commercial off-the-shelf electrical
3 devices.

4 It is another object of the present invention that the
5 aforesaid apparatus and method be relatively inexpensive to
6 implement.

7 Other objects and advantages of the present invention
8 will be apparent from the ensuing description.

9 Thus, the present invention is directed to, in one
10 aspect, an apparatus for calibrating voltage spikes used in
11 testing an electrical device, comprising an input for
12 receiving a voltage spike, and power supply inputs for
13 receiving power for energizing an electrical device under
14 test. The power supply inputs comprise a high voltage
15 input, a common input and a ground input. The apparatus
16 further comprises a plurality of outputs comprising a high
17 voltage output, a common output, and a ground output. The
18 plurality of outputs are configured for connection to
19 corresponding high voltage, common and ground inputs of the
20 electrical device under test. The power supply common and
21 ground inputs are connected to the common and ground
22 outputs, respectively. The apparatus further comprises a
23 circuit for connecting and disconnecting the power supply
24 high voltage input to and from, respectively, the high
25 voltage output, selecting a pair of the plurality of

1 outputs, transforming the voltage spike into a predetermined
2 voltage spike waveform, and applying the predetermined
3 voltage spike waveform to the selected pair of outputs.

4 In a related aspect, the present invention is directed
5 to a method of testing an electrical device, which includes
6 providing an electrical device under test having high
7 voltage, common and ground inputs, providing a power source
8 for energizing the electrical device under test wherein the
9 power source has high voltage, common and ground outputs,
10 and connecting the common and ground outputs of the power
11 source to the common and ground inputs of the electrical
12 device under test. The method further comprises selecting a
13 pair of the plurality of inputs of the electrical device,
14 connecting the power supply high voltage input to the high
15 voltage input of the electrical device under test if the
16 selected pair comprises the high voltage and common inputs
17 of the electrical device, generating a voltage spike,
18 transforming the voltage spike into a predetermined voltage
19 spike waveform, and applying the predetermined voltage spike
20 waveform to the selected pair of inputs of the electrical
21 device under test.

22

23 BRIEF DESCRIPTION OF THE DRAWINGS

24 The foregoing features of the present invention will
25 become more readily apparent and may be understood by

1 referring to the following detailed description of an
2 illustrative embodiment of the present invention, taken in
3 conjunction with the accompanying drawings, in which:

4 FIG. 1 is a block diagram showing a testing system that
5 utilizes the apparatus of the present invention;

6 FIG. 2 is a schematic diagram of one embodiment of the
7 apparatus of the present invention; and

8 FIG. 3 is a schematic diagram of a capacitive circuit
9 shown in FIG. 2.
10

11 DESCRIPTION OF THE PREFERRED EMBODIMENTS

12 The present invention is directed to a single-phase
13 voltage spike waveform calibrator for performing a voltage
14 spike test on single-phase electrical devices and equipment
15 under test.

16 Referring to FIG. 1, there is shown a testing system
17 that utilizes single phase voltage spike calibrator 10 of
18 the present invention. Calibrator 10 receives and
19 calibrates voltage spikes that are generated and provided by
20 voltage spike generator ("VSG") 12. The system shown in
21 FIG. 1 effects particular tests on the electrical device or
22 unit under test ("UUT") 14 wherein each test entails
23 providing a predetermined voltage spike waveform into UUT
24 14. UUT 14 can be any type of single phase electrical
25 device. UUT 14 includes high voltage input 16, common input

1 18 and ground input 20. Specifically, calibrator 10
2 transforms the voltage spike provided by VSG 12 into
3 particular voltage spike waveforms that are required for
4 complete survivability and compatibility testing of UUT 14.

5 Three standard tests are commonly utilized. In the
6 first test, calibrator 10 transforms the voltage spike
7 provided by VSG 12 into a first predetermined voltage spike
8 waveform which is applied to the high voltage input 16 and
9 common input 18 of UUT 14. This test is referred to as the
10 line-to-line test. In the second test, calibrator 10
11 transforms the voltage spike outputted by VSG 12 into a
12 second predetermined voltage spike waveform which is applied
13 to the high voltage input 16 and ground input 20 of UUT 14.
14 This test is referred to as the high-to-ground test. In the
15 third test, calibrator 10 transforms the voltage spike
16 provided by VSG 12 into a third predetermined voltage spike
17 waveform which is applied to the common input 18 and ground
18 connector 20 of UUT 14. This third test is referred to as
19 the common-to-ground test. In each of these aforesaid
20 tests, each of the first, second, and third predetermined
21 voltage waveforms may have the same or different waveform
22 characteristics, e.g. peak voltage, overshoot, rise time,
23 fall time, etc.

24 Referring to FIG. 1, power supply 22 provides a supply
25 voltage and current to the UUT 14. Power supply 22 includes

1 high voltage output 24, common output 26 and ground
2 connector 28 that are inputted into attenuator 30.
3 Attenuator 30 is connected between power supply 22 and
4 calibrator 10 and attenuates high voltage spikes in order to
5 prevent such spikes from being applied to power supply 22.
6 Specifically, attenuator 30 is configured to attenuate the
7 high frequency components of the voltage spike outputted by
8 VSG 12. For example, attenuator 30 is configured to
9 attenuate a voltage spike having a peak voltage of 1000
10 volts so as to yield a voltage spike having a peak voltage
11 of 300 volts. Attenuator 30 includes high voltage line 32,
12 common line 34 and ground line 36 that are connected
13 corresponding to high voltage, common and ground inputs,
14 respectively, calibrator 10. Attenuator 30 is well known in
15 the art and is therefore not discussed in detail.

16 Calibrator 10 includes high voltage input 38, common
17 input 40 and ground input 42 that are connected to high
18 voltage line 32, common line 34 and ground line 36,
19 respectively, of attenuator 30. Calibrator 10 further
20 comprises high voltage output 44, common output 46 and
21 ground output 47. Common input 40 is connected to common
22 output 46. Ground input 42 is connected to ground output
23 47. Calibrator 10 further includes high voltage input 48
24 and common input 49 that are connected to the high voltage
25 and common outputs, respectively, of VSG 12.

1 Referring to FIG. 2, calibrator 10 further includes
2 switch 50 that comprises a plurality of groups 50a-h of
3 switch contacts. Group 50a comprises switch contacts SW1-
4 11, SW1-12, SW1-13, and SW1-14. Switch contact SW1-11 is
5 connected to high voltage output 44 of calibrator 10.
6 Switch contact SW1-12 is an open circuit. Switch contact
7 SW1-13 is connected to switch contact SW1-14 and both switch
8 contacts SW1-13 and SW1-14 are connected to one end of fuse
9 52. The other end of fuse 52 is connected to high voltage
10 input 38.

11 Group 50b of switch contacts comprises switch contacts
12 SW1-21, SW1-22, SW1-23 and SW1-24. Switch contact SW1-21 is
13 connected to VSG high voltage input 48. Switch contact SW1-
14 22 is connected to high voltage output 44. Switch contact
15 SW1-23 is connected to switch contact SW1-24. Group 50c of
16 switch contacts comprises switch contacts SW1-31, SW1-32,
17 SW1-33 and SW1-34. Resistor R1 is connected between switch
18 contact SW1-24 and switch contact SW1-31. In one
19 embodiment, resistor R1 has a resistance of about one ohm.
20 Switch contact SW1-32 is an open circuit. Switch contact
21 SW1-33 is connected to high voltage output 44. Switch
22 contact SW1-34 is connected to common output 46.

23 Group 50d comprises switch contacts SW1-41, SW1-42,
24 SW1-43, and SW1-44. Switch contact SW1-41 is connected to
25 node 60 of capacitive circuit 62. Capacitive circuit 62 is

1 described in detail in the ensuing description. Switch
2 contact SW1-42 is an open circuit. Switch contact SW1-43 is
3 connected to one end of fuse 63. The other end of fuse 63
4 is connected to common input 40. Switch contact SW1-44 is
5 connected to one end of fuse 52.

6 Group 50e comprises switch contacts SW1-51, SW1-52,
7 SW1-53 and SW1-54. Switch contact SW1-51 is connected to
8 VSG common input 49 and node 64 of capacitive circuit 62.
9 Switch contact SW1-52 is connected to one end of fuse 52.
10 Switch contacts SW1-53 and SW1-54 are open circuits.

11 Group 50f comprises switch contacts SW1-81, SW1-82,
12 SW1-83, and SW1-84. Switch contact SW1-81 is connected to
13 node 66 of capacitor network 62. Switch contact SW1-82 is
14 connected to switch contact SW1-43 and one end of fuse 63.
15 Switch contacts SW1-83 and SW1-84 are connected to one end
16 of fuse 68. The other end of fuse 68 is connected to ground
17 input 42.

18 Referring to FIGS. 2 and 3, capacitive circuit 62
19 comprises capacitor networks 80 and 82 and switch 90.
20 Switch 90 comprises two groups of switch contacts. The
21 first group, group 90a, comprises switch contacts SW2-11
22 through SW2-18, switch contacts SW2-21 through SW2-28, and
23 switch contacts SW2-31 through SW2-38. Switch contacts SW2-
24 13, SW2-15, SW2-17, SW2-22, SW2-25, SW2-26, SW2-32, SW2-33,
25 and SW2-34 are open circuits. Network 80 comprises

1 capacitors C1, C2, and C3. Switch 90 can be adjusted to
2 produce a resultant capacitance between nodes 64 and 66 that
3 is based on any one of capacitors C1, C2, and C3 by
4 themselves or in any combination with each other. Hence,
5 the resulting capacitance exhibited by network 80 can be any
6 one of seven possible capacitances depending upon the
7 setting of switch 90. The seven possible resulting
8 capacitances are shown in Table I.

9

10 Table I: Possible Resulting Capacitances

11 C1

12 C2

13 C3

14 C1 + C2

15 C1 + C3

16 C2 + C3

17 C1 + C2 + C3

18 In Table I, the sign "+" designates summation. In one
19 embodiment, capacitor C1 has a capacitance of 5 uf
20 (microfarads), capacitor C2 has a capacitance of 10 uf and
21 capacitor C3 has a capacitance of 20 uf. Thus, in such an
22 embodiment, the possible resulting capacitance is between
23 5 uf and 35 uf, inclusive.

24 Network 82 also comprises three capacitors and a second
25 group of switch contacts that are part of switch 90. The

1 aforesaid switch contacts and capacitors are connected in
2 the same manner as capacitors C1, C2 and C3 and the switch
3 contacts of group 90a described above. Switch 90 can be
4 adjusted to produce a resultant capacitance between nodes 60
5 and 66 that is based on any one of capacitors in network by
6 themselves or in any combination with each other. The
7 resulting capacitance exhibited by network 82 can be any one
8 of seven possible capacitances depending upon the setting of
9 switch 90. In one embodiment, the capacitors in network 82
10 have the same capacitances as capacitors C1, C2 and C3.
11 Thus, in such an embodiment, the possible resulting
12 capacitance is also between 5 uf and 35 uf, inclusive.

13 In a preferred embodiment, switch 90 is configured so
14 that the capacitance between nodes 60 and 66, and between
15 nodes 64 and 66 is substantially the same at all times.

16 Calibrator 10 further includes monitoring circuit 92
17 for monitoring the voltage spike waveforms that are inputted
18 into UUT 14. Monitoring circuit 92 is discussed in detail
19 in the ensuing description.

20 In order to conduct the first test, known as the line-
21 to-line test, UUT 14 is de-energize by inactivating power
22 supply 22. Next, calibrator circuit 10 is connected between
23 UUT 14 and power supply 22. In a preferred embodiment,
24 attenuator 30 is connected between power supply 22 and
25 calibrator 10. Next, UUT 14 is energized by activating

1 power supply 22 and VSG 12 is connected to calibrator 10.
2 Next, switch 50 is adjusted to implement the line-to-line
3 test. When switch 50 is adjusted to implement the line-to-
4 line test, each pair of switch contacts shown in each row of
5 Table II are electrically connected together.

6

7

Table II

SW1-11	SW1-12 (open circuit)
SW1-21	SW1-22
SW1-31	SW1-32 (open circuit)
SW1-51	SW1-52
SW1-41	SW1-42 (open circuit)
SW1-81	SW1-82

8 For example, switch contacts SW1-11 and SW1-12 are connected
9 together, switch contacts SW1-51 and SW1-52 are connected
10 together, and switch contacts SW1-81 and SW1-82 are
11 connected together. As a result of each pair of switch
12 contacts in each row of Table II being connected together,
13 the VSG high voltage input 48 is connected to high voltage
14 output 44. VSG common input 49 is connected to node 64 of
15 capacitor network 82 and node 66 is connected to common
16 input 40 via switch contacts SW1-81 and SW1-82. Switch
17 contact SW1-41 is connected to SW1-42 which is connected to
18 an open circuit. Therefore, capacitor network 82 is out of
19 the circuit.

1 Next, switch 90 is adjusted to exhibit a desired
2 resulting capacitance between nodes 64 and 66. The actual
3 desired resulting capacitance is appropriate for conducting
4 the line-to-line test. As a result, the resulting
5 capacitance exhibited by capacitor network 82 transforms the
6 voltage spike generated by VSG 12 into a particular voltage
7 spike waveform having particular required waveform
8 characteristics.

9 Next, VSG 12 is activated to output a voltage spike
10 into high voltage and common inputs 48 and 49, respectively.
11 Capacitor network 80 transforms the voltage spike into the
12 desired voltage spike waveform as described in the foregoing
13 description. Switch 50 is adjusted so that the
14 aforementioned predetermined voltage spike waveform is
15 applied to the high voltage output 44 and common output 46
16 of calibrator 10 which in turn causes the predetermined
17 voltage spike waveform to be applied to the high voltage and
18 common inputs 16 and 18, respectively, of UUT 14.
19 Monitoring circuit 92 enables the actual waveform that is
20 inputted into the UUT 14 to be monitored and evaluated to
21 ensure that the waveform inputted into the UUT 14 is the
22 proper waveform for the particular test being conducted. If
23 after reviewing the waveform with monitoring circuit 92,
24 switch 90 can be adjusted to provide a different resulting
25 capacitance between nodes 64 and 66.

1 In order to conduct the high-to-ground test, switch 50
2 is adjusted so that each pair of switch contacts shown in
3 each row of Table III are electrically connected together.

4

5

Table III

SW1-11	SW1-13
SW1-21	SW1-23
SW1-31	SW1-33
SW1-51	SW1-53 (open circuit)
SW1-41	SW1-43
SW1-81	SW1-83

6 For example, switch contact SW1-11 and SW1-13 are connected
7 together, switch contacts SW1-51 and SW1-53 are connected
8 together, and switch contacts SW1-81 and SW1-83 are
9 connected together. As a result of each pair of switch
10 contacts in each row of Table III being connected together.
11 As a result of the pairs of switch contacts shown above
12 being connected together, the VSG high voltage input 48 is
13 connected to one end of resistor R1. The other end of
14 series resistor R1 is connected to high voltage output 44
15 via switch contacts SW1-31 and SW1-33. The high voltage
16 input 38 is connected directly to high voltage output 44 via
17 switch contacts SW1-13 and SW1-11. VSG common input 49 is
18 connected to node 64. Node 66 is connected to ground input
19 42 via switch contacts SW1-81 and SW1-83. The common input

1 40 is connected to node 60 via switch contacts SW1-41 and
2 SW-43.

3 Next, switch 90 is configured to exhibit the desired
4 resulting capacitance for capacitor networks 80 and 82
5 suitable for high-to-ground test. Since switch contact SW1-
6 41 is connected to SW1-43, which is connected to common
7 input 40, and switch contacts SW1-81 and SW1-83 are
8 connected together, the resulting capacitance of capacitor
9 network 82 is connected between common input 40 and ground
10 input 42, and the resulting capacitance of capacitor network
11 80 is connected between VSG common input 49 and ground input
12 42. Next, the VSG 12 is activated to output a voltage spike
13 into high voltage and common inputs 48 and 49, respectively.
14 The resulting capacitances exhibited by capacitor networks
15 80 and 82 transform the voltage spike generated by VSG 12
16 into a particular voltage spike waveform having a particular
17 waveform characteristics. The setting of switch 50 causes
18 this particular voltage spike waveform to be applied to high
19 voltage output 44 and ground output 47. As a result, the
20 waveform is applied to high voltage and ground inputs 16 and
21 input 20, respectively, of UUT 14.

22 Monitoring circuit 92 allows for the waveform that is
23 inputted into the UUT 14 to be monitored and evaluated to
24 ensure that the waveform inputted into the UUT 14 is the
25 proper waveform for the particular test being conducted.

1 In order to conduct the common-to-ground test, switch
2 50 is adjusted so that each pair of switch contacts shown in
3 each row of Table IV are electrically connected together.

4

5

Table IV

SW1-11	SW1-14
SW1-21	SW1-24
SW1-31	SW1-34
SW1-51	SW1-54 (open circuit)
SW1-41	SW1-44
SW1-81	SW1-84

6 High voltage input 38 is connected to high voltage 44, the
7 VSG high voltage input 48 is connected to one end of
8 resistor R1, the other end of resistor R1 is connected to
9 common output 46 via switch contacts SW1-31 and SW1-34, and
10 node 66 is connected to ground input 42. The high voltage
11 input 38 is connected to high voltage output 44 via switch
12 contacts SW1-11 and SW1-14. The high voltage input 38 is
13 also connected to node 60 of capacitor network 60 via switch
14 contacts SW1-41 and SW-44. Thus, the resulting capacitance
15 of capacitor network 82 is connected between high voltage
16 input 38 and ground input 42, and the resulting capacitance
17 of capacitor network 80 is connected between the VSG common
18 input 49 and ground input 42. Next, switch 90 is adjusted

1 (picofarads). Test port 100 is connected to switch contact
2 SW1-61 and test port 102 is connected to the junction of
3 resistors R2 and R3. When switch 50 is configured to
4 implement the line-to-line test, switch contact SW1-61 is
5 connected to switch contact SW1-62, and switch contact SW1-
6 71 is connected to switch contact SW1-72. In turn, switch
7 contact SW1-62 is connected to high voltage output 44, and
8 switch contact SW1-72 is connected to common output 46.
9 When switch 50 is configured to implement the high-to-ground
10 test, switch contact SW1-61 is connected to switch contact
11 SW1-63, and switch contact SW1-71 is connected to switch
12 contact SW1-73. In turn, switch contact SW1-63 is connected
13 to high voltage output 44, and switch contact SW1-73 is
14 connected to node 66. When switch 50 is configured to
15 implement the common-to-ground test, switch contact SW1-61
16 is connected to switch contact SW1-64, and switch contact
17 SW1-71 is connected to switch contact SW1-74. In turn,
18 switch contact SW1-64 is connected to common output 46 and
19 switch contact SW1-74 is connected to node 66.

20 Calibrator 10 further includes outputs 104 and 106 that
21 are connected to one end of fuse 52 and one end of fuse 63,
22 respectively. Outputs 104 and 106 are used for
23 synchronization with other test equipment.

1 In one embodiment, each switch 50 and 90 is configured
2 as a seven deck rotary switch. However, suitable switches
3 can be used as well.

4 The present invention allows for one test set up for
5 all required test conditions while UUT 14 is energized. The
6 present invention also allows for the changing of test
7 instrumentation while UUT 14 is energized. The present
8 invention allows for variation of the phase in which the
9 voltage spike is induced. This phase variation can be
10 performed while UUT 14 is energized. It is not necessary to
11 de-energize, rewire circuitry, and then re-energize UUT 14
12 in order to adjust the phase in which the voltage spike is
13 induced.

14 The present invention provides a technique for testing
15 the compatibility and survivability of electrical devices
16 which is relatively more safe and efficient than prior art
17 techniques. Furthermore, the present invention minimizes
18 test set-up and reconfiguration time. Additionally,
19 calibrator 10 can be realized inexpensively with
20 commercially available electrical components.

21 Another important feature of the present invention is
22 that calibrator 10 is portable and can be easily transported
23 and integrated with the other devices and test equipment.

24 The principals, preferred embodiments and modes of
25 operation of the present invention have been described in

1 the foregoing specification. The invention which is
2 intended to be protected herein should not, however, be
3 construed as limited to the particular forms disclosed, as
4 these are to be regarded as illustrative rather than
5 restrictive. Variations in changes may be made by those
6 skilled in the art without departing from the spirit of the
7 invention. Accordingly, the foregoing detailed description
8 should be considered exemplary in nature and not limited to
9 the scope and spirit of the invention as set forth in the
10 attached claims.

1 Attorney Docket No. 83343

2

3 APPARATUS AND METHOD FOR CALIBRATING VOLTAGE SPIKE WAVEFORMS

4

5 ABSTRACT OF THE DISCLOSURE

6 An apparatus and method for calibrating single phase voltage
7 spikes used in testing single phase electrical equipment.
8 Capacitance is selected from a capacitor network in order to
9 adjust the single phase voltage spike so as to produce a
10 predetermined voltage spike waveform having particular waveform
11 characteristics that are required to perform survivability and
12 compatibility tests.

Fig. 1

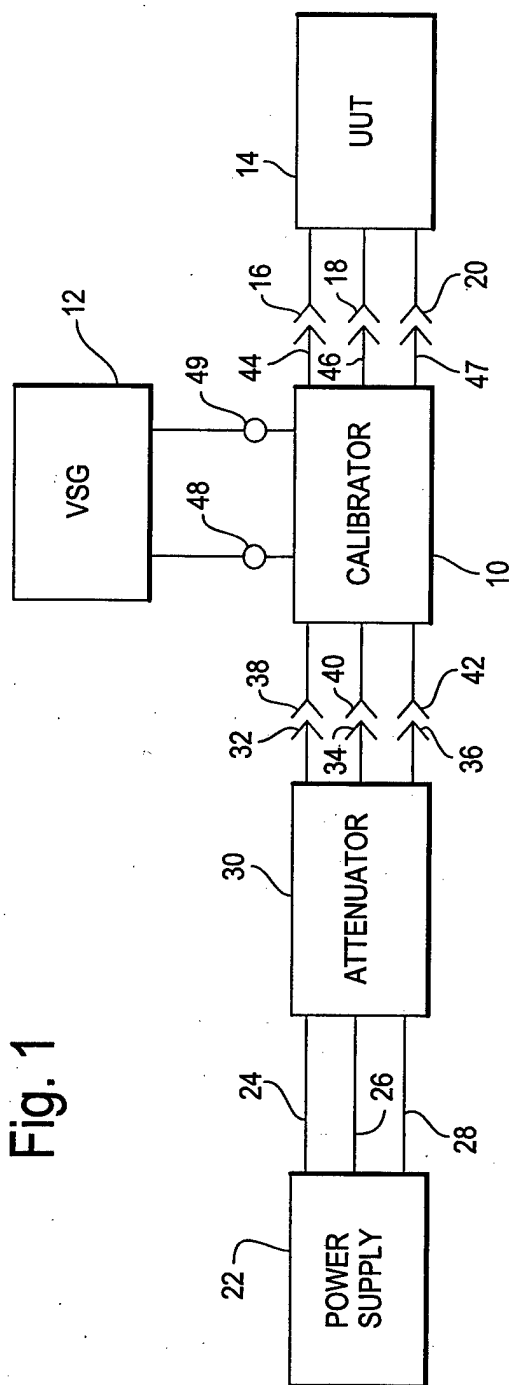
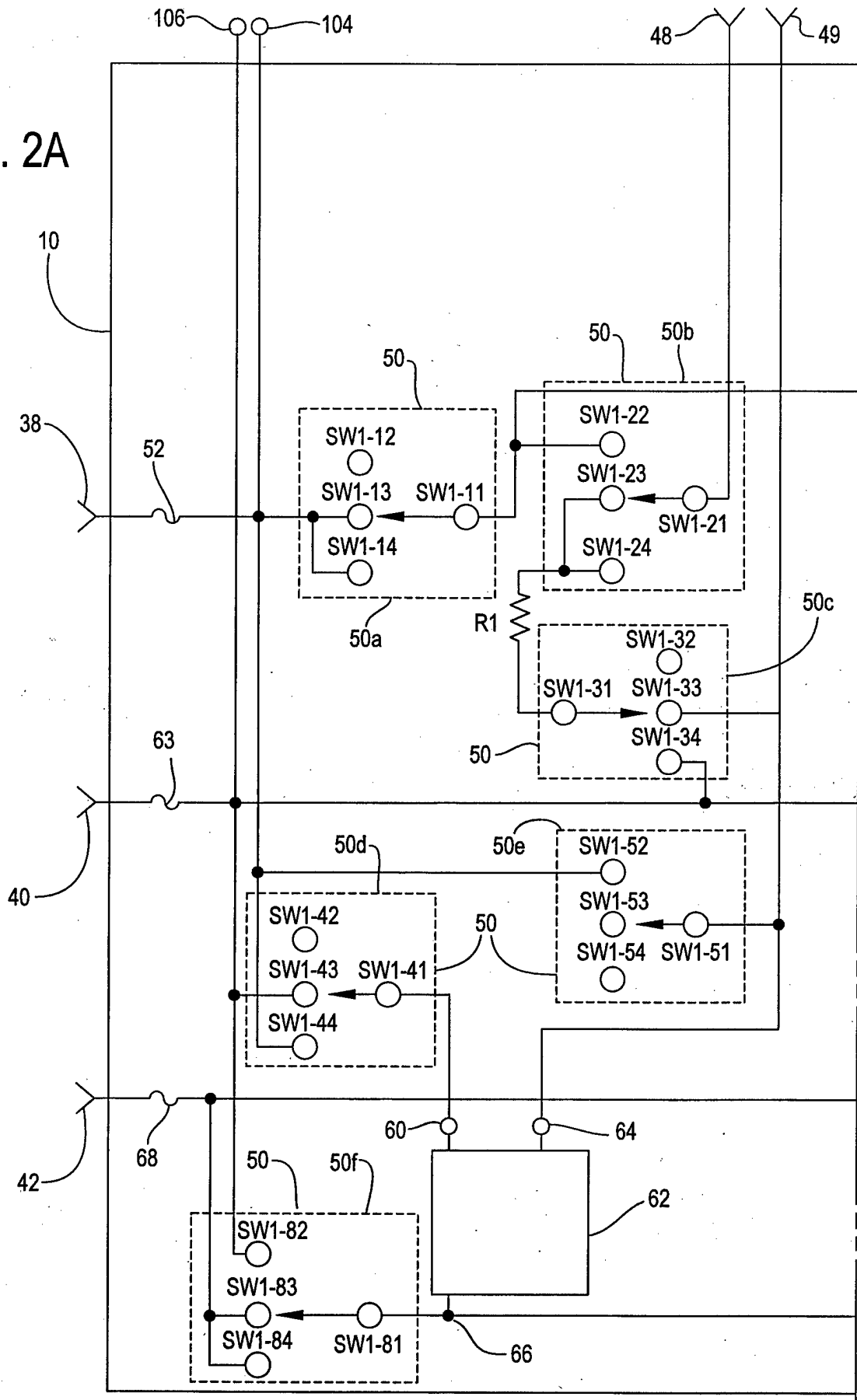


Fig. 2A



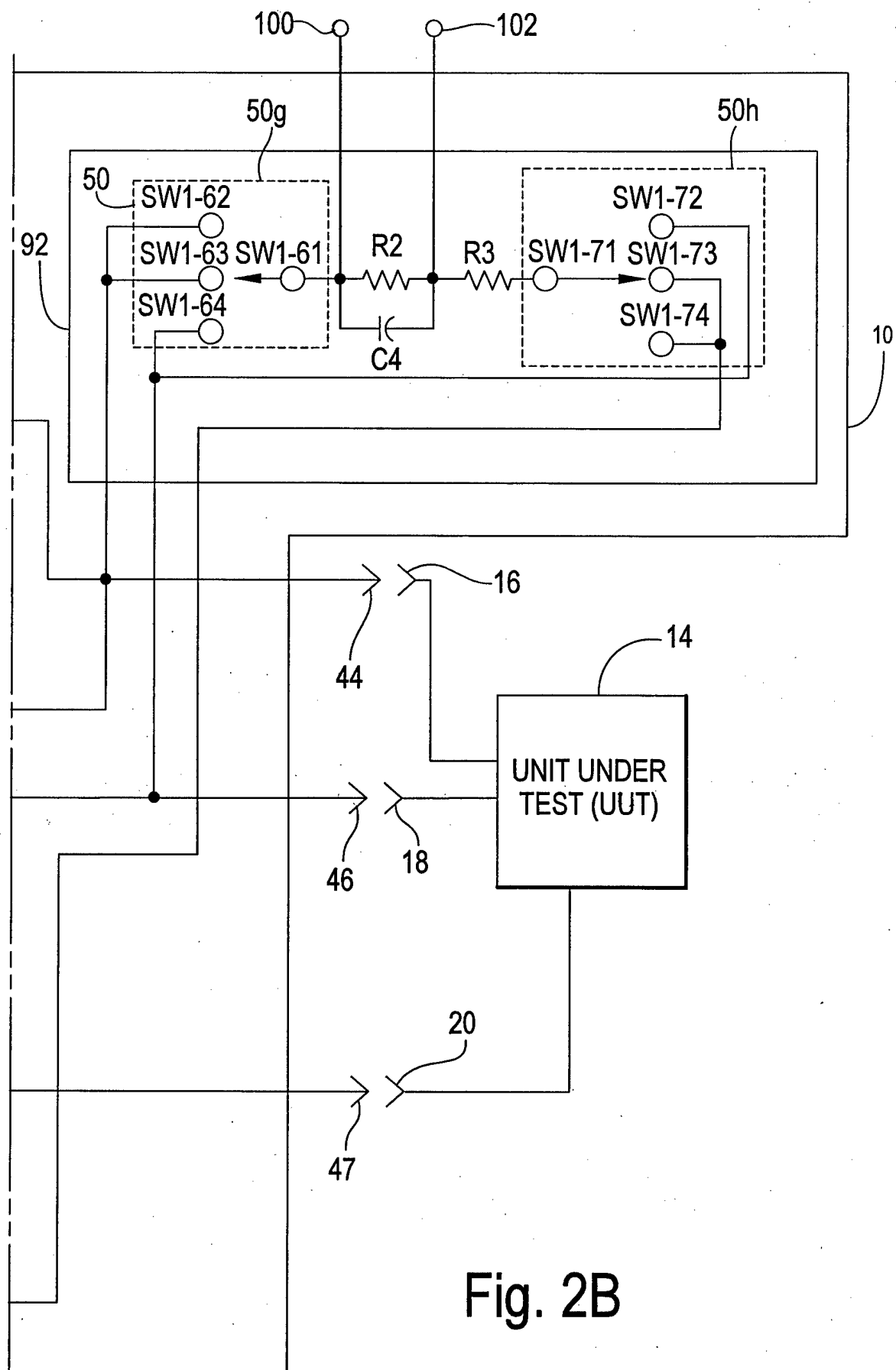


Fig. 2B

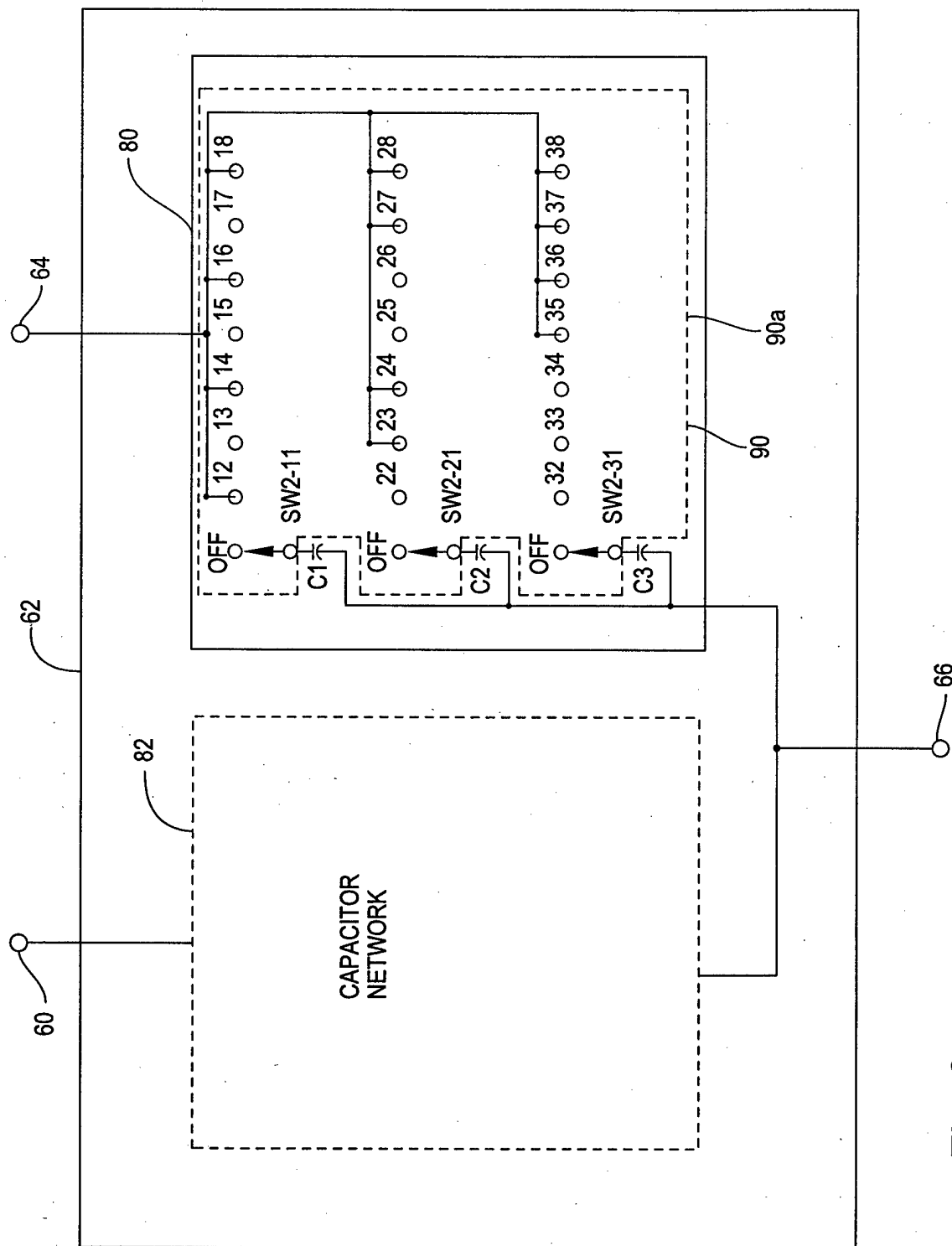


Fig. 3