

Serial No.: 09/606,098

Filing Date: 26 JUNE 2000

Inventor: PAUL BIERNACKI

NOTICE

The above identified patent application is available for licensing.
Requests for information should be addressed to:

ASSOCIATE COUNSEL (PATENTS)
CODE 1008.2
NAVAL RESEARCH LABORATORY
WASHINGTON DC 20375

DISTRIBUTION STATEMENT A
Approved for Public Release
Distribution Unlimited

DTIC QUALITY INSPECTED 3

20010110 006

CONTROL CIRCUIT, AND SYSTEM USING SAME

Background

The increasing speed with which electro-optical devices can operate has created the need for correspondingly fast devices to control them. A notable example are wavelength tunable, single-mode, semiconductor lasers, which are key components in the rapidly expanding field of fiber optics, the applications of which include wavelength division multiplexing based communication systems, measurement applications, sensor applications, and sophisticated optically controlled microwave systems. An intense effort has been devoted to optimizing and manufacturing such tunable lasers, but the predictability and performance of such lasers, as well as that of the circuit drivers needed for them, have not been explored carefully. An important example of such a laser is the tunable super structure grating distributed Bragg reflector laser, whose tremendous speed in switching from one output wavelength to another offers the scope for applications which the optics community is only beginning to explore. However, to operate a super structure grating distributed Bragg reflector laser, one needs external circuitry to separately generate four control currents, the so-

called front and back currents which control the effective cavity size of the laser, a phase section to control the phase of the laser's optical field, and the laser's gain current, which turns the laser on and controls its output power. To exploit the promise of this laser, one needs circuitry that can generate these currents with speed comparable to the laser itself, circuitry that can generate these currents accurately to ensure precise wavelength control, and circuitry that is re-programable, to permit updating circuit information as the operating parameters of the laser vary over time.

Summary of the Invention

Accordingly, it is an object of the invention to provide a circuit which can output highly accurate and precise signals.

Another object is to provide a circuit which is very fast, and thus can controllably switch between preselected outputs rapidly.

Another object is to provide such a circuit whose output parameters are continuously updatable.

Another object is to provide a laser system whose output wavelength is controlled by such a fast, accurate, and re-programmable control circuit.

In accordance with these and other objects made apparent hereinafter, the invention concerns a signal generator, having a data input, and a buffer which has a digital storage device which can store a plurality of digital words in a corresponding plurality of storage addresses. The data input and the buffer are co-operatively disposed to permit the data input to selectably address one or more of the plurality of storage addresses so as to cause the buffer to output one or more selected digital words.

Because the circuit is digital, its output, unlike that of an analog circuit, has fixed values, and hence is inherently more immune to noise. Furthermore, its accuracy is an arbitrary choice determined by the bit resolution one selects. Being digital, the outputs of the circuit are updatable simply by reading new values into the digital storage device, e.g. new settings corresponding to the drive currents for a laser whose operating parameters have drifted over time. Finally, being digital, the response of such a circuit can be extremely fast, and, moreover, computer controllable.

These and other objects are further understood from the following detailed description of particular embodiments of the invention. It is understood, however, that the invention is capable of extended application beyond the precise details of these embodiments. Changes and modifications can be made to the

embodiments that do not affect the spirit of the invention, nor exceed its scope, as expressed in the appended claims. The embodiments are described with particular reference to the accompanying drawing, wherein:

Brief Description of the Drawing

Figure 1 is a circuit diagram of a system according to the invention.

Detailed Description

Figure 1 shows a circuit device according to the invention, in which data input 10, data converter and conditioner 12 (hereafter, data converter), buffer 14, and digital to analog current driver 19, ultimately produce control currents which tune the output wavelength of laser 18. EEPROM 28 in buffer 14 contains a plurality of digital addresses, in which are stored a plurality of digital values, each value corresponding to the magnitude of a control signal for output to laser 18. Data converter 10, for example a process computer or manual control panel, is disposed to forward a digital word 13 to data input device 20. Two bits of digital word 13 are called respectively a latch bit 15 and a jump bit 17, for reasons discussed below. The remaining bits of digital word 13 contain information (hereafter

called the "address data" of word 13) coded to identify an address in EEPROM 28 in which resides a desired control signal for laser 18. Upon receipt of digital word 13 from data input 10, device 20 passes word 13 to differential receiver 22. Word 13 is coded with an address in EEPROM 28, a latch bit, and a jump bit.

Receiver 22 is preferably an interface which converts input from data input 10 from differential logic to TTL, or other conventional, logic, or other which permits use of particularly fast digital devices based on TTL. Members 10 and 20 preferably use differential logic, which is more resistant to noise, permitting members 10 and 20 to be remotely located from generator 12 and buffer 14, and still minimize the amount of noise to which the circuit is exposed. Upon data input 20 forwarding latch bit 15 to differential receiver 22 forwards the address data of word 13 to flop-flop 24, and, thereafter, upon receiving jump bit 17, forwards an enabling pulse to one-shot multivibrator 32, causing it to generate a responsive clock pulse 17'.

Flip flop 26 is disposed to receive the address data of digital word 13 from flip flop 24 and pass the address data in word 13 to EEPROM 28, both EEPROM 28 and flip-flop 26 being clocked along line 32' by one-shot multivibrator 32. Enablement

of EEPROM 28 causes EEPROM 28 to receive the address data of word 13 from flip flop 26, and to make available to buffer driver 30 the digital signal stored in EEPROM 28 at the address corresponding to the address data of digital word 13.

Multivibrator 32, responsive to enablement of jump pulse 17', drives inverter 34 which in turn sends a disable signal to driver 30. Because of inverter 34, driver 30 is disabled when jump bit 17 is enabled, and re-enabled when jump bit 17 reverses.

The digital portion of the circuit of figure 1, members 12 and 14 (or, depending on one's particular application, members 20 or 10 also), are preferably placed closely packed on one circuit board, with a common ground plane isolated from the non-digital portion of the circuit, namely member 38, 18, etc., to increase circuit reliability and increase circuit speed by minimizing the distances over which its signals must travel.

In operation, member 10 sends word 13 to device 20, which automatically forwards the address data of word 13 to differential receiver 22, along with by latch bit 15 and then jump bit 17. If the value of latch 15 is enabling, the address data of word 13 is forwarded after a short delay to flip flop 24. Similarly, if the value of jump bit 17 is enabling, differential receiver 22 strobes one-shot multivibrator 32, which clocks the

address data from flip flop 24 to flip flop 26 and enables EEPROM 28. Upon enablement, EEPROM 28 receives word 13 from flip flop 26, locates the digital control signal at the address corresponding to the address data in digital word 13, and makes the control signal available to driver 30. Simultaneously, multivibrator 32 and inverter 34 disable driver 30, until multivibrator 32's one-shot pulse has finished, whereupon driver 30 becomes enabled and receives the control signal from EEPROM 28, and forwards the signal to digital to analog converter 36, and ultimately to laser 18. By maintaining driver 30 disabled for a short time, the output to digital to analog converter 18 is nulled for a short time, and thus the control signal to laser 18 is nulled also. This is advantageous to prevent hysteresis effects in laser 18 from causing a corresponding hysteresis in laser 18's wavelength as members 12 and 14 switch laser 18 from one output mode to another.

Digital to analog converter 36 converts the digital output of driver 30 into analog form, which in turn controls current driver 38, producing a control current for laser 18. Converter 36 is typically a voltage source, and current source driver 38 converts the voltage output of converter 19 to a current signal. Laser 18 requires three such current signals plus a current

driver for the gain section, as illustrated by lines 40, 42, 44 and 46. In practice, each of these signals would be produced by three separate circuits of the kind shown in figure 1 as comprising members 12, 14, 36, 38. Preferably, however, there would only be one digital word 13, whose address data would be interpretable by each of the three circuits to data input launching of the correct digital output signal from each. This means that in practice there would be one member 10 and one member 20, which would forward digital word 13 in parallel to each of the three circuits. Laser 18 also may have a conventional cooling circuit 45 to stabilize laser 18 and minimize wavelength drift.

Because the circuit of figure 1 employs digital components, particularly those based on TTL logic, and is placed on one circuit board with the digital components closely packed, the circuit is inherently very fast, and thus can switch control signals to laser 18 very quickly. Because the output of buffer 14 is a digital signal, rather than an analog signal, current output is inherently very stable, making the signals in member 36, 38, etc. similarly stable. This permits one to dispense with complicated and inherently slow phase locked loops which may be used to keep a corresponding analog control system within

tolerances. One could, for example, use for driver 38 a straightforward operational amplifier driving a high current capacity transistor, a textbook scheme which is both inexpensive and inherently quick.

The precision of the output from member 19 is limited only by the number of bits employed in EEPROM 28, and hence can be made as precise as one's application demands within currently available technology. Because address 13 is clocked sequentially across generator 12 and buffer 14, interstage noise such as one would associate with an analog system is minimized. Such noise as is present, most notably ringing as circuit components are switched, is further minimizable by making the response time of downstream components in the circuit longer than the ringing time of upstream components, by proper grounding of the circuit, and by proper isolation of the digital portion of the circuit of figure 1, from the analog portion. In this manner, the circuit of figure 1 provides an output signal that is precise, fast, and robust against noise. Furthermore, because the output signals are stored as digital words in EEPROM 38, one can readily recalibrate the system as laser 18's operating parameters change by simply reading new values into EEPROM 28. These new values would typically come from calibration trials on laser 18, in which one

Serial No. (Unassigned)
Applicants: Biernacki et al.

Patents
Attorney Docket No. 80,252

tests the laser to determine which sets of drive currents produce which laser modes. Having done this, one simply digitizes the critical values of drive current and reads them into EEPROM 28.

The invention has been described in what is considered to be the most practical and preferred embodiments. It is recognized, however, that obvious modifications to these embodiments may occur to those with skill in this art. Accordingly, the scope of the invention is to be discerned from reference to the appended claims, wherein:

Serial No. (Unassigned)
Applicants: Biernacki et al.

Patents
Attorney Docket No. 80,252

Abstract of the Disclosure

A circuit for selectably generating a plurality of preselected digital output signals which are precise and accurate, and among which the circuit can switch rapidly. In one embodiment, the outputs are connected to analog circuit signals, and drive a optical laser such that choice of the particular outputs of the circuit permits controllable switching of the laser output wavelength.

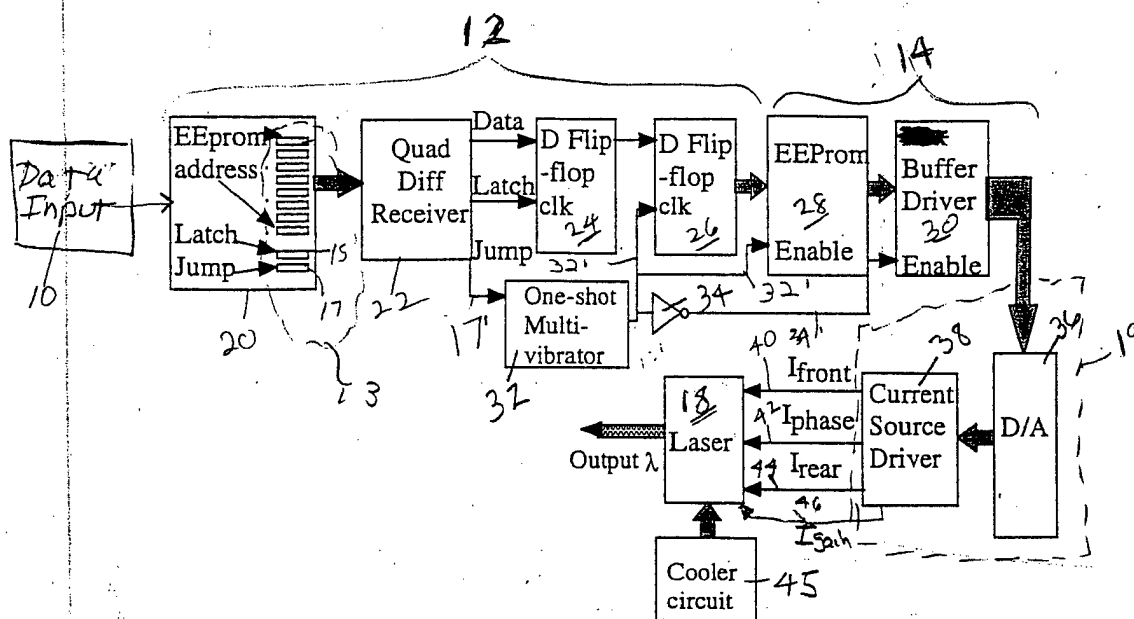


Figure ...!