PL-TR-96-1082

OPTICAL INPUT/OUTPUT (I/O) "PINS" AND "PIN" GRID ARRAYS FOR MULTICHIP MODULE (MCM) INTER-LAYER AND EXTERNAL CONNECTIVITY

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14. Abstract The increased complexity of electronic circuits and reduced component sizes has resulted in large numbers of Input/Output (I/O) interconnections for each module layer. However, the number of electrical interconnects that can be placed at module layer edges is limited. In addition, electrical interconnects are sensitive to external electromagnetic interference and interchannel electrical cross talk. In response to these issues, Physical Optics Corporation (POC) evaluated a new optical I/O "pin" and "pin" grid array concept for two-dimensional interlayer interconnects and system I/O. POC's concept is based on commercially available fibers, optical lenses, vertical cavity surface emitting lasers, and highly sensitive photodiode arrays. The advantages of the optical "pin" concept include high data rate I/O (>GHz speeds), low loss, low signal propagation delay, high immunity to Electromagnetic Interference (EMI), low cross talk at high speeds, high "pin" count (200/cm² to 2500/cm²), and low cost.

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EXECUTIVE SUMMARY

In this program entitled, "Optical I/O "pins" and "pin" grid arrays for MCM inter-layer and external connectivity," POC investigated a novel optical "pin" concept to enhance current developments in optical interconnection technology. The uniqueness of this "optical I/O pin" concept is the use of currently existing vertical cavity surface emitting lasers (VCSEL) and commercially available granded index lens. This provides a high speed, flexible, and low cost optical I/O pin and pin array for future MCM inter-layer and inter-board connections.

POC expects that the proposed optical "pin" approach will provide a standard modularized optical interconnection architecture for both military and commercial applications.

During this Phase I investigation, POC first studied the fast developing VCSEL technology, searched for and purchased the needed VCSELs sources, and finally developed a testbed demonstration and designed the driving circuits for the VCSELs used. Based on these studies, two types of I/O "pin" architectures were investigated. The first one used the VCSEL and GRIN lens combination: by properly selecting the GRIN lenses, a versatile board-to-board optical interconnection architecture was fabricated. The second one used a VCSEL-and-lensed fiber combination. POC's property fiber lensing technology was employed in this effort. Using this approach, a relatively cheap, flexible, and single optical layer to layer "pin" type interconnection module was demonstrated.

Based on the above work, POC has recognized the real potential of the "optical pin" architecture, and our recommendations for future development of this technology are provided in this report.

1.0 INTRODUCTION

The increased complexity of electronic circuits and reduced component sizes has resulted in large numbers of input/output (I/O) interconnections for each module layer. However, the number of electrical interconnects that can be placed at module layer edges is limited. In addition, electrical interconnects are sensitive to external electromagnetic interference and inter-channel electrical crosstalk. In response to these issues, Physical Optics Corporation (POC) evaluated a new optical input/output "pin" and "pin" grid array concept for two-dimensional inter-layer interconnects and system I/O. POC's concept is based on commercially available fibers, optical lenses, vertical cavity surface emitting lasers, and highly sensitive photodiode arrays. The advantages of the optical "pin" concept include high data rate input/output (> GHz speeds), low loss, low signal propagation delay, high immunity to EMI, low crosstalk at high speeds, high "pin" count (200/cm^2 to 2500/cm^2), and low cost.

On-going research and development efforts in very large scale integrated (VLSI) circuits and multichip module (MCM) packaging have led to a dramatic increase in the operating speed of compact packaged systems, increased system reliability, and reduced power consumption. As electronic circuits become more complex and physical component size becomes smaller, the number of input/output (I/O) ports and the density of the I/O between each module layer becomes very large. Since the distance between adjacent module layers is set by heat dissipation requirements, the interconnect distance is generally not small (> 4 mm). Thus, electrical interconnects based on a large number of physically connected wires or coaxial wires becomes impractical, and the system's performance is limited by electromagnetic interference (EMI) because of the long interconnect distance among these electronic interconnect paths. Furthermore, the electrical interconnects require the I/O ports be placed at the side of the module layer. Obviously, there is a limit to the number of I/O ports, and this becomes restrictive to signal distribution on each layer. There are also other drawbacks of electrical interconnects, including ohmic power losses, long delay times, and complex physical wiring.

1.1 Proposed Technology Development

To overcome the limitations outlined above, Physical Optics Corporation (POC) proposed a new optical input/output "pin" architecture for packaged high speed MCM systems. As shown in Figure 1-1, all electrical input/output pins or pin grid arrays are replaced by fiber optical I/O "pins." With these "pins" and "pin" grid arrays, inter-layer optical interconnects can be accomplished at any point within the modules, rather than being limited to the optical path side of the module layer. There is also a significant increase in I/O density (up to 2500/cm^2), since each pin can be as small as 100 μm to 200 μm in diameter; the density of the other components can be even smaller than this. The advantages of optical interconnects include high data rate signal transmission, data rates independent of the interconnect distance for multi-layer applications, large fanout density, low clock skew, reduced power consumption at high speed, and reduced sensitivity to EMI. These excellent features make optical interconnections particularly suitable for high speed packaging of MCMs and for the construction of optical "pins" and "pin" grid arrays for inter-layer interconnects and system I/O.

Vertical-cavity surface emitting lasers (VCSELs), which have a high-speed modulation capability, can be employed inside a hermetically packaged MCM (Figure 1-2) for electrical-to-optical signal conversion. Commercially available graded refractive index (GRIN) lenses

can effectively collect the diverging optical signal beams from the VCSELs and provide guided beam outputs for routing signals between several different MCM layers. High speed photodetectors with preamplifiers can be used to convert the received and guided optical signals to electrical formats. The entire structure uses only optical type input/output "pins" or "pin" grid arrays. It can also facilitate external connections between several different hermetically sealed MCM modules through an optical backplane (see Figure 1-3). The speed of the system is not limited by optics, but rather by the speed of the VCSELs and photodetector receivers. Therefore, the speed of each interconnect link can be several GHz, based on available commercial VCSELs and photodetector receivers. Over 10 GHz is possible in the near future. The present speed is already compatible with existing MCM systems. Since all of the required components are commercially available, near-term technological maturity for dual-use commercial applications is possible.

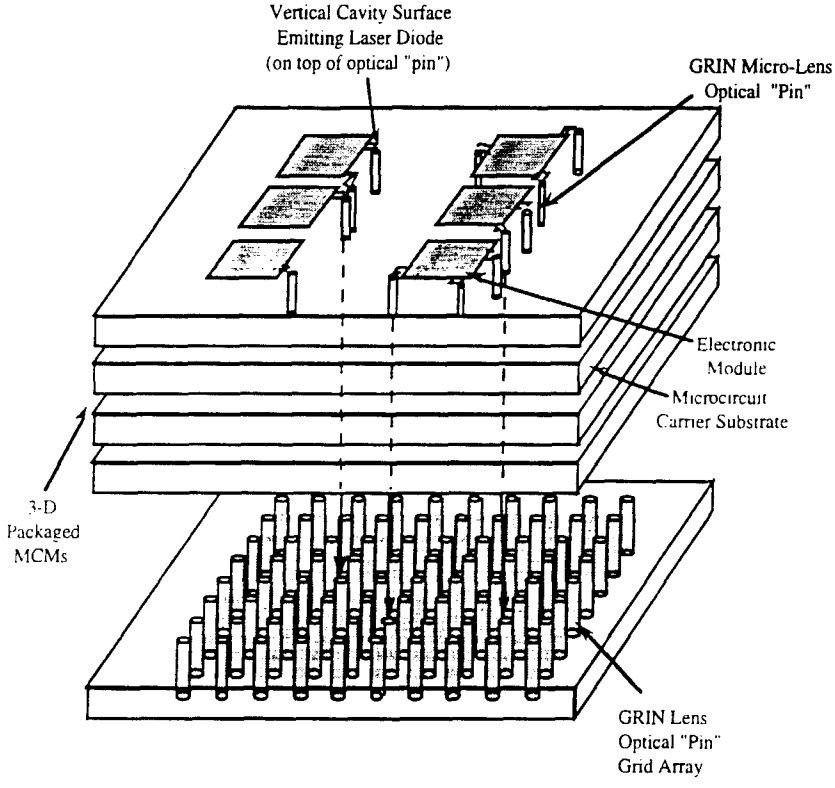


Figure 1-1 All optical input/output "pins" and "pin" grid array arrangement for compact packaged MCMs using high-speed vertical cavity surface emitting lasers, GRIN lenses, and photodetectors.

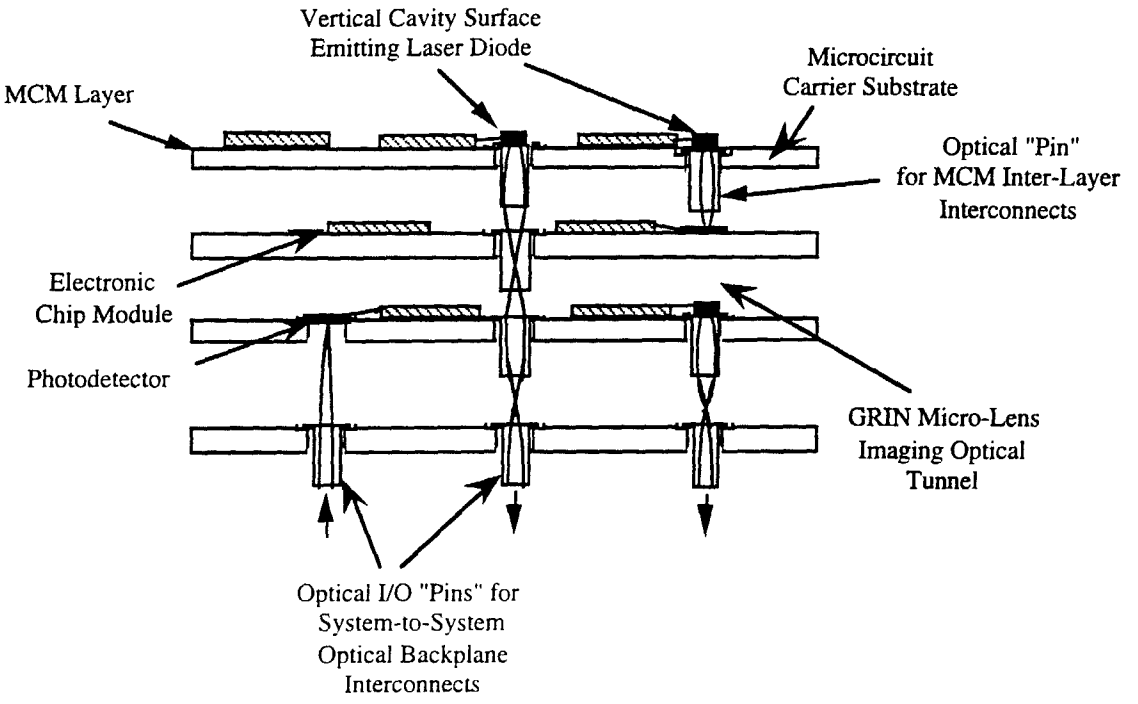


Figure 1-2 Schematic of optical interconnect structure inside the MCM package.

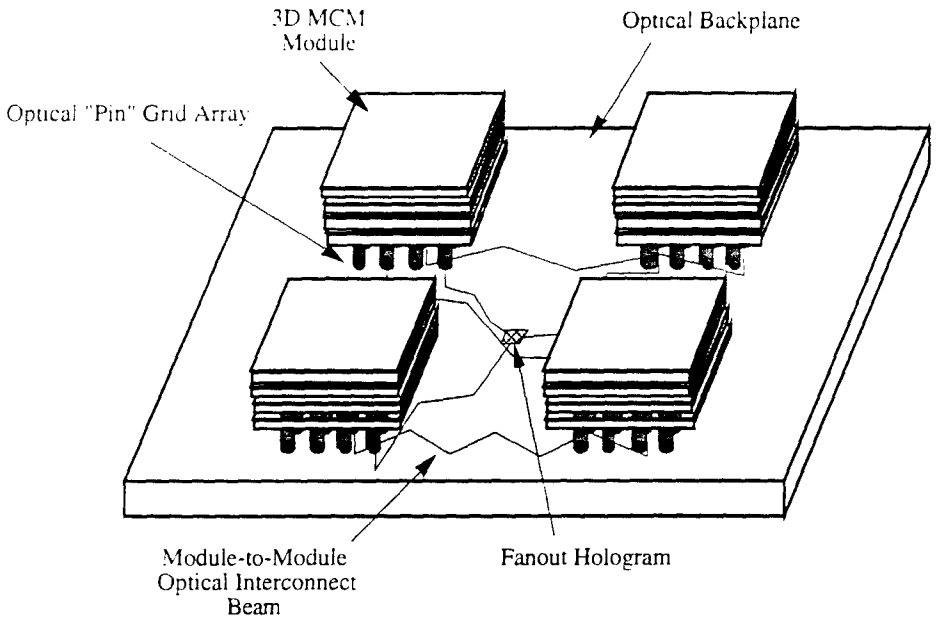


Figure 1-3 Module-to-module external interconnects using the "pin" grid arrays and an optical backplane.

1.2 Innovativeness of the Proposed Program

This optical I/O "pins" and "pin" grid array concept, when put into a practical application, will lead to a new generation of board-to-board interconnection structures, and will provide a "drop-in" type of standard chip for layer-to-layer interconnection. Unlike conventional electronical I/O pins and pin grids, which are always distributed around the side of a board on chips, the proposed optical I/O "pins" and "pin" grids array can be placed anywhere on the board, and can provide interconnection not only between two adjacent boards, but also any pairs of non-adjacent boards. Most importantly, by taking advantage of the proposed optical "pin" concept, not only can the pin density per unit area be potentially increased, but the transfer rate of information through each pin is also greatly increased. POC's proposed optical I/O "pin" concept has the following advantages:

1. It is a new optical input/output concept using GRIN lens (or lensed fiber) optical "pins."

2. The system demonstrates high data rate (greater than several GHz) signal input/output and inter-layer interconnection based on high-speed VCSEL modulation and high-speed photodetectors. Thus, there is little optical propagation delay and low clock skew.

3. It has lower power consumption than electrical interconnects for high data rate operation. Thus, capacitive and inductive loading effects are reduced.

4. Speed and bandwidth are independent of the interconnection distance. This is not true for electrical interconnects.

5. The optical interconnects and I/O improve the system's immunity to electromagnetic interference (EMI).

6. There is low optical crosstalk. GRIN lenses (or lensed fibers) function like optical waveguides, which confine the vertical propagating signal beams inside the lensing medium. Thus, there is also little radiation and associated background noise.

7. The optical signal can be transmitted through multiple layers on boards using GRIN lens (or lensed fiber) optical imaging tunnels. Signal transmission in the optical tunnels is low loss (<0.2 dB/cm). The interface loss between the VCSEL and the GRIN lens (or lensed fibers) can be controlled to be below 0.3 dB with a good match between the numerical aperture of the GRIN lens (or lensed fiber) and the laser.

8. There is no physical contact between the "pins" on adjacent receiving MCM layers. Hence, no contact damage is caused by vibration and MCM layer replacement.

9. A high "pin" count can be achieved (over 2500/cm^2).

10. The inter-layer interconnections are not restricted to the side of each layer, in contrast to electrical interconnects. The interconnections can be located at any predesigned position.

11. The entire package is compact and rugged, and all of the device components are mature. Thus, near-term commercialization for dual-use applications is possible.

2.0 PHASE I RESULTS

The Phase I goal was to perform a feasibility study of the proposed inter-layer MCM optical interconnect structure using optical "pins" and "pin" grid arrays.

In Phase I, POC used existing technologies to prove the interface issues between the compact optical "pin" and the electrical-to-optical and optical-to-electrical components.

The following Phase I objectives were set forth:

Objective 1: Demonstrate a small scale laboratory prototype of the optical I/O "pin" structure. It will consist of GRIN lens-type optical "pins," packaging substrates and boards, VCSELs, and high-speed photodetectors with preamplifiers.

Objective 2: Provide a complete design of an optical backplane and the interface requirements between the proposed optical "pin" grid arrays and the backplane for external interconnections.

Objective 3: Demonstrate prototype performance, including signal bandwidth limitations, optical throughput efficiency, crosstalk levels, and "pin" grid density.

2.1 Study and Analysis of I/O Pin Interconnect Components

Figure 2-1 shows the schematic of the board-to-board optical interconnect.

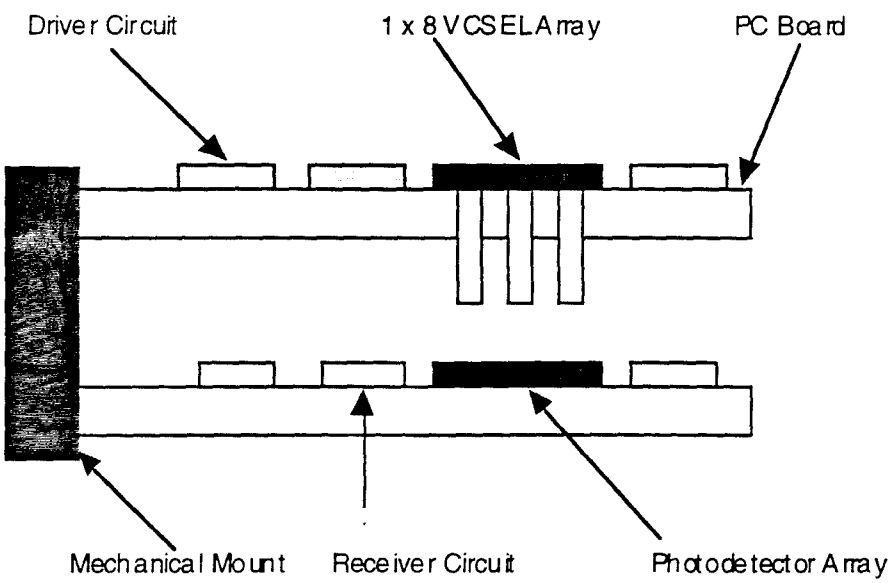


Figure 2-1 Board-to-board optical interconnect concept using optical pins.

The following components were evaluated, tested and observation noted:

- Vertical cavity surface emitting lasers (VCSEL)
- Photodetector arrays
- "pin" optical interconnect components

2.1.1 Vertical Cavity Surface Emitting Lasers (VCSEL)

Vertical cavity surface emitting lasers are low power consumption laser diodes. The driving current is typically 1 mA, while the threshold voltage is about 1.5 V. Therefore, the power dissipation is less than 2 mW. This power consumption level is much lower than other semiconductor diode lasers. Figure 2-2 shows the measured plot for voltage, current, output power, and power conversion efficiency. Clearly, the power dissipation is low, while the output optical power is high. The power conversion efficiency from electrical to optical is very high at low temperatures, and reasonably high (not shown) at room temperature. A maximum efficiency of over 25% can be achieved at room temperature. Therefore, if each laser consumes 2 mW of electrical power and emits about 500 μW of optical power, the maximum heat generated by each laser is about 1.5 mW. For interlayer optical interconnects, the required optical power is much lower than 500 μW, due to minimal losses in the lens and optical coupling (total of less than -3 dB). Thus, a power level of about 100 μW is enough for interlayer interconnect applications, and the heat generated by each VCSEL can be smaller than 1 mW. If we consider a packaging density of 100/cm^2, the total heat generated in this 1 cm^2 area is less than 100 mW. This is within the heat handling capability of multichip modules. Lower threshold VCSELs are currently in development. Future technology should allow more VCSELs to be placed in the same area, implying a high laser array packaging density.

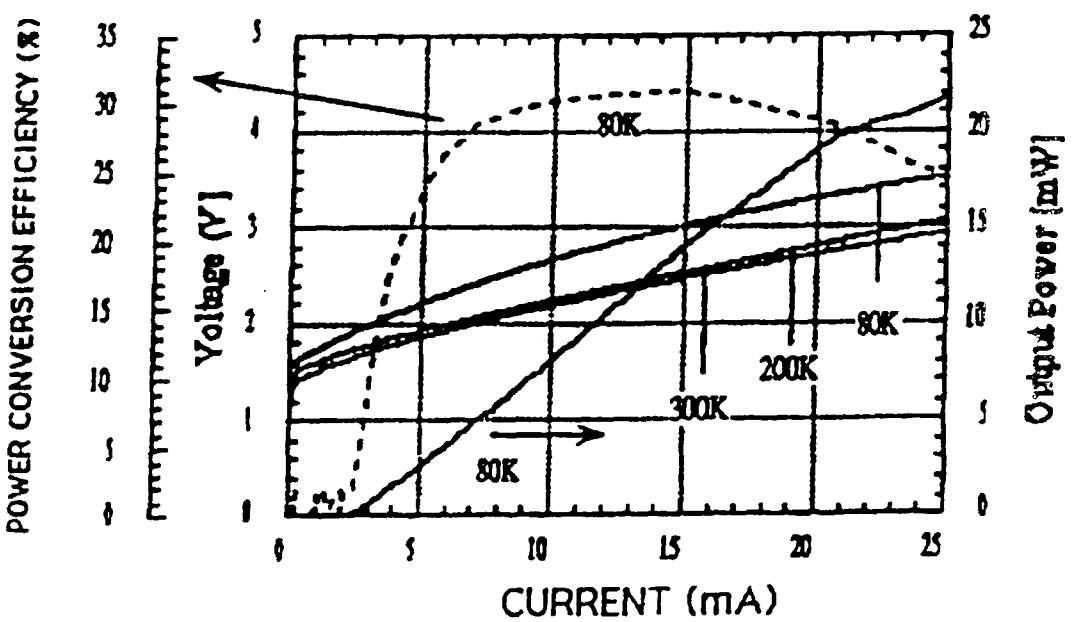


Figure 2-2 A measured VCSEL response. Low threshold voltage and driving current and high optical power output is clearly possible by the VCSEL. The electrical-to-optical power conversion efficiency is quite high.

VCSELs are key elements of the proposed optical "pin" interconnect concept. This is because of their novel properties of vertical surface light emitting. The laser light can be emitted from the VCSEL either upward or downward, depending on the laser fabrication and packaging. This is particularly suitable for our proposed vertical inter-board optical interconnects (see Figure 2-3). As described before, to ensure good optical coupling to the optical "pin," the laser's divergence angle must be smaller than the acceptance angle of the GRIN lenses. The laser divergence angle for VCSEL is typically less than 8° to 10°, while the acceptance angles of GRIN lens and lensed fiber are both larger than 20°. Thus, this requirement is satisfied.

VCSELs are available from research institutes such as the University of New Mexico and the University of California, Santa Barbara. Some aerospace corporations, such as Motorola, Honeywell, and Hewlett Packard, have the ability to make VCSELs for their own commercial uses. Until recently, no commercial company has sold VCSELs as separate components. Fortunately, VCSELs have become available from VIXEL Corp. in Colorado. The cost of a VCSEL array with two elements is about $120. The eight-element array is only about $400. With a large quantity purchase, the laser array cost can be significantly reduced. The availability of a VCSEL arrays opens up a variety of application opportunities in data communications and displays.

Figure 2-4 shows a picture of the VCSELs purchased from VIXEL Corp. The two small pieces are two-element VCSEL arrays, while the bigger center piece is an eight-element VCSEL array. The present array laser spacing is 250 μm. 125 μm spacing is also available. A custom order is needed for other specific laser pixel spacings. It is clear that high density laser packaging is possible. The overall packaging density of the optical "pin" array is limited by the heat handling capability of the MCM board.

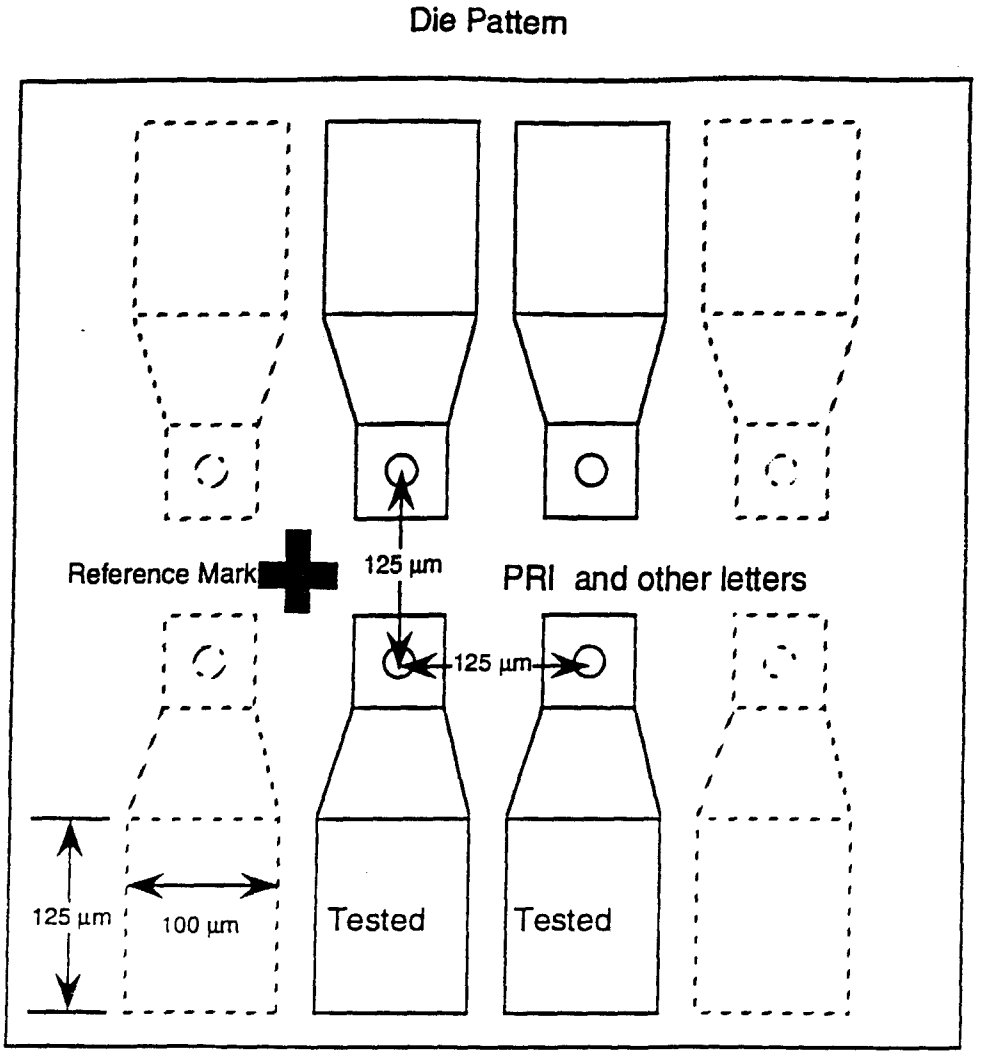


Figure 2-3 High speed (over 3 GHz) driver circuit for the VCSEL array element. Careful electrical layout is necessary to achieve high speed operation.

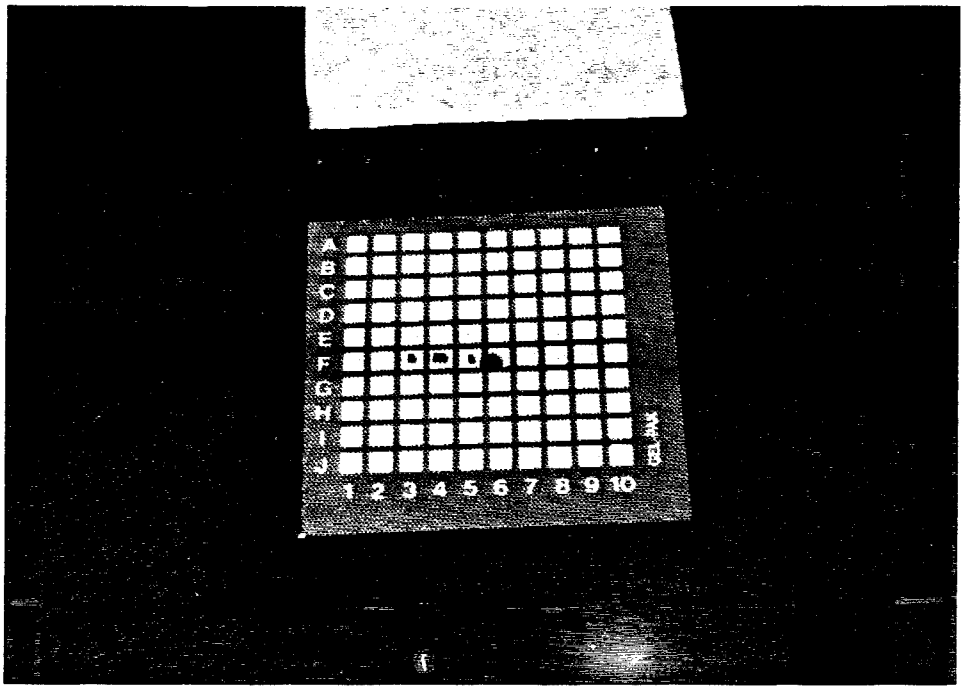


Figure 2-4 Picture of the purchased commercially available VCSEL array.

The current (I) vs. optical power (P) curve for the 1×2 and the 1×8 VCSEL arrays are given in Figures 2-5 and 2-6, respectively. The threshold current for these lasers is about 6 mA. This is reasonably good as compared to some Fabry-Perot lasers with threshold currents of about 15 mA. The maximum optical power outputs of the present lasers can be about 1 mW. Considering minimal optical loss from the optical "pin" system, the available optical power largely exceeds the requirements.

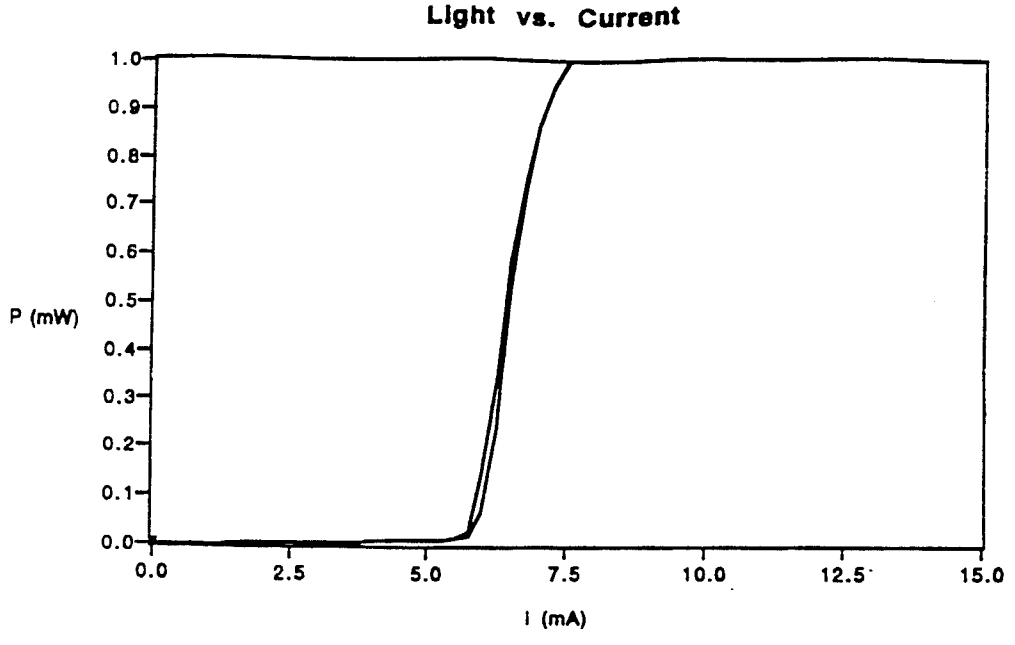


Figure 2-5 I-P curve of the 1x2 VCSEL array.

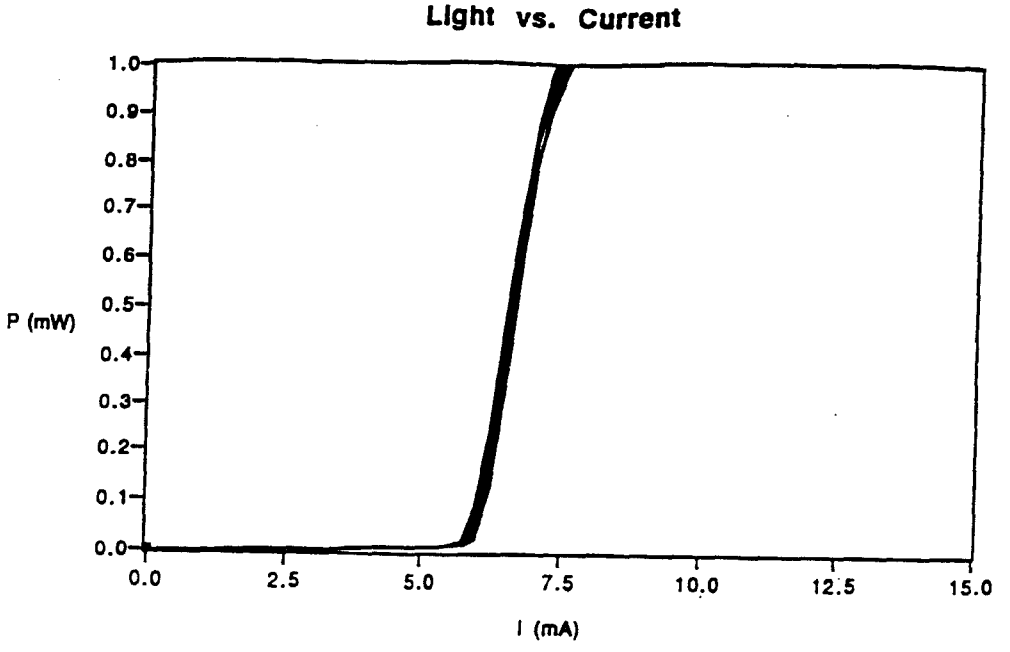


Figure 2-6 I-P curve of the 1x8 VCSEL array.

The I-V curves for the 1×2 and the 1×8 VCSEL arrays are given in Figures 2-7 and 2-8, respectively. At a threshold current of about 6 mA, the operating voltage is about 2.8 V. The electrical power consumption at the threshold operation is about 16.8 mW. As the current increases to 7 mA for normal operation, the voltage rises to about 3 V. In this case, the electrical power consumption is about 21 mW and the laser output is about 0.8 mW. The electrical-to-optical power conversion efficiency is about 3.6%. From the power conversion efficiency point of view, these VCSELs are not good enough. Improvements in VCSEL fabrication technology at VIXEL Corp. are needed. Better power conversion efficiency of about 30% has been demonstrated at the University of New Mexico.

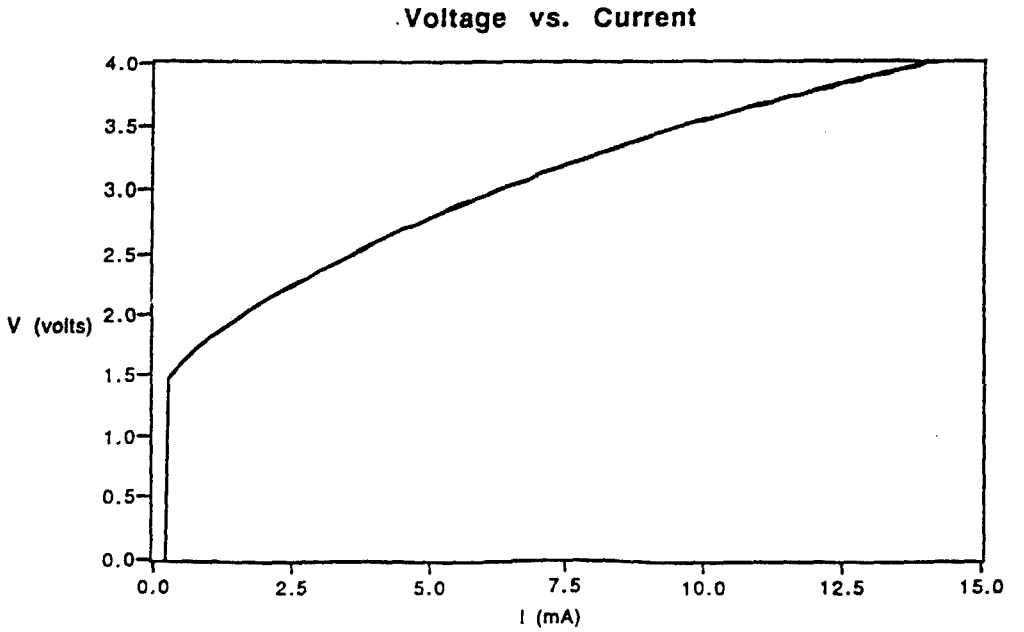


Figure 2-7 I-V curve of the 1x2 VCSEL array.

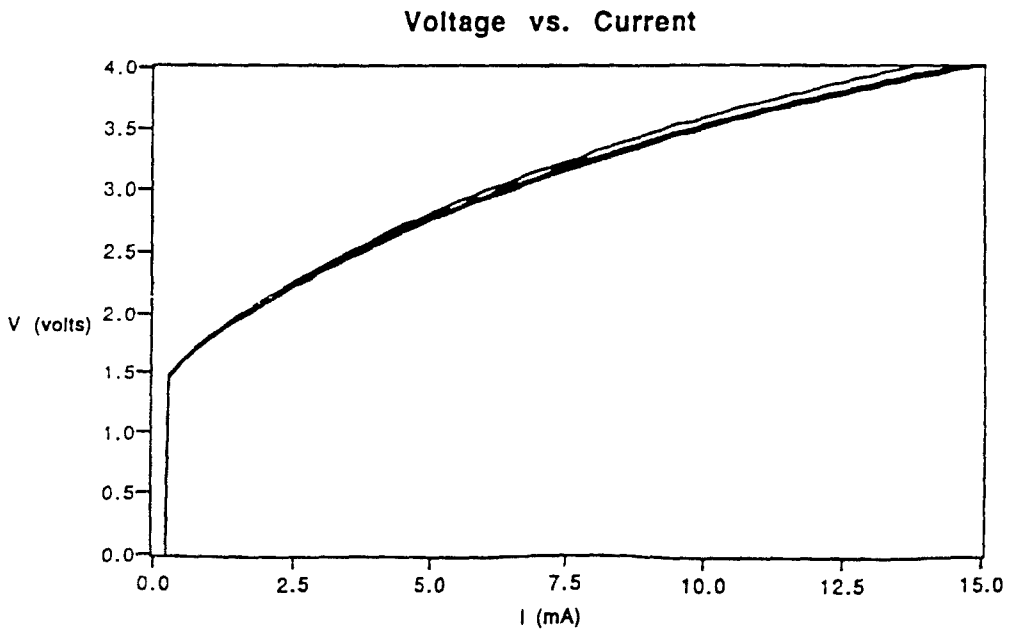


Figure 2-8 I-V curve of the 1x8 VCSEL array.

Figure 2-9 shows the packaging arrangement and wire bonding of each laser die. To drive each VCSEL element, we have designed a simple laser driving circuit (see Figure 2-10). This is a basic emitter-follower circuit design. The key feature of the circuit is the use of a high speed transistor. The input signal level is adjusted to be compatible with the emitter coupled logic (ECL) voltage levels consistent with typical MCM designs. The design and fabrication of this circuit is currently in progress. The circuit can be miniaturized using

currently available circuit design technology. This is ideal, because we would prefer to include the circuit in the chip design to form a single integrated component.

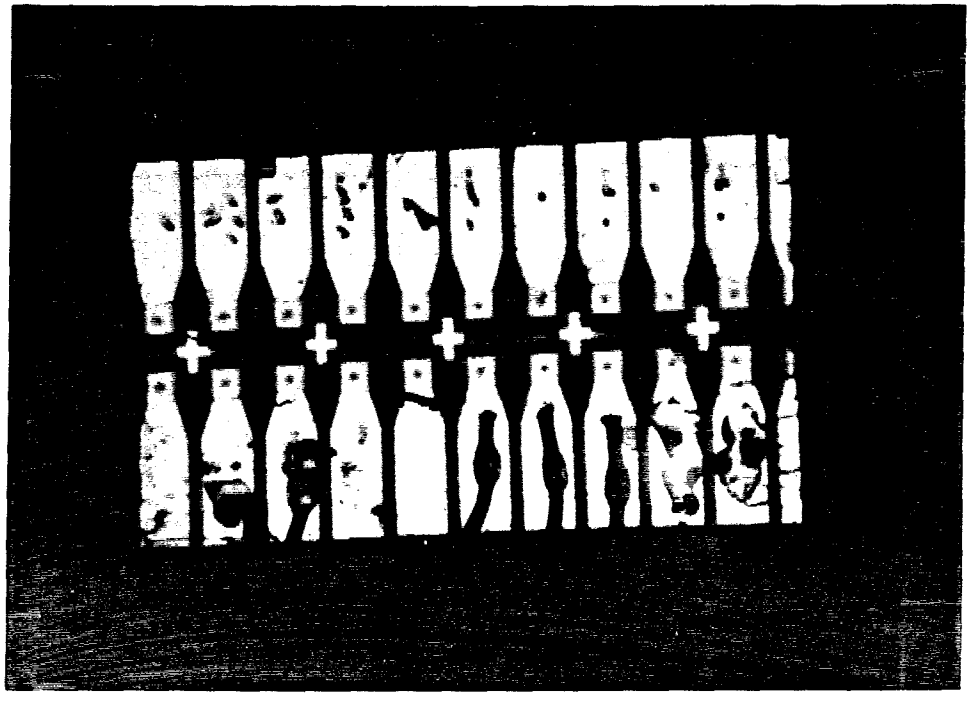


Figure 2-9 High speed (over 3 GHz) driver circuit for the VCSEL array element. Careful electrical layout is necessary to achieve high speed operation.

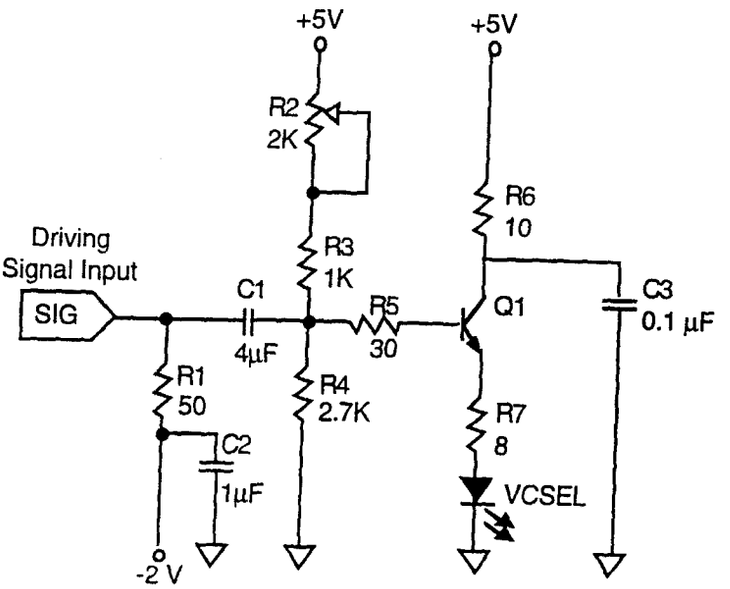
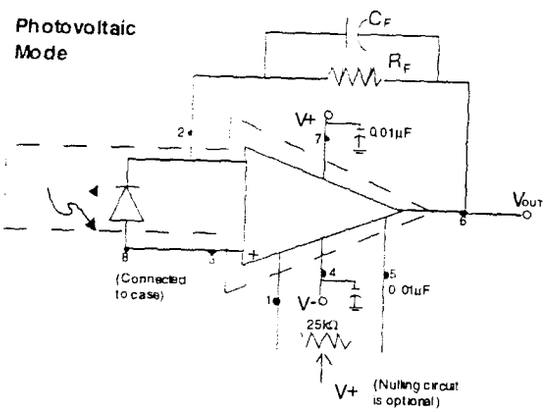


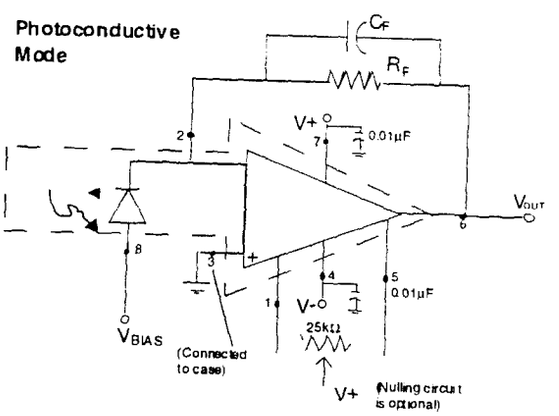
Figure 2-10 High speed driving circuit for the VCSEL.

2.1.2 Photodetector Arrays

The selected detector for the reception of the signal is a silicon array. The operating wavelength of the VCSEL is typically 760 nm - 850 nm, and silicon detectors have an optimal spectral response in that range. Furthermore, each detector in the array can be combined with a preamplifier, in a monolithic OP-AMP transimpedence amplifier configuration. Figure 2-11 shows the connections for both photovoltaic and photoconductive modes.



(a) Photovoltaic mode.



(b) Photoconductive mode.

Figure 2-11 Photodetector with OP-AMPS in a transimpedence amplifier configuration.

2.1.3 Gradient-Index (GRIN) Lens

In accordance with the program tasks, GRIN lenses (or SELFOC lenses) were first considered as the optical pin units to transfer the optical signals from the modulated VSCELs to the photodetector array.

The current development of GRIN lenses is very mature. They are widely used in optical communications, image processing, and laser optics. Because of their simplicity and maturity, they are very suitable for use as the optical pin for this investigation. The following functions can be performed using suitable GRIN lenses:

1. **Light Collimation**. The VCSEL has a small emitting area, and provides a small divergent light beam. When the output of the VCSEL directly strikes one end-face of a quarter pitch GRIN lens, a collimated light beam with a beam aperture smaller than that of the GRIN lens can be easily produced. This function can be used to transfer light information between closely positioned boards.

2. **Light Focusing**. Because the effective area of the photodetector is also small (under 100 μm^2), the collimated light from one board can be completely focused into the detector's effective area.

3. **Point-to-Point Light Connection**. By controlling the length of the GRIN lens, the optical information from VCSEL in one board can be directly focused to the detector in the other board without using a receiving lens. This function can be considered for pin interconnection between two boards with a standard separation distance.

4. **Light Relay**. In certain applications, optical I/O pin interconnection is demanded between two boards which are separated from one another by one or two boards. In this case, one or two specially selected GRIN lenses can be positioned on these intermediate boards to act as relaying I/O pins. In this way, the divergence of the light beams can be always controlled within a range which is tolerated by the required I/O pin density.

By combining the above functions, optical "pin" I/O interconnection can be realized between two boards with irregular distances. By properly selecting and utilizing the above four GRIN lens functions, the required optical I/O "pins" and "pin" grid arrays for board-to-board interconnections can be realized as shown in Figure 2-12.

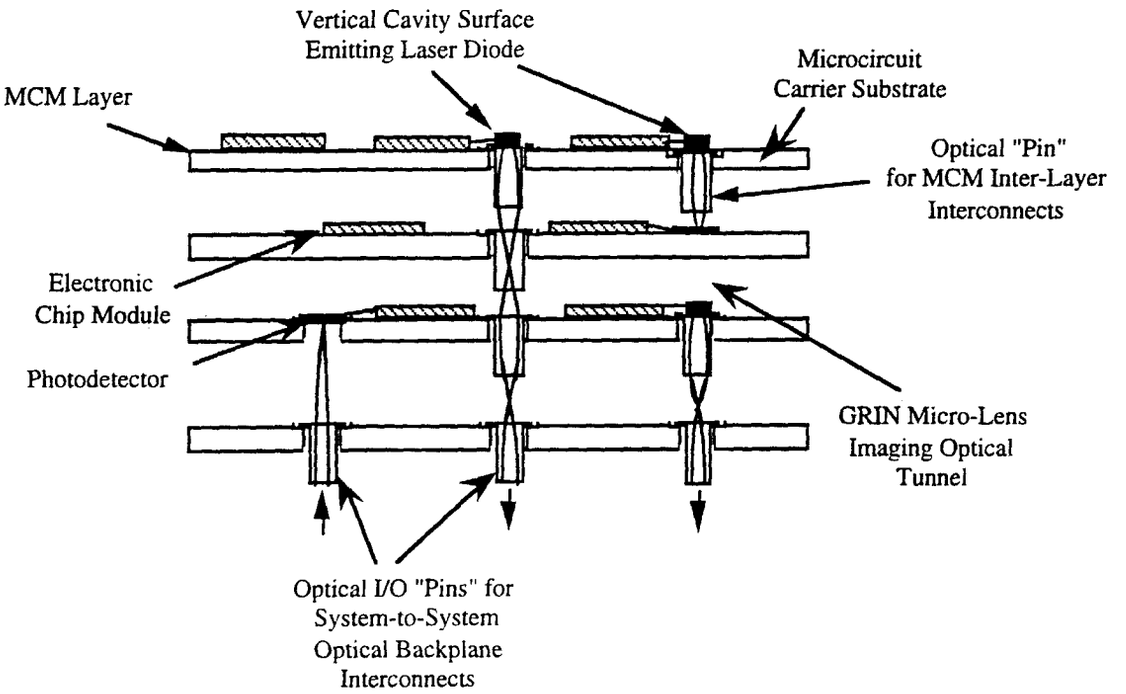


Figure 2-12 Schematic of optical interconnect structure inside the MCM package.

During the preliminary investigation, the following simple formulas have been used in the GRIN lens selection and I/O pin design.

1. Refractive index distribution of GRIN lens

$$N(\gamma) = N_0\left(1 - \frac{A}{2}\gamma^2\right) \tag{2-1}$$

where N_0 is the base refractive index at the optical axis; A is squared gradient constant; and γ is radial positions of the lens.

2. Lens pitch and length

$$Z = \frac{2\pi p}{\sqrt{A}} \tag{2-2}$$

where Z and p are the length and pitch of GRIN lens, respectively.

3. Object and image distance (see Figure 2-13)

$$\ell_2 = \frac{1}{N_0\sqrt{A}} \cdot \frac{N_0\ell_1 \cdot \sqrt{A}\cos\left(\sqrt{A}Z\right) + \sin\left(\sqrt{A}Z\right)}{N_0\ell_1 \cdot \sqrt{A}\sin\left(\sqrt{A}Z\right) - \cos\left(\sqrt{A}Z\right)} \tag{2-3}$$

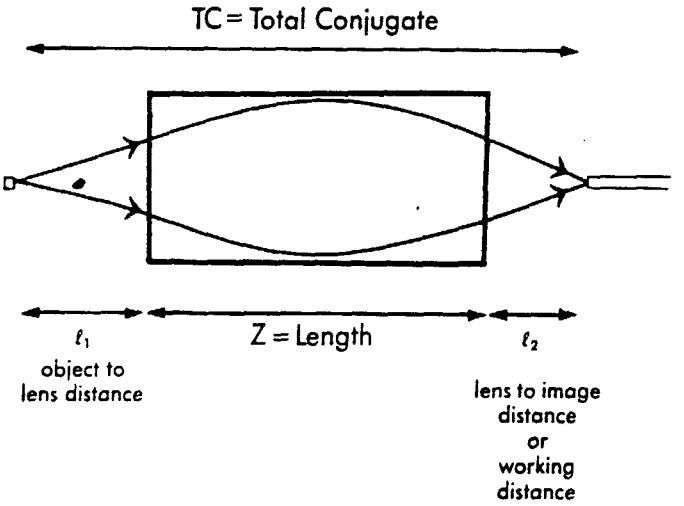


Figure 2-13 Relation between object distance and image distance.

Note that in the collimation case (1), $\ell_1 = 0$, $\ell_2 = \infty$, while in the focusing case (2), $\ell_1 = \infty$, $\ell_2 = 0$. In the point-to-point case (3) and relay case (4), ℓ_1, ℓ_2 and Z are decided by board-to-board distance.

2.2 Optical "Pin" and "Pin" Grid Array with Lensed Optical Fiber and Fiber Array

During the investigation, we found that although the "pin" architecture with GRIN lenses is promising in the long-term, it does show the following shortcomings for the near-term:

1. There are many types of GRIN lenses available, such as SLS, SCW, and SCH types with numerical apertures from 0.3 to 0.6, physical apertures from 100 μm to 6 mm, pitches from 0.11 to 0.29, and different materials for different optical wavelengths. However, the choices of current GRIN lenses are still not enough for the flexible optical "pin" application.

2. Generally speaking, the one-by-one GRIN lens assembly lacks a low cost mass production capability.

3. For large "pin" grid arrays and large number of connections, the GRIN lens "pin" is too expensive to meet commercial markets.

In order to overcome the above-mentioned shortcomings, POC has developed a second version of optical I/O "pin" and "pin" grid array architecture using standard optical fibers, silicon V-grooves, and a fiber lensing technology.

Significant improvements were made by replacing the GRIN lenses with commercially available fibers. MCM board layers can be connected using fibers with appropriate lengths. The fibers are prepared in-house by polishing one end and forming a lens on the other end. Figure 2-14 shows the schematic of a typical optical fiber "pin" with a flat polished face on one end and a lensed face on the other end.

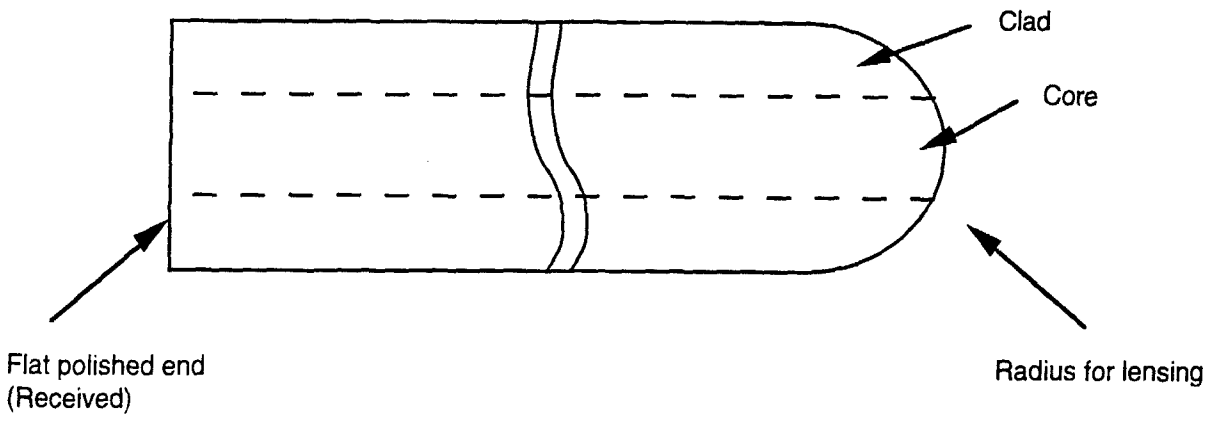
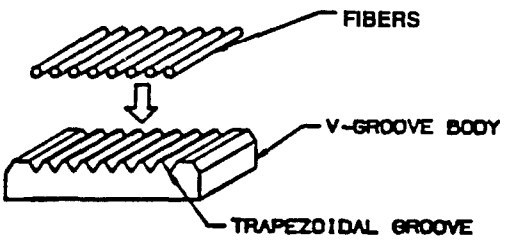


Figure 2-14 Schematic of a single lensed optical fiber "pin".

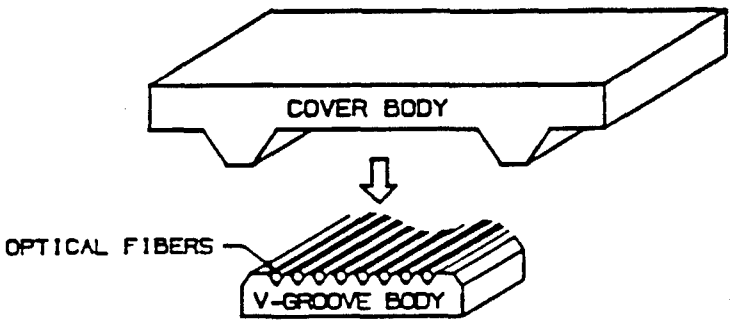
The brief fabrication procedure of the optical fiber "pin" array is as follows:

1. Cut commercially available fibers to the required length.
2. Lens one end of the fiber using POC's combined chemical etching and torching technologies.
3. Put the prepared fibers into a predesigned V-groove. Carefully align the lensed ends in a line, then fix all fibers with either epoxy or ceramic materials.
4. Cut the other ends of fibers to the exact length demanded, and then polish these ends together with the V-groove. It is beneficial to polish many pieces at the same time.

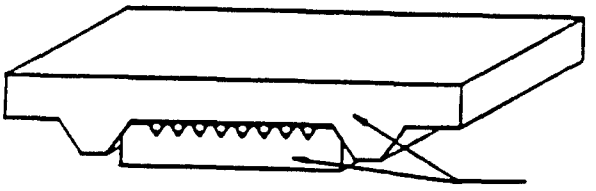
The V-grooves are designed to hold a group of fibers into place (see Figure 2-15). In this prototype, three sets of fibers are positioned and fixed in V-grooves made from a silicon substrate. The grooves are etched to accommodate the fiber dimensions used. These V-grooves can be replaced in the future with a ceramic substrate dimensioned to allow the fiber to be placed via the multi-layers in a pre-arranged fashion.



Step 1. Fibers are positioned in the V-groove



Step 2. Cover body is located on top of the V-groove body



Step 3. Completed unit

Figure 2-15 Silicon V-groove support for fibers.

Figure 2-16 shows the photograph of a lensed fiber array fabricated based on the above fabrication procedure.

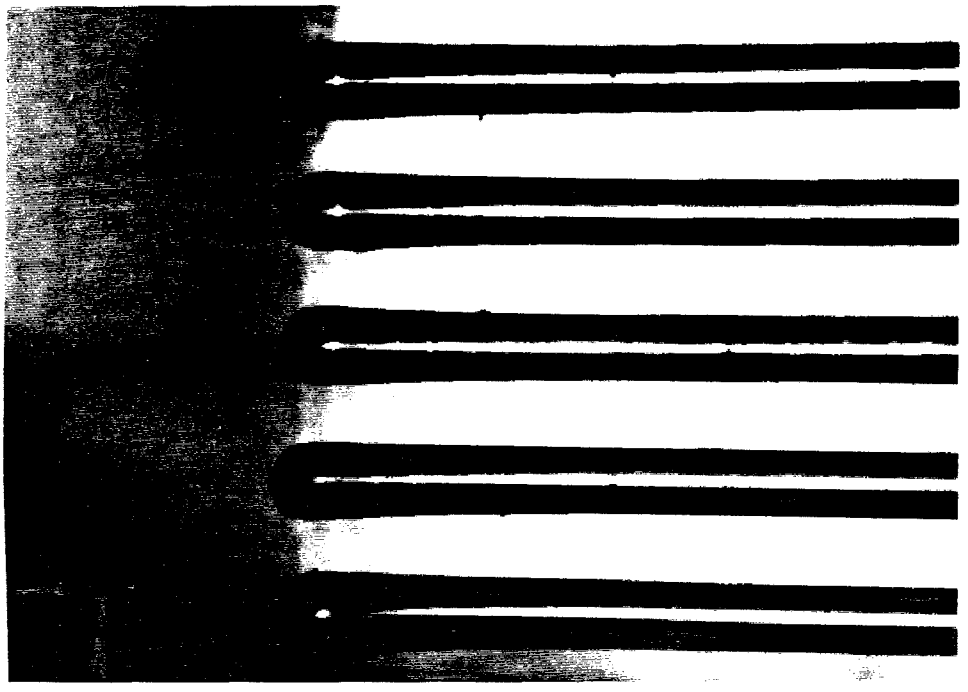


Figure 2-16 Photograph of a lensed fiber array.

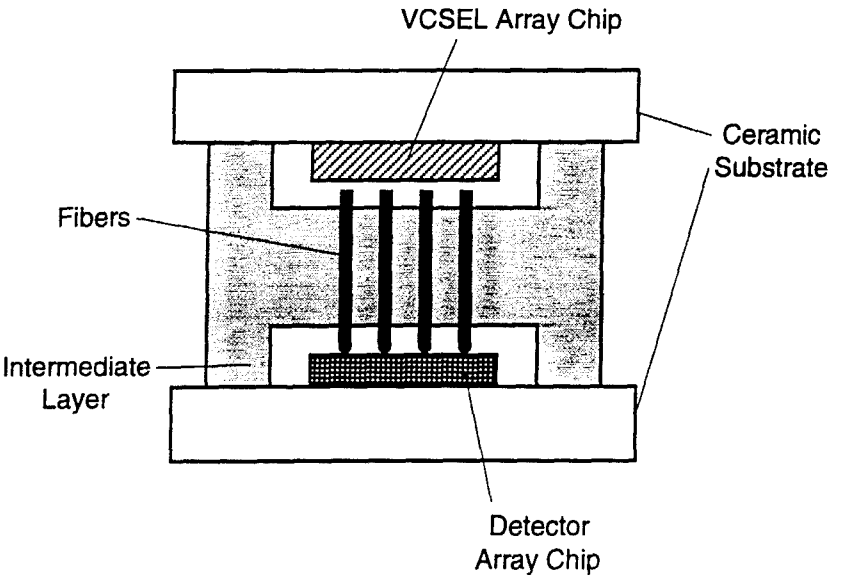
The following advantages are achieved using this optical fiber "pin" version:

1. Standardization and low cost.
2. Easy design and fabrication.
3. Small fiber and V-groove dimensions with high density potential.
4. High adaptability to any board-to-board interconnections (by controlling the fiber length).
5. Low loss and low crosstalk.

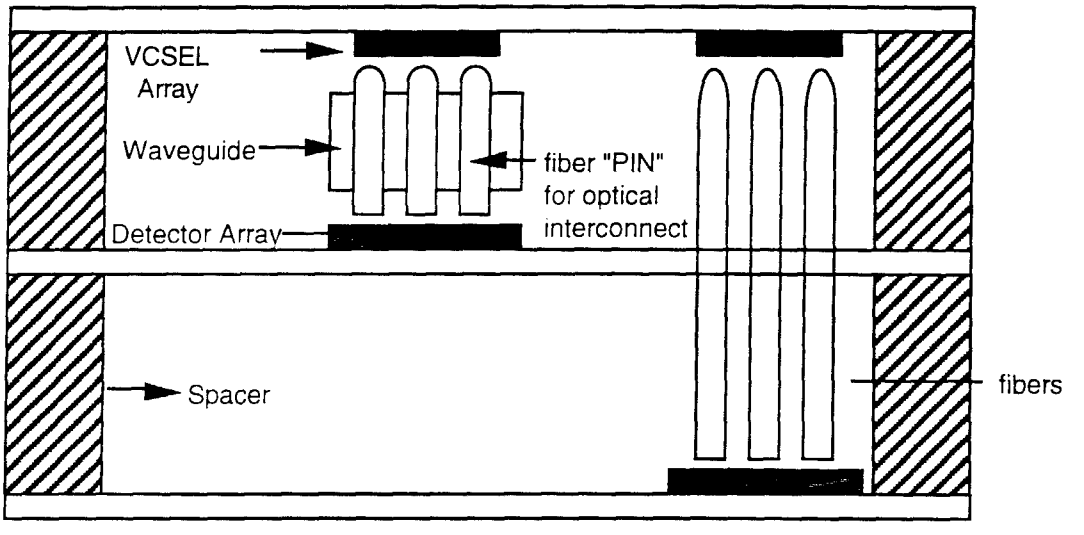
In addition, for higher interconnection quality, the flat end of the fiber can be polished in 7° – 10° angles to eliminate any back reflection to the light source.

2.3 Phase I Engineering Prototype

Based on the results of the lensed optical fiber "pin" technique, we designed a Phase I engineering prototype (Figure 2-17 (a)). The prototype consists of a VCSEL array chip, a detector array chip, and a lensed fiber pin array. The prototype is supported by two ceramic substrates and some spacers in-between the arrays. It can be expanded to a 3-layer design (see Figure 2-17 (b)), with a fiber pin array connecting layers #1 and #2, and the other connecting layers #1 and #3.



(a) Two layer optical "pin" connection.



(b) Three layer optical "pin" connection.

Figure 2-17 Schematic of board-to-board optical interconnect prototype.

The alignment procedures of the prototype are described as follows:

1. Because of the limited resources of Phase I, the lensed and prepared fibers are placed and fixed in a V-groove to provide the 250 μm (center-to-center).
2. Ideally, the ceramic substrate will accommodate the fibers via holes to the pre-arranged destination.
3. The present alignment process consists of first aligning the fiber array to the VSCEL's. At maximum output, the fibers are epoxied into position.
4. After attaching the spacer between the substrates, the detector substrate is then aligned and fixed in position.
5. After curing, the unit was tested for low frequency signal transmission.

Note that the preparation of the lensed fibers took several important precautions:

(i) The fibers were cut to the required length and stripped; (ii) it was important that the fiber ends were free of chipping and uneven surfaces, and that the cleave was perpendicular; (iii) after inspection, the fibers were placed under a microscope (70 ×) and a small torch was used to gradually flame the end face. The small diameter glass can melt rapidly; thus, the process needed constant attention.

Figure 2-18 shows the microscopic photo of the pigtailing between the fiber pin array and the VCSEL array. Figure 2-19 shows the microscopic photo of the pigtailing between the fiber pin array and the detector array. Figure 2-20 shows the photo of the finished prototype. We used a CW signal to align the fiber to the VCSEL array and the corresponding detector array.

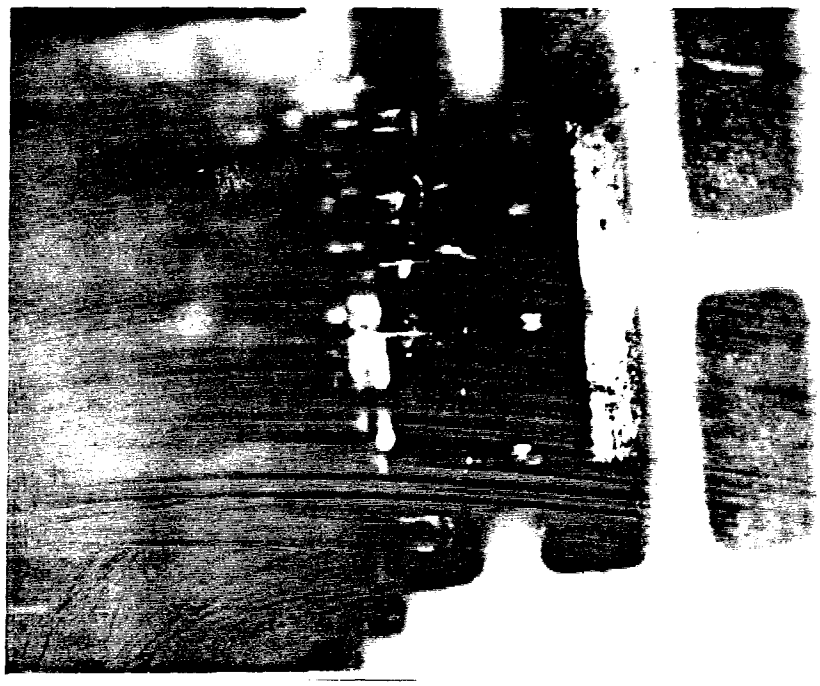


Figure 2-18 Microscopic photo of the pigtailing between the fiber pin array and the VCSEL Array.

Figure 2-19 Microscopic photo of the pigtailing between the fiber pin array and the detector array.

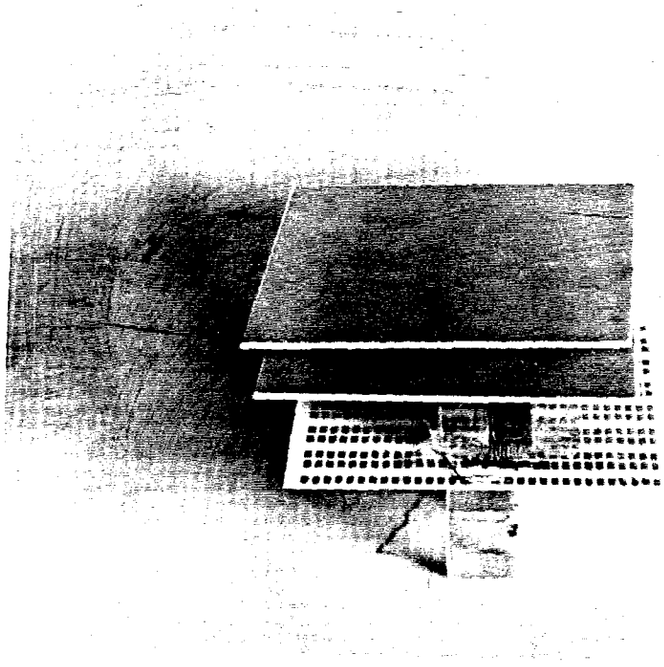


Figure 2-20 Photograph of the constructed Phase I engineering prototype.

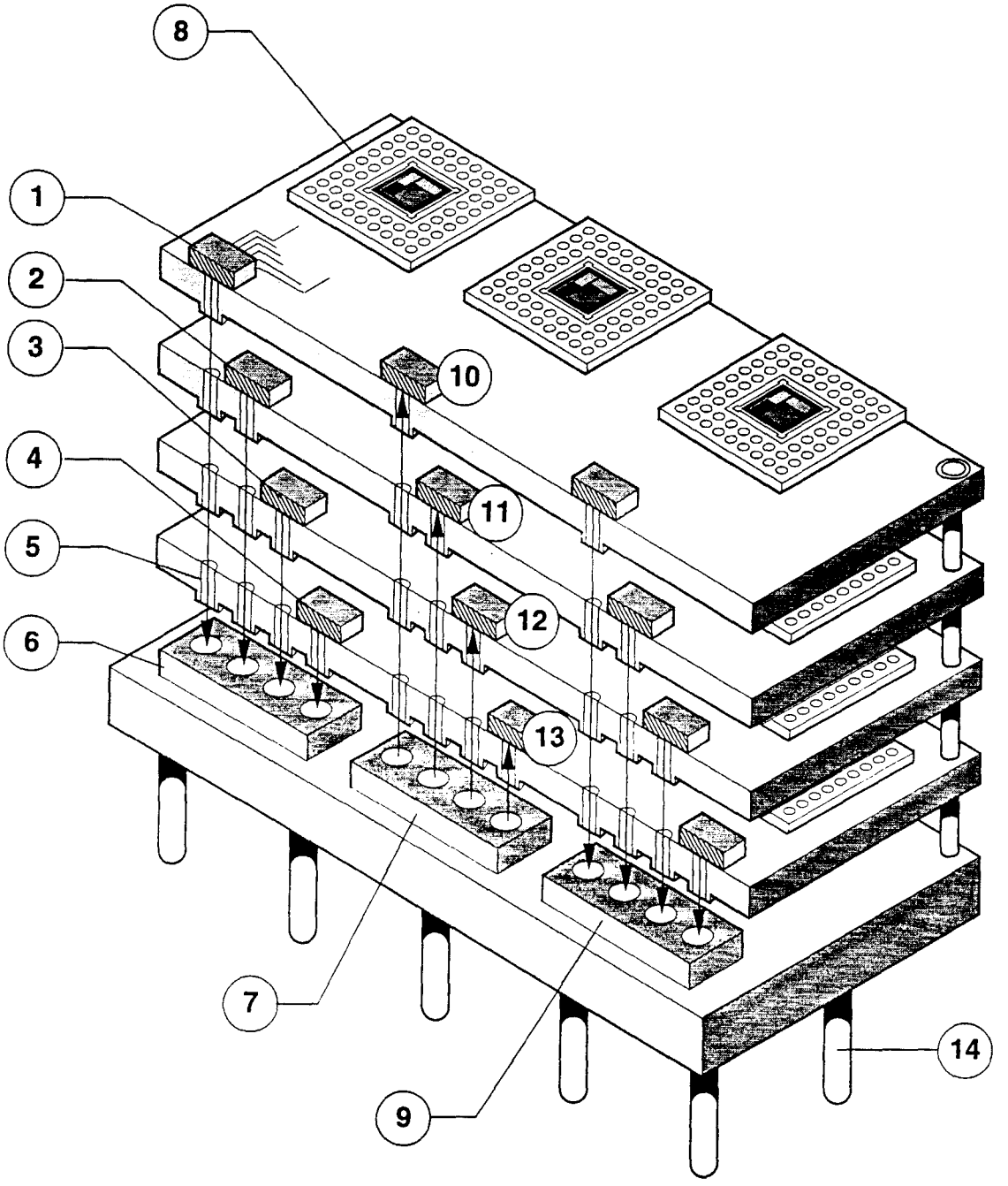
3.0 RECOMMENDATIONS FOR FUTURE DEVELOPMENT

POC feels that the optical fiber "pin" and pin grid array architecture is very promising. With the standard fiber "pin" structure developed, a new type of standard interconnect chip structure can be developed through the following two steps:

1. Design multi-layer I/O map to integrate electronics and optical interconnects for specific MCM functions.

2. Custom make ceramic boards with holes to insert prepared fibers to the designated lay-out.

A schematic of a future standard optical "pin" interconnect chip is shown in Figure 3-1. In accordance with most common requirements, a standard "drop-in" chip-type optical I/O "pins" and "pin" grid array will be designed and fabricated.



Legend:

1. Discrete VCSELs (One Per Layer)
2. Discrete VCSELs (One Per Layer)
3. Discrete VCSELs (One Per Layer)
4. Discrete VCSELs (One Per Layer)
5. GRIN Lens Placed in Non-Plated VIA
6. Detector Array
7. VCSEL Array
8. VCSEL Driver/Interface Circuitry
9. VCSEL Array
10. Discrete Detector (One Per Layer)
11. Discrete Detector (One Per Layer)
12. Discrete Detector (One Per Layer)
13. Discrete Detector (One Per Layer)
14. Standard Pin

Figure 3-1 Schematic of future standard optical "pin" interconnect chip structure.

4.0 CONCLUSIONS

In this Phase I investigation, POC has studied and experimented with two types of optical I/O pin approaches. The first approach was carried out using VCSELs, micro-GRIN lenses, and photodetector arrays. Although this is promising, some shortcomings were discovered, such as design structure and packaging difficulties caused by the limited selection of standard GRIN lenses and non-standard VCSEL arrays with 125 μm or 250 μm separation. The second approach was carried out using VSCEL's standard optical fibers with lensed ends, thin film V-grooves, and photodetector arrays. Much improvement in design, fabrication, and packaging has been achieved using this approach. In addition, the prospects for standard chip-type optical I/O "pin" interconnection is also very promising. A Phase I demonstration prototype was designed and constructed to demonstrate the proposed I/O pin interconnect technique. POC strongly believes that further development of this technology will be very beneficial for both military and commercial applications.

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