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FINAL DOCUMENTATION OF
AN ENHANCED ROBUSTNESS MODULE DESIGN
(Reference ACC Maintenance Manual
for Robustness II)

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Submitted to: Defense Advanced Research Projects Agency
Information Processing Techniques Office
1400 Wilson Boulevard, Arlington, VA 22209

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ROBUSTII.MM.V001
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ROBUSTNESS II
MAINTENANCE MANUAL

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Top Assembly, Robustness II (4 sheets), dwg # 8100133
 Parts List, Robustness II (sheet 1), dwg # 8100133

Logic Diagrams, Robustness II (6 sheets), dwg # 2600244

CHAPTER 1

1.0 INTRODUCTION

1.1 Maintenance Manual Contents - This manual describes the hardware, application, operation, and maintenance of the Robustness II Module (ACC Part #8100133) manufactured by Associated Computer Consultants, Santa Barbara, California.

1.2 Maintenance Manual Organization - This manual is divided into five chapters as follows:

- Chapter 1 - Introduction
- Chapter 2 - References
- Chapter 3 - Physical Description and Installation
- Chapter 4 - Address Selection, Programming,
and Option Selection
- Chapter 5 - Drawings, Parts List, Schematics

1.3 Robustness II Module Overview - The Robustness II Module consists of one dual-width printed circuit assembly as shown in Figure 1-1. It was designed to enhance the Digital Equipment Corporation (DEC) LSI-11 family of computer systems. Operating on the LSI-11 bus (Q-bus) as shown in Figure 1-2, the Robustness II provides features required by systems operating on telecommunication networks.

1.4 Robustness II Module Application - The Robustness II Module provides a number of functions on a single module in order to allow the programmer great flexibility in system implementation while consuming a minimum of I/O space.

1.4.1 On-Board Boot Code Space - The programmer can use the Robustness II Module to implement onboard boot code to start or restart programs automatically. The Robustness II is available with 4K or 8K words of EPROM, which take only two Q-bus address spaces. This allows operating system software to be stored in EPROM for downline loading rather than on disk or tape. By use of additional dual-width Memory Expansion Boards, which can be attached to the Robustness II Module, additional program storage is available.

1.4.2 Manual Switch Registers - Four switch registers (64 bits) are provided to allow the programmer to store semi-permanent (non-volatile) information such as system I.D., operational function configuration, or system address.

1.4.3 Elapsed Time Counter - For applications in which timing must be checked, a 10KHz counter/timer is provided that can be read at the start and finish of an operation to give an accurate account of the elapsed time during operation.

1.4.4 Watchdog Timer - A Watchdog Timer is provided to restart the system if the Watchdog Timer Register is not "written" every six seconds (or another of seven selectable timeout periods). At a power or software failure, the Watchdog Timer times out and reboots the system. This timer can be disabled for maintenance or software development by setting a switch. It cannot be accidentally disabled under software control.

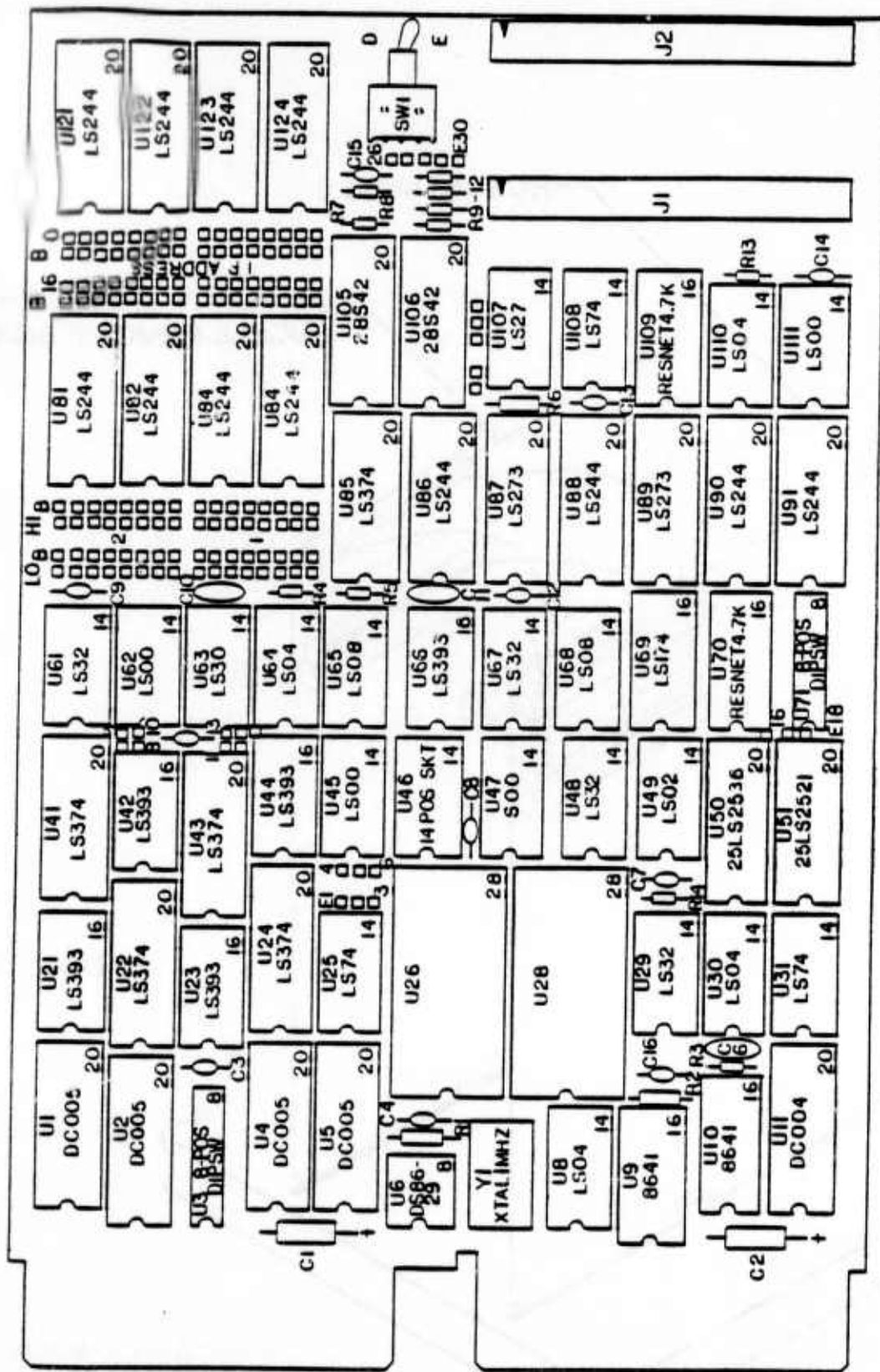


Figure 1-1 Robustness II Module

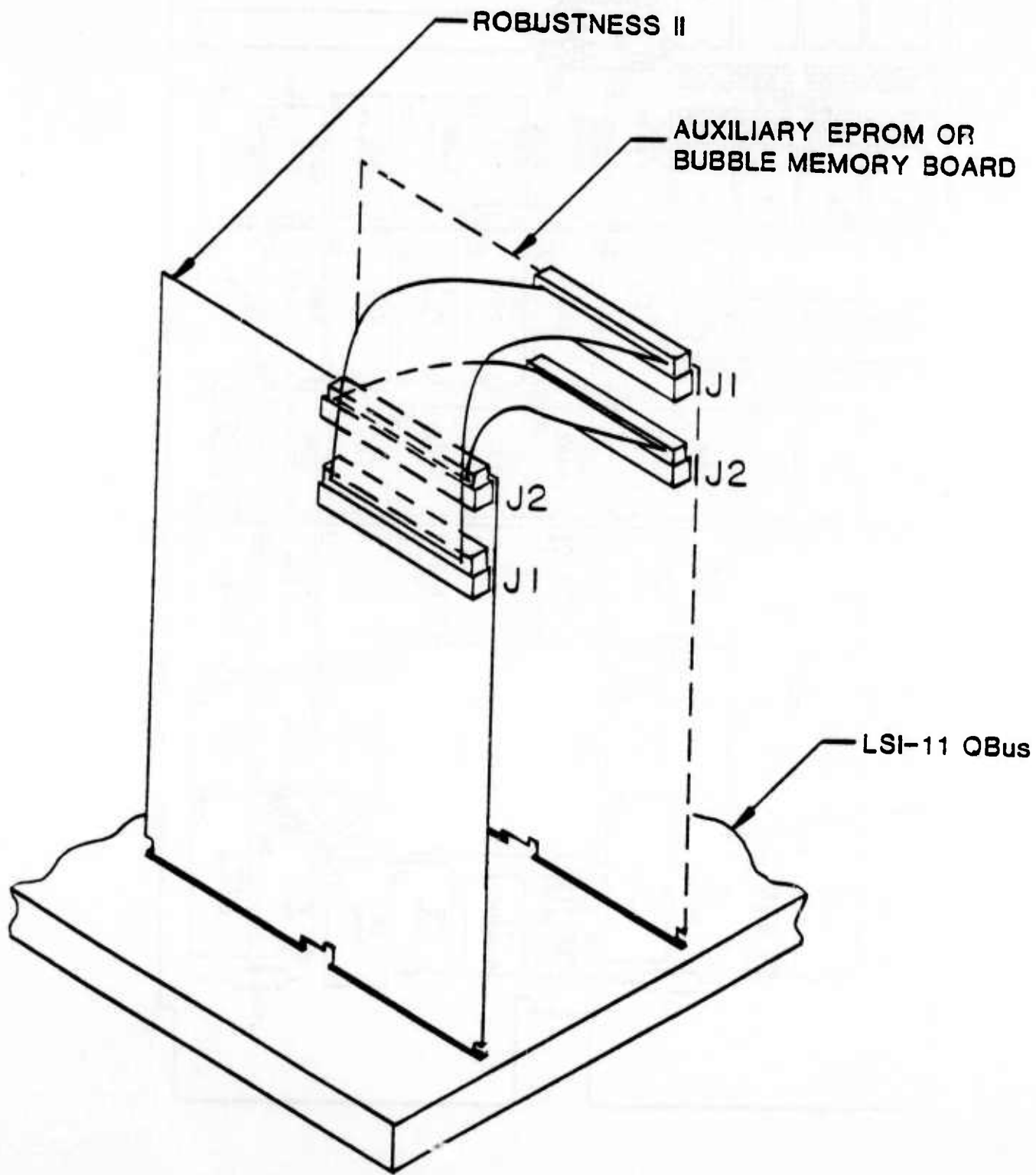


Figure 1-2 LSI-11 Backplane With Robustness II

CHAPTER 2

2.0 REFERENCES

2.1 Reference Documents - The following documents contain additional information on the Robustness II Module.

1. The TTL Data Book
Texas Instruments Incorporated
2. Interface Data Book
National Semiconductor Corporation
3. The Bipolar Microcomputer Components Data Book
Texas Instruments Incorporated
4. The MOS Memory Data Book
Texas Instruments Incorporated
5. Microcomputers and Memories
Digital Equipment Corporation
6. Microcomputer Interfaces Handbook
Digital Equipment Corporation
7. Schottky and Low-Power Schottky Data Book
Advanced Micro Devices, Incorporated

CHAPTER 3

3.0 PHYSICAL DESCRIPTION AND INSTALLATION

3.1 Robustness II Module Particulars - The Robustness II Module is a dual width printed circuit board as shown in Figure 1-1. It is connected to the LSI-11 bus (Q-bus), and requires one standard load to that bus. Though the Robustness II Module does not use interrupts or DMA transfers, it does provide grant continuity for interrupts and for DMA grant signals. The Robustness II Module consumes approximately 2.5 Amperes at +5Vdc. No other voltages are required.

3.2 External Cabling - Two connectors (J1 and J2) are provided for external cable connection to the Robustness II Module. See Figure 2-1 for an illustration of this interconnection.

3.3 Robustness II Module Organization - The Robustness II consists of three main sections which are listed below and explained in the subsequent paragraphs.

Boot PROM Section
Registers/Watchdog Timer
External Bus

3.3.1 Boot PROM Section - The two boot PROMs contain a total of 512 words (512x16 bits) of PROM. Because of the address space limitations of the LSI-11 bus I/O page, only a portion of this PROM space is used at any one time. Two configurations for PROM use are available: 256 words of PROM or 128 words of PROM. With the 256 word configuration, either of the 256 word blocks may be selected by wire wrap jumpers. In the 128 word configuration, any one of the four 128 word blocks may be selected by wire wrap jumpers. These configurations are discussed in detail in Chapter 4. The actual I/O page address of the PROM block can be set by the user.

3.3.2 Register Section - The Register Section contains eight (word) registers that provide most of the Robustness II Module functions. The base address of this block of registers in the I/O page can be set by the user (see Section 4.1). The registers listed below are described in Chapter 4.

- 00 Control/Status Register
- 02 Cell Address Register
- 04 Data Register
- 06 Timer/Counter Register (least significant word)
- 10 Timer/Counter Register (most significant word)
- 12 Switch Register No. 1 (read) Watchdog Timer (write)
- 14 Switch Register No. 2
- 16 Not Used

3.3.3 External Bus - External bus connections J1 and J2 are provided to connect up to 256K words of external RAM, ROM, PROM, EPROM or Bubble memory. All incoming control signals provide open collector inputs to allow more than one external bus connection at a time. Figure 1-2 illustrates the interconnection of memory extension boards to the External Bus.

CHAPTER 4

4.0 ADDRESS SELECTION, PROGRAMMING, AND OPTION SELECTION

4.1 Robustness II Register Block Address Selection - The register block address is controlled by the eight DIP switches on U03 and one DIP switch on U71. Figure 4-1 shows the DIP switches on U03 and U71 and the associated address line of each. The address block selected must not interfere with that of an already existing device on the LSI-11 bus. When a DIP switch is closed, the associated address line must be asserted for a match. When a DIP switch is open, the associated address line must be negated for a match. All switch settings must match their appropriate address lines before the register bank can be selected.

4.2 Control/Status Register (CSR) - This register provides status and control to the other Robustness II registers, the external bus interface, and the boot PROM section. The following table describes each of the CSR bits. These CSR bits are referred to in discussions of the other registers.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Error	Invalid Address	Not Write Enabled	Not Written	Not Used	Watch Dog Is Disabled	BD2 Can Write	BD2 Is There	All OK	Boot Select	Switch Bank Enable	BD2 Write Enable	Ext. Addr Bit 17	Ext. Addr Bit 16	Board 2 Select	Timer Latch Enable
R	R	R	R	-	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	W

W = Write Only
 R = Read Only
 R/W = Read or Write

BIT DEFINITION

- 0 Timer/counter Latch Enable - Latches the 32 bits of the counter/timer into the two counter/timer registers.
- 1 External Bus Select - Sets the external bus enable line on the external bus. Also disables on-board EPROM and enables the error bits 12, 13, and 14 to indicate errors from the external bus rather than from the Robustness II Module.
- 2 Extended Address Bit 16 - Used by the external bus to extend the addressing capability of the 16 bit cell address bus (CELADR00 - 15).
- 3 Extended Address Bit 17 - Used by external bus to extend the addressing capability of the 16 bit cell address bus (CELADR00 - 15).
- 4 Board 2 Write Enable - A high (1) sets the write enable line on the external bus. A low (0) acts as a write protect for the external bus.
- 5 Switch Register Bank Enable - A low (0) enables Bank A of both switch registers and a high (1) enables Bank B.

- 6 Boot Select (if wire-wrapped into the PROM boot addressing) - Selects one boot PROM block or another.
- 7 All OK - Indicates that the Robustness II module is functioning, and that the external bus is functioning if it is selected.
- 8 External Bus is There - Incoming signal line from external bus asserted (high) indicates that there is a board connected to the external bus.
- 9 External Bus Can Write - Incoming signal line from external bus bus asserted (high) indicates that the board connected to the external bus is writeable.
- 10 Watchdog Timer Disabled - An active low (0) signal Watchdog Timer Disabled - An active low (0) signal indicates that the watchdog timer has been disabled by switch 1 on the Robustness II card edge.
- 11 Not Used
- 12 Address Not Writeable - An error bit. When asserted (high) indicates that a write was tried to read only memory. Any write to the Robustness II EPROM will cause this error. An error of this type from the external bus is possible but indication of the error depends on the external bus configuration to so indicate.
- 13 Address Not Write Enabled - An error bit. When asserted (high) indicates that a write was tried 1) to the Robustness II EPROM, or 2) to the external bus while CSR bit 2 (external bus write enable) was negated.
- 14 Invalid Address for Robustness II - When asserted (high), indicates that the given address is out of range of the EPROM (either 4K or 8K words selected). When the external bus is selected and CSR bit 2 is asserted (high), an error signal from the external bus (BD2BAD) asserted (high) will also assert this error bit.
- 15 Error - Master error bit. Logical OR of CSR error bits 12, 13, and 14.

4.3 Cell Address/Data Register - The Robustness II module supports either 4K or 8K words of board EPROM memory. This memory is accessed through two registers, the Cell Address Register (address XX02) and the Data Register (address XX04). To read a block of memory, the programmer loads the starting address into the Cell Address Register, then reads the Data Register. To access the next word, the Cell Address Register is loaded with the next word address and the Data Register is again read. Unlike a standard bus address, the Cell Address Register addresses words only, so the first word is at address 0 (octal), the next at address 1, then 2, 3, 4, and so on. See 4.3.1 and 4.3.2 for details.

4.3.1 Cell Address Register - The cell address register is a 16 bit read/write latch. When written to, this register latches the 16 bit word of address information onto the cell address bus (CELADR00 - 15). This address word selects one data word, which is placed on the BDA bus when the data register is read. The address word is used by the onboard EPROM (CELADR00 - 11), or by the external bus (CELADR00 - 15) if it has been selected. The cell address register is configured for word addressing only. The least significant bit of the cell address bus (CELADR00) indicates low word/high word, not low byte/high byte. This configuration extends the 18 bit address range to 256K words, from the normal 256K bytes usually accessible by an 18 bit address. A block of data can be consecutively read by continually updating the cell address register with the address of the next word of data, and then reading the cell data register.

4.3.2 Data Register - There is no actual hardware data register. The address information latched onto the cell address bus (CELADR00 - 15) selects the memory word, and a read or write to the cell data register performs a read or write to or from the selected memory word. Since the memory word is tri-stated (buffered) onto the BDA bus, an actual hardware data register is not necessary.

4.4 The Timer/Counter Registers 1 and 2 - The 32 bit timer/counter runs continuously at 10KHz and can be latched into the two timer/counter registers at any time by ORing a 1 into CSR bit 0. Then the registers can be read at the programmer's leisure. The least significant word is at address XX06, and the most significant is at address XX10. An event can be timed by latching the timer/counter registers, starting the event, and then reading the registers to get the starting time. When the event is completed, the timer/counter registers are again latched, and the first reading is subtracted from the second to give the elapsed time in 10KHz increments. This may be converted to a more convenient format, such as minutes, seconds, tenths and hundredths, as required.

4.4.1 Details of Timer/Counter Registers 1 and 2 - The 32 bit timer/counter uses a 10KHz clock, which is derived from a 1 MHz crystal oscillator. A one written to bit 0 of the CSR latches the 32 bits of the timer/counter, in two 16 bit halves, into timer/counter registers 1 and 2 where they can be read. The 32 bits are latched so that one 16 bit half does not increment into the next between reads and cause a false reading. Timer/counter register 2 contains the most significant 16 bits.

4.5 Watchdog Timer - The watchdog timer is provided as a watchdog to the system. If the system fails to reset the watchdog timer for any reason, the watchdog timer will reinitialize the system. The watchdog timer is reset by writing a 370 or 371 (octal) to address XX12 of switch register 1 before the timeout period has expired. The timeout period is factory set at approximately six seconds, but may be changed as explained in chapter 4. The watchdog timer may be disabled by setting switch 1 to the D position. When the watchdog timer is enabled, CSR bit 10 is asserted (1); when disabled, CRS bit 10 is negated (0).

4.5.1 Details of Watchdog Timer - The Watchdog Timer will restart and reboot the CPU if the program in control fails to reset the timer by writing 370 or 371 (octal) into the Watchdog Timer Register. This ensures that hardware or software interruptions to proper program flow do not disable the system for any longer than one watchdog timeout period (factory set at 6 seconds). The timeout period can be changed by the user to accommodate other programming environments. The Watchdog Timer can be disabled by setting switch 1 to the D (disabled) position.

NOTE

The Switch Register 1 (see 4.6) and Watchdog Timer Register functions are performed by one dual function register. A read of this register will provide the contents of Switch Register 1. A write of the correct code to this register will reset the Watchdog Timer.

4.6 Switch Registers 1 and 2 - The two 16 bit switch registers will access a total of 64 bits of information through bank selection. Switch register 1 will read Bank A1 (16 bits) and Bank B1 (16 bits), while switch register 2 will read Bank A2 (16 bits) and Bank B2 (16 bits). Bank selection is enabled by CSR bit 05. A low (0) selects Bank A, and a high (1) selects Bank B. Each of the bits is a wire wrap stake pair that, when wrapped, equals a low (0), and when unwrapped, equals a high (1).

4.7 External Bus - The external bus consists of an address bus (CELADR00 - 15, and CSR bits 2 and 3 for extended address lines 16 and 17), a data bus (BDA00 - 15), and a control bus (including CSR bit 01, external bus enable). Any number of external devices may be connected to the external bus. All of the incoming control lines are pulled up and are designed for open-collector (wired-OR, active low) connection of a number of boards. A total of 256K words of any type of memory may be connected. RAM, ROM, EPROM, EEPROM, or Bubble memory can be connected using the available control signals.

4.8 Configuration of Options - The following options are wire-wrap selectable by the user and are discussed in the paragraphs that follow. A directory of wire wrap locations is given in Figure 4-2.

- EPROM Memory Space
- Address out of Range Error
- Watchdog Timer
- Counter/Timer Reset
- Switch Register Wiring

4.8.1 EPROM Memory Space - The Robustness II Module provides the option of either 4K or 8K words of onboard EPROM. Figure 4-3 shows the installation of 4K words of EPROM (2532) and the associated 4K wire wrap jumper. For the 4K installation, pin 1 of the 24 pin 2532 EPROM must be inserted in pin 3 of the 28 pin EPROM socket. Figure 4-4 shows the installation of 8K words of EPROM (2564) and the associated wire wrap jumper.

4.8.2 Address Out of Range Error - CSR bit 14 (INVADR) indicates an address that is out of range for the onboard 4K or 8K word EPROM. The address limit has a default setting of 4K words, but may be changed for 8K words. The procedure to change the address limit is shown in Figure 4-5.

4.8.3 Watchdog Timer - The watchdog timer reinitializes the system if it is allowed to time out. It can be disabled by setting switch 1 to the D position. As set, the watchdog timer will time out after approximately 6 seconds. This timeout period can be changed by changing the input clock frequency. There are eight clock frequencies available. Figure 4-6 shows how to cut the existing trace and wire wrap the selected clock frequency (time) to the input of the watchdog timer.

4.8.4 Counter/Timer Reset - The counter/timer runs continuously and is normally reset only on system initialization. An optional input is available that allows the user to wire a reset switch into the counter timer reset circuit. This allows the user to reset the counter/timer switch by pushing a button. Figure 4-7 shows the connecting points for a user supplied switch.

4.8.5 Switch Register Wiring - The configuration for the 64 bits of the switch registers is shown in Figure 4-8. Each of the 64 bits has a pair of wire wrap stakes designed to install a jumper clip. If the clip is installed, that bit will read as a zero (0). If the clip is left off, (open), the bit will read as a one (1).

4.8.6 Boot PROM Block Address - The boot PROM block starting address is selected by switches 3 through 7 on U71. Figure 4-9 shows how to set the switches for the address selected.

4.8.6.1 Boot PROM Block Size - The boot PROM block size is selectable as either a 128 word or 256 word block. Figure 4-10 shows how to set both configurations.

4.8.6.2 Boot PROM Configuration - The Robustness II contains two 28S42 PROMs. These PROMs are 512 X 8 bits each in low byte-high byte parallel, and provide 512 16 bit words of PROM. The PROMs can be configured in either 128 or 256 word blocks, and the blocks may be either fixed or switched under software control. Figures 4-11 and 4-12 show the possible configurations and the wire wrap jumper configurations for each.

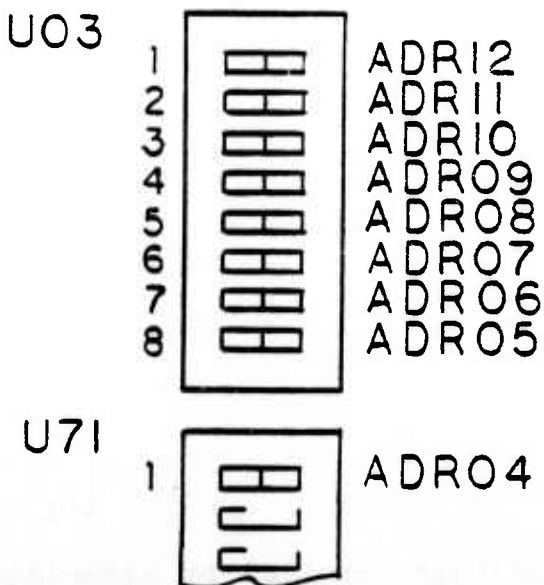
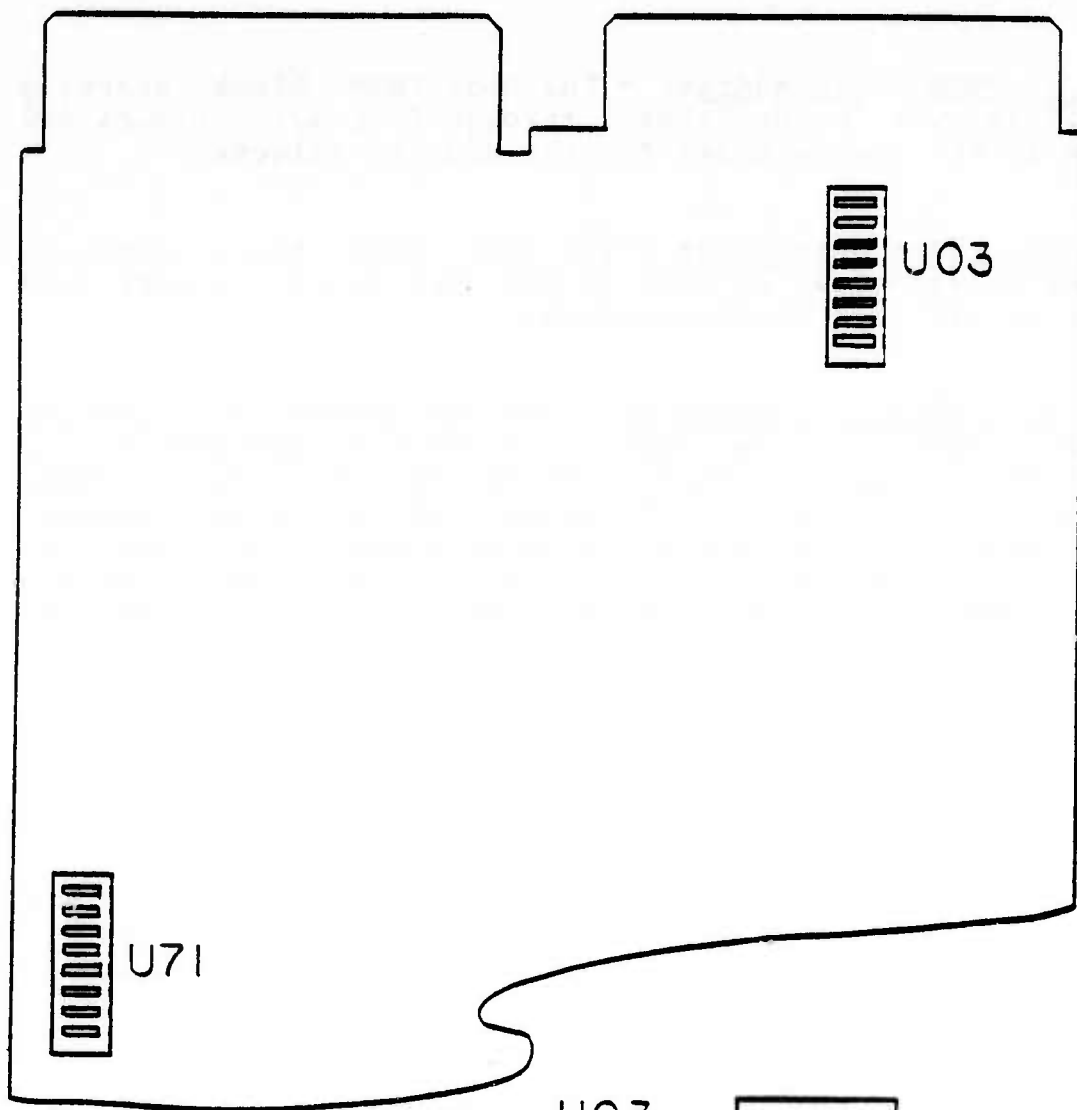
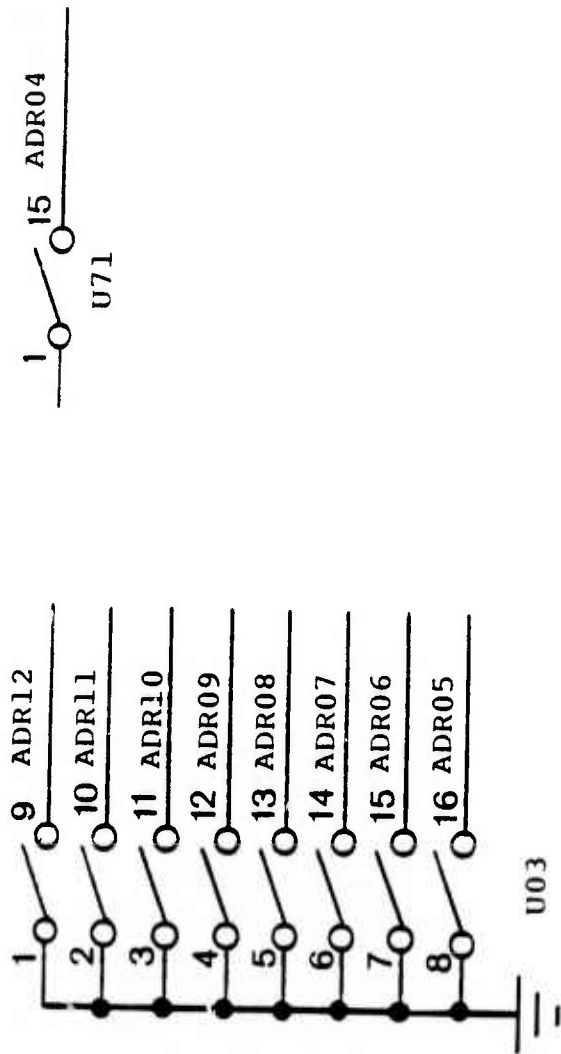


Figure 4-1. Robustness II Register Block
 Address Selection (Sheet 1 of 2)
 4-10



4-11

Register Block Address	7	17	15	16	7	13	12	5	11	10	8	7	6	5	4	3	2	1	0
Address in Binary	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0
Register Block Switch Settings	X	X	X	X	X	X	C	C	0	0	0	0	0	0	0	X	X	X	X

X = Don't Care
 C = Closed
 0 = Open

Figure 4-1. Robustness II Register Block Address Selection (Sheet 2 of 2)

E-POINT	SIGNAL	FIGURE NUMBER
E1	CELADR12	4-3
E2	2532 EPROMS, PIN 23 (VPP)	4-3
E3	VCC	4-3
E4	TLATCH OUT	4-13
E5	TLATS	4-13
E6	TLATCH IN	4-13
E7	TMR03	4-6
E8	TMR10	4-6
E9	TMR09	4-6
E10	TMR11	4-6
E11	TMR04	4-6
E12	TMR06	4-6
E13	TMR05	4-6
E14	TMR07	4-6
E15	TMR08 - TO WATCHDOG TIMER	4-6
E16	BDA08	4-10
E17	U71, PIN 10 (MAT08)	4-10
E18	U51, PIN 14 (MAT08)	4-10
E19	NOT USED	
E20	GND	4-5
E21	U107, PIN 11, GND	4-5
E22	CELADR12	4-5
E23	U107, PIN 10	4-5
E24	BRESET-	4-7
E25	GND	4-7
E26	U85, PIN 2, ROM08A	4-11, 4-12
E27	ROM08, U105, U106	4-11, 4-12
E28	GND	4-11, 4-12
E29	VP	4-11, 4-12
E30	BD2SEL	4-11, 4-12
E31	WR0OUT (U69, PIN 11)	4-14

Figure 4-2. Robustness II Wire-Wrap Locations (Sheet 1 of 2)

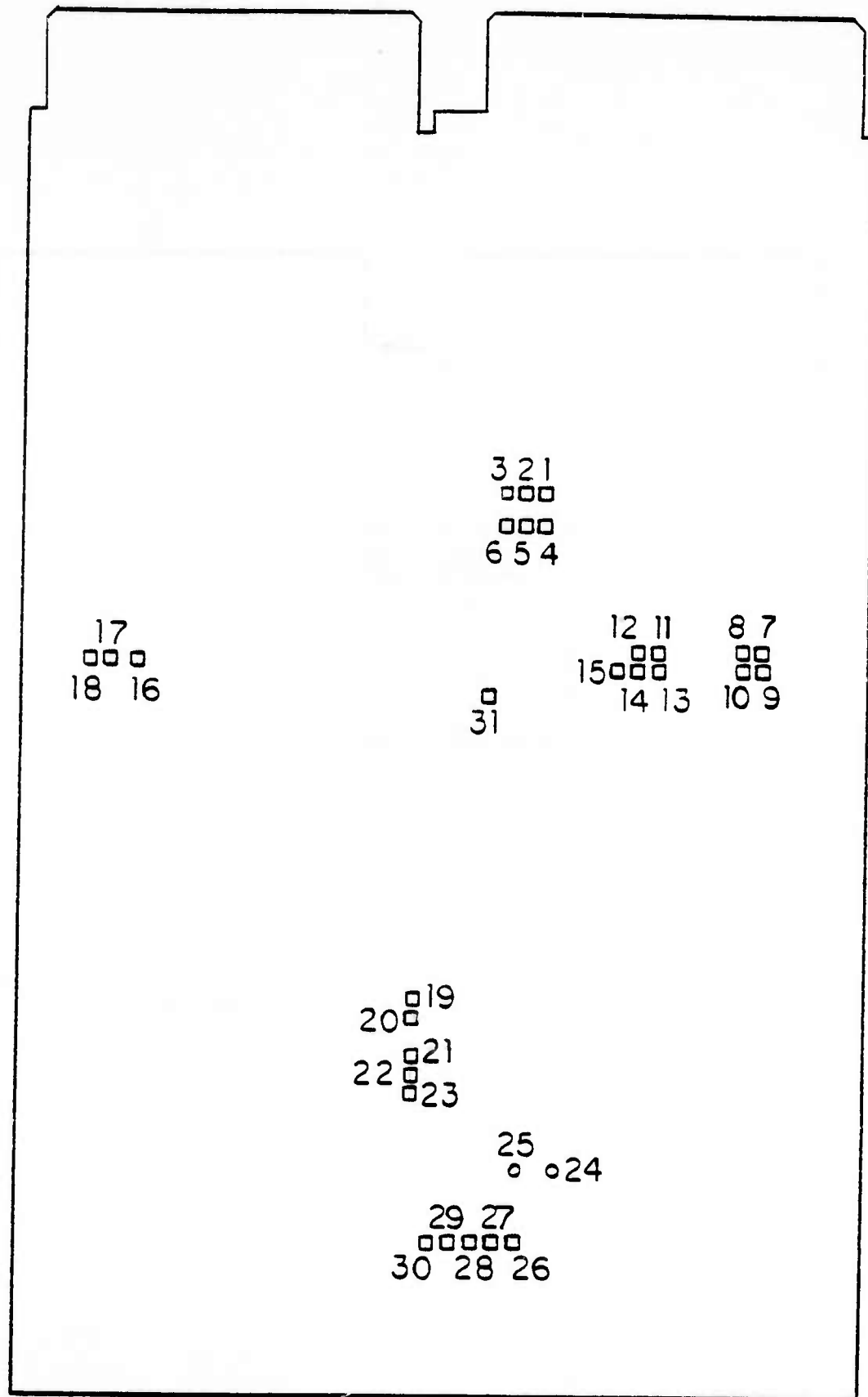


Figure 4-2 Robustness II Wire Wrap Locations (sheet 2 of 2)

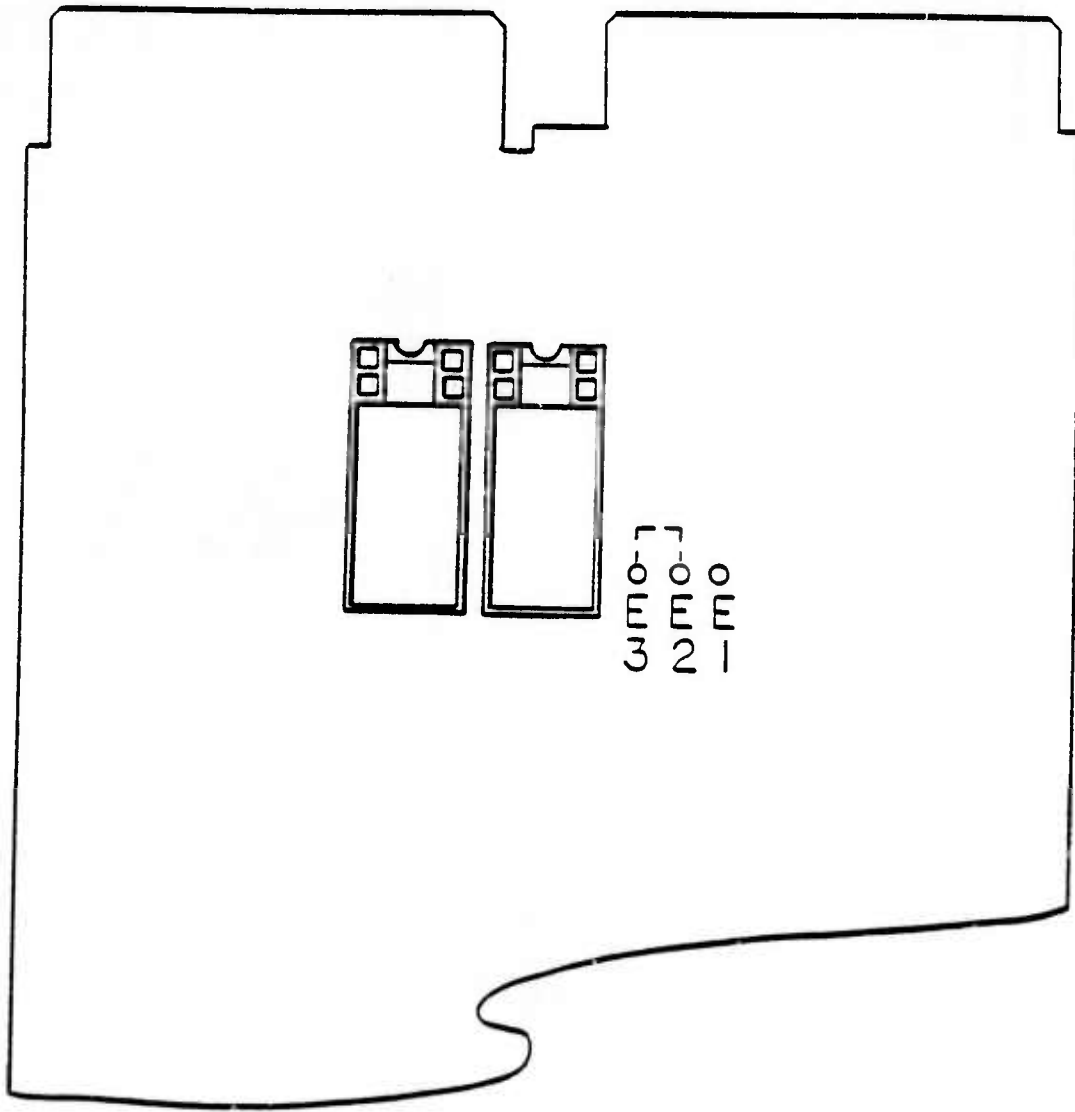


Figure 4-3 Configuration for 4K Words Using 2532 EPROMs

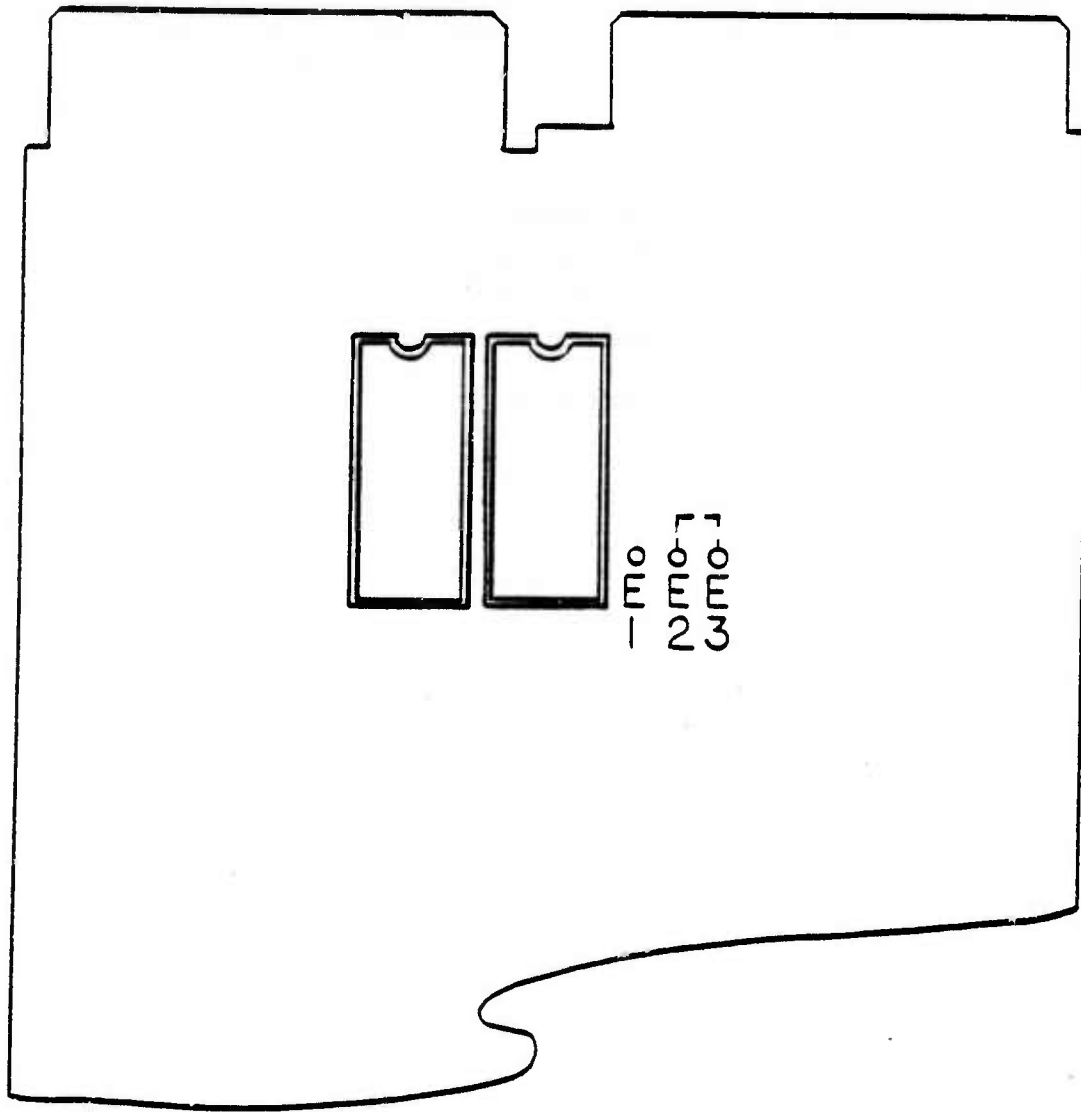
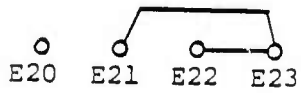
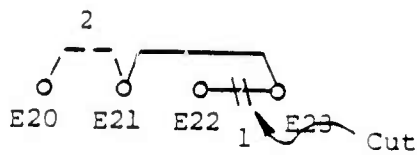


Figure 4-4 Configuration for 8K Words Using 2564 EPROMs.



On Board Address Range Check

Wire Wrap for 4K Words EPROM (Factory Wired)



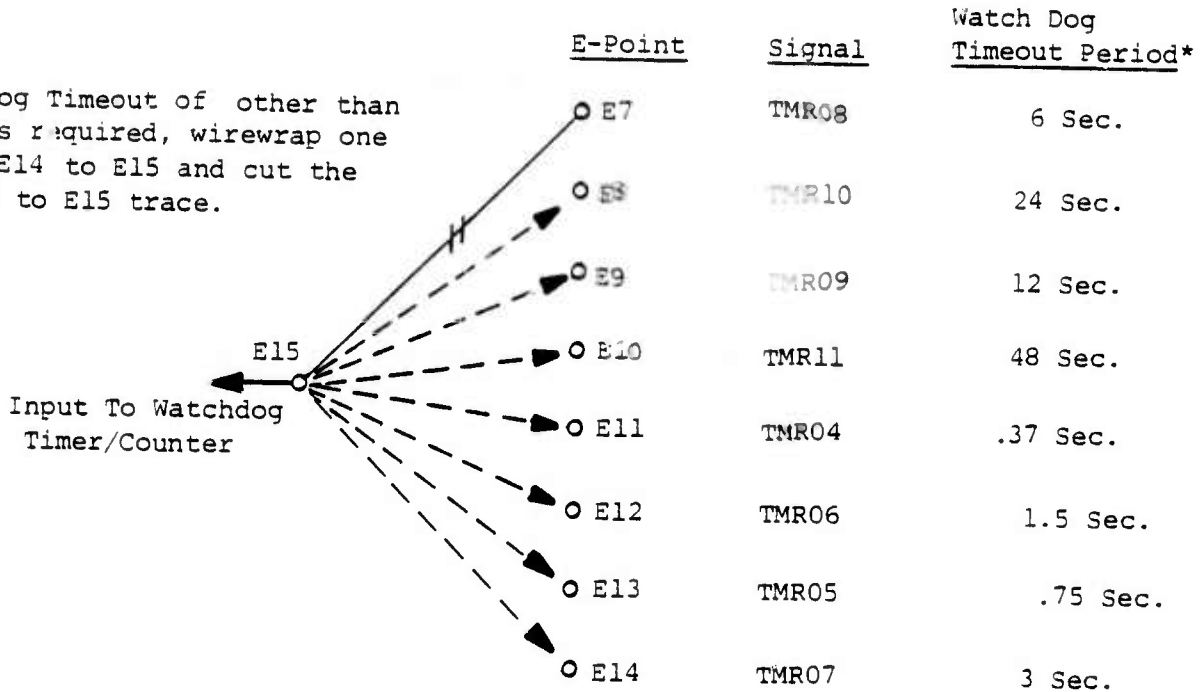
On Board Address Range Check

Wire Wrap for 8K Words EPROM (User Wired)

- 1 Cut the trace on layer 6 (solder side of board) between E22 and E23
- 2 Add a wirewrap jumper between E20 and E21

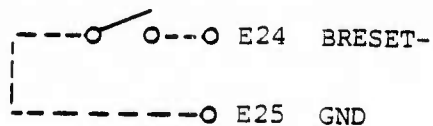
Figure 4-5

If a Watchdog Timeout of other than 6 seconds is required, wirewrap one of Pins E8-E14 to E15 and cut the existing E7 to E15 trace.



* Times are approximate

Figure 4-6 Watchdog Timer Counter Input Select



Off Board Switch connected by the User to reset the counter/timer to zero.

Figure 4-7

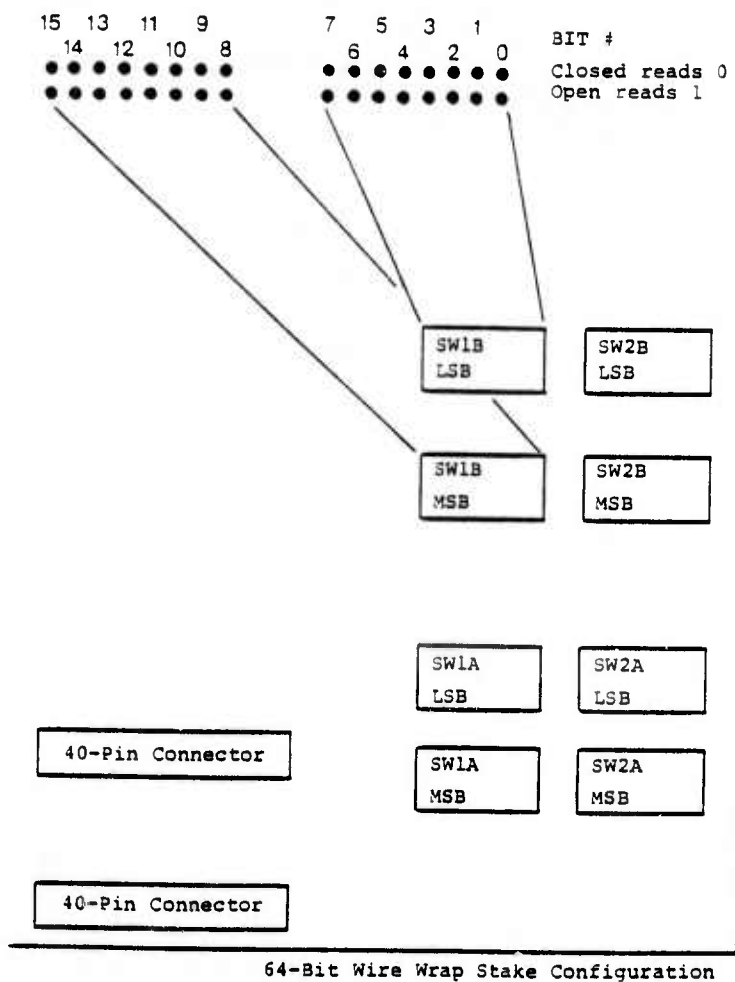
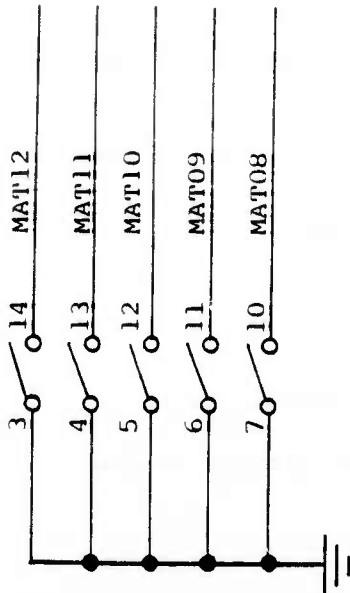


Figure 4-8



Address Line Number	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Boot PROM Address	7	7	7	7	7	3	3	0	0	0	0	0	0	0	0	0	0
Boot PROM Address/Binary	1	1	1	1	1	0	1	1	0	0	0	0	0	0	0	0	0
Boot PROM Switch Settings	X	X	X	X	O	C	O	O	C	X	X	X	X	X	X	X	X

- 1 O = Open or 1
- C = Closed or 0
- X = Do not Care

2 On boards shipped to SRI, the switches have been removed and wire wrap stakes put in their place. A closed switch position would then be equal to a wire wrap wire and an open switch position equal to no wire.

Figure 4-9

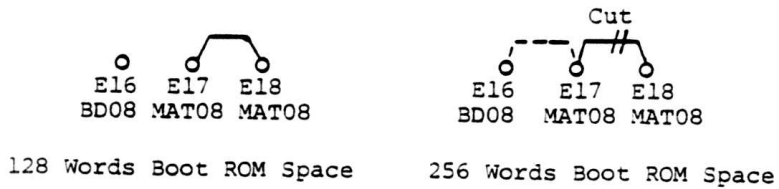


Figure 4-10

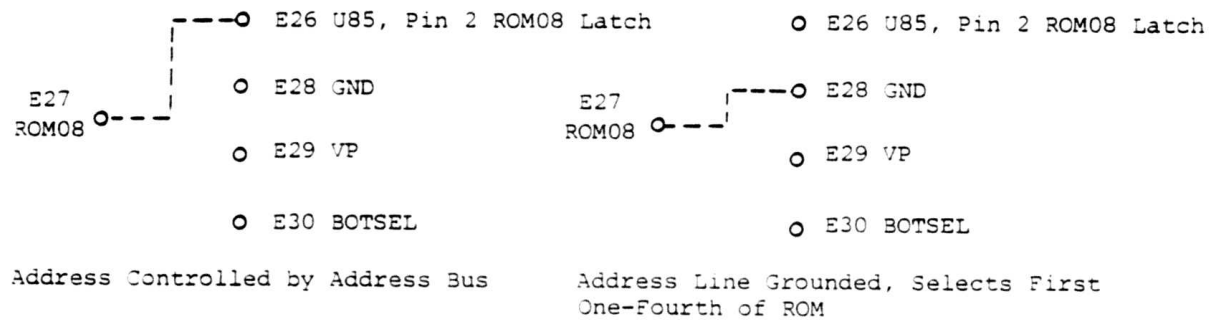


Figure 4-11

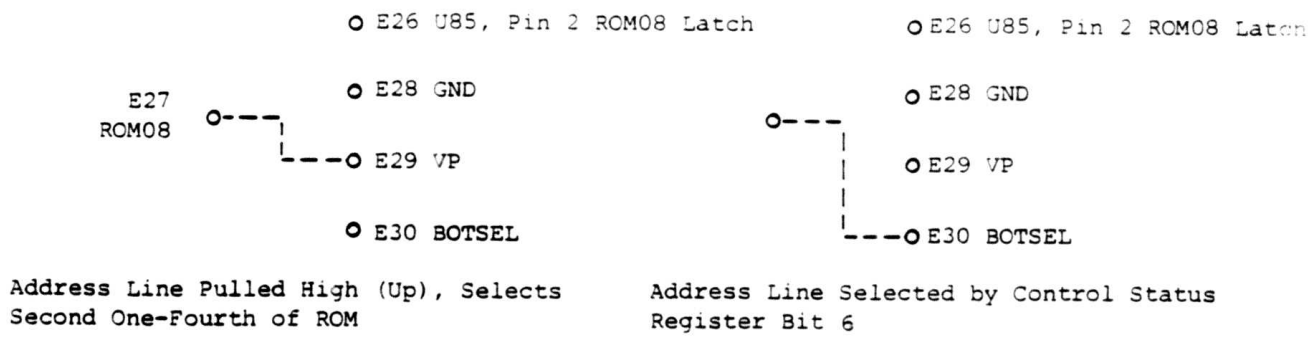
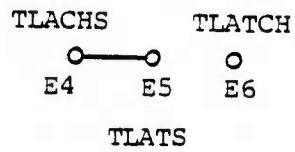


Figure 4-12



Production Use Only

Figure 4-13

○ E31 WRDOUT

Signal Deleted but Available for Use

J2 layer 6, pins 26, 27, 28, and 29 are not attached directly to the ground plane, but are available for use when trace is cut. Used as extra signal lines on external bus.

Figure 4-14

CHAPTER 5

5.0 DRAWINGS, PARTS LIST, AND SCHEMATICS

<u>Drawing Number</u>	<u>Revision Level</u>	<u>Date</u>	<u>Drawing Title</u>
8100133 (4 sheets)	2	--	P.C. Assembly Robustness II Module
2600466 (6 sheets)	6	--	Logic Diagram Robustness II Module

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 ADMINISTRATION POLICY AND
 PROCEDURES. FOR INFORMATION
 CONTACT THE NATIONAL ARCHIVES
 AT COLLEGE PARK, MARYLAND
 20740-6001

ITEM NO.	QTY	PCB NO.	PART OR IDENTIFYING NO.	MANUFACTURER OR DESCRIPTION
44	1		6800098	PC BOARD ROBUSTNESS II
43	70		0000246	PWR AND GND CLIPS
42	110		0600011	WIRE WRAP STAKES
41	1		5400000	DEC PRGRM TRANS INTC DCKII
40	2		0500014	SWITCH DIP 8 POS 74K5B085
39	1		0300080	SOCKET 8 PIN DIP DIL B08P108
38	2		0300053	CONNECTOR 40PIN RT ANGLE
37	1		0700176	CAP CER 2700pf
36	1		0700175	CAP CER .0022nf
35	1		0700174	CAP CER .47uf
ITEM NO.	QTY	PCB NO.	PART OR IDENTIFYING NO.	MANUFACTURER OR DESCRIPTION

PARTS LIST

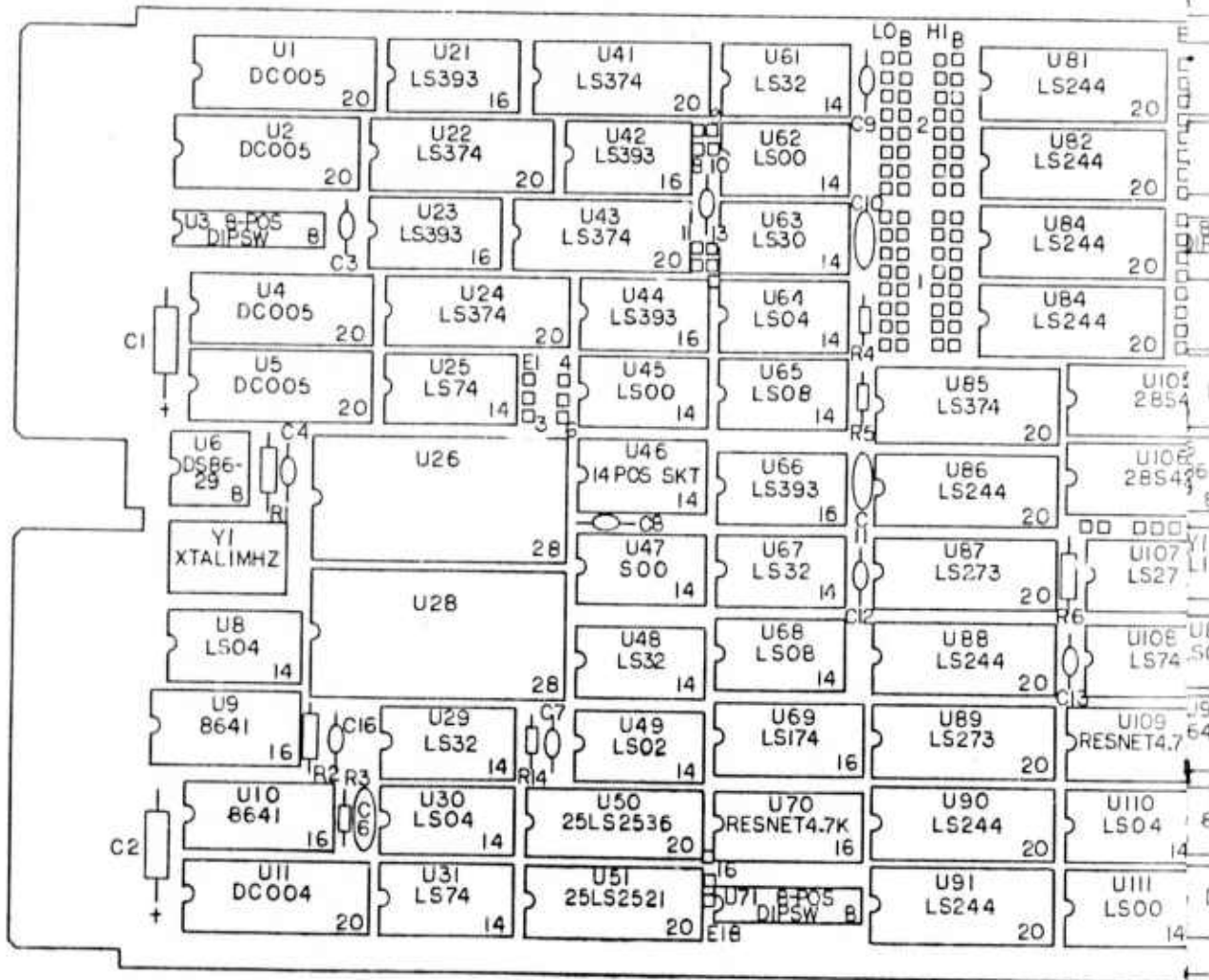
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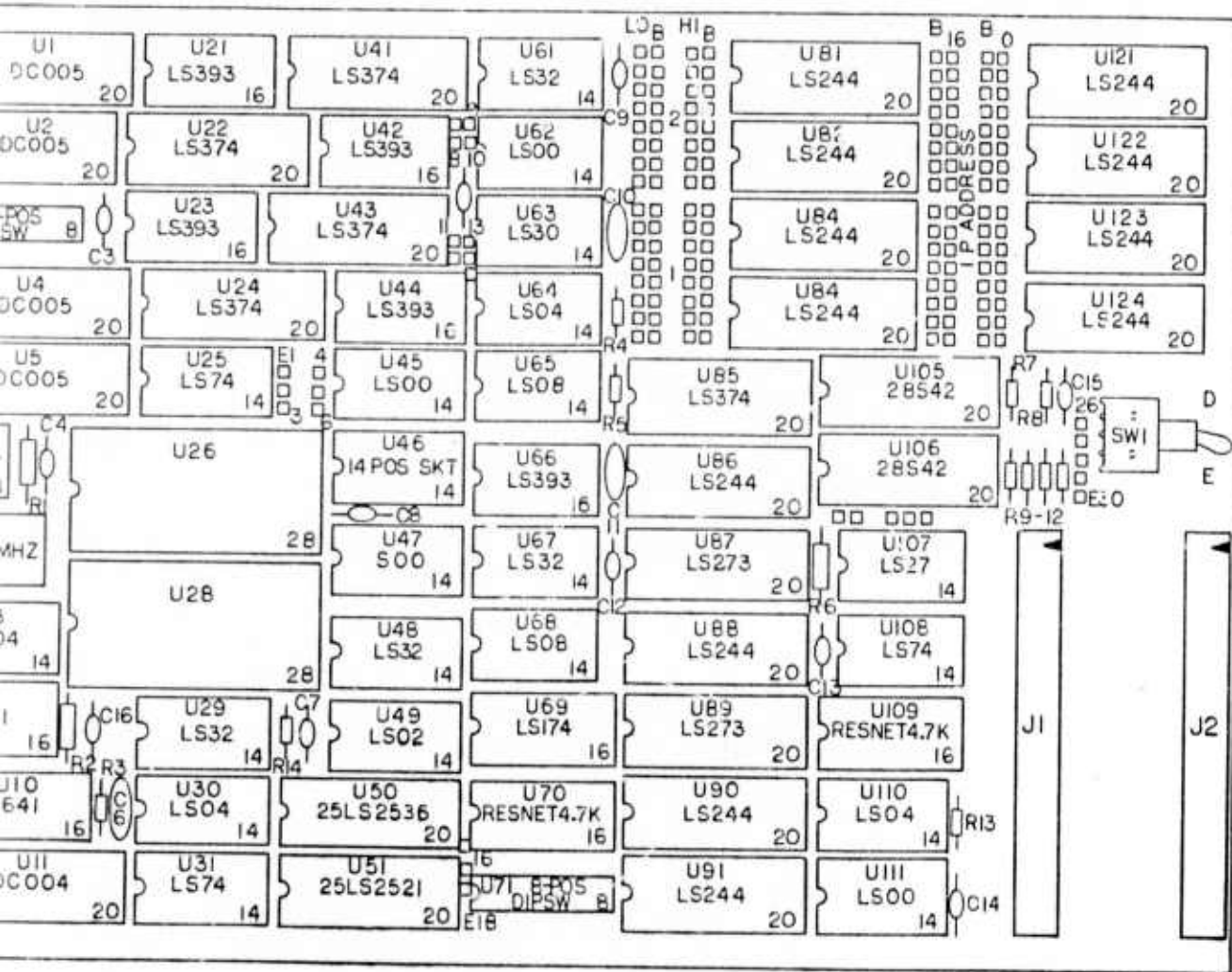
D

C

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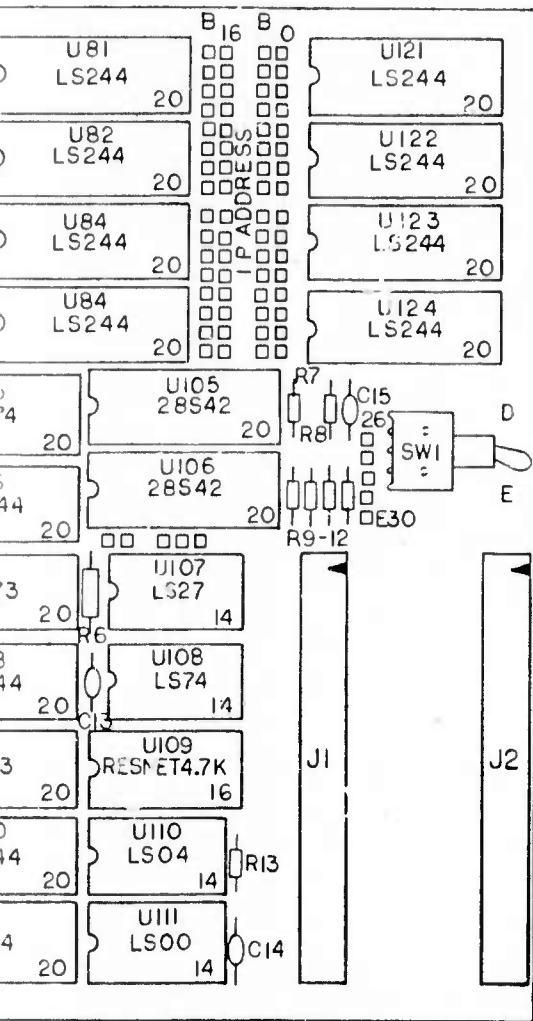
ITEM NO.	QTY REQD	FROM NO.	PART OR IDENTIFYING NO.	CONTRACT NO.
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE:				APPROVALS
FRACTIONS DECIMALS ANGLES				
MATERIAL				DRAWN <i>W. Midtall</i> 29
FINISH				CHECKED <i>R. Loper</i> 12
NEXT ASSY		USED ON		ISSUED
APPLICATION			DO NOT SCALE DRAWING	

DWG NO. 8100133

REV 2 2

1

REVISIONS			
ZONE	REV	DESCRIPTION	DATE
		SEE SHT 1	



8100133 REV 2 2

PC ASSEMBLY

ITEM NO.	QTY	FRGM REGD NO	FRGM NO	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATER. SPECIFICATION
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .XX .XXX						
MATERIAL			CONTRACT NO.		PARTS LIST	
FINISH			APPROVALS		DATE	
NEXT ASBY			DRAWN		12/1/87	
USED ON			CHECKED		12/1/87	
APPLICATION			ISSUED		SCALE: NONE	
DO NOT SCALE DRAWING			(A)		SHEET 2 OF 4	

ACC ASSOCIATED COMPUTER CONSULTANTS
Santa Barbara, California 93101

PC ASSY
ROBUSTNESS II

SIZE: D FRGM NO: 61550 DWG NO: 8100133 REV: 2

4

3

2

1

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B

7

6

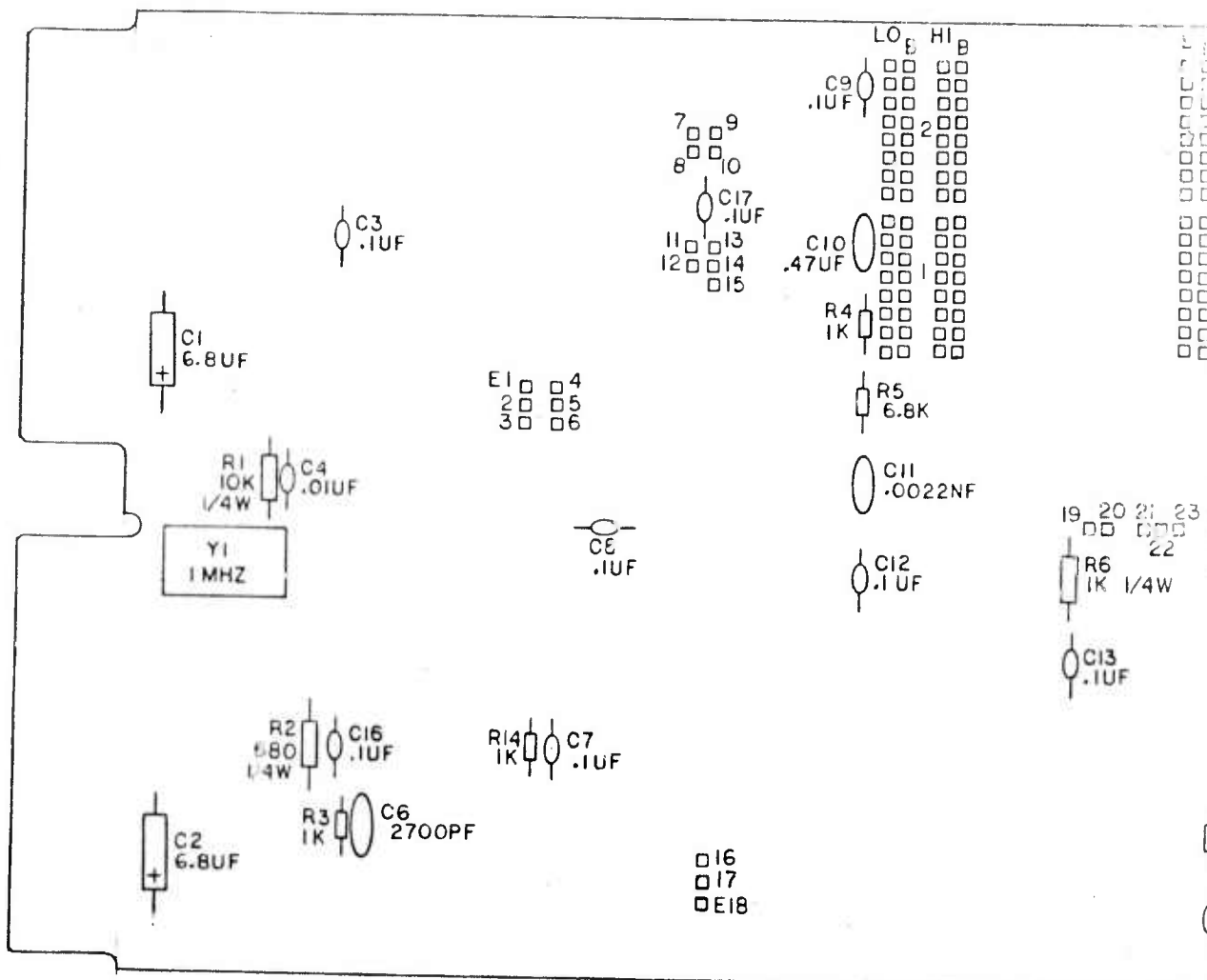
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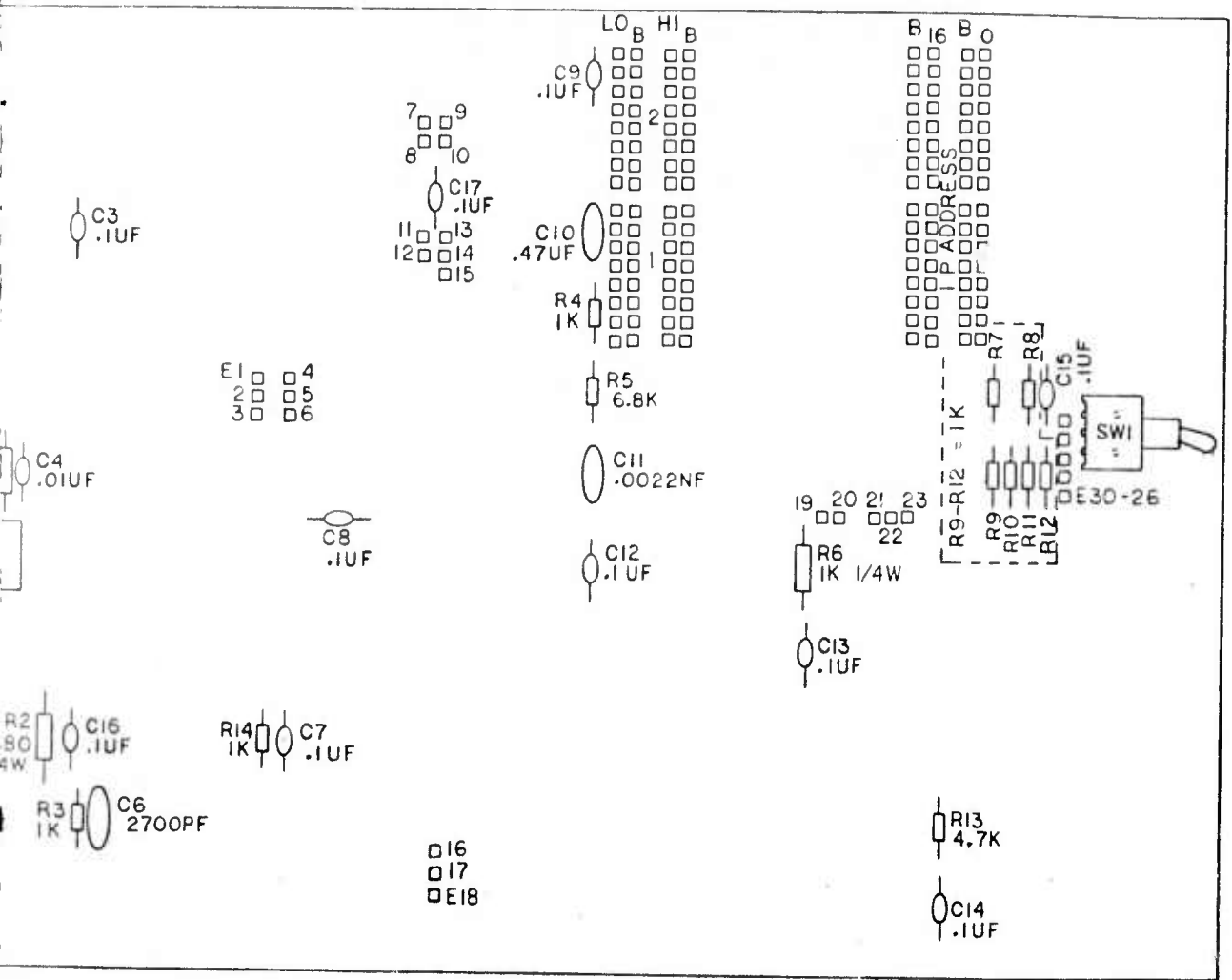
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C

B

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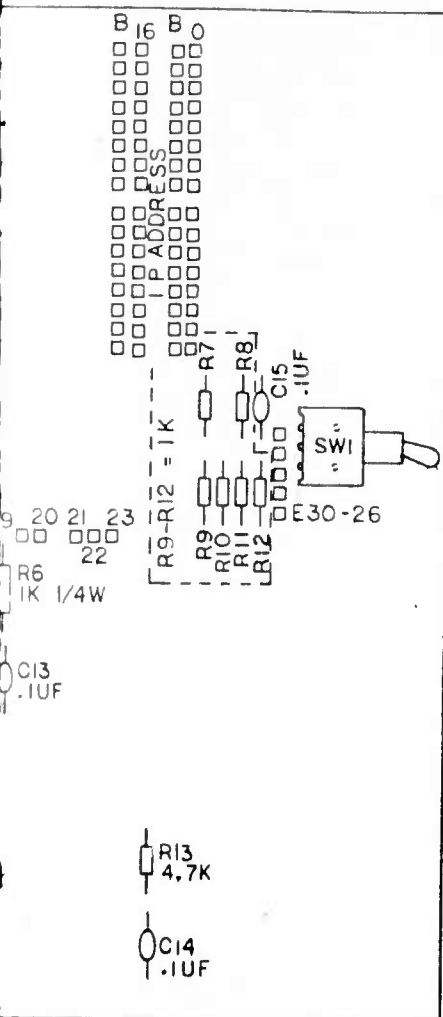




W/W POS

ITEM NO.	QTY REQD.	FORM NO.	PART OR IDENTIFYING NO.	CONTRACT NO.
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE FRACTIONS DECIMALS ANGLES .XX.X .XXX.X .XXX.X				APPROVALS
MATERIAL				DRAWN <i>M. Loper</i>
FINISH				CHECKED <i>M. Loper</i>
NEXT ASSY USED ON				ISSUED
APPLICATION				DO NOT SCALE DRAWING

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED
		SEE SH1		



D

C

REV 3 2

DWG NO 8100133

FAB GUIDE
W/W POSTS-DISCRETES-XTAL-SWITCH

ITEM NO	QTY REQD	PBCM NO	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION	MATERIAL SPECIFICATION
PARTS LIST					
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .XXX°			CONTRACT NO. ACC ASSOCIATED COMPUTER CONSULTANTS Santa Barbara, California 93101		
MATERIAL		APPROVALS		DATE	
FINISH		DRAWN		11/19/82	
NEXT ASSY		CHECKED		11/19/82	
USED ON		ISSUED			
APPLICATION		DO NOT SCALE DRAWING		SIZE D PBCM NO. 61550 DWG. NO. 8100133 REV. 2	
				SCALE 2:1 SHEET 3 OF 4	

A

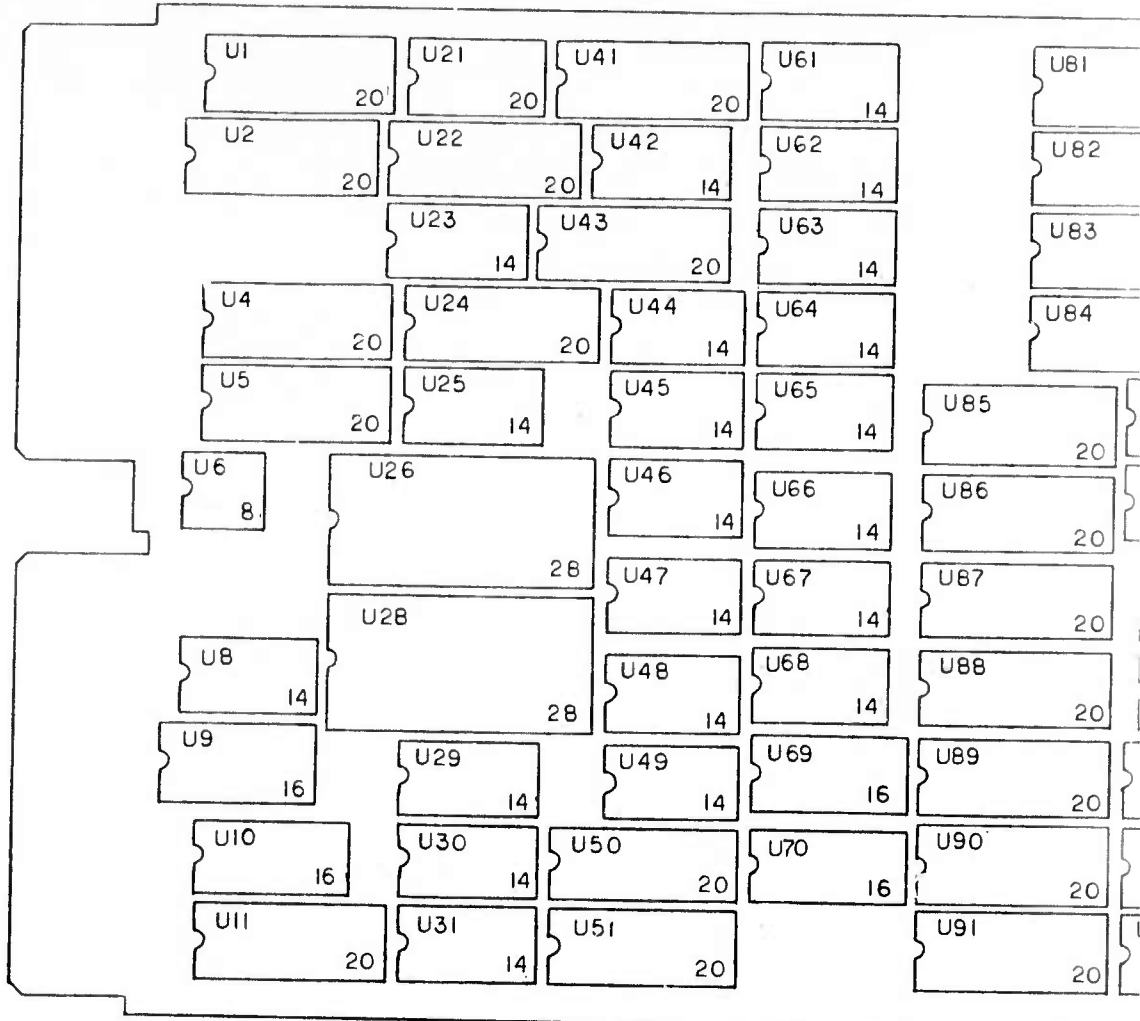
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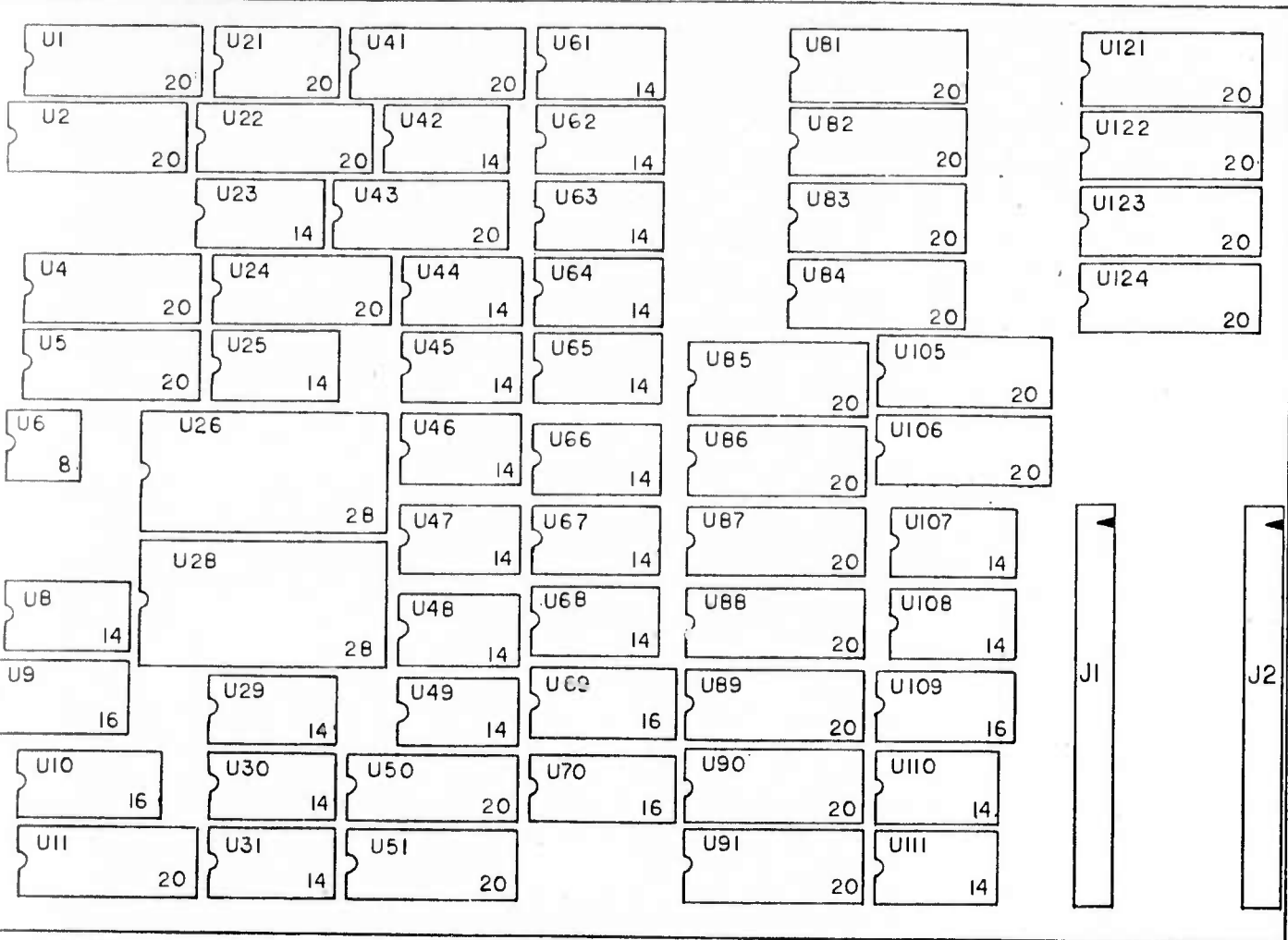
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SO

ITEM NO.	QTY REQD.	PCOM NO.	PART OR IDENTIFYING NO.	CONTRACT NO.
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .001 .001 .001				
MATERIAL				APPROVALS
FINISH				DRAWN <i>Middell</i> 2/2/20
NEXT ASSEMBLY USED ON				CHECKED <i>M/OPEN</i> 12/11
APPLICATION				ISSUED
DO NOT SCALE DRAWING				(A)

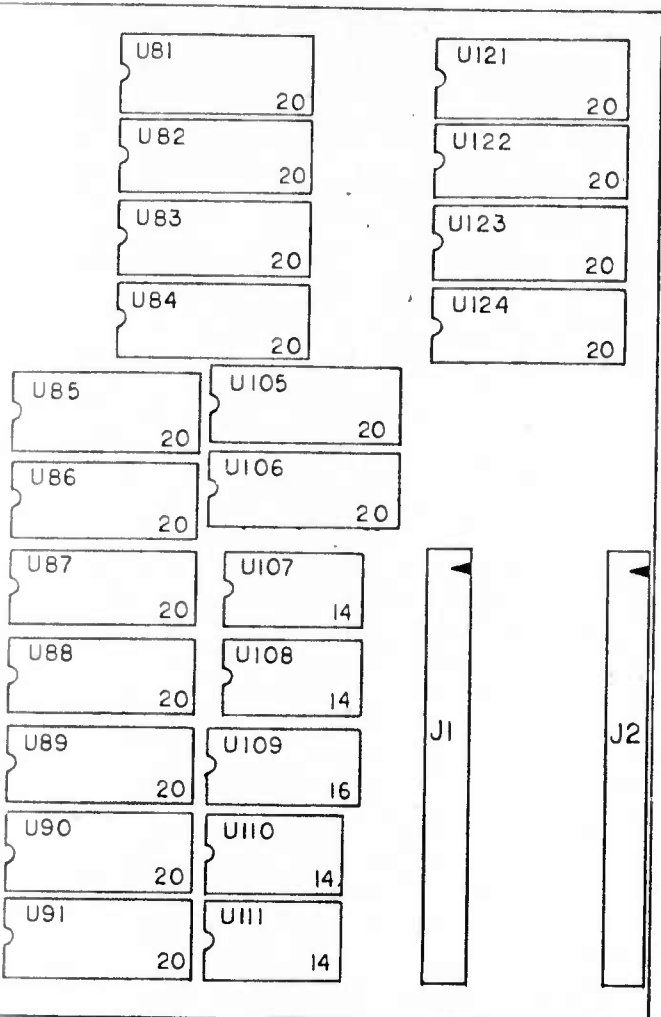
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3

DWG NO. 8100133 SH 4 REV 2

1

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED
		SEE SHT 1		



FAB GUIDE
SOCKET-CONNECTORS

ITEM NO.	QTY REQD.	FRGM NO.	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL SPECIFICATION
PARTS LIST					
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES ' .XX' .XXX "			CONTRACT NO.		
MATERIAL			APPROVALS DATE		
FINISH			DRAWN <i>Middell</i> 2/24/82		
NEXT ASSY USED ON			CHECKED <i>M/LOPER</i> 12/1/82		
APPLICATION			ISSUED		
DO NOT SCALE DRAWING			SCALE 2/1		
			SIZE FRGM NO. DWG. NO. REV		
			D 61550 8100133 2		
			SHEET 4 OF 4		

DWG NO. 8100133 SH 4 REV 2

4

3

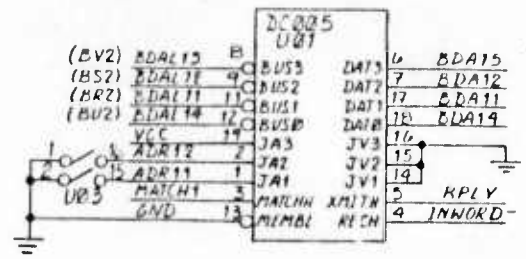
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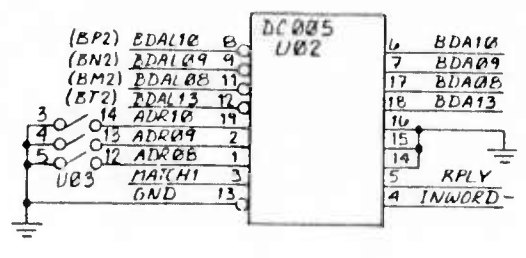
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REGISTER SELECT

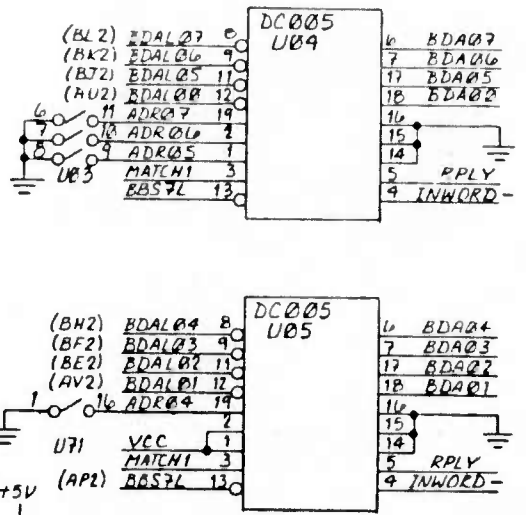
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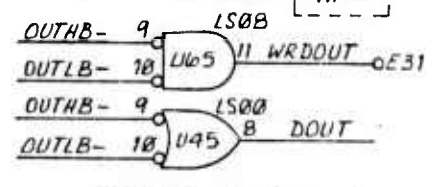
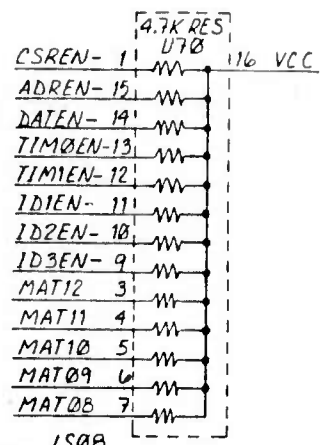
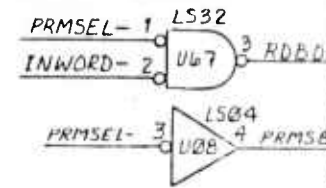
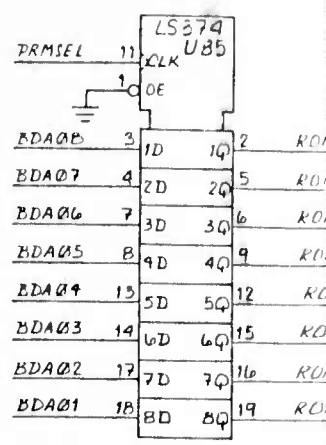
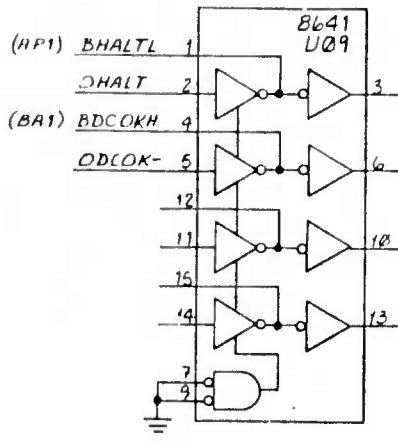
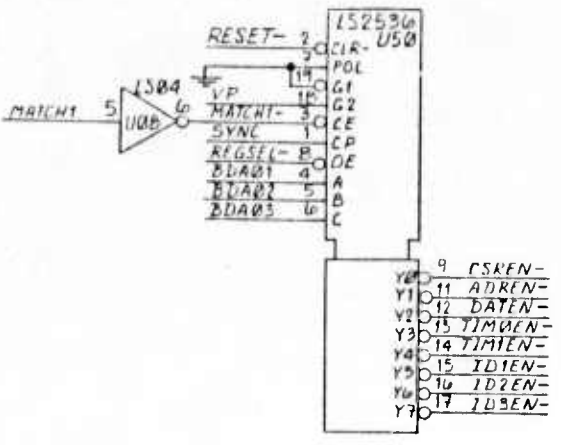
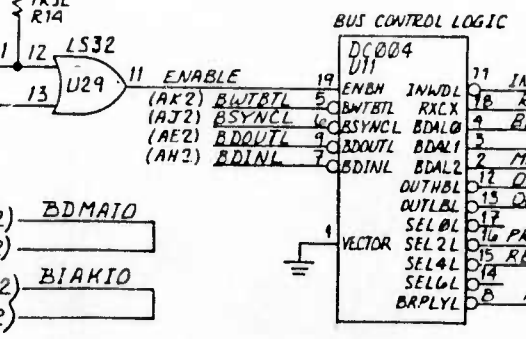
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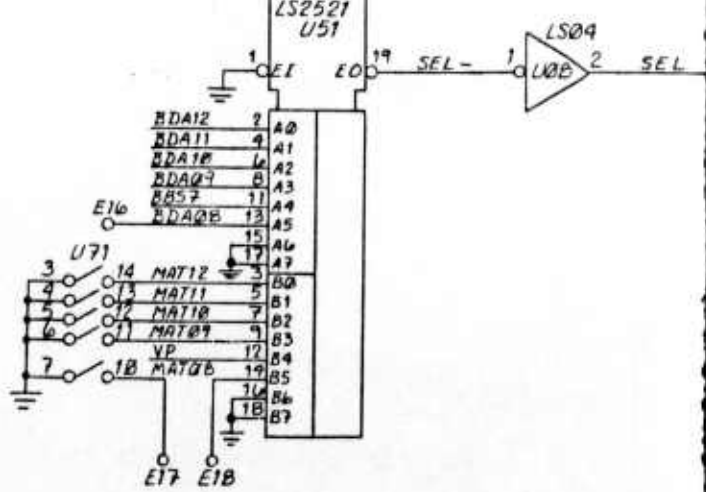
B



A



BOOT SELECT (DECODE)

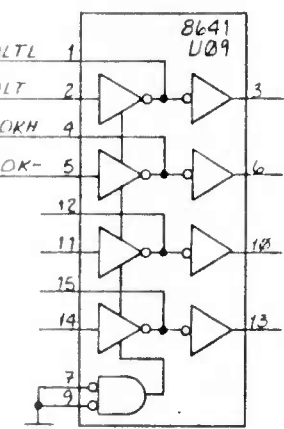
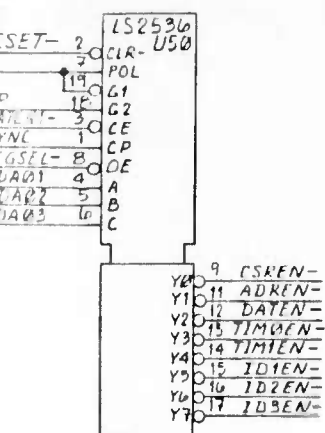


LAST REF DES	
C 17	R 14
CR	U124
E 31	VR
J 2	Y 1

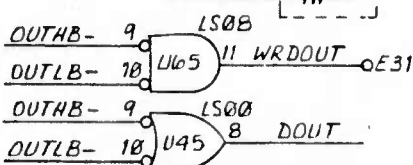
- 6. USE CIRCUIT BOARD ACC NO. 6800098 REV. B
 - 7. FOR WIRE-WRAP VERSION SEE ACC NO. _____
 - 4. FOR ASSEMBLY DRAWING SEE ACC NO. 6100133
 - 8. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
 - 1. ALL RESISTANCE VALUES ARE IN OHMS, 25% 1/4W.
- NOTES: UNLESS OTHERWISE SPECIFIED

ZONE	REV	DESCRIPTION
1		PRELIMINARY
2		PRELIM
3		PRELIMINARY CHG.D.
4		PRELIM
5		PRELIM
6		PRELIM

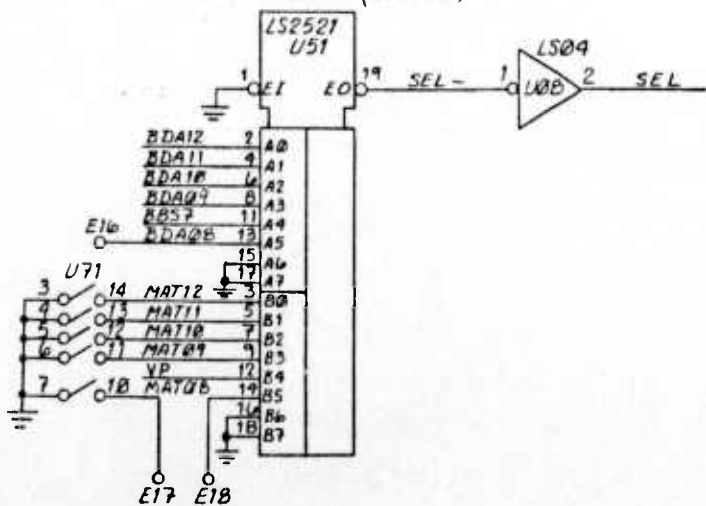
REGISTER SELECT



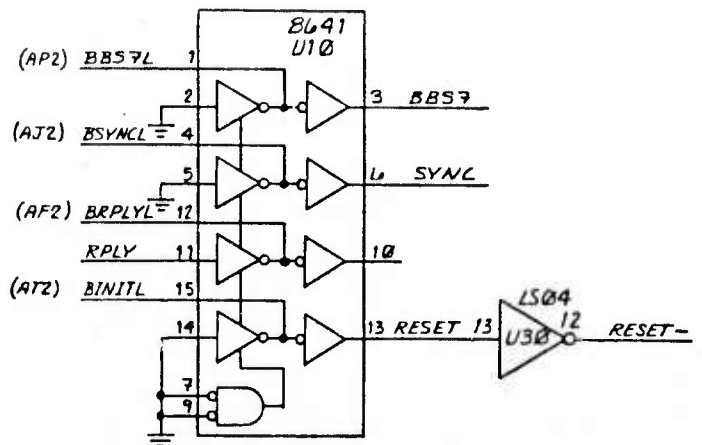
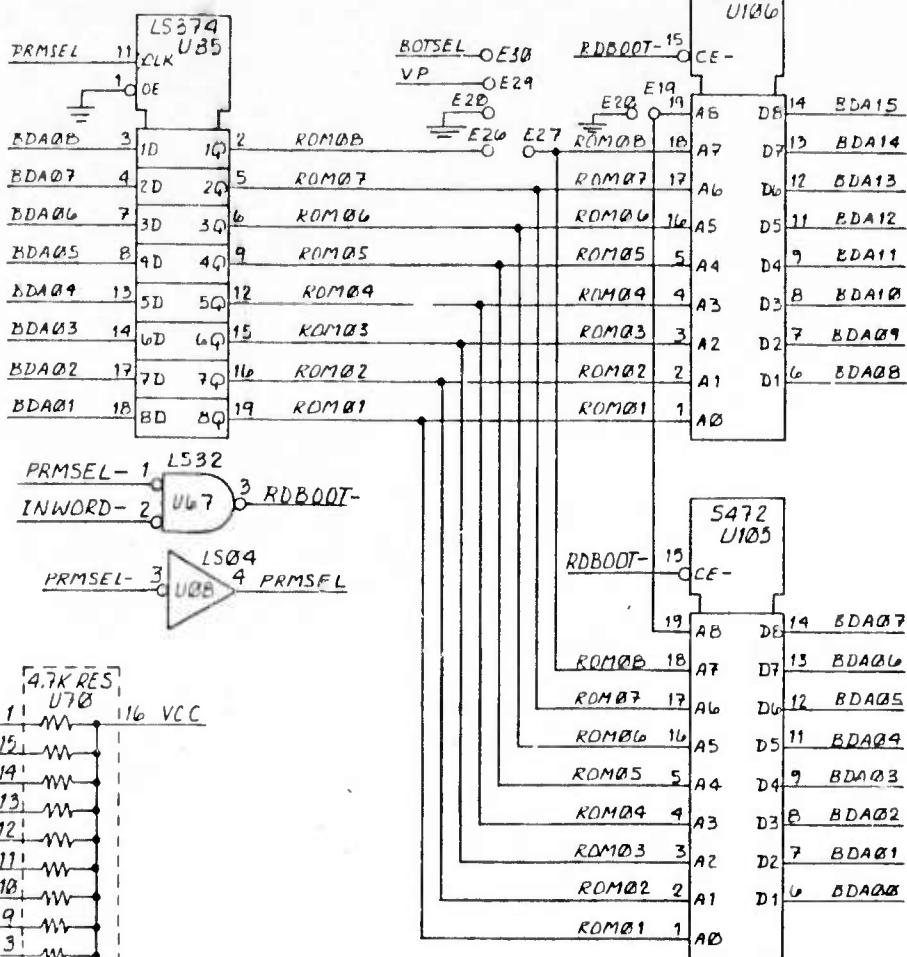
RL6
VP
IKR
U41



BOOT SELECT (DECODE)



BOOT ROMS



BUS INTERFACE, SELECTION LOGIC

ITEM NO.	QTY REQD.	FCM NO.	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .XX .XXX				
MATERIAL			CONTRACT NO.	
FINISH			APPROVALS DATE	
NEXT ASSY			DRAWN WEDDELL 2-4-82	
USED ON			CHECKED M/... 10/4/82	
APPLICATION			ISSUED	
DO NOT SCALE DRAWING			SIZE FCM NO. D 61550	
			SCALE NONE	

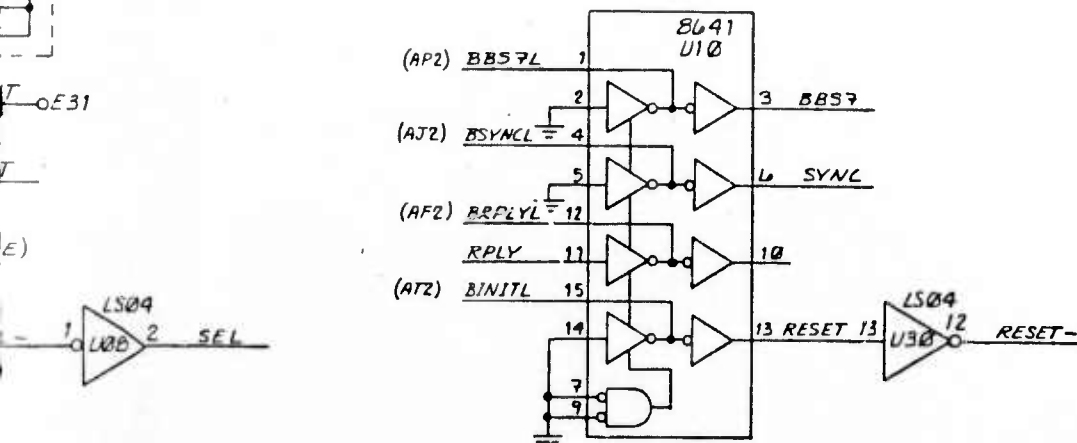
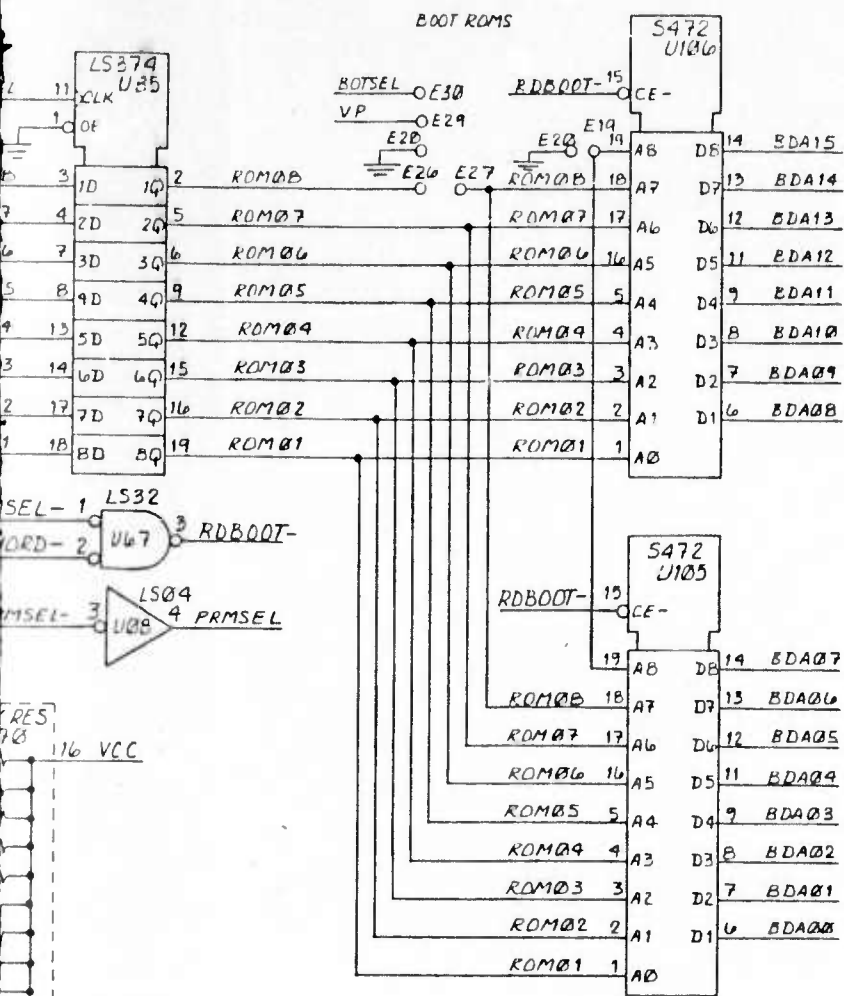
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3

2600466

1

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED
	1	PRELIMINARY	2-18-82	
	2	PRELIM.	3-22-82	
	3	PRELIMINARY CHGD. SMTS. 1	5-24-82	
	4	PRELIM.	7-16-82	ML
	5	PRELIM	9-24-82	ML
	6	PRELIM	11-22-82	ML



BUS INTERFACE, SELECTION LOGIC, BOOT PROM

ITEM NO.	QTY	FRGM	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL SPECIFICATION
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES : .XXX : 2					
MATERIAL			CONTRACT NO.		
FINISH			APPROVALS		
NEXT ASSY			DATE		
USED ON			DRAWN WEDDELL 2-4-82		
APPLICATION			CHECKED M/... 10/4/82		
DO NOT SCALE DRAWING			ISSUED		
			SIZE FRGM NO. DWG. NO. 2600466 REV 6		
			SCALE NONE SHEET 1 OF 6		

4

3

2

1

Dwg No 2600466

A

D

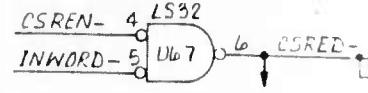
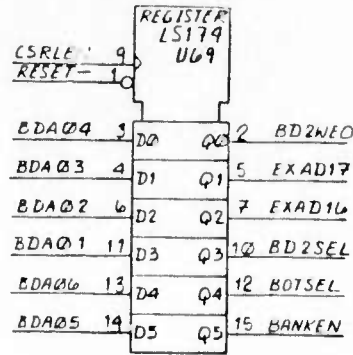
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B

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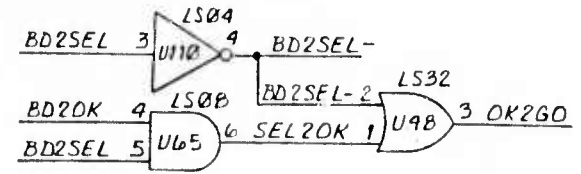
8 7 6 5

D



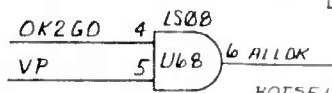
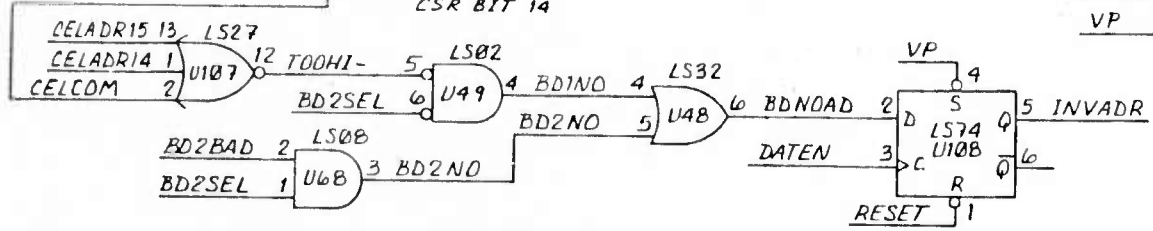
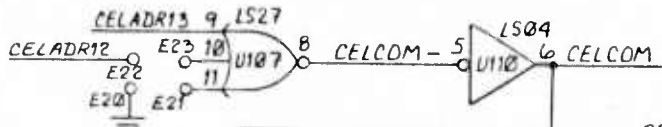
ERROR
INVADR
NONWEN
NONWRT

DISABL-
BD2CW
BD2IS



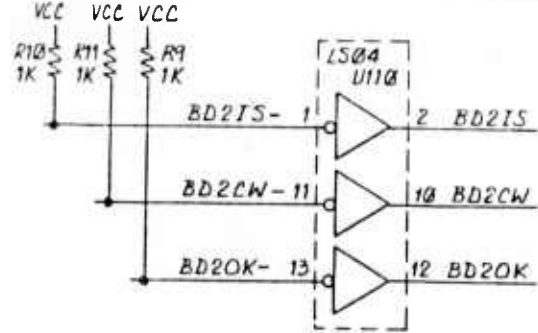
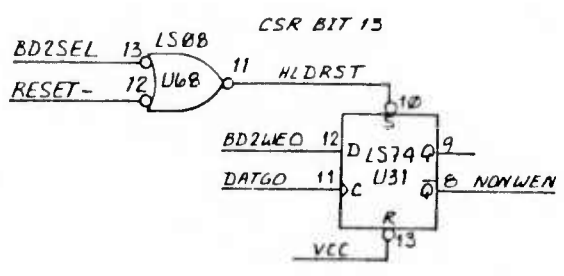
CSRED-

C



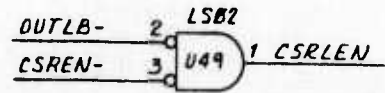
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ALLDK
HOTSEL
BANKEN
BD2WEO
EXAD17
EXAD16
BD2SEL

B

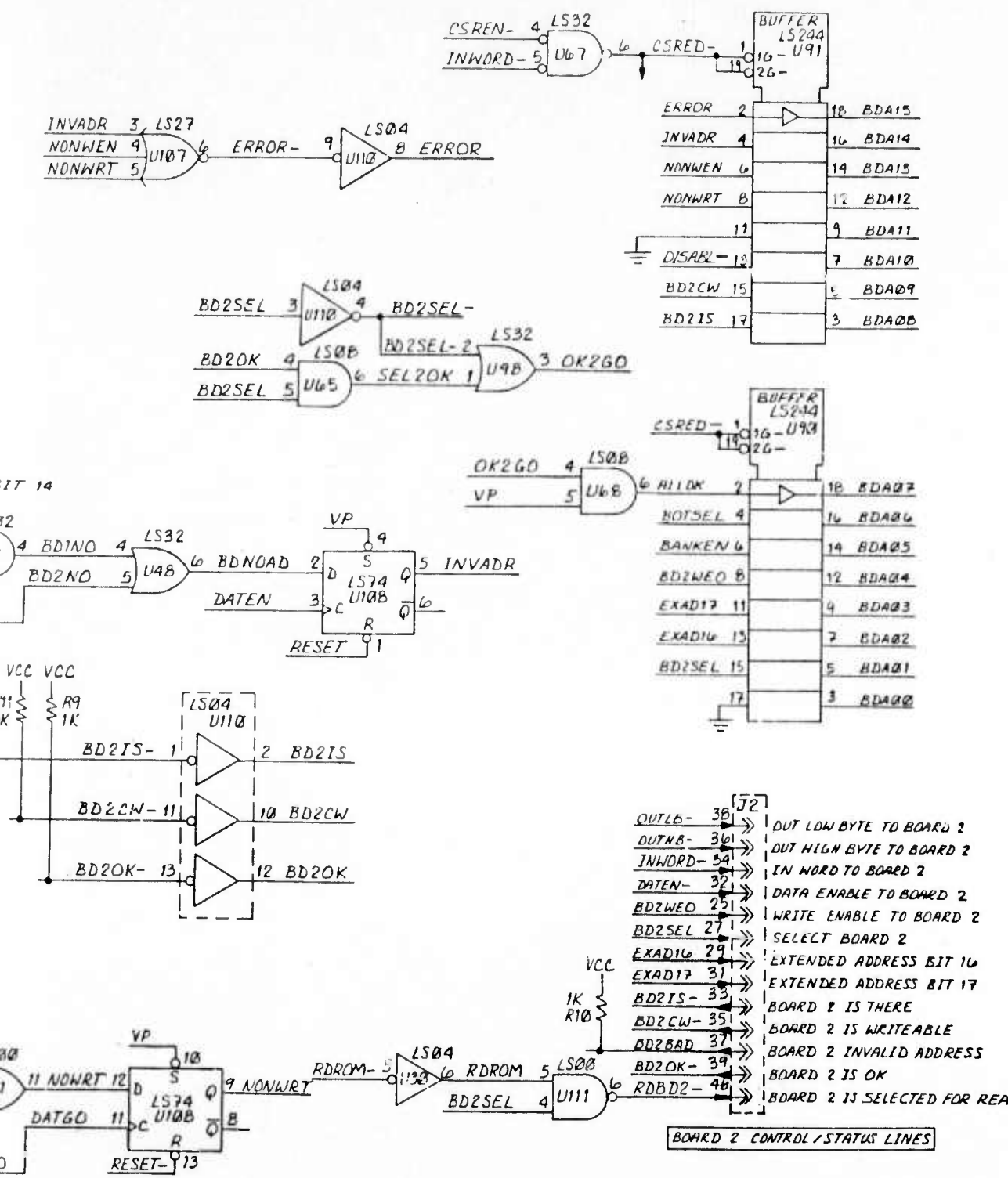


OUTLB- 38
OUTWA- 36
INWORD- 54
DATEN- 32
BD2WEO 25
BD2SEL 27
EXAD16 29
EXAD17 31
BD2IS- 35
BD2CW- 35
BD2BAD 37
BD2OK- 39
RDBD2- 40

A



8 7 6 5



BOARD 2 ADDRESS LINES

- CELADR15 1 [J1]
- CELADR14 3 [J1]
- CELADR13 5 [J1]
- CELADR12 7 [J1]
- CELADR11 9 [J1]
- CELADR10 11 [J1]
- CELADR09 13 [J1]
- CELADR08 15 [J1]
- CELADR07 17 [J1]
- CELADR06 19 [J1]
- CELADR05 21 [J1]
- CELADR04 23 [J1]
- CELADR03 25 [J1]
- CELADR02 27 [J1]
- CELADR01 29 [J1]
- CELADR00 31 [J1]
- BDA15 33 [J1]
- BDA14 35 [J1]
- BDA13 37 [J1]
- BDA12 39 [J1]

ALL ARE

- OUTLB- 38 [J2] OUT LOW BYTE TO BOARD 2
- OUTHB- 36 [J2] OUT HIGH BYTE TO BOARD 2
- INWORD- 34 [J2] IN WORD TO BOARD 2
- DATEN- 32 [J2] DATA ENABLE TO BOARD 2
- BD2WEO 29 [J2] WRITE ENABLE TO BOARD 2
- BD2SEL 27 [J2] SELECT BOARD 2
- EXAD16 29 [J2] EXTENDED ADDRESS BIT 16
- EXAD17 31 [J2] EXTENDED ADDRESS BIT 17
- BD2TS- 33 [J2] BOARD 2 IS THERE
- BD2CW- 35 [J2] BOARD 2 IS WRITEABLE
- BD2BAD 37 [J2] BOARD 2 INVALID ADDRESS
- BD2OK- 39 [J2] BOARD 2 IS OK
- RDBD2- 40 [J2] BOARD 2 IS SELECTED FOR READ

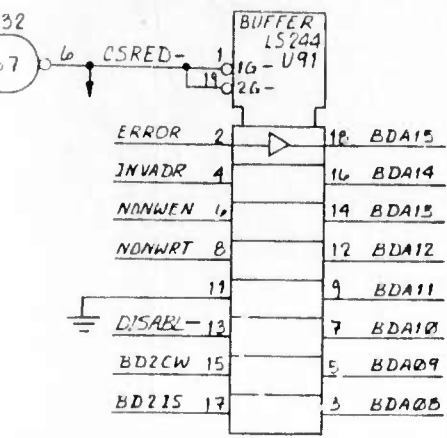
BOARD 2 CONTROL/STATUS LINES

- BDA11 1 [J2]
- BDA18 3 [J2]
- BDA09 5 [J2]
- BDA08 7 [J2]
- BDA07 9 [J2]
- BDA06 11 [J2]
- BDA05 13 [J2]
- BDA04 15 [J2]
- BDA03 17 [J2]
- BDA02 19 [J2]
- BDA01 21 [J2]
- BDA00 23 [J2]

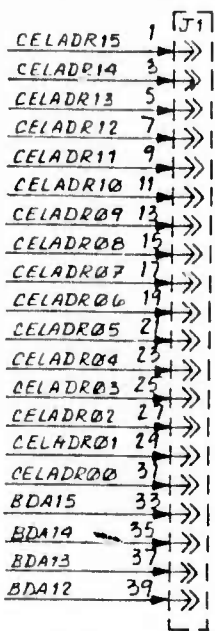
BOARD 2 DATA LINES

CO AND EX

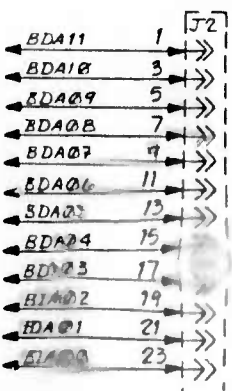
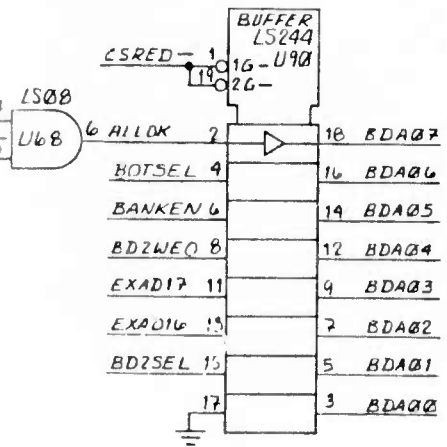
ITEM NO	QTY REQD	PRCN NO	PART OR IDENTIFYING NO	PART
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .XXX .				
MATERIAL			APPROVALS	DATE
FINISH			DRAWN	10/4/82
NEXT FABY			CHECKED	10/4/82
USED ON			ISSUED	
APPLICATION			DO NOT SCALE DRAWING	



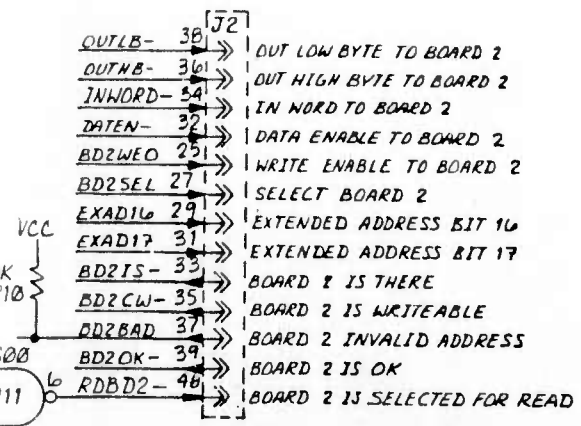
BOARD 2 ADDRESS LINES



ALL UNMARKED PINS ON J1 AND J2 ARE TO GND



BOARD 2 DATA LINES



BOARD 2 CONTROL/STATUS LINES

CONTROL STATUS REGISTER AND EXTERNAL BUS TO BD NO 2

ITEM NO	QTY REQD	FRGM NO	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION	MATERIAL SPECIFICATION
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE FRACTIONS DECIMALS ANGLES					
MATERIAL			CONTRACT NO		
FINISH			APPROVALS		
NEXT ASSY			DATE		
USED ON			DRAWN		
APPLICATION			CHECKED		
DO NOT SCALE DRAWING			ISSUED		
			SIZE		
			FRGM NO		
			DWG NO		
			REV		
			SCALE		
			SHEET		

ACC ASSOCIATED COMPUTER CONSULTANTS Santa Barbara, California 93101

LOGIC DIAGRAM ROBUSTNESS II MOD

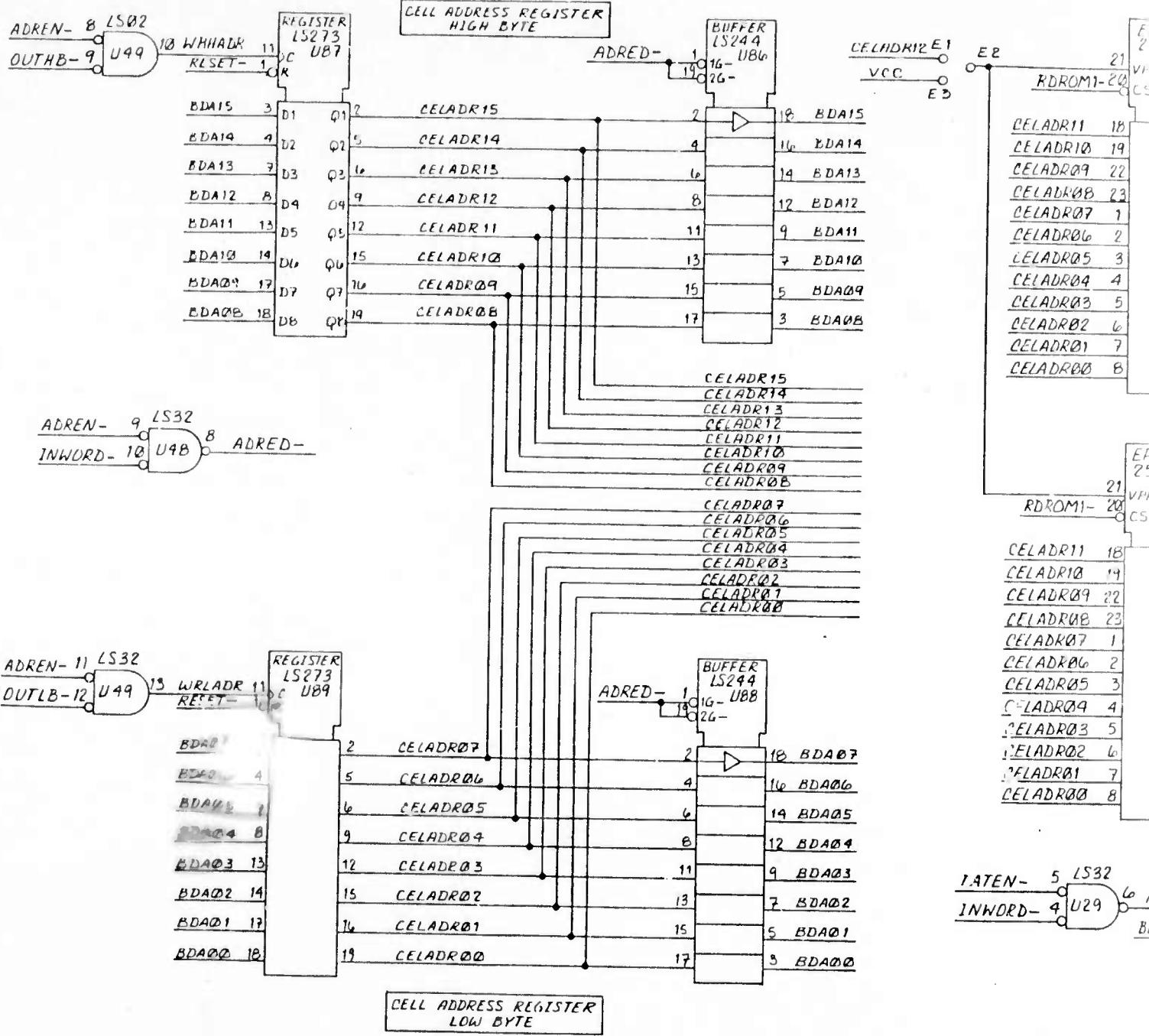
DATE: 2-9-82
DRAWN: WEDDELL
CHECKED: M. LORCH
ISSUED: 10/4/82

SIZE: D
FRGM NO: 61550
DWG NO: 2600466
REV: 6

SCALE: NONE
SHEET: 2 OF 6

DWG NO 2600466 REV 2

THIS DESIGN IS THE PROPERTY OF...
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 THIS DESIGN IS THE PROPERTY OF...
 REPRODUCED OR TRANSMITTED IN ANY FORM OR BY ANY MEANS, WITHOUT PERMISSION IN WRITING FROM THE AUTHOR.



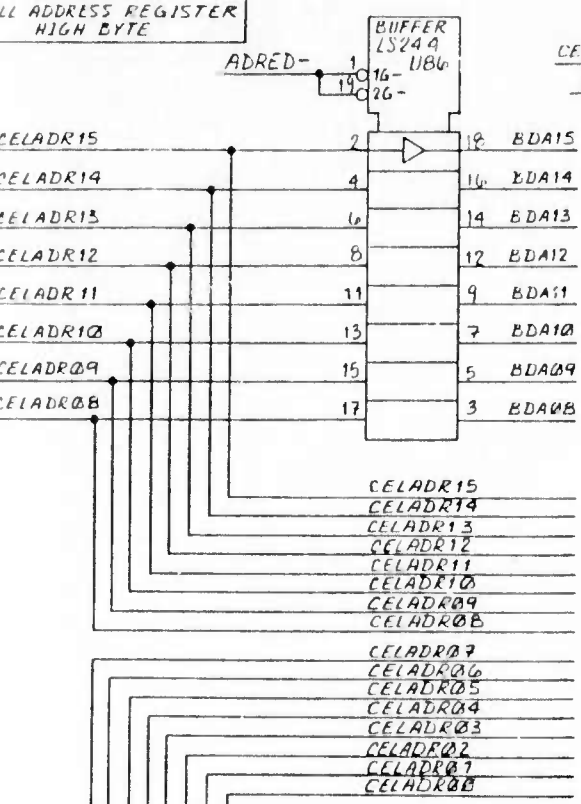
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C

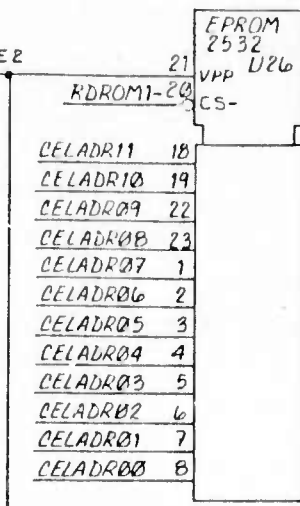
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A

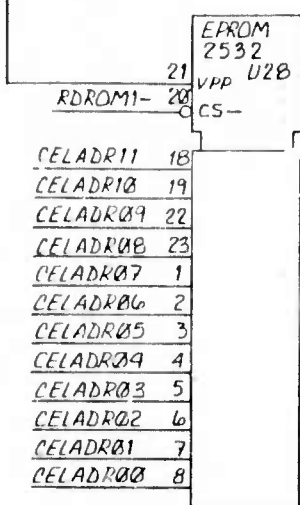
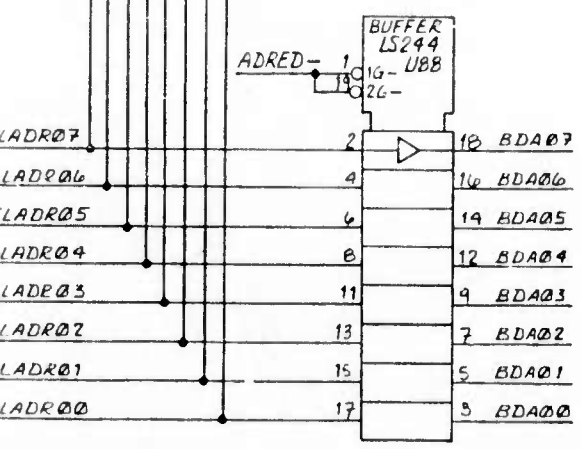
CELL ADDRESS REGISTER HIGH BYTE



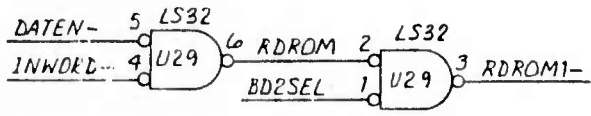
CELADR12 E1
VCC
E3



CELL DATA REGISTER HIGH BYTE



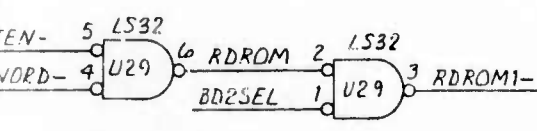
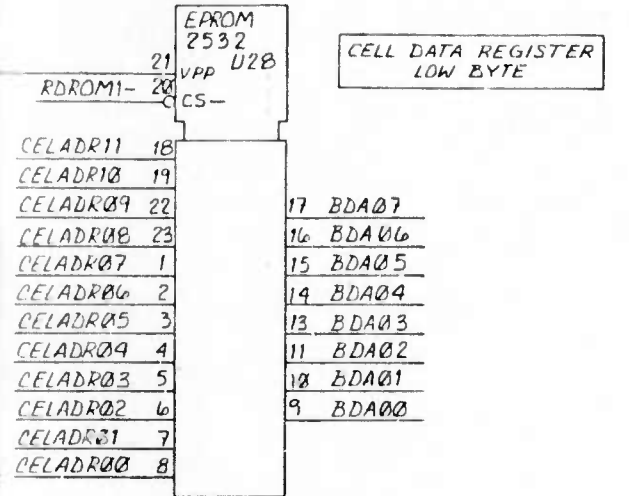
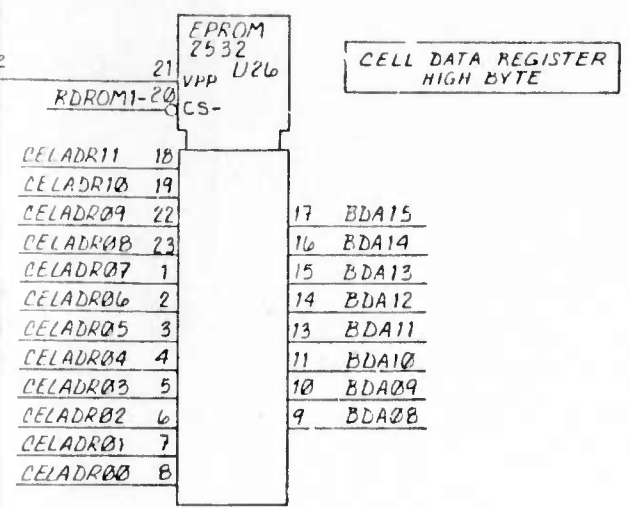
CELL DATA REGISTER LOW BYTE



CELL ADDRESS REGISTER LOW BYTE

CELL AD

ITEM NO	QTY	FROM	PART OR IDENTIFYING NO
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE:			
FRACTIONS		DECIMALS	ANGLES
CONTRACT NO			
APPROVALS			
DRAWN WEDDELL			
CHECKED M. L. ...			
ISSUED			
NEXT ASSY		USED ON	
APPLICATION		DO NOT SCALE DRAWING	



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C
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DWG NO 2600466 SH 3 OF 6

CELL ADDRESS AND DATA REGISTERS

ITEM NO	QTY REQD	FCRM NO	PART OR IDENTIFYING NO	MANUFACTURE OR DESCRIPTION	MATERIAL SPECIFICATION
PARTS LIST					
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE FRACTIONS DECIMALS ANGLES 1 .XX 1 .XXX 1 .XXX 1			CONTRACT NO		
MATERIAL			APPROVALS DATE		
FINISH			DRAWN WEDDELL 2-4-82		
NEXT ASSY USED ON			CHECKED M. L. 12/4/82		
APPLICATION			ISSUED		
DO NOT SCALE DRAWING			SIZE PCHM NO DWG NO REV D 61550 2600466 6		
			SCALE NONE SHEET 3 OF 6		

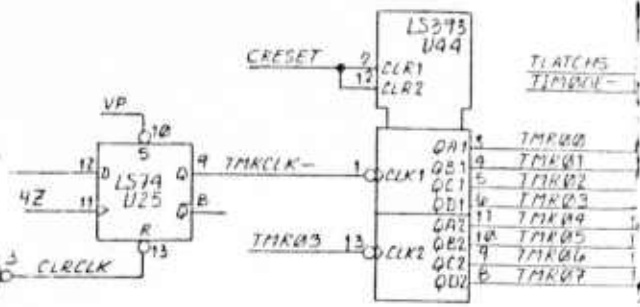
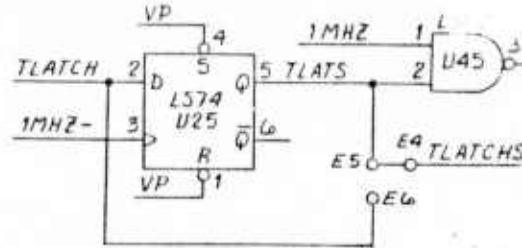
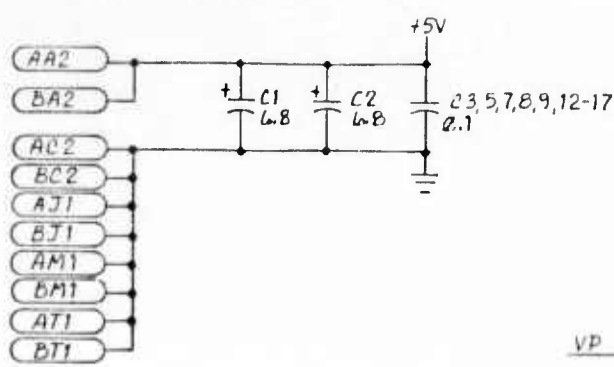
ACC ASSOCIATED COMPUTER CONSULTANTS
Santa Barbara, California 93101

LOGIC DIAGRAM
ROBUSTNESS II MOD

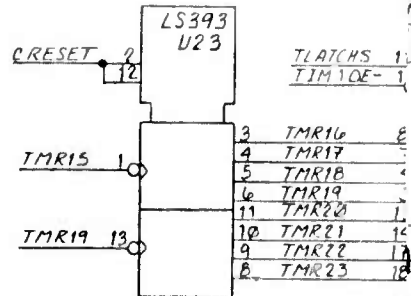
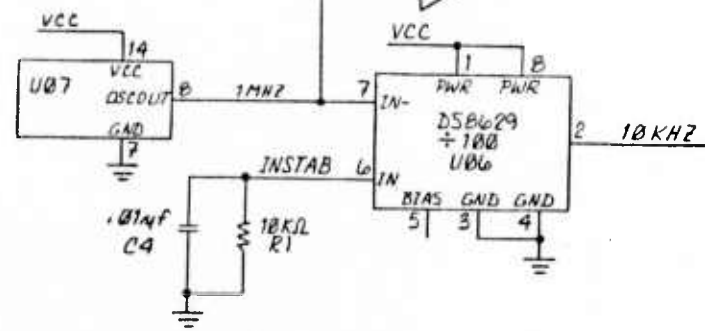
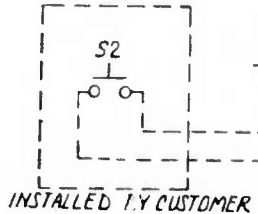
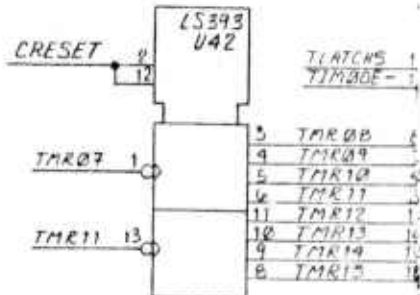
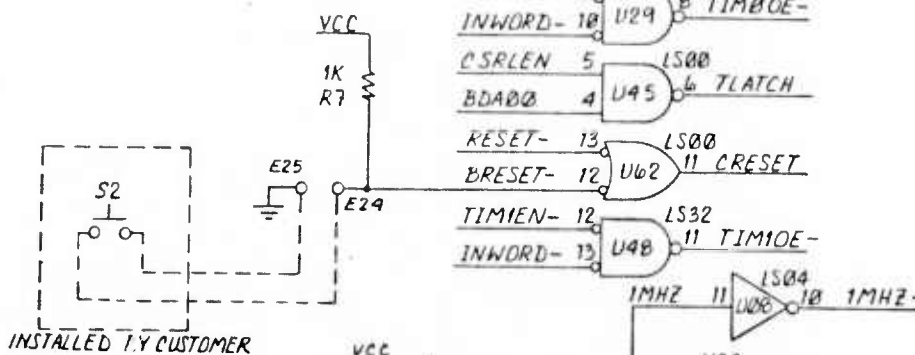
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8 7 6 5

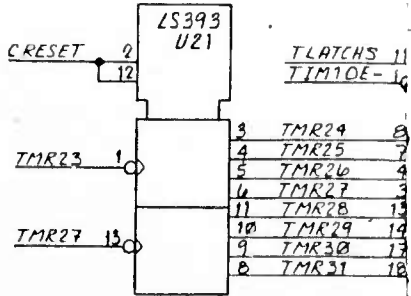
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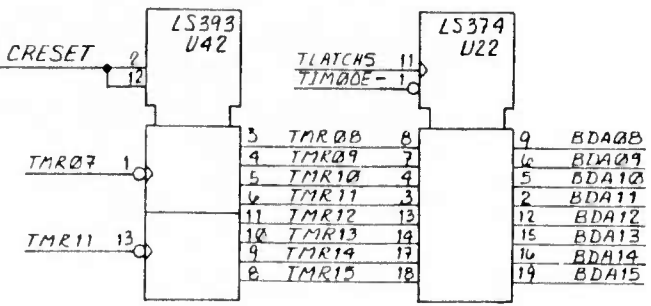
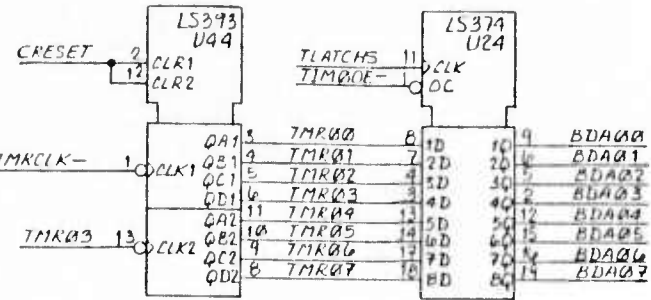
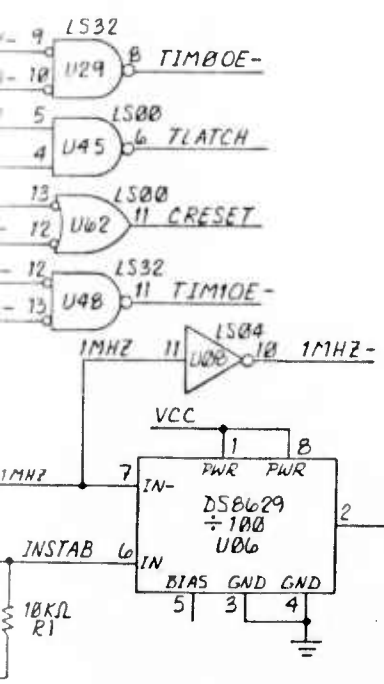
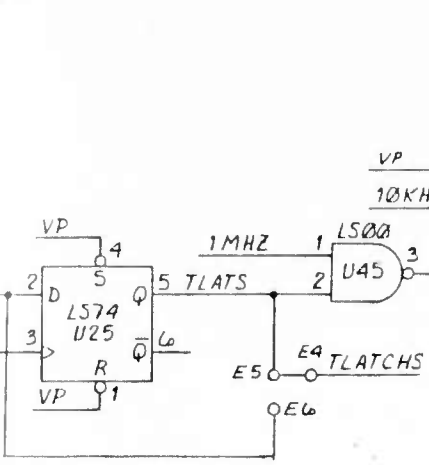
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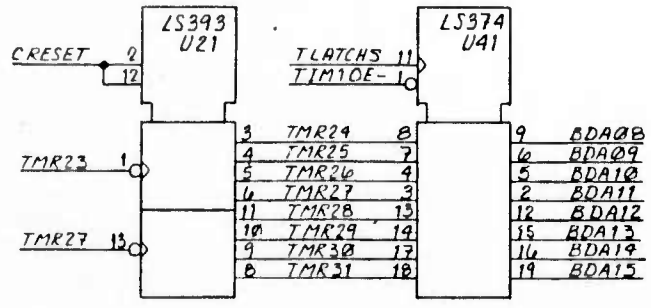
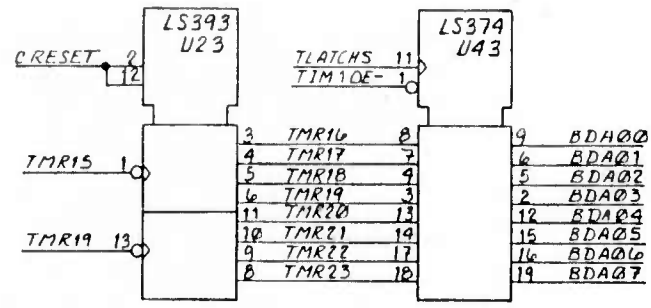
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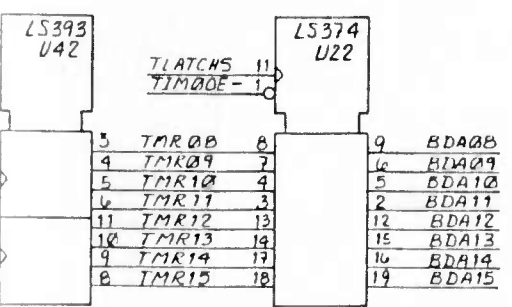
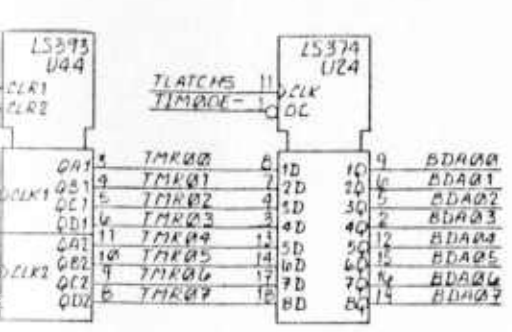


- TMR04 ○ E11
- TMR05 ○ E13
- TMR06 ○ E12
- TMR07 ○ E14
- TMR08 ○ E7
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- TMR10 ○ E8
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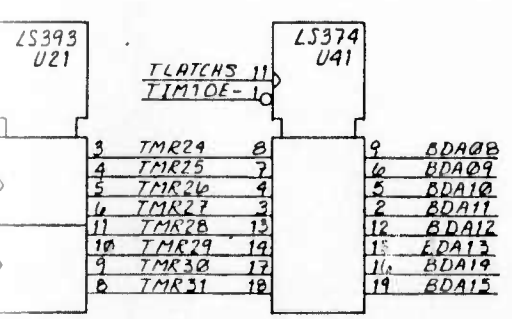
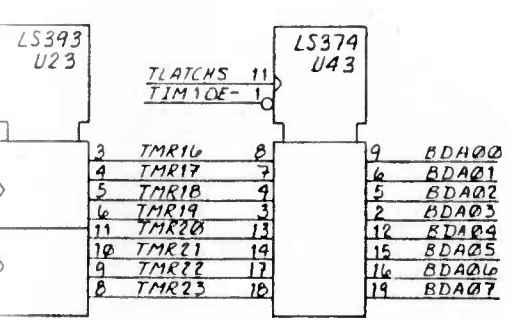


TIMER A

ITEM NO.	QTY	REQD	FSC NO.	PART OR IDENTIFYING NO.
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES				
CONTRACT NO.				
APPROVALS				
DRAWN: WEDDELL				
CHECKED: [Signature]				
ISSUED				
MATERIAL				
FINISH				
NEXT ASSY				
USED ON				
APPLICATION				
DO NOT SCALE DRAWING				



- TMR04 - E11
- TMR05 - E13
- TMR06 - E12
- TMR07 - E14
- TMR08 - E7
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- TMR10 - E8
- TMR11 - E10



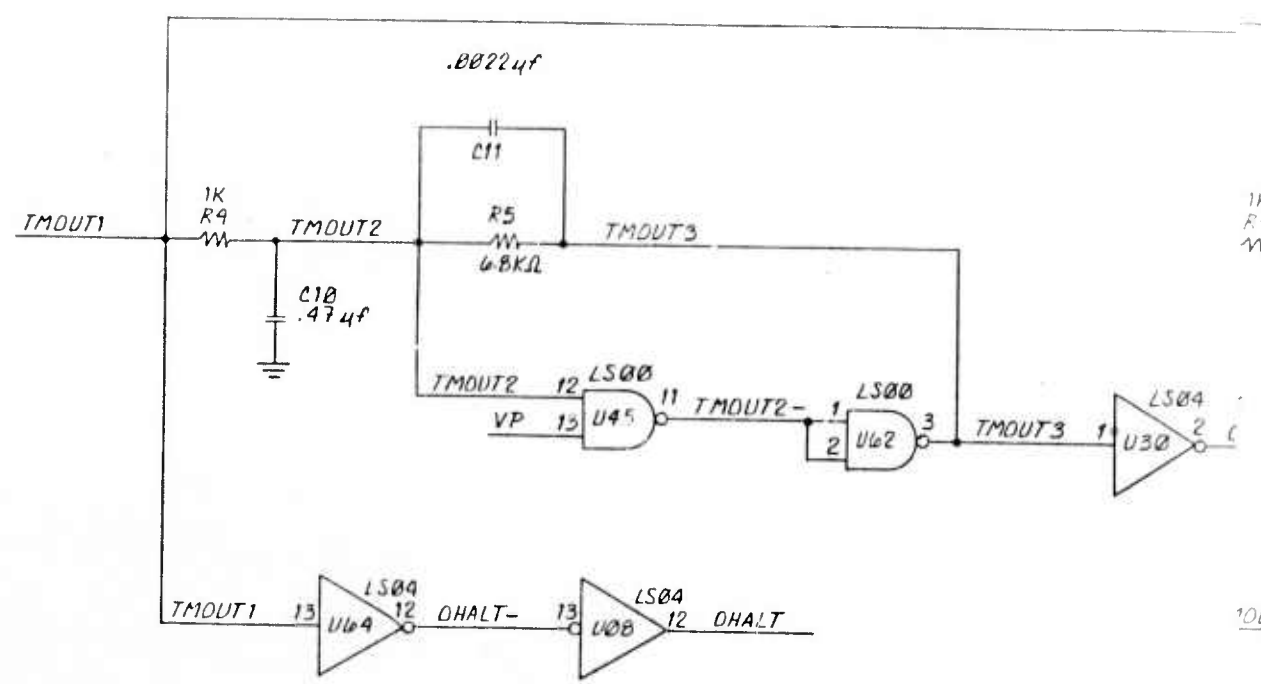
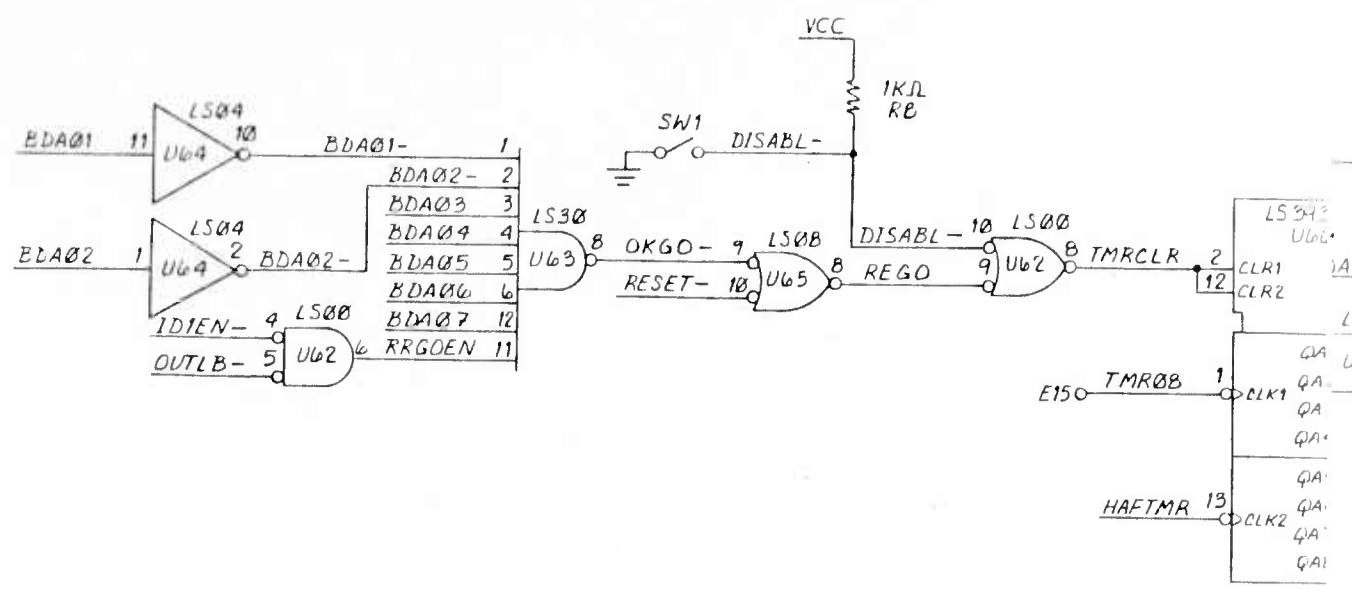
TIMER AND TIMER REGISTER I AND 2

ITEM NO	QTY	FCM NO	UNIT OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION	MATERIAL SPECIFICATION
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .XX1 .XXX1					
MATERIAL				CONTRACT NO.	
FINISH				APPROVALS	
NEXT ASSY				DATE	
USED ON				DRAWN WEDDELL 2-9-82	
APPLICATION				CHECKED M. L. 10/1/82	
DO NOT SCALE DRAWING				ISSUED	
				SCALE NONE	
				SIZE FCM NO D 61550	
				DWG. NO. 2600466	
				SHEET 4 OF 6	

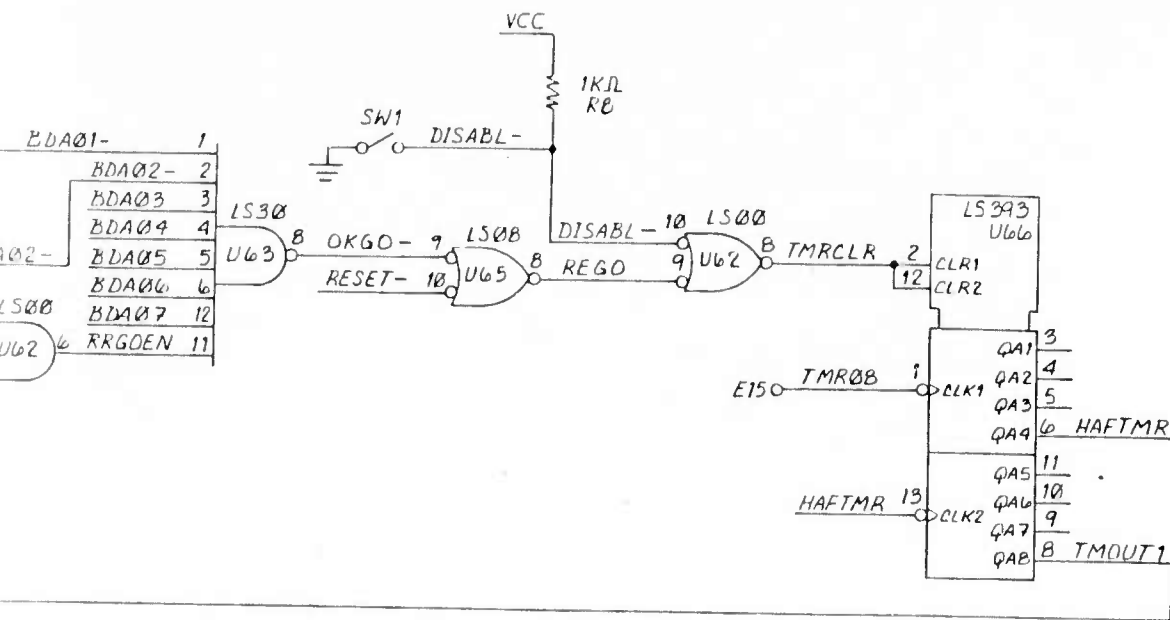
DWG NO 2600466 REV 4 E

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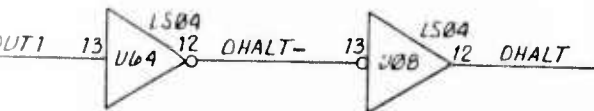
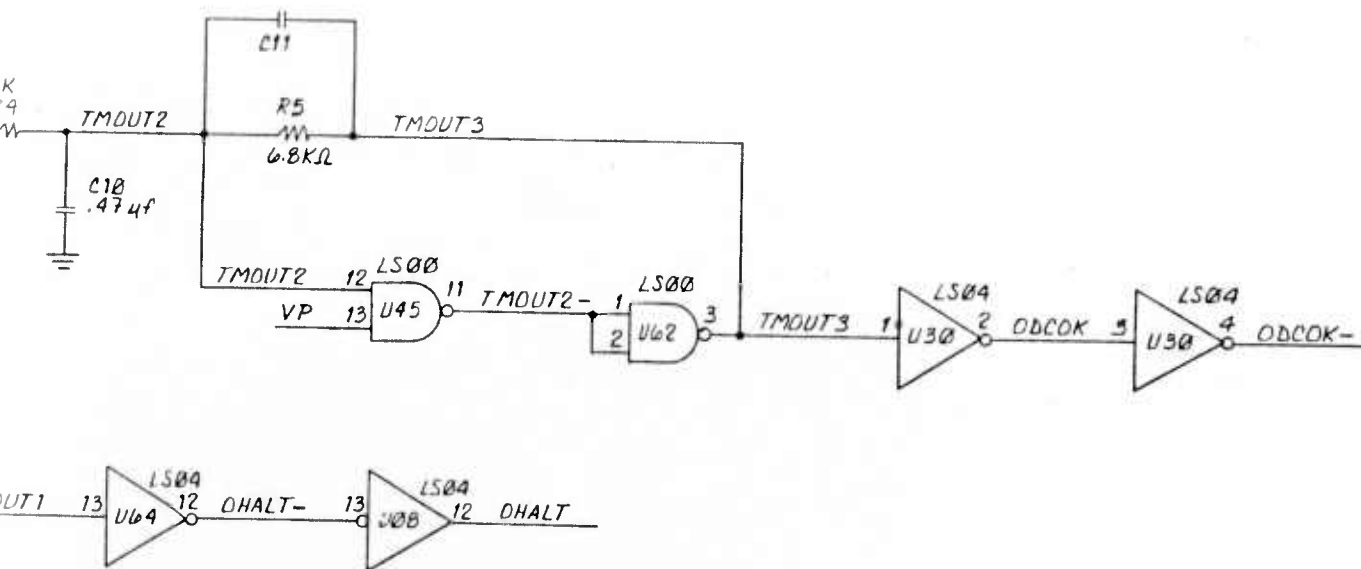
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REV	NO

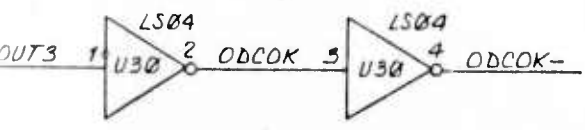
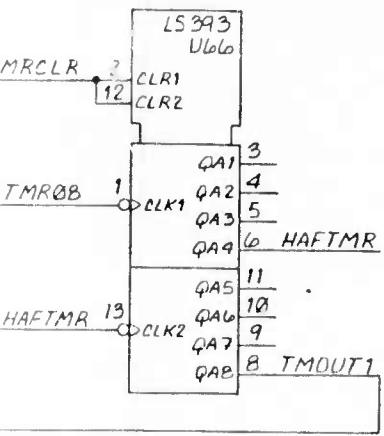


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ITEM NO.	QTY	REQD	FCM NO.	PART OR IDENTIFYING NO.
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE:				
FRACTIONS		DECIMALS	ANGLES	
.XX		.XXX	°	
MATERIAL				CONTRACT NO.
FINISH				APPROVALS
NEXT ASSY				USED ON
APPLICATION				DO NOT SCALE DRAWING

DWG NO. 2600466		REV. 5	REV. 7	1
REVISIONS				
ZONE	REV.	DESCRIPTION	DATE	APPROVED
SEE SH1				



DWG NO. 2600466 REV. 5 6

WATCH DOG TIMER

ITEM NO.	QTY REQD.	FRGM NO.	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL SPECIFICATION
PARTS LIST					
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE FRACTIONS DECIMALS ANGLES .XX .XXX .XXX			CONTRACT NO.		
MATERIAL			APPROVALS DATE		
FINISH			DRAWN <i>Chidwell</i> 28 Sept 82		
NEXT ASSY USED ON			CHECKED <i>M. Lujan</i> 10/1/82		
APPLICATION			ISSUED		
DO NOT SCALE DRAWING			SIZE D 61550 DWG NO. 2600466 REV. 5		
			SCALE NONE SHEET 5 OF 6		

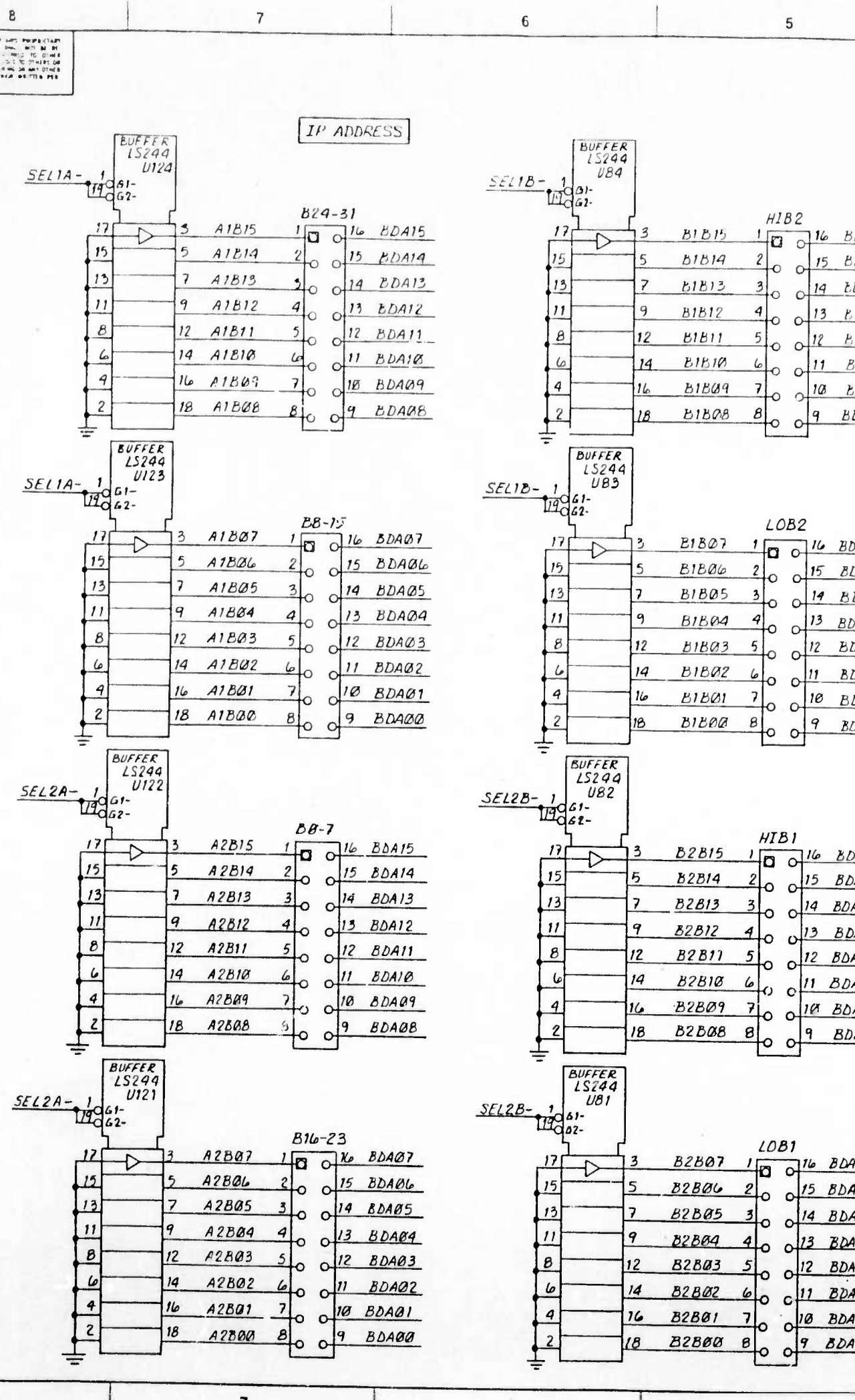
ACC ASSOCIATED COMPUTER CONSULTANTS Santa Barbara, California 93101

LOGIC DIAGRAM ROBUSTNESS II MOD

(C)

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IP ADDRESS

B24-31

HIB2

B8-15

LOB2

B8-7

HIB1

B16-23

LOB1

D

C

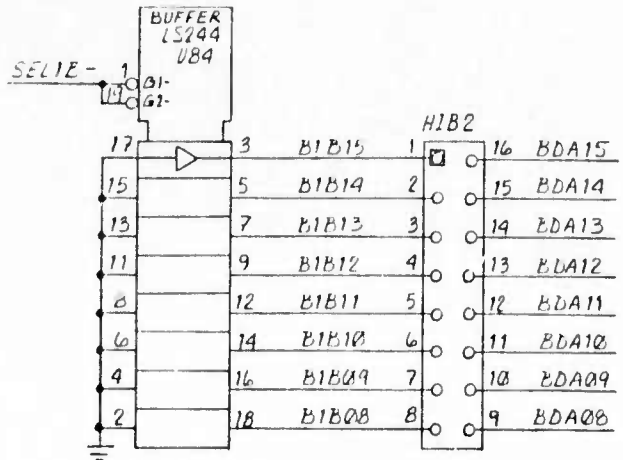
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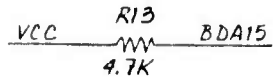
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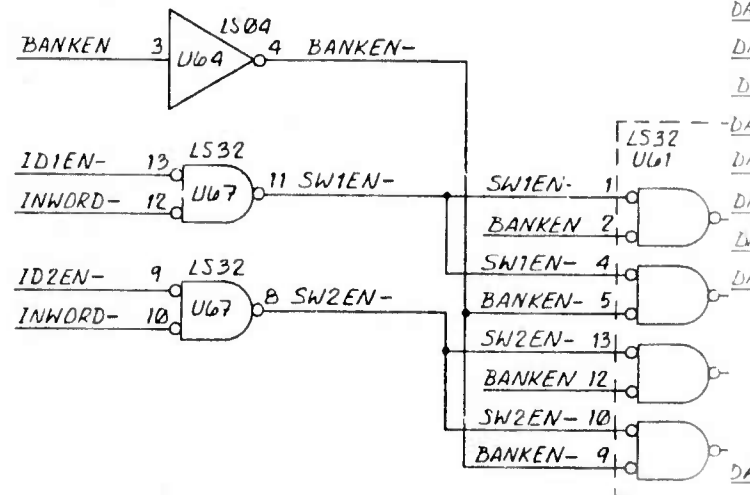
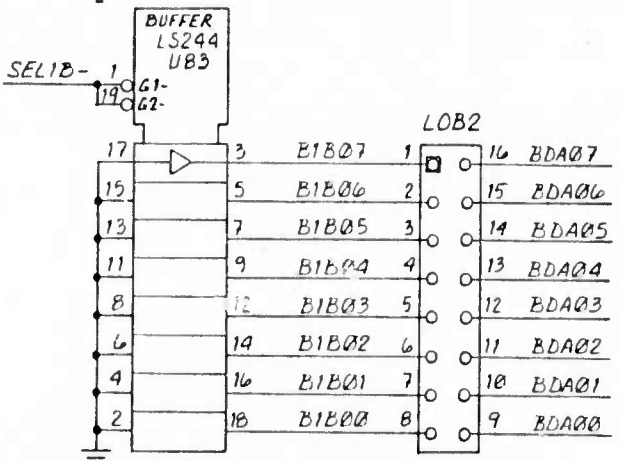
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13	BDA12
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11	BDA10
10	BDA09
9	BDA08



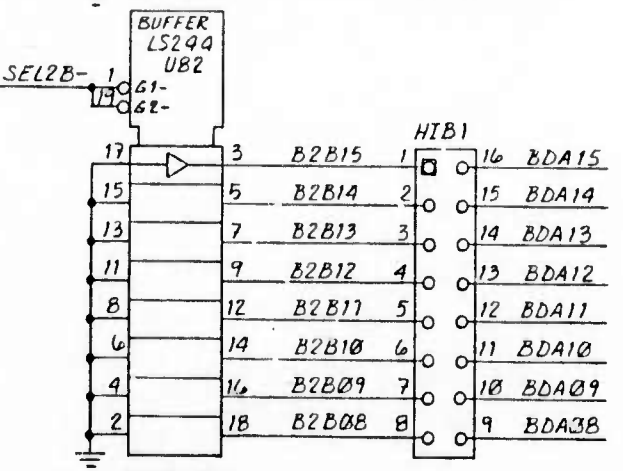
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BDA01	3	BDA14
BDA02	2	BDA13
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BDA07	12	BDA08



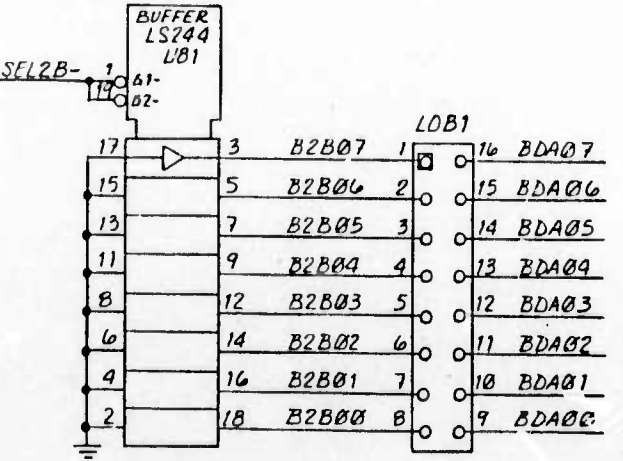
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9	BDA00



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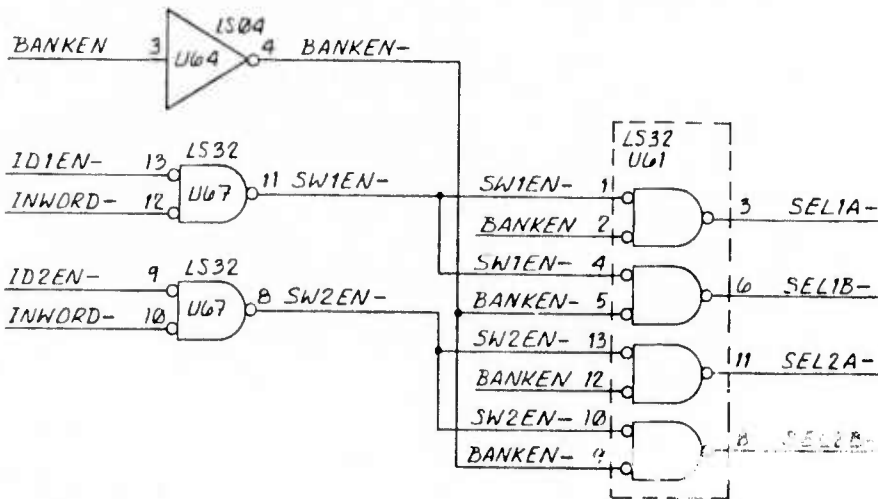
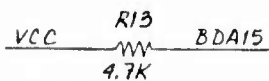
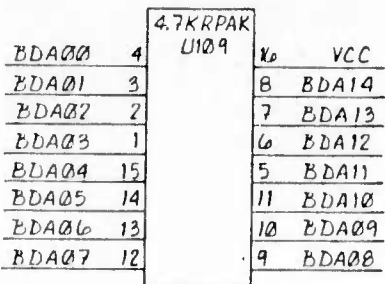


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10	BDA01
9	BDA00



ITEM NO	QTY REQD	RCM NO	PART OR IDENTIFYING NO	CONTRACT NO
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE:				APPROVALS
FRACTIONS DECIMALS ANGLES				
MATERIAL				DRAWN WEDDELL
FINISH				CHECKED M. L. L...
NEXT ASSY		USED ON		ISSUED
APPLICATION				DO NOT SCALE DRAWING

DWG NO		2600466		REV	6	REV	6
REVISIONS							
ZONE	REV	DESCRIPTION				DATE	APPROVED
		SEE SH 1					




SWITCH REGISTERS

ITEM NO	QTY REQD	FRGM NO	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION	MATERIAL SPECIFICATION
PARTS LIST					
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES 1 .001 1/2 .001 1/2 .001				CONTRACT NO APPROVALS DATE DRAWN <i>WEDDELL</i> 5-18-82 CHECKED <i>PA LARA</i> 1-7-82 ISSUED	
MATERIAL				ACC ASSOCIATED COMPUTER CONSULTANTS Santa Barbara, California 93101	
FINISH				LOGIC DIAGRAM ROBUSTNESS II MOD	
NEXT ASSY	USED ON	APPLICATION		DO NOT SCALE DRAWING	SIZE D FRGM NO 61550 DWG NO 2600466 REV 6
				SCALE NONE	SHEET 6 OF 6

DWG NO 2600466 REV 6

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

REPORT DOCUMENTATION PAGE		READ INSTRUCTIONS BEFORE COMPLETING FORM
1. REPORT NUMBER 002	2. GOVT ACCESSION NO.	3. RECIPIENT'S CATALOG NUMBER
4. TITLE (and Subtitle) ROBUSTNESS II FINAL DOCUMENTATION "ROBUSTNESS II MAINTENANCE MANUAL"		5. TYPE OF REPORT & PERIOD COVERED Final Documentation
		6. PERFORMING ORG. REPORT NUMBER ACC-25-002 (ROBUSTII-MM-V001)
7. AUTHOR(s) Shawn Miner (805)963-9431		8. CONTRACT OR GRANT NUMBER(s) MDA903-82-C-0478
9. PERFORMING ORGANIZATION NAME AND ADDRESS Associated Computer Consultants 720 Santa Barbara Street Santa Barbara, CA 93101		10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS DARPA Order No.: 4024
11. CONTROLLING OFFICE NAME AND ADDRESS Defense Supply Service-Washington Room ID-245, Pentagon Washington, DC 20310, Attn: L. F. Meekins		12. REPORT DATE 29 December 1982
		13. NUMBER OF PAGES 35
14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office) DCASMA-VAN NUYS Code S0512A 6230 Van Nuys Blvd. Van Nuys, CA 91108 (213)997-3101		15. SECURITY CLASS. (of this report) UNCLASSIFIED
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18. SUPPLEMENTARY NOTES N/A		
19. KEY WORDS (Continue on reverse side if necessary and identify by block number) <u>ROBUSTNESS II</u> <u>LSI-11/23</u> <u>ROBUSTNESS MODULE</u> <u>BOOT MODULE</u> <u>LSI-11 BOOT</u>		
20. ABSTRACT (Continue on reverse side if necessary and identify by block number) For the enhanced version of the Robustness Module, the Robustness II, this document provides: installation, programming, and maintenance information in the form of text; assembly drawings; socket and pin location diagrams for memory and option selection; schematic diagrams and parts list. The ROBUSTNESS II is used in the LSI Network gateway; and provides: 128 Word (16-Bit) BOOT ROM, space for 8k Words of EPROM, Watch Dog Timing, Elapsed Time Counter (31 bits at 10KHz Clock Rate), -- continued on opposite side		