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Final Technical Report
October 1979

CMOS LIFE SUITABILITY EVALUATION PROGRAM

McDonnell Douglas Astronautics Company

R. C. Maurer

ROME AIR DEVELOPMENT CENTER
Air Force Systems Command
Griffiss Air Force Base, New York 13441

RADC-TR-79-167 has been reviewed and is approved for publication.

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

The results of a matrix of high-temperature accelerated life tests, 125°C life tests, and 250 hour 250°C lot acceptance tests were evaluated to determine the reliability of a cross-section of the (CMOS) family of devices. The devices evaluated included a NOR gate, a flip-flop, a four bit adder, and a counter/divider. Each device was procured from two different manufacturers, and from three different lots of each manufacturer.

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PREFACE

The work described in this report was performed by the Parts Evaluation Laboratory section of the McDonnell Douglas Astronautics Company-St. Louis (MDAC-St. Louis) Engineering Reliability Department during the period between June 1976 and November 1978. This work was performed for the USAF Rome Air Development Center under Contract Number F30602-76-C-0335. The work conducted was directed by Captain Donald T. McCullough of RADC.

Significant technical contributions were made by Messrs. Gordon Johnson, Gary Keller, Michael Roberts, and Edward Sisul of the MDAC-St. Louis Engineering Reliability Department.

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EVALUATION

This effort was designed to evaluate the reliability of a cross section of the CMOS family of digital integrated circuits as procured to the requirements of MIL-STD-883. The high temperature (250°C) lot acceptance test (Method 5005.3) specified in that standard was also evaluated.

During the course of the study, a failure mechanism involving dendritic metal growth along the glass seal of one of the package types was found. The CMOS devices showed considerable lot to lot variation. No way was found by the contractor to predict the poor reliability behavior of some lots prior to the life test. No correlation was found between specific failure modes and the apparent activation energies. Surface mechanisms accounted for 74% of the failures however.

RADC is continuing the research on accelerated testing techniques to isolate possible test induced failures and to look for other accelerating factors such as applied voltage. The CMOS devices in this effort were operated at their maximum rated voltages. However, in actual use conditions, they are normally operated well below their maximum voltage ratings. The field failure rate data are much better than the results of this test would lead one to expect.

The contractor concluded that the high temperature Lot Acceptance Test specified in MIL-STD-883, Method 5005.3, is approximately 50% effective as a method of screening for device and lot reliability. Since that offers a no better than random chance of selecting a good lot, the contractor states that more information is needed for a lot acceptance test.

The principal failure mode was excess drain to source leakage current, I_{SS}. The secondary failure mode concerns the glass seals that many different manufacturers use in their packages. This type package often failed due to hermeticity loss after the temperature cycling associated with life tests. Pin-to-pin shorts occurred due to metal dentritic formations in the glass. The contractor concluded that lead was precipitating out of the glass following reduction of the lead oxide constituent.

This contract achieved its goals, but introduced some serious questions about the accelerated test as a predictor of technology reliability. CMOS devices do seem to have a slightly lower reliability than bipolar devices for small scale integrated circuits. There is no solid evidence that this is true for LSI however.

Donald T. McCullough

DONALD T. McCULLOUGH, Capt, USAF
Project Engineer

1.0 INTRODUCTION

The CMOS technology, due to its inherent low power dissipation and high noise immunity, offers many benefits to military electronic systems in terms of reduced size, weight, and power consumption. However, previous life tests of a single CMOS device type conducted at MDAC-St. Louis and funded by RADC and NASA-MSFC have shown the failure rates due to surface effects of the CMOS devices were several orders of maynitude greater than that of bipolar digital devices. These life tests were limited to a single CMOS device.

The objective of this program was to evaluate the reliability of a cross-section of the CMOS family of digital microcircuits. Included in the evaluation were: a) device electrical characterizations, b) analyses of device physical characteristics, c) determinations of device thermal characteristics, d) high temperature accelerated test studies of device aging characteristics, e) high temperature (250°C) Lot Acceptance Test Studies, and f) MIL-STD-883, 125°C Life Test. Results of the evaluations provided information related to the following:

a) The acceptability of CMOS devices for MIL-M-38510 Class S applications.
b) Failure mechanisms at elevated temperatures and 125°C use-temperatures.
c) Failure distributions at accelerated test conditions.
d) Arrhenius model parameters and failure rates.

This report provides a general description of the overall program and presents the results of tests and evaluations performed throughout the program. Also included in this report are the results of failure analyses and data evaluations performed for the CMOS microcircuits.

2.0 PROGRAM DESCRIPTION

The overall CMOS Life Suitability Evaluation Program is depicted in Figure 1. A total of 4 device types from two manufacturers each were included in the program. The specific CMOS device types and manufacturer codes are shown in Table 1. A minimum of 330 devices of each manufacturer's microcircuit type were procured in 3 different lots (different wafer runs and different packaging runs), two lots of 130 devices minimum and one lot of 70 devices minimum. The 4001 and 4013 device types were procured to the electrical requirements of the JEDEC Specification for B Series CMOS (JEDEC STD. No. 11). The 4008 and 4017 device types were procured to the MIL-M-38510 electrical requirements. All device types were procured to MIL-STD-883 Class B, or equivalent, processing requirements, with the exception of the burn-in test which was not performed. Upon receipt at MDAC-St. Louis, all devices were subjected to an external visual examination, and electrical tests. The electrical testing consisted of MIL-M-38510 Group A dc tests (or similar tests based on the JEDEC Specifications as applicable) performed at ambients of 25°C, -55°C and 125°C. Dynamic testing per the applicable MIL-M-38510 Specification was also performed on a pass/fail basis for all Lot C devices intended for the 250 hour, 250°C Lot Acceptance Test. However, where a high percentage of devices did not meet the MIL-M-38510 parameter limits, the end-point limits were adjusted, as required, to obtain an adequate number of devices for accelerated life testing.

Subsequent to performing the initial examinations and tests, acceptable devices were allocated, by serial number, to test groups. Device allocation for each manufacturer's device type is as shown in Table 2.

A total of nine devices of each manufacturer's device types were allocated for construction analysis. These analyses were destructive physical analyses to determine construction methods, manufacturing process techniques and workmanship used in the fabrication of devices. Results were used to predict potential reliability problems, to determine possible accelerated life test limitations due to materials used in device fabrication, and to facilitate subsequent failure analyses.

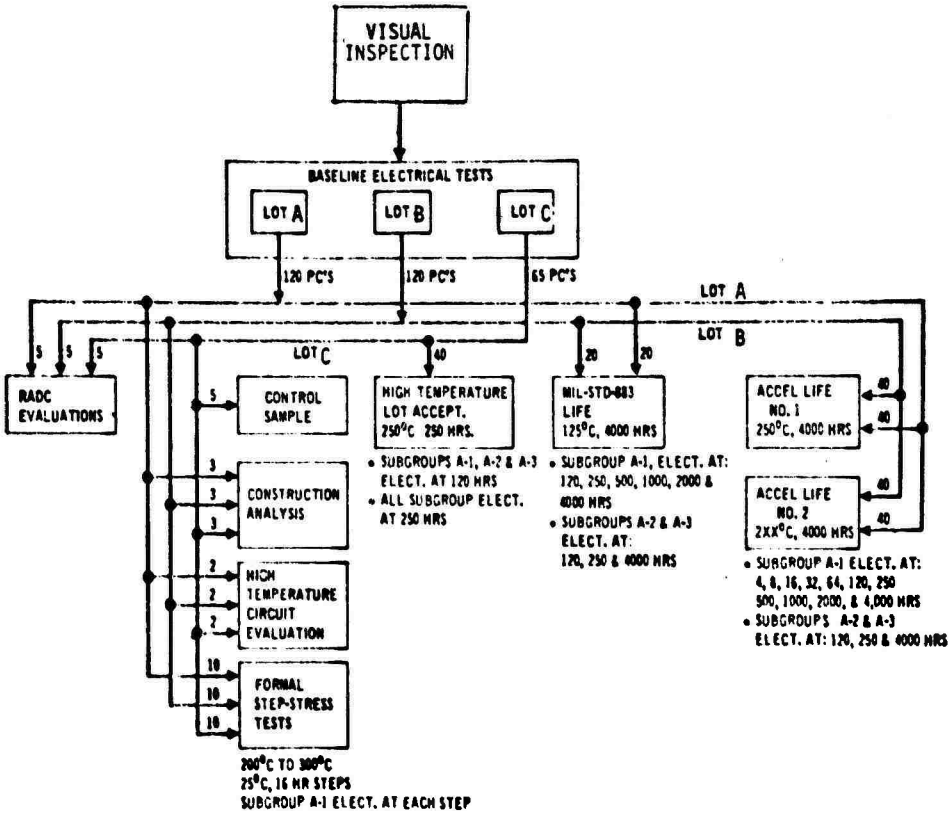


FIGURE 1. CMOS MICROCIRCUIT TEST PROGRAM

TABLE 1. CMOS MICROCIRCUIT TYPES

SPECIFICATION REFERENCE*	COMMERCIAL PART NO. & PACKAGE	DEVICE TYPE	MANUFACTURER CODE
JEDEC SPECIFICATION FOR B SERIES CMOS & MIL-STD-883	4001 B 14 PIN DIP	QUAD 2-INPUT NOR GATE	A B
JEDEC SPECIFICATION FOR B SERIES CMOS & MIL-STD-883	4013 B 14 PIN DIP	DUAL D-TYPE FLIP FLOP	B C
M38510/05401 BEC	4008 16 PIN DIP	FOUR-BIT FULL ADDER	C D
M38510/05601 BEC	4017 16 PIN DIP	DECADE COUNTER/ DIVIDER	A D

* ALL MICROCIRCUITS SCREENED TO MIL-STD-883, CLASS B MINUS THE BURN-IN.

TABLE 2. DEVICE ALLOCATION

	NO. OF DEVICES		
	LOT A	LOT B	LOT C
Construction Analysis	3	3	3
Initial Device Studies			
Circuit Evaluation & Thermal Studies	2	2	2
Formal Step Stress	10	10	10
RADC Evaluations	5	[illegible]	5
Lot Acceptance Test	-	-	40
MIL-STD-883 125°C Life Test	20	20	0
Accelerated Life Test #1	40	40	-
Accelerated Life Test #2	40	40	-
Control Sample	-	-	5

The initial device studies, performed with thirty-six devices of each manufacturer's device type, were prerequisites to performing the accelerated life tests. These studies included development of bias circuits for accelerated life tests, step-stress tests and thermal resistance measurements for computing device junction temperatures at anticipated life test temperatures.

The high temperature tests performed with 240 devices of each manufacturer's device type consisted of: a 250 hour, 250°C Lot Acceptance Test; a MIL-STD-883, 125°C, 4,000 hour life test, and two 4,000 hour accelerated life tests at ambient temperatures of 250°C and one other temperature above 200°C (as determined from bias circuit evaluations). The data from these tests provided information about device failure mechanisms, failure distributions, and life acceleration factors. The Lot Acceptance Test was conducted for 250 hours. The long term life tests were conducted for 4,000 hours or 65% failure, whichever occured first. Interim electrical tests were performed on life test devices after cool-down to room temperature with bias applied. These measurements consisted of dc electrical tests at 25°C which were performed at the intervals shown in Table 3. Test subgroups are defined in Appendix B. Unless otherwise directed by the Project Engineer, all devices that failed an Interim Test were removed from the life test and subjected to failure analysis. At the conclusion of each life test, surviving devices were subjected to the same set of dc electrical tests performed prior to life testing.

A control sample of each manufacturer's device type (five 4001B, five 4013B, four M38510/05401, and four M38510/05601) was subjected to electrical testing each time the test devices were subjected to Interim or Final Electrical Tests. The purpose of the control sample was to provide a check on the long term stability of the automated test equipment.

TABLE 13. SCHEDULE OF ELECTRICAL MEASUREMENTS

TEST DURATION HOURS	250°C, 250 HRS LOT ACCEPTANCE TEST				ACCELERATED LIFE TESTS			MIL-STD-883 TEST		
	MIL-M-38510 SUBGROUP				MIL-M-38510 SUBGROUP			MIL-M-38510 SUBGROUP		
	A1, A7	A2	A3	A4-A6 A8-A11	A1, A7	A2	A3	A1, A7	A2	A3
0	X	X	X	X	X	X	X	X	X	X
4					X					
8					X					
16					X					
32					X					
64					X					
120	X	X	X		X	X	X	X	X	X
250	X	X	X	X	X	X	X	X	X	X
500					X			X		
1000					X			X		
2000					X			X		
4000					X	X	X	X	X	X
6000 ⚠1					X	X	X	X	X	X

⚠1 THE TEST DURATION WAS EXTENDED TO 6,000 HOURS FOR SELECTED 4001 AND 4013 CELLS.

3.0 RESULTS OF PRE-LIFE TESTS AND EVALUATIONS

3.1 EXTERNAL VISUAL EXAMINATIONS AND HERMETICITY TESTS

Upon receipt at MDAC-St. Louis, all devices were examined for conformance to purchase order requirements for device type, package style, lead finish, and marking. Each device was examined at 3X magnification for evidence of gross damage to package, package seals, and leads. These visual examinations revealed varying degrees of shipping damage to the Manufacturer A and Manufacturer C Cerdip packages, misaligned lids on the Manufacturer B packages, and lack of lot identification on 288 Manufacturer A devices. Details of these findings and the actions taken are as follows:

a) Shipping Damage - The damaged Cerdip packages were shipped in plastic rail containers. Eleven (three Manufacturer C's 4013B, four Manufacturer C's 4008, and four Manufacturer A's 4017) devices had separated at the glass frit seal as shown in Figure 2, and eleven devices had portions of the ceramic package chipped away. Typical examples of chipped packages are shown in Figure 3. This type of damage was duplicated in the laboratory by dropping full plastic shipping rails on their ends. Since the extent of any minor damage to package seals was unknown, all Manufacturer A's devices were returned for replacement. Replacement Manufacturer C devices were not available, and all devices in each damaged shipment were subjected to hermeticity tests per MIL-STD-883 Method 1014.1, Conditions A1 and C2. All devices passing the hermeticity tests were considered acceptable for life testing.

b) Misaligned Lids - The Manufacturer B microcircuits were packaged in a white ceramic dual in-line package. This package has a full metal lid which was not properly aligned in all cases during the final sealing process of the devices. Packages with misaligned lids created a possibility of having nonhermetic devices in life test, therefore, hermeticity tests were performed on the Manufacturer B devices.

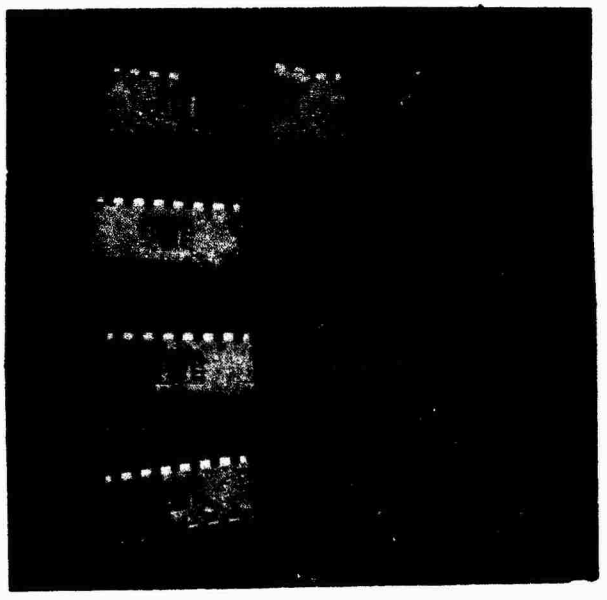


FIGURE 2. CERDIP PACKAGES BROKEN IN SHIPPING CONTAINERS

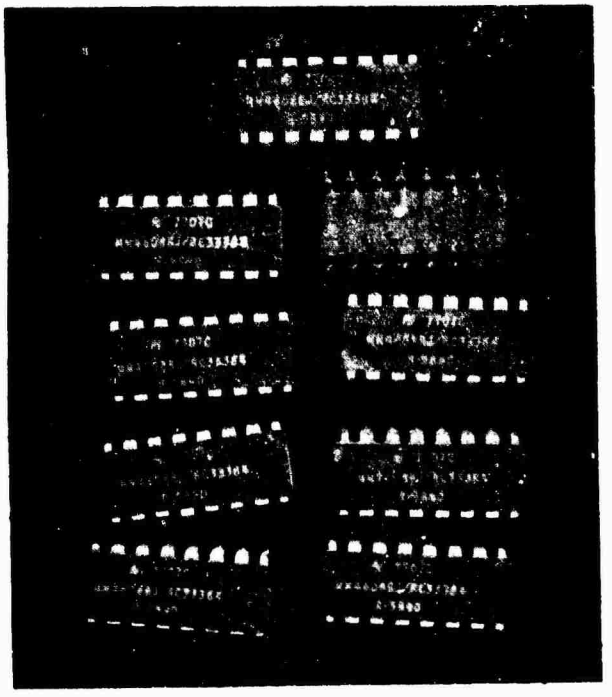


FIGURE 3. CERDIP PACKAGES CHIPPED IN SHIPPING CONTAINERS

c) Lot Identification - Manufacturer A supplied 228 MIL-M-38510/05601 (4017) devices without proper lot identification markings. These were returned to the manufacturer, and replacement devices were obtained.

A summary of the visual inspection and hermeticity test results is provided in Table 4. Replacement devices for visual rejects are included in the number of devices available for visual inspection found in Table 4.

3.2 BASELINE ELECTRICAL PERFORMANCE TEST

All devices surviving the initial visual inspection and hermeticity tests were subjected to electrical performance tests at 25°C, 125°C, and -55°C. The dc electrical tests for the 4001B and the 4013B devices were based on a proposed MIL-M-38510 slash sheet dated September 1976 and the JEDEC Standard Specification for Description of "B" series CMOS devices. The dc electrical tests for the remaining two devices were initially established as those contained in MIL-M-38510/05401 and MIL-M-38510/05601. The Lot C dynamic tests were the applicable MIL-M-38510 Group A test subgroups 4, 8, 9, 10 and 11. Some of the MIL-M-38510 parameter limits were subsequently relaxed to obtain a sufficient number of "good" devices for life testing. A high percentage of the 4008 devices failed to meet the initially established test limits for the I_{SS}, I_{IL2}, t_{PHL}, and the t_{PLH} parameters, and 4017 devices failed to meet the limits for I_{IH}, I_{IL}, and I_{SS}. Therefore, these parameter limits were revised as shown in Table 5. Complete details of the electrical test conditions and limits used for testing each device type are contained in Appendix B.

Results of the initial electrical testing using the revised test limits as contained in Appendix B can be found in Table 6. During initial test all the MIL-M-38510/05601 devices failed the set-up time test (T_{SHL}) at 125°C. Since these tests were only performed on the Lot C devices, these test failures were ignored and the devices subjected to subsequent tests. Later, in conjunction with RADC, the test fixture was re-examined and found to be defective for this particular test. The Lot C test survivors were then retested and all devices passed. Parametric data taken at 25°C for each manufacturer's device

TABLE 4. INITIAL INSPECTION AND HERMETICITY TEST RESULTS

COMMERCIAL PART NO.	MANU-FACTURER	VISUAL INSPECTION		HERMETICITY TEST				TOTAL NO. FAILED DEVICES	TOTAL NO. ACCEPTABLE DEVICES
		NO. INTO TEST	NO. FAILED	FINE LEAK		GROSS LEAK			
				NO. INTO TEST	NO. FAILED	NO. INTO TEST	NO. FAILED		
40018	A	360	1		NOT REQUIRED			1	359
40018	B	330	3	74	0	74	4	7	323
4013B	B	330	10		NOT REQUIRED			10	320
40138	C	330	8	126	1	125	7	16	314
400B	C	330	4	196	1	195	23	28	302
400B	D	323	1		NOT REQUIRED			1	322
4017	A	720	361		NOT REQUIRED			361	359
4017	D	330	2		NOT REQUIRED			2	328

TABLE 5. REVISED MIL-M-38510 PARAMETER LIMITS

MIL-M-38510 SLASH SHEET	SYMBOL	TEST NO.	MIL-M-38510 LIMIT		REVISED LIMIT		SUBGROUP	UNITS
			MIN	MAX	MIN	MAX		
05401	I_{SS}	19-46	---	-0.5	---	-10.0	1	µA
	I_{SS}	19-46	---	-5.0		-10.0	2	µA
	I_{IL2}	116-124	---	-45	---	-150	2	nA
	t_{PHL}	162-173	100	2250	80	2250	11	ns
	t_{PLH}	178-189	100	2900	90	2900	9	ns
			150	4350	130	4350	10	ns
			100	2900	80	2900	11	ns
05601	I_{IH}	1-3	---	1.0	---	10.0	1	nA
	I_{IH}	1-3	---	10.0	---	100	2	nA
	I_{IH}	1-3	---	1.0	---	10.0	3	nA
	I_{IL}	4-6	---	1.0	---	10.0	1	nA
	I_{IL}	4-6	---	10.0	---	100	2	nA
	I_{IL}	4-6	---	1.0	---	10.0	3	nA
	I_{SS}	14-15	---	500	---	5000	1	nA
	I_{SS}	14-15	---	5	---	100	2	µA

TABLE 6. INITIAL ELECTRICAL TEST RESULTS

DEVICE	MFR	LOT	25°C		125°C		-55°C		TOTAL FAILED
			NO. TESTED	FAILED	NO. TESTED	FAILED	NO. TESTED	FAILED	
4001	A	A	144	0	144	2	144	1	2
		B	143	0	143	3	143	0	3
		C	72	0	72	0	72	0	0
4001	B	A	126	0	126	0	126	0	0
		B	130	1	130	1	130	1	1
		C	67	0	67	0	67	0	0
4013	C	A	118	2	118	2	118	1	2
		B	128	0	128	0	128	2	2
		C	68	1	68	1	68	1	1
4013	B	A	123	2	123	1	123	0	2
		B	127	1	127	1	127	1	1
		C	70	0	70	0	70	0	0
4008	C	A	129	5	129	6	129	0	8
		B	111	2	111	2	111	1	2
		C	61	1	61	2	61	0	2
4008	D	A	130	4	130	5	130	5	5
		B	123	1	123	1	123	0	1
		C	69	4	69	1	69	0	4
4017	A	A	141	2	141	5	141	10	14
		B	140	8	140	2	140	7	9
		C	69	0	69	0⚠	69	1	1
4017	D	A	129	1	129	2	129	2	3
		B	127	2	127	2	127	3	3
		C	67	1	67	1⚠	66	1	2

type is shown in Tables 7 through 10. These tables provide parameter limits, a computed mean value of the parameter for all devices meeting the revised specification limits, and a computed standard deviation of the measured parameter values. Examination of the electrical test data revealed only minor deviations in parameter values between different manufacturers except for the dynamic tests and the 4001 and 4013 negative clamp diode (V_{IC}-) parameters. The difference between manufacturers in the dynamic parameters can be attributed to individual device capacitance and internal lead length. The difference in the negative clamp diode parameters can be attributed to the difference between manufacturers in designing input protection networks. Figure 4 shows the input protection networks for the devices in this program. There were also marked differences between parameter values in different lots of the same manufacturer. The V_{OL1} parameter of both manufacturer's 4013 devices varied by lot. Lots B and C of Manufacturer B's 4013 devices also exhibited slightly larger I_{SS} currents than Lot A. Likewise, Lot A of Manufacturer C's M38510/05401 (4008) devices, Lot C of Manufacturer D's M38510/05401 (4008) devices, and Lot A of Manufacturer A's M38510/05601 (4017) devices exhibited larger I_{SS} mean values than the devices in other lots from the same manufacturer. The construction analyses indicated no anomalies between lots that would account for these differences in parameter values. In the subsequent life tests, the 4013 devices did not exhibit V_{OL1} failures or a major degradation in the V_{OL1} parameter values. The lots of 4008 and 4017 devices which exhibited larger I_{SS} values did result in a larger proportion of failures due to this parameter. This would indicate that the difference in number of failures due to this parameter was the probable result of lot to lot variations in the distribution of parameter values rather than a difference in the acceleration factors.

3.3 MICROCIRCUIT CONSTRUCTION DETAILS

A destructive physical analysis of three devices from each lot of each manufacturer's device type was performed to determine the materials, construction methods, process techniques and quality of workmanship used in device fabrication. With the exception of the Manufacturer A MIL-M-38510/05601 (4017) devices, no construction features, anomalies or construction differences

TABLE 7. 4001B INITIAL ELECTRICAL 25°C PARAMETER CHARACTERIZATION

PARAMETER	LIMITS		MANUFACTURER A						MANUFACTURER B						UNITS
			LOT A		LOT B		LOT C		LOT A		LOT B		LOT C		
	MIN	MAX	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	
V_{IC+}	---	1.5	0.808	0.009	0.808	0.009	0.806	0.008	0.828	0.017	0.825	0.017	0.823	0.015	V
V_{IC-}	---	-6.0	-2.314	0.082	-2.351	0.076	-2.353	0.081	-1.234	0.464	-1.169	0.393	-1.183	0.409	V
I_{SS}	---	-1.0	-0.001	0.002	-0.002	0.006	-0.001	0.001	-0.001	0.001	-0.002	0.000	0.002	0.001	μA
V_{OL1}	---	0.4	0.200	0.017	0.210	0.022	0.205	0.020	0.154	0.015	0.165	0.012	0.144	0.017	V
V_{OL2}	---	.05	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	V
V_{OL3}	---	1.5	0.001	0.001	0.001	0.001	0.001	0.000	0.001	0.000	0.001	0.000	0.001	0.000	V
V_{OH1}	4.6	---	4.928	0.000	4.927	0.000	4.929	0.010	4.927	0.000	4.919	0.000	4.916	0.019	V
V_{OH2}	4.95	---	5.000	0.000	5.000	0.000	5.000	0.006	5.000	0.000	5.000	0.000	5.000	0.024	V
V_{OH3}	13.5	---	14.998	0.170	14.998	0.172	14.999	0.103	14.994	0.139	14.995	0.143	14.996	0.044	V
I_{IH1}	-0.1	---	0.000	0.000	0.001	0.001	0.001	0.002	-0.000	0.000	0.000	0.000	0.000	0.000	μA
I_{IL1}	---	0.1	-0.001	0.001	-0.001	0.004	-0.001	0.002	0.000	0.000	0.000	0.000	0.000	0.000	μA
t_{PHL}	30	210	TEST NOT REQUIRED				113.06	7.055	TEST NOT REQUIRED				59.64	6.369	ns
t_{PLH}	30	210					113.94	6.360					57.92	5.191	ns
t_{THL}	40	300					85.25	6.190					54.75	4.946	ns
t_{TLH}	50	410					66.55	3.337					65.83	4.421	ns

TABLE 8. 4013B INITIAL ELECTRICAL 25°C PARAMETER CHARACTERIZATION

PARAMETER	LIMITS		MANUFACTURER C						MANUFACTURER B						UNITS
			LOT A		LOT B		LOT C		LOT A		LOT B		LOT C		
	MIN	MAX	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	
V_{IC+}	---	1.5	0.809	0.010	0.816	0.009	0.811	0.010	0.800	0.009	.803	.008	0.799	0.088	V
V_{IC-}	---	-6.0	-0.987	0.062	-1.006	0.072	-0.995	0.066	-1.803	0.037	-1.644	0.050	-1.569	0.029	V
I_{SS}	---	-1.0	-0.004	0.011	-0.005	0.011	-0.005	0.010	-.007	0.011	-0.018	0.091	-0.015	0.086	µA
V_{OL1}	---	0.4	0.217	0.006	0.164	0.006	0.162	0.007	0.134	0.013	0.098	0.008	0.155	0.011	V
V_{OL2}	---	0.5	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	V
V_{OL3}	---	1.5	0.000	0.000	0.000	0.000	0.000	0.000	0.001	0.000	0.000	0.000	0.000	0.000	V
V_{OH1}	4.6	---	4.893	0.000	4.873	0.000	4.893	0.012	4.921	0.000	4.923	0.000	4.915	0.012	V
V_{OH2}	4.95	---	5.000	0.009	5.000	0.012	5.000	0.000	5.000	0.014	5.000	0.000	5.000	0.004	V
V_{OH3}	13.5	---	15.000	0.018	15.000	0.040	15.000	0.014	14.998	0.163	14.998	0.166	14.999	0.060	V
I_{IH1}	---	0.1	-0.000	0.001	-0.000	0.000	-0.000	0.000	-0.002	0.008	-0.001	0.003	-0.003	0.011	µA
I_{IL1}	-0.1	---	-0.000	0.001	-0.000	0.000	0.001	0.008	0.000	0.000	0.000	0.001	0.000	0.001	µA
t_{PHL}	70	500	TEST NOT REQUIRED				124.7	37.319	TEST NOT REQUIRED				114.40	24.876	nS
t_{PLH}	70	550					149.4	16.387					120.78	15.531	nS
t_{THL}	15	300					83.03	8.491					60.94	6.284	nS
t_{TLH}	15	300					103.0	8.078					68.91	3.204	nS
t_P	---	300					79.88	4.577					33.20	2.670	nS
t_{SHL}	---	150					16.56	4.480					27.61	1.376	nS
t_{SLH}	---	150					18.29	3.372					16.05	1.261	nS
t_{HHL}	---	150					-11.10	1.323					-22.27	1.529	nS
t_{HLH}	---	150					4.726	1.152					-1.962	1.224	nS

TABLE 9. MIL-M-38510/05401 (4008) INITIAL ELECTRICAL 25°C PARAMETER CHARACTERIZATION

PARAMETER	LIMITS		MANUFACTURER C						MANUFACTURER D						UNITS
			LOT A		LOT B		LOT C		LOT A		LOT B		LOT C		
	MIN	MAX	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	
V_{IC+}	---	7.5	0.825	0.011	0.825	0.009	0.824	0.012	0.757	0.009	0.753	0.009	0.755	0.009	V
V_{IC-}	---	-6	-1.095	0.024	-1.074	0.023	-1.094	0.090	-0.731	0.009	-0.735	0.009	-0.732	0.009	V
I_{SS}	---	-10.0	-0.012	0.048	0.000	0.017	-0.151	0.018	-0.002	0.006	0.004	0.007	-0.043	0.034	µA
V_{OH1}	4.5	---	4.893	0.087	4.997	0.000	4.893	0.054	4.947	0.036	4.941	0.044	4.948	0.041	V
V_{OH2}	4.95	---	5.000	0.006	5.000	0.000	5.000	0.014	5.000	0.000	5.000	0.004	5.000	0.011	V
V_{OH3}	11.25	---	12.495	0.068	12.492	0.138	12.495	0.155	12.490	0.117	12.493	0.131	12.490	0.119	V
V_{OL1}	---	0.5	0.030	0.027	0.000	0.002	0.030	0.013	0.026	0.024	0.035	0.032	0.026	0.023	V
V_{OL2}	---	.05	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	V
V_{OL3}	---	1.25	0.003	0.001	0.005	0.028	0.003	0.001	0.004	0.001	0.002	0.000	0.003	0.001	V
I_{IH1}	---	9.0	0.082	0.614	-0.015	0.147	0.079	0.164	0.514	1.154	-0.030	0.051	0.240	0.647	nA
I_{IH2}	---	1.0	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	nA
I_{IL1}	---	-9.0	-0.363	0.465	-0.225	0.251	-0.442	0.207	-0.040	0.013	-0.079	0.029	-0.065	0.012	nA
t_{PHL}	100	2,250	TEST NOT REQUIRED				155.4	19.27	TEST NOT REQUIRED				187.7	59.98	ns
t_{PHL}	40	750					145.5	11.23					155.6	8.615	ns
t_{PHL}	20	300					78.59	6.949					83.54	4.459	ns
t_{PLH}	90	2,900					159.2	28.77					186.9	60.82	ns
t_{PLH}	100	750					169.7	15.55					148.4	7.859	ns
t_{PLH}	20	300					76.46	7.646					79.92	3.806	ns
t_{THL}	120	10,000					70.21	7.333					76.81	4.467	ns
t_{THL}	30	520					54.95	3.549					61.51	2.454	ns
t_{TLH}	120	10,000					112.7	13.80					91.63	285.2	ns
t_{TLH}	30	520					108.9	11.10					69.60	4.368	ns

TABLE 10. MIL-M-38510/05601 (4017) INITIAL ELECTRICAL 25°C PARAMETER CHARACTERIZATION

PARAMETER	LIMITS		MANUFACTURER A						MANUFACTURER D						UNITS
	MIN	MAX	LOT A		LOT B		LOT C		LOT A		LOT B		LOT C		
			MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	
I_{IH}		-10.0	-1.361	1.055	-0.854	1.147	-0.207	1.179	-1.306	0.836	-0.979	0.875	-0.682	0.874	nA
I_{IL}		-10.0	-0.849	0.522	-0.251	0.349	0.161	0.242	-0.460	0.241	-0.181	0.423	0.072	0.415	nA
V_{OH1}	4.20	5.10	4.976	0.080	4.977	0.079	4.976	0.017	4.839	0.076	4.872	0.069	4.774	0.000	V
V_{HC1}	4.20	5.10	4.866	0.027	4.873	0.027	4.862	0.017	4.836	0.027	4.865	0.025	4.768	0.023	V
V_{OL1}	-0.01	0.50	0.020	0.003	0.018	0.002	0.021	0.002	0.085	0.015	0.084	0.014	0.017	0.016	V
V_{LC1}	-0.01	0.50	0.057	0.013	0.051	0.004	0.062	0.005	0.180	0.005	0.172	0.008	0.203	0.004	V
V_{OH2}	14.99	15.10	15.000	0.065	15.000	0.050	15.000	0.046	15.000	0.072	14.999	0.112	14.999	0.123	V
V_{HC2}	14.99	15.10	15.001	0.000	15.001	0.021	15.001	0.000	15.001	0.013	15.000	0.037	14.999	0.050	V
V_{OL2}	-0.01	0.01	0.003	0.002	0.001	0.001	0.003	0.000	0.002	0.001	0.004	0.002	0.005	0.001	V
V_{LC2}	-0.01	0.01	0.003	0.002	0.001	0.001	0.003	0.000	0.001	0.001	0.003	0.001	0.005	0.001	V
I_{SS}		-5.0	-0.188	0.533	-0.050	0.004	-0.053	0.013	-0.047	0.029	-0.039	0.034	-0.032	0.008	µA
V_{THN}			2.334	0.140	2.095	0.119	2.265	0.104	1.861	0.033	1.768	0.033	1.950	0.019	V
V_{THP}			-1.533	0.103	-1.671	0.113	-1.774	0.124	-2.072	0.041	-1.845	0.081	-2.444	0.051	V
t_{PHL1}		1450	TEST NOT REQUIRED				533	40	TEST NOT REQUIRED				456	24	ns
t_{PHL2}		1800					631	52					535	42	ns
t_{PLH1}		1450					439	32					418	20	ns
t_{PLH2}		1800					554	78					895	78	ns
t_{THL1}		550					98	6					224	8	ns
t_{THL2}		2250					147	12					325	41	ns
t_{TLH1}		550					122	8					220	31	ns
t_{TLH2}		2250					143	12					1061	74	ns
t_{PHL3}		1800					756	105					536	40	ns
t_{PHL4}		1450					680	52					388	21	ns
t_{PHL5}		1800					719	54					856	60	ns

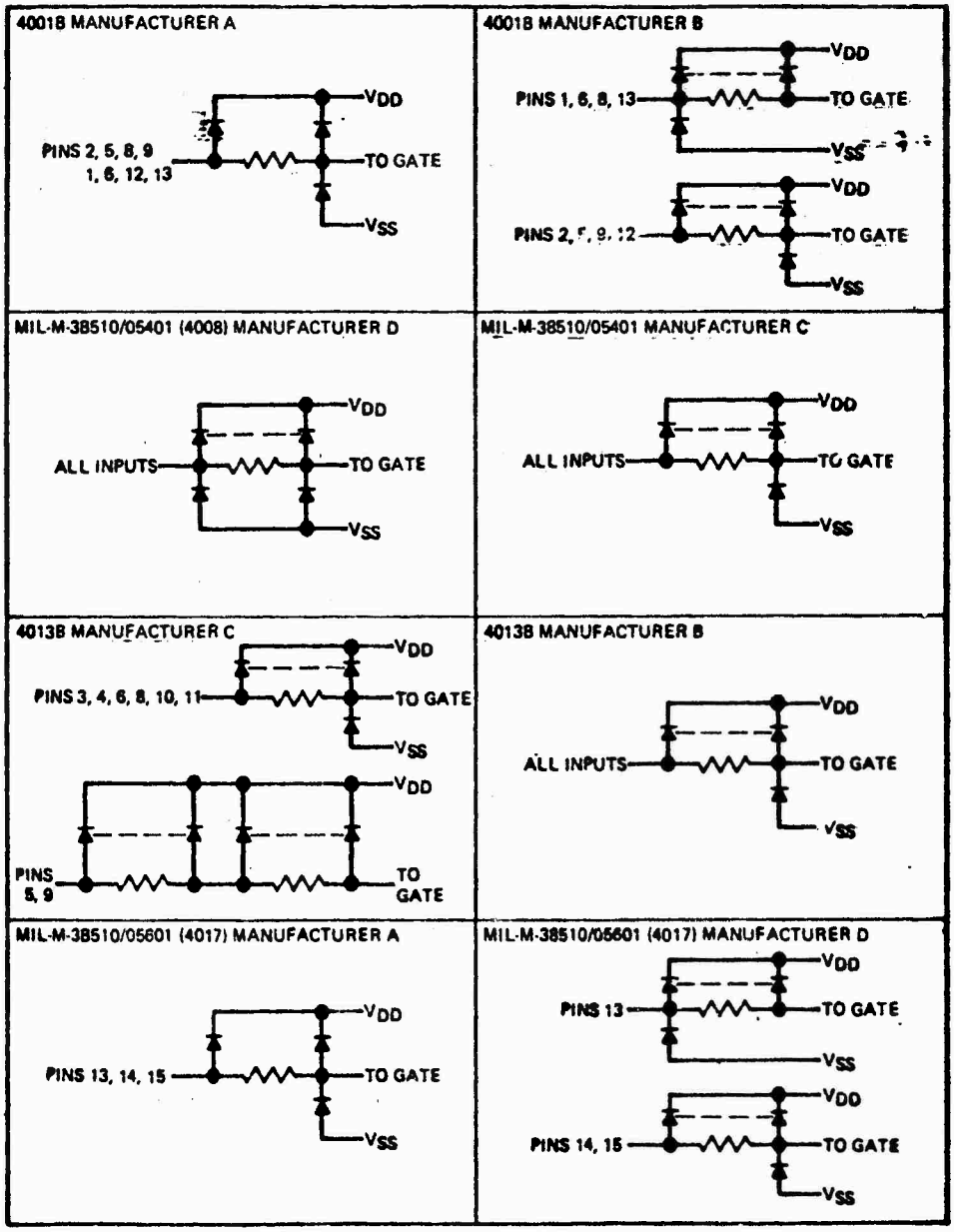


FIGURE 4. DEVICE INPUT PROTECTION NETWORKS

were noted between the three lots of each manufacturer's device type. The chip surface of the Manufacturer A's Lot B and Lot C 4017 devices contained the identification number 5KF-A, while the Lot A devices contained the identification number 15KF. Other than this difference, the metallization and diffusion patterns in all three lots appeared identical. A summary of the major construction features noted in each device type is shown in Table 11. Complete results of these analyses, including schematics and chip topography are contained in Appendix A.

Certain construction features that could impact life test results were noted in some of the manufacturer's device types. These included: a) Manufacturer B's package lead seal, b) Manufacturer A's wafer scribe technique, and c) Manufacturer D's die attach technique. The Manufacturer B ceramic/glass package with metal top and bottom is more susceptible to cracked lead seals during temperature cycling than the other packages [1]. Consequently, the inherent temperature cycling due to installing/removing devices for electrical testing during life testing could result in cracked lead seals and loss of hermeticity. This manufacturer had 92 4001 device failures which were leak tested and of the 46 leak test failures 27 or 58% were attributed to cracks in the package.

The Manufacturer A die was laser scribed which could result in a build-up of silicon material at the scribe. This build-up of silicon increases the suspectibility of devices to fail due to wire-to-die shorts. Molten silicon could also be splattered on the die surface and be a contributing factor to device failures. No evidence of laser scribe debris was observed on the surface of the devices examined. However, five of this manufacturer's devices did fail during accelerated life tests due to wire-to-die shorts caused by hillocks from the laser scribing.

The Manufacturer D die is attached to the header with epoxy, and long-term exposure to high temperature can degrade the integrity of the die bond. There is also a danger that moisture in the epoxy can be released during high temperature exposure and be a contributing factor to device failures. Some of

TABLE 11. MICROCIRCUIT CONSTRUCTION CHARACTERISTICS

PART TYPE	MANUFACTURER	PACKAGE TYPE	PACKAGE MATERIAL	LID SEAL	LEAD MATERIALS			CHIP CHARACTERISTICS			WIRE BONDS	
					EXTERNAL	INTERNAL WIRE	LEAD FRAME	ATTACH	METALLIZATION	SCRIBE	CHIP	FRAME
40010	A	14 PIN CERDIP	CERAMIC	GLASS FRIT	Sn/Pb PLATED ALLOY 42	A1	A1 CLAD ALLOY 42	Au/Si EUTECTIC	A1	LASER	ULTRASONIC	ULTRASONIC
	B	14 PIN CERAMIC/ METAL TOP & BOTTOM	CERAMIC/Au PLATED KOVAR TOP & BOTTOM	SOLDER	Au PLATED KOVAR	A1	Au CLAD KOVAR	Au/Si EUTECTIC	A1	MECHANICAL	ULTRASONIC	ULTRASONIC
40130	C	14 PIN CERDIP	CERAMIC	GLASS FRIT	Au PLATED ALLOY 42	A1	Au CLAD ALLOY 42	Au/Si EUTECTIC	A1	MECHANICAL	ULTRASONIC	ULTRASONIC
	B	14 PIN CERAMIC/ METAL TOP & BOTTOM	CERAMIC/Au PLATED KOVAR TOP & BOTTOM	SOLDER	Au PLATED KOVAR	A1	Au CLAD KOVAR	Au/Si EUTECTIC	A1	MECHANICAL	ULTRASONIC	ULTRASONIC
MIL-M-38510/ 05401 (4000)	C	16 PIN CERDIP	CERAMIC	GLASS FRIT	Au PLATED ALLOY 42	A1	A1 CLAD ALLOY 42	Au/Si EUTECTIC	A1	MECHANICAL	ULTRASONIC	ULTRASONIC
	D	16 PIN BOTTOM BRAZE	CERAMIC/Ni PLATED KOVAR LID	SOLDER	Ni PLATED KOVAR	A1	A1 CLAD KOVAR	Ag FILLED EPOXY	A1	MECHANICAL	ULTRASONIC	ULTRASONIC
MIL-M-38510/ 05401 (4017)	A	16 PIN CERDIP	CERAMIC	GLASS FRIT	Sn/Pb PLATED ALLOY 42	A1	A1 CLAD ALLOY 42	Au/Si EUTECTIC	A1	LASER	ULTRASONIC	ULTRASONIC
	D	16 PIN BOTTOM BRAZE	CERAMIC/Ni PLATED KOVAR LID	SOLDER	Ni PLATED KOVAR	A1	A1 CLAD KOVAR	Ag FILLED EPOXY	A1	MECHANICAL	ULTRASONIC	ULTRASONIC

the failure mechanisms exhibited by this manufacturer's devices could have been accelerated by moisture released from the epoxy.

Seventy-three devices were subjected to Gas Mass Spectrometer Analysis. This analysis was performed by RADC and the percentage of water vapor content found within the devices is shown in Table 12. A water vapor content average of 3.0% was noted within the Manufacturer B 4013B devices while the Manufacturer C 4013B devices exhibited no traces of water. The life test results were inconclusive in determining the relationship between surface related mechanisms and water vapor content.

3.4 BIAS CIRCUIT EVALUATION

Short term high temperature tests of two devices per lot of each manufacturers' device type were conducted to evaluate candidate bias circuits. The circuit evaluations were performed to verify that the following conditions existed:

a) That maximum rated voltage could be maintained across the device with minimal current at the accelerated test temperature.
b) That no abrupt change in output voltage state occurred over the anticipated range of life test temperatures, and
c) That thermal runaway did not occur at the maximum life test temperature.

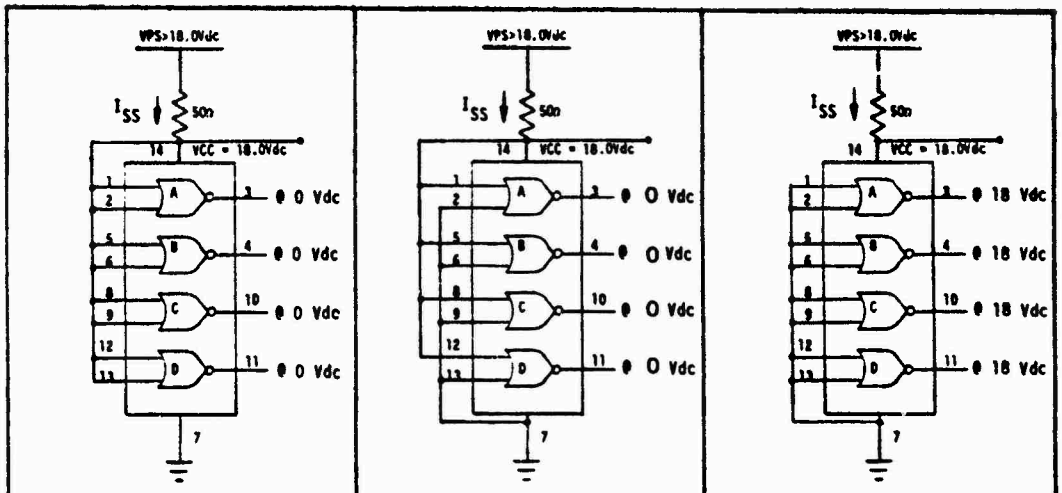
Results of the bias circuit evaluations were as follows:

3.4.1 4001B Circuit Evaluation - The results of evaluating three 4001B candidate bias circuits (A, B, and C) over the temperature range of 125°C through 275°C are shown in Figure 5. Each of the candidate bias circuits evaluated for the quadruple two-input NOR gate met the conditions stated above. Candidate Circuit A connected all inputs to V_{DD}, Circuit C connected all inputs to V_{SS}, and Circuit B connected one input of each NOR gate to V_{DD} and the other to V_{SS}. An equal number of positive and negative voltage gate oxide stresses was desirable in the CMOS devices, therefore, candidate Circuit B was selected for life test. The outputs of all NOR gates are low in this selection.

TABLE 12. WATER VAPOR CONTENT - %

MANUFACTURER	DEVICE TYPE	LOT	NO. TESTED	% AVERAGE	% RANGE
A	4001B	A	1	1.3	1.3
		B	3	1.9	1.0 - 3.0
		C	3	2.7	1.8 - 3.6
B	4001B	A	5	2.0	0.5 - 3.6
		B	5	0	0
		C	3	0	0
	4013B	A	2	3.0	2.3 - 3.7
		B	5	0	0
		C	3	0.1	0 - 0.2
C	4013B	A	5	0	0
		B	4	0	0
		C	5	0	0
	MIL-M-38510/ 05401 (4008)	A	5	0.2	0 - 0.8
		B	5	0.2	0 - 1.0
		C	5	0	0
D	MIL-M-38510/ 05401 (4008)	A	4	0.3	0.2 - 0.4
		B	5	0.2	0.1 - 0.3
		C	5	0.2	0.1 - 0.3

NOTE: MIL-M-38510/05601 (4017) DEVICES WERE NOT INCLUDED IN THE ANALYSIS



	CIRCUIT A		CIRCUIT B		CIRCUIT C	
			PREFERRED CIRCUIT			
T_A °C	I_{SS} (μA)		I_{SS} (μA)		I_{SS} (μA)	
	MFR A	MFR B	MFR A	MFR B	MFR A	MFR B
125	.35	.13	.5	.10	.6	.12
150	2.0	.77	2.27	.47	3.5	.57
175	10	4.3	9.8	2.9	11	3.6
200	30	24	46	16	40	15
225	222	111	179	72	135	61
250	868	492	637	270	462	211
275	2535	1170	2039	879	1382	637

Average I_{SS} values of six devices - two devices from each of three lots.

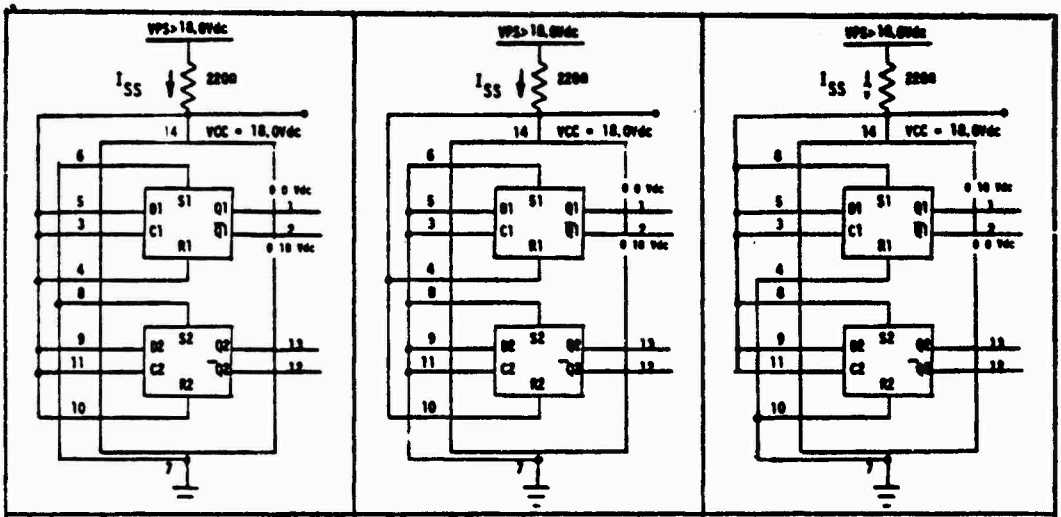
FIGURE 5. 4001B CANDIDATE BIAS CIRCUITS

3.4.2 4013B Circuit Evaluation - The results of evaluating three 4013B candidate bias circuits (A, B, and C) over the temperature range of 125°C through 275°C are as shown in Figure 6. No appreciable difference between the candidate bias circuits was observed. The selected bias circuit, Candidate B, provided a high voltage level at the Q outputs. For this output condition the reset input was connected to V_{DD} and all other inputs are connected to ground. In each of the candidate bias configurations one-half of the device transistors were biased on, and none of the circuits has an advantage over the other, therefore, Circuit B was selected. Although the Manufacturer C devices drew excessive current in each of the candidate circuits at the maximum temperature of 275°C, a 250°C life test temperature was considered safe. The onset of the excessive current condition was not observed until 265°C.

3.4.3 MIL-M-38510/05401 (4008) Circuit Evaluation - The results of the 4008 circuit evaluation tests are shown in Figure 7. These results indicated no significant difference in each of the three candidate bias circuits (A, B, and C). In each circuit the output voltages remained stable while the input currents were approximately equal. Circuit C with one modification was selected as the bias circuit for step-stress and life testing, since the modified Circuit C (Figure 8) provides all possible voltage stress combinations on the input stages of the adders.

Since both manufacturer's devices exhibited excessive current at 275°C, the maximum life test temperature was limited to 250°C. At 200°C, one Manufacturer D Lot A device did draw approximately three times the current of the other five devices on test and exhibited failed I_{SS} and V_{OH} parameters after cool-down to room temperature. However, analysis of this device indicated that the failed parameter values were not the result of excessive stresses induced by the bias circuit.

3.4.4 MIL-M-38510/05601 (4017) Circuit Evaluation - The results of the 4017 candidate bias circuit evaluation test are shown in Figure 9. Three candidate circuits (A, B, and C) were evaluated and the output voltage levels remained stable over the temperature range of 25°C to 260°C in each of the three circuits. However, Circuit A is the only circuit that provides control over

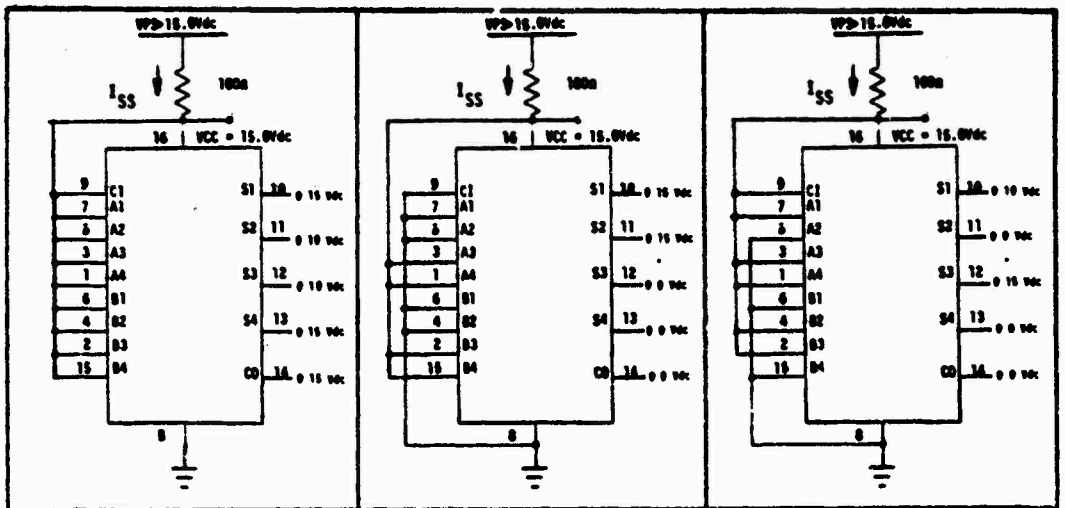


	CIRCUIT A		CIRCUIT B		CIRCUIT C	
			PREFERRED CIRCUIT			
T_A °C	I_{SS} (μA)		I_{SS} (μA)		I_{SS} (μA)	
	MFR. C	MFR. B	MFR. C	MFR. B	MFR. C	MFR. B
125	.37	.24	.47	.22	.85	.83
150	1.97	1.33	2.17	1.10	3.27	1.83
175	9.5	6.53	11.2	6.42	13.2	6.52
200	48	33.8	54.5	32.5	60	30.77
225	227	157.9	241	142	241	158.
250	881	614.6	957	559	947	605
275	*	2080	*	2208	*	2059

*THERMAL RUNAWAY

Average I_{SS} values of six devices - two devices from each of three lots.

FIGURE 6. 4013B CANDIDATE BIAS CIRCUITS

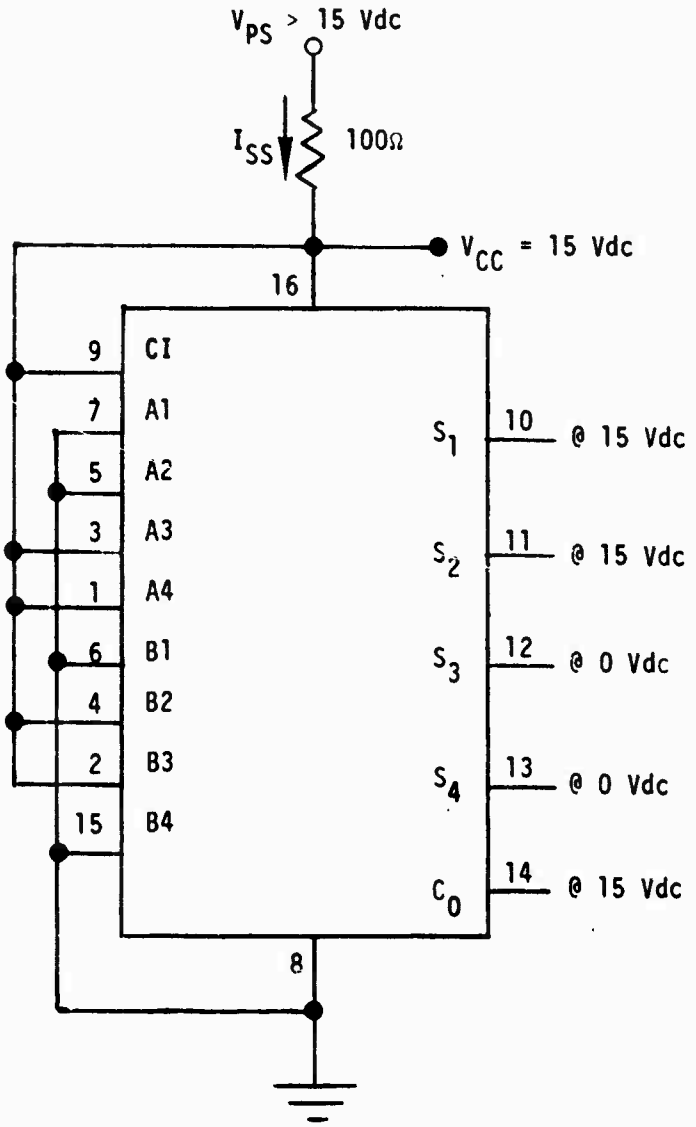


	CIRCUIT A		CIRCUIT B		CIRCUIT C	
T_A °C	I_{SS} (μA)		I_{SS} (μA)		I_{SS} (μA)	
	MFR. C	MFR. D	MFR. C	MFR. D	MFR. C	MFR. D
125	.69	.51	.79	.50	1.2	.25
150	3.1	2.6	3.2	2.1	3.7	2.3
175	14.6	14.4	14.2	15.4	15.7	14.9
200	68.2	84.7	73.1	85.8	73.9	81.6
225	293	394	246	416	323	291
250	1080	1532	1308	1685	1272	1715
275	*	*	*	*	*	*

*THERMAL RUNAWAY

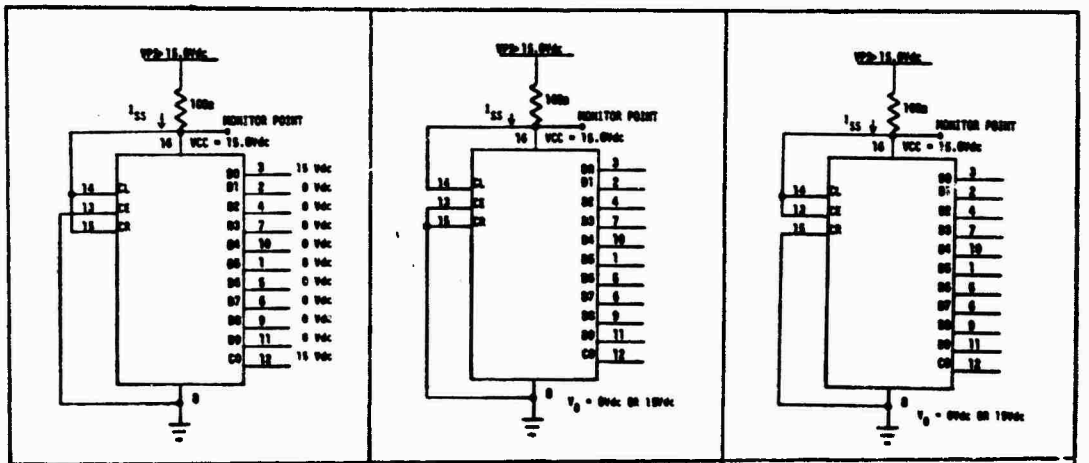
Average I_{SS} values of six devices - two devices from each of three lots

FIGURE 7. MIL-M-38510/05401 (4008) CANDIDATE BIAS CIRCUITS



1. THE ABOVE CIRCUIT DIFFERS FROM CIRCUIT C SHOWN IN FIGURE 7 BY THE CONNECTION AT THE A1 (PIN 7) INPUT. IN CIRCUIT C, A1 IS CONNECTED TO V_{CC} AND ALL OTHER INPUTS ARE THE SAME.

FIGURE 8. MIL-M-38510/05401 (4008) PREFERRED CIRCUIT



	CIRCUIT A (Preferred Circuit)		CIRCUIT B		CIRCUIT C	
T_A °C	I_{SS} (μA)		I_{SS} (μA)		I_{SS} (μA)	
	MFR. A	MFR. D	MFR. A	MFR. D	MFR. A	MFR. D
125	3.17	0.13	5.92	5.43	5.60	0.15
150	12.35	0.89	22.57	6.98	21.47	0.90
175	90.30	5.60	82.90	8.04	81.12	5.39
200	340.8	31.18	320.9	35.12	317.5	31.33
225	1140	141.1	1057	152.6	1072	143.3
250	3915	580.3	3848	619.3	3743	530.6
275	*	*	*	*	*	1940

* THERMAL RUNAWAY.

AVERAGE I_{SS} VALUES OF SIX DEVICES - TWO DEVICES FROM EACH OF THREE LOTS.

FIGURE 9. MIL-M-38510/05601 (4017) CANDIDATE BIAS CIRCUITS

the output logic levels. Output control is established in Circuit A by placing the reset input at +15 VDC (Logic 1). In circuits B and C, the reset input is grounded (Logic 0), and the logic levels of the outputs are not controlled. Thus the output logic levels appear in a random fashion upon application of device voltages. Since it is desirable to have voltage stress conditions on all devices that are repeatable after each set of electrical measurements, Circuit A is the only acceptable circuit. The maximum temperature at which devices could be safely operated in Circuit A was determined from the device current (I_{SS}) - temperature characteristics. At ambient temperatures of 250°C and below, device current averages were below 4 mA. These current levels were considered acceptable. However, above 270°C the Manufacturer A devices experienced thermal runaway. Thus, the maximum life test temperature was limited to 250°C.

3.5 STEP STRESS TESTS

After the selection of a bias configuration, 30 devices (ten per lot) of each manufacturer's device type were subjected to step stress testing. These tests were performed to further evaluate the bias configurations and to obtain additional data on device failures for the final determination of accelerated life test conditions. Each manufacturer's devices were operated in the selected bias configuration for 16 hours in a test oven at 175°C. After 16 hours of operation at 175°C, devices were allowed to cool-down under bias, and electrical testing was performed at 25°C. Surviving devices were returned to test at an ambient temperature of 200°C for an additional 16 hours of operation. This sequence was repeated in 25°C increments until a temperature of 275°C was reached, or until all surviving devices experienced thermal runaway. A summary of the step stress test results for all device types is shown in Table 13. Brief discussions of the test results for each device type are provided in the following paragraphs.

3.5.1 4001B Step Stress Results - A total of ten (four Lot A, six Lot B, and zero Lot C) Manufacturer A 4001Bs failed during the step stress test. Nine of the failed devices exhibited excessive I_{SS} due to a bake recoverable surface instability mechanism. One device failed I_{SS}, V_{OL}, and V_{OH} and the

TABLE 13. STEP STRESS RESULTS

PART TYPE	MANUFACTURER	LOT	CUMULATIVE NO. OF FAILURES				
			175°C/ 16 HR	200°C/ 32 HR	225°C/ 48 HR	250°C/ 64 HR	275°C/ 80 HR
4001B	A	A	1	1	1	1	4
		B	0	0	0	3	6
		C	0	0	0	0	0
	B	A	0	0	0	4 1 device (4)	6
		B	0	0	0	0	0
		C	0	0	0	0	2 (4)
4013B	C	A	1	1	1	2	2
		B	0	0	0	0	2
		C	2	2	2	2	2
	B	A	0	0	0	0	0
		B	1	1	1	2	2
		C	0	0	0	0	1
4008	C	A	0	1 (2)	1	2 (2)	(1)
		B (3)	0	0	0	0	
		C	0	0	0	0	
	D	A	0	0	0	0	
		B	0	1	1	1	
		C	0	0	1 (2)	1	(1)
4017	A	A	0	0	0	0	1 (5)
		B	0	0	0	0	0
		C	0	0	0	0	0
	D	A	0	0	0	2 (4)	(4) 4
		B	0	0	0	0	0
		C	1	2	9	10	10 (5)

TEN DEVICES PER LOT INTO TEST.

(1) DEVICES DREW EXCESSIVE CURRENT, TEST TERMINATED.

(2) DEVICES INADVERTENTLY REMOVED FROM TEST.

(3) EIGHT DEVICES INTO TEST.

(4) FAILED DUE TO TEST ANOMALIES.

(5) DEVICES DREW EXCESSIVE CURRENT/ TEST PERFORMED AT 260°C.

cause of failure was not determined. A total of eight (six Lot A, zero Lot B, and two Lot C) Manufacturer B 4001Bs failed during the test. The two Lot C failures and one of the Lot A failures were due to melted or migrated open metallization caused by test anomalies. The remaining five Lot A failures exhibited excessive I_{SS} due to a bake recoverable surface instability mechanism.

All of the lots were considered to be a typical production lot, however, based on failure rates shown in Table 13, the Manufacturer A Lot C and the Manufacturer B Lots B and C were expected to, and did exhibit better aging characteristics than the other lots during life testing. In addition, none of the lots exhibited a high percentage of failures at the 250°C step. Therefore, life testing at 250°C with an initial measurement point at four hours was considered reasonable.

3.5.2 4013B Step Stress Results - A total of six (two Lot A, two Lot B, and two Lot C) Manufacturer C devices failed during step stress test. All failed devices exhibited excessive I_{SS} of which four (two Lot A and two Lot B) failures were attributed to bake recoverable surface mechanisms. The two Lot C device failures were due to a degraded drain junction in a n-channel transistor caused by a mask misalignment. A total of three (zero Lot A, two Lot B, and one Lot C) Manufacturer B devices failed during step stress. All three devices exhibited excessive I_{SS} which was attributed to a bake recoverable surface related mechanism.

None of the lots exhibited abnormal failure distributions, and 250°C was considered a reasonable maximum life test temperature.

3.5.3 MIL-M-38510/05401 (4008) Step Stress Results - One Manufacturer D (Lot B) device failure was noted during step stress evaluation, and the single failure was due to excessive I_{IH1}. The failed I_{IH1} parameter was attributed to bulk degradation of an input protection diode due to electrical overstress caused by a defective test fixture.

No failures occurred in the remaining Manufacturer D (Lot A and Lot C) and Manufacturer C (Lot A, Lot B, and Lot C) devices during step stress

evaluations. However, the devices did draw excessive current at 275°C, and the maximum life test temperature was limited to 250°C.

3.5.4 MIL-M-38510/05601 (4017) Step Stress Results - One Manufacturer A (Lot A) device failure was noted during step stress evaluation. This device failed an I_{SS} parameter which was found to be due to a bake-recoverable surface instability mechanism.

Fourteen Manufacturer D (four Lot A, zero Lot B, and ten Lot C) devices failed during step stress evaluation. Nine of the Lot C devices failed an I_{SS} parameter and like the Manufacturer A device, these failures were due to a bake recoverable surface instability mechanism. One Lot C device which failed V_{OH} and V_{OL} parameters was not bake recoverable. The remaining four Lot A device failures were due to excessive I_{IH} which was attributed to degradation of an input protection diode. This degradation was found to be due to electrical overstress caused by a defective test fixture.

3.6 JUNCTION TEMPERATURE DETERMINATIONS

Upon completion of the bias circuit evaluation and step stress tests, the maximum junction temperatures that would be experienced during life testing were determined for each manufacturer's device type. The forward voltage of a substrate diode, which is a function of temperature, was used to determine device junction temperatures. Ambient temperatures and circuit configurations during the time junction temperature measurements were being performed were consistent with expected accelerated life test conditions. A MDAC-St. Louis thermal resistance tester was used to make the substrate diode forward voltage measurements. This tester permits the life test bias conditions to be established on the device under test for 99.9% of the time and only briefly (1 millisecond) forward biases the substrate diode. The largest ΔT_J calculated for all of the device types was only 3.6°C. The calculated junction temperature for each device type at each life test temperature is included in the summary of life test conditions contained in Section 5.0.

4.0 LOT ACCEPTANCE TESTS

4.1 TEST DESCRIPTION

The Lot Acceptance Tests were performed to verify the acceptability of MIL-STD-883, Method 5005.5, as an effective method for the screening of CMOS devices for Class S applications. The specified MIL-STD-883 test requires MIL-M-38510 subgroups A1, A2, and A3 electrical tests at the 120 hour point and full subgroup A electrical tests at the 250 hour point. This test is a dual gate test of 40 devices with the following accept reject criteria: at gate 1, the 120 hour point, failures are limited to 20 percent or fewer of the test sample, at gate 2 the 250 hour point, the failures are limited to 40 percent of the test sample. A particular lot must pass both gates to the above criteria in order to be accepted.

4.2 TEST RESULTS

Forty devices of one lot (labeled Lot C) from each manufacturer's device type were subjected to the full lot acceptance test. The devices were operated in the previously selected accelerated life test circuit at 250°C and were electrically tested per the specification at the 120 and 250 hour points. The results of these tests are shown in Table 14.

Also, in order to correlate the life test data and the Lot Acceptance data, group A1, A2, and A3 electrical tests were performed on the 250°C Lot A and B life tests devices at the 120 and 250 hour points. Since all but one of the Lot C acceptance test failures were detected in the group A1, A2 and A3 electrical test, it is valid to compare the 250°C life test data with the Lot C acceptance test data. A table comparing the results of these tests with respect to the MIL-STD-883, Method 5005.5 criteria, is shown in Table 15. Examination of the table shows that 37.5 percent of the lots would fail the lot acceptance criteria. With the exception of the M38510/05401 (4008) devices, there appears to be a large difference between different lots of the same manufacturer. The largest number of failures occurred in Manufacturer D's M38510/05601 (4017) test samples. Over two-thirds of these devices failed the lot acceptance criteria. The correlation of this data and the accelerated life test results is contained in detail in Section 7.0.

TABLE 14. LOT ACCEPTANCE TEST RESULTS

DEVICE	MFR	LOT	QTY	NUMBER OF FAILURES AT MEASUREMENT TIME																TOTAL NO. OF FAILURES
				120 HOURS				250 HOURS												
				DC PARAMETRIC				DC PARAMETRIC				CAP.	TRUTH TABLE	TIMING PARAMETERS						
				A	H	C	TOTAL	A	H	C	TOTAL			A	H	C	TOTAL			
4001	A	C	40	1	4	0	5	0	0	0	0	0	N/A	0	0	0	0			5
	B	C	40	4	0	0	4	3	2	2	3	0	N/A	0	0	0	0			7
4013	C	C	40	6	0	0	6	3	0	0	3	0	0	0	0	0	0			9
	B	C	40	3	2	0	5	9	1	0	10	0	0	0	0	0	0			15
M38510 /05401 (4008)	C	C	40	0	0	0	0	1	1	1	1	0	1	1	1	1	1			1
	D	C	40	4	7	0	7	3	6	0	8	0	0	0	0	0	0			15
M38510 /05601 (4017)	A	C	40	2	0	0	2	0	0	0	0	0	0	1	0	0	1			3
	D	C	40	39	0	0	39	(2)	-	-	-	0	0	0	0	0	0 (1)			39

(1) TEST PERFORMED AT 120 HOURS.

(2) TEST TERMINATED AT 120 HOURS. DYNAMIC TESTS PERFORMED ON THE ONE REMAINING GOOD DEVICE.

A = AMBIENT (25°C)
H = HOT (125°C)
C = COLD (-55°C)

TABLE 15. LOT ACCEPTANCE COMPARISON

OEVICE	MANUFACTURER	LOT	QUANTITY ON TEST	CUMULATIVE FAILURES		MIL-STD-883 METHOO 5005.5	
				120 HR	250 HR	GATE 1[1]	GATE 2[2]
4001	A	A	40	24	26	FAIL	FAIL
		B	40	27	31	FAIL	FAIL
		C	40	5	5	PASS	PASS
	B	A	40	25	35	FAIL	FAIL
		B	40	0	3	PASS	PASS
		C	40	4	7	PASS	PASS
4013	C	A	39	8	9	FAIL	PASS
		B	40	10	13	FAIL	PASS
		C	40	6	9	PASS	PASS
	B	A	40	0	1	PASS	PASS
		B	40	3	3	PASS	PASS
		C	40	5	15	PASS	PASS
M38510 /05401 (4008)	C	A	40	3	3	PASS	PASS
		B	38	1	1	PASS	PASS
		C	40	0	1	PASS	PASS
	D	A	40	3	10	PASS	PASS
		B	40	8	11	PASS	PASS
		C	40	7	15	PASS	PASS
M38510 /05601 (4017)	A	A	40	10	11	FAIL	PASS
		B	40	4	4	PASS	PASS
		C	40	2	3	PASS	PASS
	D	A	40	7	25	PASS	FAIL
		B	40	10	18	FAIL	FAIL
		C	40	39	39[3]	FAIL	FAIL

[1] FAILURES LIMITEO TO 20% OF TEST SAMPLE.

[2] FAILURES LIMITEO TO 40% OF TEST SAMPLE.

[3] TEST TERMINATED AT 120 HOURS.

5.0 LIFE TESTS

5.1 LIFE TEST CONDITIONS

The life tests conducted consisted of: a) a MIL-STD-883, 125°C, 4,000 hour life test, b) a 250°C, 4,000 hour Accelerated Life Test, and c) a 225°C, 4,000 hour Accelerated Life Test. In addition, selected 4001 and 4013 125°C and accelerated life tests were extended to 6,000 hours. The allocation of devices for each test is shown in Table 16. A summary of the life test conditions is shown in Figures 10 through 13 for each device type. The bias conditions were the same for all lots of each device type, and with the exception on the Manufacturer A 4017 devices, the resultant power dissipated in the devices was similar. The Manufacturer A Lot A 4017 devices had a different identification number on the chip surface, as was noted in Section 3.3, than the other two lots from the same Manufacturer. The Lot A device had a 7609 date code, the Lot B device had a 7628 date code, and the Lot C device a 7643 date code. The power dissipated in the Lot A devices was an order of magnitude greater than the other two lots. The construction analysis revealed no difference in layout or processing that would account for the anomoly. The sequence for performing life tests is shown in Figure 14. The schedule for electrical parameter measurement is shown in Table 3.

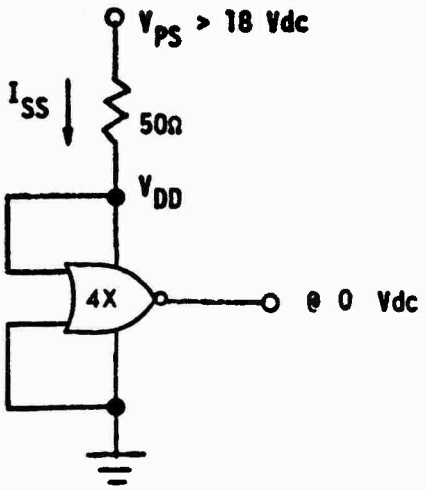
5.2 LIFE TEST RESULTS

All long term life tests, with the exception of one test cell, were continued to at least the 4,000 hour point or to the 65% failure level. Several of the 4001 and 4013 life tests which experienced low failure rates were extended to 6,000 hours. One test cell, the Manufacturer A 4017, Lot B, 250°C cell, was terminated early at the 3,000 hour point with only 18% failures to permit timely program completion. The results of the life tests are summarized in Tables 17 through 20. These tables show the cumulative number of devices failing the interim and final electrical tests.

Examination of these tables shows that the 125°C life test resulted in only a total of 6% failures, with the worst case test cell exhibiting less than 18% failures. The long term high temperature accelerated life tests resulted in 63% of the total devices failing. Figure 15 shows the percentage of devices failed by part type, manufacturer, and lot.

TABLE 16. ALLOCATION OF DEVICES

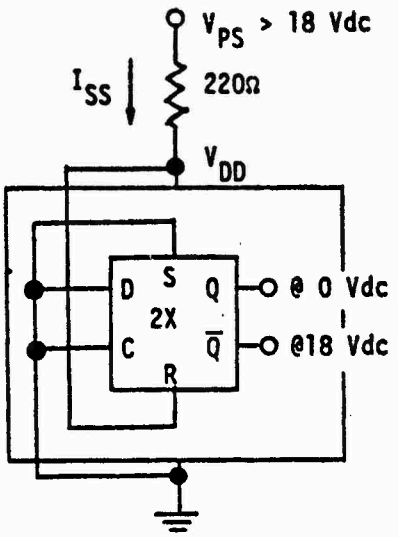
OEVICE	MFR	LOT	TEST			
			250°C, 250 HOUR LOT ACCEPTANCE	MIL-STO-883 125°C LIFE	225°C ACCELERATEO LIFE	250°C ACCELERATEO LIFE
4001	A	A	-	20	40	40
		B	-	20	40	40
		C	40	-	-	-
	B	A	-	20	40	40
		B	-	20	40	40
		C	40	-	-	-
4013	C	A	-	20	38	39
		B	-	20	40	40
		C	40	-	-	-
	B	A	-	20	40	40
		B	-	20	40	40
		C	40	-	-	-
4008	C	A	-	20	40	40
		B	-	20	38	38
		C	40	-	-	-
	0	A	-	20	40	40
		B	-	20	40	40
		C	40	-	-	-
4017	A	A	-	20	40	40
		B	-	20	40	40
		C	40	-	-	-
	0	A	-	20	40	40
		B	-	20	40	40
		C	40	-	-	-



MANUFACTURER	T_A AMBIENT TEMPERATURE (°C)	LOT	V_{DD} DEVICE VOLTAGE (VOLTS)	I_{SS} DEVICE CURRENT (MICRO AMPS)	P_d POWER DISSIPATION (MILLI WATTS)	T_J JUNCTION TEMPERATURE (°C)
A	125	A	18	.6	.011	127.2
		B	18	.6	.011	126.7
	225	A	18	180	3.2	226.7
		B	18	215	3.9	226.6
	250	A	18	636	11.4	252.4
		B	18	753	13.5	252.4
		C	18	523	9.4	252.0
B	125	A	18	.4	.007	127.4
		B	18	.2	.004	127.7
	225	A	18	85	1.54	226.5
		B	18	77	1.39	226.3
	250	A	18	322	5.8	251.8
		B	18	283	5.1	251.6
		C	18	205	3.7	251.4

DEVICE CONDITIONS ARE APPROXIMATE AVERAGE VALUES

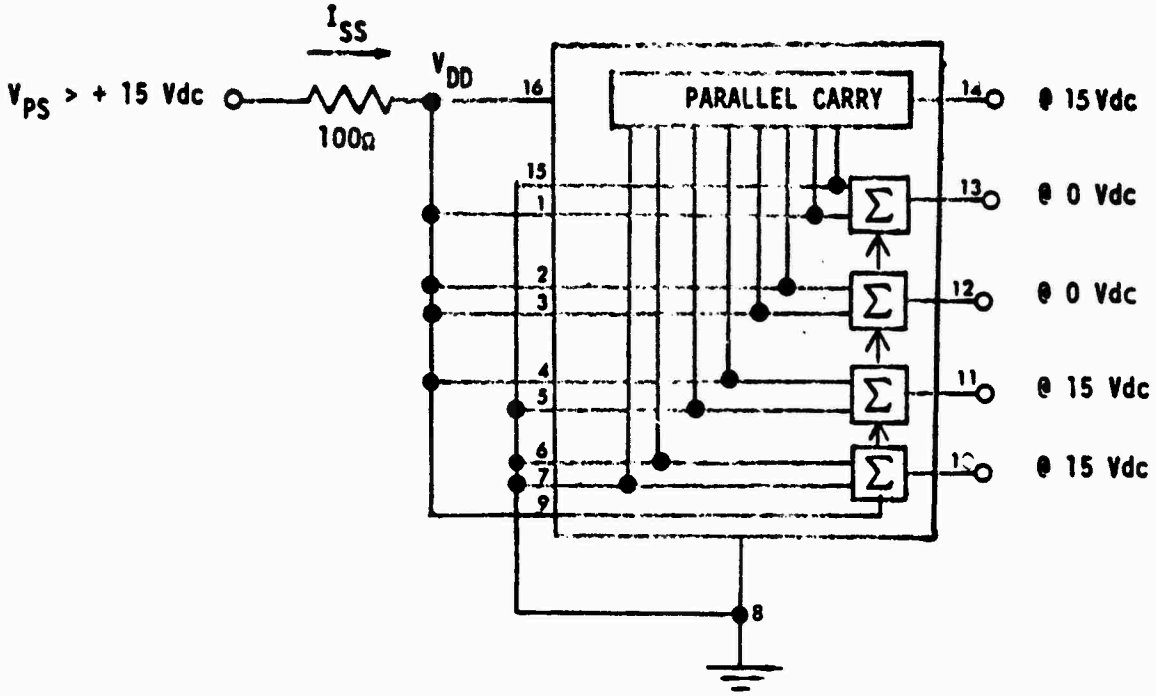
FIGURE 10. 4001B SUMMARY OF LIFE TEST CONDITIONS



MANUFACTURER	T_A AMBIENT TEMPERATURE (°C)	LOT	V_{DD} DEVICE VOLTAGE (VOLTS)	I_{SS} DEVICE CURRENT (MICRO AMPS)	P_d POWER DISSIPATION (MILLI WATTS)	T_J JUNCTION TEMPERATURE (°C)
C	125	A	18	.64	.011	125.0
		B	18	.25	.005	125.0
	225	A	18	270	4.8	225.2
		B	18	216	3.9	225.2
	250	A	18	1081	19.0	250.5
		B	18	862	15.2	250.6
		C	18	927	16.3	250.5
B	125	A	18	.16	.003	125.1
		B	18	.25	.005	125.1
	225	A	18	137	2.5	225.2
		B	18	153	2.8	225.2
	250	A	18	544	9.7	250.5
		B	18	608	10.8	250.6
		C	18	526	9.4	250.6

DEVICE CONDITIONS ARE APPROXIMATE AVERAGE VALUES

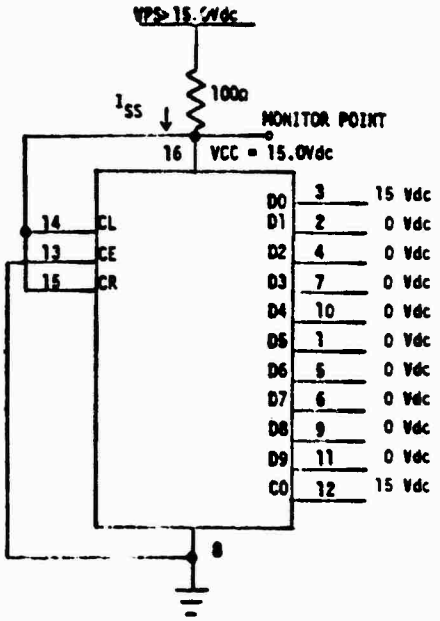
FIGURE 11. 4013B SUMMARY OF LIFE TEST CONDITIONS



MANUFACTURER	T_A AMBIENT TEMPERATURE (°C)	LOT	V_{DD} DEVICE VOLTAGE (VOLTS)	I_{SS} DEVICE CURRENT (MICRO AMPS)	P_d POWER DISSIPATION (MILLI WATTS)	T_J JUNCTION TEMPERATURE (°C)
C	125	A	15	.875	.013	125.1
		B	15	1.32	.020	125.3
	225	A	15	330	4.94	225.4
		B	15	250	3.75	225.3
	250	A	15	1181	17.5	250.6
		B	15	954	14.3	250.6
		C	15	1681	24.9	251.9
D	125	A	15	.32	.005	126.1
		B	15	.36	.005	126.8
	225	A	15	354	5.29	225.7
		B	15	390	5.84	225.6
	250	A	15	1482	21.8	252.0
		B	15	1709	25.1	251.7
		C	15	1838	27	251.7

DEVICE CONDITIONS ARE APPROXIMATE AVERAGE VALUES

FIGURE 12. MIL-M-38510/05401 (4008) SUMMARY OF LIFE TEST CONDITIONS



MANUFACTURER	T_A AMBIENT TEMPERATURE (°C)	LOT	V_{DD} DEVICE VOLTAGE (VOLTS)	I_{SS} DEVICE CURRENT (μA)	P_d POWER DISSPIATION (mW)	T_J JUNCTION TEMPERATURE (°C)
A	125	A	15	16.1	0.24	125.1
		B		0.4	0.01	125.0
	225	A		2320	34.8	226.2
		B		535	8.03	225.5
	250	A		7845	118	253.6
		B		1990	29.9	251.3
		C		1910	28.7	251.6
D	125	A		0.1	0.00	125.0
		B		0.2	0.00	125.0
	225	A		124	1.86	225.6
		B		169	2.54	225.8
	250	A		525	7.88	251.0
		B		698	10.3	251.1
		C	15	528	7.92	251.5

DEVICE CONDITIONS ARE APPROXIMATE AVERAGE VALUES.

FIGURE 13. MIL-M-38510/07601 (4017) SUMMARY OF LIFE TEST CONDITIONS

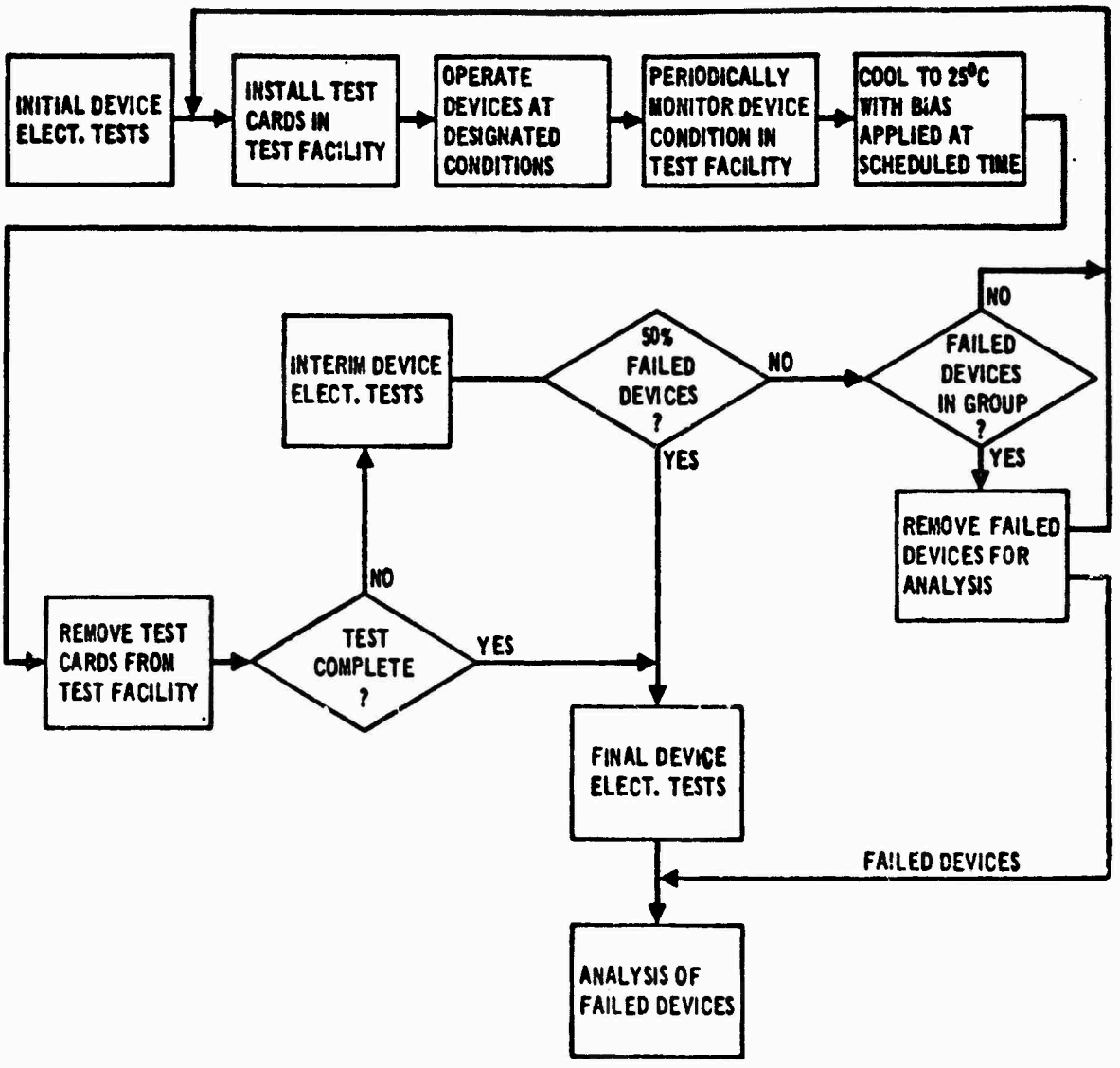


FIGURE 14. - LIFE TESTING SEQUENCE

TABLE 17. ACCELERATED LIFE TEST RESULTS - 4001

PART	CELL	LOT	MFR. CODE	QTY	TEMP	CUMULATIVE NO. OF FAILURES												
						4	8	16	32	64	120 △1	250 △1	500	1000	2000	4000	FINAL △1	5000 △1
4001	A111	A	A	40	250	2	10	13	19	22	24	26	26	26	28	29	29	-
	A112	A		40	225	1	1	1	3	6	12	15	17	19	20	23	23	-
	D110	A		20	125	--	--	--	--	--	0	0	0	0	0	0	0	0
	B111	B		40	250	3	9	14	19	24	27	31	32	TESTING TERMINATED			-	-
	B112	B		40	225	0	0	3	6	9	12	18	22	25	33	37	37	-
	D110	B		20	125	--	--	--	--	--	1	1	1	1	1	1	1	2
	A411	A	B	40	250	8	11	13	17	22	25	35	TESTING TERMINATED				-	-
	A412	A		40	225	1	7	10	10	15	18	28	33	TESTING TERMINATED			-	-
	D410	A		20	125	--	--	--	--	--	0	0	1	1	2	2	2	3
	B411	B		40	250	0	0	0	0	0	0	3	5	11	17	25	25	-
	B412	B		40	225	0	0	0	1	1	1	1	1	3	3	6	6	16
	D410	B		20	125	--	--	--	--	--	0	0	0	0	1	1	1	1

△1 PARAMETRIC TESTING PERFORMED AT 25°C, -55°C and 125°C AT THE 120, 250 AND FINAL HOUR POINTS.
PARAMETRIC TESTING PERFORMED AT 25°C ONLY AT ALL OTHER POINTS.

TABLE 18. ACCELERATED LIFE TEST RESULTS - 4013

PART	CELL	LOT	MFR. CODE	QTY	TEMP	CUMULATIVE NO. OF FAILURES												
						4	8	16	32	64	120 ⚠	250 ⚠	500	1000	2000	4000	FINAL ⚠	6000 ⚠
4013	A221	A	C	39	250	4	4	5	5	7	8	9	9	9	12	13	15	20
	A222	A		38	225	0	0	0	0	0	1	1	1	1	9	12	19	-
	0220	A		20	125	--	--	--	--	--	1	1	1	1	1	1	1	1
	B221	B		40	250	5	7	7	8	9	10	13	18	24	35	36	37	-
	B222	B		40	225	4	4	4	4	5	5	10	11	13	19	27	27	-
	D220	B	↓	20	125	--	--	--	--	--	4	5	5	6	6	6	6	6
	A421	A	B	40	250	0	0	0	0	0	0	1	1	1	1	1	1	1
	A422	A		40	225	0	0	0	0	0	0	0	0	0	1	1	1	3
	D420	A		20	125	--	--	--	--	--	0	0	0	0	0	0	0	0
	B421	B		40	250	3	3	3	3	3	3	3	3	4	6	14	15	20
	B422	B		40	225	0	0	0	0	1	1	1	1	1	1	1	3	3
↓	D420	B	↓	20	125	--	--	--	--	--	0	0	0	0	0	0	0	0

⚠ PARAMETRIC TESTING PERFORMED AT 25°C, -55°C AND 125°C AT THE 120, 250 AND FINAL HOUR POINTS.
PARAMETRIC TESTING PERFORMED AT 25°C ONLY AT ALL OTHER POINTS.

TABLE 19. ACCELERATED LIFE TEST RESULTS - M38510/05401 (4008)

PART	CELL	LOT	MFR. CODE	QTY	TEMP	CUMULATIVE NO. OF FAILURES											
						4	8	16	32	64	120 ⚠	250 ⚠	500	1000	2000	4000	FINAL ⚠
4008	A231	A	C	40	250	0	0	0	0	0	3	3	4	7	14	23	25
	A232	A		40	225	0	0	1	3	4	6	6	6	6	11	15	18
	D230	A		20	125	--	--	--	--	--	0	0	1	1	1	2	2
	B231	B		38	250	0	0	0	0	0	1	1	2	2	9	13	14
	B232	B		38	225	0	0	0	0	0	1	3	3	4	6	10	11
	D230	B		20	125	--	--	--	--	--	0	1	1	1	1	1	1
	A331	A	D	40	250	0	0	0	0	0	3	10	18	39	--	--	40
	A332	A		40	225	0	0	0	1	2	5	8	9	17	30	40	--
	D330	A		20	125	--	--	--	--	--	0	0	0	0	0	1	7
	B331	B		40	250	1	1	2	2	4	8	11	37	--	--	--	37
	B332	B		40	225	1	1	2	2	2	5	8	12	12	36	--	40
	D330	B		20	125	--	--	--	--	--	0	0	0	0	0	0	5

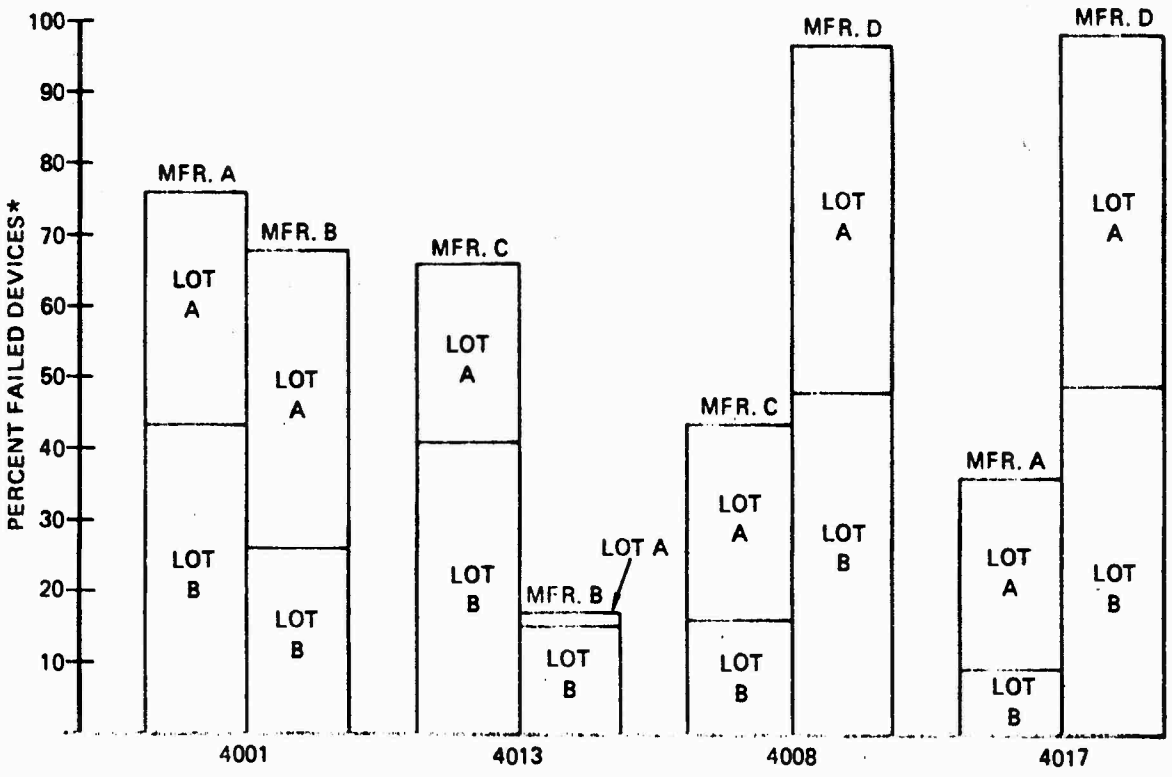
⚠ Parametric testing performed at 25°C, -55°C and 125°C at the 120, 250 and final hour points.
Parametric testing performed at 25°C only at all other points.

TABLE 20. ACCELERATED LIFE TEST RESULTS - M38510/05601 (4017)

PART	CELL	'LOT	MFR. CODE	QTY	TEMP	CUMULATIVE NO. OF FAILURES											
						4	8	16	32	64	120 △1	250 △1	500	1000	2000	4000	FINAL △1
4017	A141	A	A	40	250	2	2	2	2	2	10	11	12	15	21	25 △2	28
	A142	A		40	225	1	2	2	2	3	3	7	9	11	14	16	18
	D140	A		20	125	-	-	-	-	-	2	2	2	2	2	2	2
	B141	B		40	250	0	0	0	0	1	4	4	4	4	4	7 △2	8
	B142	B		40	225	1	1	1	1	1	1	1	1	2	5	8	8
	D140	B		20	125	-	-	-	-	-	0	0	0	0	0	0	0
	A341	A	D	40	250	1	2	3	3	4	7	25	40	-	-	-	-
	A342	A		40	225	0	0	0	0	1	3	9	13	22	40	-	-
	D340	A		20	125	-	-	-	-	-	1	2	2	2	5	6	6
	B341	B		40	250	1	2	2	2	4	10	18	38	-	-	-	38
	B342	B		40	225	1	1	1	1	2	4	9	12	14	37	-	40
	D340	B		20	125	-	-	-	-	-	0	0	0	0	0	0	0

△1 PARAMETRIC TESTING PERFORMED AT 25°C, -55°C AND 125°C AT THE 120, 250 AND FINAL HOUR POINTS. PARAMETRIC TESTING PERFORMED AT 25°C ONLY AT ALL OTHER POINTS.

△2 TERMINATED AT 3,000 HOUR POINT.



*TOTALS MADE AT TOTAL TIME FOR EACH PART TYPE.

FIGURE 15. COMPARISON OF DEVICES FAILED DURING LONG TERM HIGH TEMPERATURE ACCELERATED TESTS

6.0 FAILURE ANALYSIS

A total of sixty-eight (68) devices failed initial electrical tests. Because initial electrical failures are generally caused by subtle processing variations rather than any degradation mechanism, no formal analysis was performed on these devices. However, 62 of the failed devices were baked for 16 hours at 250°C and retested. Fifteen devices recovered, indicating that their failure was the result of a surface instability mechanism induced during processing or screening. The 47 devices that did not recover after the bake were delidded and examined optically. No device contained any obvious anomaly which could account for the failure. This indicated that these failures were probably caused by processing variations or by subtle defects.

All step stress, lot acceptance, and life test failures were analyzed in detail and summaries of the failure analysis findings by device type and manufacturer are shown in Appendix D. The goal of the failure analysis was to determine the specific element or junction responsible for the failure symptoms and then establish the specific failure mode, mechanism, and the probable cause of failure. However, this goal was not always completely achieved in the case of surface related (recoverable) failures because of the nature of the failures and the complexity of the device types. For reasons detailed in Appendix D, the specific leaky transistor or junction could not always be pin-pointed, within the scope of this program, and therefore the specific failure mechanism, such as cation drift, charge separation, etc., could not be determined. Consequently, these failures are categorized in the general classification of surface instability.

7.0 DATA EVALUATION AND CORRELATIONS

Evaluations and correlation of the data generated during the program were performed to determine microcircuit aging characteristics. This was accomplished through comparison of the failure modes observed in each test, plots of failure distributions, Arrhenius model evaluations, and calculations of use-temperature failure rates. The determination of failure distributions, Arrhenius model parameters and use-temperature failure rates generally followed published techniques [2], [3] and [4].

7.1 FAILURE MECHANISM INDENTIFICATION

The types of failure mechanisms which resulted in electrical parameter failures at 25°C during step stress, lot acceptance and life testing are shown by device lots in Tables 21 thru 24, and are summarized in Table 25. Seventy-eight failures were caused by test related problems (electrical overstress, open chassis solder joints, etc.). Of the remaining failures, 81% were due to surface related mechanisms. All of these failures most probably were caused by ionic contamination in or on the passivation layers. Sixteen percent (16%) of the failures were the result of package related mechanisms, lead (Pb) reduction and nickel migration. Two percent (2%) of the failures were undefined and 1% were due to miscellaneous mechanisms. A summary of the types of defects which initiated the mechanisms and the suspected causes of the defects is shown in Table 26. The absolute cause of failure in many instances could not be determined. Consequently many of the failures identified as process-related may ultimately or indirectly involve the design or materials of the part. Nevertheless, the failures attributed to process related problems probably can be reduced by a tightening of process controls.

7.2 FAILURE TIME CALCULATION

The failed devices exhibited out of tolerance parameter values or, in a few cases, catastrophic failures. At each measurement time, the values of the test parameters were recorded. After a device had failed, the failed parameter value and the previous nonfailed values of that parameter, with

TABLE 21. SUMMARY OF THE 4001B 25°C ELECTRICAL FAILURES

FAILURE MECHANISMS	MANUFACTURER A				MANUFACTURER B			
	LOT A	LOT B	LOT C	TOTAL	LOT A	LOT B	LOT C	TOTAL
CATION DRIFT	44	61	1	106	58	7	-	65
CHARGE SEPARATION	-	6	-	6	-	-	-	-
DENDRITE GROWTH	6	5	-	11	-	-	-	-
LOSS OF HERMETICITY	-	-	-	-	17	25	2	44
Al WIRE SAG	2	3	-	5	-	-	-	-
ELECTRICAL OVERSTRESS	1	-	-	1	1	8	7	16
NONE (TEST ERROR)	2	2	-	4	1	-	-	1
UNDEFINED	1	-	-	1	-	-	-	-
TOTAL	56	77	1	134	77	40	9	126

TABLE 22. SUMMARY OF THE 4013B 25°C ELECTRICAL FAILURES

FAILURE MECHANISMS	MANUFACTURER B				MANUFACTURER C			
	LOT A	LOT B	LOT C	TOTAL	LOT A	LOT B	LOT C	TOTAL
SURFACE INSTABILITY	1	14	4	19	5	3	-	8
CATION DRIFT	-	-	-	-	6	59	8	73
CHARGE SEPARATION	1	-	-	1	7	5	-	12
CHARGE ACCUMULATION	-	4	8	12	-	-	-	-
DENDRITE GROWTH	-	-	-	-	12	2	-	14
Al-Si ALLOYING	-	-	-	-	-	-	2	2
ELECTRICAL OVERSTRESS	-	-	-	-	2	-	1	3
UNDEFINED	2	4	1	7	1	-	-	1
TOTAL	4	22	13	39	33	69	11	113

TABLE 23. SUMMARY OF THE MIL-M-38510/05401 (4008) 25°C ELECTRICAL FAILURES

FAILURE MECHANISMS	MANUFACTURER D				MANUFACTURER C			
	LOT A	LOT B	LOT C	TOTAL	LOT A	LOT B	LOT C	TOTAL
SURFACE INSTABILITY	58	54	2	114	26	8	1	35
CHARGE SEPARATION	4	5	4	13	1	1	-	2
DENDRITE GROWTH	-	-	-	-	8	7	-	15
ELECTRICAL OVERSTRESS	7	9	1	17	-	-	-	-
NONE (TEST ERROR)	1	-	1	2	4	3	-	7
UNDEFINED	-	-	-	-	-	1	-	1
TOTAL	70	68	8	146	39	20	1	60

TABLE 24. SUMMARY OF THE MIL-M-38510/05601 (4017) 25°C ELECTRICAL FAILURES

FAILURE MECHANISMS	MANUFACTURER A				MANUFACTURER D			
	LOT A	LOT B	LOT C	TOTAL	LOT A	LOT B	LOT C	TOTAL
SURFACE INSTABILITY	12	1	1	14	23	30	-	53
CATION DRIFT	7	1	-	8	-	5	48	53
CHARGE SEPARATION	-	-	-	-	38	14	-	52
DENDRITE GROWTH	13	10	-	23	-	-	-	-
NICKEL MIGRATION	-	-	-	-	12	11	-	23
ELECTRICAL OVERSTRESS	-	-	-	-	8	14	-	22
NONE (TEST ERROR)	1	-	-	1	4	-	-	4
UNDEFINED	1	-	2	3	3	-	1	4
TOTAL	34	12	3	49	88	74	49	211

TABLE 25. FAILURE MECHANISMS SUMMARY OF THE 25°C ELECTRICAL FAILURES

FAILURE MECHAMISMS	DEVICE TYPE								
	4001		4013		4008		4017		TOTAL
	MFR A	MFR B	MFR B	MFR C	MFR D	MFR C	MFR A	MFR D	
SURFACE INSTABILITY	-	-	19	8	114	35	14	53	243
CATION DRIFT	106	65	-	73	-	-	8	53	305
CHARGE SEPARATION	6	-	1	12	13	2	-	52	86
CHARGE ACCUMULATION	-	-	12	-	-	-	-	-	12
DENDRITE GROWTH	11	-	-	14	-	15	23	-	63
NICKEL MIGRATION	-	-	-	-	-	-	-	23	23
LOSS OF HERMETICITY	-	44	-	-	-	-	-	-	44
Al WIRE SAG	5	-	-	-	-	-	-	-	5
Al-Si ALLOYING	-	-	-	2	-	-	-	-	2
ELECTRICAL OVERSTRESS	1	16	-	3	17	-	-	22	59
NONE (TEST ERROR)	4	1	-	-	2	7	1	4	19
UNDEFINED	1	-	7	1	-	1	3	4	17
TOTAL	134	126	39	113	146	60	49	211	678

TABLE 26. SUMMARY OF DEFECTS/CAUSES OF THE 25°C ELECTRICAL FAILURES

DEFECT CATEGORY	4001		4013		4017		4008		TOTALS
	MFR A	MFR B	MFR B	MFR C	MFR A	MFR D	MFR D	MFR C	
SURFACE	112	65	32	93	22	158	127	37	646
PACKAGE	11	44	-	14	23	23	-	15	130
DIE (SCRIBE)	5	-	-	-	-	-	-	-	5
OXIDE (MASK)	-	-	-	2	-	-	-	-	2
ELECTRICAL OVERSTRESS	1	16	-	3	-	22	17	-	59
TEST ERROR	4	1	-	-	1	4	2	7	19
UNDEFINED	1	-	7	1	3	4	-	1	17
TOTAL	134	126	39	113	49	211	146	60	878
CAUSE CATEGORY									
PROCESS	112	65	32	93	22	158	127	37	646
MATERIALS	11	-	-	14	23	-	-	15	63
WORKMANSHIP	5	18	-	2	-	23	-	-	48
DESIGN	-	26	-	-	-	-	-	-	26
TEST	5	17	-	3	1	26	19	7	78
UNDEFINED	1	-	7	1	3	4	-	1	17

the corresponding measurement times were used to generate an empirical equation that related time to the parameter value. Solving the empirical equation, using the failed parameter limit provided an interpolated estimate of the actual failure time. When a device exhibited more than one failed parameter, the parameter which was related to the primary failure mechanism was used. Various equations were evaluated in an attempt to provide a good fit to the data points. Interpolation of the estimated failure time was made on all devices using a linear equation with the parameter value versus test measurement times, and versus the natural logarithm of the test measurement times. Also, interpolations were made using a quadratic equation with the parameter value versus the actual, and versus the natural logarithm of the test measurement times [5]. For the out-of-tolerance failures, the three point logarithmic quadratic equation method seemed to provide the best fit. For those failures where there was a sudden shift in the data, such as for a catastrophic failure, the above methods did not provide a good fit to the data, and the midpoint between the two electrical measurement times was used.

7.3 FAILURE DISTRIBUTIONS

Distributions of the times to failure were determined for each lot of each manufacturer's device type whenever sufficient data was available. Those failures due to test related problems, and due to life test fixture related problems were not included in the distributions. Also not included in the distributions were the 125°C and -55°C failures that did not subsequently fail at 25°C. They were not included in these particular distributions because measurements were not made at -55°C and 125°C at every measurement. Only a few of the devices exhibited sufficient failures during the 4000 hour MIL-STD-883 125°C life test to determine a failure distribution.

The failure time distributions were originally assumed to be bimodal distributions that could be represented by two single lognormal distributions [6]: an early distribution of failures (Freak), and a later distribution of failures (Main). This bimodal distribution is:

$$\text{Cdf}\{\text{life}\}_{\text{TOTAL}} = \left| \frac{1}{\sigma_F \sqrt{2\pi}} \int_0^t \frac{1}{t'} \exp \left| - \frac{(\ln t' - \mu_F)^2}{2\sigma_F^2} \right| dt' \right| \quad (\%_F)$$

$$+ \left| \frac{1}{\sigma_M \sqrt{2\pi}} \int_0^t \frac{1}{t'} \exp \left| - \frac{(\ln t' - \mu_M)^2}{2\sigma_M^2} \right| dt' \right| \quad (\%_M) \qquad (1)$$

where:

μ_F = ln (median life of the Freak Distribution)

σ_F = standard deviation of the Freak Distribution

μ_M = ln (median life of the Main Distribution)

σ_M = standard deviation of the Main Distribution

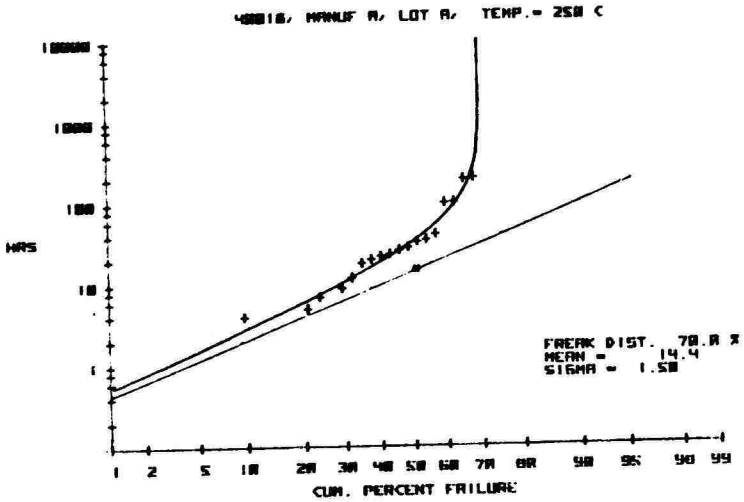
$\%_F$ = the percentage of the total population that is described by the Freak Distribution

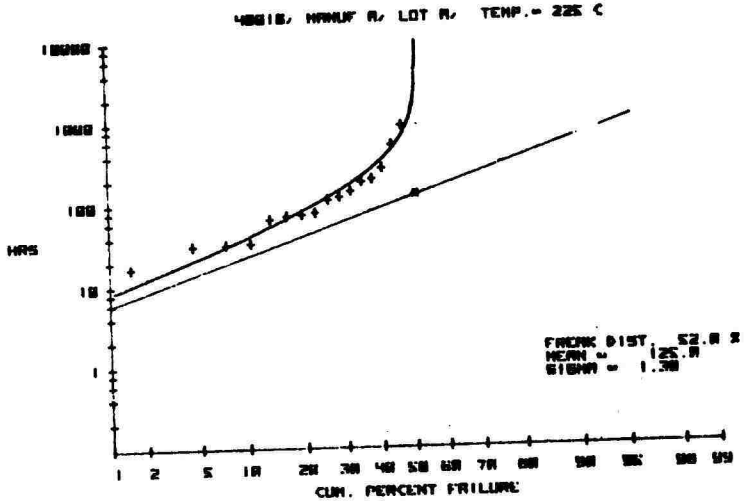
$\%_M$ = the percentage of the total population that is described by the Main Distribution

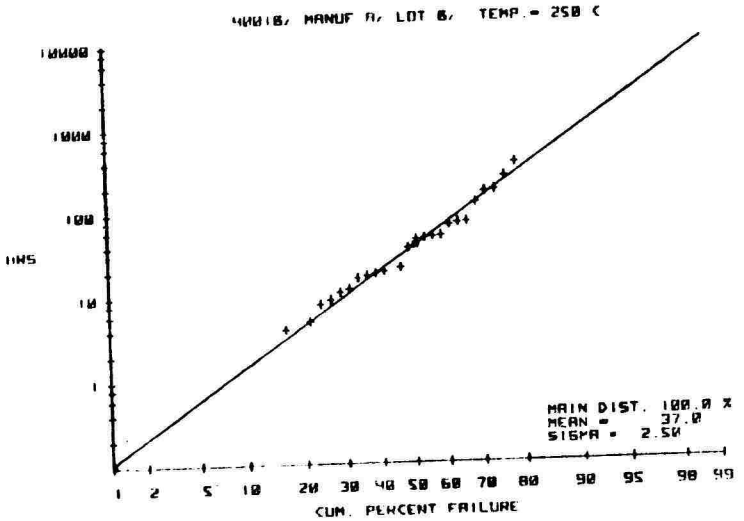
t = use time

The bimodal distribution was initially fitted using a graphical method [3], [4]. Then the graphic result was used with equation (1) and the calculated probability was compared to the test probability at each failure time. From this starting point, the values of the unknowns in equation (1) were iterated and the probabilities compared until plots of the resulting equation appeared to provide good representations of the observed data.

7.3.1 4001B Failure Distributions - The predominant failure mechanism for the Manufacturer A 4001 devices was excessive I_{DSS} current, probably caused by cation contamination. This mechanism predominated in both lots. The Lot B devices also exhibited a few failures due to a degraded input-to-V_{SS} protection diode, probably caused by mobile ions in or on a passivation layer. These two mechanisms are both surface related and the combined failure distributions for these mechanisms are shown in Figure 16. The failures due







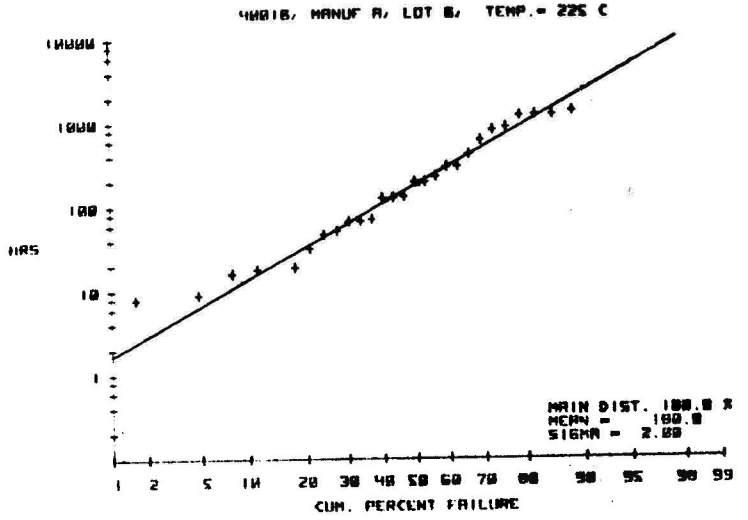


FIGURE 16. MANUFACTURER A 4001B FAILURE DISTRIBUTION PLOTS - SURFACE RELATED

to dendrite growth, a package related mechanism, were not included in the failure distributions and did not exhibit sufficient failures to plot separately. Also not included were the failures due to wire-to-die shorts caused by hillocks from the laser scribing. This mechanism is primarily a temperature cycling mechanism and not a time-temperature related mechanism.

The curves of Manufacturer A's Lot A 4001B device seem to indicate the possibility of a bimodal distribution, but there is insufficient data to make a determination of the Main median life. The early or Freak population represents an average of 61% of the Lot A devices. The Lot B devices exhibited a single lognormal distribution.

Thirty-five percent of Manufacturer B's 4001B failures were due to loss of hermeticity, and since this is a temperature cycling mechanism, the devices were not included in the failure distribution plots. Fifteen of the remaining sixty-four failures were delidded without being leak tested to avoid affecting their leakage currents. These devices exhibited the same failure symptoms as the hermetic devices, and were included in the failure distributions. The primary failure mechanism for the hermetic devices was determined to be cation drift or charge separation caused by contamination in the passivation layer. The failure distributions for this mechanism are shown in Figure 17. Both lots of devices tended to exhibit a bimodal failure distribution, but the Lot B devices had only a few hermetic devices remaining, and the failure distributions are best estimates of the actual distributions. There were also three lot A failures in the MIL-STD-883 life test which were due to the same mechanism, and this distribution is shown in Figure 18.

7.3.2 4013B Failure Distributions - The predominant failure symptom of the Manufacturer B's 4013B devices was excessive device current (I_{SS}). This failure symptom was exhibited by 84% of Manufactuer B's failed devices . Eighty-one percent of the I_{SS} failures were reversible, indicative of surface related mechanisms. However, the devices failed various combinations of the three I_{SS} tests, and this indicated several failure modes. Seven

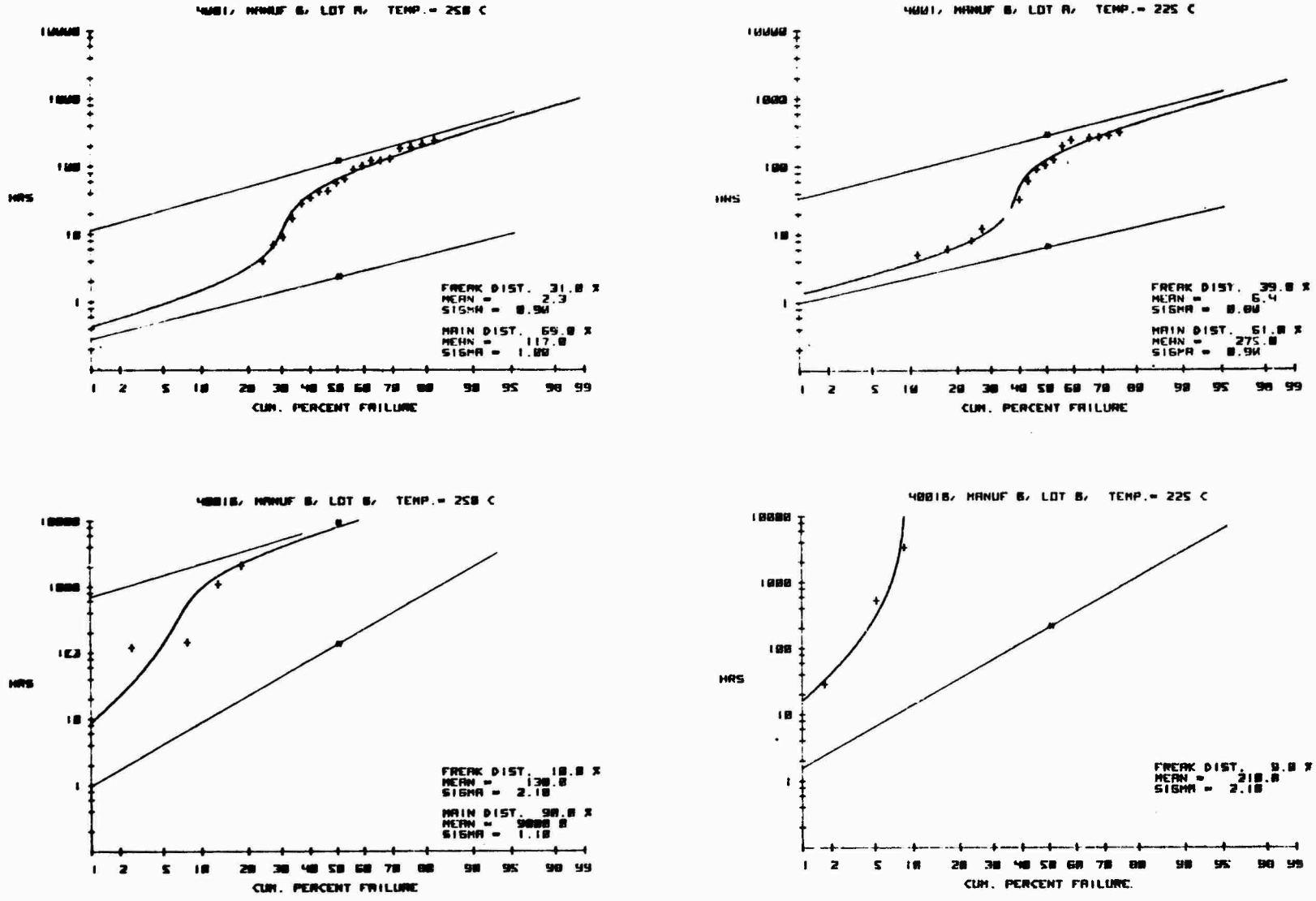


FIGURE 17. MANUFACTURER B 4001B FAILURE DISTRIBUTIONS - SURFACE RELATED

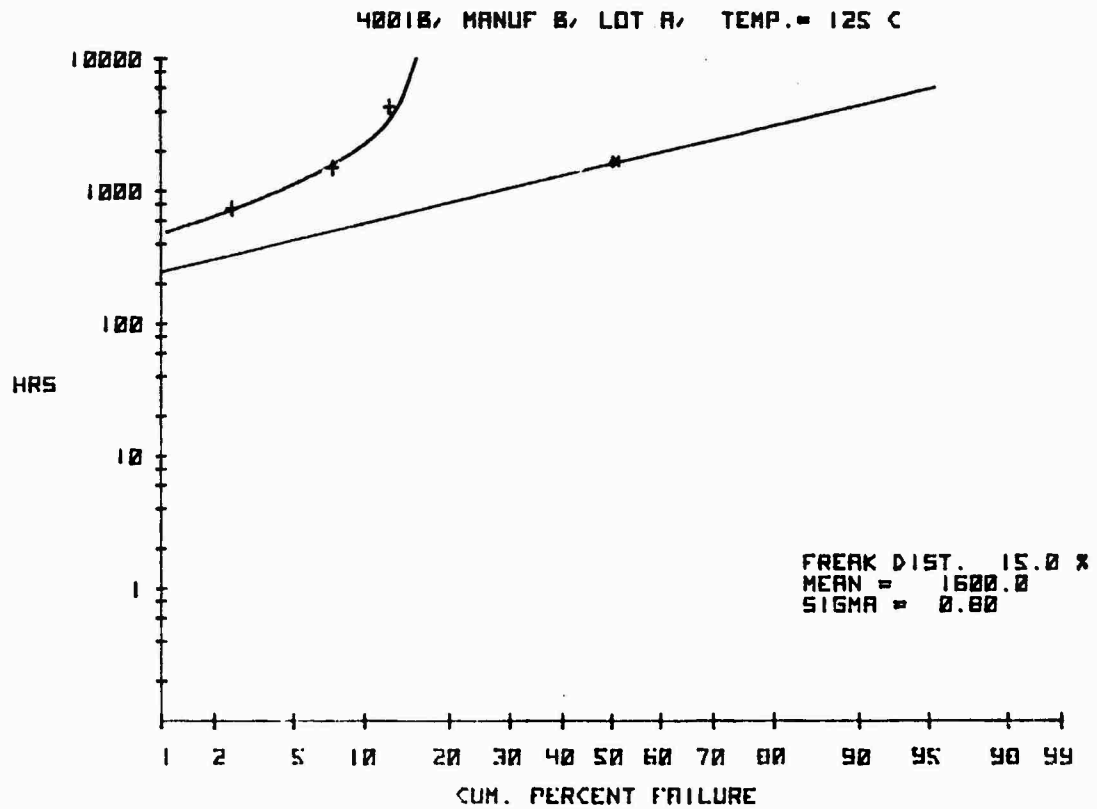


FIGURE 18. MANUFACTURER B LOT A 4001B 125°C FAILURE DISTRIBUTION - SURFACE RELATED

devices failing I_{SS} were not bake recoverable, but failure analyses did not determine the exact failure mechanism. One device also failed I_{IL1} due to charge separation, also a surface related mechanism. Only one Manufacturer B life test cell (250°C - Lot B) exhibited sufficient failures to generate a failure distribution plot, and this plot is shown in Figure 19. The only failures excluded from this distribution were the 125°C only failures. The distribution plot suggests a bimodal distribution with 92% of devices in the Main population. However, there was insufficient Freak population failure time resolution to determine the median life or the standard deviation of the Freak population.

The Manufacturer C 4013 devices exhibited several surface related mechanisms. The devices also exhibited a few failures due to a package related mechanism, the shorting of a pin to the header caused by dendrite growth. There were insufficient dendrite growth failures to plot a failure distribution. All surface related mechanisms were combined to plot the failure distributions shown in Figure 20. The Lot A devices exhibited a bimodal failure distribution with 12% to 25% of the devices in the Freak population. The Main population had a median life of approximately 10,000 hours at 250°C, but the Main failure distribution could not be determined for the 225°C devices. The Lot B devices also exhibited a bimodal distribution and in this case the Freak population median life accounted for an average of 18% of the population, and the Freak median life was 2.0 hours at 250°C and 2.5 hours at 225°C.

The MIL-STD-883 125°C life test of Manufacturer C's 4013 devices also generated sufficient failures to determine a failure distribution for the Freak population. This distribution is shown in Figure 21.

7.3.3 MIL-M-38510/05401 (4008) Failure Distribution - The Manufacturer D MIL-M-38510/05401 (4008) devices exhibited two surface related mechanisms. The largest group of failures was attributed to surface instability caused by ionic contamination. The other valid test failures were attributed to charge separation in an input protection diode, also caused by ionic contamination. The failure distributions for the surface related mechanisms, shown

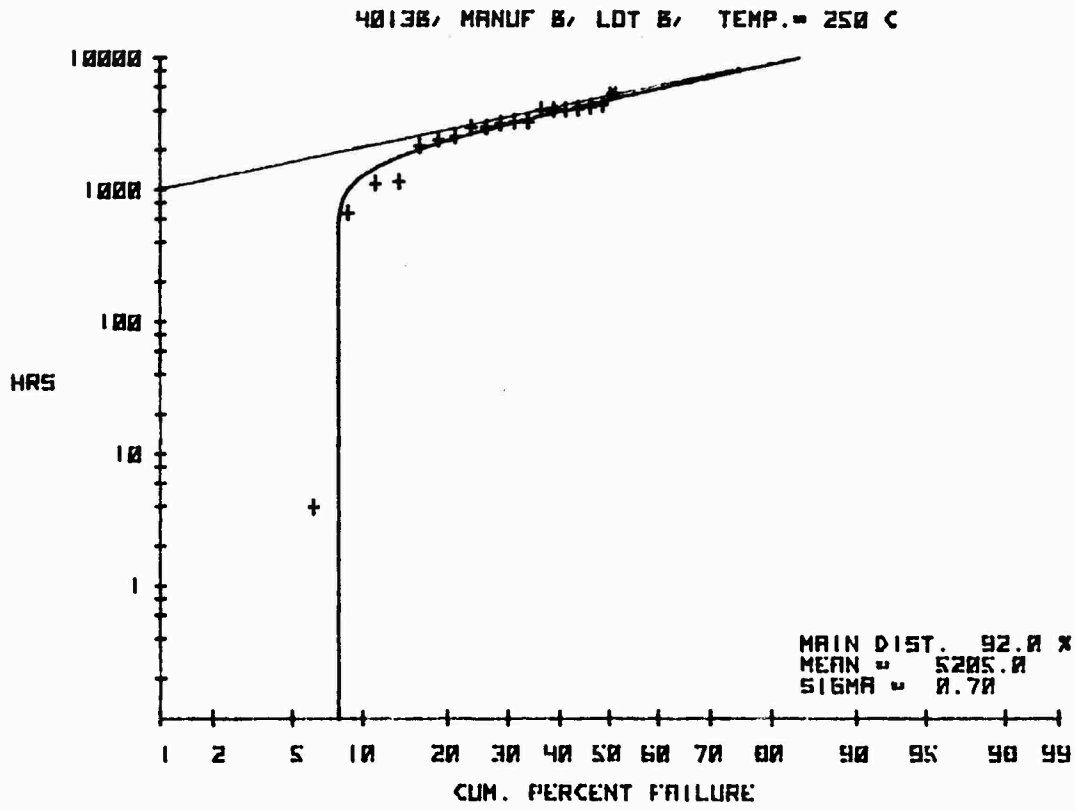


FIGURE 19. MANUFACTURER B 4013B FAILURE DISTRIBUTION - SURFACE RELATED

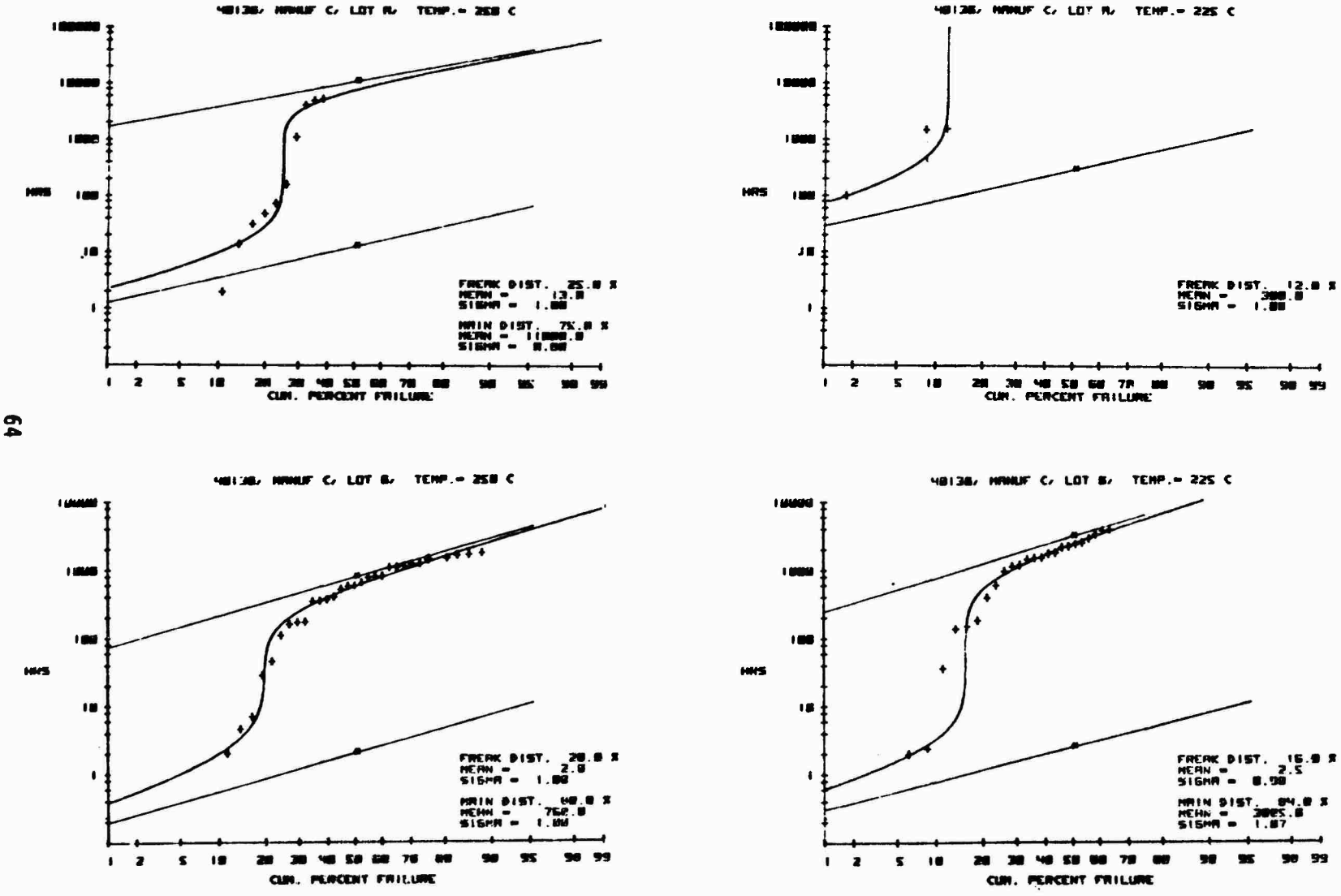


FIGURE 20. MANUFACTURER C 4013B FAILURE DISTRIBUTIONS - SURFACE RELATED

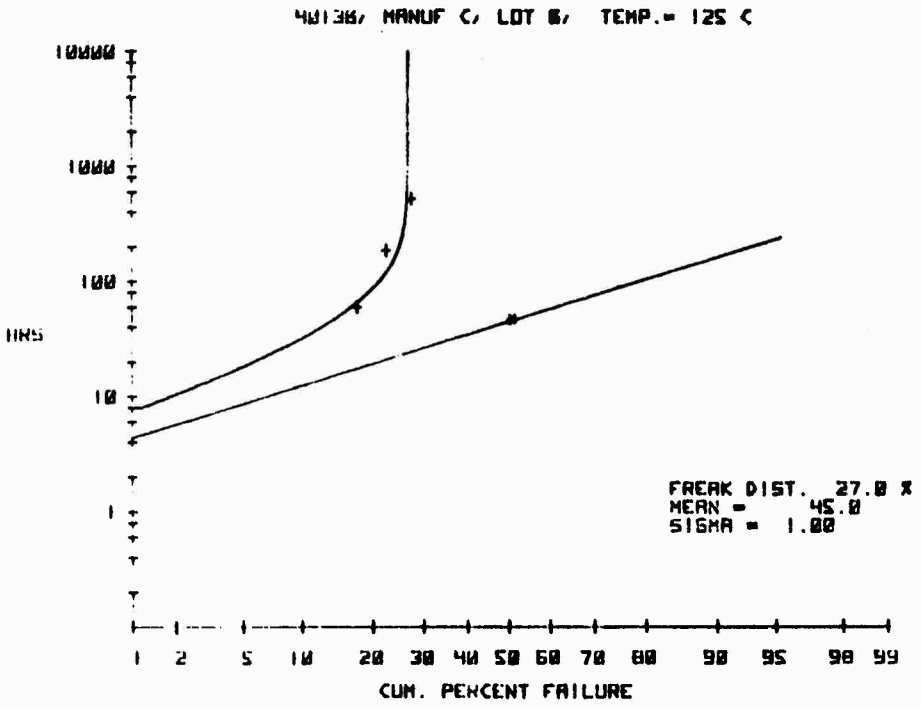


FIGURE 21. MANUFACTURER C 4013B 125°C FAILURE DISTRIBUTION - SURFACE RELATED

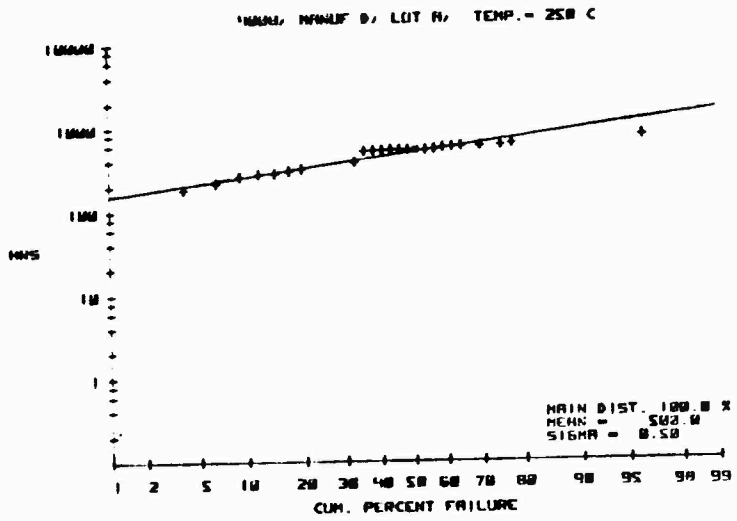
in Figure 22, indicate a bimodal distribution for the Lot B devices and the 225°C Lot A test group. The Lot A Freak population was 7% and the average Freak population for the Lot B devices was 14%.

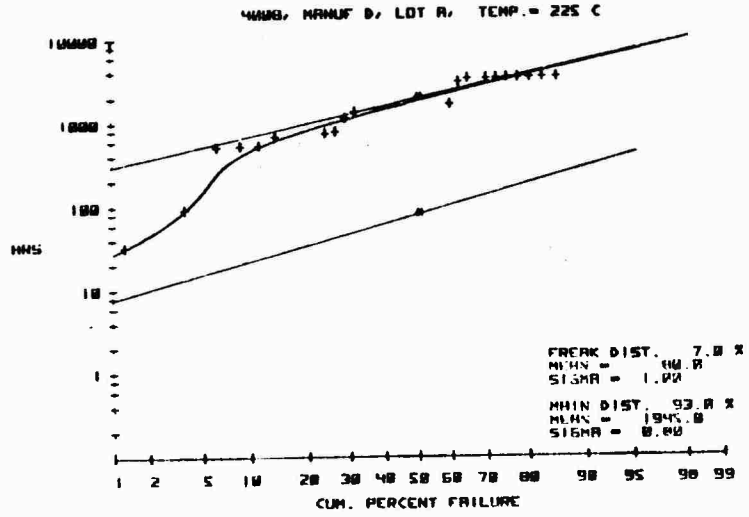
The Manufacturer C MIL-M-38510/05401 (4008) devices exhibited surface related failure mechanisms similar to the Manufacturer D 4008 devices. However, the Manufacturer C devices also exhibited 15 failures (pin-to-header shorts) which were attributed to dendrite growth. There were insufficient failures at each test temperature to determine a plot for the dendrite growth mechanism. The Lot A surface related failures were characterized by a bimodal distribution in the 225°C test group and a single lognormal distribution for the 250°C test group, as shown in Figure 23. The 125°C Lot A life test resulted in two surface related failures. The plot of these failures (Figure 24) using the same sigma as the 225°C failures suggests a bimodal distribution with approximately 8% of the devices in the Freak population. Although the 250°C test group resulted in a single lognormal distribution, failure analysis revealed no difference in the failure mechanism.

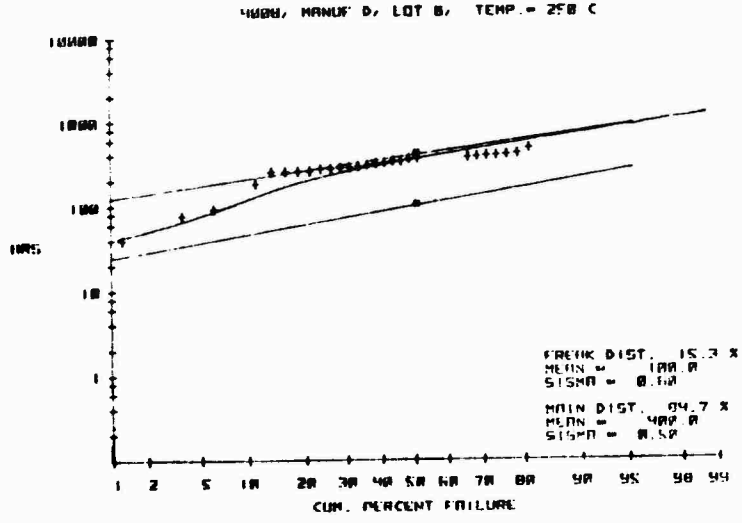
The Manufacturer C Lot B devices exhibited only a few failures, and some were attributed to dendrite growth. The surface related failures were plotted, and are shown in the previous Figure 23. The plots suggest a single lognormal distribution.

7.3.4 MIL-M-38510/05601 (4017) Failure Distributions - The Manufacturer D MIL-M-38510/05601 (4017) devices exhibited several surface related mechanisms which were caused by ionic contamination. The surface related failures exhibited a bimodal distribution for the Lot A devices and a single lognormal distribution for the Lot B devices as shown in Figure 25. There was nothing noted in the failure analysis that would account for this difference.

The Manufacturer A MIL-M-38510/05601 (4017) devices exhibited two surface related mechanisms, a channeled output transistor caused by cation drift in the gate oxide, and an undefined surface instability mechanism







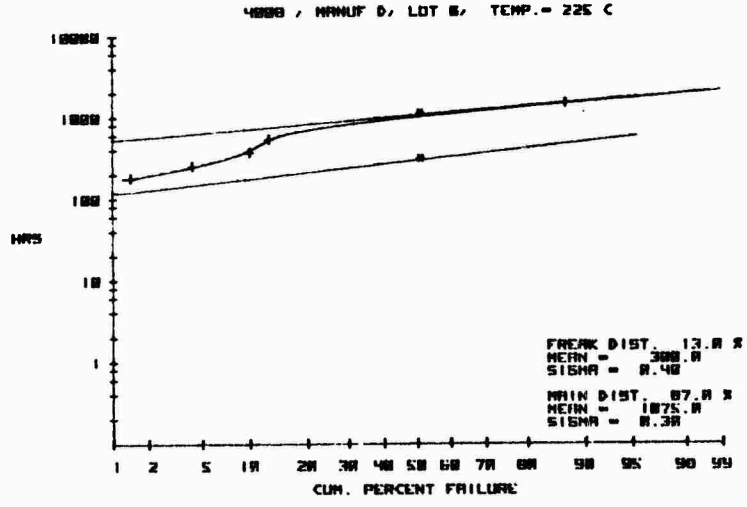


FIGURE 22. MANUFACTURER D 4008 FAILURE DISTRIBUTIONS - SURFACE RELATED

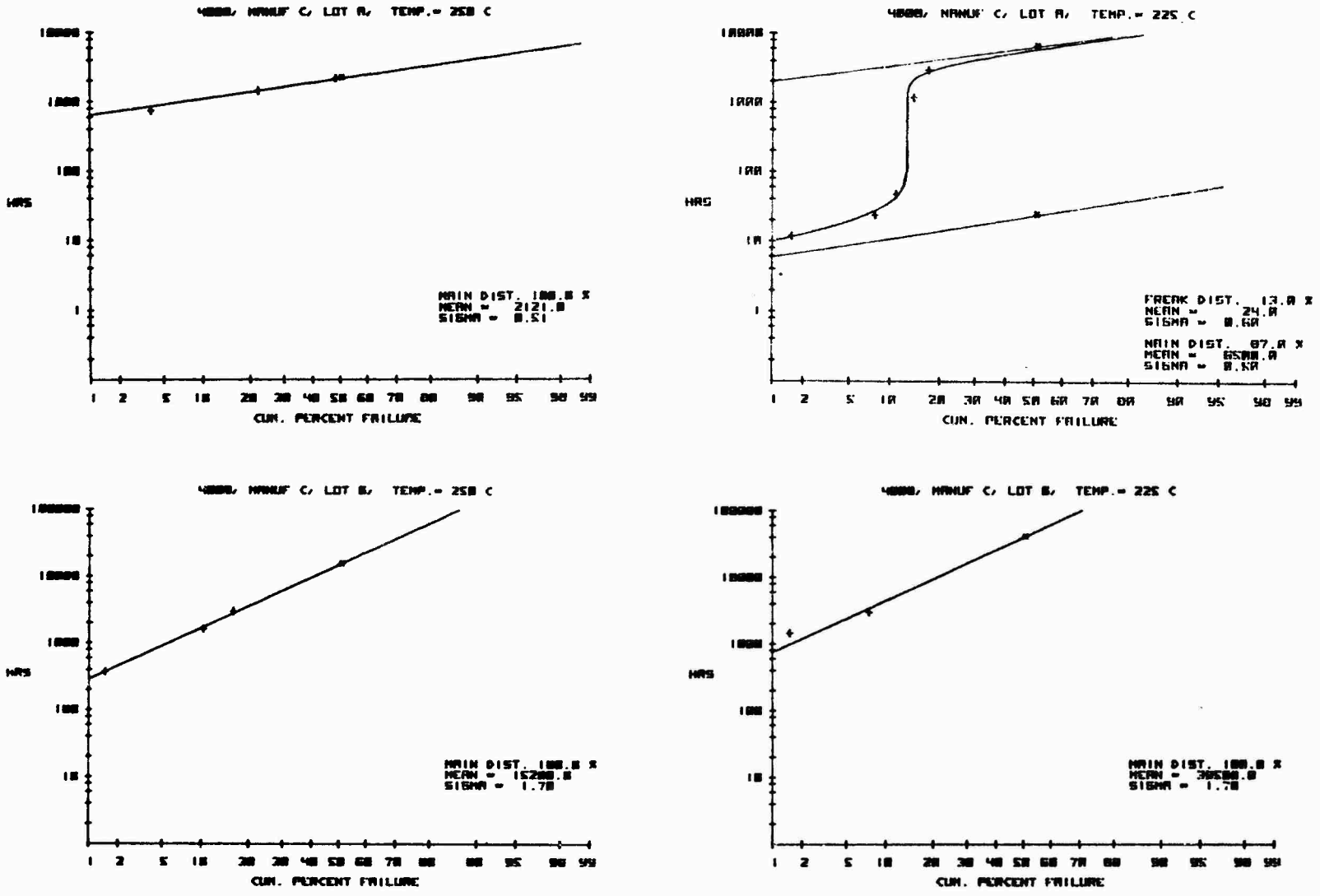


FIGURE 23. MANUFACTURER C 4008 FAILURE DISTRIBUTIONS - SURFACE RELATED

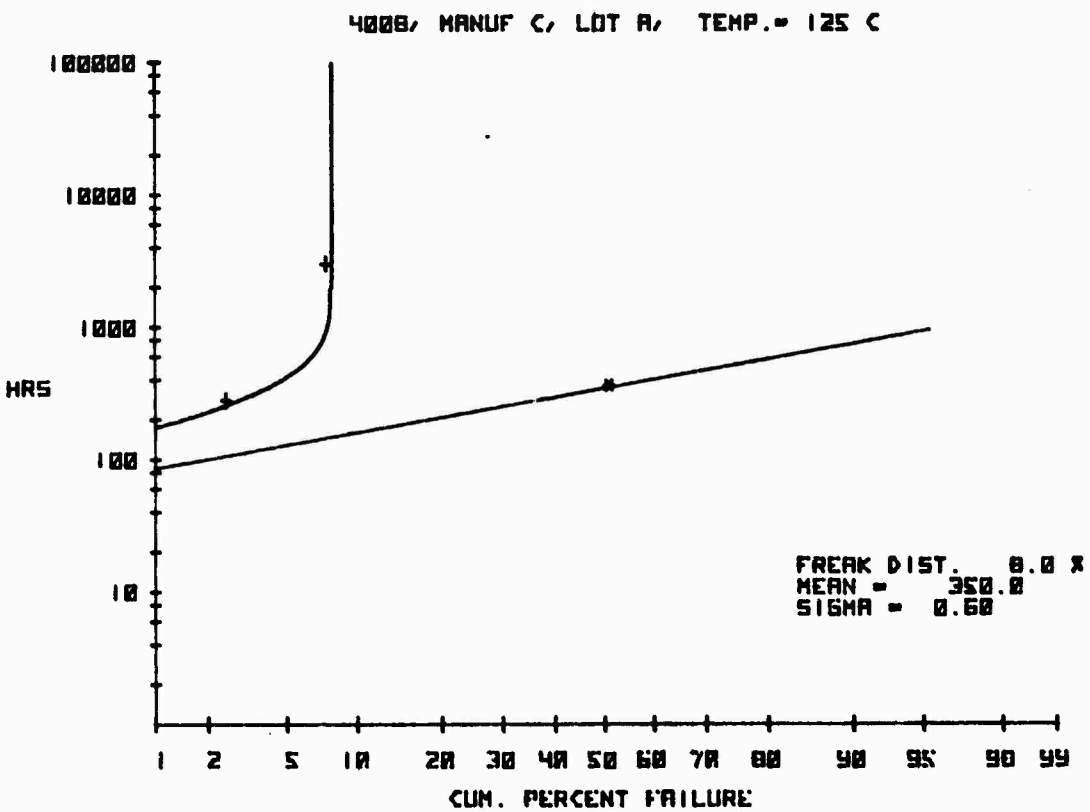


FIGURE 24. MANUFACTURER C LOT A 4008 125°C FAILURE DISTRIBUTION - SURFACE RELATED

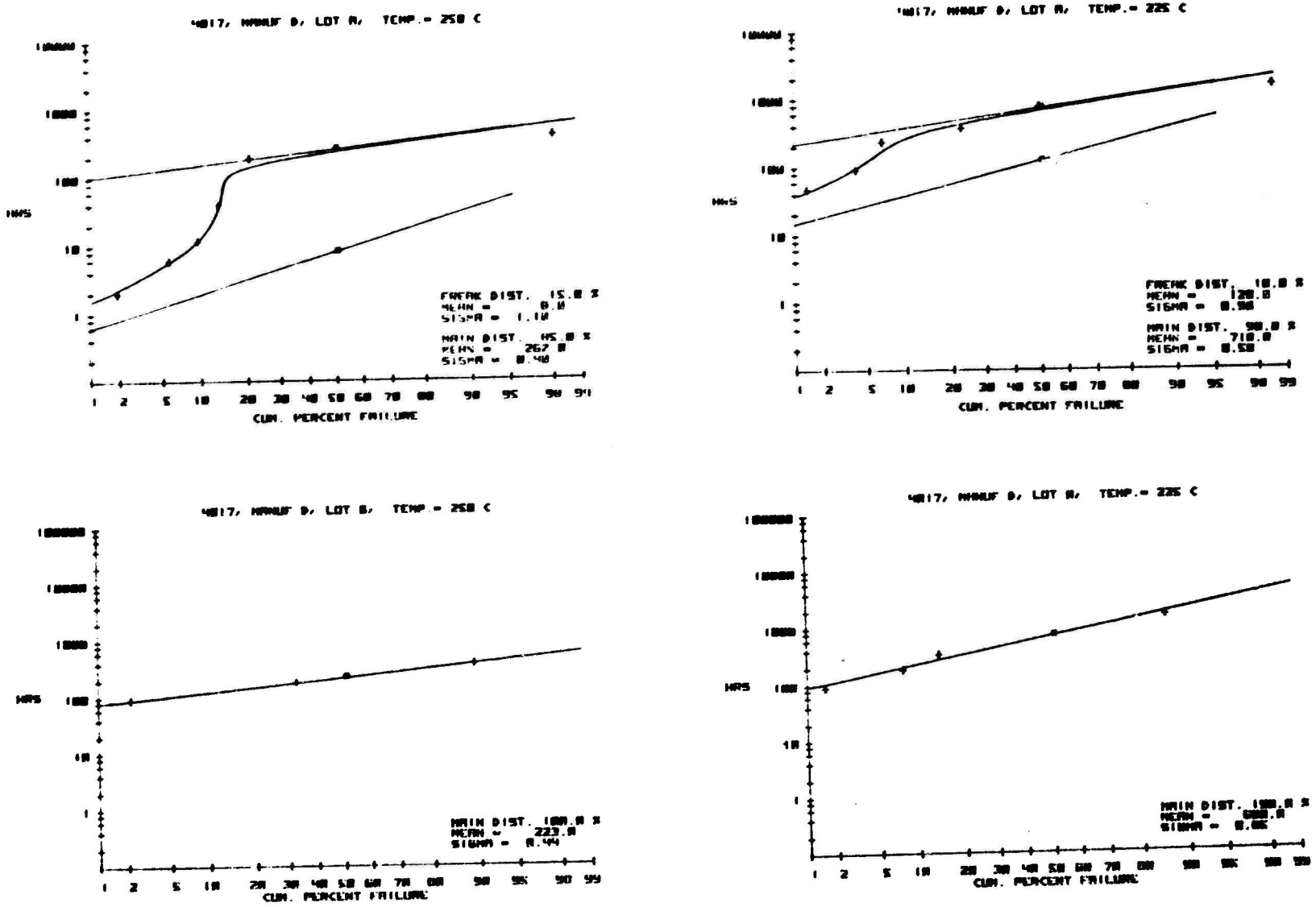


FIGURE 25. MANUFACTURER D 4017 FAILURE DISTRIBUTIONS - SURFACE RELATED

probably caused by ionic contamination. These two surface related mechanisms generated the bimodal distributions shown in Figure 26 for the Lot A devices. There was insufficient data to plot distributions for the Lot B devices.

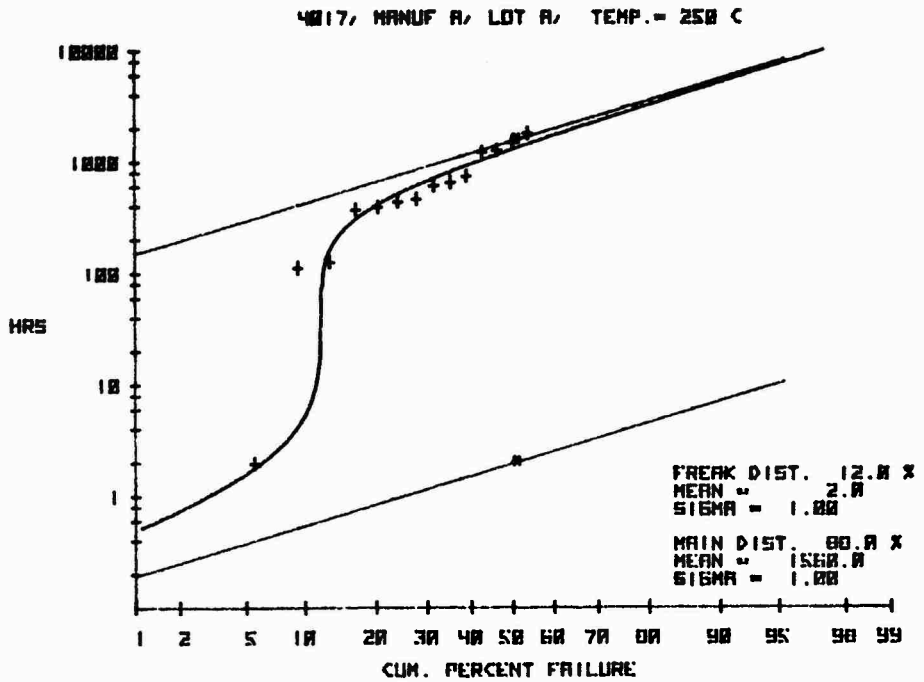
A total of 8% of Manufacturer A's Lot A and Lot B 4017 devices failed due to dendrite growth between adjacent pins caused by the reduction and precipitation of lead (Pb) contained in the glass frit. Failure distributions for this mechanism are shown in Figure 27.

The Manufacturer D 4017s exhibited a failure mechanism similar to the Manufacturer A 4017s. The failure mechanism of the Manufacture D devices was a dendrite growth caused by the migration of nickel across the surface of the ceramic and was observed in 29% of the Lot A and Lot B 250°C life test devices. There were no similar failures in the 225°C and 125°C cells of this device. This suggests this mechanism is not a problem at temperatures less than 250°C. The Lot A nickel migration failures were all observed at the 500 hour test time, and the failure distribution could not be determined. However, the distribution for the Lot B devices was determined, and is shown in the previously mentioned Figure 27.

7.4 AGING CHARACTERISTICS

Sufficient multiple temperature data was generated during the accelerated life tests to evaluate aging characteristics for most lots of each device type. The Arrhenius reaction rate model [4] was found to provide a good representation of the aging characteristics for both the Freak and Main device distributions, and the single lognormal distributions, and was used to relate median lifetime and junction temperatures as follows:

$$t_{50\%} = A \exp\left[\frac{E_A}{k T}\right] \qquad (2)$$



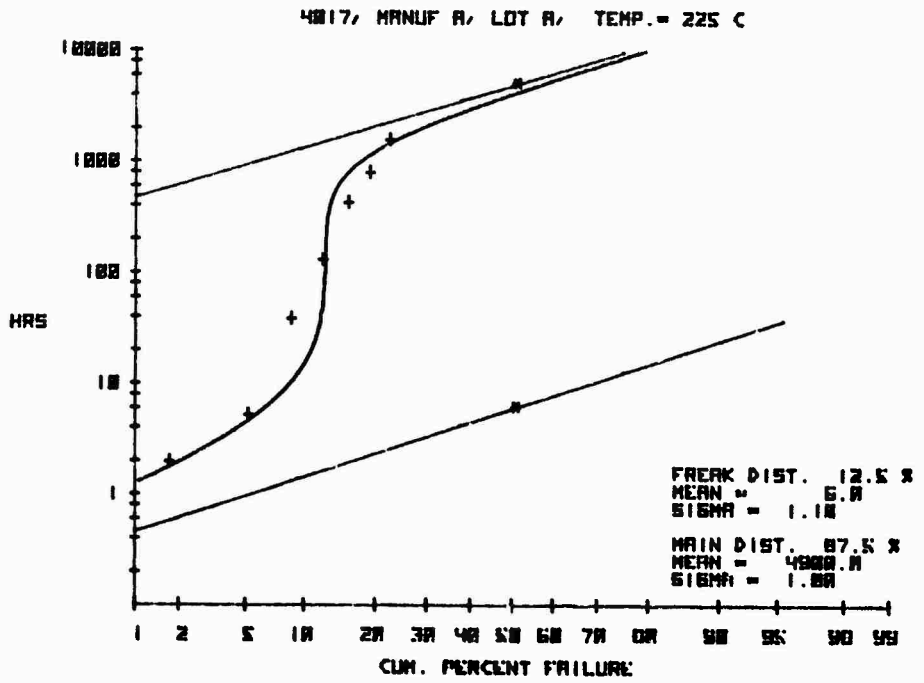


FIGURE 26. MANUFACTURER A 4017 FAILURE DISTRIBUTIONS - SURFACE RELATED

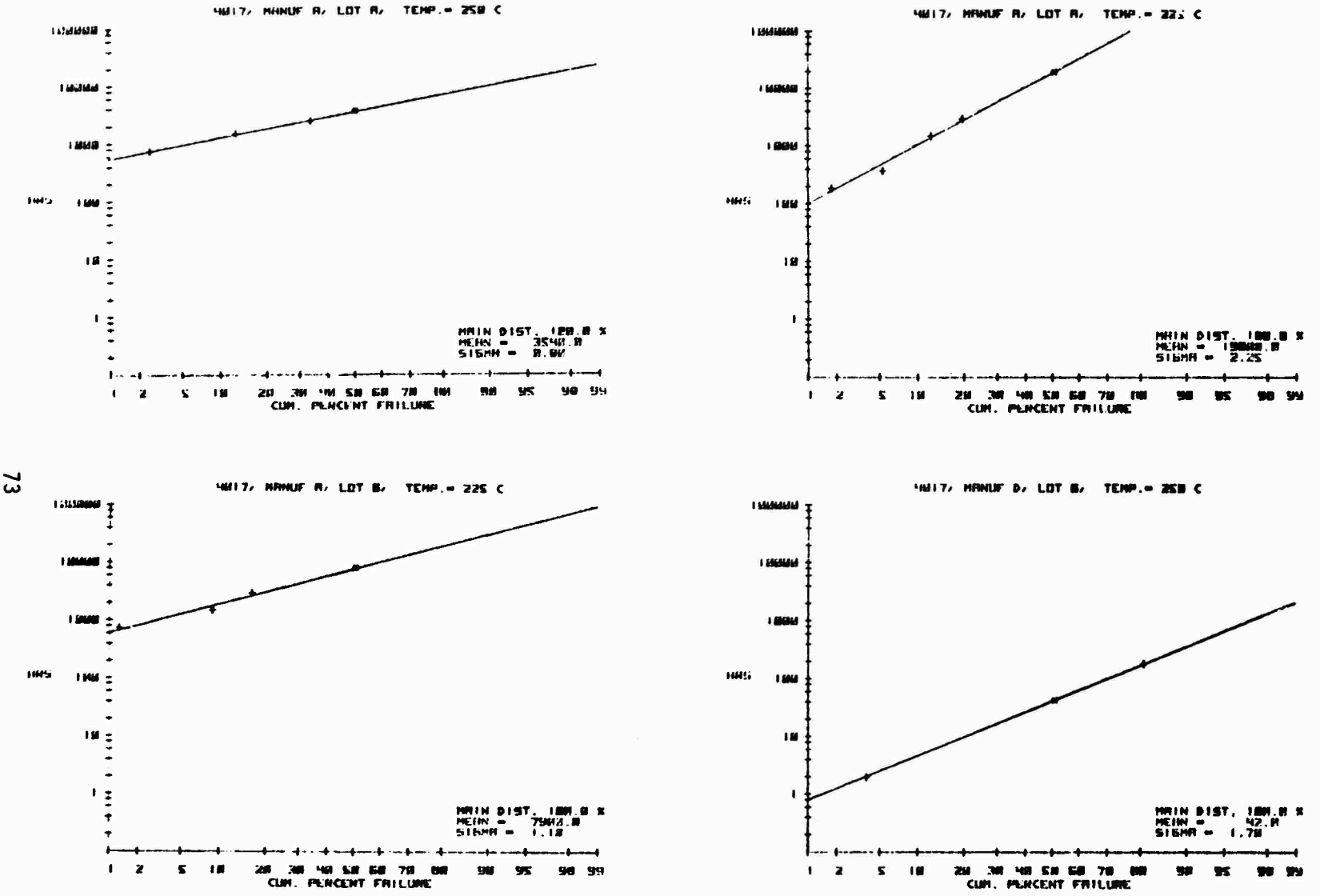


FIGURE 27. 4017 FAILURE DISTRIBUTIONS - DENDRITE GROWTH

where

$t_{50\%}$ = Freak or Main population median lifetime at a junction temperature.

A = A constant.

E_A = Experimental activation energy - eV.

k = Boltzman's constant - 8.617 x 10^{-5} eV/Kelvin.

T = Absolute junction temperature K - Kelvin.

The linear transform of this equation is:

$$\ln t_{50\%} = \ln A + \frac{E_A}{k}\left[\frac{1}{T}\right] \qquad (3)$$

The transformed Arrhenius equation was evaluated using a linear regression analysis that assumes the junction temperature is a known value and natural log of the median life [ln ($t_{50\%}$)] is the only variable [7], [8].

7.4.1 4001 Arrhenius Plots

Arrhenius plots were generated for both manufacturers' 4001 devices. The Arrhenius plots for Manufacturer A's Lot A devices exhibited a bimodal distribution but there was only sufficient data to fully characterize the Freak population. The activation energy for the Lot A Freak population was 1.94 eV. The Lot B devices exhibited a single lognormal distribution with an activation energy of 1.42 eV. The similarity in activation energies between lots suggest similiar failure mechanisms for both lots as was indicated by the failure analysis.

Manufacturer B's Lot A devices exhibited a bimodal failure distribution. However, there was insufficient data to determine an Arrhenius plot for the main population of the Lot B devices. The Freak activation energy for Lot A was 0.94 eV, and the Main activation energy was 0.77 eV. The Lot B Freak activation energy was 0.43 eV. This would seem to indicate different

failure mechanisms but this was not confirmed by the failure analysis findings. The Arrhenuis plot for the Lot B devices is based on only a few failures at each test temperature, and the actual activation energy might possibly be higher. The Arrhenius plots for both manufacturers are shown in Figure 28.

7.4.2 4013B Arrhenius Plots - The Manufacturer B 4013 devices did not exhibit sufficient failures to generate Arrhenius plots. The Manufacturer C devices exhibited bimodal distributions for both lots, and the Arrhenius plots for these lots are shown in Figure 29. However, there were insufficient failures in the Lot A 225°C test cell to determine the Main median life, thus the Lot A Arrhenius plot only contains a plot for the Freak population. The Lot A Freak activation energy is 2.82 eV. This is considered to be high, but since the distribution is based only on a small number of failures at each test temperature, the actual activation energy may be smaller. The activation energy for the Lot B devices is 0.46 eV for the Freak population and 1.24 eV for the Main population. The failure analysis discovered several surface related mechanisms, but they could not be correlated to the difference in activation energies.

7.4.3 4008 Arrhenius Plots - Arrhenius plots for both manufacturers 4008s are shown in Figure 30. Although the failures in both lots of Manufacturer C's Lot B 4008 devices were attributed to the same failure mechanism, the Lot A devices exhibited a bimodal distribution with an activation energy of 0.46 eV for the Freak population and 1.01 eV for the Main population. The Lot B devices exhibited a single lognormal distribution with an activation energy of 0.86 eV. Only a small percentage of failures were experienced in the life tests. Thus, the variation in activation energies is probably due to experimental errors.

The Manufacturer D Lot A devices exhibited a single lognormal distribution with an activation energy of 1.22 eV. The Lot B devices exhibited a bimodal distribution with similar activation energies of 0.99 eV for the Freak population and 0.89 eV for the Main population.

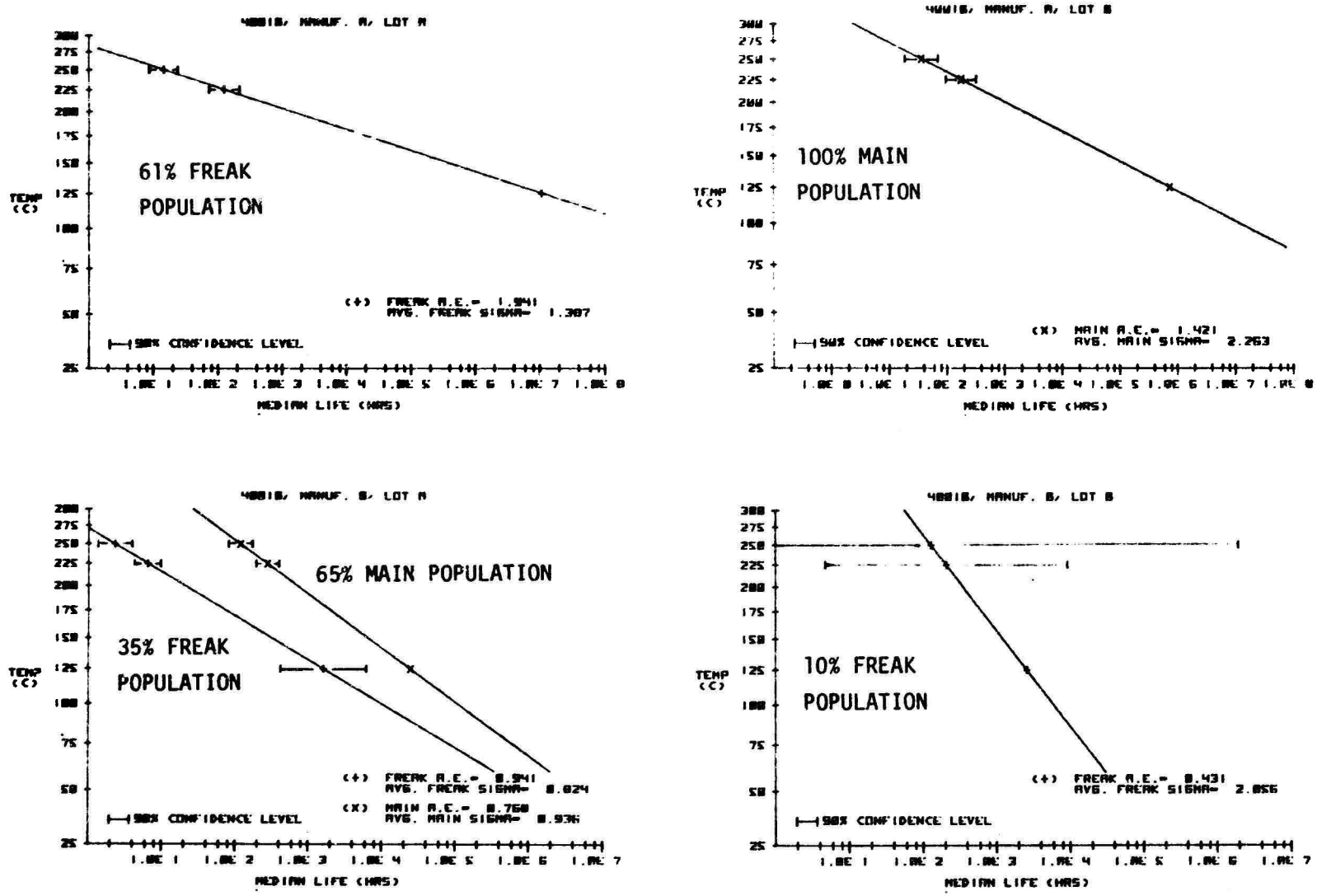
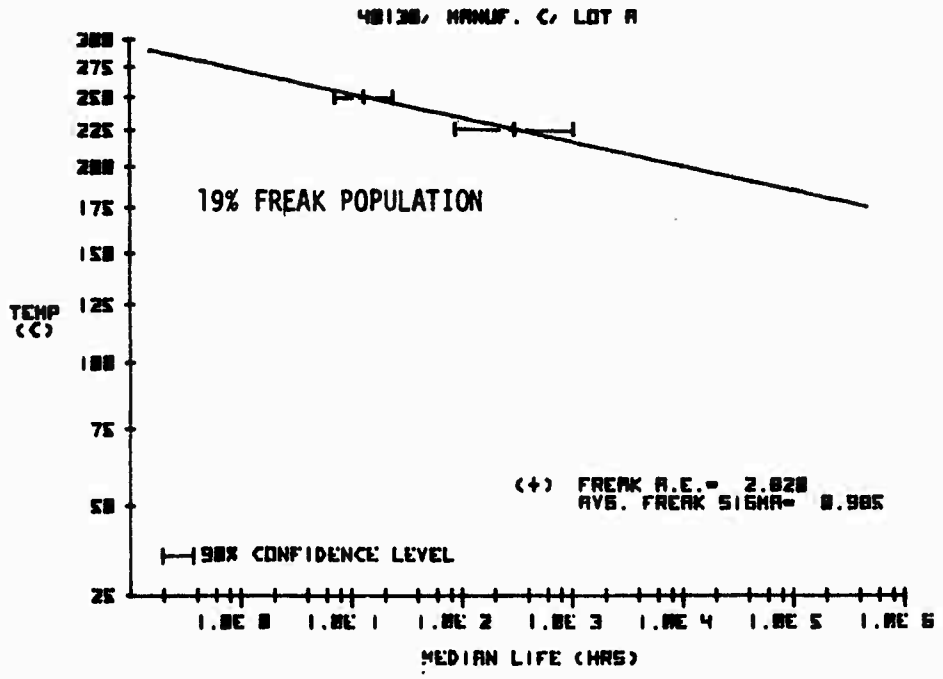


FIGURE 28. 4001B ARRHENIUS PLOTS - SURFACE RELATED



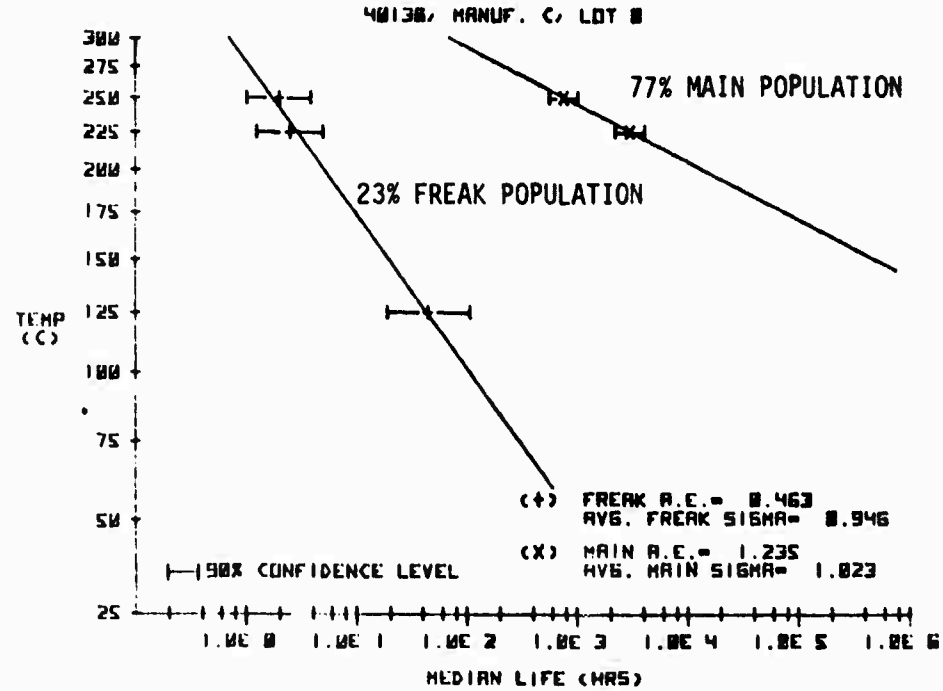


FIGURE 29. MANUFACTURER C 4013B ARRHENIUS PLOT - SURFACE RELATED

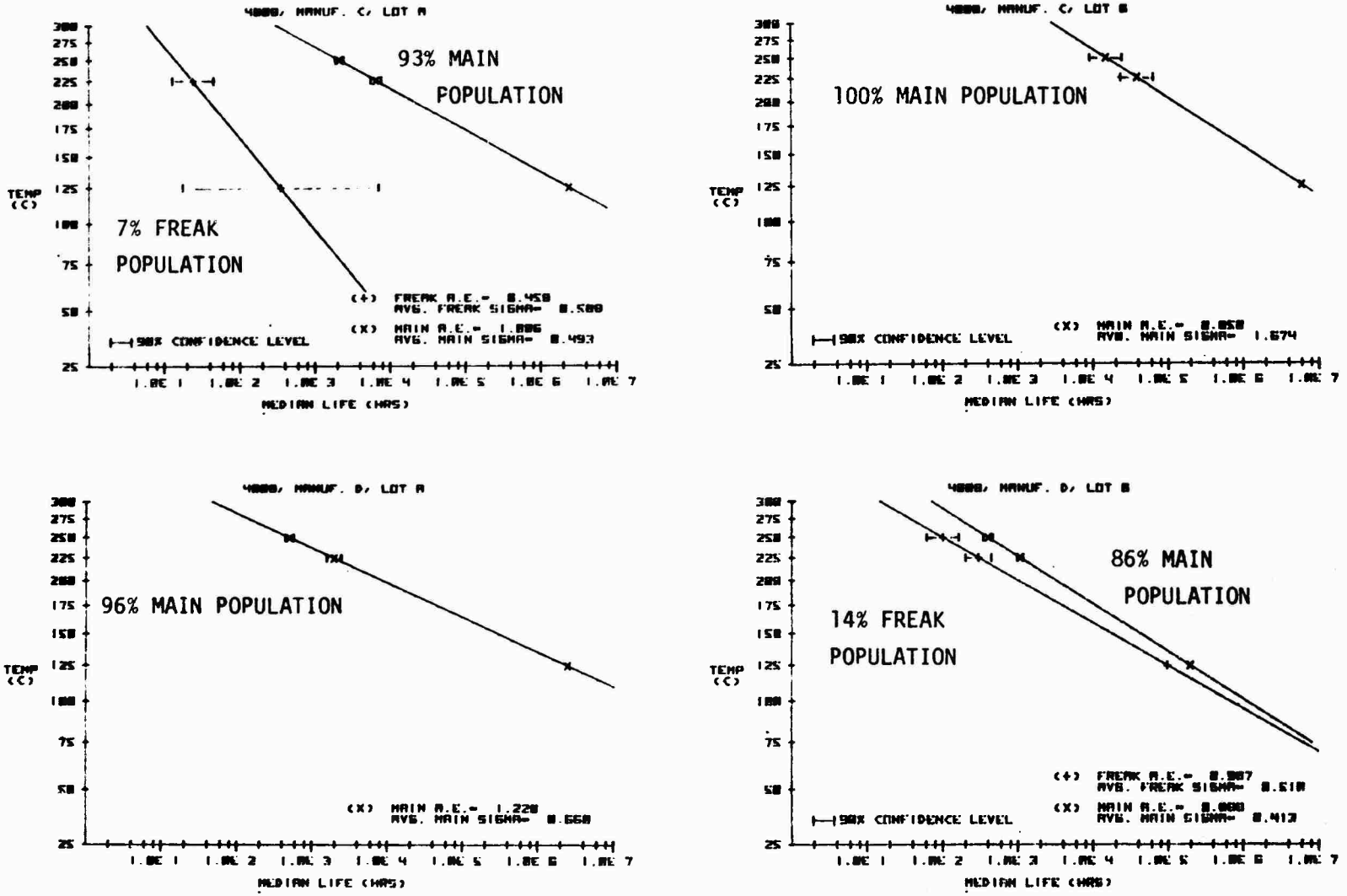


FIGURE 30. 4008 ARRHENIUS PLOTS - SURFACE RELATED

7.4.4 4017 Arrhenius Plots - The Arrhenius plots for both manufacturers 4017s are shown in Figure 31. The Manufacturer A 4017 devices exhibited a bimodal distribution for the Lot A devices, but there was insufficient data to generate plots for the Lot B devices. The Freak and Main Lot A populations exhibited similar activation energies, 0.99 eV and 1.03 eV, respectively, indicating similar failure mechanisms for both populations.

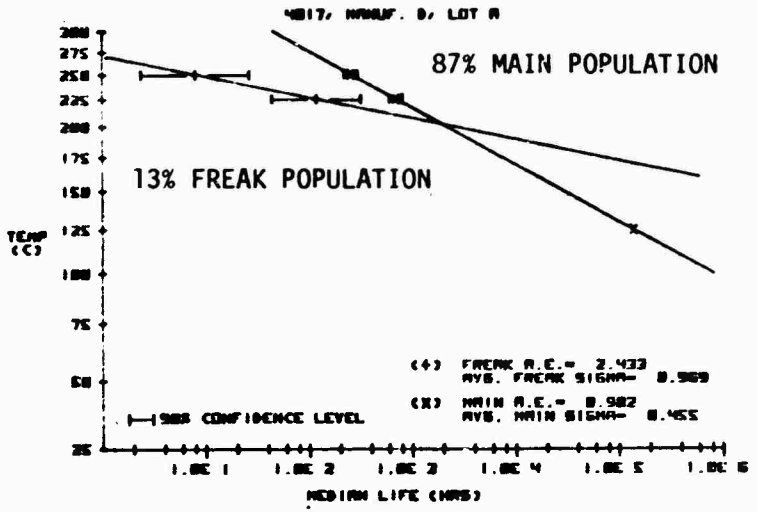
The Manufacturer D devices exhibited a bimodal distribution for Lot A and a single lognormal distribution for Lot B. The 0.90 eV activation energy for the Lot A Main population is similar to the 1.02 eV activation energy for the Lot B single distribution. However, the Lot A Freak population had an activation energy of 2.43 eV. This is dissimilar to the Main activation energy, but the failure analysis did not indicate any difference in failure mechanisms.

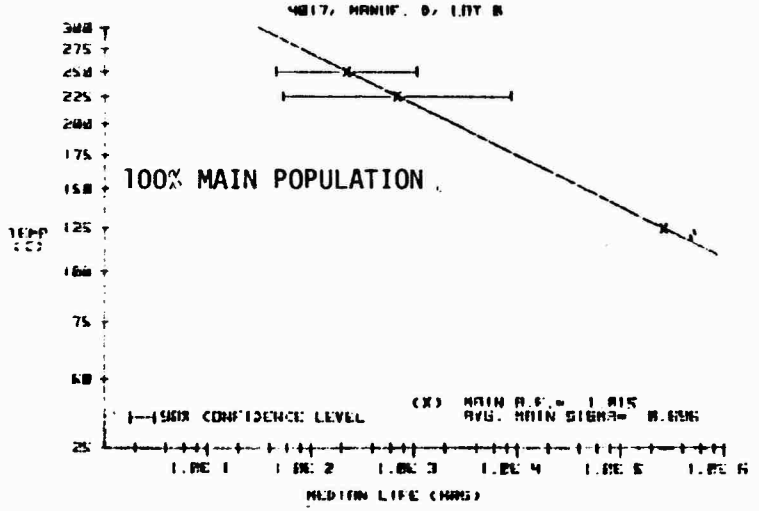
The Manufacturer A Lot A 4017 devices also exhibited sufficient failures due to a dendrite growth mechanism to generate the Arrhenius plot shown in Figure 32.

7.5 FAILURE RATES

Calculation of use-temperature failure rates was made using the values shown in Table 27 for Arrhenius model parameters (constant "A" and activation energy "E_A"), average value of lognormal distribution standard deviation, and percent Freak and Main population. The failure rate for a single distribution is defined as [9]:

$$\lambda(t) = \frac{f(t)}{R(t)} \qquad (4)$$





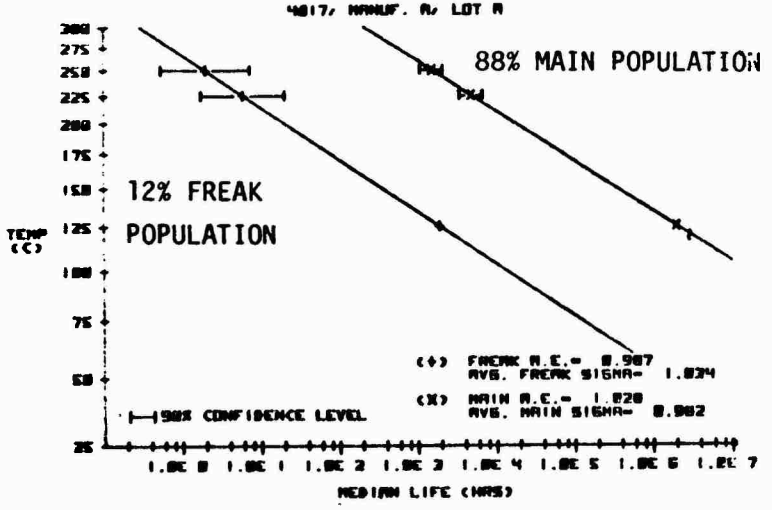


FIGURE 31. 4017 ARRHENIUS PLOTS - SURFACE RELATED

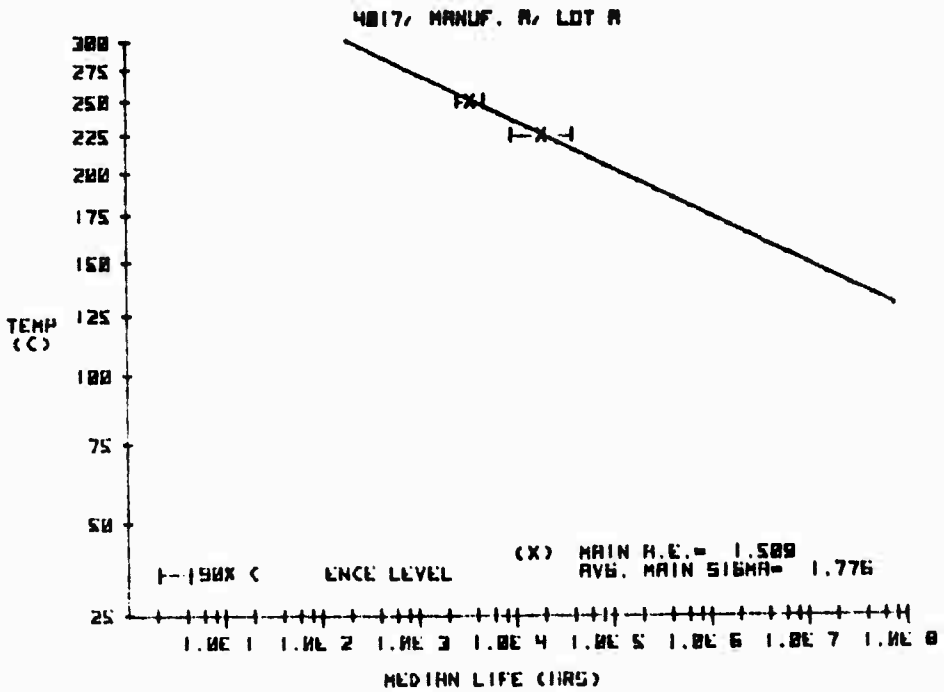


FIGURE 32. MANUFACTURER A 40° ARRHENIUS PLOT - DENDRITE GROWTH

TABLE 27. SUMMARY OF FAILURE RATE PARAMETERS

						FREAK			MAIN		
DEVICE TYPE	MFR	LOT	FAILURE MECHANISM	AVG % FREAK	AVG % MAIN	E_A (eV)	A	σ AVG	E_A (eV)	A	σ AVG
4001B	A	A	CATION DRIFT	61	39	1.94	2.86×10^{-18}	1.39	⚠1	-	-
		B		0	100	-	-	-	1.42	7.54×10^{-13}	2.26
	B	A		35	65	0.94	1.95×10^{-9}	0.82	0.77	4.71×10^{-6}	0.94
		B		10	90	0.43	9.20×10^{-3}	2.06	⚠1	-	-
4013B	C	A	CATION DRIFT	19	81	2.82	8.94×10^{-27}	0.98	⚠1	-	-
		B		23	77	0.46	6.12×10^{-5}	0.95	1.23	9.65×10^{-10}	1.02
4008	C	A	SURFACE INSTABILITY	7	93	0.46	5.58×10^{-4}	0.59	1.01	4.32×10^{-7}	0.49
		B		0	100	-	-	-	0.86	8.27×10^{-5}	1.67
	D	A		4	96	⚠1	-	-	1.22	8.78×10^{-10}	0.66
		B		14	86	0.99	3.11×10^{-8}	0.51	0.89	1.11×10^{-6}	0.41
4017	A	A	SURFACE INSTABILITY	12	88	0.99	6.22×10^{-10}	1.03	1.03	1.94×10^{-7}	0.98
	D	A	CHARGE SEPARATION	13	87	2.43	2.94×10^{-23}	0.97	0.90	5.27×10^{-7}	0.46
		B	SURFACE INSTABILITY	0	100	-	-	-	1.01	3.75×10^{-8}	0.70

⚠1 INSUFFICIENT DATA TO CALCULATE ACTIVATION ENERGY

where:

$\lambda(t)$ = the instantaneous failure rate at time t.

$f(t)$ = the failure density at time t.

$R(t)$ = the reliability at time t.

Also, a lognormal failure rate for a single distribution is defined as [10]:

$$\lambda(t) = \frac{\frac{1}{t\,\sigma\sqrt{2\pi}} \exp\left\{-\frac{(\ln t - \mu)^2}{2\sigma^2}\right\}}{\frac{1}{\sigma\sqrt{2\pi}} \int_t^\infty \frac{1}{t'} \exp\left\{-\frac{(\ln t - \mu)^2}{2\sigma^2}\right\} dt'} \qquad (5)$$

where:

μ = ln (median life)

σ = the standard deviation

Assuming that an Arrhenius equation defines the median life at a junction temperature provides the following temperature dependent, lognormal failure rate:

$$\lambda(t) = \frac{\frac{1}{t\,\sigma\sqrt{2\pi}} \exp\left\{-\frac{[\ln t - (\ln A + E_A/k\,T)]^2}{2\sigma^2}\right\}}{\frac{1}{\sigma\sqrt{2\pi}} \int_t^\infty \frac{1}{t'} \exp\left\{-\frac{[\ln t' - (\ln A + E_A/k\,T)]^2}{2\sigma^2}\right\} dt'} \qquad (6)$$

For a bimodal distribution consisting of two lognormal failure rates, the total failure rate is defined as:

$$\lambda(t)_{Total} = \left\{\lambda(t)_{Freak}\right\} (\%\ Freak) + \left\{\lambda(t)_{Main}\right\} (\%\ Main) \qquad (7)$$

These techniques were used to calculate the maximum instantaneous failure rates shown in Table 28. The maximum instantaneous failure rate over the first 10^5 hours of 125°C use-time varied from 4.16×10^{-3} failures per hour to 1.15×10^{-32} failures per hour. However, three lots (Manufacturer B Lot B 4001, Manufacturer C Lot A 4013, and Manufacturer C Lot B 4008) exhibited less than 10% failures in at least one of the high temperature (200°C or 250°C) life tests. Thus, the calculated failure rates for these lots are only best estimates and may vary from the actual failure rates. Also two of these lots, the Manufacturer C Lot A 4013 and Lot B 4008, and one additional lot, the Manufacturer A Lot A 4001, exhibited single failures in the 125°C life test which were unexpected based on the calculated failure rates. These were isolated random failures due to the same, or similar, mechanisms as the failures observed in the high temperature life tests. The random failures are due to either higher actual failure rates or to smaller distributions of Freak failures which were masked by larger distributions of similar mechanisms at the higher temperatures.

Using the calculated failure rates as a basis, the following recommendations on burn-in are made for each individual lot. Where there is a single lognormal distribution, as for the Manufacturer A Lot B 4001 devices, the Manufacturer C Lot B 4008 devices, and Manufacturer D Lot B 4017 devices, an improvement in failure rate cannot be achieved without sacrificing a high percentage of the total population. The failure rate for the Manufacturer A 4001 Lot A Main distribution could not be determined but the Freak population, which accounts for 61% of the total population, has an acceptable failure rate, and thus a burn-in for 1445 hours at 275°C is not recommended. The Manufacturer D 4008 Lot A devices exhibited an acceptable failure rate, with less than 4% of the devices in the Freak population. The failure rate however, does not include the effect of the Freak population since the data was insufficient to determine a failure rate for the Freak population.

TABLE 28. FAILURE RATE SUMMARY

DEVICE TYPE	MFR	LOT	MAXIMUM INSTANTANEOUS FAILURE RATE IN 10^5 HOURS OF USE TIME (FAILURE/HOUR)				BURN-IN CONDITIONS		BURN-IN RECOMMENDED
			WITHOUT BURN-IN		WITH BURN-IN				
			125°C	50°C	125°C	50°C	TIME (HkS)	Tj (°C)	
4001B	A	A	6.16×10^{-9}	4.09×10^{-42}	(1)	-	1445	275	NO
		B	3.12×10^{-5}	3.30×10^{-12}	(2)	-	-	-	NO
	B	A	2.33×10^{-4}	4.32×10^{-8}	3.25×10^{-5}	1.26×10^{-9}	90	250	YES
		B	5.67×10^{-5}	3.08×10^{-6}	(1)	-	(3)	-	NO
4013B	C	A	1.15×10^{-32}	0	(1)	-	442	275	NO
		B	4.16×10^{-3}	1.82×10^{-4}	5.05×10^{-9}	1.47×10^{-35}	55	250	YES
4008	C	A	2.23×10^{-4}	1.01×10^{-5}	1.85×10^{-14}	5.93×10^{-92}	165	250	YES
		B	1.20×10^{-7}	1.09×10^{-13}	(2)	-	-	-	NO
	D	A	4.57×10^{-11}	2.30×10^{-71}	(1)	-	-	-	NO
		B	4.69×10^{-6}	1.67×10^{-43}	2.77×10^{-6}	3.24×10^{-63}	1774	250	NO
4017	A	A	4.81×10^{-5}	1.39×10^{-8}	3.76×10^{-8}	1.60×10^{-28}	178	250	YES
	D	A	7.59×10^{-6}	2.30×10^{-48}	8.72×10^{-6}	2.64×10^{-48}	3094	250	NO
		B	2.42×10^{-6}	4.25×10^{-33}	(2)	-	-	-	NO

(1) INSUFFICIENT DATA TO DETERMINE FAILURE RATE.
(2) SINGLE LOGNORMAL DISTRIBUTION, BURN-IN NOT RECOMMENDED.
(3) BURN-IN IN EXCESS OF 1.29×10^5 HOURS REQUIRED.

Burn-in is also not recommended for Manufacturer D's 4008 Lot B and 4017 Lot A devices. Burn-in at 250°C for 1774 hours for the Manufacturer D 4008 Lot B devices would only slightly improve the failure rate and would result in 80% of the Main population being removed. The failure rate for the Manufacturer D 4017 Lot A devices would actually increase slightly due to the fact that the median lifetime of the Main population is less than that of the Freak population at temperatures less than 200°C. Burn-in for the Manufacturer B 4001 Lot B devices, which exhibited only a few failures, would require in excess of 100,000 hours at 250°C which is impractical. The Manufacturer C Lot A 4013 devices also exhibited only a few failures, but if the actual failure rate even approximates the calculated 1×10^{-32} failures per hour, burn-in would not be needed.

Burn-in is recommended for the Manufacturer C Lot A 4008 devices, the Manufacturer C Lot B 4013 devices and the Manufacturer A Lot A 4017 devices, since burn-in would result in a large improvement in failure rate with virtually none of the Main population being removed. The Manufacturer B Lot A 4001 device would result in an improvement in the failure rate of one order of magnitude. However the Main population would be reduced by 11% and since the Freak population accounts for 35% of the total population this would result in the total population being reduced by 42%.

The effectiveness of a burn-in appears to vary from lot to lot and device type to device type. However, the use of a 100% burn-in would have little effect on the acceptable lots, and would eliminate the high failure rate devices, thus improving the overall reliability.

Comparison of the 125°C and 50°C failure rates illustrate the value of junction temperature derating to achieve improved failure rates for the predominant failure mechanisms. Additional factors for secondary failure modes must be included in the total device failure rates prior to using the failure rates for reliability estimates.

7.6 LOT ACCEPTANCE TEST CORRELATION

The results of the 250°C life tests at the 120 and 250 hour points were evaluated to the MIL-STD-883, Method 5005.5 Lot Acceptance test criteria, and compared to the calculated failure rates to determine the effectiveness of the Lot Acceptance test. A particular lot fails the Lot Acceptance test criteria if 20 percent of the devices fail at the 120 hour electrical test point, or 40 percent of the devices fail at the 250 hour electrical test point. A maximum instantaneous failure rate of less than 1×10^{-5} failures per hour during 10^5 hours of 125°C use-time was assumed to constitute an acceptable lot, and test effectiveness (TE) was defined as:

$$TE = 100\ (N_{G/A} + N_{B/R})/N_T \qquad (8)$$

where:

$N_{G/A}$ = number of "good" lots accepted
$N_{B/R}$ = number of "bad" lots rejected
N_T = total number of lots tested

Thus, a test that is 100% effective will accept only "good" lots and reject all "bad" lots. Based on the thirteen lots of devices where sufficient data was collected to calculate 125°C failure rates (Table 29), the Lot Acceptance test accepted only three of seven "good" lots and rejected only four of six "bad" lots. Thus a correct decision was only made for seven of the thirteen lots, or the test was 54% effective. The failure rates for two of the lots are based on less than ten percent total failures, and may be inaccurate. However, excluding these two lots from the test effectiveness calculation only increases the test effectiveness to sixty percent.

TABLE 29. LOT ACCEPTANCE TEST COMPARISON

DEVICE	MFR	LOT	LOT ACCEPTANCE TEST RESULTS	125°C FAILURE RATE (FAILURES/HOUR)
4001	A	A	FAIL	6.16×10^{-9}
		B	FAIL	3.12×10^{-5}
	B	A	FAIL	2.33×10^{-4}
		B	PASS	5.67×10^{-5} (2)
4013	C	A	FAIL	1.15×10^{-32} (2)
		B	FAIL	4.16×10^{-3}
	B	A	PASS	(1)
		B	PASS	(1)
4008	C	A	PASS	2.23×10^{-4}
		B	PASS	1.20×10^{-7} (2)
	D	A	PASS	4.57×10^{-11}
		B	PASS	4.69×10^{-6}
4017	A	A	FAIL	4.81×10^{-5}
		B	PASS	(1)
	D	A	FAIL	7.59×10^{-6}
		B	FAIL	2.42×10^{-6}

(1) INSUFFICIENT DATA TO DETERMINE FAILURE RATE

(2) FAILURE RATES BASED ON LESS THAN 10% OF THE TEST GROUP FAILING.

8.0 CONCLUSIONS AND RECOMMENDATIONS

The results of this program indicate that high reliability CMOS devices that would be acceptable for MIL-M-38510 Class S applications can be manufactured, but there is a lack of consistency in lot to lot processing. The principal failure mechanisms were surface related and were responsible for 74% of the failed devices in this study. These mechanisms were responsible for several different failure modes and in some cases several different categories of failures in a single device.

The matrix of high temperature accelerated life tests showed a wide variance in aging characteristics between microcircuit types and even between different lots of the same manufacturer. The failure distributions were either single lognormal or bimodal distributions. The failure rates were generally less than 5×10^{-4} failures per hour at a use-temperature of 125°C over the first ten years. Burn-in requirements vary and, in some cases, would not be effective in improving the failure rates without sacrificing a high percentage of the total population. The MIL-STD-883 125°C life tests exhibited the same failure mechanisms but did not, in most cases, generate sufficient failures to determine a failure distribution.

The Class S Lot Acceptance test as specified in MIL-STD-883, Method 5005.5 is approximately 50% effective as a method of screening for device and lot reliability. To minimize the possibility of rejecting "good" lots or accepting "bad" lots, a two temperature Lot Acceptance test is recommended. A two temperature Lot Acceptance test at temperatures above 200°C would permit control of the lot activation energy as well as the pre-exponential factor in the Arrhenius equation. A 100% burn-in is also recommended. Although burn-in would not improve all lots, it would improve the reliability of those lots which have a Freak population with a high failure rate. The burn-in conditions should be determined from the results of life characterization studies to maximize the effectiveness of the burn-in.

The elimination or reduction of surface related failure mechanisms in CMOS devices would also greatly improve the reliability of the devices. Improved manufacturing process controls are necessary to reduce the contamination responsible for the observed surface related mechanisms. The elimination, or reduction, of surface related mechanisms, combined with a two temperature Lot Acceptance test and 100% burn-in will assure that the failure rates of CMOS device will be maintained at a level that will make the devices acceptable for Class S applications.

9.0 REFERENCES

[1] G. M. Johnson, "Voltage Stress Effects on Microcircuit Accelerated Life Test Failure Rates", Final Technical Report, NASA Contract NAS8-31177, page 6, August 1976.

[2] D. S. Peck & C. H. Zierdt, Jr., "The Reliability of Semiconductor Devices in the Bell System", Proceedings of the IEEE, Vol. 62, pp. 185-211, February 1974.

[3] D. S. Peck, "The Analysis of Data from Accelerated Stress Tests", Proceedings 9th Annual Reliability Physics Symp., pp. 68-83, 1971.

[4] F. H. Reynolds, "Thermally Accelerated Aging of Semiconductor Components", Proceedings of IEEE, Vol. 62, pp. 212-222, February 1974.

[5] P. J. Davis, "Interpolation and Approximation", Dover Publications Inc., N.Y., 1975.

[6] J. Aitchison and H. A. C. Brown, "The Lognormal Distribution", Cambridge University Press, N.Y., 1969.

[7] M. G. Natrella, "Experimental Statistics", National Bureau of Standards Handbook 91, 1963.

[8] F. S. Acton, "Analysis of Straight Line Data ", Dover Publications, Inc., N.Y., 1966.

[9] I. Bazovsky, "Reliability Theory and Practice", Prentice-Hall, Inc., Englewood Cliffs, New Jersey, 1961.

[10] L. R. Goldthwaite, "Failure Rate Study for the Log Normal Lifetime Model", IRE (NSRQCE) Conference, pp. 208-213, 1961.

APPENDIX A

MICROCIRCUIT CONSTRUCTION ANALYSIS

TABLE OF CONTENTS

APPENDIX A1

CONSTRUCTION ANALYSIS

4001B

MANUFACTURER A

QUAD 2-INPUT NOR GATE

DATE CODE 7634

MICROCIRCUIT CONSTRUCTION INFORMATION
BASELINE ANALYSIS

S/N C-125 DATE CODE 7705 DATE: 5/2/77

PART NAME: QUAD 2-INPUT NOR GATE

MANUFACTURER'S PART NO: CCL 4001/BD MANUFACTURER: A

GENERIC PART NO: 4001B PACKAGE TYPE: 14 PIN DIP

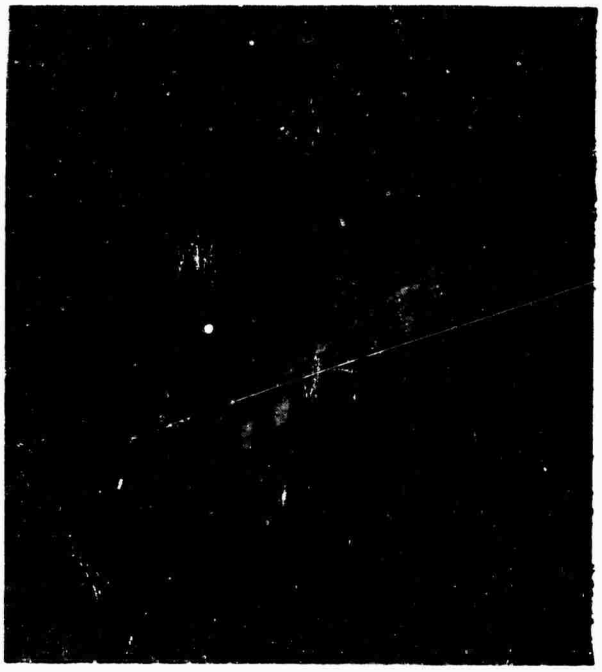
MILITARY SPECIFICATION TYPE: M38510/05202BCC

DESCRIPTION	DETAIL
DIE	
Passivation Type	Silicon Dioxide
Glassivation Type	Vapox
Basic Die Construction	Planar
Die Dimensions	0.0426 x 0.0497
Metallization Type	Aluminum
Metallization Thickness	———
Number of Metallization Layers	One
Metallization Interlayer Insulation Type	None
Bonding Pad Size	0.0054 x 0.0054
Die Photograph	(See Figure A7)
Scribe Method	Laser
INTERCONNECTIONS	
Die Mounting Material	Gold-Silicon Eutectic
Wire Material	Aluminum
Wire Diameter	0.001
Longest Lead Length	0.075
Wire Bond Type(s) Post	Ultrasonic (See Figure A4)
Die	Ultrasonic (See Figure A3)
Inte-connection Photograph	(See Figure A2)

DESCRIPTION	DETAIL
PACKAGE	
Lead/Lead Frame Material	Alloy 42
Lead/Lead Frame Finish - Internal	Aluminum
Lead/Lead Frame Finish - External	Tin Lead Plate
Lead/Lead Frame Finish - Feed Thru	None
Header/Case Material	Ceramic (Al_2O_3)
Cap/Lid Material	Ceramic (Al_2O_3)
Case Seal Material/Method	Glass Frit
Lead Seal Material/Method	Glass Frit
Cavity Size	0.165 X 0.261
Package Photograph	(See Figure A1)

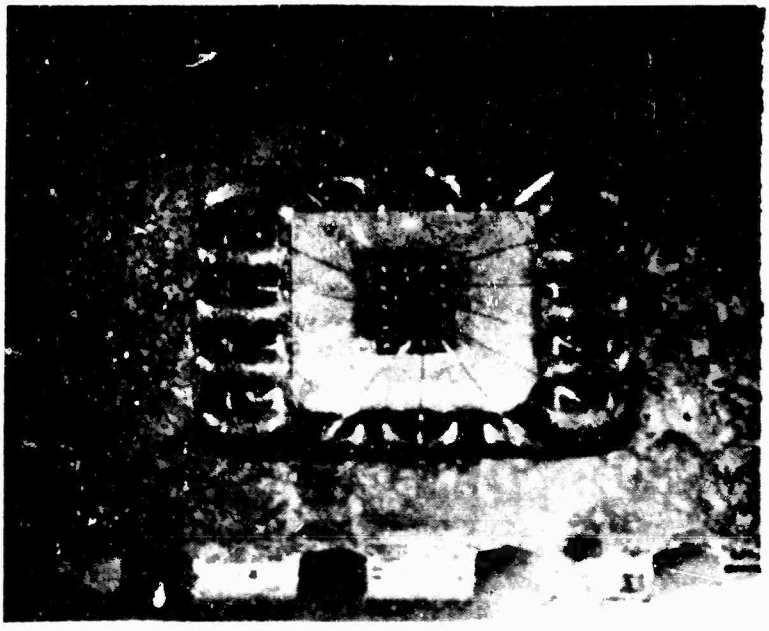
Notes:

1. Additional markings (bottom) - MALAYSIA BFBX.
2. All dimensions are in inches.



3X S/N A11

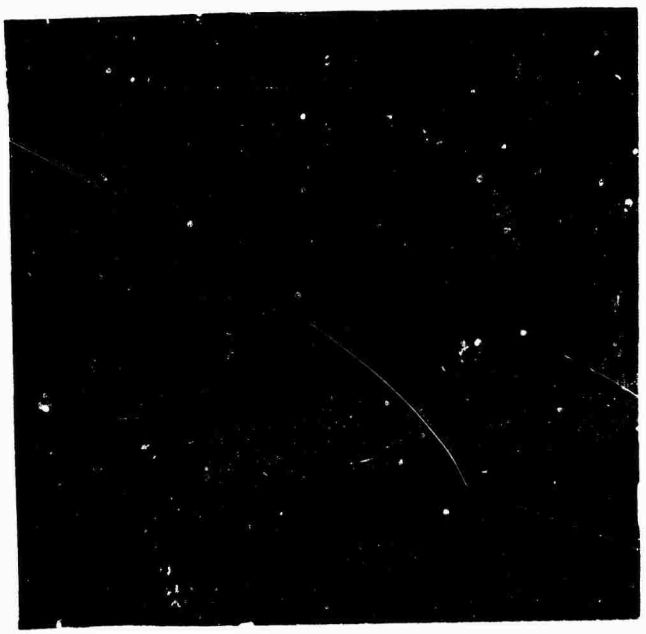
FIGURE A1 - PACKAGE PHOTO



10X S/N A11

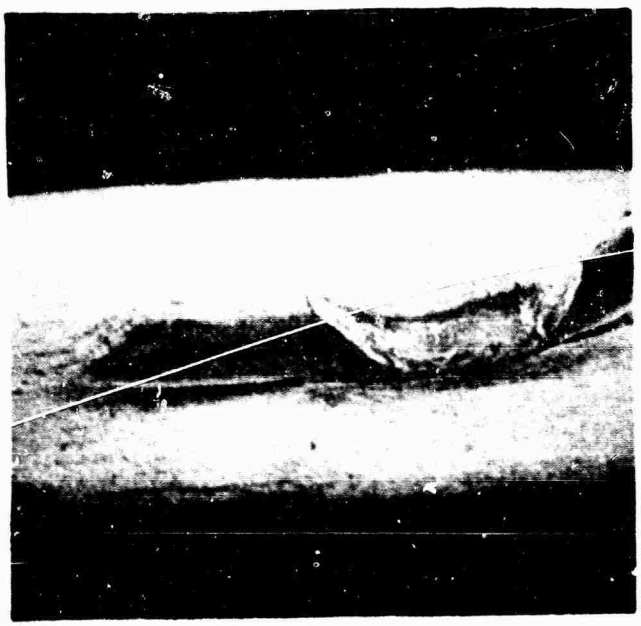
FIGURE A2 - INTERCONNECTION PHOTOGRAPH

620X
(SEM-1.2KV)



S/N A11

FIGURE A3 - WIRE BOND AT DIE



350X
(SEM-1.2KV)

S/N A11

FIGURE A4 - WIRE BOND AT LEAD FRAME

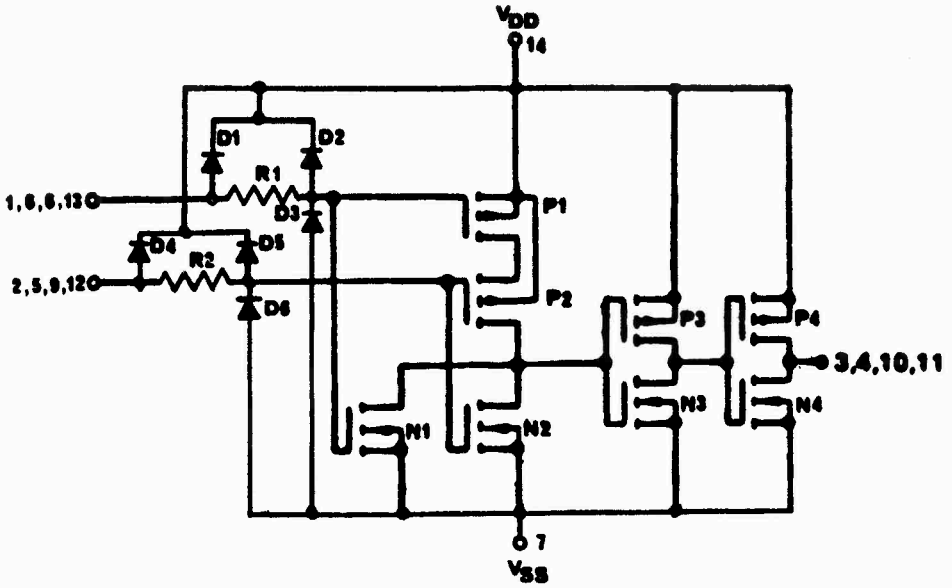


FIGURE A5 - SCHEMATIC DIAGRAM OF ONE NOR GATE

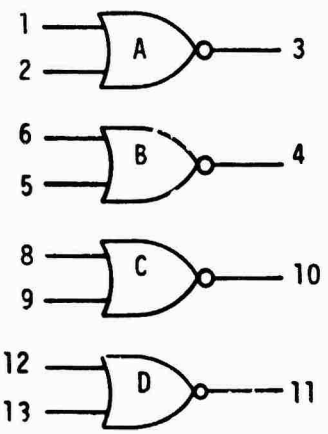
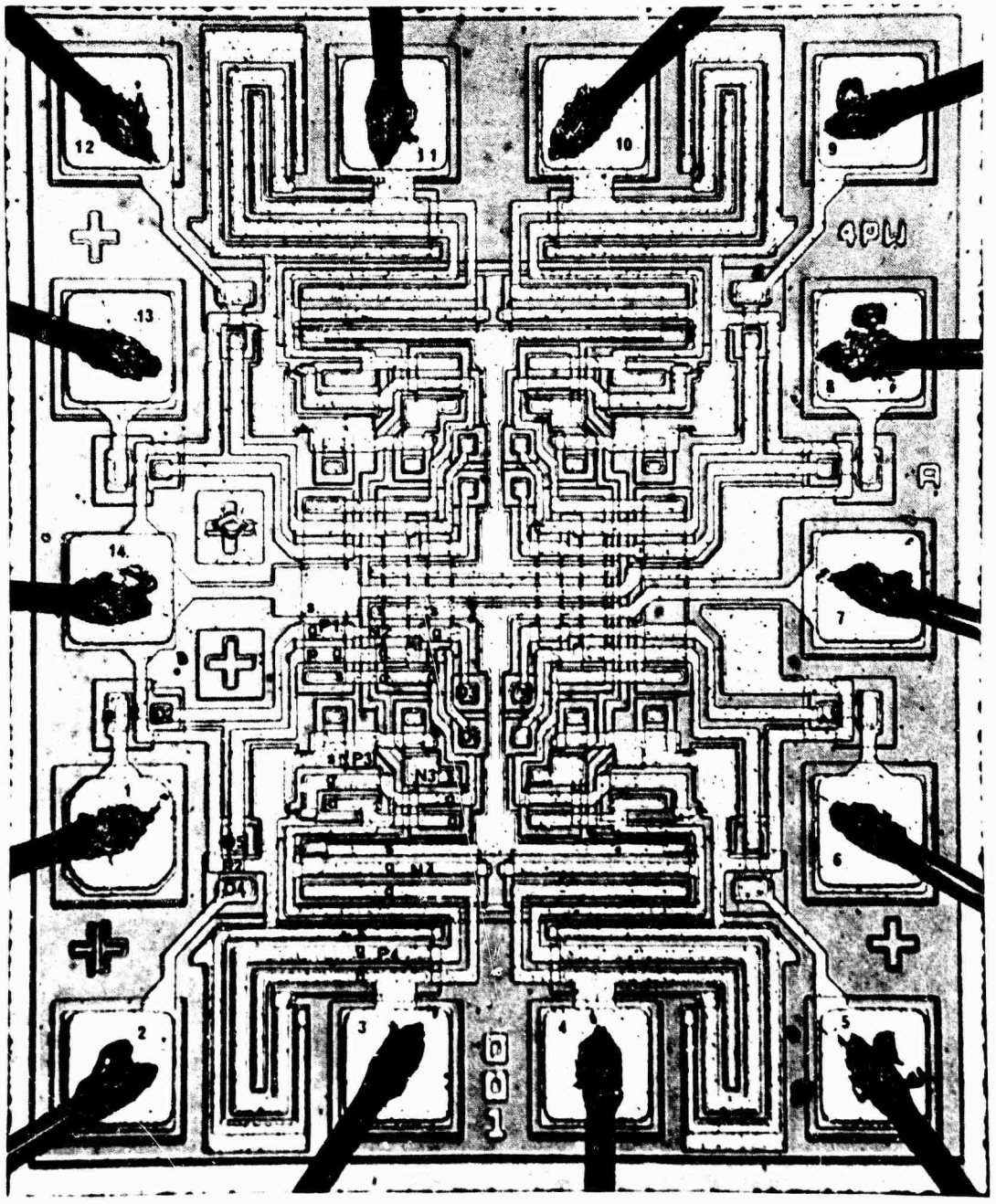


FIGURE A6 LOGIC DIAGRAM



145X

S/N C142

FIGURE A7 - DIE PHOTOGRAPHY

APPENDIX A2

CONSTRUCTION ANALYSIS

4001B

MANUFACTURER B

QUAD 2-INPUT NOR GATE

DATE CODE 7705

MICROCIRCUIT CONSTRUCTION INFORMATION
BASELINE ANALYSIS

S/N C125 DATE CODE 7705 DATE: 5/2/77

PART NAME: QUAD 2-INPUT NOR GATE

MANUFACTURER'S PART NO: CCL4001/BD MANUFACTURER: B

GENERIC PART NO: 4001B PACKAGE TYPE: 14 PIN DIP

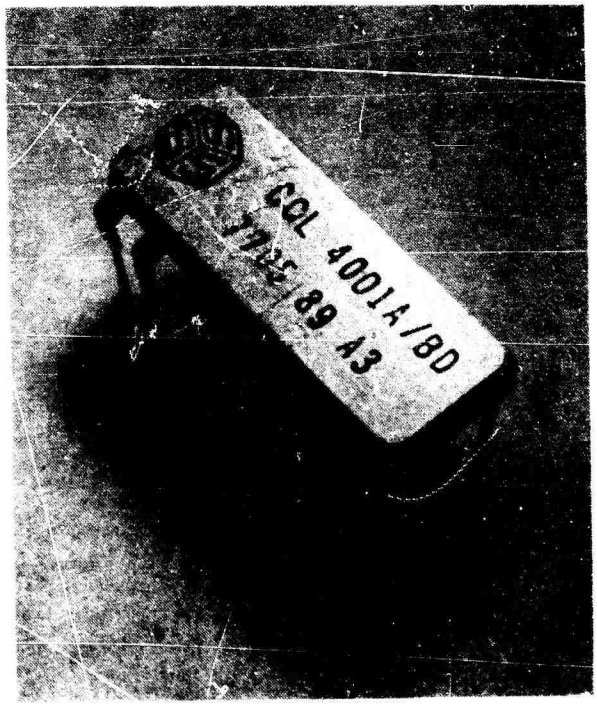
MILITARY SPECIFICATION TYPE: M38510/05202BCC

DESCRIPTION	DETAIL
DIE	
Passivation Type	Silicon Dioxide
Glassivation Type	Phosphorus Glass
Basic Die Construction	Planar
Die Dimensions	0.049 X 0.035
Metallization Type	Aluminum
Metallization Thickness	———
Number of Metallization Layers	One
Metallization Interlayer Insulation Type	None
Bonding Pad Size	0.0038 X 0.0038
Die Photograph	(See Figure A14)
Scribe Method	Mechanical
INTERCONNECTIONS	
Die Mounting Material	Gold Silicon Eutectic
Wire Material	Aluminum
Wire Diameter	0.001
Longest Lead Length	0.106
Wire Bond Type(s) Post	Ultrasonic (See Figure A11)
Die	Ultrasonic (See Figure A10)
Interconnection Photograph	(See Figure A9)

DESCRIPTION	DETAIL
PACKAGE	
Lead/Lead Frame Material	Kovar
Lead/Lead Frame Finish - Internal	Gold Plate
Lead/Lead Frame Finish - External	Gold Plate
Lead/Lead Frame Finish - Feed Thru	Molybdenum-Manganese
Header/Case Material	Ceramic
Cap/Lid Material	Gold Plated Kovar
Case Seal Material/Method	Solder
Lead Seal Material/Method	Ceramic
Cavity Size	0.161 X 0.384
Package Photograph	(See Figure A8)

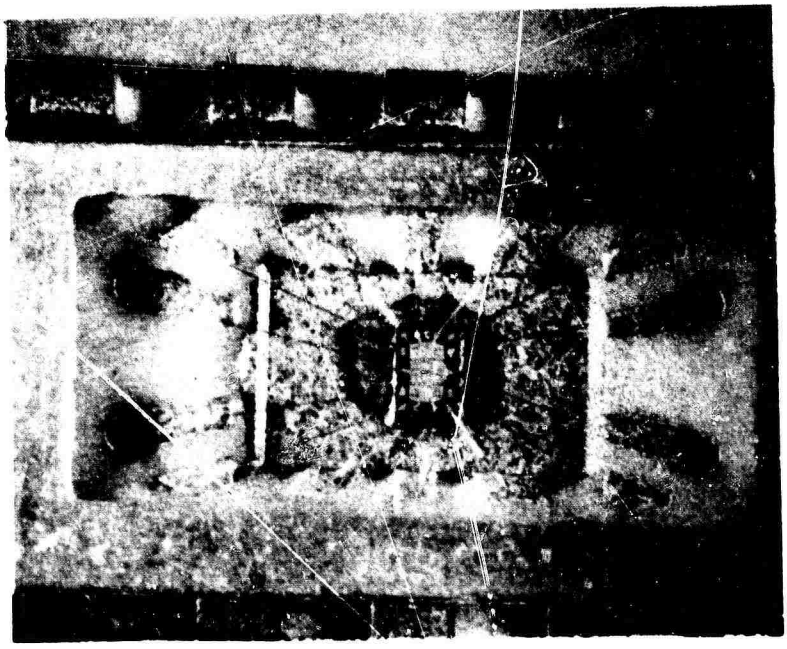
Note:

1. All dimensions are in inches.



3X S/N C125

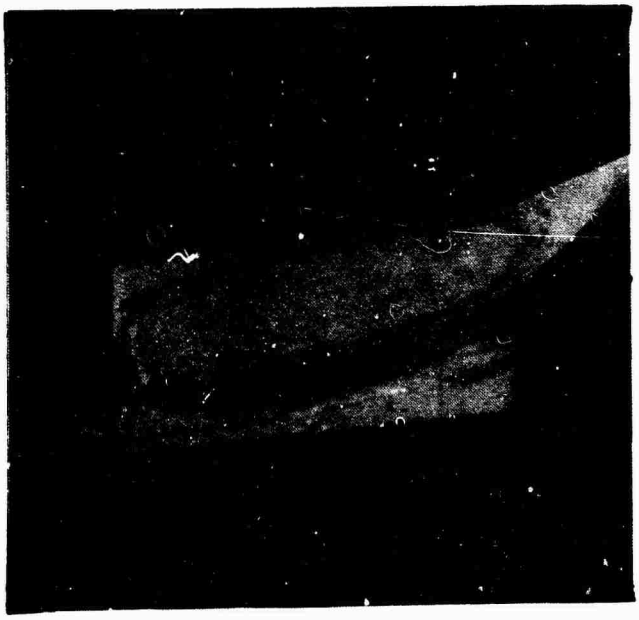
FIGURE A8 - PACKAGE PHOTOGRAPH



10X S/N C125

FIGURE A9 - INTERCONNECTION PHOTOGRAPH

700X
(SEM-1.2KV)



S/N C125

FIGURE A10 - WIRE BOND AT DIE

430X
(SEM-1.2KV)

S/N C125

FIGURE A11 - WIRE BOND AT LEAD FRAME

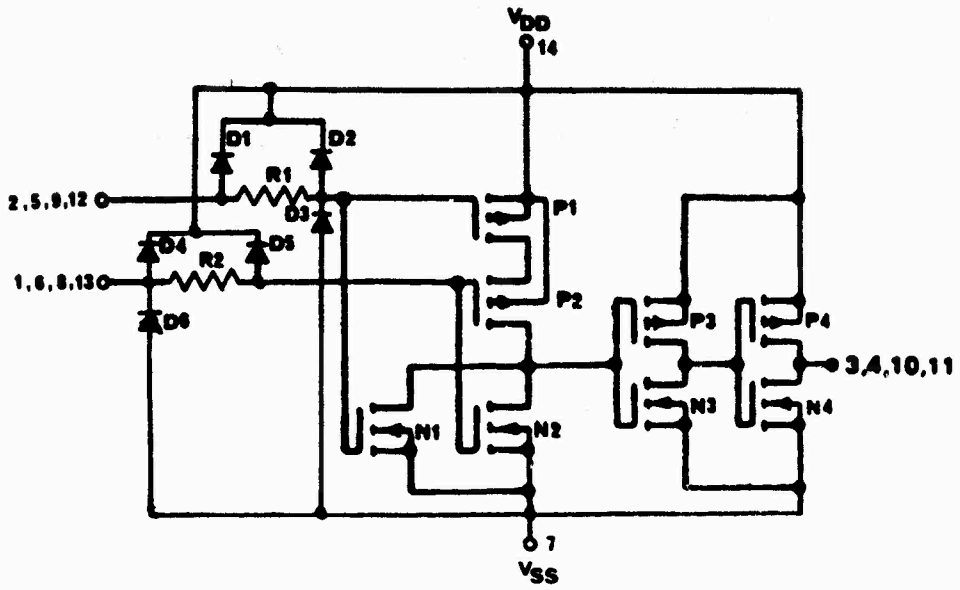


FIGURE A12 - SCHEMATIC DIAGRAM OF ONE NOR GATE

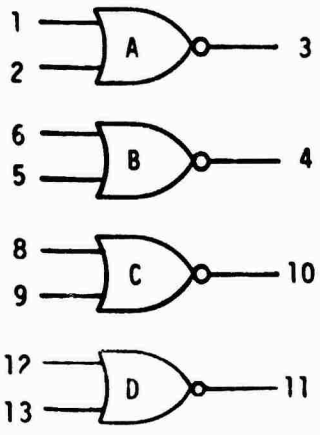
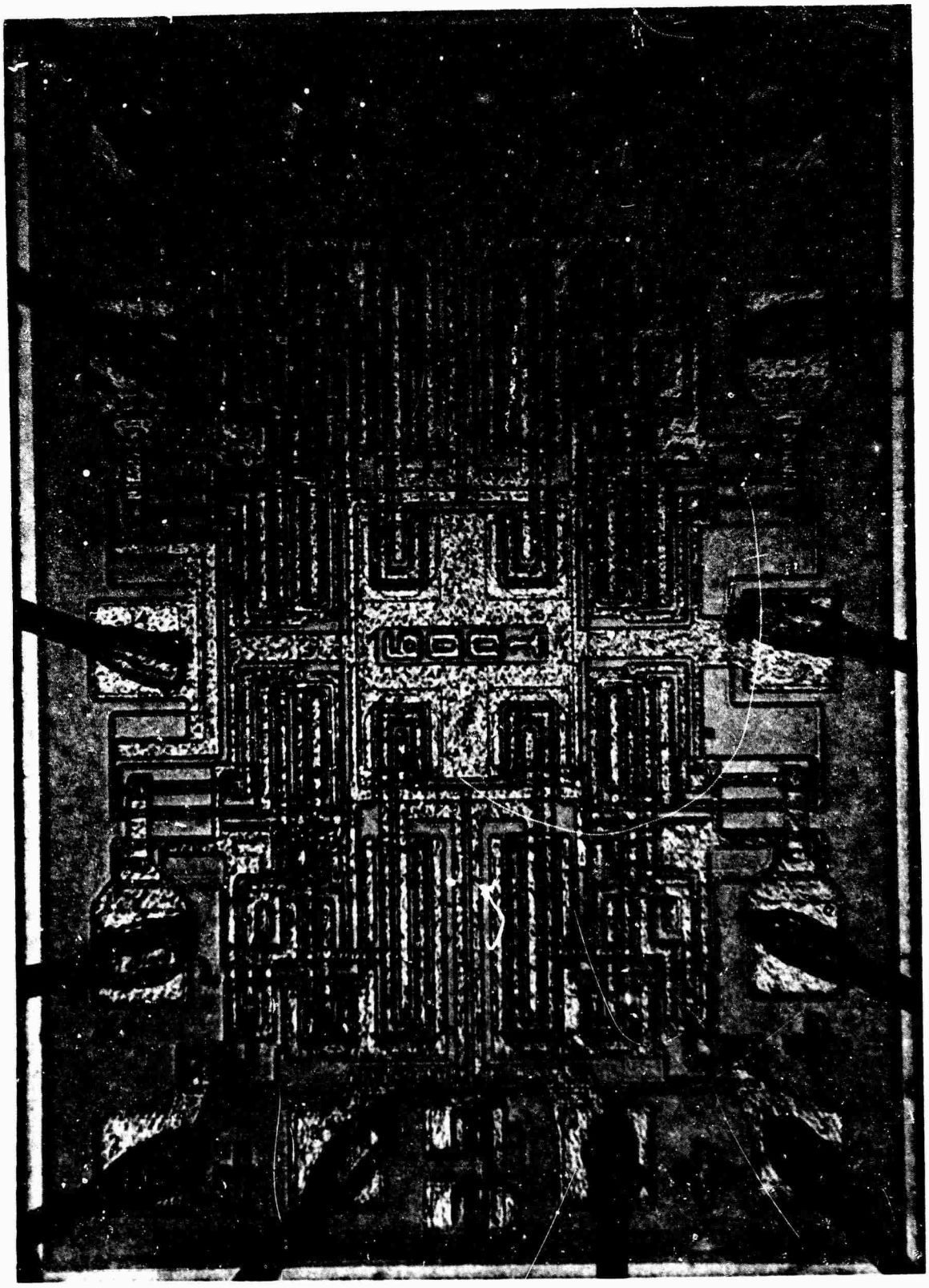


FIGURE A13 - LOGIC DIAGRAM



200X S/N 0125

FIGURE A13 - DIE PHOTOGRAPH

APPENDIX A3

CONSTRUCTION ANALYSIS

4013B

MANUFACTURER C

DUAL D EDGE TRIGGERED FLIP FLOP

DATE CODE 7652C

MICROCIRCUIT CONSTRUCTION INFORMATION
BASELINE ANALYSIS

S/N C141 DATE CODE 7652 DATE: 5/2/77

PART NAME: DUAL D EDGE TRIGGERED FLIP FLOP WITH CLEAR AND PRESET

MANUFACTURER'S PART NO: CD4013BJ/RC3383 MANUFACTURER: C

GENERIC PART NO: 4013B PACKAGE TYPE: 14 PIN DIP

MILITARY SPECIFICATION TYPE: M38510/05101BDC

DESCRIPTION	DETAIL
DIE	
Passivation Type	Silicon Dioxide
Glassivation Type	Vapox
Basic Die Construction	Planar
Die Dimensions	0.054 X 0.063
Metallization Type	Aluminum
Metallization Thickness	———
Number of Metallization Layers	One
Metallization Interlayer Insulation Type	None
Bonding Pad Size	0.005 X 0.005
Die Photograph	(See Figure A21)
Scribe Method	Mechanical
INTERCONNECTIONS	
Die Mounting Material	Gold Silicon Eutectic
Wire Material	Aluminum
Wire Diameter	0.001
Longest Lead Length	0.078
Wire Bond Type(s) Post	Ultrasonic (See Figure A18)
Die	Ultrasonic (See Figure A17)
Interconnection Photograph	(See Figure A16)

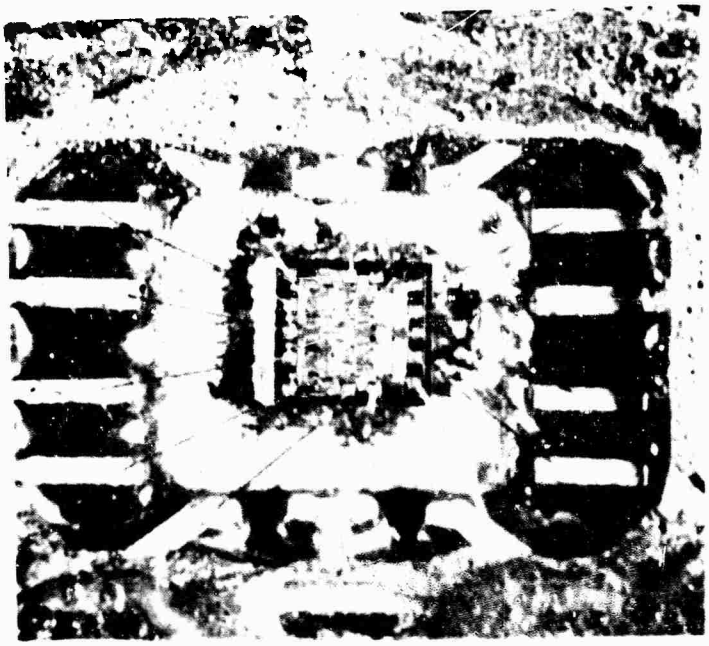
DESCRIPTION	DETAIL
PACKAGE	
Lead/Lead Frame Material	Alloy 42
Lead/Lead Frame Finish - Internal	Gold Plate
Lead/Lead Frame Finish - External	Gold Plate
Lead/Lead Frame Finish - Feed Thru	None
Header/Case Material	Ceramic
Cap/Lid Material	Ceramic
Case Seal Material/Method	Glass Frit
Lead Seal Material/Method	Glass Frit
Cavity Size	0.159 X 0.263
Package Photograph	(See Figure A15)

Note:

1. All dimensions are in inches.

4X S/N C143

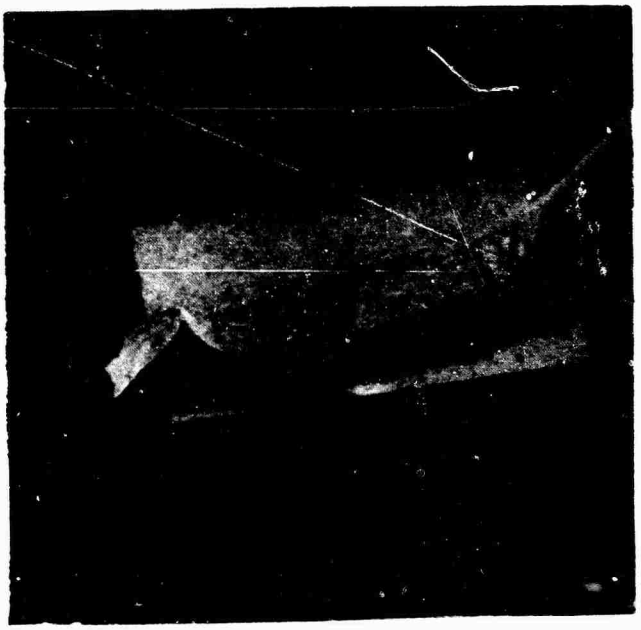
FIGURE A15 - PACKAGE PHOTOGRAPH



15X S/N C143

FIGURE [illegible] - INTERCONNECTION PHOTOGRAPH

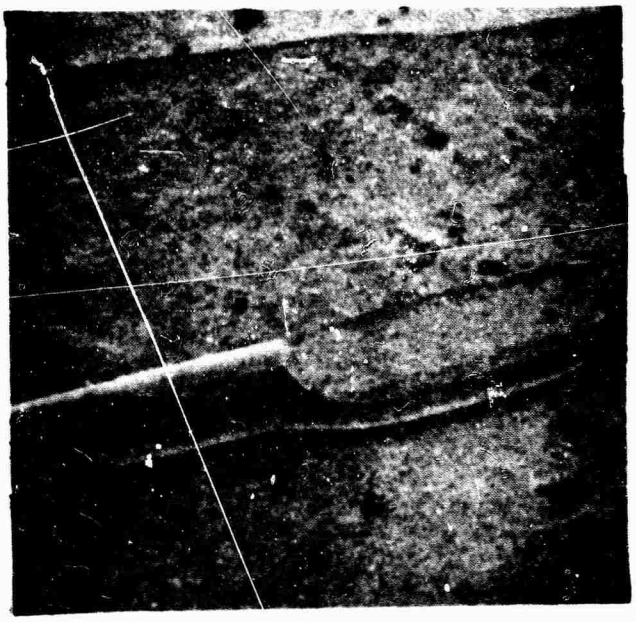
525X
(SEM-1.2KV)



S/N C141

FIGURE A17 - WIRE BOND AT DIE

430X
(SEM-1.2KV)



S/N C141

FIGURE A18 - WIRE BOND AT LEAD FRAME

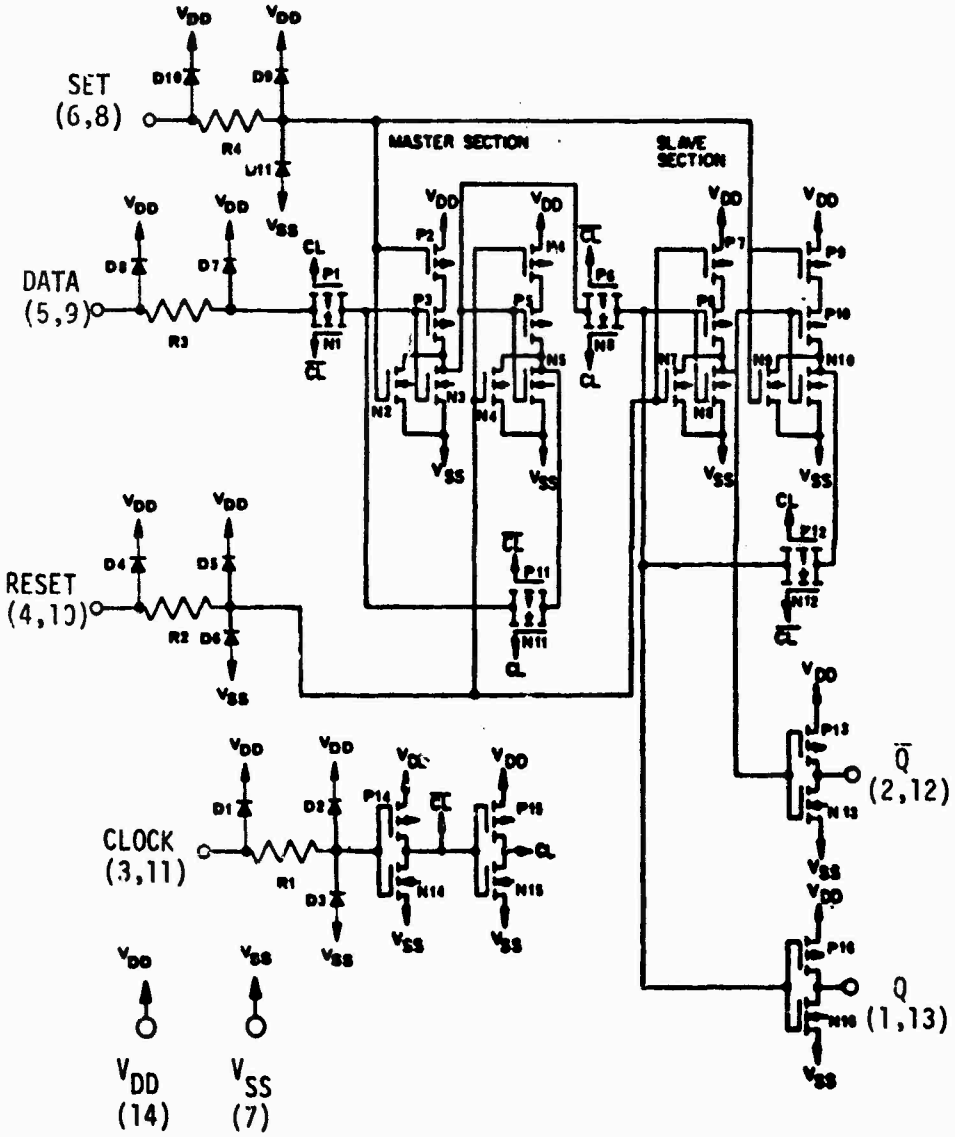


FIGURE A19 - SCHEMATIC DIAGRAM OF ONE FLIP/FLOP

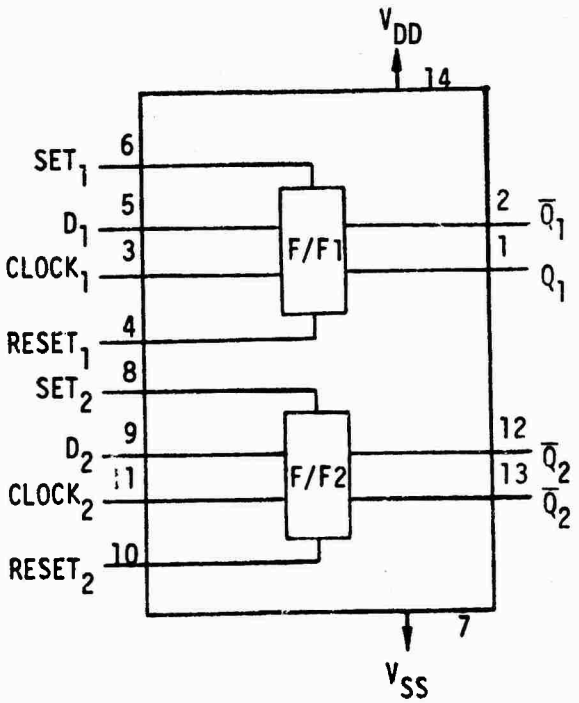
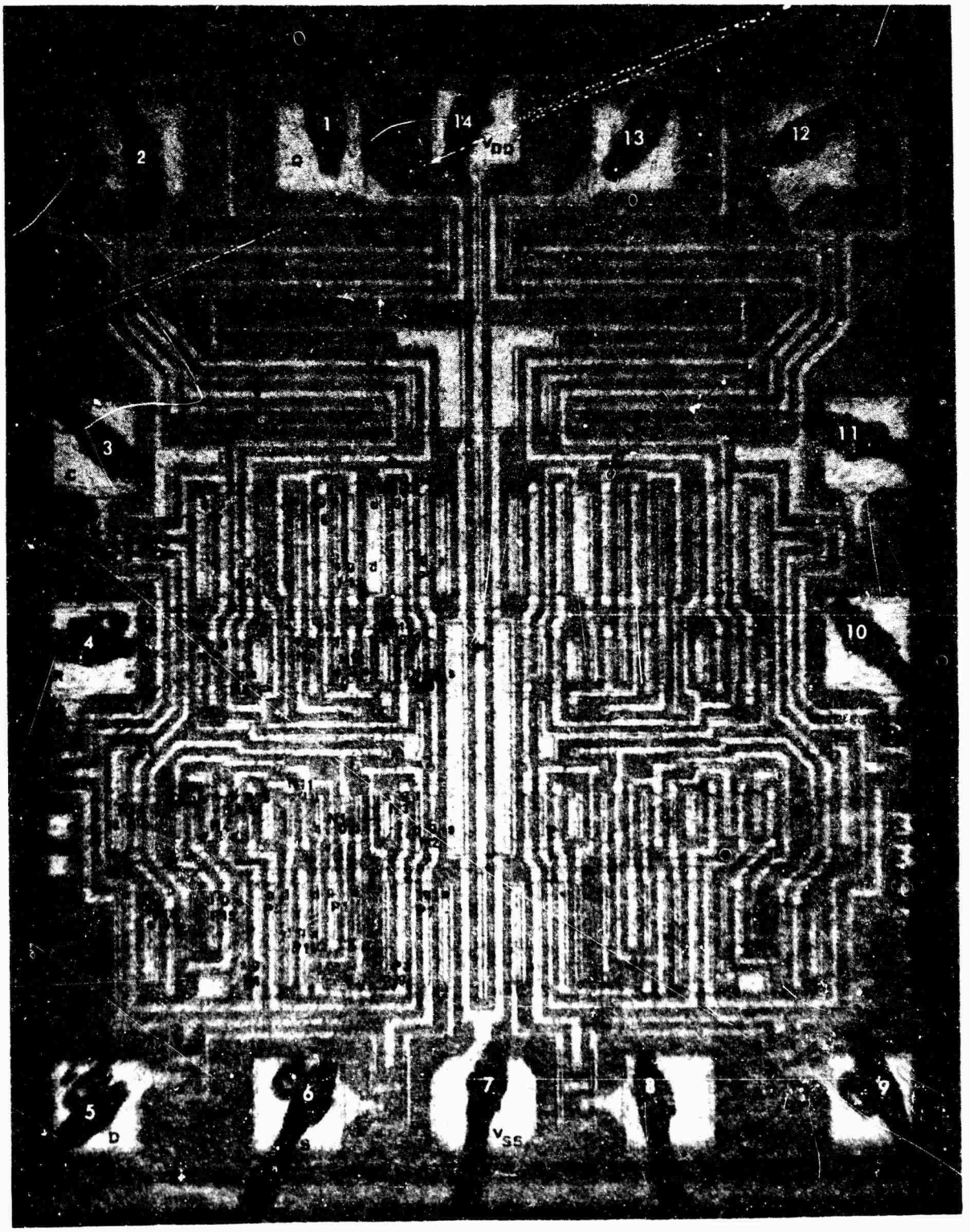


FIGURE A20 - LOGIC DIAGRAM



142X

S-A-0141

FIGURE A23 - DIE PHOTOGRAPH

APPENDIX A4

CONSTRUCTION ANALYSIS

4013B

MANUFACTURER B

DUAL D EDGE TRIGGERED FLIP FLOP

DATE CODE 7643

MICROCIRCUIT CONSTRUCTION INFORMATION
BASELINE ANALYSIS

S/N A23 DATE CODE 7643 DATE: 5/2/77

PART NAME: DUAL D EDGE TRIGGERED FLIP FLOP

MANUFACTURER'S PART NO: CCL4013A/BD MANUFACTURER: B

GENERIC PART NO: 4013B PACKAGE TYPE: 14 PIN DIP

MILITARY SPECIFICATION TYPE: M38510/05101BDC

DESCRIPTION	DETAIL
DIE	
Passivation Type	Silicon Dioxide
Glassivation Type	Phosphorus Glass
Basic Die Construction	Planar
Die Dimensions	0.047 X 0.057
Metallization Type	Aluminum
Metallization Thickness	———
Number of Metallization Layers	One
Metallization Interlayer Insulation Type	None
Bonding Pad Size	0.0037 X 0.0037
Die Photograph	(See Figure A28)
Scribe Method	Mechanical
INTERCONNECTIONS	
Die Mounting Material	Gold Silicon Eutectic
Wire Material	Aluminum
Wire Diameter	0.001
Longest Lead Length	0.106
Wire Bond Type(s) Post	Ultrasonic (See Figure A25)
Die	Ultrasonic (See Figure A24)
Interconnection Photograph	(See Figure A23)

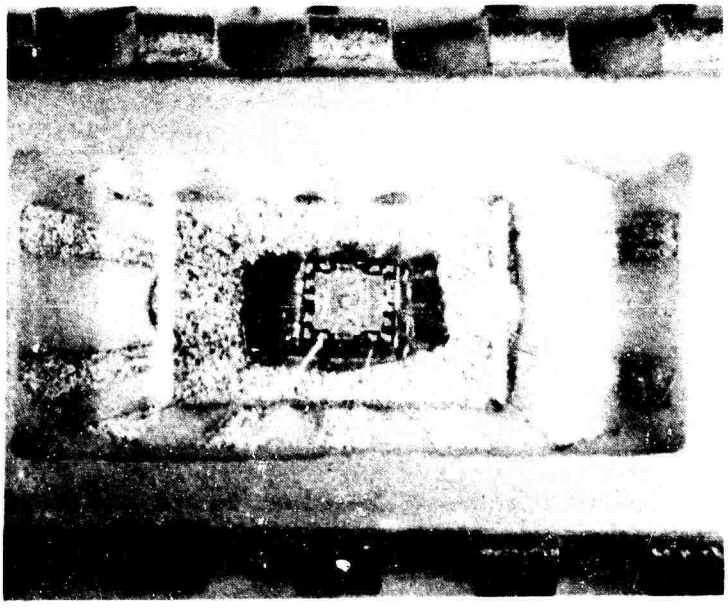
DESCRIPTION	DETAIL
PACKAGE	
Lead/Lead Frame Material	Kovar
Lead/Lead Frame Finish - Internal	Gold Plate
Lead/Lead Frame Finish - External	Gold Plate
Lead/Lead Frame Finish - Fced Thru	Molybdenum-Manganese
Header/Case Material	Ceramic
Cap/Lid Material	Gold Plated Kovar
Case Seal Material/Method	Solder
Lead Seal Material/Method	Ceramic
Cavity Size	0.161 X 0.383
Package Photograph	(See Figure A22)

Note:

1. All dimensions are in inches.

21X S/N A23

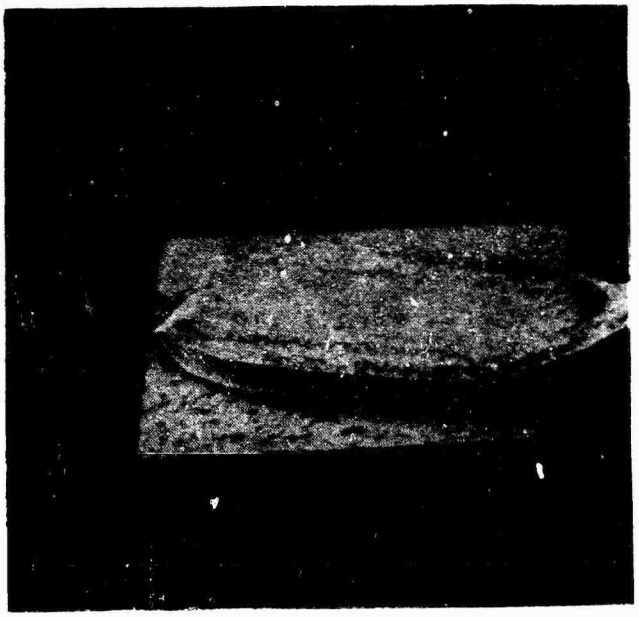
FIGURE A22 - PACKAGE PHOTOGRAPH



10X S/N A23

FIGURE A23 - INTERCONNECTION PHOTOGRAPH

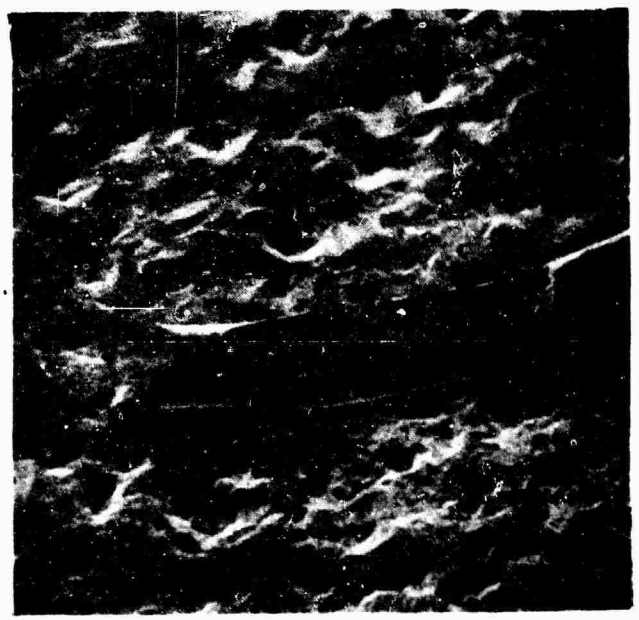
660X
(SEM-1.2KV)



S/N A23

FIGURE A24 - WIRE BOND AT DIE

930X
(SEM-1.2KV)



S/N A23

FIGURE A25 - WIRE BOND AT LEAD FRAME

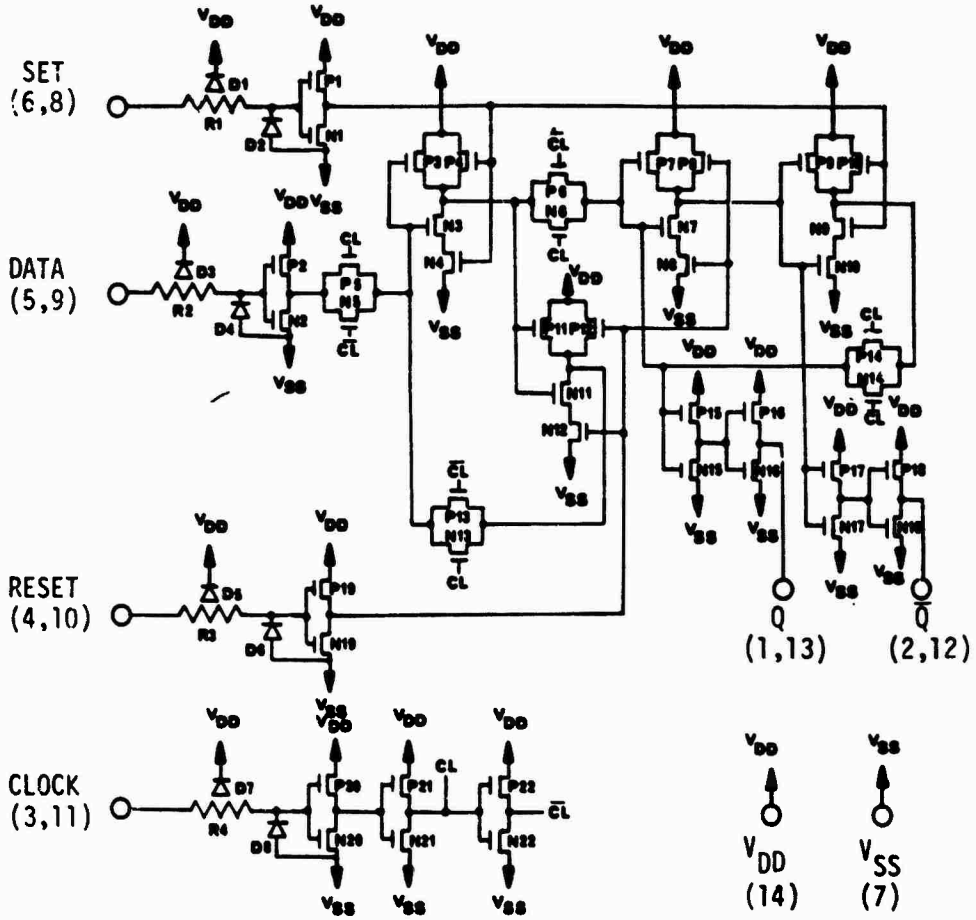


FIGURE A26 - SCHEMATIC DIAGRAM OF ONE FLIP/FLOP

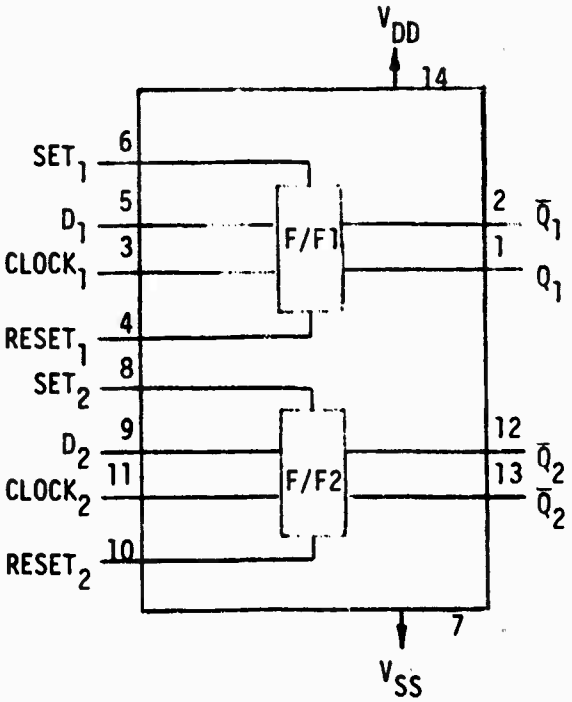
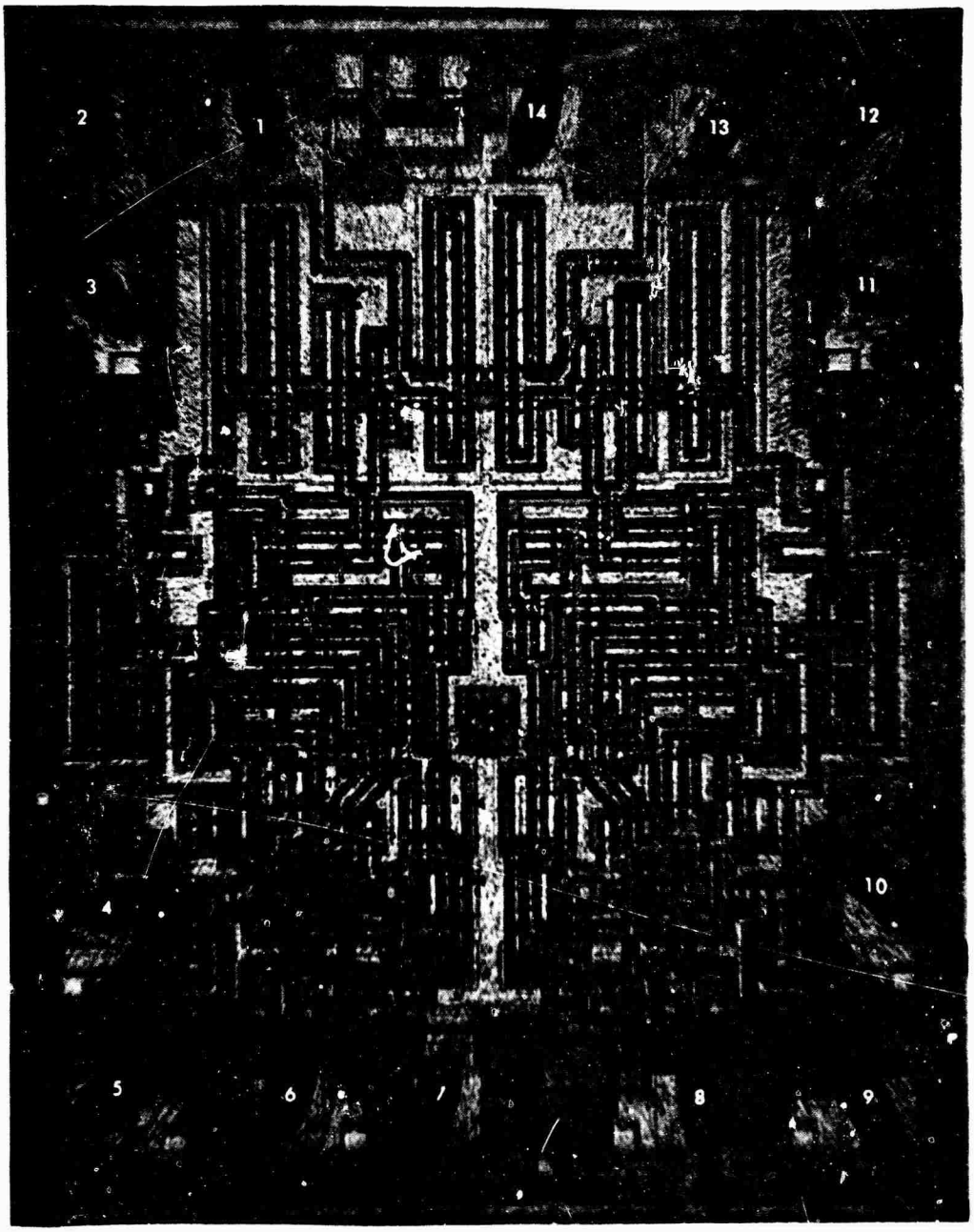


FIGURE A27 FUNCTIONAL BLOCK DIAGRAM



124X S/N A23

FIGURE A28 - DIE PHOTOGRAPH

APPENDIX A5

CONSTRUCTION ANALYSIS

M38510/05401BDC

MANUFACTURER C

FOUR BIT FULL ADDER

DATE CODE 7652A

MICROCIRCUIT CONSTRUCTION INFORMATION
BASELINE ANALYSIS

S/N A22 DATE CODE 7652A DATE: 5/2/77

PART NAME: FOUR BIT FULL ADDER

MANUFACTURER'S PART NO: MM4608BJ/RC33384 MANUFACTURER: C

GENERIC PART NO: 4008 PACKAGE TYPE: 16 PIN DIP

MILITARY SPECIFICATION TYPE: M38510/05401BDC

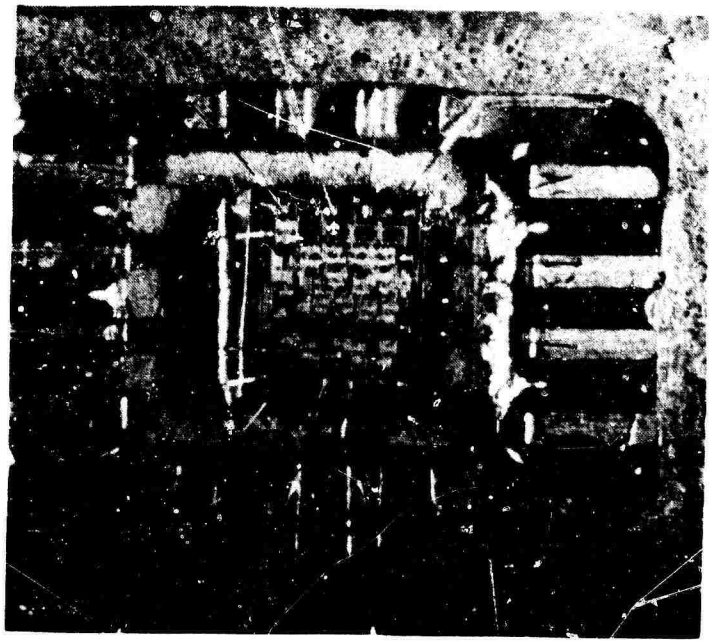
DESCRIPTION	DETAIL
DIE	
Passivation Type	Silicon Dioxide
Glassivation Type	Vapox
Basic Die Construction	Planar
Die Dimensions	0.071 X 0.080
Metallization Type	Aluminum
Metallization Thickness	———
Number of Metallization Layers	One
Metallization Interlayer Insulation Type	None
Bonding Pad Size	0.0044 X 0.0044
Die Photograph	(See Figure A36)
Scribe Method	Mechanical
INTERCONNECTIONS	
Die Mounting Material	Gold-Silicon Eutectic
Wire Material	Aluminum
Wire Diameter	0.001
Longest Lead Length	0.115
Wire Bond Type(s) Post	Ultrasonic (See Figure A32)
Die	Ultrasonic (See Figure A31)
Interconnection Photograph	(See Figure A30)

DESCRIPTION	DETAIL
PACKAGE	
Lead/Lead Frame Material	Alloy 42
Lead/Lead Frame Finish - Internal	Aluminum Plate
Lead/Lead Frame Finish - External	Gold Plate
Lead/Lead Frame Finish - Feed Thru	None
Header/Case Material	Ceramic
Cap/Lid Material	Ceramic
Case Seal Material/Method	Glass Frit
Lead Seal Material/Method	Glass Frit
Cavity Size	0.161 X 0.270
Package Photograph	(See Figure A29)

Note:
1. All dimensions are in inches.

4X S/N A22

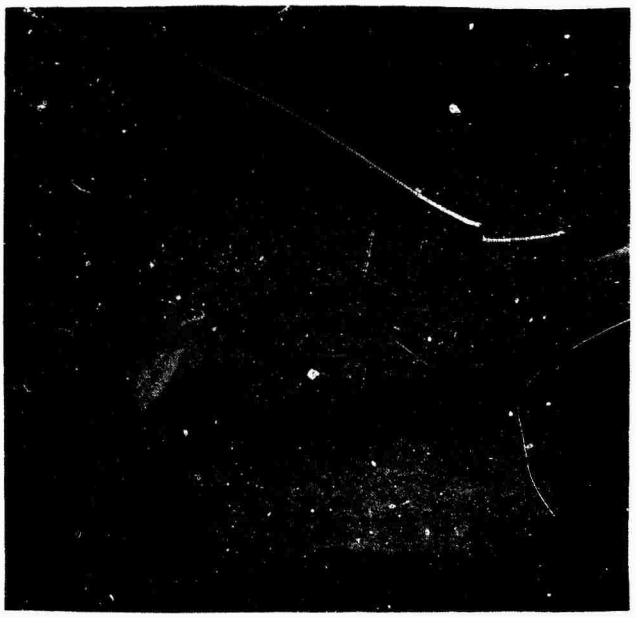
FIGURE A29 - PACKAGE PHOTOGRAPH



13X S/N A22

FIGURE A30 - INTERCONNECTION PHOTOGRAPH

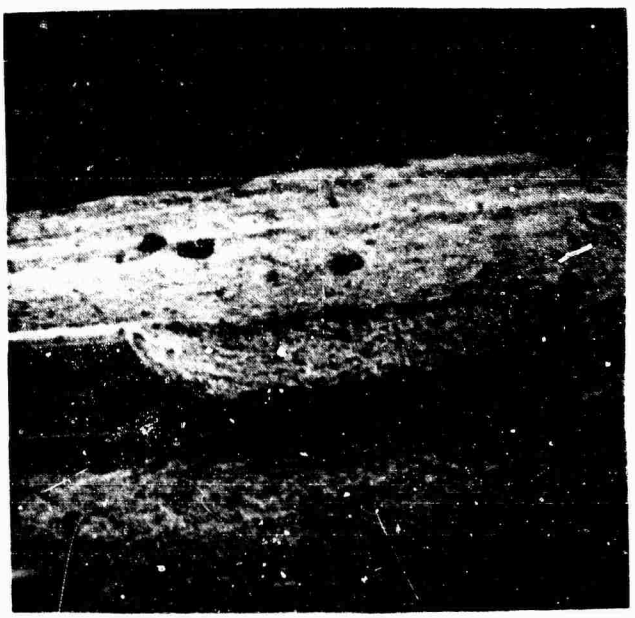
530X
(SEM-1.2KV)



S/N A23

FIGURE A31 - WIRE BOND AT DIE

530X
(SEM-1.2KV)



S/N A23

FIGURE A32 - WIRE BOND AT LEAD FRAME

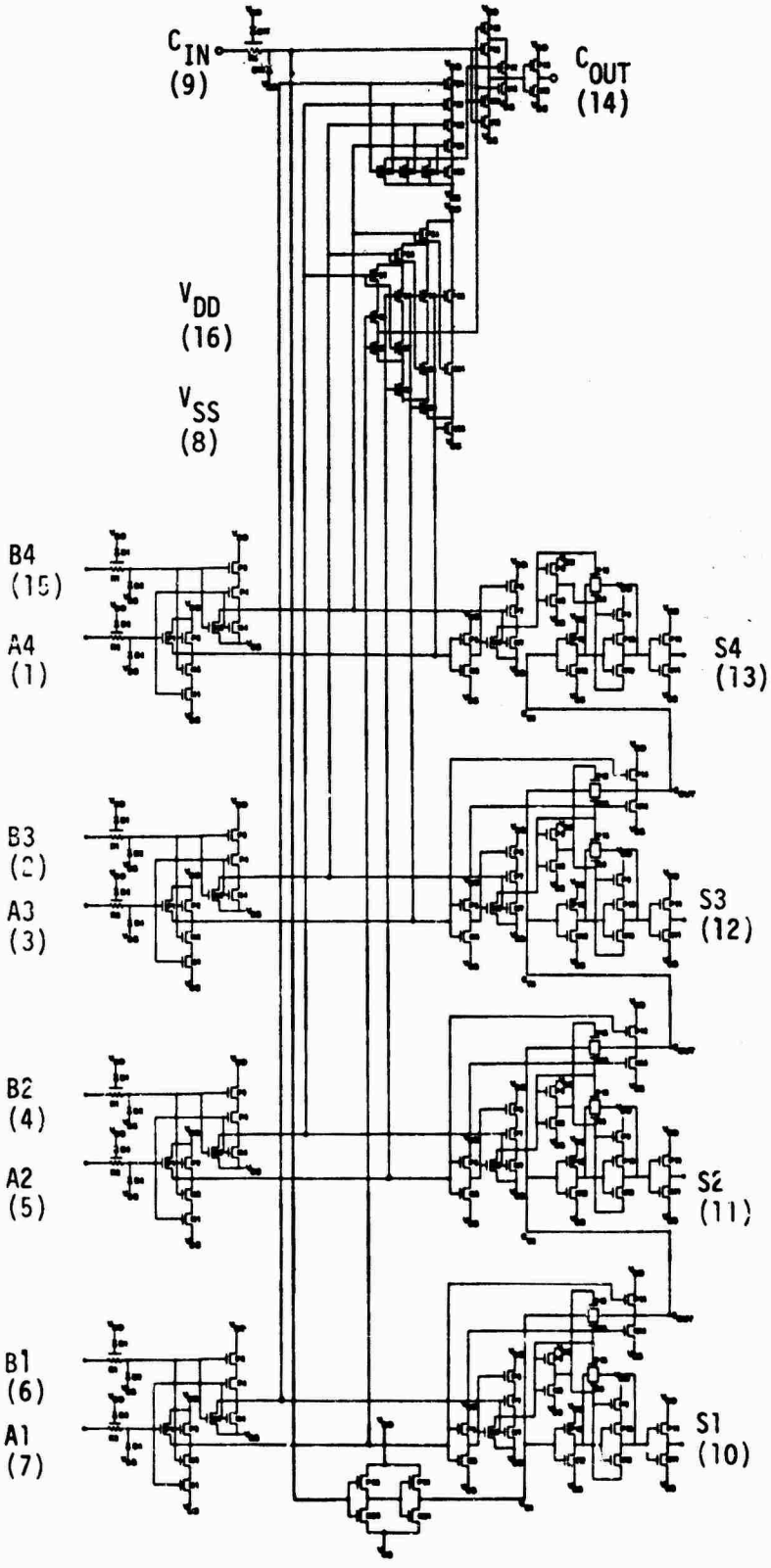


FIGURE A33. SCHEMATIC DIAGRAM

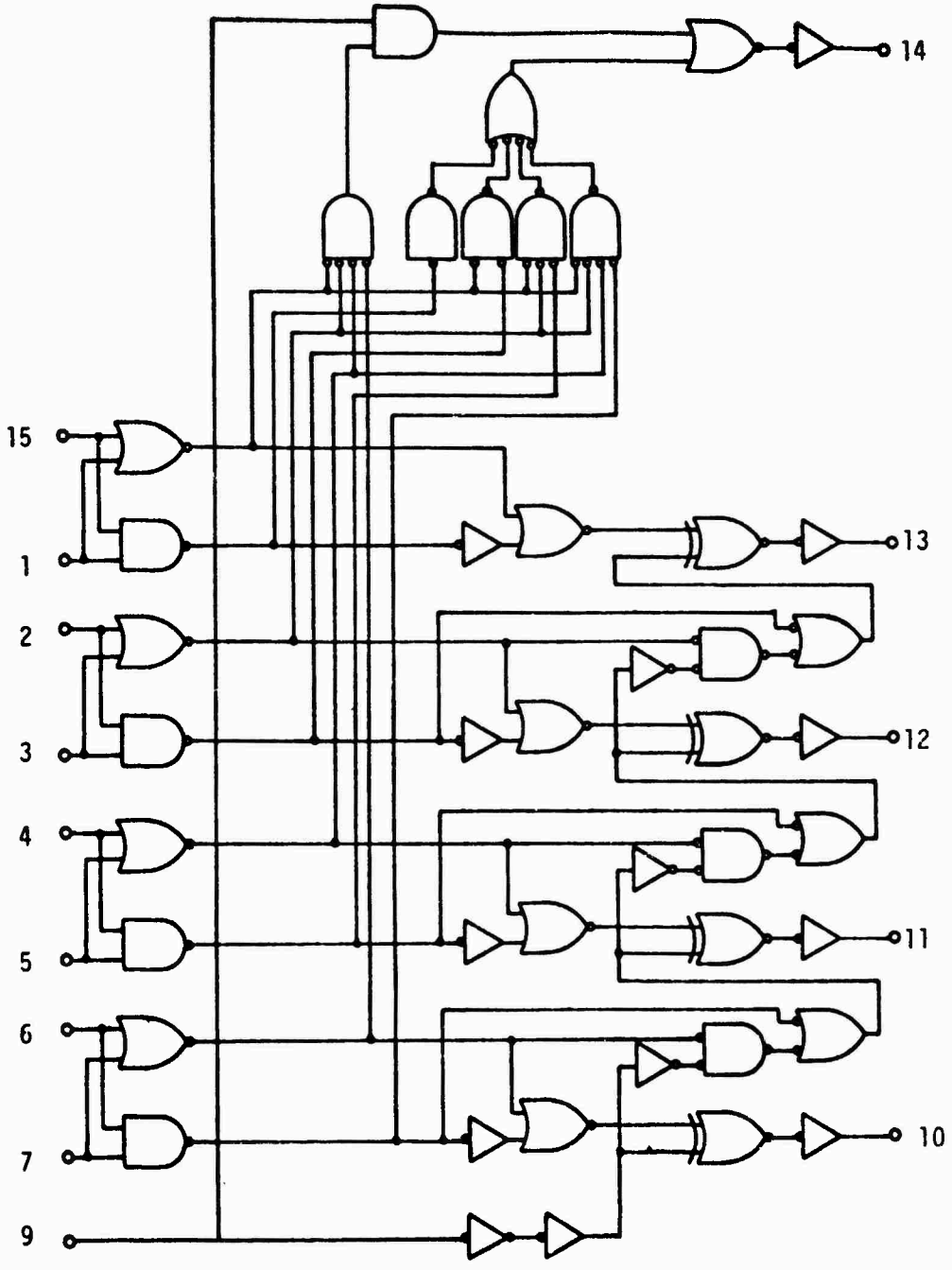
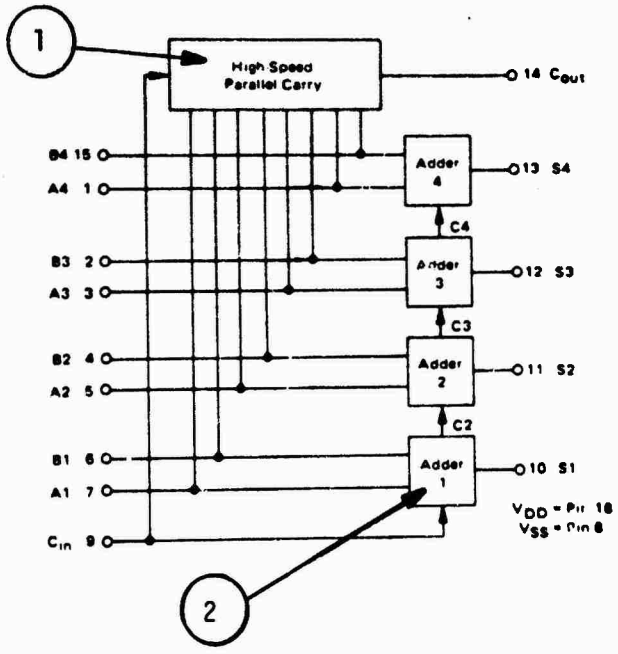


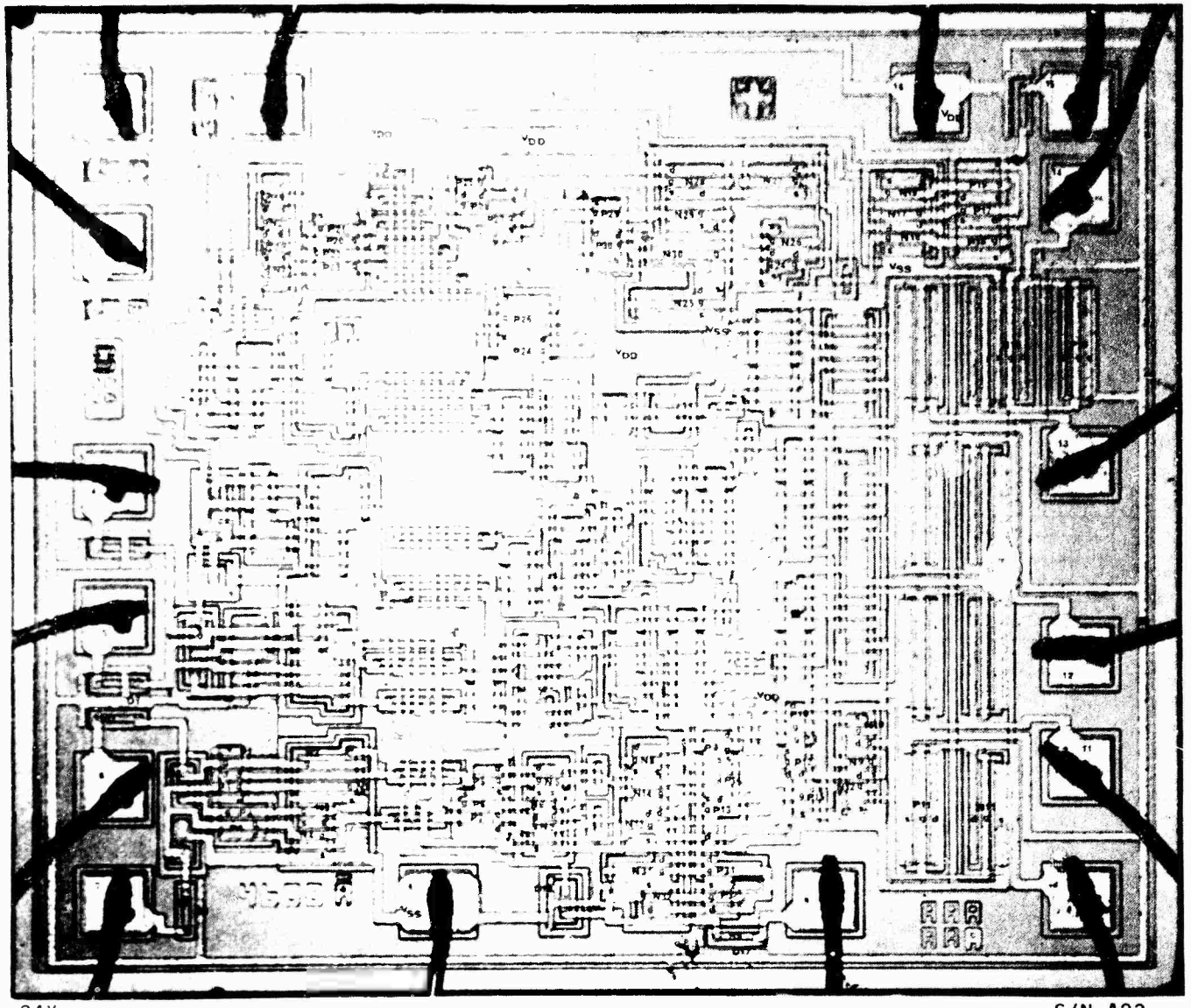
FIGURE A34. LOGIC DIAGRAM



1 PARALLEL CARRY CIRCUIT - FIGURE A37 AND FIGURE A38

2 ADDER CIRCUIT - FIGURE A39 AND FIGURE A40

FIGURE A35 - FUNCTIONAL BLOCK DIAGRAM



94X S/N A23

FIGURE A36 - DIE PHOTOGRAPH

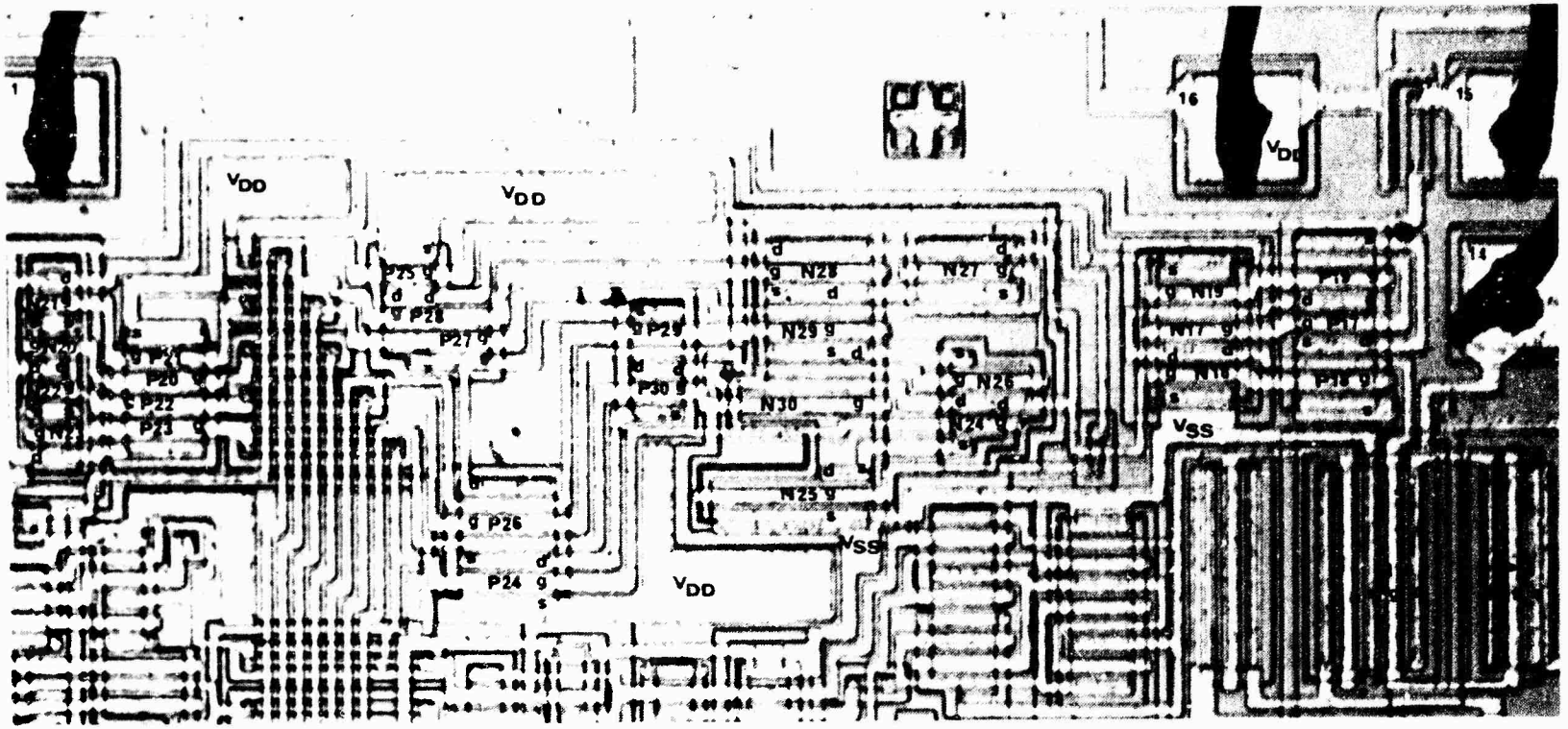


FIGURE A 37 - PARALLEL CARRY CIRCUIT

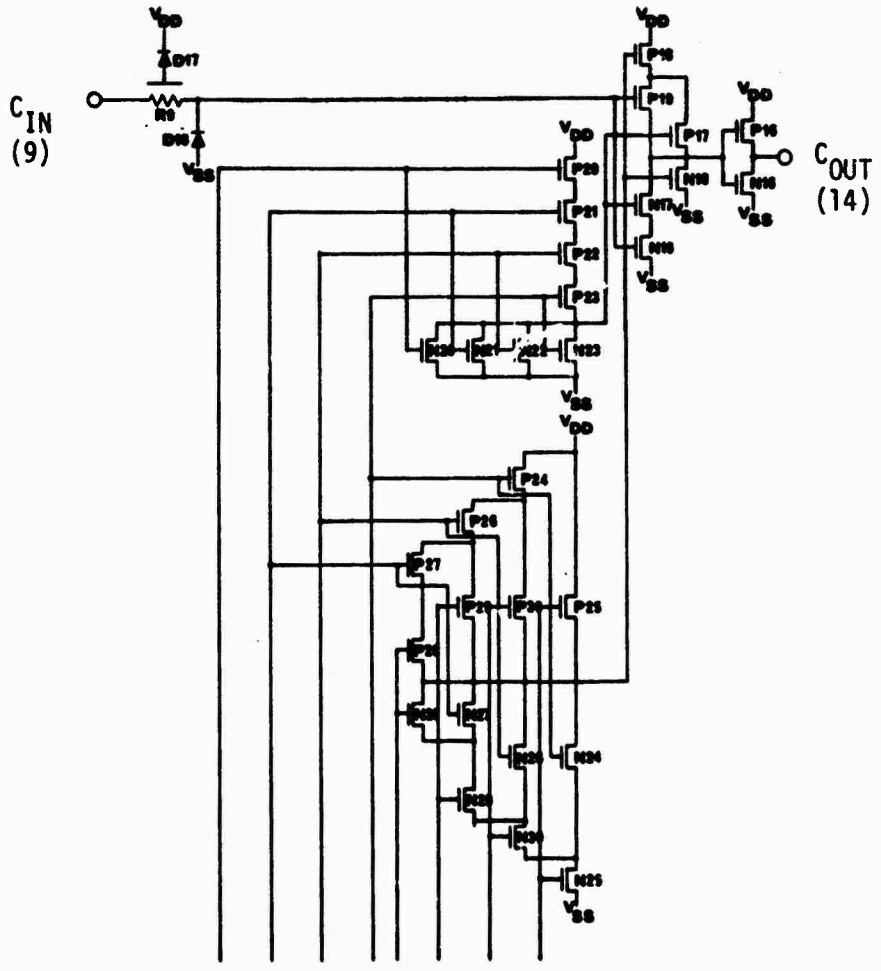


FIGURE A 38 - SCHEMATIC DIAGRAM OF PARALLEL CARRY CIRCUIT

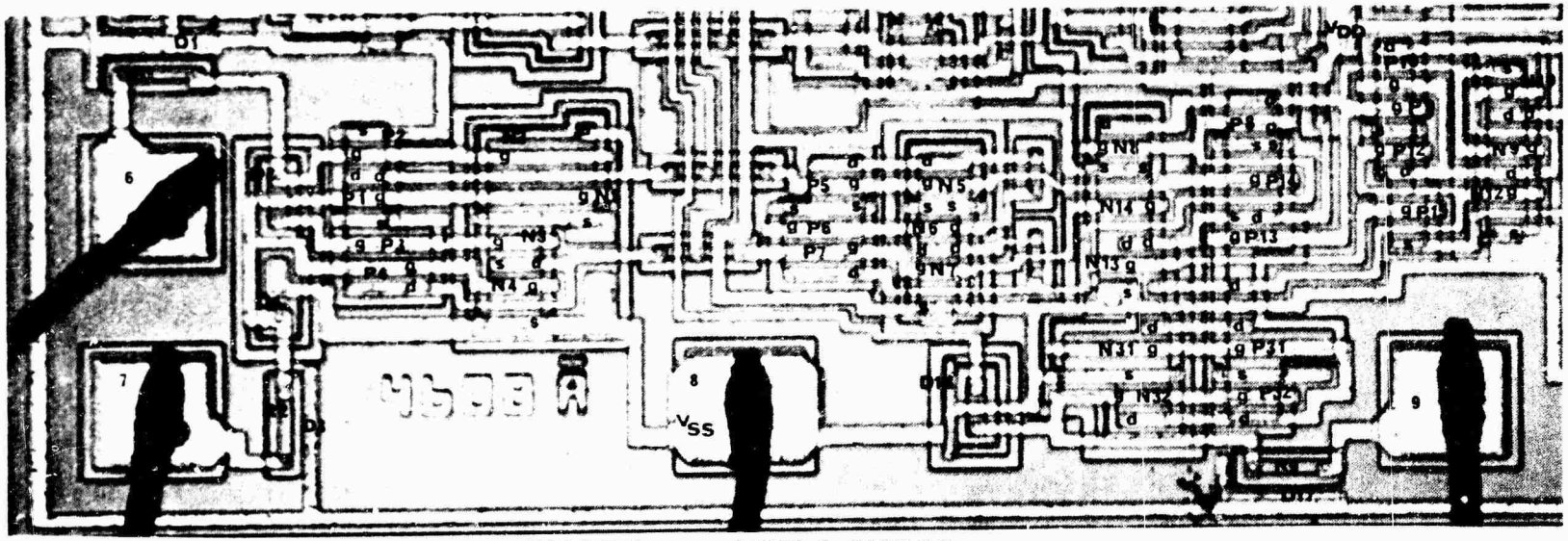


FIGURE A39 - ADDER 1 CIRCUIT

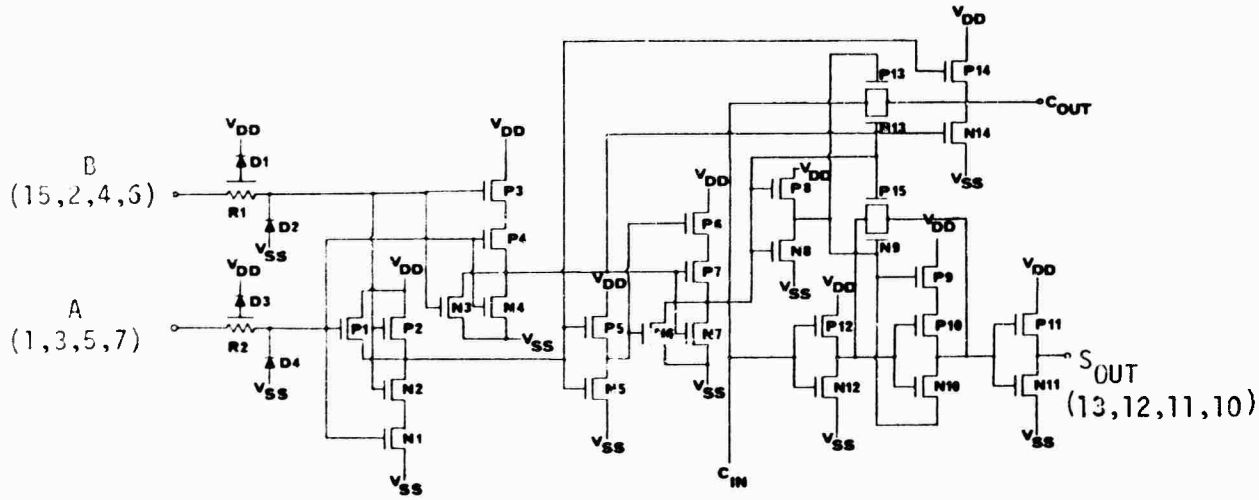


FIGURE A40 - SCHEMATIC DIAGRAM OF A TYPICAL ADDER CIRCUIT

APPENDIX A6

CONSTRUCTION ANALYSIS

M38510/05401BEC

MANUFACTURER D

FOUR BIT FULL ADDER

DATE CODE 7703

MICROCIRCUIT CONSTRUCTION INFORMATION
BASELINE ANALYSIS

S/N C154 DATE CODE 7703 DATE: 5/2/77

PART NAME: FOUR BIT FULL ADDER

MANUFACTURER'S PART NO: 85744 MANUFACTURER: D

GENERIC PART NO: 4008R PACKAGE TYPE: 16 PIN DIP

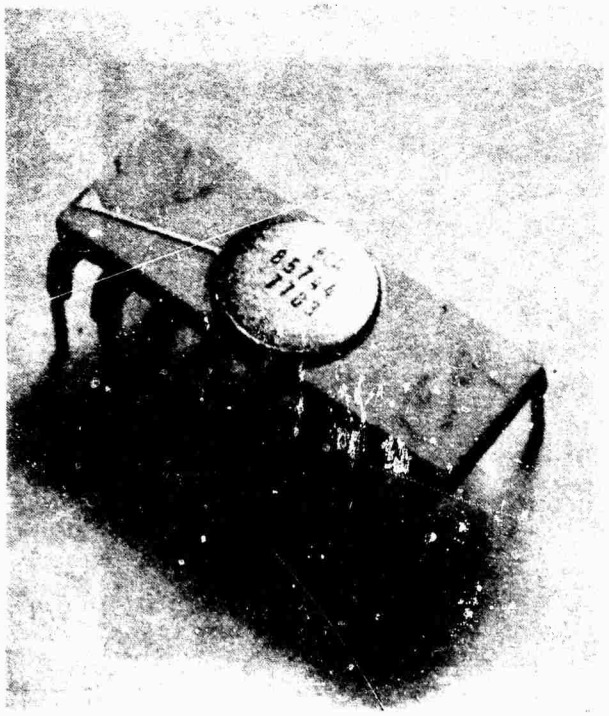
MILITARY SPECIFICATION TYPE: M38510/05401BEC

DESCRIPTION	DETAIL
DIE	
Passivation Type	Silicon Dioxide
Glassivation Type	Silicon Dioxide
Basic Die Construction	Planar
Die Dimensions	0.081 X 0.085
Metallization Type	Aluminum
Metallization Thickness	———
Number of Metallization Layers	One
Metallization Interlayer Insulation Type	None
Bonding Pad Size	0.004 X 0.004
Die Photograph	(See Figure A48)
Scribe Method	Mechanical
INTERCONNECTIONS	
Die Mounting Material	Silver Filled Epoxy
Wire Material	Aluminum
Wire Diameter	0.0014
Longest Lead Length	0.043
Wire Bond Type(s) Post	Ultrasonic (See Figure A44)
Die	Ultrasonic (See Figure A43)
Interconnection Photograph	(See Figure A42)

DESCRIPTION	DETAIL
PACKAGE	
Lead/Lead Frame Material	Kovar
Lead/Lead Frame Finish - Internal	Aluminum
Lead/Lead Frame Finish - External	Nickel Plate
Lead/Lead Frame Finish - Feed Thru	Tungsten
Header/Case Material	Ceramic
Cap/Lid Material	Nickel Plated Kovar
Case Seal Material/Method	Solder
Lead Seal Material/Method	Ceramic
Cavity Size	0.163 Dia.
Package Photograph	(See Figure A41)

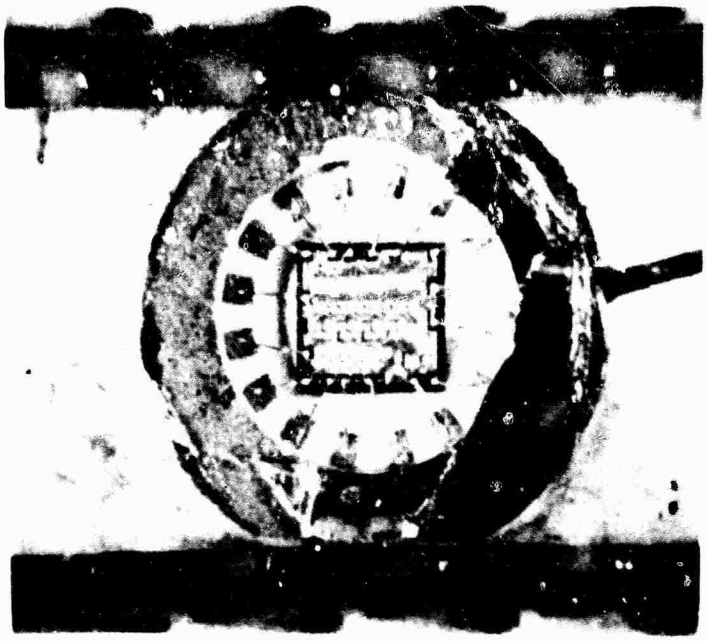
Note:

1. All dimensions are in inches.



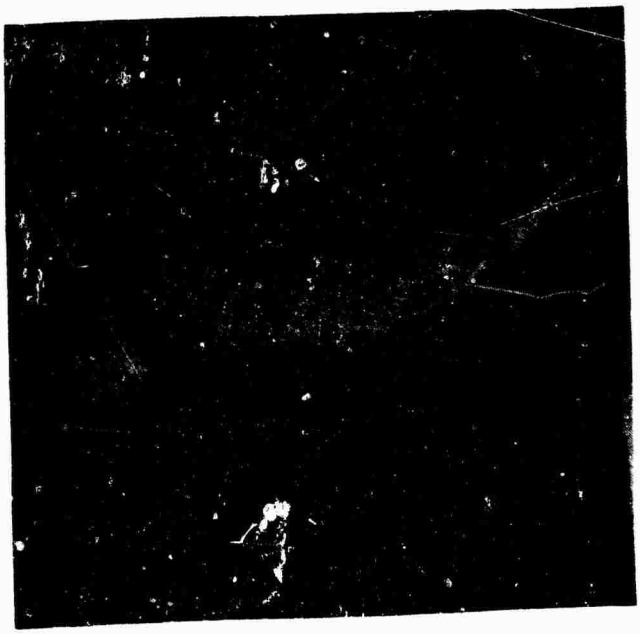
4X S/N C154

FIGURE A41 - PACKAGE PHOTOGRAPH



10X S/N C154

FIGURE A42 - INTERCONNECTION PHOTOGRAPH



E25X
(SEM-1.2KV)

S/N C154

FIGURE A43 - WIRE BOND AT DIE

250X
(SEM-1.2KV)

S/N C154

FIGURE A44 - WIRE BOND AT LEAD FRAME

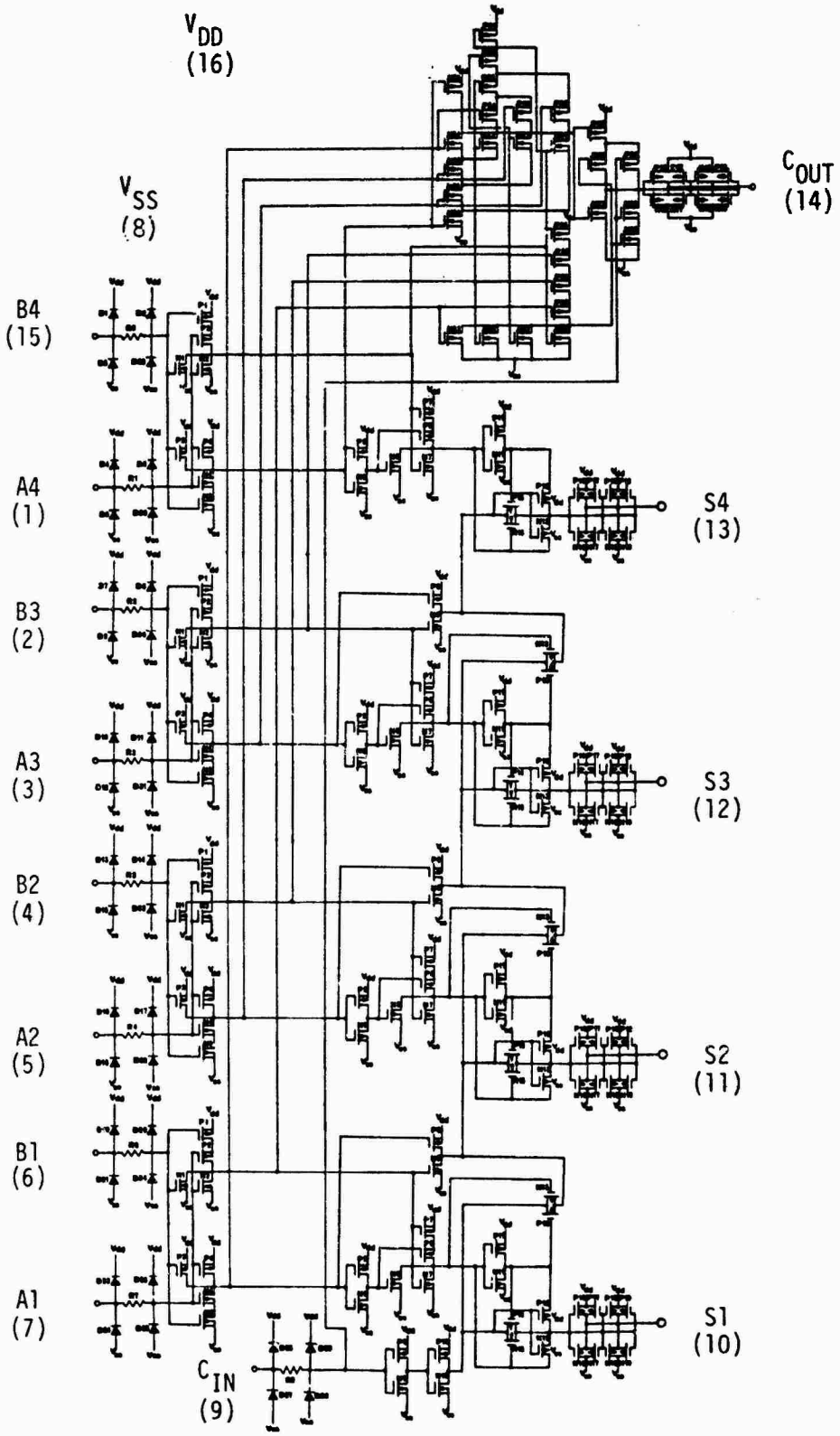


FIGURE A45. SCHEMATIC DIAGRAM

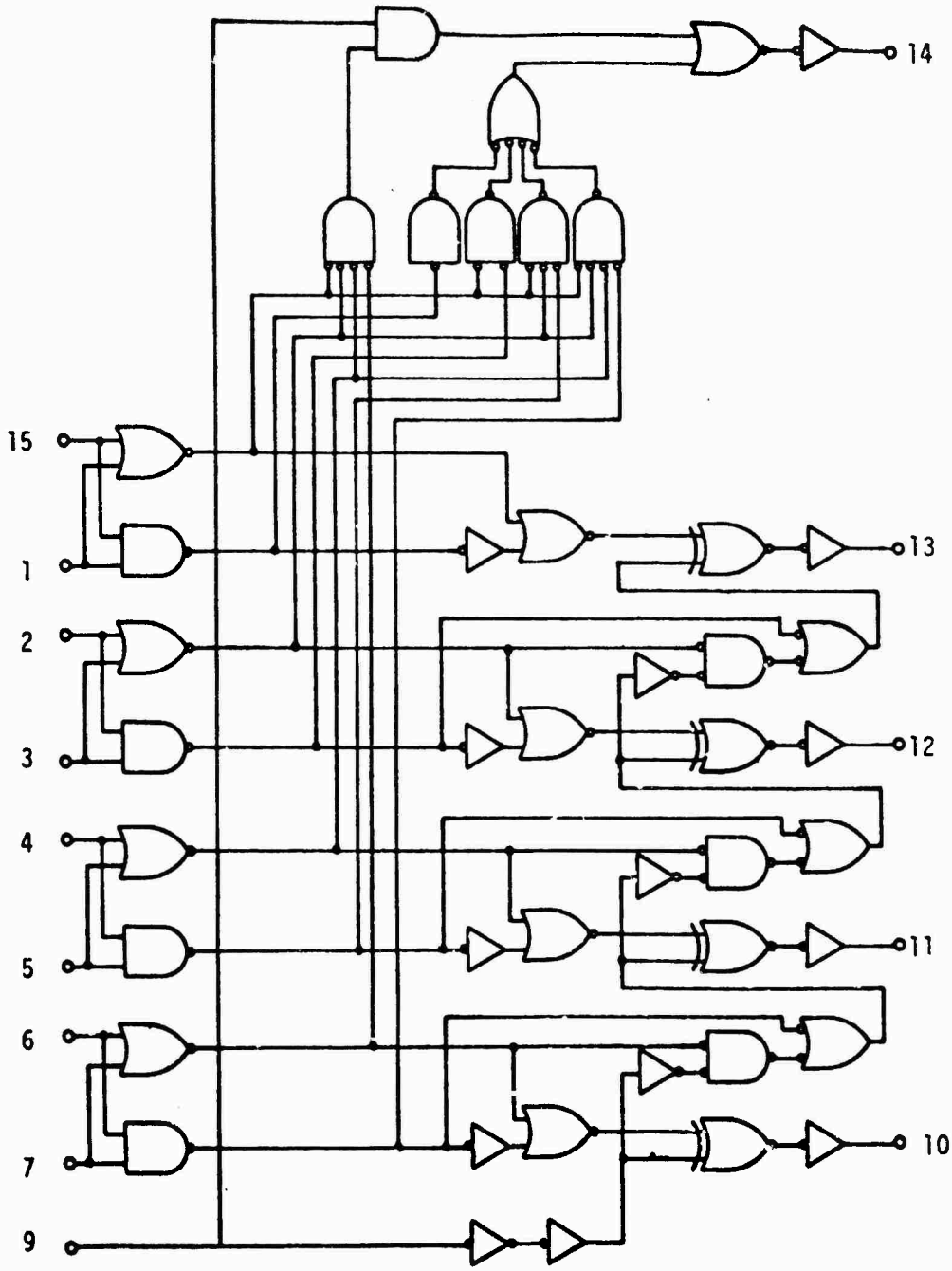
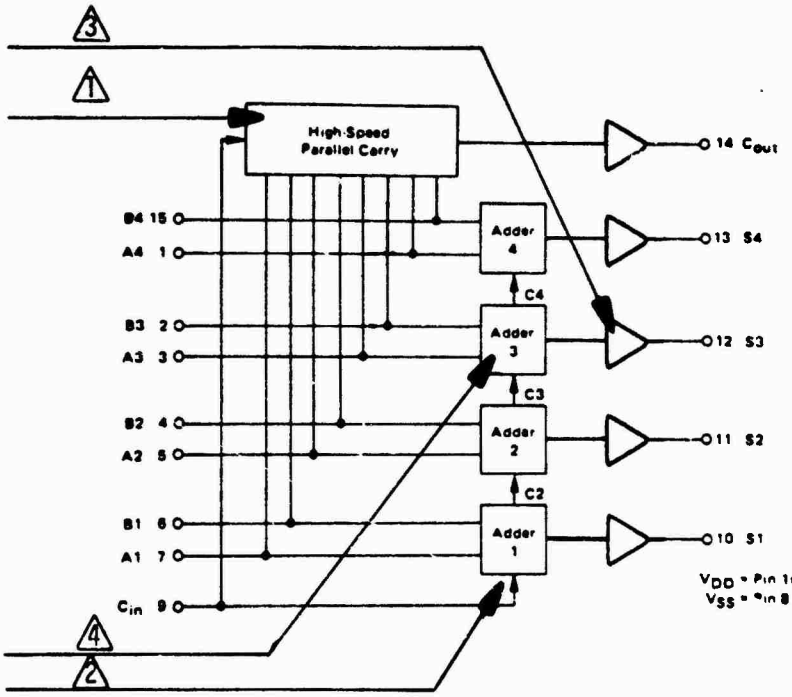


FIGURE A46. LOGIC DIAGRAM



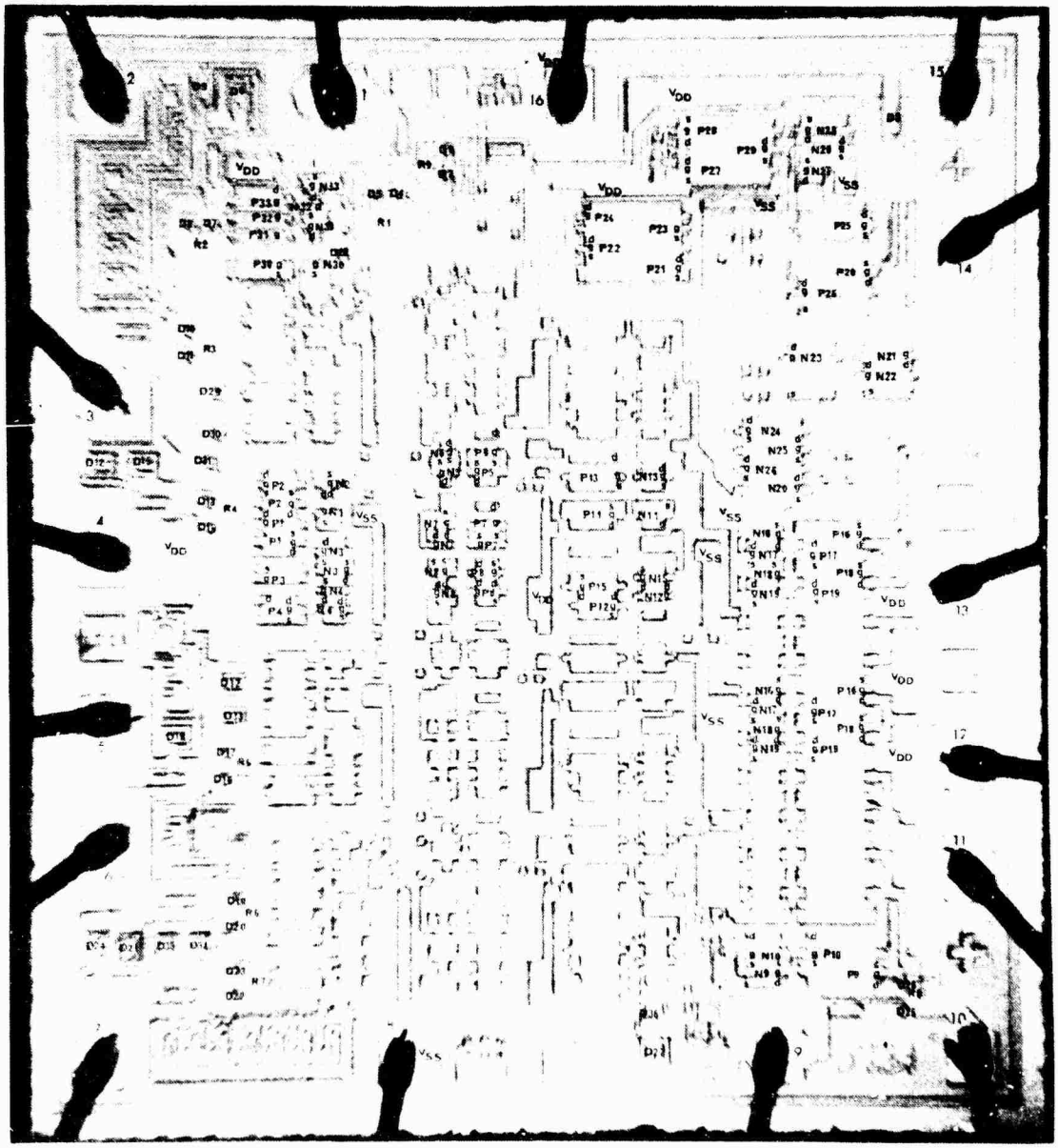
1 PARALLEL CARRY CIRCUIT - FIGURE A49 AND FIGURE A50

2 CARRY INPUT CIRCUIT - FIGURE A51 AND FIGURE A52

3 OUTPUT CIRCUIT - FIGURE A53 AND FIGURE A54

4 ADDER 3 CIRCUIT - FIGURE A55 AND FIGURE A56

FIGURE A47 - FUNCTIONAL BLOCK DIAGRAM



74X

S/N C154

FIGURE A48 - DIE PHOTOGRAPH

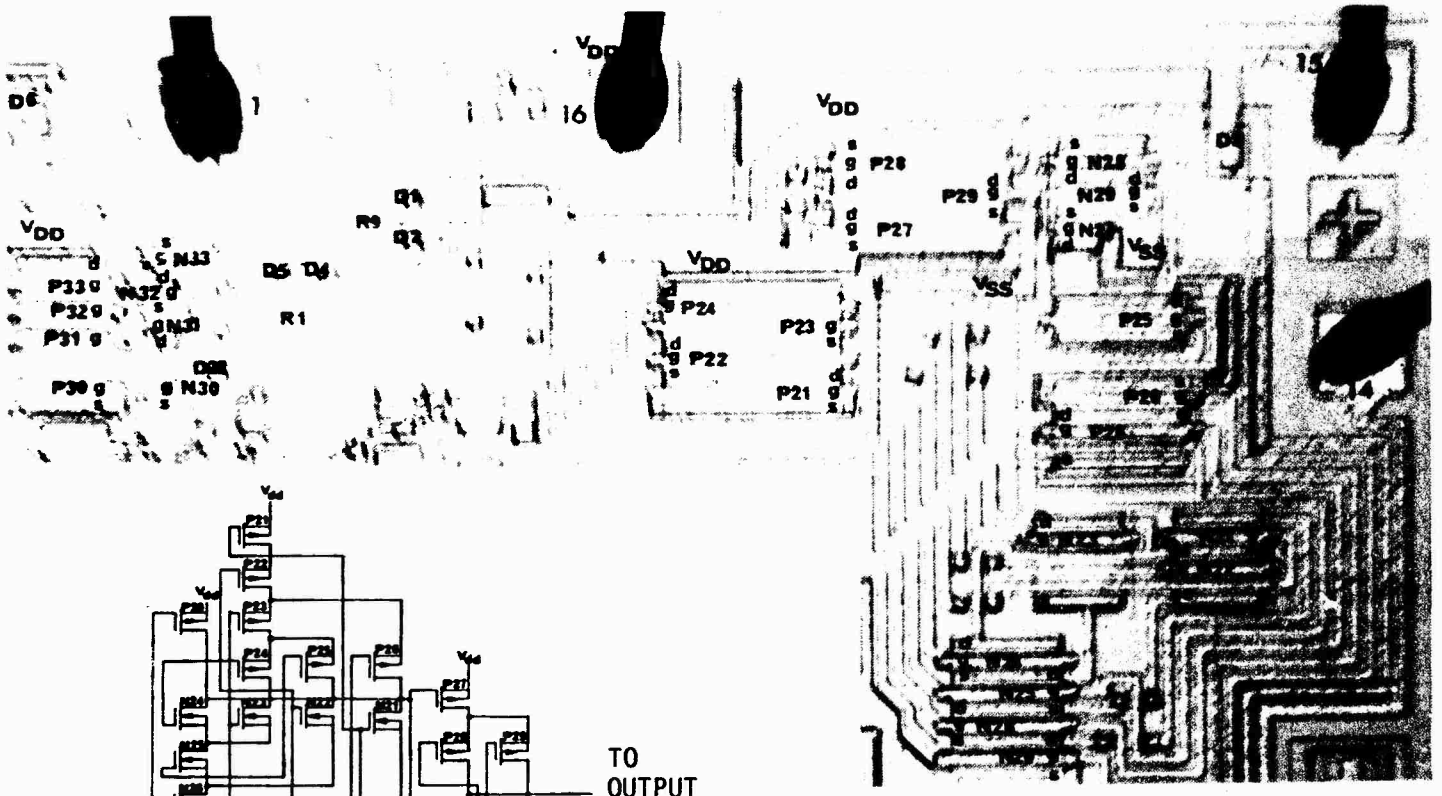


FIGURE A 49 - PARALLEL CARRY CIRCUIT

FIGURE A 50 - SCHEMATIC DIAGRAM OF PARALLEL CARRY CIRCUIT

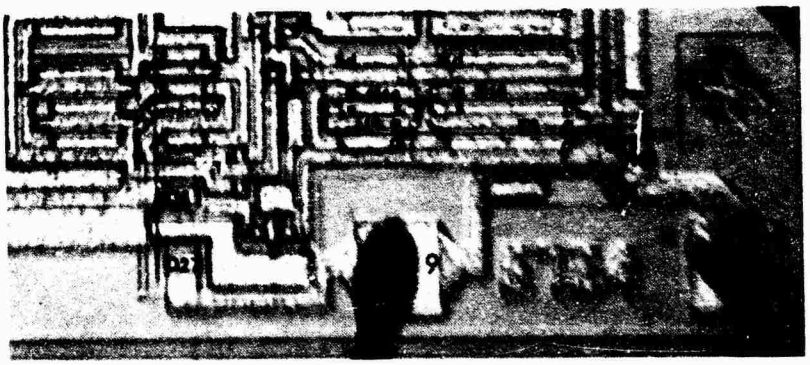


FIGURE A51- CARRY INPUT CIRCUIT

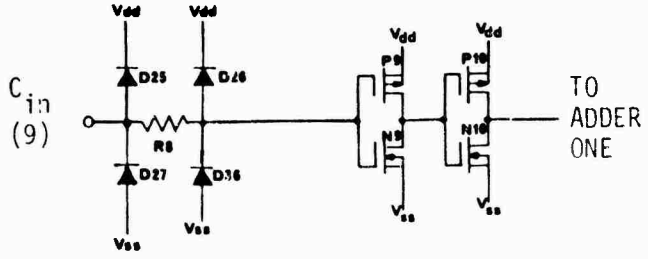


FIGURE A52- SCHEMATIC DIAGRAM OF CARRY INPUT CIRCUIT

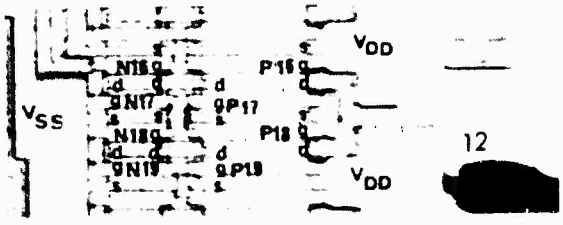


FIGURE A53- TYPICAL OUTPUT CIRCUIT

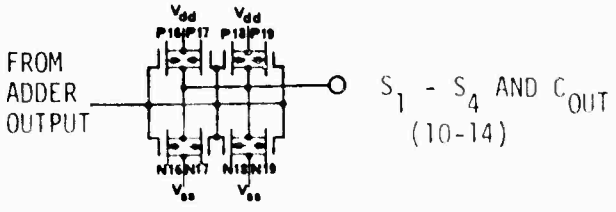


FIGURE A54- SCHEMATIC DIAGRAM OF OUTPUT CIRCUIT

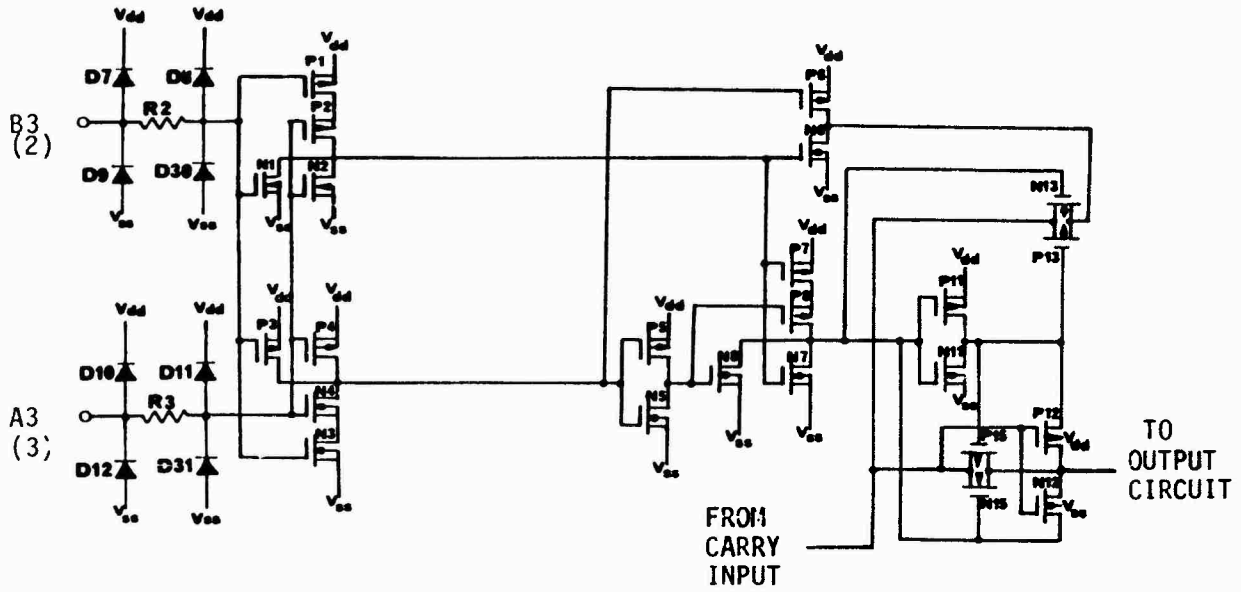


FIGURE A55 - SCHEMATIC DIAGRAM OF ADDER CIRCUIT

FIGURE A56 - ADDER THREE CIRCUIT

APPENDIX A7

CONSTRUCTION ANALYSIS

M38510/05601BEB

MANUFACTURER A

DECADE COUNTER/DIVIDER

DATE CODE 7628

MICROCIRCUIT CONSTRUCTION INFORMATION
BASELINE ANALYSIS

S/N B53 DATE CODE 7628 DATE: 2/8/77

PART NAME: DECADE COUNTER/DIVIDER

MANUFACTURER'S PART NO: MC14017BAL MANUFACTURER: A

GENERIC PART NO: 4017 PACKAGE TYPE: 16 PIN DIP

MILITARY SPECIFICATION TYPE: M38510-05601BEB

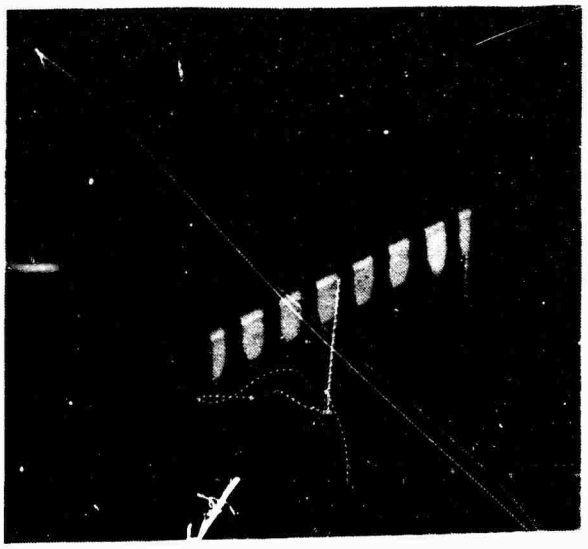
DESCRIPTION	DETAIL
DIE	
Passivation Type	Silicon Dioxide
Glassivation Type	Vapor
Basic Die Construction	Planar
Die Dimensions	0.080 x 0.080
Metallization Type	Aluminum
Metallization Thickness	———
Number of Metallization Layers	One
Metallization Interlayer Insulation Type	None
Bonding Pad-Size	0.0048 x 0.0048
Die Photograph	(See Figure A63)
Scribe Method	Laser
INTERCONNECTIONS	
Die Mounting Material	Gold Silicone Eutectic
Wire Material	Aluminum
Wire Diameter	0.001
Longest Lead Length	0.071
Wire Bond Type(s) Post	Ultrasonic (See Figure A60)
Die	Ultrasonic (See Figure A59)
Interconnection Photograph	(See Figure A58)

DESCRIPTION	DETAIL
PACKAGE	
Lead/Lead Frame Material	Alloy 42
Lead/Lead Frame Finish - Internal	Aluminum
Lead/Lead Frame Finish - External	Tin Lead Plate
Lead/Lead Frame Finish - Feed Thru	None
Header/Case Material	Ceramic (Al_2O_3)
Cap/Lid Material	Ceramic (Al_2O_3)
Case Seal Material/Method	Glass Frit
Lead Seal Material/Method	Glass Frit
Cavity Size	0.25 x 0.162
Package Photograph	(See Figure A57)

Note:

1. All dimensions are in inches.

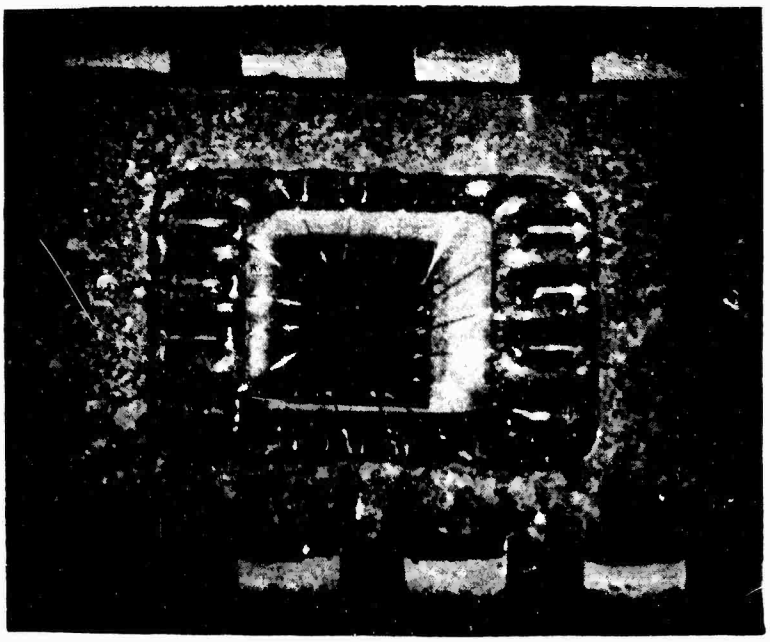
3X



S/N B53

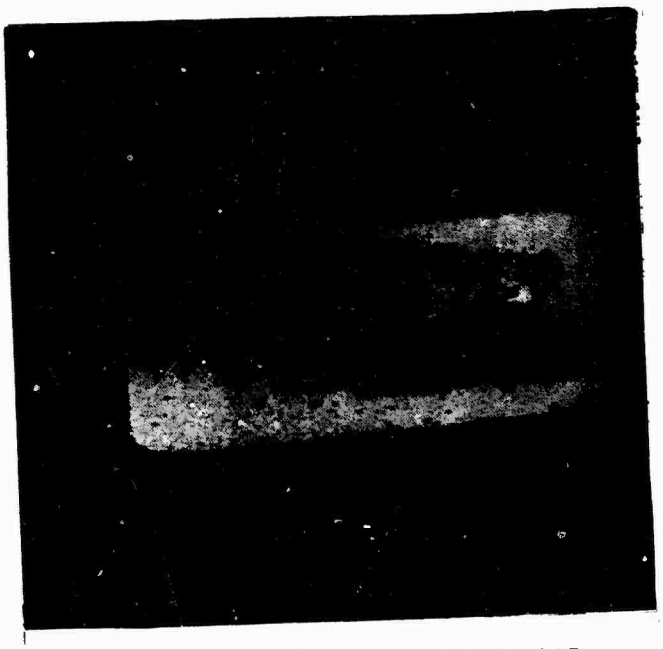
FIGURE A57 - PACKAGE PHOTOGRAPH

10X



S/N B51

FIGURE A58 - INTERCONNECTION PHOTOGRAPH



620X
(SEM-1.2KV)

S/N B53

FIGURE A59 - WIRE BOND AT DIE

440X
(SEM-1.2KV)

S/N B51

FIGURE A60 - WIRE BOND AT LEAD FRAME

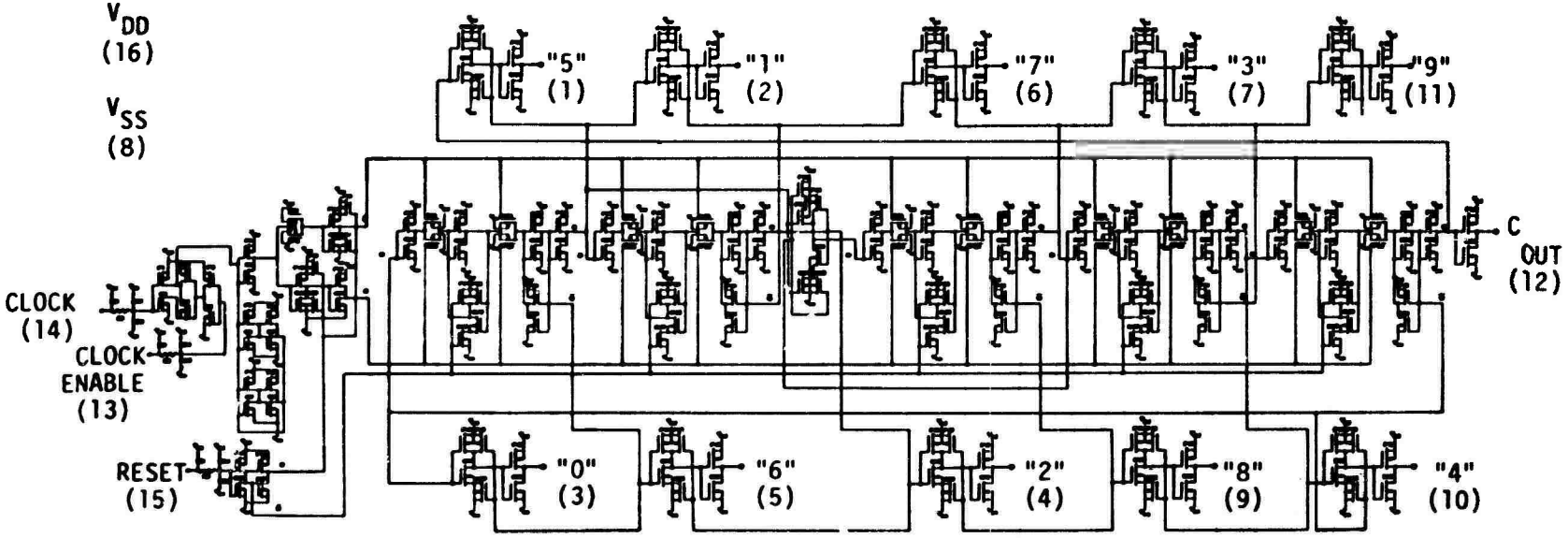
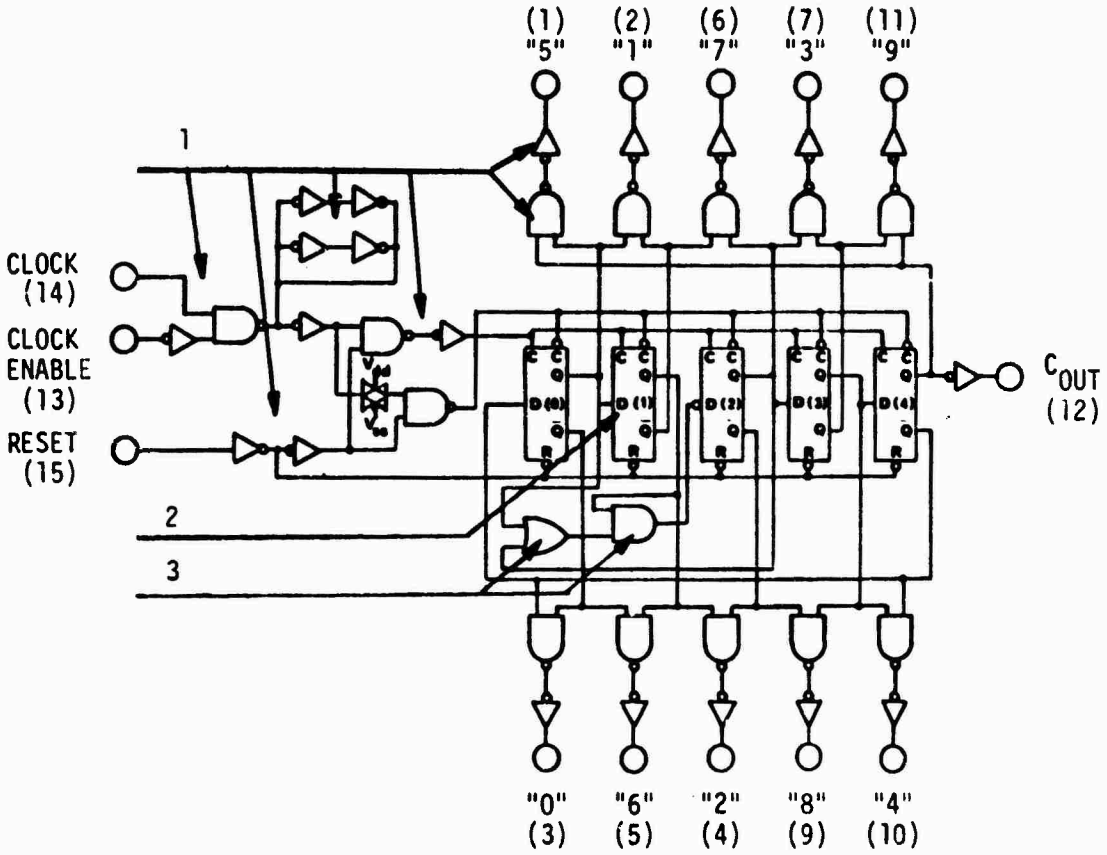


FIGURE A61. SCHEMATIC DIAGRAM

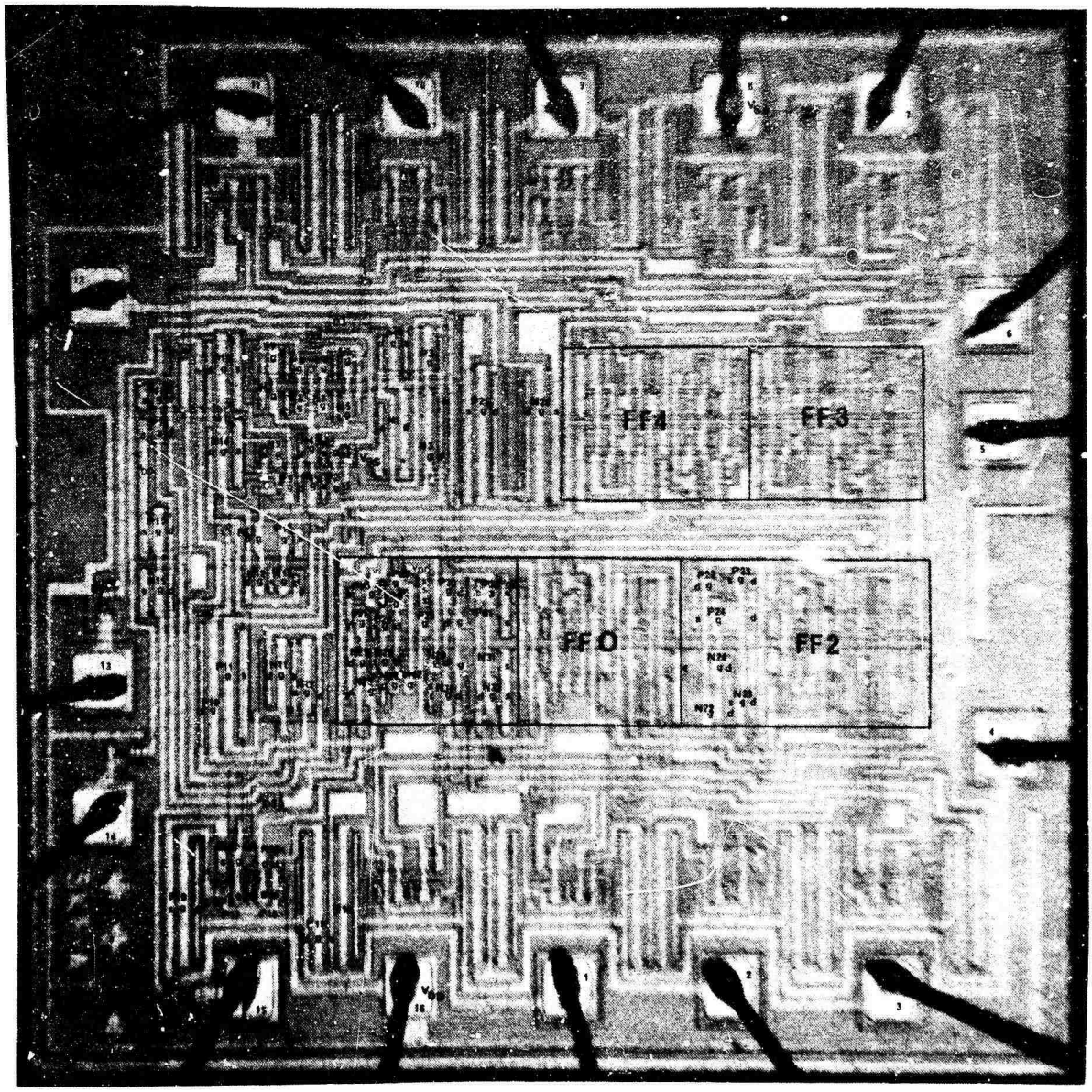


1 INPUT CIRCUIT AND A TYPICAL OUTPUT CIRCUIT - FIGURE A64 AND FIGURE A65

2 A TYPICAL FLIP/FLOP CIRCUIT - FIGURE A66 AND FIGURE A67

3 F/F-2 INPUT GATING CIRCUIT - FIGURE A68 AND FIGURE A69

FIGURE A62. FUNCTIONAL BLOCK DIAGRAM



83X S/N B53

FIGURE A63 - DIE PHOTOGRAPH

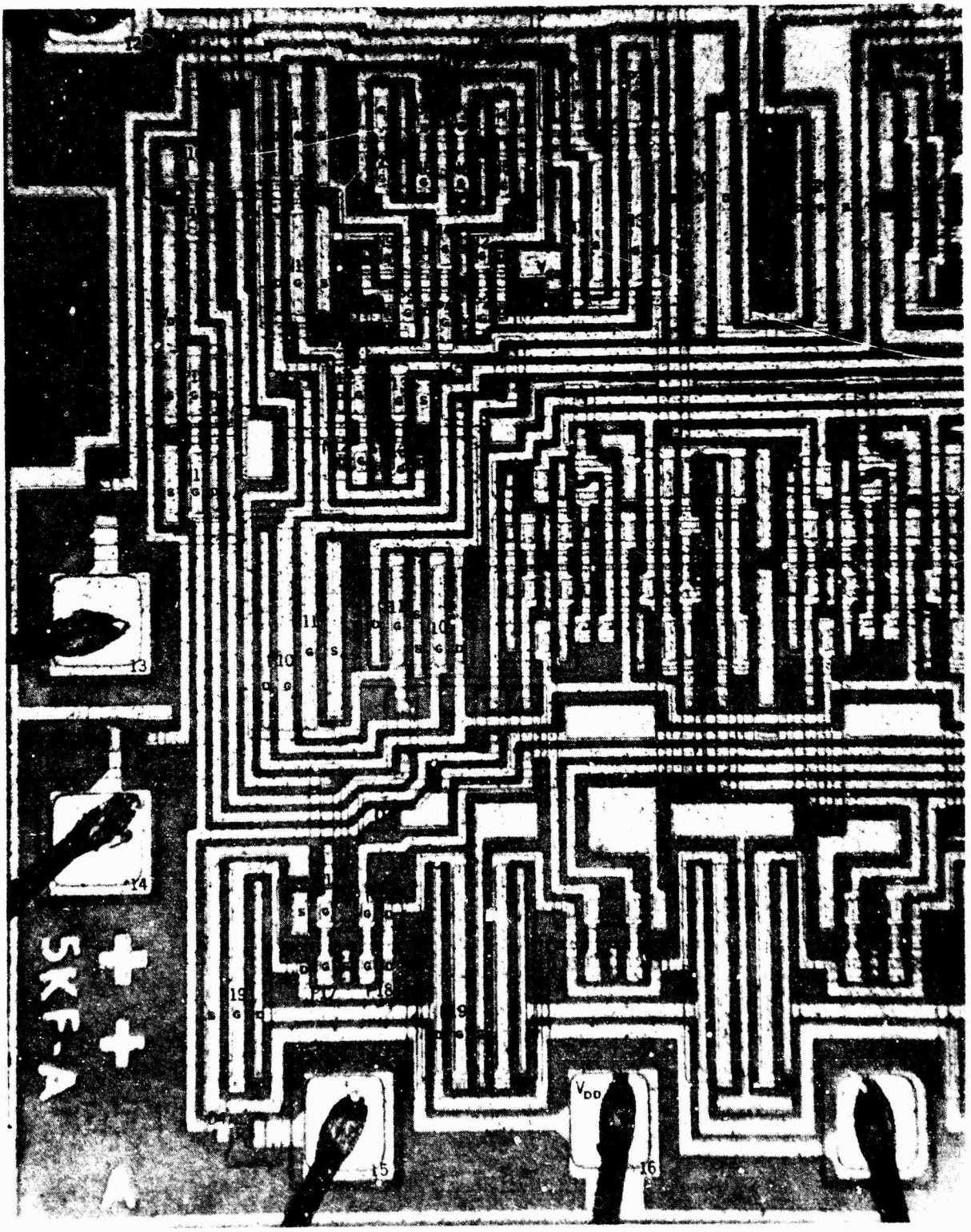


FIGURE A64. INPUT CIRCUIT AND A TYPICAL OUTPUT CIRCUIT

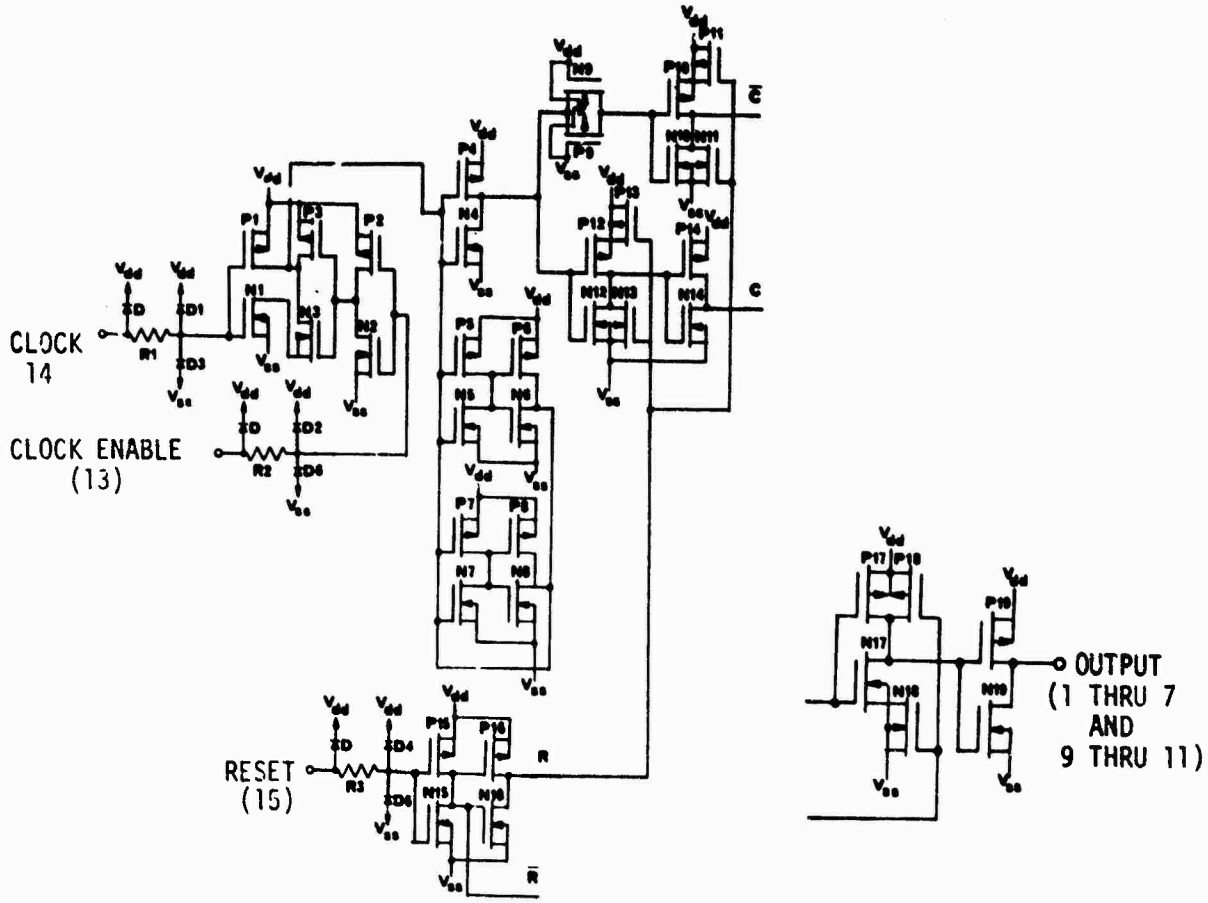


FIGURE A65- SCHEMATIC DIAGRAM OF DEVICE INPUT CIRCUIT AND A TYPICAL OUTPUT CIRCUIT

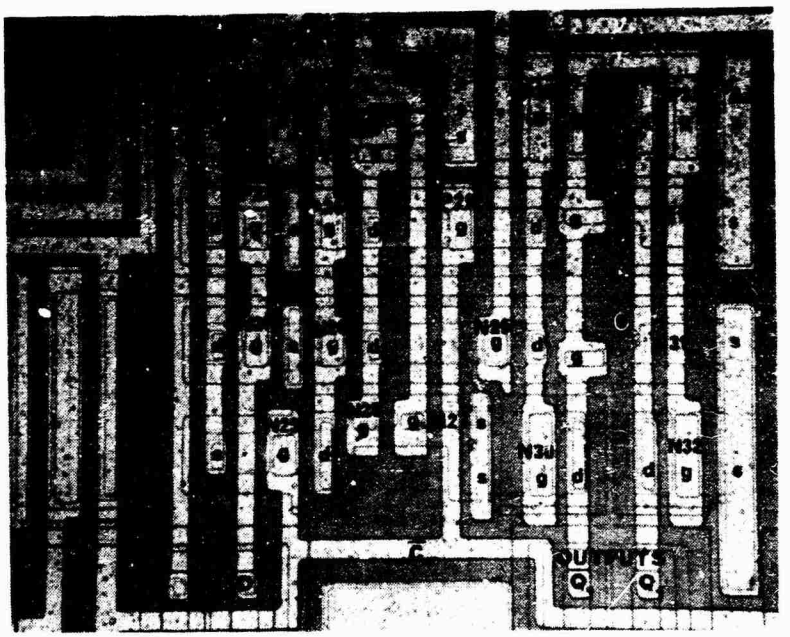


FIGURE A66 - A TYPICAL FLIP/FLOP

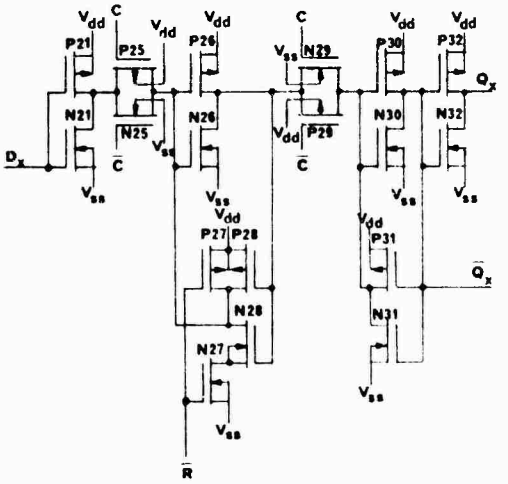


FIGURE A67 - SCHEMATIC DIAGRAM OF A TYPICAL FLIP/FLOP CIRCUIT

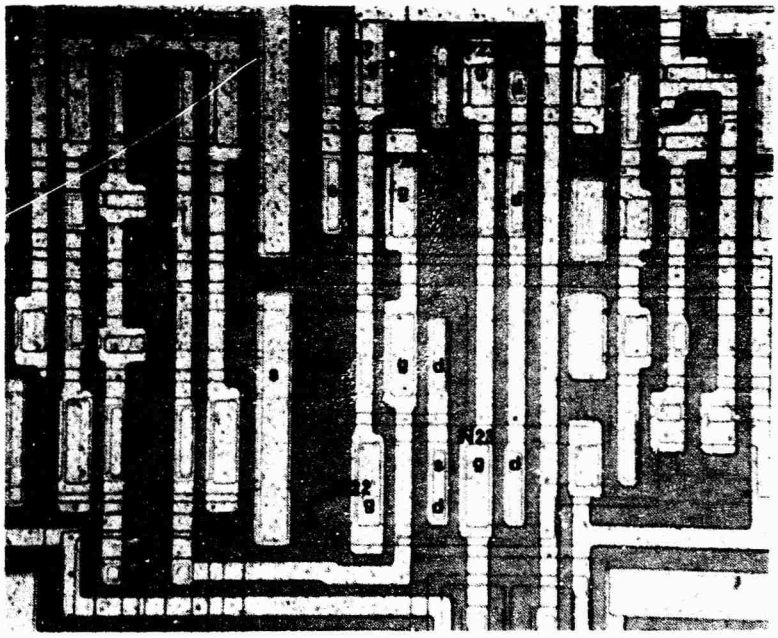


FIGURE A68 - F/F2 INPUT GATING CIRCUIT

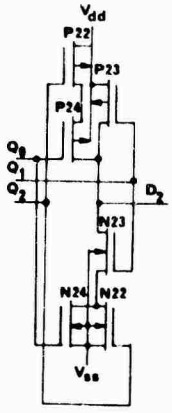


FIGURE A69 - SCHEMATIC DIAGRAM OF F/F2 INPUT GATING CIRCUIT

APPENDIX A8

CONSTRUCTION ANALYSIS

M38510/05601BEB

MANUFACTURER D

DECADE COUNTER/DIVIDER

DATE CODE 7703

MICROCIRCUIT CONSTRUCTION INFORMATION
BASELINE ANALYSIS

S/N A341 DATE CODE 7703 DATE: 7/20/77

PART NAME: DECADE COUNTER/DIVIDER

MANUFACTURER'S PART NO: 85746 MANUFACTURER: D

GENERIC PART NO: 4017 PACKAGE TYPE: 16 PIN DIP

MILITARY SPECIFICATION TYPE: M38510/05601BEB

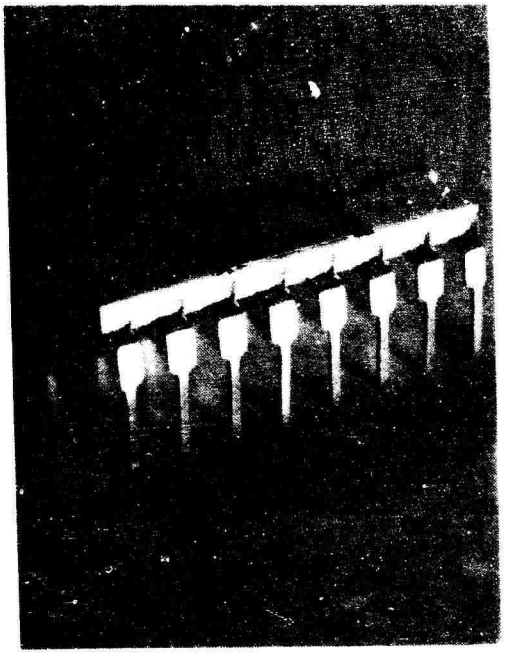
DESCRIPTION	DETAIL
DIE	
Passivation Type	Silicon Dioxide
Glassivation Type	Silicon Dioxide
Basic Die Construction	Planar
Die Dimensions	0.075 x 0.078
Metallization Type	Aluminum
Metallization Thickness	
Number of Metallization Layers	One
Metallization Interlayer Insulation Type	None
Bonding Pad Size	0.0038 x 0.0038
Die Photograph	(See Figure A76)
Scribe Method	Mechanical
INTERCONNECTIONS	
Die Mounting Material	Silver Filled Epoxy
Wire Material	Aluminum
Wire Diameter	0.0013
Longest Lead Length	0.074
Wire Bond Type(s) Post	Ultrasonic (See Figure A73)
Die	Ultrasonic (See Figure A72)
Interconnection Photograph	(See Figure A71)

DESCRIPTION	DETAIL
PACKAGE	
Lead/Lead Frame Material	Kovar
Lead/Lead Frame Finish - Internal	Aluminum
Lead/Lead Frame Finish - External	Nickel Plate
Lead/Lead Frame Finish - Feed Thru	Tungsten
Header/Case Material	Ceramic
Cap/Lid Material	Nickel Plated Kovar
Case Seal Material/Method	Solder
Lead Seal Material/Method	Ceramic
Cavity Size	0.228 x 0.178
Package Photograph	(See Figure A70)

Note:

1. All dimensions are in inches.

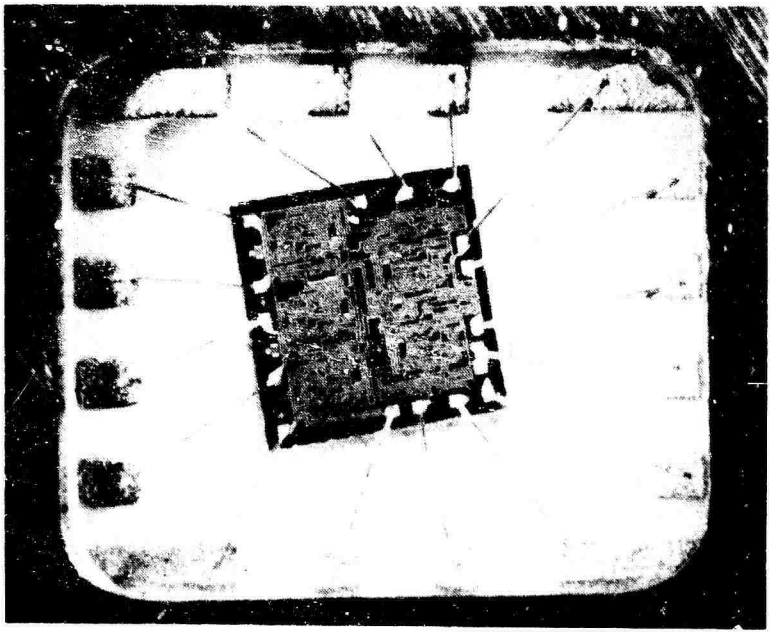
3X



S/N A341

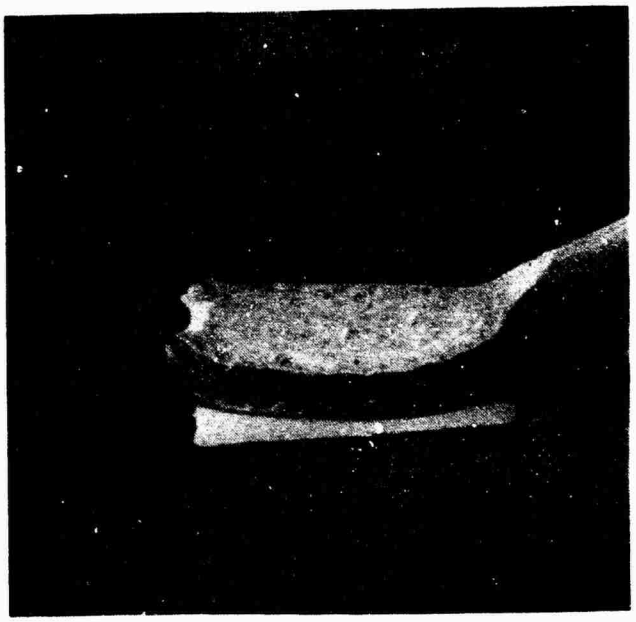
FIGURE A70 - PACKAGE PHOTOGRAPH

18X



S/N A341

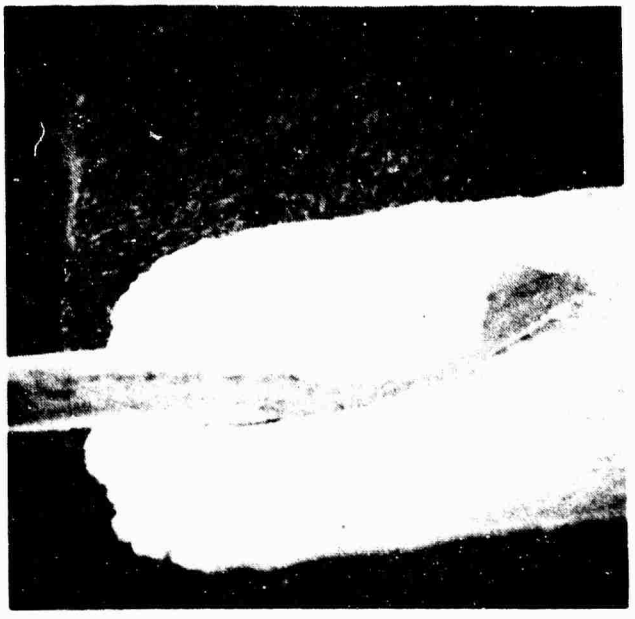
FIGURE A71 - INTERCONNECTION PHOTOGRAPH



430X
(SEM-1.2KV)

S/N A341

FIGURE A72 - WIRE BOND AT DIE



250X
(SEM-1.2KV)

S/N A341

FIGURE A73 - WIRE BOND AT LEAD FRAME

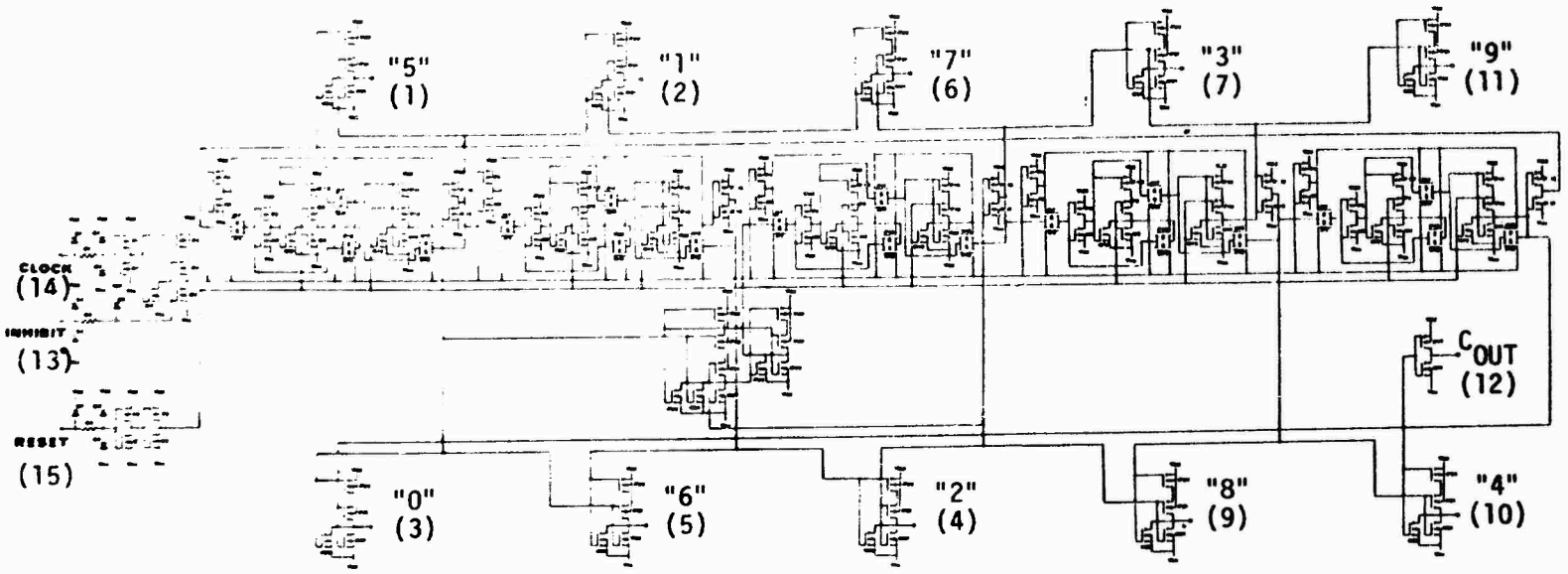
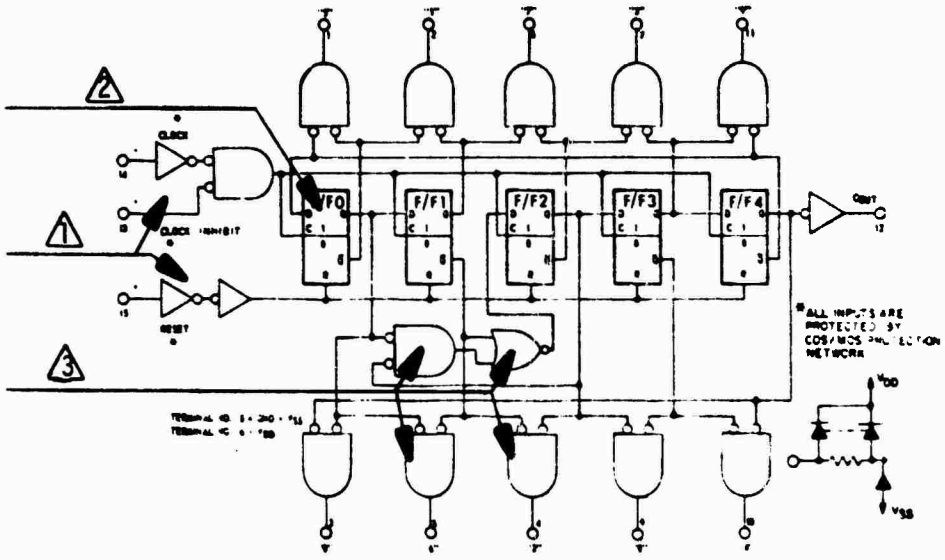
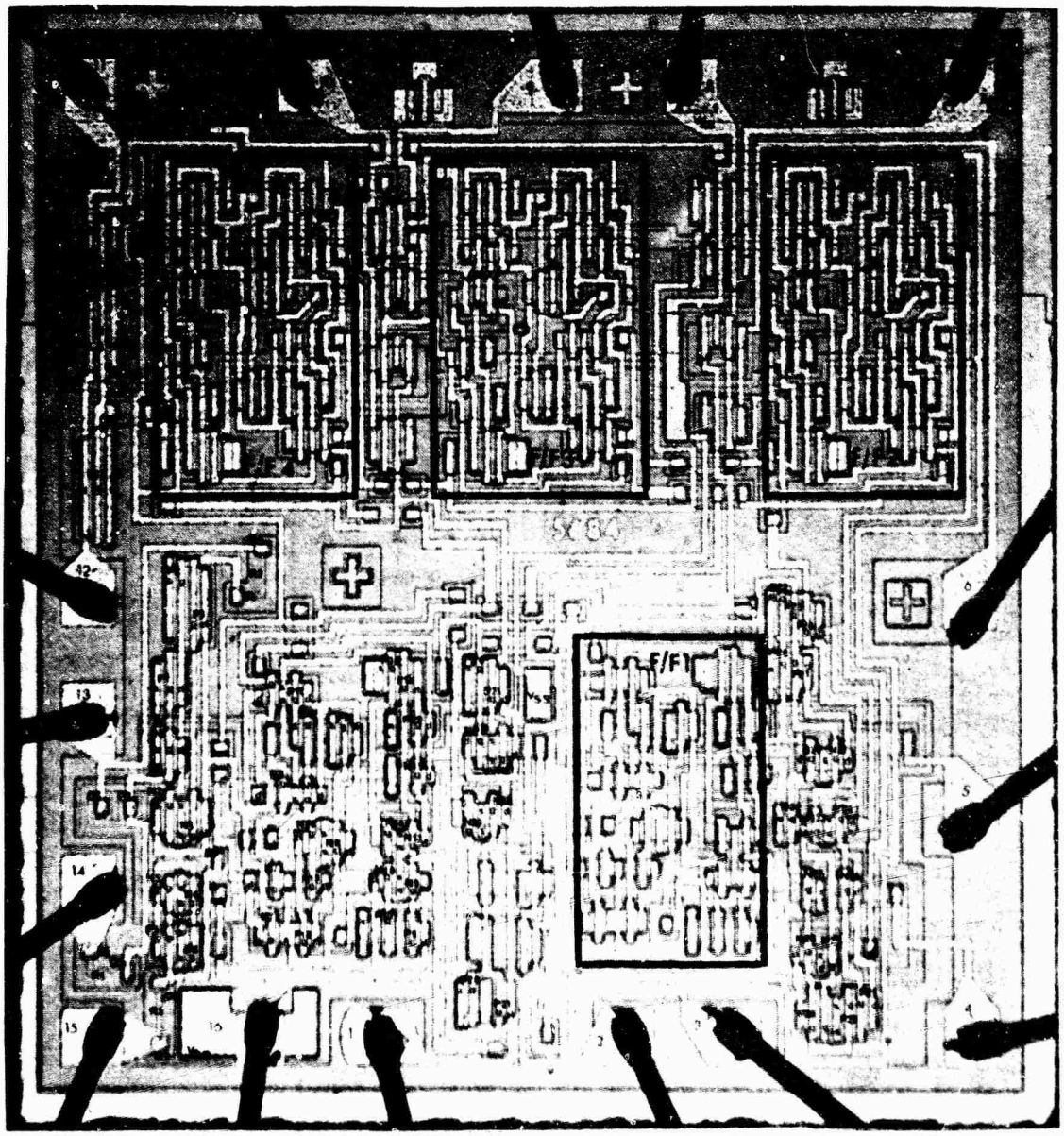


FIGURE A74. SCHEMATIC DIAGRAM



1. INPUT CIRCUIT - FIGURE A77 AND FIGURE A78
2. FLIP/FLOP CIRCUIT - FIGURE A79 AND FIGURE A80
3. F/F2 INPUT GATING CIRCUIT AND OUTPUT CIRCUITS - FIGURE A81 AND FIGURE A82

FIGURE A75 - FUNCTIONAL BLOCK DIAGRAM



85X

S/N A341

FIGURE A76 - DIE PHOTOGRAPH

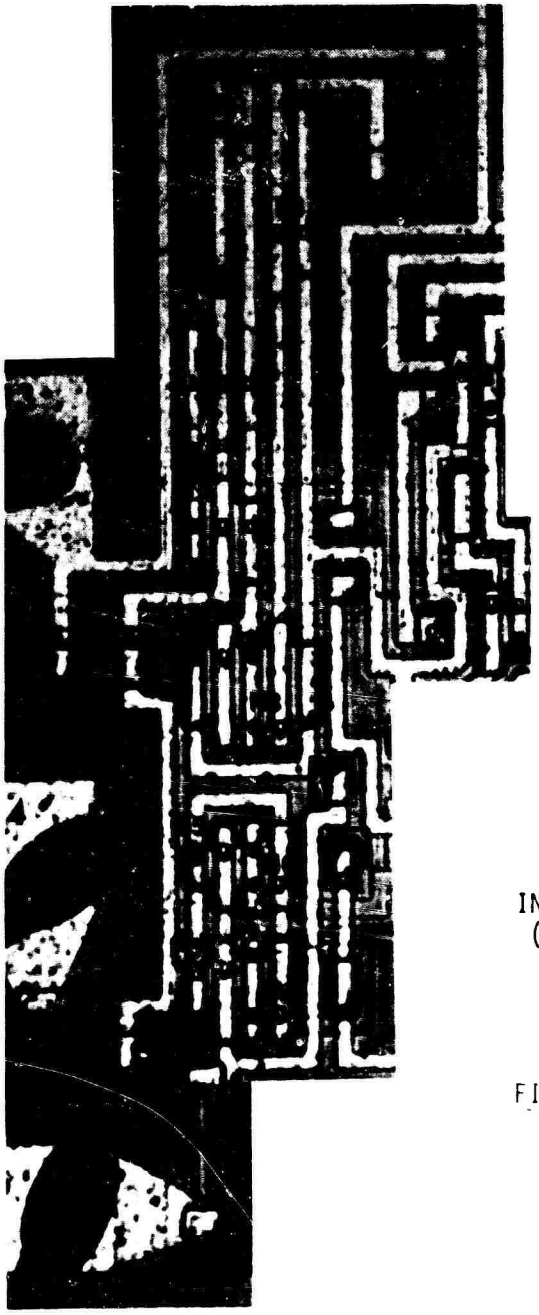


FIGURE A77. INPUT CIRCUIT

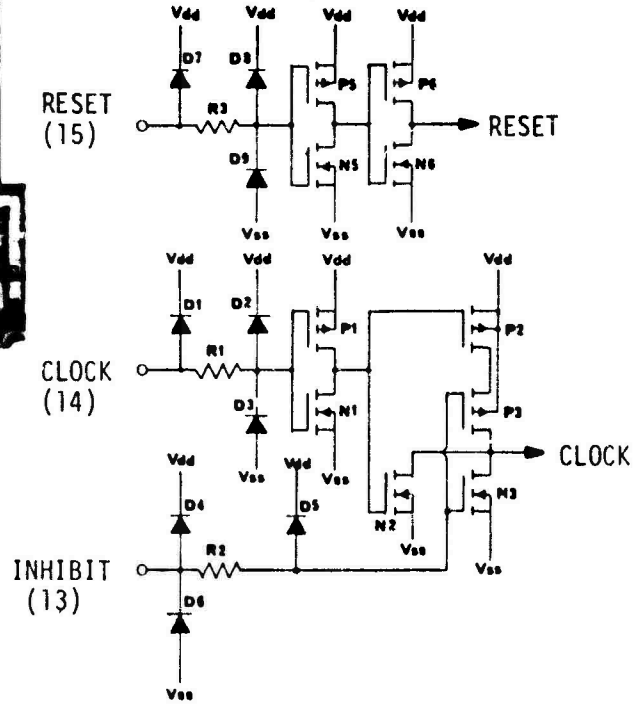


FIGURE A78. SCHEMATIC DIAGRAM OF INPUT CIRCUIT

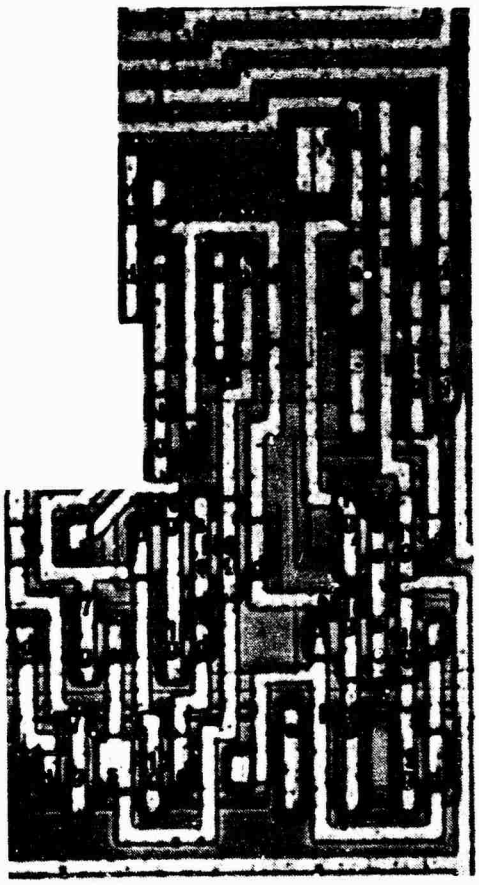


FIGURE A79. TYPICAL FLIP/FLOP CIRCUIT

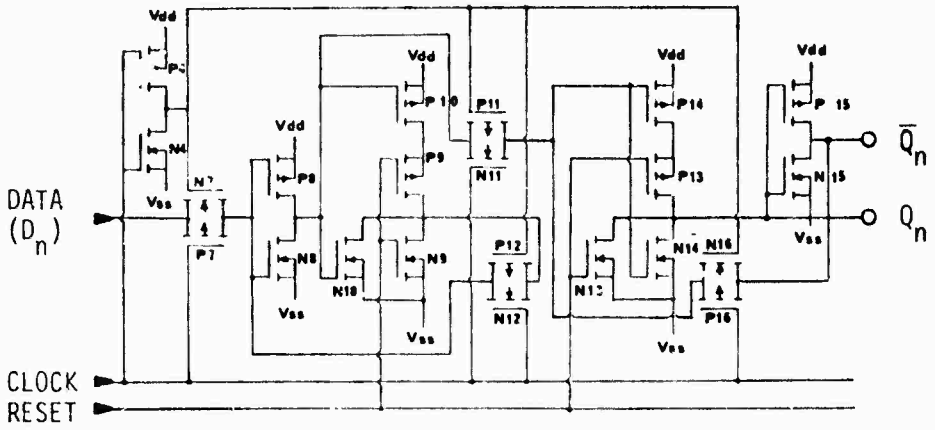


FIGURE A80. SCHEMATIC DIAGRAM OF FLIP/FLOP CIRCUIT

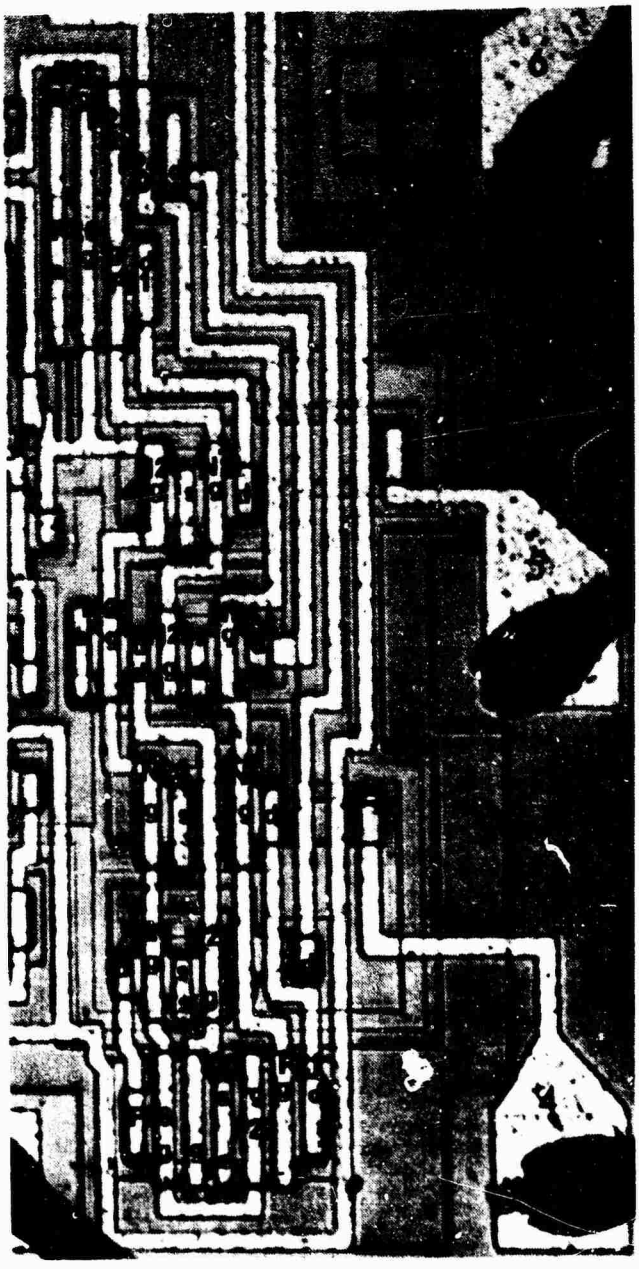


FIGURE A81. F/F2 INPUT GATING CIRCUIT AND TWO TYPICAL OUTPUT CIRCUITS

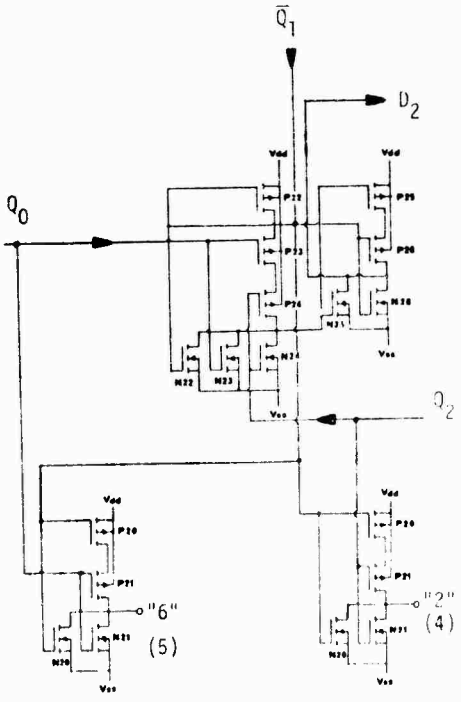


FIGURE A82. SCHEMATIC DIAGRAM OF F/F2 INPUT GATING CIRCUIT AND OF TWO TYPICAL OUTPUT CIRCUITS

APPENDIX B

ELECTRICAL TEST CONDITIONS

TABLE OF CONTENTS

TABLE B1. D.C. TEST LIST FOR 4001B

	INITIAL/FINAL TEST #'S			INTERIM TEST #'S
PARAMETER	25°C	+125°C	-55°C	
VIC (POS)	1,2,3,4,5,6,7,8			1,2,3,4,5,6,7,8
VIC (NEG)	9,10,11,12,13,14,15,16			9,10,11,12,13,14,15,16
ISS	17,18,19	17,18,19		17,18,19
VOL 1	20,21,22,23,24,25,26,27	20,21,22,23,24,25,26,27	20,21,22,23,24,25,26,27	20,21,22,23,24,25.26.27
VOL 2	28,29,30,21,32,33,34,35	28,29,30,31,32,33,34,35	28,29,30,31,32,33,34,35	28,29,30,31,32,33,34,35
VOL 3	36,37,38,39,40,41,42,43	36,37,38,39,40,41,42,43	36,37,38,39,40,41,42,43	36,37,38,39,40, 41,42,43
VOH 1	44,45,46,47	44,45,46,47	44,45,46,47	44,45,46,47
VOH 2	48,49,50,51	48,49,50,51	48,49,50,51	48,49,50,51
VOH 3	52,53,54,55	52,53,54,54	52,53,54,55	52,53,54,55
IIL 1	56			56
IIL 2		57,58,59,60,61,62,63,64		
IIH 1	65			65
IIH 2		66,67,68,69,70,71,72,73		

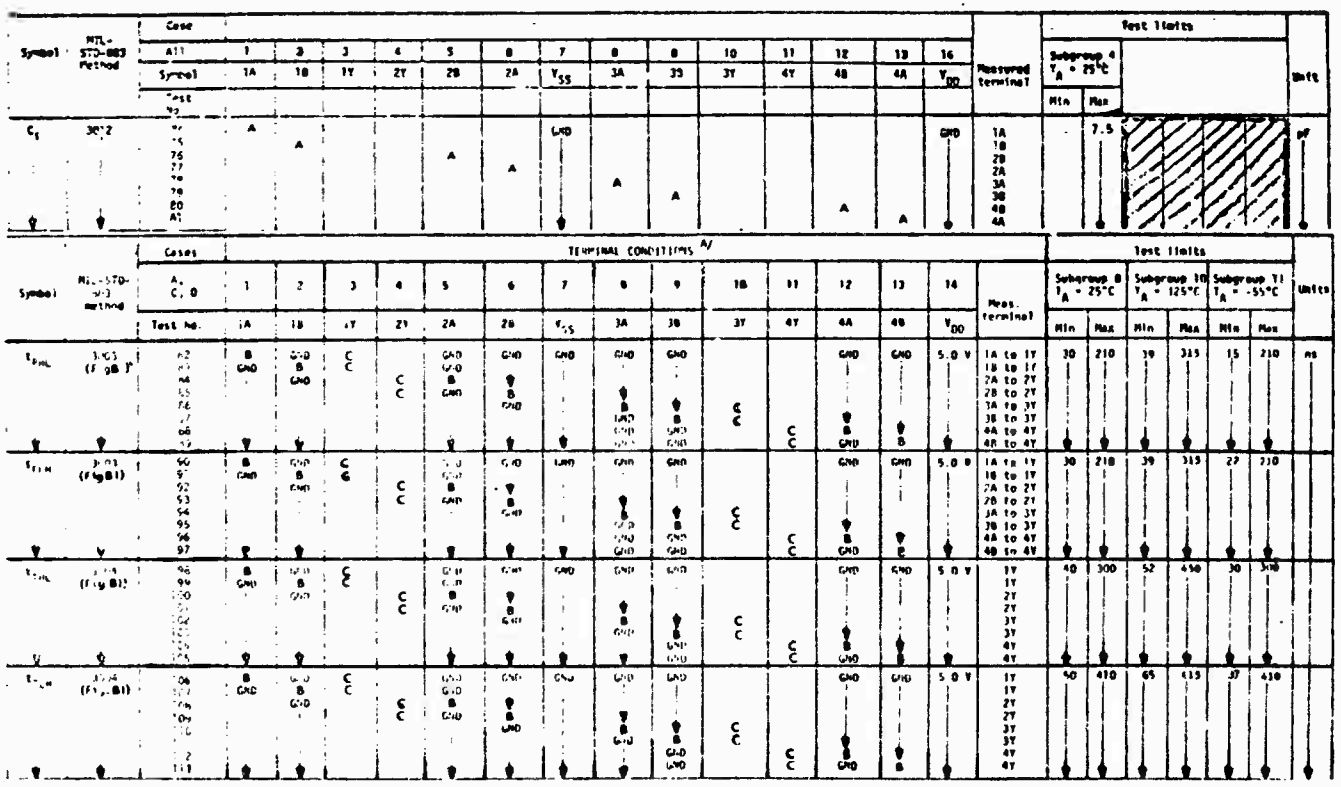
TABLE B2. A.C. TEST LIST FOR 4001B

PARAMETER	DYNAMIC TEST
C_I	74-81
t PHL	82-89
t PLH	90-97
t THL	98-105
t TLH	105-113

TABLE B3. TEST SPECIFICATIONS FOR 4001B

SYMBOL	MIL-STD-883 METHOD	CASE OUTLINE	TERMINAL CONDITIONS (PINS NOT DESIGNATED ARE OPEN)																	TEST LIMITS						
			ALL	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16		SUB GP 1 T_A=25°C		SUB GP 2 T_A=125°C		SUB GP 3 T_A=-55°C		
			SEE BELOW	1A	1B	1Y	2Y	2A	2B	VSS	3A	3B	3Y	4Y	4A	4B	VDD			MIN	MAX	MIN	MAX	MIN	MAX	UNIT
			TEST NO.																							
I_{IC} (POS)			1 2 3 4 5 6 7 8	1ma	1ma			1ma	1ma		1ma	1ma			1ma	1ma	GND			1A 1B 2A 2B 3A 3B 4A 4B		1.5					Vdc
I_{IC} (NEG)			9 10 11 12 13 14 15 16	-1ma	1ma			-1ma	-1ma	GND V	-1ma	-1ma			-1ma	-1ma				1A 1B 2A 2B 3A 3B 4A 4B		-6.0					Vdc
I_{SS}	3005	17 18 19	15.0V GND GND	GND 15.0V GND				GND 15.0V GND	15.0V GND GND	GND	15.0V GND GND	GND 15.0V GND			GND 15.0V GND	15.0V GND GND	15.0V			VSS		-1.0		-30.0			μA
V_{OL1}	3006	20 21 22 23 24 25 26 27	VIH1 GND GND GND	GND VIH1 GND GND	IOL1 IOL1		IOL1 IOL1	GND GND VIH1 GND GND GND	GND VIH1 GND GND GND GND	GND GND GND	GND VIH1 GND GND GND	GND VIH1 GND GND	IOL1 IOL1	IOL1 IOL1	GND VIH1 GND	GND GND VIH1	5.0V 5.0V 5.0V			1Y 1Y 2Y 2Y 3Y 3Y 4Y 4Y		0.4		0.4 0.4 0.4		0.4 0.4 0.4	Vdc
V_{OL2}	3006	28 29 30 31 32 33 34 35	VIH1 GND	GND VIH1 GND				GND GND VIH1 GND	GND VIH1 GND	GND	GND VIH1 GND	GND VIH1 GND GND			GND VIH1 GND	GND VIH1	5.0V			1Y 1Y 2Y 2Y 3Y 3Y 4Y 4Y		.05		.05		.05	Vdc
V_{OL3}	3006	36 37 38 39 40 41 42 43	VIH2 GND	GND VIH2 GND				GND GND VIH2 GND	GND VIH2 GND	GND	GND VIH2 GND	GND VIH2 GND			GND VIH2 GND	GND VIH2	15.0V			1Y 1Y 2Y 2Y 3Y 3Y 4Y 4Y		1.5		1.5		1.5	Vdc
V_{OH1}	3007	44 45 46 47	VIL1 5.0V	VIL1 5.0V	IOH1		IOH1	5.0V VIL1 5.0V	5.0V VIL1 5.0V	GND	5.0V VIL1 5.0V	5.0V VIL1 5.0V	IOH1	IOH1	5.0V VIL1 VIL1	5.0V VIL1 VIL1	5.0V			1Y 2Y 3Y 4Y	4.6		4.6		4.6		Vdc
V_{OH2}	3007	48 49 50 51	VIL1 5.0V	VIL1 5.0V				5.0V VIL1 5.0V 5.0V	5.0V VIL1 5.0V 5.0V	GND	5.0V VIL1 5.0V	5.0V VIL1 5.0V			5.0V VIL1 VIL1	5.0V VIL1 VIL1	5.0V 5.0V			1Y 2Y 3Y 4Y	4.95		4.95		4.95		Vdc
V_{OH3}	3007	52 53 54 55	VIL2 15.0V	VIL2 15.0V				15.0V VIL2 15.0V	15.0V VIL2 15.0V	GND	15.0V VIL2 15.0V	15.0V VIL2 15.0V			15.0V VIL2 VIL2	15.0V VIL2 VIL2	15.0V			1Y 2Y 3Y 4Y	13.5		13.5		13.5		Vdc
I_{IL1}	3009	56	GND	GND				GND	GND	GND	GND	GND			GND	GND	15.0V			ALL TOGETHER	-0.1						μA
I_{IL2}	3009	57 58 59 60 61 62 63 64	GND	GND				GND	GND	GND	GND	GND			GND	GND	15.0V			1A 1B 2A 2B 3A 3B 4A 4B		-1.0					μA
I_{IH1}	3010	65	15.0V	15.0V				15.0V	15.0V	GND	15.0V	15.0V			15.0V	15.0V	15.0V			ALL TOGETHER		+0.1					μA
I_{IH2}	3010	66 67 68 69 70 71 72 73	15.0V GND	GND 15.0V GND				GND GND 15.0V GND	GND 15.0V VIC	GND	GND 15.0V VIC	GND 15.0V VIC			GND 15.0V GND	GND 15.0V	15.0V			1A 1B 2A 2B 3A 3B 4A 4B				+1.0			μA

TABLE B3. TEST SPECIFICATIONS FOR 4001B (Cont.)
TERMINAL CONDITIONS (PINS NOT DESIGNATED ARE OPEN)



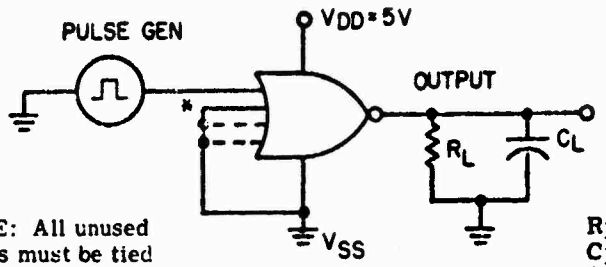
A. The input capacitance shall be measured between the specified measurement terminal and the V_{SS} terminal. The measurement frequency shall be within the range of 100 khz and 1.0 mHz.

B. Pulse Conditions - See Figure B1.

C. Load Conditions - See Figure B1.

TABLE B3. TEST SPECIFICATIONS FOR 4001B (Cont.)

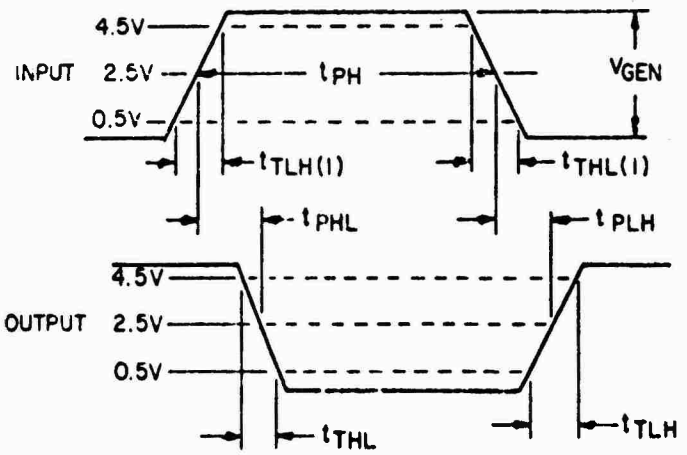
TEMP.	VIL1	VIH1	VIL2	VIH2	IOL1	IOH1
25°C	1.1	3.8	3.36	11.42	0.51	-0.2
-55°C	1.35	3.95	3.65	11.7	0.64	-0.25
125°C	0.85	3.6	3.03	11.12	0.36	-0.14
UNITS	V	V	V	V	mA	mA



* NOTE: All unused inputs must be tied to VSS.

TEST CIRCUIT

R_L = 200 kΩ
C_L = 50 pF ±5 (includes wiring and probe capacitance)



DYNAMIC TEST WAVEFORMS

Input pulse

$V_{GEN} = V_{DD} \pm 1.0\%$
$t_{PH} = 2.5 \pm 0.1$ µs
$t_{THL(1)} = t_{TLH(1)} = 10$ ns
Pulse repetition period = 5.0 ± 1 µs

FIGURE B1. SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS

TABLE B4. D.C. TEST LIST FOR 4013B

PARAMETER	INITIAL/FINAL TEST #'S			INTERIM TEST #'S
	25°C	+125°C	-55°C	25°C
VIC (POS)	1,2,3,4,5,6, 7,8			1,2,3,4,5,6
VIC (NEG)	9,10,11,12,13, 14,15			9,10,11,12,13, 14,15
ISS	17,18,19	17,18,19		17,18,19
VOL 1	20,21,22,23	20,21,22,23	20,21,22,23	20,21,22,23
VOL 2	24,25,26,27	24,25,26,27	24,25,26,27	24,25,26,27
VOL 3	28,29,30,31	28,29,30,31	28,29,30,31	28,29,30,31
VOH 1	32,33,34,35	32,33,34,35	32,33,34,35	32,33,34,35
VOH 2	36,37,38,39	36,37,38,39	36,37,38,39	36,37,38,39
VOH 3	40,41,42,43	40,41,42,43	40,41,42,43	40,41,42,43
IIL 1	44			44
IIL 2		45,46,47,48, 49,50,51,52		
IIH 1	53			53
IIH 2		54,55,56,57,58 59,60,61,62		

TABLE B5. A.C. TEST LIST FOR 4013B

PARAMETER	DYNAMIC TEST
C_I	62-69
TRUTH TABLE	70-86
t PHL	87-90
t PHL (R or S)	91-94
t PLH	95-98
t PLH (R or S)	99-102
t THL	103-106
t TLH	107-110
fcL	111,112
TTLHCL	113,114
tP	115,116
t SHL	117,118
t SLH	119,120
t HHL	121,122
t HLH	123,124

TABLE B6. TEST SPECIFICATIONS FOR 4013B

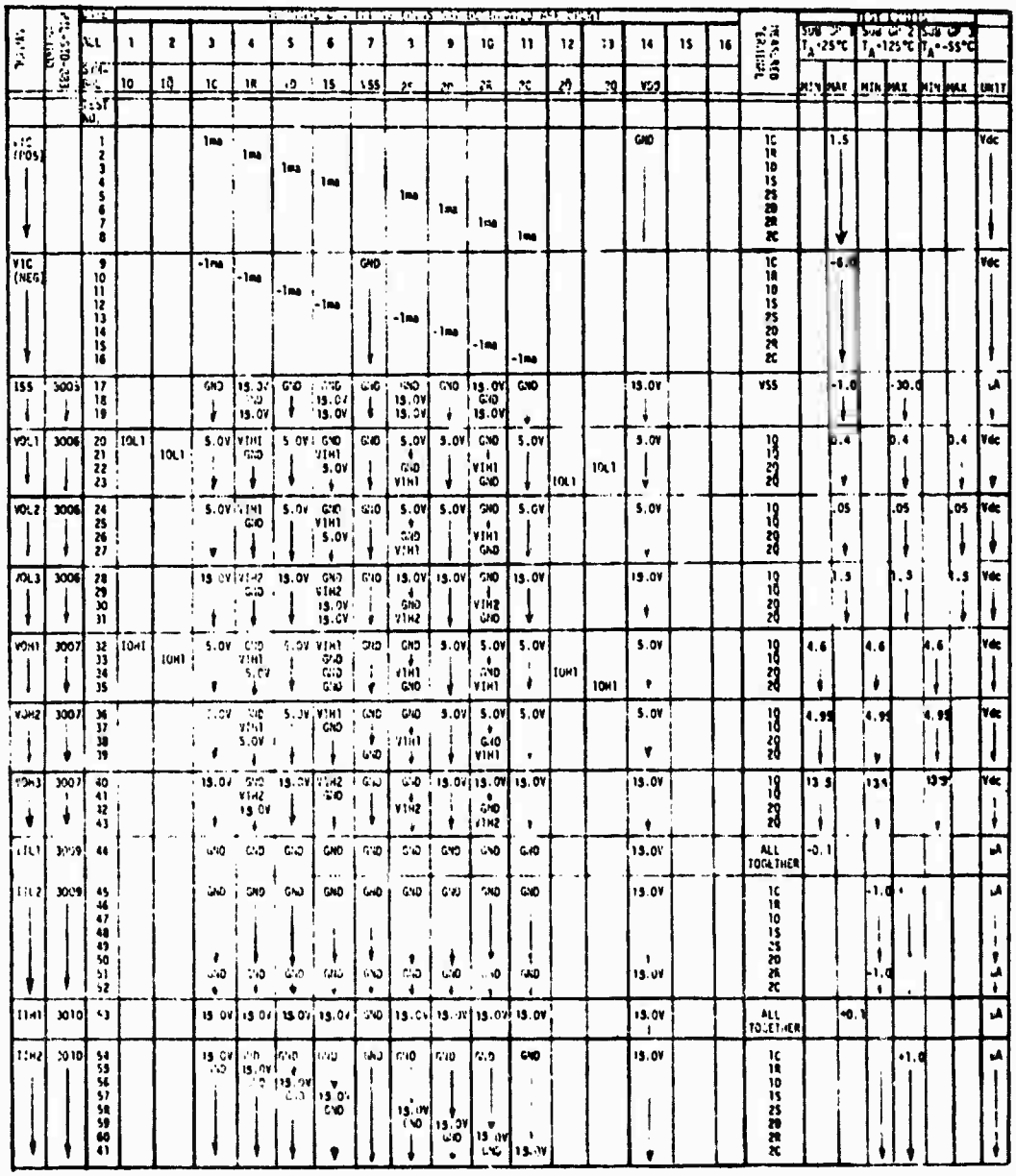


TABLE B6. TEST SPECIFICATIONS FOR 4013B (Cont.)

Symbol	MIL-STD-883 method	Cases C, D	Terminal conditions and limits														Measured terminal	Test limits						Units
		Symbol	Q_1	$\overline{Q}_1$	CLK_1	RS_1	D_1	SET_1	V_{SS}	SET_2	D_2	RS_2	CLK_2	Q_2	$\overline{Q}_2$	V_{DD}								
		Test No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14		Min	Max	Min	Max	Min	Max	
																		Subgroup 4 T_A = 25°C						
C_i	3012	62 63 64 65 66 67 68 69			B	B	B	B	GND	B	B	B	B			GND	CLK_1 RS_1 D_1 SET_1 SET_2 D_2 RS_2 CLK_2		7.5					pF

TABLE B6. TEST SPECIFICATIONS FOR 4013B (Cont.)

Symbol	MIL-STD-883 method	Case C, D	Terminal conditions and limits														Measured terminal	Test limits						Units
																		Subgroup 7 T_A = 25°C		Subgroup 8				
																				T_A = 125°C		T_A = -55°C		
		Symbol	Q_1	$\bar{Q}_1$	CLK_1	RS_1	D_1	SET_1	V_{SS}	SET_2	D_2	RS_2	CLK_2	$\bar{Q}_2$	Q_2	V_{DD}								
		Test No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14		Min	Max	Min	Max	Min	Max	
Truth table test	3016	70			5.0 V	GND	GND	GND	GND	GND	GND	GND	5.0 V			5.0 V	None							
		71			GND		GND				GND		GND				None							
		72	L	H	5.0 V		GND				GND		5.0 V	H	L		All outputs							
		73	L	H	5.0 V		5.0 V				5.0 V		5.0 V	H	L									
		74	L	H	GND								GND	H	L									
		75	H	L	5.0 V								5.0 V	L	H									
		76	L	H	5.0 V	5.0 V						5.0 V	5.0 V	H	L									
		77	L	H	GND	5.0 V						5.0 V	GND	H	L									
		78	L	H	5.0 V	5.0 V						5.0 V	5.0 V	H	L									
		79	H	L	5.0 V	GND	GND	5.0 V		5.0 V	GND	GND	5.0 V	L	H									
		80	H	L	GND			5.0 V		5.0 V			GND	L	H									
		81	H	L	5.0 V			5.0 V		5.0 V			5.0 V	L	H									
		82	H	L	5.0 V			GND		GND			5.0 V	L	H									
		83	H	L	GND			GND		GND			GND	L	H									
		84	L	H	5.0 V			GND		GND			5.0 V	H	L									
		85	H	H	5.0 V	5.0 V	5.0 V	5.0 V		5.0 V	5.0 V	5.0 V	5.0 V	H	H									
		86	H	H	GND	5.0 V	5.0 V	5.0 V		5.0 V	5.0 V	5.0 V	GND	H	H									
																		Subgroup 9 T_A=25°C		Subgroup 10 T_A= 125°C		Subgroup 11 T_A = -55°C		
t_{PHL}	3003 (Fig 82)	87	OUT		IN				GND							5.0 V	CLK_1 to Q_1	70	500	70	750	50	500	ns
		88		OUT	IN												CLK_1 to $\bar{Q}_1$							
		89											IN		OUT		CLK_2 to Q_2							
		90											IN	OUT			CLK_2 to $\bar{Q}_2$							
t_{PHL} R or S	3003 (Fig 82)	91		OUT				IN									SET_1 to Q_1		550		825		550	
		92	OUT			IN											RS_1 to Q_1							
		93								IN				OUT			SET_2 to Q_2							
		94										IN			OUT		RS_2 to Q_2							
t_{PLH}	3003 (Fig 82)	95	OUT		IN												CLK_1 to Q_1							
		96		OUT	IN												CLK_1 to $\bar{Q}_1$							
		97											IN		OUT		CLK_2 to Q_2							
		98											IN	OUT			CLK_2 to $\bar{Q}_2$							

See notes C and D

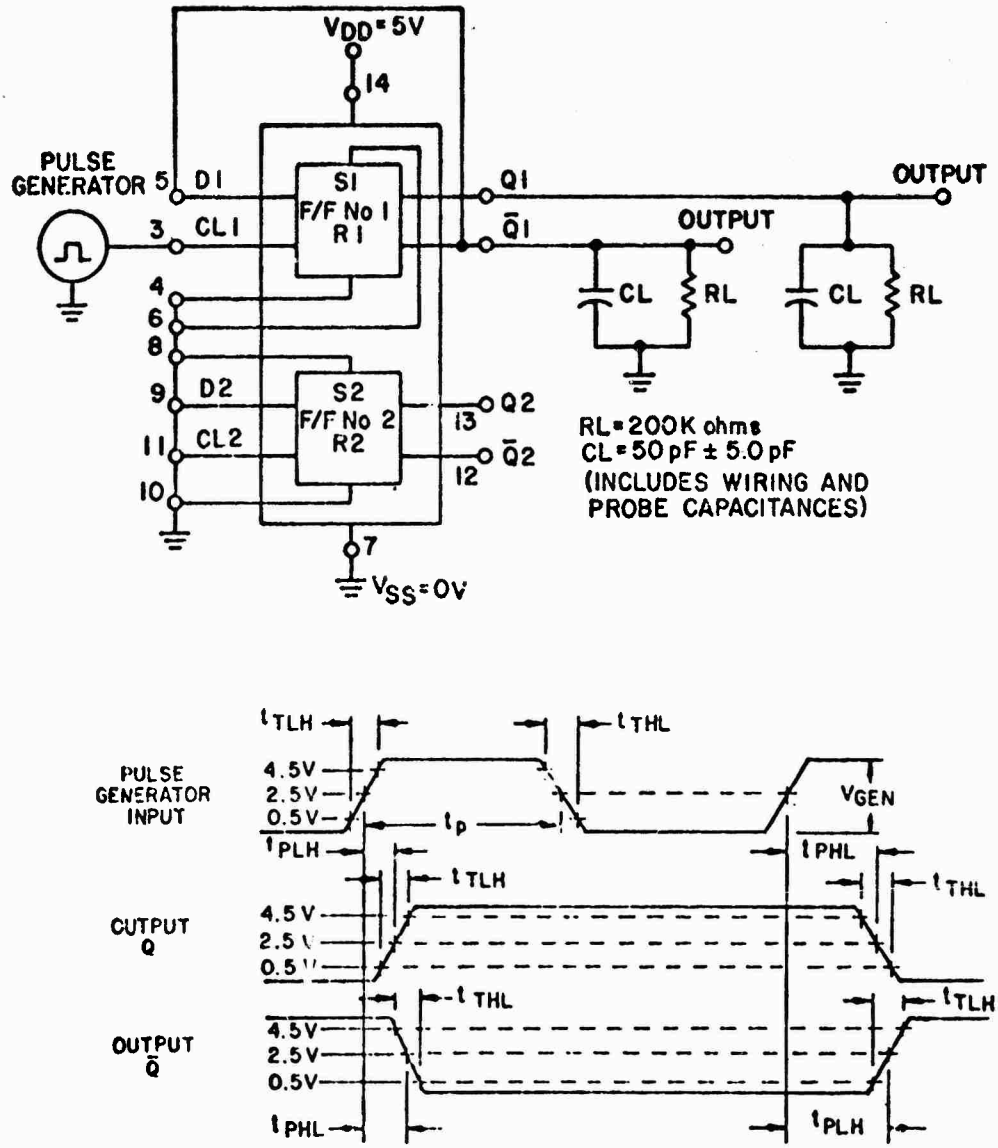
TABLE B6. TEST SPECIFICATIONS FOR 4013B (Cont.)

Symbol	MIL-STD-883 method	Cases C, D	Terminal conditions and limits														Measured terminal	Test limits						Units
																		Subgroup 9 T_A = 25°C		Subgroup 10 T_A = 125°C		Subgroup 11 T_A = -55°C		
		Symbol	Q_1	$\overline{Q}_1$	CLK_1	RS_1	D_1	SET_1	V_{SS}	SET_2	D_2	RS_2	CLK_2	$\overline{Q}_2$	Q_2	V_{DD}		Min	Max	Min	Max	Min	Max	
		Test No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14								
t_{PLH} R or S	3003 (Fig 8-3)	99	OUT					IN	GND							5.0 V	SET_1 to Q_1	100	420	100	630	70	420	ns
		100		OUT		IN											RS_1 to $\overline{Q}_1$							
		101								IN					OUT		SET_2 to Q_2							
		102										IN		OUT			RS_2 to $\overline{Q}_2$							
t_{THL}	3004 (Fig 8-2)	103	OUT		IN												Q_1	15	300	20	450	10	300	
		104		OUT	IN												$\overline{Q}_1$							
		105											IN		OUT		Q_2							
		106											IN	OUT			$\overline{Q}_2$							
t_{TLH}	3004 (Fig 8-2)	107	OUT		IN												Q_1		350		525		350	
		108		OUT	IN												$\overline{Q}_1$							
		109											IN	OUT			Q_2							
		110											IN		OUT		$\overline{Q}_2$							
f_{CL} (max) See note E	(Fig 8-2)	111	OUT		IN												CLK_1		0.67		1.0		0.67	µs
		112											IN		OUT		CLK_2		0.67		1.0		0.67	µs
t_{TLHCL} (MAX) See note F	(Fig 8-2)	113	OUT		IN												CLK_1	15		15		10		µs
		114											IN		OUT		CLK_2	15		15		10		µs
t_P See note G	(Fig 8-2)	115	OUT		IN												CLK_1		300		450		300	ns
		116											IN		OUT		CLK_2		300		450		300	
t_{SHL} t_{SHL}	(Fig 8-4)	117			IN		IN				IN		IN				D_1 to CLK_1 D_2 to CLK_2		150		225		150	
t_{SLH} t_{SLH}		119			IN		IN				IN		IN				D_1 to CLK_1 D_2 to CLK_2							
t_{RHL} t_{RHL}	(Fig 8-5)	121			IN		IN				IN		IN				D_1 to CLK_1 D_2 to CLK_2							
t_{RLH} t_{RLH}		123			IN		IN				IN		IN				D_1 to CLK_1 D_2 to CLK_2							

NOTES
A. Pins not designated may be "high" level logic, "low" level logic or open.
B. Capacitance shall be measured between the designated terminal and V_{SS} at a frequency of 1 MHz.
C. Test number 70 thru 86 shall be run in sequence and the functional tests shall be performed with V_{IH} and V_{DD} = 5.0V
D. L = 0.5V maximum and H = 4.5V minimum.
E. The maximum clock frequency (f_{CL} requirement is considered met if proper output state changes occur with the pulse repetition period set to that given in the limits column.
F. Pulse repetition period = 100 µsec, 50 percent duty cycle. The maximum clock transition time (t_{TLHCL}) requirement is considered met if proper output state changes occur with the rise time set to that given in the limits column.
G. The minimum clock pulse width (t_p) requirement is considered met if proper output state changes occur with the pulse width set to that given in the limits column.

TABLE B6. TEST SPECIFICATIONS FOR 4013B (Cont.)

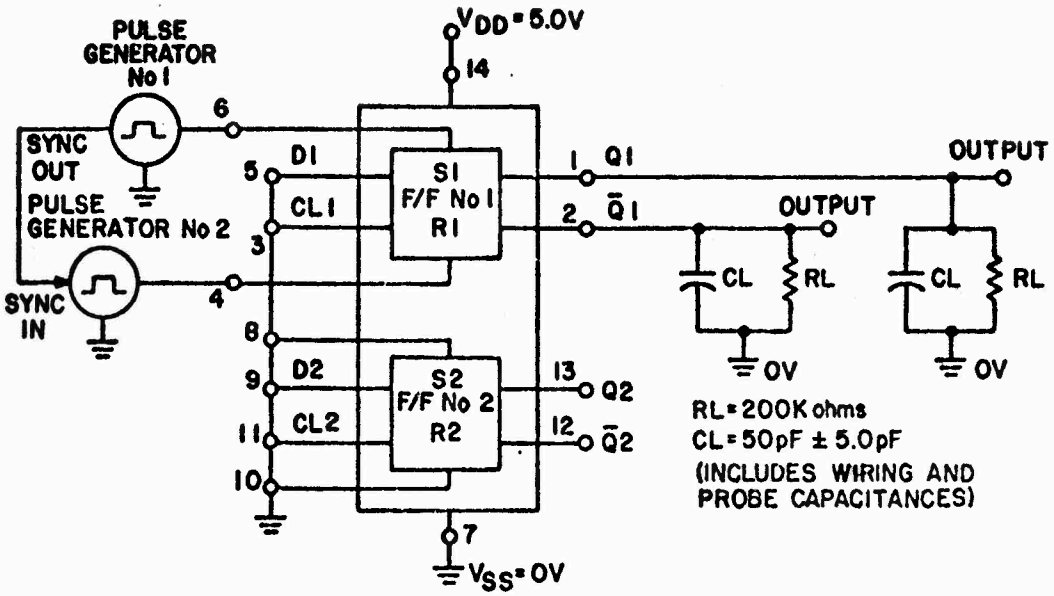
TEMP.	VIL1	VIH1	VIL2	VIH2	IOL1	IOH1
25°C	1.1	3.8	3.36	11.42	0.51	-0.2
-55°C	1.35	3.95	3.65	11.7	0.54	-0.25
125°C	0.85	3.6	3.03	11.12	0.36	-0.14
UNITS	V	V	V	V	mA	mA

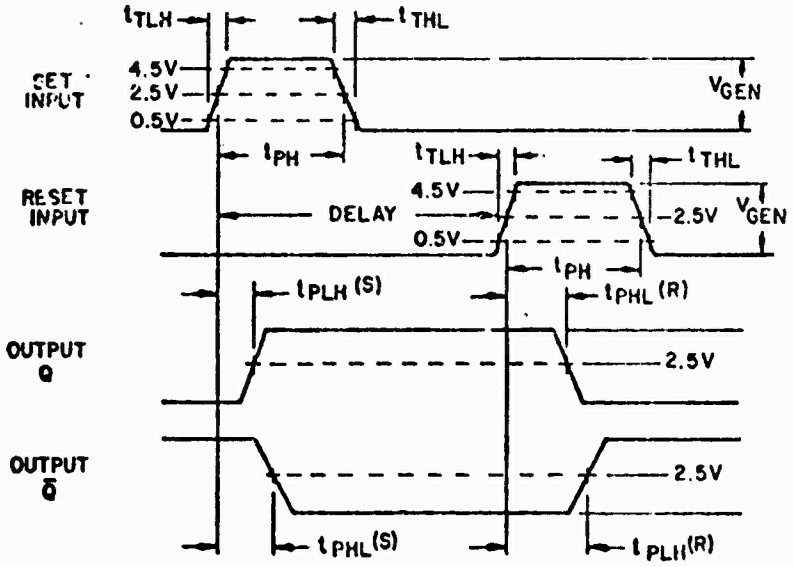


NOTES:

1. The pulse generator has the following characteristics: $V_{gen} = V_{DD} \pm 1\%$, duty cycle = 50%, $t_{TLH} = t_{THL} \simeq 20$ ns. and pulse repetition period = 5.0 ± 0.5 μs.
2. Identical switching measurements are obtained from F/F No. 1 and F/F No. 2.
3. For f_{CL} and tp the pulse repetition period is variable.

FIGURE B2. SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS

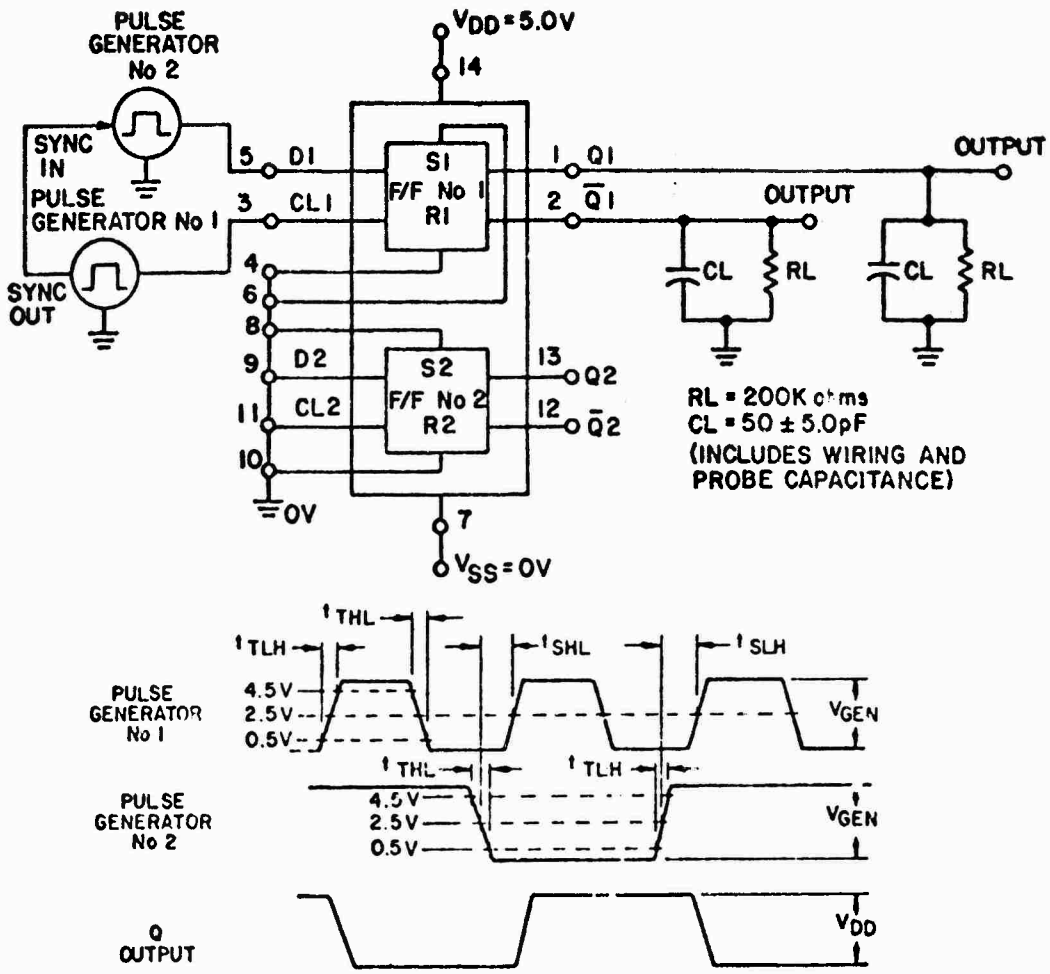




NOTES:

1. The pulse generators have the following characteristics: V_{gen} = VDD ±1%, t_{PH} = 1.0 ±0.1 μs, $t_{THL} = t_{TLH} \simeq 20$ ns and pulse repetition period = 5.0 ±0.5 μs.
2. The reset pulse delay is 2.5 ±0.25 μs.
3. Identical switching measurements are obtained from F/F No. 1 and F/F No. 2.

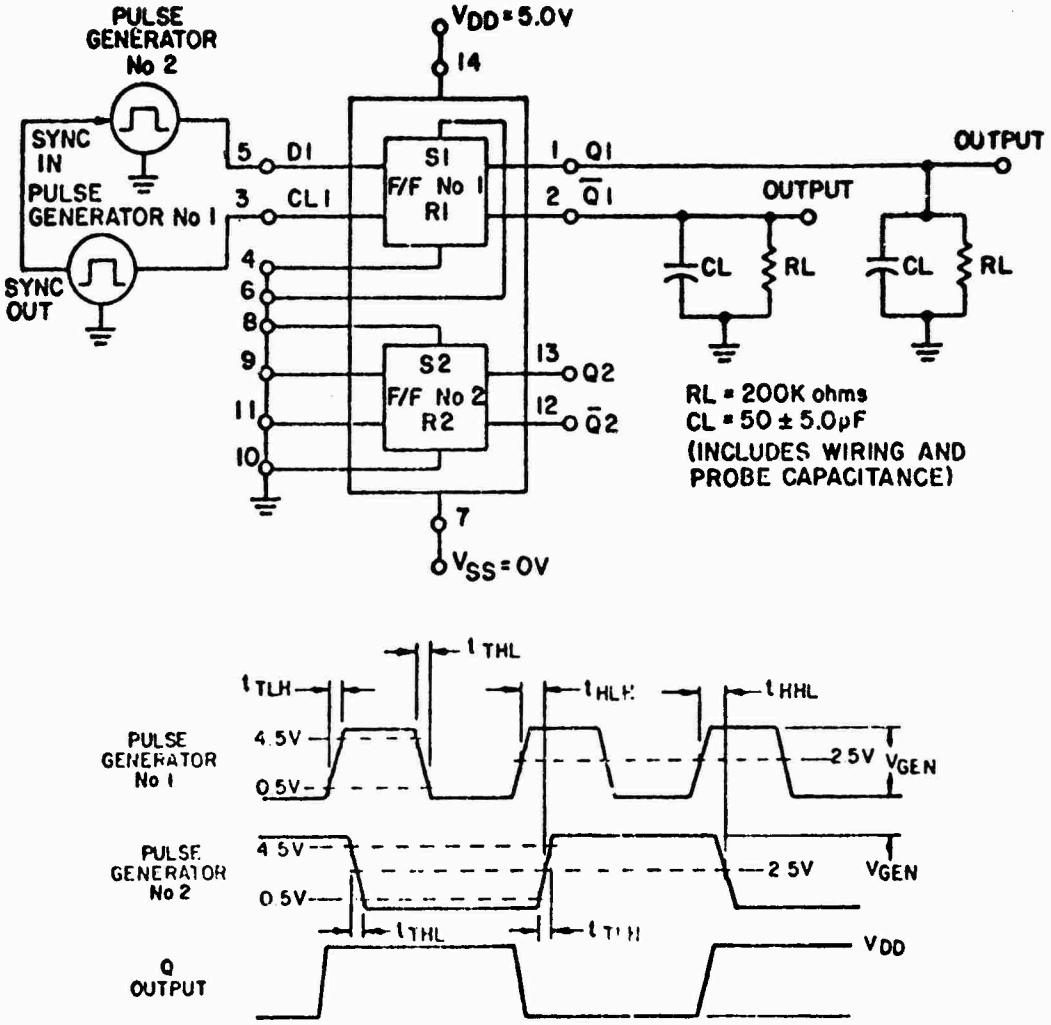
FIGURE B3. SET-RESET SWITCHING TEST CIRCUIT AND WAVEFORMS



NOTES:

1. Pulse generator No. 1 has the following characteristics: $V_{gen} = V_{DD} \pm 1\%$, duty cycle = 50%, $t_{TLH} = t_{THL} \simeq 20$ ns and pulse repetition period = 5.0 ± 0.5 μs.
2. Pulse generator No. 2 has the following characteristics: $V_{gen} = V_{DD} \pm 1.0\%$, duty cycle = variable, $t_{TLH} = t_{THL} \simeq 20$ ns and pulse repetition period = twice that of pulse generator No. 1.
3. Identical measurements are obtained from F/F No. 1 and F/F No. 2.

FIGURE B4. SET-UP TIME TEST CIRCUIT AND WAVEFORMS



NOTES:

1. Pulse generator No. 1 has the following characteristics: $V_{gen} = V_{DD} \pm 1\%$, duty cycle = 50%, $t_{TLH} = t_{THL} \simeq 20$ ns and pulse repetition period = 5.0 ±0.5 μs.
2. Pulse generator No. 2 has the following characteristics: $V_{gen} = V_{DD} \pm 1\%$, duty cycle = variable, $t_{TLH} = t_{THL} \simeq 20$ ns and pulse repetition period = twice that of pulse generator No. 1.
3. Identical measurements are obtained from either F/F No. 1 and F/F No. 2.

FIGURE B5. HOLD TIME TEST CIRCUIT AND WAVEFORMS

TABLE B7. D.C. TEST LIST FOR M38510/05401

PARAMETER	INITIAL/FINAL TEST #'S			INTERIM TEST #'S
	25°C	+125°C	-55°C	25°C
VIC+	1-9			1-9
VIC-	10-18			10-18
ISS	19-46	19-46		19-46
VOH1	47-52	47-52	47-52	47-52
VOH2	53-58	53-58	53-58	53-58
VOH3	59-77	59-77	59-77	59-77
VOL1	78-82	78-82	78-82	78-82
VOL2	83-87	83-87	83-87	83-87
VOL3	88-104	88-104	88-104	88-104
IIH	105	106-114		105
IIL	115	116-124		115

TABLE B8. A.C. TEST LIST FOR M38510/05401

PARAMETER	DYNAMIC TEST
CI	125-133
TRUTH TABLE	134-161
t PHL	162-177
t PLH	178-193
t THL	194-199
t TLH	200-205

TABLE B9 TEST SPECIFICATION FOR M38510/05401

Symbol	MIL-STD-883 method	Case E, F	Terminal conditions and limits																Measured terminal	Test limits						Units
			1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16		Subgroup 1 T_A = 25°C		Subgroup 2 T_A = 125°C		Subgroup 3 T_A = -55°C		
		Test No.	A4	B3	A3	B2	A2	B1	A1	V_{SS}	C_{IN}	S1	S2	S3	S4	C_{OUT}	B4	V_{DD}		Min	Max	Min	Max	Min	Max	
$V_{IC(POS)}$		1	1 mA															GND	A4		1.5					Vdc
		2		1 mA															B3							
		3			1 mA														A3							
		4				1 mA													B2							
		5					1 mA												A2							
		6						1 mA											B1							
		7							1 mA										A1							
		8									1 mA								C_{IN}							
		9															1 mA		B4							
$V_{IC(NEG)}$		10	-1 mA							GND									A4		-5					Vdc
		11		-1 mA															B3							
		12			-1 mA														A3							
		13				-1 mA													B2							
		14					-1 mA												A2							
		15						-1 mA											B1							
		16							-1 mA										A1							
		17									-1 mA								C_{IN}							
		18															-1 mA		B4							
I_{SS}	3005	19	GND	GND	GND	GND	GND	GND	GND	GND	GND						GND	15 V	V_{SS}		-10.0		-10.0			μA
		20	15 V	15 V	15 V	15 V	15 V	GND	GND		15 V						15 V									
		21	15 V		GND	GND	GND	15 V	15 V								15 V									
		22	15 V		GND	15 V	15 V	15 V	GND								GND									
		23	GND		15 V		15 V	15 V	15 V								GND									
		24	15 V		GND		GND	GND	GND								GND									
		25	GND		15 V		GND	15 V	GND		GND						15 V									
		26	15 V	GND	GND		15 V	15 V	GND		15 V						GND									
		27	15 V	15 V	GND		GND	GND	15 V		15 V						GND									
		28	15 V	15 V	GND	GND	GND	15 V			15 V						GND									
		29	GND	GND	15 V	GND	15 V	GND			GND						15 V									
		30	GND	GND	GND	GND		15 V			15 V						15 V									
		31	15 V	15 V	GND	15 V		GND	GND		15 V						GND									
		32		GND	15 V	15 V		15 V	GND		15 V															
		33		GND	15 V	15 V	GND	15 V	15 V		GND															
		34		15 V	GND	15 V	GND	15 V	GND		15 V															
		35			15 V	GND	GND	GND			GND															
		36			GND	GND	GND	15 V			15 V						GND									
		37	GND		GND	GND	15 V	15 V			15 V						15 V									
		38	15 V	GND	GND	GND	15 V	15 V	15 V		GND						GND									
		39	GND	GND	15 V	GND	15 V	15 V	GND		15 V						15 V									
		40	15 V			GND	GND	GND	15 V		15 V						GND									
		41				GND	15 V	15 V	GND		GND															
		42				15 V	GND	15 V	GND		GND															
		43				15 V	GND	GND	15 V		GND															
		44				GND	15 V		GND		15 V															
		45	GND	15 V	GND	GND	15 V		15 V		15 V						15 V									
		46	GND	15 V	GND	GND	GND		GND		GND						15 V									

TABLE B9. TEST SPECIFICATIONS FOR M38510/05401 (Continued)

Symbol	MIL-STD-883 method	Case E, F	Terminal conditions and limits																Measured terminal	Test limits						Units
			1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16		Subgroup 1 T_A = 25°C		Subgroup 2 T_A = 125 C		Subgroup 3 T_A = -55 C		
		Test No.	A4	B3	A3	B2	A2	B1	A1	V_{SS}	C_{IN}	S1	S2	S3	S4	C_{OUT}	R4	V_{DD}		Min	Max	Min	Max	Min	Max	
V_{OH1}	3006	47	V_{IL1}	V_{IL1}	V_{IL1}	V_{IL1}	V_{IL1}	V_{IL1}	V_{IH1}	GND	V_{IL1}	I_{OH1}	I_{OH1}	I_{OH1}	I_{OH1}	I_{OH2}	V_{IL1}	5.0 V	S1	4.5		4.5		4.5		Vdc
		48			V_{IL1}		V_{IH1}		V_{IL1}										S2							
		49	V_{IH1}		V_{IH1}		V_{IL1}										V_{IH1}		S3							
		50			V_{IL1}												V_{IL1}		S4							
		51			V_{IL1}											I_{OH2}			C_{OUT}							
		52			V_{IH1}		V_{IH1}		V_{IH1}		V_{IH1}					I_{OH2}			C_{OUT}							
V_{OH2}		53	V_{IL1}		V_{IL1}		V_{IL1}		V_{IH1}		V_{IL1}								S1	4.95		4.95		4.95		
		54			V_{IL1}		V_{IH1}		V_{IL1}										S2							
		55			V_{IH1}		V_{IL1}												S3							
		56	V_{IH1}		V_{IL1}												V_{IH1}		S4							
		57			V_{IL1}												V_{IL1}		C_{OUT}							
		58			V_{IH1}		V_{IH1}		V_{IH1}		V_{IH1}								C_{OUT}							
V_{OH3}		59	V_{IL2}	V_{IL2}	V_{IL2}	V_{IL2}	V_{IL2}	V_{IL2}	V_{IH2}		V_{IL2}						V_{IL2}	12.5 V	S1	11.25		11.25		11.25		
		60						V_{IH2}	V_{IL2}		V_{IL2}								S1							
		61						V_{IL2}	V_{IL2}		V_{IH2}								S1							
		62						V_{IH2}	V_{IH2}		V_{IL2}								S1							
		63						V_{IH2}	V_{IH2}		V_{IH2}								S1							
		64				V_{IH2}	V_{IH2}	V_{IH2}	V_{IH2}		V_{IH2}								S2							
		65				V_{IH2}	V_{IL2}	V_{IL2}	V_{IH2}		V_{IL2}								S2							
		66				V_{IL1}	V_{IH2}	V_{IL2}	V_{IH2}		V_{IH2}								S2							
		67		V_{IH2}		V_{IL2}	V_{IL2}	V_{IL2}	V_{IL2}		V_{IL2}								S3							
		68		V_{IL2}		V_{IL2}	V_{IL2}	V_{IH2}	V_{IL2}		V_{IH2}								S3							
		69		V_{IH2}		V_{IH2}	V_{IH2}	V_{IH2}	V_{IH2}		V_{IH2}								S3							
		70		V_{IL2}		V_{IH2}	V_{IH2}	V_{IH2}	V_{IH2}		V_{IH2}								S3							
		71	V_{IH2}		V_{IH2}	V_{IH2}	V_{IH2}	V_{IH2}	V_{IH2}		V_{IH2}						V_{IH2}		S4							
		72	V_{IL2}	V_{IH2}	V_{IH2}	V_{IH2}	V_{IH2}	V_{IH2}	V_{IH2}		V_{IH2}						V_{IH2}		S4							
		73	V_{IH2}	V_{IH2}	V_{IH2}	V_{IH2}	V_{IH2}	V_{IH2}	V_{IH2}		V_{IH2}						V_{IL2}		S4							
		74	V_{IL2}	V_{IH2}	V_{IH2}	V_{IH2}	V_{IH2}	V_{IH2}	V_{IH2}		V_{IH2}						V_{IL2}		S4							
		75	V_{IH2}	V_{IH2}	V_{IH2}	V_{IH2}	V_{IH2}	V_{IH2}	V_{IH2}		V_{IH2}						V_{IH2}		C_{OUT}							
		76	V_{IL2}	V_{IH2}	V_{IH2}	V_{IH2}	V_{IH2}	V_{IH2}	V_{IH2}		V_{IH2}						V_{IH2}		C_{OUT}							
		77	V_{IH2}	V_{IL2}	V_{IL2}	V_{IL2}	V_{IL2}	V_{IH2}	V_{IL2}		V_{IL2}						V_{IH2}		C_{OUT}							
V_{OL1}	3007	78	V_{IL1}	V_{IL1}	V_{IL1}	V_{IL1}	V_{IL1}	V_{IL1}	V_{IL1}		V_{IL1}	I_{OL1}	I_{OL1}	I_{OL1}	I_{OL1}	I_{OL2}	V_{IL1}	5.0 V	S1		0.5		0.5		0.5	Vdc
		79																	S2							
		80																	S3							
		81																	S4							
		82																	C_{OUT}							
V_{OL2}		83																	S1		.05		.05		.05	Vdc
		84																	S2							
		85																	S3							
		86																	S4							
		87																	C_{OUT}							

TABLE B9. TEST SPECIFICATION FOR M38510/05401 (Continued)

Symbol	MIL-STD-883 method	Case E, F	Terminal conditions and limits																Measured terminal	Test limits						Units
			1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16		Subgroup 1 T_A = 25°C		Subgroup 2 T_A = 125°C		Subgroup 3 T_A = -55°C		
		Test No.	A4	B3	A3	B2	A2	B1	A1	V_{SS}	C_{IN}	S1	S2	S3	S4	C_{OUT}	B4	V_{DD}		Min	Max	Min	Max	Min	Max	
V_{OL3}	3007	88 89 90 91 92 93 94 95 96 97 98 99 100 101 102 103 104	V_{IL2} V_{IH2} V_{IH2} V_{IL2} V_{IL2}	V_{IL2} V_{IH2} V_{IH2} V_{IH2} V_{IH2}	V_{IL2} V_{IH2} V_{IL2} V_{IH2} V_{IL2}	V_{IL2} V_{IH2} V_{IH2} V_{IL2} V_{IH2} V_{IH2} V_{IL2}	V_{IL2} V_{IH2} V_{IL2} V_{IH2} V_{IL2} V_{IH2} V_{IH2} V_{IL2}	V_{IL2} V_{IL2} V_{IH2} V_{IH2} V_{IL2} V_{IL2} V_{IH2} V_{IH2} V_{IL2}	V_{IL2} V_{IH2} V_{IL2} V_{IH2} V_{IL2} V_{IL2} V_{IH2} V_{IH2} V_{IL2}	GND	V_{IL2} V_{IH2} V_{IH2} V_{IL2}						V_{IL2} V_{IH2} V_{IL2} V_{IH2} V_{IH2}	12.5 V	S1 S1 S1 S1 S2 S2 S2 S2 S3 S3 S3 S3 S4 S4 B4 S4 C_{OUT}		1.25		1.25		1.25	Vdc
I_{IH1} see note 3	3010	105	15 V	15 V	15 V	15 V	15 V	15 V	15 V		15 V						15 V	15 V	All inputs together		8.0					nA
I_{IH2}	3010	106 107 108 109 110 111 112 113 114	15 V GND	GND 15 V GND	GND GND 15 V GND	GND 15 V GND	GND 15 V GND	GND 15 V GND	GND 15 V GND GND		GND 15 V GND						GND 15 V		A4 B3 A3 B2 A2 B1 A1 C_{IN} B4		1.0		45			nA
I_{IL1} see note 3	3009	115	GND	GND	GND	GND	GND	GND	GND		GND						GND	15 V	All inputs together		-9.0					nA
I_{IH3}	3500	116 117 118 119 120 121 122 123 124	GND	GND	GND	GND	GND	GND	GND		GND						GND	15 V	A4 B3 A3 B2 A2 B1 A1 C_{IN} B4				-150			nA

TABLE B9. TEST SPECIFICATION FOR M38510/05401 (Continued)

Symbol	MIL-STD-883 method	Case E, F	Terminal conditions and limits															Measured terminal	Test limits						Units
			1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Subgroup 4 T_A = 25 C						
		Test No.	A4	B3	A3	B2	A2	B1	A1	V_{SS}	C_{IN}	S1	S2	S3	S4	C_{OUT}	B4	V_{DD}		Min	Max				
C_I	3012	125	K							GND									A4		15				pF
		126		K															B3						
		127			K														A3						
		128				K													B2						
		129					K												A2						
		130						K											B1						
		131							K										A1						
		132									K								C_{IN}						
		133															K		B4						
																				Subgroup 7 T_A 25 C		Subgroup 8 T_A 125 C		T_A -55 C		
																				Min	Max	Min	Max	Min	Max	
Truth table test	3014	134	GND	GND	GND	GND	GND	GND	GND	GND	GND	L	L	L	L	L	GND	5 V	All outputs	See notes L and M						
		135	5 V	5 V	5 V	5 V	5 V	GND	GND		5 V	H	L	H	H	H	5 V									
		136	5 V		GND	GND	GND	5 V	5 V			H	H	H	L	H	5 V									
		137	5 V		GND	5 V	5 V	5 V	GND			L		L	L	H	GND									
		138	GND		5 V		5 V	5 V	5 V			H		H	H	L	GND									
		139	5 V		GND		GND	GND	GND			H		H	H	L	GND									
		140	GND		5 V		GND	5 V	GND		GND	H		L	L	H	5 V									
		141	5 V	GND	GND		5 V	5 V	GND		5 V	L		H	H	L	GND									
		142	5 V	5 V	GND		GND	GND	5 V		5 V	L	L	L	L	H	GND									
		143	5 V	5 V	GND	GND	GND	5 V			5 V	H	H	H	H	L	GND									
		144	GND	GND	5 V	GND	5 V	GND			GND		H	H	H	L	5 V									
		145	GND	GND	GND	GND		5 V			5 V		L	H	H	L	5 V									
		146	5 V	5 V	GND	5 V		GND	GND		5 V	L	L	L	L	H	GND									
		147		GND	5 V			5 V	GND		5 V		H													
		148		GND	5 V		GND	5 V	5 V		GND		L													
		149		5 V	GND		GND	5 V	GND		5 V															
		150			5 V	GND	GND	GND			GND															
		151			GND	GND	5 V	5 V			5 V															
		152	GND		GND	5 V					5 V		H				5 V									
		153	5 V		GND	GND			5 V		GND		L				GND									
		154	GND	GND	5 V				GND		5 V		L				5 V									
		155	5 V	GND	5 V		GND	GND	5 V		5 V		H	H	H	L	GND									
		156					5 V	5 V	GND		GND	H														
		157				5 V	GND	5 V	GND		GND															
		158				5 V	GND	GND	5 V		GND															
		159				GND	5 V		GND		5 V															
		160	GND	5 V	GND	GND	5 V		5 V		5 V	L	L	L	L	H	5 V									
		161	GND	5 V	GND	GND	GND		GND		GND	L	L	H	H	L	5 V									

TABLE B9. TEST SPECIFICATIONS FOR M38510/05401

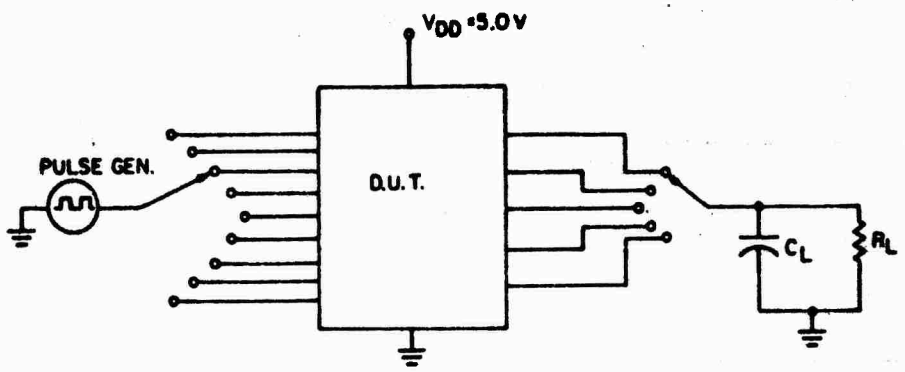
Symbol	MIL-STD-883 method	Case E, F	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Measured terminal	Test limits: Subgroup 9 T_A = 25 C Min	Subgroup 9 T_A = 25 C Max	Subgroup 10 T_A = 125 C Min	Subgroup 10 T_A = 125 C Max	Subgroup 11 T_A = -55 C Min	Subgroup 11 T_A = -55 C Max	Units
		Test No	A4	B3	A3	B2	A2	B1	A1	V_{SS}	C_{IN}	S1	S2	S3	S4	C_{OUT}	B4	V_{DD}								
t_{PHL}	3003 (Fig 8 6)	162	GND	GND	GND	GND	GND	GND	IN	GND	GND	OUT					GND	5 V	A1 to S1	100	2250	150	3375	80	2250	ns
		163					GND	IN	GND			OUT							B1 to S1							
		164					IN	GND					OUT						A2 to S2							
		165				IN	GND						OUT						B2 to S2							
		166			IN	GND								OUT					A3 to S3							
		167		IN	GND									OUT					B3 to S3							
		168	IN	GND											OUT				A4 to S4							
		169	GND												OUT		IN		B4 to S4							
		170									IN	OUT							C_{IN} to S1							
		171											OUT						C_{IN} to S2							
		172												OUT					C_{IN} to S3							
		173													OUT				C_{IN} to S4							
		174									GND					OUT	IN		B4 to C_{OUT}	40	750	60	1125	40	750	
		175	IN								GND						GND		A4 to C_{OUT}	40	750	60	1125	40	750	
		176	5 V		5 V		5 V		5 V		IN						GND		C_{IN} to C_{OUT}	20	300	30	450	20	300	
		177	GND	5 V	GND	5 V	GND	5 V	GND		IN						5 V		C_{IN} to C_{OUT}	20	300	30	450	20	300	
t_{PLH}		178	GND	GND	GND	GND	GND	GND	IN		GND	OUT					GND		A1 to S1	90	2900	130	4350	80	2900	
		179					GND	IN	GND			OUT							B1 to S1							
		180					IN	GND					OUT						A2 to S2							
		181				IN	GND						OUT						B2 to S2							
		182			IN	GND								OUT					A3 to S3							
		183		IN	GND									OUT					B3 to S3							
		184	IN	GND											OUT				A4 to S4							
		185	GND												OUT		IN		B4 to S4							
		186									IN	OUT							C_{IN} to S1							
		187											OUT						C_{IN} to S2							
		188												OUT					C_{IN} to S3							
		189													OUT				C_{IN} to S4							
		190									GND					OUT	IN		B4 to C_{OUT}	100	750	60	1125	40	750	
		191	IN								GND						GND		A4 to C_{OUT}	100	750	60	1125	40	750	
		192	5 V		5 V		5 V		5 V		IN						GND		C_{IN} to C_{OUT}	20	300	30	450	20	300	
		193	GND	5 V	GND	5 V	GND	5 V	GND		IN						5 V		C_{IN} to C_{OUT}	20	300	30	450	20	300	

TABLE B9. TEST SPECIFICATIONS FOR M38510/05401 (Continued)

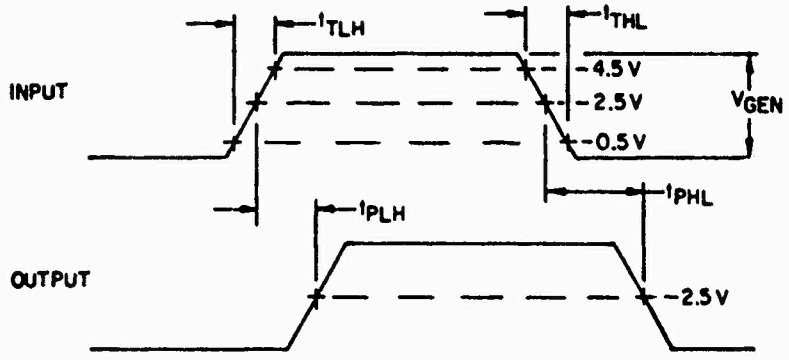
Symbol	MIL-STD-883 method	Case E, F	Terminal conditions and limits																Measured terminal	Test limits						Units
			1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16		Subgroup 9 T_A = 25°C		Subgroup 10 T_A = 125°C		Subgroup 11 T_A = -55°C		
		Test No.	A4	B3	A3	B2	A2	B1	A1	V_{SS}	C_{IN}	S1	S2	S3	S4	C_{OUT}	B4	V_{DD}		Min	Max	Min	Max	Min	Max	
t_{THL}	3004 (Fig 8 6)	194	GND	GND	GND	GND	GND	GND	IN	GND	GND	OUT	OUT	OUT	OUT		GND	5 V	S1	30	10000	30	15000	30	10000	ns
		195	↓	GND	GND	IN	5 V	5 V	5 V										S2							
		196	↓	5 V	IN	5 V	5 V	GND	GND										S3							
		197	IN	5 V	5 V	GND	GND	↓	↓								5 V		S4							
		198	IN	GND	GND	GND	GND	↓	↓		↓					OUT	5 V		C_{OUT}		520	45	780		520	
		199	5 V	GND	5 V	GND	5 V	↓	5 V		IN					OUT	GND		C_{OUT}		520	45	780		520	
t_{TLH}		200	GND	GND	GND	GND	GND	GND	IN		GND	OUT	OUT	OUT	OUT		GND		S1	30	10000	30	15000	30	10000	
		201	↓	GND	GND	IN	5 V	5 V	5 V								↓		S2							
		202	↓	5 V	IN	5 V	5 V	GND	GND										S3							
		203	IN	5 V	5 V	GND	GND		↓								5 V		S4							
		204	IN	GND	GND	GND	GND		↓		↓					OUT	5 V		C_{OUT}		520	45	780		520	
		205	5 V	GND	5 V	GND	5 V	↓	5 V		IN					OUT	GND		C_{OUT}		520	45	780		520	

NOTES

A. Pins not designated may be "high" level logic, "low" level logic or open.
B. I_{OH1} = -0.05 mA @ 25°C, -0.035 mA @ 125°C, -0.06 mA @ -55°C.
C. I_{OH2} = -0.25 mA @ 25°C, -0.175 mA @ 125°C, -0.31 mA @ -55°C.
D. I_{OL1} = 0.05 mA @ 25°C, 0.035 mA @ 125°C, 0.06 mA @ -55°C.
E. I_{OL2} = 0.25 mA @ 25°C, 0.175 mA @ 125°C, 0.31 mA @ -55°C.
F. V_{IH1} = 3.8 V @ 25°C, 3.6 V @ 125°C, 3.95 V @ -55°C.
G. V_{IH2} = 9.5 V @ 25°C, 9.25 V @ 125°C, 9.75 V @ -55°C.
H. V_{IL1} = 1.1 V @ 25°C, 0.85 V @ 125°C, 1.35 V @ -55°C.
I. V_{IL2} = 2.8 V @ 25°C, 2.55 V @ 125°C, 3.05 V @ -55°C.
J. For IIL and IIH at 25°C, All inputs will be measured together.
K. Capacitance shall be measured between the designated terminal and VSS at a frequency of 1 MHz.
L. Test numbers 134 through 161 shall be run in sequence.
M. L=0.5V max and H=4.5V min.



R_L = 200 kΩ
C_L = 50 pF ±5.0 pF (includes wiring and probe capacitance)



NOTES:

1. The pulse generator has the following characteristics: $V_{gen}=V_{DD}$ ±1%, duty cycle=50%, $t_{TLH} = t_{THL} \geq$ 20ns and pulse repetition period = 50±5µs.
2. See table B9 for complete terminal conditions.

FIGURE B6. Switching Times Test Circuit and Waveforms

TABLE B10. D.C. TEST LIST FOR M38510-05601

PARAMETER	INITIAL/FINAL TEST #'S			INTERIM TEST #'S
	25°C	+125°C	-55°C	25°C
IIH	1-3	1-3	1-3	1-3
IIL	4-6	4-6	4-6	4-6
VOH 1	7	7	7	7
VOL 1	8	8	8	8
VOH 2	9	9	9	9
VOL 2	10	10	10	10
VI $\overline{CE}$	11	11	11	11
VI $\overline{CL}$	12	12	12	12
VIR	13	13	13	13
ISS	14,15	14,15	14,15	14,15

TABLE B11. A.C. TEST LIST FOR M38510/05601

PARAMETER	DYNAMIC TEST
CI	16-18
t PHL 1	19
t PHL 2	20
t PLH 1	21
t PLH 2	22
t THL 1	23
t THL 2	24
t TLH 1	25
t TLH 2	26
t SHL 1	27
t SHL 2	28
t PHL 3	29
t PHL 4	30
t PHL 5	31

TABLE B12. TEST SPECIFICATIONS FOR M38510/05601

Symbol	MIL-STD 883 method	Case E, F	Terminal conditions (pins not designated are open)																	Meas. terminal	Test limits Subgroup 1 T_A = 25°C Min	Subgroup 1 T_A = 25°C Max	Subgroup 2 T_A = 125°C Min	Subgroup 2 T_A = 125°C Max	Subgroup 3 T_A = -55°C Min	Subgroup 3 T_A = -55°C Max	Units
		Test No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16									
			"1"	"2"	"4"	"8"	"T"	"S"		V_{SS}	"A"	"B"	"C"	Carry out	Clock enable	Clock	Reset	V_{DD}									
I_{DD}	3010	1								GND					15 V	GND	GND	15 V	13		10		100		10	mAdc
		2													GND	15 V	GND		14								
		3													GND	GND	15 V		15								
I_{CL}	3006	4															GND		15								
		5																	14								
		6																	15								
V_{OH1}	3005	7	P	P	P	P	P	P	P		P	P	P	H	B	B	B	5.5 V	B	4.20		4.20		4.50		Vdc
V_{OL1}	3007	8	G	G	G	G	G	G	G		G	G	G	J	B	B	B	5.0 V	B		500		500		500	mVdc
V_{OH2}	3006	9													A	A	A	15 V	A	14.90		14.90		14.80		Vdc
V_{OL2}	3007	10													A	A	A	15 V	A		10		50		10	mVdc
V_{ICE}		11																5.0 V	C	3.50		3.25		3.65		Vdc
V_{ICL}		12																5.0 V	D		1.50		1.75			
V_{IR}		13																5.0 V	E		1.50		1.75			
I_{IH}	3009	14													GND	GND	GND	15 V	5		5.0		100		500	μAdc
I_{IH}	3009	15													15 V	15 V	15 V	15 V	6		5.0		100		500	μAdc
																				Subgroup 4 T_A = 25°C Min	Subgroup 4 T_A = 25°C Max					
C_I	3012	16								GND					R			GND	13		12.0					pF
		17														B			14		15.0					
		18															R		15		12.0					
																				Subgrp 5 T_A = 25°C Min	Subgrp 5 T_A = 25°C Max	Subgrp 10 T_A = 125°C Min	Subgrp 10 T_A = 125°C Max	Subgrp 11 T_A = -55°C Min	Subgrp 11 T_A = -55°C Max	
t_{PHL1}	3003	19	P	P	P	P	P	P	P	GND	P	P	P	P	GND	K	GND	5.0 V	19		1.45		2.10		1.45	μs
t_{PHL2}		20																	N		1.80		2.70		1.80	
t_{PLH1}		21																	13		1.45		2.10		1.45	
t_{PLH1}		22																	N		1.80		2.70		1.80	
t_{THL1}	3004	13																	19		950		825		550	ns
t_{THL2}		14																	N		1.25		1.50		2.25	μs
t_{TLH1}		25																	23		350		825		500	ns
t_{TLH2}		26																	N		1.25		1.50		2.25	μs
t_{SHL1}		27													L	L	L		N		750		1.50		2.25	ns
t_{SHL2}		28													L	L	L		3		500		1125		750	
t_{PHL3}	3003	29	P	P	P	P	P	P	P		P	P	P	P	GND	M	M		6		1.80		2.70		1.80	μs
t_{PHL4}	3003	30	P	P	P	P	P	P	P		P	P	P	P	GND	M	M		13		1.45		2.10		1.45	
t_{PHL4}	3007	31	P	P	P	P	P	P	P		P	P	P	P	GND	M	M		T		1.80		2.70		1.80	

Subgroup 7 Verify truth table, figure B14 V_{DD} = 5.0 Vdc V_{OL} = V_{SS} + 0.50 Vdc; V_{OH} = V_{DD} -0.50 Vdc; T_A = 25°C.

Subgroup 8 Same test, terminal conditions and limits as subgroup 7, except T_A = 125°C and -55°C.

NOTES:

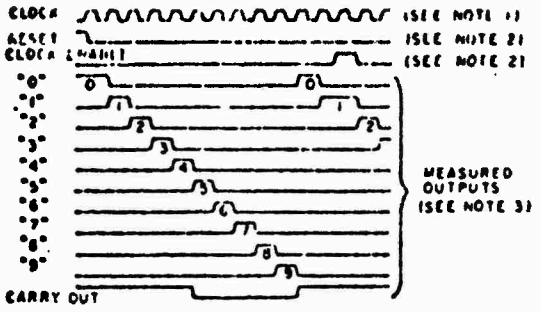
A. Each output shall be measured using timing diagram of figure B8.
B. Each output shall be measured using timing diagram of figure B9.
C. See figure B10.
D. See figure B11.
E. See figure B12.
F. I_{OH} = -30 μAdc @ 25°C; = 21 μAdc @125°C; = 37.5 μAdc @ -55°C.
G. I_{OL} = 50 μAdc @ 25°C; = 35 μAdc @125°C; = 60 μAdc @ -55°C
H. I_{OH} = -150 μAdc @ 25°C; = -105 μAdc @125°C; = -185 μAdc @ -55°C
J. I_{OL} = 150 μAdc @ 25°C; = 105 μAdc @125°C; = 185 μAdc @ -55°C.
K. See figure B13 for test conditions and measurement points.
L. See figure B14 for test conditions and measurement points.
M. See figure B15 for test conditions and measurement points.
N. Each decoded output "0" through "9" shall be measured.
P. Load conditions: C_L = 50 pF, R_L = 200 kΩ.
R. Measurement frequency: 100 kHz≤fmx≤1.0 MHz.
S. Decoded outputs "1" through "9" shall be measured.
T. Decoded output "0" only shall be measured.

INPUTS				OUTPUTS			
Clock	Clock enable	Reset	D_{n-1}	Q_n	N_n	"O_n"	
X	H	L	X	Q_{n-1}	N_{n-1}	"O_n"$_{-1}$	(No change)
X	X	H	X	L	L	H	
↘	X	L	X	Q_{n-1}	N_{n-1}	"O_n"$_{-1}$	(No change)
↗	L	L	L	L	N-1_{n-1}	"9_n"$_{-1}$	
↗	L	L	H	H	N-1_{n-1}	"9_n"$_{-1}$	

On chip

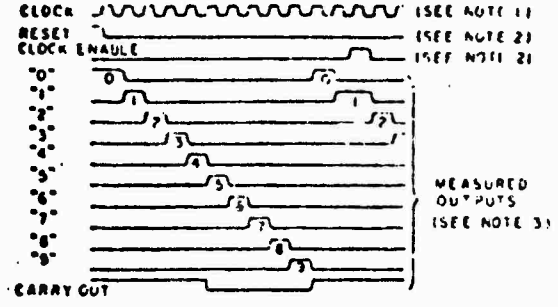
N = any decoded output, "1" through "9".

FIGURE B7. Truth Table



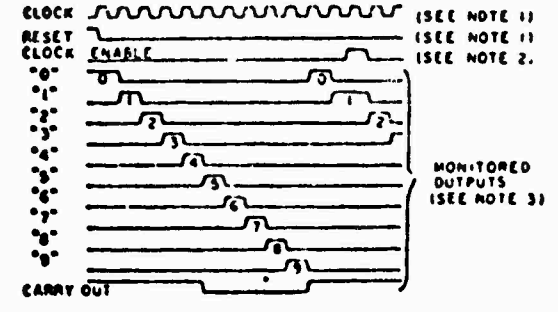
NOTES:
1. Clock input pulse conditions: V_{IH} = 14.5 V, V_{IL} = 0.5 V.
2. Reset and clock enable input pulse conditions: V_{IH} = 15 V, V_{IL} = 0 V.
3. See Table B4-3 tests 9 and 10, for output voltage levels (V_{OH2} and V_{OL2} respectively).

FIGURE B8. Timing diagram



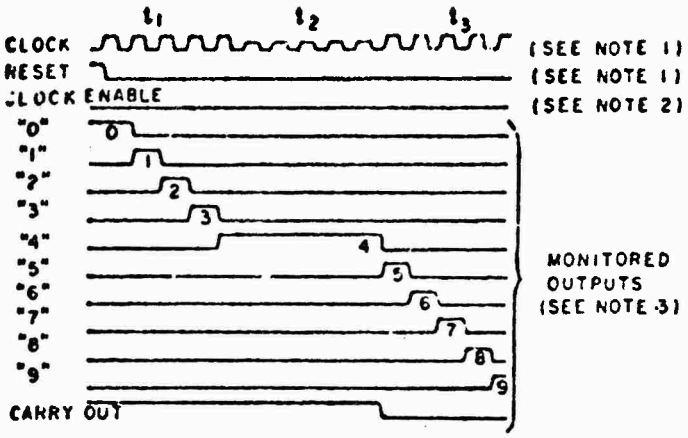
NOTES:
1. Clock input pulse conditions: V_{IH} = 4.5 V, V_{IL} = 0.5 V.
2. Reset and clock enable input pulse conditions: V_{IH} = 5.0 V, V_{IL} = 0 V.
3. See Table B4-3 tests 7 and 8, for output voltage levels (V_{OH1} and V_{OL1} respectively).

FIGURE B9. Timing diagram



NOTES:
1. Clock and reset input pulse conditions: V_{IH} = 5 V, V_{IL} = 0 V.
2. Clock enable input pulse conditions: V_{ICE} = 3.5 V at 25°C, 3.25 V at 125°C and 3.65 V at -55°C; V_{IL} = 1.5 V.
3. Monitor each output. Compliance established via no change in state of the observed output at -55°C ≤ T_A ≤ 125°C during clock enable duration while clocking. Acceptable output voltage levels from which to monitor a change or no change in state of the observed output shall be 4.95 V minimum for a "1" and 50 mV maximum for a "0".

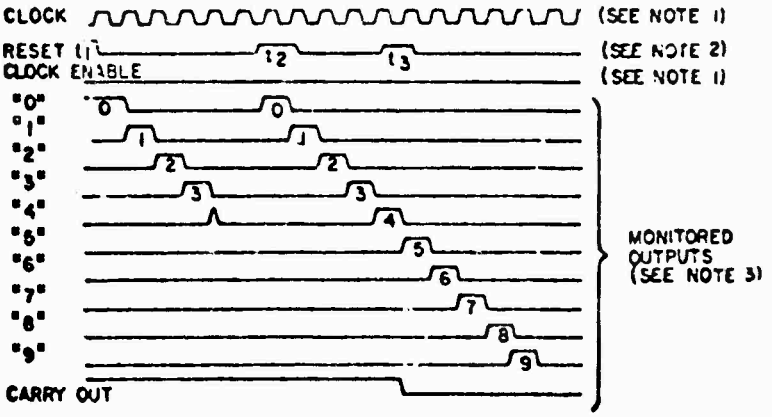
FIGURE B10. TIMING DIAGRAM



NOTES:

1. Clock input pulse conditions: V_{IH} = 3.5 V during t_1 and t_3, $V_{I\overline{CL}}$ = 1.5 V at 25°C, 1.25 V at 125°C and 1.75 V at -55°C during t_2 and V_{IL} = 0 V.
2. Reset and preset input pulse conditions: V_{IH} = 5.0 V, V_{IL} = 0 V.
3. Monitor each output. Compliance established via no change in state of the observed output while clocking at the t_2 voltage levels. Acceptable output voltage levels from which to monitor a change or no change in state of the observed output shall be 4.95 V minimum for a "1" and 50 mV maximum for a "0".

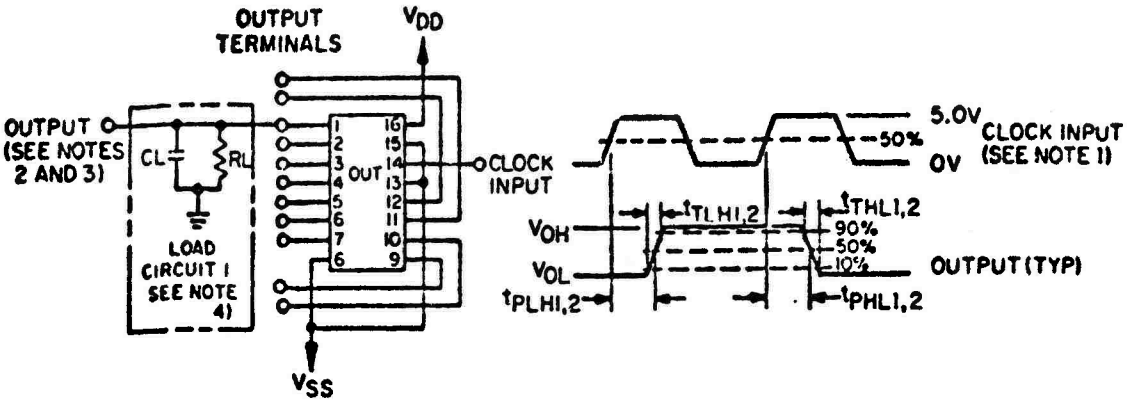
FIGURE B11. Timing diagram



NOTES:

1. Clock and clock enable input pulse conditions: V_{IH} = 5 V, V_{IL} = 0 V.
2. Reset input pulse conditions: V_{IH} = 5 V during t_1, $V_{I\overline{R}}$ = 3.5 V during t_2. $V_{I\overline{R}}$ = 1.5 V at 25°C, 1.25 V at 125°C and 1.75 at -55°C during t_3 and V_{IL} = 0 V.
3. Monitor each output. Compliance established via setting all outputs to the low level state at t_1, and t_2 and counting properly at all other times. The low level state shall be 50 mV maximum at $-55°C \leq T \leq 125°C$.

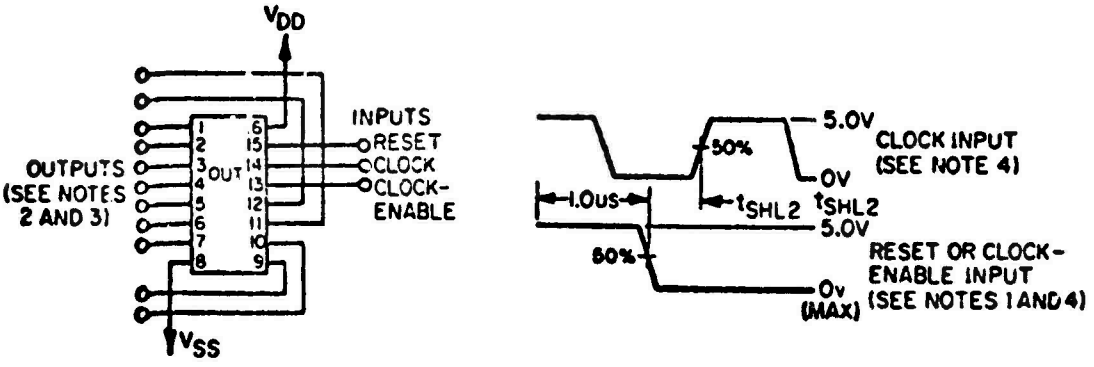
FIGURE B12. TIMING DIAGRAM



NOTES:

1. Clock input pulse conditions: 0 to 5ρ volt squarewave. f = 450 kHz @ 25° C and -55° C, = 350 kHz @ 125° C. tr and tf $\leq$ 15 ns; 50 percent duty cycle.
2. Connect each output terminal to a load circuit as shown.
3. Test each output separately.
4. Load conditions: C_L = 50 pF; R_L = 200k Ohms.

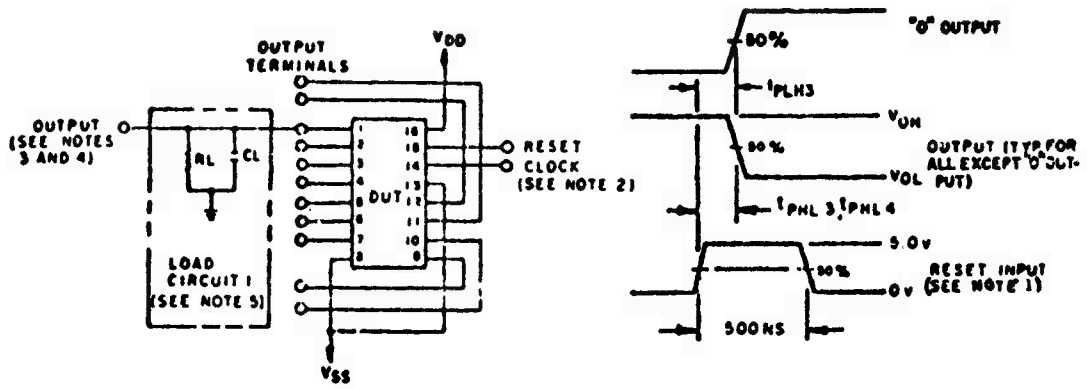
FIGURE B13. TRANSITION/PROPAGATION DELAY TIME TEST CIRCUIT AND WAVEFORM (CLOCK INPUT TO OUTPUTS).



NOTES:

1. When applying clock-enable input pulse connect reset input to V_{SS} then applying reset input pulse connect clock-enable input to V_{SS}.
2. During t_{SHL2} test, monitor output terminal 2 only; during t_{SHL1} test, monitor each output separately.
3. Compliance is established via a change of state at the examined output.
4. Clock input pulse conditions: 0 to 5.0 volt squarewave. f = 450 kHz @ 25° C and -55° C, = 350 kHz @ 125° C; tr and tf $\leq$ 15 ns; 50 percent duty cycle.

FIGURE B14. REMOVAL/SET-UP TIMES TEST CIRCUIT AND WAVEFORM (RESET AND CLOCK-ENABLE TO CLOCK INPUT).



NOTES:

1. Reset input pulse condition: tr and tf $\leq$ 30 ns.
2. Apply clock pulses until output under test is in the "1" state (high level output voltage state).
3. Connect each output terminal to a load circuit as shown.
4. Test each output separately.
5. Load conditions: C_L = 50 pF; R_L = 200k Ohms.

FIGURE B15. PROPAGATION DELAY TIMES TEST CIRCUIT AND WAVEFORM (RESET INPUT TO OUTPUTS).

APPENDIX C

PARAMETER CHARACTERIZATION

APPENDIX C
PARAMETER CHARACTERIZATION

Electrical parameter measurements were performed on all devices prior to the start of life test, during life test and at the conclusion of each life test. The initial and final data was summarized for each device life test and is shown in Tables C1 thru C24. A comparison was made to detect any shifts in parameter values which would have occurred during each accelerated life test.

A shift in the mean parameter value between the pre-life electrical test and the post-life electrical test was not unexpected for parameters which had a history of failures during the interim electrical tests since in many cases a particular failure mechanism will cause degradation of the same parameter in all the test devices. Also the sample size for the post-life test electrical tests has, in several cases, been notably reduced. No attempt was made to determine the mechanism(s) which caused shifts in parameter values which did not cause a device to fail an interim electrical test. Mechanisms for failed parameters are discussed in Appendix D.

Long term stability of the automated test equipment was verified by testing a control sample of each manufacturer's device prior to each interim electrical test. Where apparent shifts in parameters occurred which did not exhibit electrical test failures during interim tests, the data was compared to the control data to determine if the shift in data was due to test set drift or variations due to test set recalibration. There were no major shifts which could be attributed to parameter degradation which did not result in several devices failing that particular parameter.

TABLE C1. MANUFACTURER A MIL-M-38510/05202 (4001) LOT A 25°C PARAMETER CHARACTERIZATION

PARAMETER	LIMITS		INITIAL TEST		250°C LIFE TEST 4,000 HR DATA SAMPLE SIZE=11		225°C LIFE TEST 4,000 HR DATA SAMPLE SIZE=17		125°C LIFE TEST 6,000 HR DATA SAMPLE SIZE=20		125°C LIFE TEST 4,000 HR DATA SAMPLE SIZE=20		UNITS
	MIN	MAX	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	
V_{IC+}	-	1.5	0.808	0.009	0.814	0.024	0.841	0.036	0.819	0.018	0.808	0.006	V
V_{IC-}	-	-6.0	-2.314	0.082	-2.403	0.094	-2.411	0.105	-2.319	0.075	-2.332	0.078	V
I_{SS}	-	-1.0	-0.001	0.002	-0.006	0.009	-0.046	0.134	-0.001	0.001	-0.001	0.001	µA
V_{OL1}	-	0.4	0.200	0.017	0.198	0.018	0.197	0.021	0.193	0.013	0.194	0.013	V
V_{OL2}	-	0.05	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	V
V_{OL3}	-	1.5	0.001	0.001	0.001	0.001	0.001	0.000	0.001	0.001	0.001	0.001	V
V_{OH1}	4.6	-	4.928	0.000	4.924	0.017	4.926	0.016	4.929	0.022	4.928	0.022	V
V_{OH2}	4.95	-	5.000	0.000	5.000	0.000	5.000	0.022	5.000	0.027	5.000	0.028	V
V_{OH3}	13.5	-	14.998	0.170	14.999	0.030	14.999	0.043	14.999	0.044	14.999	0.036	V
I_{IH1}	-	0.1	0.000	0.000	0.003	0.010	0.000	0.000	0.000	0.000	0.000	0.000	µA
I_{IL1}	-0.1	-	-0.001	0.001	-0.004	0.011	-0.002	0.008	0.000	0.000	0.000	0.000	µA

TABLE C2. MANUFACTURER A MIL-M-38510/05202 (4001) LOT B 25°C PARAMETER CHARACTERIZATION

PARAMETER	LIMITS		INITIAL TEST		250°C LIFE TEST 500 HR DATA SAMPLE SIZE = 8		225°C LIFE TEST 2000 HR DATA SAMPLE SIZE = 7		125°C LIFE TEST 6000 HR DATA SAMPLE SIZE = 18		125°C LIFE TEST 4000 HR DATA SAMPLE SIZE = 19		UNITS
	MIN	MAX	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	
V_{IC^+}	-	1.5	0.808	0.009	0.802	0.005	0.803	0.005	0.849	0.061	0.813	0.006	V
V_{IC^-}	-	-6.0	-2.351	0.076	-2.369	0.068	-2.407	0.057	-2.358	0.074	-2.367	0.073	V
I_{SS}	-	-1.0	-0.002	0.006	-0.007	0.029	-0.012	0.024	-0.001	0.001	-0.002	0.001	μA
V_{OL1}	-	0.4	0.210	0.022	0.185	0.009	0.185	0.008	0.207	0.018	0.211	0.020	V
V_{OL2}	-	0.05	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	V
V_{OL3}	-	1.5	0.001	0.001	0.001	0.000	0.001	0.000	0.001	0.001	0.001	0.001	V
V_{OH1}	4.6	-	4.927	0.000	4.934	0.000	4.934	0.004	4.928	0.019	4.928	0.019	V
V_{OH2}	4.95	-	5.000	0.000	5.000	0.000	5.000	0.000	5.000	0.022	5.000	0.026	V
V_{OH3}	13.5	-	14.998	0.172	15.000	0.042	14.999	0.021	14.999	0.040	14.999	0.038	V
I_{IH1}	-	0.1	0.001	0.001	0.000	0.001	0.011	0.027	0.000	0.000	0.000	0.000	μA
I_{IL1}	-0.1	-	-0.001	0.004	-0.001	0.000	-0.002	0.001	0.000	0.000	0.000	0.000	μA

TABLE C3. MANUFACTURER A MIL-M-38510/05202 (4001) LOT C 25°C PARAMETER CHARACTERIZATION

PARAMETER	LIMITS		INITIAL TEST		250°C LIFE TEST 250 HR DATA SAMPLE SIZE=39		UNITS
	MIN	MAX	MEAN	SIGMA	MEAN	SIGMA	
V_{IC+}	-	1.5	0.806	0.008	0.805	0.005	V
V_{IC-}	-	-6.0	-2.353	0.081	-2.353	0.080	V
I_{SS}	-	-1.0	-0.001	0.001	0.007	0.008	µA
V_{OL1}	-	0.4	0.205	0.020	0.198	0.021	V
V_{OL2}	-	0.05	0.000	0.000	0.000	0.000	V
V_{OL3}	-	1.5	0.001	0.000	0.001	0.000	V
V_{OH1}	4.6	-	4.929	0.010	4.932	0.028	V
V_{OH2}	4.95	-	5.000	0.006	5.000	0.016	V
V_{OH3}	13.5	-	14.999	0.103	14.999	0.048	V
I_{IH1}	-	0.1	0.001	0.002	0.000	0.000	µA
I_{IL1}	-0.1	-	-0.001	0.002	0.000	0.000	µA
t_{PHL}	30	210	113.0	7.055	113.1	10.34	ns
t_{PLH}	30	210	113.4	6.360	111.0	6.069	ns
t_{THL}	40	300	85.25	6.190	85.68	10.22	ns
t_{TLH}	50	410	66.55	3.337	64.25	3.149	ns

TABLE C4. MANUFACTURER B MIL-M-38510/05202 (4001) LOT A 25°C PARAMETER CHARACTERIZATION

PARAMETER	LIMITS		INITIAL TEST		250°C LIFE TEST 250 HR DATA SAMPLE SIZE = 5		225°C LIFE TEST 500 HR DATA SAMPLE SIZE = 7		125°C LIFE TEST 6000 HR DATA SAMPLE SIZE = 20		125°C LIFE TEST 4000 HR DATA SAMPLE SIZE = 20		UNITS
	MIN	MAX	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	
V_{IC}^+	-	1.5	0.828	0.017	0.837	0.014	0.826	0.016	0.904	0.099	0.851	0.023	V
V_{IC}^-	-	-6.0	-1.234	0.464	-1.270	0.496	-1.256	0.486	-1.338	0.487	-1.245	0.462	V
I_{SS}	-	-1.0	-0.001	0.001	-0.352	0.222	-0.417	0.248	-0.150	0.178	-0.153	0.210	µA
V_{OL1}	-	0.4	0.154	0.015	0.158	0.013	0.137	0.016	0.156	0.014	0.157	0.014	V
V_{OL2}	-	0.05	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	V
V_{OL3}	-	1.5	0.001	0.000	0.001	0.000	0.001	0.001	0.001	0.000	0.001	0.001	V
V_{OH1}	4.6	-	4.927	0.000	4.926	0.006	4.929	0.000	4.929	0.015	4.928	0.018	V
V_{OH2}	4.95	-	5.000	0.000	5.000	0.000	5.000	0.000	5.000	0.021	5.000	0.025	V
V_{OH3}	13.5	-	14.994	0.139	14.996	0.025	14.995	0.029	14.995	0.038	14.995	0.041	V
I_{IH1}	-	0.1	0.000	0.000	0.001	0.001	0.004	0.007	0.000	0.000	0.000	0.000	µA
I_{IL1}	-0.1	-	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	µA

TABLE C5. MANUFACTURER B MIL-M-38510/05202 (4001) LOT B 25°C PARAMETER CHARACTERIZATION

PARAMETER	LIMITS		INITIAL TEST		250°C LIFE TEST 4000 HR DATA SAMPLE SIZE = 15		225°C LIFE TEST				125°C LIFE TEST				UNITS
							6000 HR DATA SAMPLE SIZE = 26		4000 HR DATA SAMPLE SIZE = 34		6000 HR DATA SAMPLE SIZE = 19		4000 HR DATA SAMPLE SIZE = 19		
	MIN	MAX	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	
V_{IC^+}	--	1.5	0.825	0.017	0.847	0.019	0.968	0.099	0.870	0.118	1.052	0.116	0.850	0.023	V
V_{IC^-}	--	-6.0	-1.169	0.393	-1.193	0.398	-1.344	0.409	-1.211	0.413	-1.411	0.402	-1.181	0.388	V
I_{SS}	--	-1.0	-0.002	0.012	-0.001	0.000	-0.070	0.158	-0.137	0.218	-0.013	0.025	-0.011	0.024	µA
V_{OL1}	--	0.4	0.165	0.000	0.198	0.016	0.174	0.016	0.175	0.015	0.163	0.012	0.164	0.012	V
V_{OL2}	--	0.05	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	V
V_{OL3}	--	1.5	0.001	0.000	0.001	0.000	0.001	0.000	0.001	0.000	0.001	0.000	0.001	0.000	V
V_{OH1}	4.6	--	4.919	0.000	4.920	0.011	4.922	0.024	4.920	0.026	4.923	0.021	4.923	0.018	V
V_{OH2}	4.95	--	5.000	0.000	5.000	0.017	5.000	0.033	5.000	0.036	5.000	0.024	5.000	0.026	V
V_{OH3}	13.5	--	14.995	0.143	14.997	0.041	14.997	0.036	14.997	0.037	14.996	0.042	14.997	0.036	V
I_{IH1}	--	0.1	0.000	0.000	0.000	0.000	0.005	0.016	0.000	0.000	0.000	0.000	0.001	0.005	µA
I_{IL1}	-0.1	--	0.000	0.000	0.000	0.000	-0.001	0.006	0.000	0.000	0.000	0.000	0.000	0.000	µA

TABLE C6. MANUFACTURER B MIL-M-38510/05202 (4001) LOT C 25°C PARAMETER CHARACTERIZATION

PARAMETER	LIMITS		INITIAL TEST		250°C LIFE TEST 250 HR DATA SAMPLE SIZE = 33		UNITS
	MIN	MAX	MEAN	SIGMA	MEAN	SIGMA	
V_{IC+}	-	1.5	0.823	0.015	0.823	0.014	V
V_{IC-}	-	-6.0	-1.183	0.409	-1.189	0.408	V
I_{SS}	-	-1.0	0.002	0.001	-0.011	0.022	µA
V_{OL1}	-	0.4	0.144	0.017	0.147	0.016	V
V_{OL2}	-	0.05	0.000	0.000	0.000	0.000	V
V_{OL3}	-	1.50	0.001	0.000	0.001	0.000	V
V_{OH1}	4.6	-	4.916	0.019	4.920	0.027	V
V_{OH2}	4.95	-	5.000	0.024	5.000	0.015	V
V_{OH3}	13.5	-	14.996	0.044	14.995	0.045	V
I_{IH1}	-	0.1	0.000	0.000	0.001	0.003	µA
I_{IL1}	-0.1	-	0.000	0.000	0.000	0.000	µA
t_{PHL}	30	210	59.64	6.369	59.37	6.055	ns
t_{PLH}	30	210	57.92	5.191	56.37	5.501	ns
t_{THL}	40	300	54.75	4.946	54.94	4.911	ns
t_{TLH}	50	410	65.83	4.421	64.44	4.366	ns

TABLE C7. MANUFACTURER B MIL-M-38510/05101 (4013) LOT A 25°C PARAMETER CHARACTERIZATION

PARAMETER	LIMITS		INITIAL TEST		250°C LIFE TEST				225°C LIFE TEST				125°C LIFE TEST				UNITS
					6000 HR DATA SAMPLE SIZE = 39		4000 HR DATA SAMPLE SIZE = 39		6000 HR DATA SAMPLE SIZE = 37		4000 HR DATA SAMPLE SIZE = 39		6000 HR DATA SAMPLE SIZE = 20		4000 HR DATA SAMPLE SIZE = 20		
	MIN	MAX	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	
V_{IC^+}	--	1.5	0.800	0.009	0.925	0.093	0.970	0.083	0.863	0.081	0.858	0.038	1.037	0.075	0.843	0.008	V
V_{IC^-}	--	-6.0	-1.803	0.037	-1.955	0.111	-2.010	0.112	-1.884	0.089	-1.856	0.097	-2.067	0.076	-1.856	0.026	V
I_{SS}	--	-1.0	-0.007	0.011	-0.010	0.013	-0.008	0.012	-0.009	0.013	-0.008	0.011	-0.031	0.100	-0.026	0.078	µA
V_{OL1}	--	0.4	0.134	0.013	0.140	0.014	0.144	0.014	0.140	0.016	0.138	0.015	0.132	0.011	0.134	0.011	V
V_{OL2}	--	0.5	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	V
V_{OL3}	--	1.5	0.001	0.000	0.001	0.000	0.000	0.000	0.000	0.000	0.001	0.000	0.001	0.000	0.000	0.000	V
V_{OH1}	4.66	--	4.921	0.000	4.920	0.026	4.918	0.028	4.920	0.025	4.921	0.027	4.921	0.020	4.919	0.024	V
V_{OH2}	4.95	--	5.000	0.014	5.000	0.037	5.000	0.038	5.000	0.037	5.000	0.038	5.000	0.028	5.000	0.028	V
V_{OH3}	13.5	--	14.998	0.163	14.999	0.028	14.999	0.038	14.999	0.042	14.999	0.037	14.999	0.048	14.999	0.025	V
I_{IL1}	-0.1	--	-0.002	0.000	-0.003	0.013	-0.003	0.011	-0.001	0.001	-0.001	0.007	0.000	0.000	0.000	0.000	µA
I_{IH1}	--	0.1	-0.000	0.000	0.000	0.002	-0.000	0.000	0.001	0.004	-0.000	0.000	0.000	0.000	0.000	0.000	µA

TABLE C8. MANUFACTURER B MIL-M-38510/05101 (4013) LOT B 25°C PARAMETER CHARACTERIZATION

PARAMETER	LIMITS		INITIAL TEST		250°C LIFE TEST				225°C LIFE TEST				125°C LIFE TEST				UNITS
					6000 HR DATA SAMPLE SIZE = 20		4000 HR DATA SAMPLE SIZE = 26		6000 HR DATA SAMPLE SIZE = 37		4000 HR DATA SAMPLE SIZE = 39		6000 HR DATA SAMPLE SIZE = 20		4000 HR DATA SAMPLE SIZE = 20		
	MIN	MAX	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	
V_{IC}^+	--	1.5	0.803	0.008	0.830	0.028	1.151	0.091	0.869	0.060	1.239	0.173	1.072	0.029	0.844	0.007	V
V_{IC}^-	--	-6.0	-1.644	0.050	-1.686	0.055	-2.029	0.109	-1.729	0.084	-2.141	0.183	-1.926	0.076	-1.704	0.046	V
I_{SS}	--	-1.0	-0.018	0.091	-0.102	0.246	-0.031	0.063	-0.017	0.033	-0.033	0.127	-0.009	0.012	-0.009	0.012	µA
V_{OL1}	--	0.4	0.098	0.008	0.095	0.007	0.097	0.007	0.106	0.011	0.102	0.009	0.101	0.009	0.102	0.009	V
V_{OL2}	--	0.5	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	V
V_{OL3}	--	1.5	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	V
V_{OH1}	4.6	--	4.923	0.000	4.917	0.023	4.915	0.025	4.914	0.028	4.914	0.030	4.920	0.022	4.919	0.021	V
V_{OH2}	4.95	--	5.000	0.000	5.000	0.027	5.000	0.033	5.000	0.037	5.000	0.034	5.000	0.028	5.000	0.028	V
V_{OH3}	13.5	--	14.998	0.166	15.000	0.046	14.999	0.037	14.999	0.030	15.000	0.049	14.999	0.026	14.999	0.049	V
I_{IL1}	-0.1	--	-0.001	0.003	-0.003	0.006	-0.001	0.003	0.000	0.001	-0.000	0.001	-0.001	0.005	-0.001	0.004	µA
I_{IH1}	--	0.1	0.000	0.001	0.000	0.001	0.000	0.001	0.000	0.000	-0.000	0.001	0.000	0.002	0.000	0.002	µA

TABLE C9. MANUFACTURER B MIL-M-38510/05101 (4013) LOT C 25°C PARAMETER CHARACTERIZATION

PARAMETER	LIMITS		INITIAL TEST		250° LIFE TEST 250 HR DATA SAMPLE SIZE = 26		UNITS
	MIN	MAX	MEAN	SIGMA	MEAN	SIGMA	
V_{IC+}	-	1.5	0.799	0.008	0.794	0.004	V
V_{IC-}	-	-6.0	-1.569	0.029	-1.572	0.022	V
I_{SS}	-	-1.0	-0.015	0.086	-0.053	0.101	μA
V_{OL1}	-	0.4	0.155	0.011	0.153	0.010	V
V_{OL2}	-	0.5	0.000	0.000	0.000	0.000	V
V_{OL3}	-	1.5	0.000	0.000	0.000	0.000	V
V_{OH1}	4.6	-	4.915	0.012	4.915	0.022	V
V_{OH2}	4.95	-	5.000	0.004	5.000	0.022	V
V_{OH3}	13.5	-	14.999	0.060	15.000	0.048	V
I_{IL1}	-0.1	-	-0.003	0.011	-0.002	0.004	μA
I_{IH1}	-	0.1	0.000	0.001	0.000	0.000	μA
t_{PHL}	70	500	114.4	24.87	114.7	21.30	ns
t_{PLH}	70	550	120.7	15.53	120.7	13.65	ns
t_{THL}	15	300	60.94	5.284	61.44	6.379	ns
t_{TLH}	15	350	68.01	3.204	69.79	3.478	ns
t_{P}	-	300	33.20	2.670	27.57	4.362	ns
t_{SHL}	-	150	27.61	1.376	35.90	2.954	ns
t_{SLH}	-	150	16.05	1.261	17.61	1.768	ns
t_{HHL}	-	150	-22.27	1.529	-30.53	3.171	ns
t_{HLH}	-	150	-1.962	1.224	-4.708	2.064	ns

TABLE C10. MANUFACTURER C MIL-M-38510/05101 (4013) LOT A 25°C PARAMETER CHARACTERIZATION

PARAMETER	LIMITS		INITIAL TEST		250°C LIFE TEST				225°C LIFE TEST		125°C LIFE TEST				UNITS
					6000 HR DATA SAMPLE SIZE = 20		4000 HR DATA SAMPLE SIZE = 26		4000 HR DATA SAMPLE SIZE = 26		6000 HR DATA SAMPLE SIZE = 19		4000 HR DATA SAMPLE SIZE = 19		
	MIN	MAX	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	
V_{IC}^+	--	1.5	0.809	0.010	0.838	0.017	1.113	0.134	0.841	0.031	0.951	0.051	0.868	0.050	V
V_{IC}^-	--	-6.0	-0.987	0.062	-1.046	0.125	-1.318	0.295	-1.022	0.069	-1.128	0.087	-1.036	0.078	V
I_{SS}	--	-1.0	-0.004	0.011	-0.007	0.024	-0.019	0.042	-0.021	0.035	-0.010	0.012	-0.010	0.012	µA
V_{OL1}	--	0.4	0.127	0.006	0.125	0.006	0.127	0.005	0.125	0.007	0.123	0.005	0.125	0.005	V
V_{OL2}	--	0.5	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	V
V_{OL3}	--	1.5	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	V
V_{OH1}	4.6	--	4.893	0.000	4.886	0.024	4.882	0.028	4.885	0.026	4.892	0.020	4.890	0.020	V
V_{OH2}	4.95	--	5.000	0.009	5.000	0.027	5.000	0.033	5.000	0.032	5.000	0.027	5.000	0.026	V
V_{OH3}	13.5	--	15.000	0.018	15.000	0.053	15.000	0.058	15.000	0.055	15.00	0.053	15.000	0.053	V
I_{IL1}	-0.1	--	-0.000	0.001	-0.001	0.007	-0.003	0.010	-0.009	0.016	-0.002	0.009	-0.001	0.002	µA
I_{IH1}	--	0.1	-0.000	0.001	0.001	0.004	0.006	0.020	0.000	0.001	0.000	0.000	0.000	0.000	µA

TABLE C11. MAN''FACTURER C MIL-M-38510/05101 (4013) LOT B 25°C PARAMETER CHARACTERIZATION

PARAMETER	LIMITS		INITIAL TEST		250°C LIFE TEST 4000 HR OATA SAMPLE SIZE = 5		225°C LIFE TEST 4000 HR OATA SAMPLE SIZE = 14		125°C LIFE TEST 6000 HR DATA SAMPLE SIZE = 14		125°C LIFE TEST 4000 HR DATA SAMPLE SIZE = 14		UNITS
	MIN	MAX	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	
V_{IC}^+	-	1.5	0.816	0.009	1.214	0.131	0.973	0.135	0.949	0.085	0.855	0.016	V
V_{IC}^-	-	-6.0	-1.006	0.072	-1.576	0.179	-1.233	0.170	-1.130	0.118	-1.040	0.072	V
I_{SS}	-	-1.0	-0.005	0.011	-0.217	0.279	-0.160	0.224	-0.011	0.016	-0.010	0.013	µA
V_{OL1}	-	0.4	0.164	0.006	0.168	0.008	0.165	0.008	0.164	0.004	0.166	0.004	V
V_{OL2}	-	0.5	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	V
V_{OL3}	-	1.5	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	V
V_{OH1}	4.6	-	4.873	0.000	4.862	0.020	4.861	0.022	4.876	0.011	4.874	0.012	V
V_{OH2}	4.95	-	5.000	0.012	5.000	0.004	5.000	0.012	5.000	0.015	5.000	0.012	V
V_{OH3}	13.5	-	15.000	0.040	15.000	0.033	15.000	0.052	15.00	0.055	15.000	0.055	V
I_{IL1}	-0.1	-	-0.000	0.000	-0.000	0.001	-0.015	0.026	0.000	0.000	0.000	0.000	µA
I_{IL1}	-	0.1	-0.000	0.000	0.018	0.025	0.031	0.033	0.000	0.000	0.000	0.000	µA

TABLE C12. MANUFACTURER C MIL-M-38510/05101 (4013) LOT C 25°C PARAMETER CHARACTERIZATION

PARAMETERS	LIMITS		INITIAL TEST		250°C LIFE TEST 250 HR DATA SAMPLE SIZE = 31		UNITS
	MIN	MAX	MEAN	SIGMA	MEAN	SIGMA	
V_{IC+}	-	1.5	0.811	0.010	0.817	0.007	V
V_{IC-}	-	-6.0	-0.995	0.066	-1.016	0.067	V
I_{SS}	-	-1.0	-0.005	0.010	-0.061	0.153	µA
V_{OL1}	-	0.4	0.162	0.007	0.158	0.006	V
V_{OL2}	-	0.5	0.000	0.000	-0.000	0.000	V
V_{OL3}	-	1.5	0.000	0.000	0.000	0.000	V
V_{OH1}	4.6	-	4.893	0.012	4.887	0.028	V
V_{OH2}	4.95	-	5.000	0.000	5.000	0.000	V
V_{OH3}	13.5	-	15.00	0.014	15.000	0.016	V
I_{IL1}	-0.1	-	-0.000	0.000	-0.002	0.009	µA
I_{IH1}	-	0.1	0.001	0.008	0.008	.021	µA
t_{PHL}	70	500	124.7	37.13	124.2	31.80	ns
t_{PLH}	70	550	149.4	16.38	149.3	21.27	ns
t_{THL}	15	300	83.03	8.491	83.30	9.197	ns
t_{TLH}	15	350	103.8	8.678	111.4	8.578	ns
t_{P}	-	300	79.88	4.577	78.76	4.166	ns
t_{SHL}	-	150	16.56	4.480	22.82	9.353	ns
t_{SLH}	-	150	18.29	3.372	13.97	2.467	ns
t_{HHL}	-	150	-11.10	1.323	-13.43	2.103	ns
t_{HLH}	-	150	4.726	1.152	5.794	1.207	ns

TABLE C13. MANUFACTURER C MIL-M-38510/05401 (4008) LOT A 25°C PARAMETER CHARACTERIZATION

PARAMETER	LIMITS		INITIAL TEST		250°C LIFE TEST 4000 HR DATA SAMPLE SIZE=18		225°C LIFE TEST 4000 HR DATA SAMPLE SIZE=25		125°C LIFE TEST 4000 HR DATA SAMPLE SIZE=18		UNITS
	MIN	MAX	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	
V_{IC^+}	-	1.5	0.824	0.011	1.230	0.232	0.849	0.045	0.939	0.170	V
V_{IC^-}	-	-6.0	-1.094	0.024	-1.558	0.223	-1.140	0.138	-1.200	0.182	V
I_{SS}	-	-10.0	-0.151	0.759	-1.167	2.196	-0.100	0.269	-0.460	1.187	µA
V_{OH1}	4.5	-	4.893	0.087	4.891	0.094	4.890	0.097	4.894	0.091	V
V_{OH2}	4.95	-	5.000	0.004	5.000	0.031	5.000	0.035	5.000	0.031	V
V_{OH3}	11.25	-	12.495	0.068	12.496	0.047	12.495	0.099	12.497	0.045	V
V_{OL1}	-	0.5	0.030	0.027	0.030	0.027	0.033	0.035	0.030	0.027	V
V_{OL2}	-	0.05	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	V
V_{OL3}	-	1.25	0.003	0.001	0.002	0.001	0.007	0.036	0.002	0.000	V
I_{IH1}	-	9.0	0.079	0.579	0.186	0.983	0.057	0.090	-0.006	0.178	nA
I_{IL1}	-	-9.0	-0.442	0.584	-0.964	1.430	-0.468	0.323	-1.152	1.312	nA

TABLE C14. MANUFACTURER C MIL-M-38510/05401 (4008) LOT B 25°C PARAMETER CHARACTERIZATION

PARAMETER	LIMITS		INITIAL TEST		250°C LIFE TEST 4000 HR DATA SAMPLE SIZE=26		225°C LIFE TEST 4000 HR DATA SAMPLE SIZE=31		125°C LIFE TEST 4000 HR DATA SAMPLE SIZE=19		UNITS
	MIN	MAX	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	
V_{IC^+}	-	1.5	0.825	0.009	0.865	0.026	0.966	0.167	1.069	0.251	V
V_{IC^-}	-	-6.0	-1.074	0.023	-1.125	0.033	-1.237	0.178	-1.378	0.051	V
I_{SS}	-	-10.0	0.000	0.017	-0.063	0.387	-0.006	0.016	-0.003	0.003	µA
V_{OH1}	4.5	-	4.997	0.000	4.872	0.112	4.878	0.105	4.882	0.101	V
V_{OH2}	4.95	-	5.000	0.000	5.000	0.037	5.000	0.031	5.000	0.014	V
V_{OH3}	11.25	-	12.492	0.138	12.490	0.101	12.492	0.105	12.493	0.076	V
V_{OL1}	-	0.5	0.000	0.002	0.020	0.018	0.020	0.018	0.020	0.018	V
V_{OL2}	-	0.05	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	V
V_{OL3}	-	1.25	0.005	0.028	0.006	0.005	0.005	0.001	0.004	0.001	V
I_{IH1}	-	9.0	-0.015	0.147	0.067	0.038	0.036	0.050	-0.106	0.024	nA
I_{IL1}	-	-9.0	-0.225	0.251	-0.486	1.559	-0.406	0.926	-0.212	0.093	nA

TABLE C15. MANUFACTURER C MIL-M-38510/05401 (4008) LOT C 25°C PARAMETER CHARACTERIZATION

PARAMETER	LIMITS		INITIAL TEST		250°C LIFE TEST 250 HR DATA SAMPLE SIZE = 39		UNITS
	MIN	MAX	MEAN	SIGMA	MEAN	SIGMA	
V_{IC+}	-	1.5	0.826	0.012	0.833	0.015	V
V_{IC-}	-	-6.0	-1.103	0.090	-1.124	0.102	V
I_{SS}	-	-10.0	-0.001	0.018	-0.006	0.017	μA
V_{OH1}	4.5	-	4.975	0.054	4.898	0.088	V
V_{OH2}	4.95	-	5.000	0.014	5.000	0.023	V
V_{OH3}	11.25	-	12.494	0.155	12.494	0.141	V
V_{OL1}	-	0.5	0.005	0.013	0.020	0.018	V
V_{OL2}	-	0.05	0.000	0.000	0.000	0.000	V
V_{OL3}	-	1.25	0.005	0.001	0.004	0.001	V
I_{IH1}	-	9.0	0.008	0.1 64	-0.052	0.091	nA
I_{IL1}	-	-9.0	-0.234	0.207	-0.187	0.075	nA
t_{PHL}	100	2250	155.4	20.18	123.1	17.29	ns
t_{PHL}	40	750	145.5	12.84	114.2	10.75	ns
t_{PHL}	20	300	78.60	7.651	63.00	5.379	ns
t_{PHL}	90	2900	159.2	29.12	132.4	22.66	ns
t_{PLH}	100	750	169.7	16.95	139.7	15.63	ns
t_{PLH}	20	300	76.47	8.234	71.73	8.897	ns
t_{PLH}	120	10,000	70.21	7.538	57.81	5.399	ns
t_{THL}	30	520	54.95	3.903	46.96	3.312	ns
t_{THL}	120	10,000	112.8	14.60	100.1	17.94	ns
t_{THL}	30	520	109.0	11.94	146.0	47.38	ns
t_{TLH}							

TABLE C16. MANUFACTURER D MIL-M-38510/05401 (4008) LOT A 25°C PARAMETER CHARACTERIZATION

PARAMETER	LIMITS		INITIAL TEST		250°C LIFE TEST 1000 HR DATA SAMPLE SIZE=1		225°C LIFE TEST 2000 HR DATA SAMPLE SIZE=10		125°C LIFE TEST 4000 HR DATA SAMPLE SIZE=19		UNITS
	MIN	MAX	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	
V_{IC^+}	-	1.5	0.757	0.009	0.760	0.006	0.835	0.090	0.781	0.095	V
V_{IC^-}	-	-6.0	-0.731	0.009	-0.749	0.027	-0.798	0.127	-0.742	0.055	V
I_{SS}	-	-10.0	-0.002	0.006	-2.071	1.992	-3.044	2.186	-0.003	0.002	μA
V_{OH1}	4.5	-	4.947	0.036	4.938	0.052	4.941	0.050	4.948	0.049	V
V_{OH2}	4.95	-	5.000	0.000	5.000	0.004	5.000	0.014	5.000	0.034	V
V_{OH3}	11.25	-	12.490	0.117	12.495	0.022	12.495	0.031	12.494	0.083	V
V_{OL1}	-	0.5	0.026	0.024	0.028	0.026	0.029	0.027	0.026	0.023	V
V_{OL2}	-	0.05	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	V
V_{OL3}	-	1.25	0.004	0.001	0.002	0.000	0.003	0.003	0.002	0.001	V
I_{IH1}	-	9.0	0.514	1.154	0.376	-	0.354	0.133	0.195	0.202	nA
I_{IL1}	-	-9.0	-0.040	0.013	-0.346	-	-0.499	1.370	-0.118		nA

TABLE C17. MANUFACTURER D MIL-M-38510/05401 (4008) LOT B 25°C PARAMETER CHARACTERIZATION

PARAMETER	LIMITS		INITIAL TEST		250°C LIFE TEST 500 HR DATA SAMPLE SIZE=3		225°C LIFE TEST 1000 HR DATA SAMPLE SIZE=30		125°C LIFE TEST 4000 HR DATA SAMPLE SIZE=20		UNITS
	MIN	MAX	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	
V_{IC^+}	-	1.5	0.753	0.009	0.756	0.006	0.782	0.027	0.900	0.210	V
V_{IC^-}	-	-6.0	-0.731	0.009	-0.739	0.005	-0.757	0.023	-0.896	0.223	V
I_{SS}	-	-10.0	-0.002	0.007	-1.709	2.300	-0.065	0.225	-0.063	0.352	µA
V_{OH1}	4.5	-	4.947	0.044	4.936	0.054	4.933	0.062	4.939	0.055	V
V_{OH2}	4.95	-	5.000	0.004	5.000	0.000	5.000	0.031	5.000	0.035	V
V_{OH3}	11.25	-	12.493	0.131	12.496	0.038	12.493	0.093	12.495	0.068	V
V_{OL1}	-	0.5	0.035	0.032	0.040	0.037	0.037	0.034	0.035	0.031	V
V_{OL2}	-	0.05	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	V
V_{OL3}	-	1.25	0.002	0.000	0.001	0.000	0.002	0.002	0.002	0.001	V
I_{IH1}	-	9.0	-0.030	0.051	0.047	0.036	0.105	0.171	-0.015	0.041	nA
I_{IL1}	-	-9.0	-0.079	0.029	-0.048	0.027	-0.036	0.009	-0.094	0.041	nA

TABLE C18. MANUFACTURER D MIL-M-38510/05401 (4008) LOT C 25°C PARAMETER CHARACTERIZATION

PARAMETER	LIMITS		INITIAL TEST		250°C LIFE TEST 250 HR DATA SAMPLE SIZE = 30		UNITS
	MIN	MAX	MEAN	SIGMA	MEAN	SIGMA	
V_{IC+}	-	1.5	0.755	0.009	0.758	0.010	V
V_{IC-}	-	-6.0	-0.732	0.015	-0.736	0.025	V
I_{SS}	-	-10.0	-0.043	0.443	-0.279	0.565	µA
V_{OH1}	4.5	-	4.948	0.041	4.943	0.054	V
V_{OH2}	4.95	-	5.000	0.010	5.000	0.033	V
V_{OH3}	11.25	-	12.490	0.120	12.495	0.074	V
V_{OL1}	-	0.5	0.026	0.023	0.030	0.028	V
V_{OL2}	-	0.05	0.000	0.000	0.000	0.000	V
V_{OL3}	-	1.25	0.003	0.001	0.002	0.002	V
I_{IH1}	-	9.0	0.240	0.831	0.005	0.161	nA
I_{IL1}	-	-9.0	-0.065	0.013	-0.297	0.646	nA
t_{PHL}	100	2250	187.7	59.98	161.2	51.66	ns
t_{PHL}	40	750	155.6	8.615	128.2	8.403	ns
t_{PHL}	20	300	83.54	4.459	68.34	4.062	ns
t_{PLH}	90	2900	186.9	60.82	166.8	41.73	ns
t_{PLH}	100	750	148.4	7.869	137.6	7.310	ns
t_{PLH}	20	300	79.92	3.806	74.44	5.397	ns
t_{THL}	120	10,000	76.81	4.467	75.74	12.21	ns
t_{THL}	30	520	61.51	2.454	54.288	2.309	ns
t_{TLH}	120	10,000	91.63	285.2	66.61	7.238	ns
t_{TLH}	30	520	69.60	4.368	69.42	6.722	ns

TABLE C19 . MANUFACTURER A MIL-M-38510/05601 (4017) LOT A 25°C PARAMETER CHARACTERIZATION

PARAMETER	LIMITS		INITIAL TEST		250°C LIFE TEST 3,000 HR DATA SAMPLE SIZE=18		225°C LIFE TEST 4,000 HR DATA SAMPLE SIZE=25		125°C LIFE TEST 4,000 HR DATA SAMPLE SIZE=18		UNITS
	MIN	MAX	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	
I_{IH}	-	-10.0	-1.361	1.055	-1.055	0.328	-1.059	0.469	-1.788	0.628	nA
I_{IL}	-	-10.0	-0.849	0.522	-1.080	0.195	-1.286	0.749	-1.906	0.611	nA
V_{OH1}	4.20	5.10	4.976	0.080	4.975	0.032	4.976	0.025	4.978	0.031	V
V_{HC1}	4.20	5.10	4.866	0.027	4.858	0.021	4.866	0.011	4.874	0.006	V
V_{OL1}	-0.01	0.50	0.020	0.003	0.027	0.022	0.023	0.016	0.020	0.002	V
V_{LC1}	-0.01	0.50	0.057	0.013	0.085	0.086	0.073	0.061	0.055	0.006	V
V_{OH2}	14.99	15.10	15.000	0.065	15.003	0.042	15.003	0.042	15.003	0.037	V
V_{HC2}	14.99	15.10	15.001	0.000	15.003	0.014	15.003	0.023	15.003	0.014	V
V_{OL2}	-0.01	0.01	0.003	0.002	0.001	0.001	0.001	0.001	0.003	0.001	V
V_{LC2}	-0.01	0.01	0.003	0.002	0.001	0.001	0.001	0.001	0.003	0.001	V
I_{SS}	-	-5.0	-0.188	0.533	-0.257	0.620	-0.106	0.376	-0.018	0.096	µA

PARAMETER	LIMITS		INITIAL TEST		250°C LIFE TEST 3000 HR DATA SAMPLE SIZE=36		225°C LIFE TEST 4000 HR DATA SAMPLE SIZE=32		125°C LIFE TEST 4000 HR DATA SAMPLE SIZE=20		UNITS
	MIN	MAX	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	
I_{IH}	-	-10.0	-0.854	1.147	-0.617	1.177	-0.716	0.916	-1.159	0.527	nA
I_{IL}	-	-10.0	-0.251	0.349	-0.799	0.261	-0.863	0.214	-1.032	0.303	nA
V_{OH1}	4.20	5.10	4.977	0.079	4.979	0.012	4.978	0.016	4.980	0.024	V
V_{HC1}	4.20	5.10	4.873	0.027	4.873	0.014	4.873	0.016	4.879	0.012	V
V_{OL1}	-0.01	0.50	0.018	0.002	0.018	0.005	0.017	0.002	0.019	0.002	V
V_{LC1}	-0.01	0.50	0.051	0.004	0.049	0.005	0.047	0.003	0.051	0.005	V
V_{OH2}	14.99	15.10	15.000	0.050	15.003	0.110	15.003	0.094	15.003	0.032	V
V_{HC2}	14.99	15.10	15.001	0.021	15.003	0.036	15.003	0.036	15.003	0.024	V
V_{OL2}	-0.01	0.01	0.001	0.001	0.001	0.001	0.000	0.001	0.003	0.001	V
V_{LC2}	-0.01	0.01	0.001	0.001	0.001	0.001	0.000	0.001	0.003	0.000	V
I_{SS}	-	-5.0	-0.050	0.004	0.004	0.148	-0.079	0.563	0.034	0.005	µA

TABLE C21. MANUFACTURER A MIL-M-38510/05601 (4017) LOT C 25°C PARAMETER CHARACTERIZATION

PARAMETER	LIMITS		INITIAL TEST		250°C LIFE TEST 250 HR DATA SAMPLE SIZE = 38		UNITS
	MIN	MAX	MEAN	SIGMA	MEAN	SIGMA	
I_{IH}	-	-10.0	-0.207	1.179	-1.864	0.295	nA
I_{IL}	-	-10.0	0.161	0.242	-1.967	0.266	nA
V_{OH1}	4.20	5.10	4.976	0.017	4.977	0.023	V
V_{HC1}	4.20	5.10	4.862	0.017	4.826	0.007	V
V_{OL1}	-0.01	0.50	0.021	0.002	0.021	0.001	V
V_{LC1}	-0.01	0.50	0.062	0.005	0.057	0.004	V
V_{OH2}	14.99	15.10	15.000	0.046	15.002	0.139	V
V_{HC2}	14.99	15.10	15.001	0.000	15.003	0.036	V
V_{OL2}	-0.01	0.01	0.003	0.000	0.002	0.001	V
V_{LC2}	-0.01	0.01	0.003	0.000	0.002	0.001	V
I_{SS}	-	-5.0	-0.053	0.013	-0.018	0.093	μA
t_{PHC}	-	1450	533	40	520.5	38.21	ns
t_{PHL}	-	1800	631	52	628.7	51.52	ns
t_{PLC}	-	1450	439	32	443.5	34.70	ns
t_{PLH}	-	1800	554	78	548.9	70.48	ns
t_{THC}	-	550	98	6	95.03	6.795	ns
t_{THL}	-	2250	147	12	145.3	15.87	ns
t_{TLC}	-	550	122	8	123.0	8.740	ns
t_{TLH}	-	2250	143	12	140.0	17.02	ns
t_{RHL}	-	1800	756	105	770.0	108.7	ns
t_{RLC}	-	1450	680	52	701.	55.63	ns
t_{RLH}	-	1800	719	54	753.0	56.53	ns

TABLE C22. MANUFACTURER D MIL-M-38510/05601 (4017) LOT A 25°C PARAMETER CHARACTERIZATION

PARAMETER	LIMITS		INITIAL TEST		250°C LIFE TEST 120 HR DATA SAMPLE SIZE=34		225°C LIFE TEST 1000 HR DATA SAMPLE SIZE=18		125°C LIFE TEST 4000 HR DATA SAMPLE SIZE=15		UNITS
	MIN	MAX	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	
I_{IH}	-	-10.0	-1.306	0.836	-1.087	0.544	-1.645	1.005	-1.390	0.537	nA
I_{IL}	-	-10.0	-0.460	0.241	-1.339	0.253	-2.247	0.482	-1.320	0.271	nA
V_{OH1}	4.20	5.10	4.839	0.076	4.843	0.012	4.844	0.028	4.843	0.028	V
V_{HC1}	4.20	5.10	4.836	0.027	4.828	0.000	4.825	0.010	4.838	0.007	V
V_{OL1}	-0.01	0.50	0.085	0.015	0.101	0.023	0.105	0.023	0.085	0.015	V
V_{LC1}	-0.01	0.50	0.180	0.005	0.180	0.003	0.182	0.004	0.182	0.006	V
V_{OH2}	14.99	15.10	15.000	0.072	15.002	0.090	15.003	0.044	15.004	0.039	V
V_{HC2}	14.99	15.10	15.001	0.013	15.002	0.020	15.003	0.029	15.004	0.024	V
V_{OL2}	-0.01	0.01	0.002	0.001	0.002	0.001	0.000	0.001	0.003	0.001	V
V_{LC2}	-0.01	0.01	0.001	0.001	0.002	0.001	0.000	0.000	0.002	0.001	V
I_{SS}	-	-5.0	-0.047	0.029	0.026	0.117	-0.547	0.908	0.039	0.003	µA

TABLE C23. MANUFACTURER D MIL-M-38510/05601 (4017) LOT B 25°C PARAMETER CHARACTERIZATION

PARAMETER	LIMITS		INITIAL TEST		250°C LIFE TEST 250 HR DATA SAMPLE SIZE=25		225°C LIFE TEST 1000 HR DATA SAMPLE SIZE=26		125°C LIFE TEST 4000 HR DATA SAMPLE SIZE=20		UNITS
	MIN	MAX	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	
I_{IH}	-	-10.0	-0.979	0.875	-0.918	0.605	-1.821	0.866	-1.100	0.571	nA
I_{IL}	-	-10.0	-0.181	0.423	-1.134	0.456	-2.205	0.489	-1.110	0.286	nA
V_{OH1}	4.20	5.10	4.872	0.069	4.870	0.030	4.867	0.031	4.874	0.021	V
V_{HC1}	4.20	5.10	4.865	0.025	4.856	0.012	4.854	0.015	4.867	0.008	V
V_{OL1}	-0.01	0.50	0.084	0.014	0.092	0.025	0.095	0.028	0.083	0.014	V
V_{LC1}	-0.01	0.50	0.172	0.005	0.168	0.006	0.169	0.004	0.171	0.004	V
V_{OH2}	14.99	15.10	14.999	0.112	15.001	0.000	15.003	0.047	15.004	0.040	V
V_{HC2}	14.99	15.10	15.000	0.037	15.001	0.020	15.003	0.030	15.004	0.026	V
V_{OL2}	-0.01	0.01	0.004	0.002	0.000	0.000	-0.001	0.000	0.003	0.001	V
V_{LC2}	-0.01	0.01	0.003	0.001	0.000	0.000	-0.001	0.000	0.003	0.001	V
I_{SS}	-	-5.0	-0.039	0.034	-0.436	0.677	-0.194	0.704	0.033	0.020	μA

TABLE C24. MANUFACTURER D MIL-M-38510/05601 (4017) LOT C 25°C PARAMETER CHARACTERIZATION

PARAMETER	LIMITS		INITIAL TEST		250° LIFE TEST 120 HR DATA SAMPLE SIZE = 40*		UNITS
	MIN	MAX	MEAN	SIGMA	MEAN	SIGMA	
I_{IH}	-	-10.0	-0.682	0.874	7.053	39.99	nA
I_{IL}	-	-10.0	0.072	0.415	-1.466	0.377	nA
V_{OH1}	4.20	5.10	4.774	0.000	3.999	1.640	V
V_{HC1}	4.20	5.10	4.768	0.023	0.605	5.978	V
V_{OL1}	-0.01	0.50	0.017	0.016	0.370	0.873	V
V_{LC1}	-0.01	0.50	0.203	0.004	0.459	0.977	V
V_{OH2}	14.99	15.10	14.999	0.123	14.262	2.661	V
V_{HC2}	14.99	15.10	14.999	0.050	14.008	0.586	V
V_{OL2}	-0.01	0.01	0.005	0.001	0.281	0.839	V
V_{LC2}	-0.01	0.01	0.005	0.001	0.351	2.215	V
I_{SS}	-	-5.0	-0.032	0.008	161.7	68.32	µA
t_{PHL1}	-	1450	456	24			ns
t_{PHL2}	-	1800	535	42			ns
t_{PLH1}	-	1450	418	20			ns
t_{PLH2}	-	1800	895	78			ns
t_{THC1}	-	550	224	8	TEST NOT PERFORMED		ns
t_{THL2}	-	2250	325	41			ns
t_{TLH1}	-	550	220	31			ns
t_{TLH2}	-	2250	1061	74			ns
t_{PHL3}	-	1800	536	40			ns
t_{PHL4}	-	1450	388	21			ns
t_{PHL5}	-	1800	856	60			ns

* SAMPLE SIZE INCLUDES 39 DEVICES THAT FAILED

APPENDIX D

FAILURE ANALYSIS

TABLE OF CONTENTS

1.0 INTRODUCTION

All parts that failed an electrical test during Step Stress, Lot Acceptance, and Life testing were analyzed to determine the particular failure mode, failure mechanism, and probable cause of failure. The general analysis procedure was as follows:

1) All failed parts were retested on the Automated Microcircuit Tester to verify their failure.
2) Room temperature failed parameters were confirmed using a curve tracer or, if necessary, a bench test set.
3) The failure was isolated to a specific stage, element, and junction to the extent possible via external pin-pin curve tracer measurements.
4) Failures were classified into subgroups on the basis of the analysis findings to this point.
5) A representative sample of parts (the smaller of five parts per lot or the entire subgroup) from each identifiable subgroup was subjected to detailed analysis.
6) Three parts or the excess number of parts over five in each subgroup per lot, whichever was less, were delivered to RADC.
7) The remaining samples from each subgroup were subjected to the following steps to confirm their categorization and to obtain any additional information:
   a) Unpowered Bake - Each part was subjected to an unpowered bake and retested. The exact time and temperature of the bake depended on the time and temperature at which the failure occurred. Usually, an overnight bake (16 hours) at the test temperature sufficed.
   b) Leak Tests - Each part was subjected to a helium bomb fine leak test and a fluorocarbon gross leak test.
   c) Delidding - Each part was delidded and subjected to routine optical examinations and documentations.

During this program, 981 failures occurred. A total of 679 failures were the result of excessive I_{SS} at 25°C caused by a reversible surface related

mechanism. Analysis of these 679 failures proved very difficult and time consuming. The I_{SS} failures in two device types (the Manufacturer B 4001 and Manufacturer D 4008) could not be classified into subgroups externally. In four device types, external troubleshooting of the I_{SS} failures indicated that 8 to 15 possible subgroups existed. The I_{SS} failures were usually caused by one or more leaky circuit transistors. The nature and location of the leakage was such that it could only be pin-pointed by die level probing. Because of the complexity of the devices and because in many instances the leakage was unstable (decaying with time), die level severing and probing was not undertaken unless methods of externally pin-pointing the leaky transistor or stage could be developed and a sufficient quantity of failed parts were available.

Due to the complexities and difficulties encountered in analysis of the 25°C failures, most of the parts that exhibited only +125°C or -55°C parametric failures were not analyzed in detail, but were baked and retested. Also, in the 4008 and 4017 device types, a few random failure types (those displayed by only one or two parts) were not investigated in detail in order to concentrate on the 25°C I_{SS} failures.

2.0 FAILURE ANALYSIS OVERVIEW

Summaries of the failure analysis results for each device type are contained in Tables D1 through D8. Each table contains a brief description of the failure symptoms, failure mode, failure mechanism, and cause of failure for each type of failure displayed by each device type during this program. The last column in each table lists the paragraph number of the analysis report that discusses each type of failure in detail. Certain types of failures contain no detailed discussion. Failure modes which are self-explanatory, such as pin broken off, inadvertent removal, retest OK, etc., are discussed in detail only the first time such modes appear on the tables. Also, the +125C°/ -55°C only failures and the 4008/4017 random failures that were not analyzed in detail are listed in the tables, but are not discussed further in the reports.

TABLE D1. MANUFACTURER A 4001B FAILURE ANALYSIS SUMMARY

A. FAILED PARAMETERS OR SYMPTOMS B. FAILURE MODE C. FAILURE MECHANISM D. CAUSE OF FAILURE	QUANTITY OF FAILURES BY FAILURE TIME (HOURS) AND TEST CELL										F/A PARA REF
	STEP STRESS			LOT ACCEPT LOT C	ACCELERATED LIFE						
					LOT A			LOT B			
	LOT A	LOT B	LOT C	250°C	250°C	225°C	125°C	250°C	225°C	125°C	
A. I_{SS} [19] B. Excessive I_{DSS} in N1 or N2 A ie N4 C. Cation Drift D. Cation Contamination in the Gate Oxide	3080H/275°C	3064H/250°C 3080H/275°C		10120 HRS	168 HRS 808 3016 6032 3064 20120 20250	104 HRS 1032 3064 50120 30250 10500 201000		304 HRS 608 5016 5032 4064 30120 40250 10500	3016 HRS 3032 3064 30120 60250 30600 201000	10120 HRS	3.1
A. I_{IH1} or I_{IL1} B. Degraded Input Protect Diode C. Charge Separation D. Mobile Ions in the Passivation								1064	101000 402000		3.2
A. I_{IH1} and I_{IL1} B. Pin-Pin Short in the Glass Seal C. Reduction and Precipitation of Pb D. Pb Glass					202000 104000	102000 204000			302000 204000		3.3
A. I_{IL1} B. Wire-Die Short C. Sagging or Flexing of Aluminum Wire D. Hillocks from Laser Scribe or Entrapped Particle					104	10120			102000 204000		3.4
A. I_{SS}, V_{OL} & V_{OH} B., C., & D. Not Determined	1010H/175°										3.5
A. Open Pin B. Open Aluminum Stripe C. Electromigration D. Excessive Drain Current						104000					3.5
A. I_{IH2} @ +125°C Only B. Not Determined (Recovered when left on Test) C. Not Determined D. Not Determined				40120							3.5
A. Open Circuits B. Broken Leads C. None D. Mishandling									10500	106000	3.6
A., B., & C. None D. Inadvertent Removal from Test						1032					3.6
A. V_{OL3} B. & C. None (Retest OK) D. Test Error						10500					3.6
TOTAL NUMBER OF FAILED PARTS	4	6	0	5	29	23	0	32	37	2	

TABLE D2. MANUFACTURER B 4001B FAILURE ANALYSIS SUMMARY

A. FAILED PARAMETERS OR SYMPTOMS B. FAILURE MODE C. FAILURE MECHANISM D. CAUSE OF FAILURE	QUANTITY OF FAILURES BY FAILURE TIME (HOURS) AND TEST CELL										F/A PARA REF
	STEP STRESS			LOT ACCEPT LOT C	ACCELERATED LIFE						
					LOT A			LOT B			
	LOT A	LOT B	LOT C	250°C	250°C	225°C	125°C	250°C	225°C	125°C	
A. I_{SS} [17] and/or I_{SS} [18] and/or I_{SS} [19] B. Not Determined C. Surface Instability D. Loss of Hermeticity	10275°C			20250 HRS	108 HRS 1016 1032 1064 40250	104 HRS 10120 69250		601000 HRS 302000 404000	101000 HRS 104000	102000	6.1
A. I_{ILI} and/or I_{IHI} B. Not Determined C. Surface Instability D. Loss of Hermeticity								104000	104000 606000 *206000		6.1
A. V_{IC} + B. Open Wire Bond C. Corrosion D. Loss of Hermeticity									206000		6.1
A. I_{SS} [17] and/or I_{SS} [18] and/or I_{SS} [19] B. Excessive I_{DSS} or Degraded P-Well Junction C. Cation Drift or Charge Separation D. Contamination in Passivation (All Parts were Hermetic)	20250°C 10175°C				604 208 3032 4064 30120 40250	508 1016 4064 40250 40500	102000 106000	20250 102000	1032 104000		6.2
A. I_{SS} [17] and/or I_{SS} [18] and/or I_{SS} [19] B. Excessive I_{DSS} or Degraded P-Well C. Cation Drift or Charge Separation D. Contamination or Loss of Hermeticity (These Parts were not Leak Tested)	10250°C				104 1016 20250	108 2016 1064 20120 10500	10500		101000	102000	6.2
A. Open and Shorted Pins B. Open Stripes and Shorted Junctions C. Aluminum Electromigration D. Open V_{SS} Connection on Program Board	10250°C		10275°C	40120 10250				10250 20500 202000 304000			6.3
A. Open Pin 4 and Pin 11 B. Melted Stripe C. Electrical Overstress D. Test Error			10275°C								6.3
A., B., & C. None D. Inadvertently Removed from Test					104						6.3
TOTAL NUMBER OF FAILED PARTS	6	0	2	7	35	33	3	25	16	1	

+125°C Only

TABLE D3. MANUFACTURER C 4013B FAILURE ANALYSIS SUMMARY

A. FAILED PARAMETERS OR SYMPTOMS B. FAILURE MODE C. FAILURE MECHANISM D. CAUSE OF FAILURE	QUANTITY OF FAILURES BY FAILURE TIME (HOURS) AND TEST CELL										F/A PARA REF
	STEP STRESS			LOT ACCEPT LOT C	ACCELERATED LIFE						
					LOT A			LOT B			
	LOT A	LOT B	LOT C	250°C	250°C	225°C	125°C	250°C	225°C	125°C	
A. I_{SS} [18] or I_{SS} [10] & [19] B. Excessive I_{DSS} in an N-Channel "ON" Transistor C. Cation Drift D. Cation Contamination in the Gate Oxide				4 @ 120 2 @ 250			1 @ 120	3 @ 4 1 @ 8 1 @ 120 1 @ 250 3 @ 500 3 @ 1000 6 @ 2000	3 @ 4 1 @ 1000 2 @ 2000 3 @ 4000	3 @ 120	5.1 5.1.1
A. I_{SS} [19] or I_{SS} [18] & [19] B. Excessive I_{DSS} in a P-Channel "ON" Transistor C. Cation Drift or Dipole Polarization D. Cations or Dipoles in the Oxide					1 @ 120 1 @ 250	1 @ 2000		1 @ 4 1 @ 64 1 @ 250	1 @ 250 1 @ 500 1 @ 1000 1 @ 2000 2 @ 4000	1 @ 1000	5.1 5.1.2
A. I_{SS} [17] and/or I_{SS} [18] and/or I_{SS} [19] B. Degraded Drain or P-Well Junction C. Charge Separation D. Ionic Contamination in the Passivation					2 @ 4 2 @ 64	2 @ 2000		1 @ 0 1 @ 1000 *1 @ 4000	1 @ 4 1 @ 64	1 @ 250	5.1 5.1.3
A. I_{SS} [17] and/or I_{SS} [10] and/or I_{SS} [19] B. Unknown (Recovered) C. Surface Instability D. Probably Ionic Contam.	1 @ 175°C 1 @ 250°C	2 @ 275°C			1 @ 4 1 @ 16 1 @ 2000 *1 @ 4000			1 @ 4	*2 @ 250		5.1 5.1.3
A. I_{IH1} B. Excessive I_{DSS} in N1 C. Cation Drift D. Cation Contamination in the Gate Oxide				1 @ 120 1 @ 250				1 @ 32 1 @ 250 1 @ 500 2 @ 1000 3 @ 2000 1 @ 4000	2 @ 250 3 @ 2000 2 @ 4000	1 @ 120	5.2
A. I_{IH1} B. Excessive I_{DSS} in P1 C. Cation Drift or Polarization D. Cations or Dipoles in the Oxide					1 @ 4 1 @ 6000						5.2
A. I_{IL1} B. Channeled Input Protect Diode C. Charge Separation D. Ionic Contamination in the Passivation						1 @ 120					5.5
A. I_{IL1} or I_{SS} B. Pin Shorted to Header C. P_b Reduction and Precipitation D. P_b Glass					1 @ 2000 1 @ 4000 2 @ 6000	5 @ 2000 3 @ 4000		1 @ 500	1 @ 4000		5.3
A. I_{IH1} and I_{SS} B. Degraded M15 C. Probably Al-Si Alloying D. Misregistered Ohmic Contact Window			2 @ 175°C								5.4
A. I_{IH1} B. Shorted Gate in N4 C. Dielectric Breakdown D. Probably a Transient or Static Discharge				1 @ 120							5.5
A. I_{IH1} B. Degraded Input Protect Diode C. Probably Electrical Overstress D. Not Determined					1 @ 6000						5.5
A. I_{IH1} B. Not Determined C. Not Determined D. Not Determined					1 @ 6000						5.5
A. V_{IC} + B. Damaged Ohmic Contact C. Electrical Overstress D. Not Determined					1 @ 2000						5.5
+125°C FAILURES - NOT ANALYZED IN DETAIL											
A. I_{IH}/I_{IL} @ +125°C Only - Bake Recovered					1 @ 4000	7 @ 4000					
TOTAL NUMBER OF FAILED PARTS	2	2	2	9	20	19	1	37	27	6	

*125°C Only

TABLE D4. MANUFACTURER B 4013B FAILURE ANALYSIS SUMMARY

A. FAILED PARAMETERS OR SYMPTOMS B. FAILURE MODE C. FAILURE MECHANISM D. CAUSE OF FAILURE	QUANTITY OF FAILURES BY FAILURE TIME (HOURS) AND TEST CELL										F/A PARA REF
	STEP STRESS			LOT ACCEPT LOT C	ACCELERATED LIFE						
					LOT A			LOT B			
	LOT A	LOT B	LOT C	250°C	250°C	225°C	125°C	250°C	225°C	125°C	
A. I_{SS} [17], [18], and [19] B. Excessive I_{DSS} in N20 or N22 C. Charge Accumulation in Gate Oxide D. Ionic Contamination and Possibly Moisture				8 @ 250				2 @ 4000 2 @ 6000			6.1 + 6.1.1
A. I_{SS} [17], [18], or [19] B. Not Determined C. Surface Instability (Bake Recoverable) D. Not Determined		1 @ 175° 1 @ 250°	1 @ 275°	2 @ 120 1 @ 250		1 @ 2000		1 @ 4 1 @ 1000 2 @ 2000 5 @ 4000 3 @ 6000			6.1 + 6.1.2
A. I_{SS} [17], [18], or [19] B. Not Determined C. Non Bake Recoverable D. Not Determined				1 @ 120	1 @ 250	1 @ 6000		2 @ 4 1 @ 4000	1 @ 64		6.1 + 6.1.2
A. I_{II} B. Channeled B3 C. Charge Separation D. Ionic Contamination in the Passivation						1 @ 6000					6.2
+125°C FAILURES NOT ANALYZED IN DETAIL											
A. I_{SS} [17] @ +125°C Only - Bake Recoverable				2 @ 120 1 @ 250				1 @ 4000	2 @ 4000		
TOTAL NUMBER OF FAILED PARTS	0	2	1	15	1	3	0	20	3	0	

TABLE D5 - MANUFACTURER D 4017 FAILURE ANALYSIS SUMMARY

A. FAILURE PARAMETER OR SYMPTOMS B. FAILURE MODE C. FAILURE MECHANISM D. CAUSE OF FAILURE	QUANTITY OF FAILURES AND TIME OF FAILURES (HOURS) BY TEST CELL										F/A PARA. REF
	STEP STRESS			LOT ACCEPT	ACCELERATED LIFE						
	LOT	LOT	LOT	LOT C	LOT A			LOT B			
	A	B	C	250°C	250°C	225°C	125°C	250°C	225°C	125°C	
A. I_{DSS} (Type 1) B. EXCESSIVE I_{DSS} IN N17 OR N20 C. CATION MIGRATION D. IONIC CONTAMINATION AND POSSIBLY MOISTURE			10200°C 70225°C 10250°C	390120				39500	*10250 ●10500		7.1 " 7.1.1
A. I_{SS} (Type 2) B. DEGRADED P26 DRAIN JUNCTION C. CHARGE SEPARATION D. IONIC CONTAMINATION IN THE PASSIVATION					1 864 1 0250 4 0500 *1 0500 ●5 0500	1 0500 ●2 0500 8 01000 14 02000		10120 20250 *10250 10500	802000		7,' " 7.1.2
A. I_{SS} (TYPE 3, 4, AND 5) B. NOT DETERMINED C. SURFACE INSTABILITY (BAKE RECOVERABLE) D. PROBABLY IONIC CONTAMINATION					104 10250 40500 ●20500	1864 *10500 101000		20250 *10250 40500 *10500	10120 1002000		7.1 " 7.1.3
A. I_{SS} (TYPE 6) B. PIN-PIN SHORTS C. NICKEL MIGRATION (DENDRITE GROWTH D. CHEMICAL RESIDUES					40500 ●80500			104 80500 *20500			7.1 " 7.1.4
A. I_{SS} (TYPES 7 THRU 15) B. NOT DETERMINED (NOT ANALYZED) C. SURFACE INSTABILITY (RECOVERED) D. PROBABLY IONIC CONTAMINATION					108 1016 30500	1 0120 ●1 0500 ●1 0100 4 02000		10250 20500	10500 502000		7.1 " 7.1.5
A. I_{IN} [1] B. DEGRADED D6 C. PROBABLY ALUMINUM-SILICON MIGRATION (ELECTRICAL OVERSTRESS) D. OPEN V_{SS} CHASSIS SOLDER JOINT	20250°C 20260°C				20120	20500		108 2064 30250	104 1864 20250 20500 201000		7.2
A. I_{IL} [4] B. CHANNELED D4-D5 C. CHARGE SEPARATION D. IONIC CONTAMINATION						10250			10250		7.3
A. V_{OH2} B & C NONE (RETEST OK) D. TEST ERROR					10250		1 02000				
A. I_{IL} AND I_{IH} B & C NONE (RETEST OK) D. TEST ERROR							2 02000				
RANDOM FAILURES AND +125°C/-55°C FAILURES - NOT ANALYZED IN DETAIL											
A. I_{SS} @+125°C ONLY - BAKE RECOVERABLE						10250			10250 202000		
A. V_{OH2} @+125°C ONLY - BAKE RECOVERABLE									102000		
A. I_{IL} [6] @ -55°C ONLY RECOVERED WHEN LEFT ON TEST							10250				
A. CATASTROPHIC							10120 104000				
A. COUNT STOPS AT "3"			10175°C								
A. T.T. AND V_{IH}						10500					
TOTAL NUMBER OF FAILED PARTS	4	0	10	39	40	40	6	38	40	0	

NOTES

* FAILED I_{SS}, V_{OH2} OR V_{OL2} @ +125° OR -55°C ONLY AT 120 HRS

● FAILED I_{SS}, V_{OH2} OR V_{OL2} @ +125° OR -55°C ONLY AT 250 HRS

TABLE D6. MANUFACTURER A 4017 FAILURE ANALYSIS SUMMARY

A. FAILED PARAMETERS OR SYMPTOMS B. FAILURE MODE C. FAILURE MECHANISM D. CAUSE OF FAILURE	QUANTITY OF FAILURES BY FAILURE TIME (HOURS) AND TEST CELL										FA PARA REF
	STEP STRESS			LOT ACCEPT LOT C	ACCELERATED LIFE						
					LOT A			LOT B			
	LOT A	LOT B	LOT C	250°C	250°C	225°C	125°C	250°C	225°C	125°C	
A. I_{SS}, I_{IL}, I_{IH}, or V_{OH2} B. Pin-Pin Short C. Pb Reduction and Precipitation (Dendrite Growth) D. Pb Glass					1 @ 1000 2 @ 2000 4 @ 3000	1 @ 250 1 @ 500 2 @ 2000 2 @ 4000		3 @ 3000	1 @ 1000 3 @ 2000 3 @ 4000		8.1
A. V_{OH2} B. Channeled N-Channel Output Transistor C. Cation Drift D. Cations in the Gate Oxide					1 @ 4 1 @ 500 2 @ 2000	1 @ 4 1 @ 8	1 @ 120		1 @ 4		8.2
A. I_{SS} B. Not Determined (Not Analyzed) C. Surface Instability (Bake Recoverable) D. Probably Ionic Contamination	1 @ 260°C			1 @ 120	1 @ 4 1 @ 120 2 @ 1000 1 @ 2000	1 @ 64 1 @ 250 1 @ 500 1 @ 1000 1 @ 2000	1 @ 120	1 @ 64			8.3
A. V_{OH2} Catastrophic B. and C. None (Retest OK) D. Test Error						1 @ 1000					
RANDOM FAILURES AND +12°C/-55°C FAILURES THAT WERE NOT ANALYZED IN DETAIL											
A. I_{SS} @ -55°C or +125°C Only - Bake Recovered					7 @ 120 2 @ 3000	2 @ 250 2 @ 4000		3 @ 120 1 @ 3000			
A. V_{OH2} @ -55°C or +125°C Only - Bake Recovered					1 @ 250 1 @ 3000						
A. Truth Table Errors				1 @ 120	1 @ 2000						
A. t_{SHL2}				1 @ 250							
TOTAL NUMBER OF FAILED PARTS	1	0	0	3	28	18	2	6	8	0	

TABLE D7. MANUFACTURER D 4008 FAILURE ANALYSIS SUMMARY

A. FAILED PARAMETERS OR SYMPTOMS B. FAILURE MODE C. FAILURE MECHANISM D. CAUSE OF FAILURE	QUANTITY OF FAILURES BY FAILURE TIME (HOURS) AND TEST CELL										F/A PARA REF
	STEP STRESS			LOT ACCEPT LOT C	ACCELERATED LIFE						
					LOT A			LOT B			
	LOT A	LOT B	LOT C	250°C	250°C	225°C	125°C	250°C	225°C	125°C	
A. I_{SS} B. Not Determined C. Surface Instability (Bake Recoverable) D. Probably Ionic Contamination				2@120	2@250 8@500 20@1000	1@64 5@1000 12@2000 10@4000		1@16 1@120 1@250 26@500	2@500 23@2000		9.1
A. I_{IH1} B. Degraded Input Protection Diode C. Electrical Overstress D. Excessive Forward Current due to Open Chassis Solder Joint		1@32H/200°C		1@120	1@120 1@250	1@32 1@500 1@1000 1@2000	1@4000	2@64 1@250	1@4 1@16 2@250 1@500		9.2
A. I_{IH1} or I_{IL1} B. Channeled Input Protection Diode C. Charge Separation D. Ionic Contamination				1@120 3@250	1@250 1@1000	1@120 1@1000		1@4 1@120	1@250 1@500 1@2000		9.3
A. V_{IC} * B. & C. None (Retest OK) D. Test Error						1@1000					
A. None B. None C. None D. Inadvertent Removal			1@48H/225°C								
+125°C/-55°C FAILURES THAT WERE NOT ANALYZED IN DETAIL											
A. I_{IH1} @ +125°C Only - Bake Recovered							6@4000			4@4000	
A. I_{SS} @ +125°C or -55°C Only - Bake Recovered				3@120 5@250	2@120 3@250 1@1000	2@120 3@250		2@120 1@250	3@120 4@2000	1@4000	
TOTAL NUMBER OF FAILED PARTS	0	1	1	15	40	40	7	37	40	5	

TABLE D8. MANUFACTURER C 4008 FAILURE ANALYSIS SUMMARY

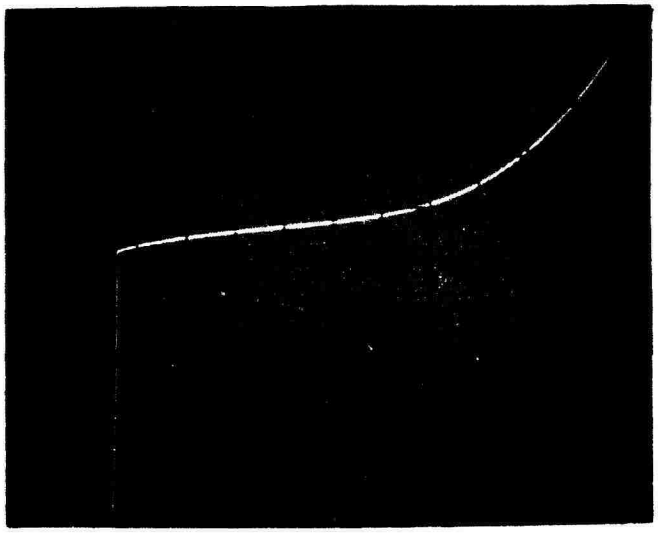
A. FAILED PARAMETERS OR SYMPTOMS B. FAILURE MODE C. FAILURE MECHANISM D. CAUSE OF FAILURE	QUANTITY OF FAILURES BY FAILURE TIME (HOURS) AND TEST CELL										FAILURE RATE
	STEP STRESS			LOT ACCEPT LOT C	ACCELERATED LIFE						
					LOT A			LOT B			
	LOT A	LOT B	LOT C	250°C	250°C	225°C	125°C	250°C	225°C	125°C	
A. I_{SS} B. Primarily Excessive I_{DSS} In an Off N-Channel Transistor C. Surface Instability (Bake Recoverable) D. Probably Ionic Contamination				1@250	2@1000 7@2000 9@4000	1@16 2@32 1@64 1@120 1@7000 1@4000	1@500	3@2000 2@4000	1@2000 2@4000		10.1
A. I_{IL1} or I_{SS} B. Pin-to-Header Short C. Pb Reduction & Precipitation D. Pb Glass					1@500	4@2000 3@4000		1@250 2@4000	1@1000 1@2000 2@4000		10.2
A. I_{IH1} or I_{IL1} B. Channeled Input Diode C. Charge Separation D. Ionic Contamination							1@4000			1@250	10.3
A. V_{IC} + B. & C. None (Retest OK) D. Test Error					1@1000						
A. I_{SS} @ 125°C & -55°C B. Open Pin 7 C. Broken Lead D. Mishandling						1@120					
A. None B. None C. None D. Inadvertently Removed from Test or Test Error	1@32H/200°C 1@64H/250°C							3@2000			
RANDOM FAILURES OR +125°C/-55°C FAILURES NOT ANALYZED IN DETAIL											
A. V_{OH3} and V_{OL3}								1@2000			
A. V_{OH3} @ -55°C Only - Bake Recovered									1@4000		
A. I_{SS} and I_{IL} at Pins 5 & 6 @ +125°C Only - Bake Recovered						1@4000					
A. [illegible] Only - Bake Recovered					3@1[illegible] [illegible]@4000	[illegible]@4000		1@120 1@4000	1@120 2@250		
[illegible] NUMBER OF FAILURES	2	0	0	1	[illegible]	18	2	14	11	1	

3.0 4001 QUAD TWO-INPUT NOR GATE - MANUFACTURER A

3.1 I_{SS} FAILURES - SURFACE INSTABILITY (CATION DRIFT)

One hundred-six parts (44 Lot A, 61 Lot B, 1 Lot C) failed due to excessive quiescent current, inputs low (I_{SS} [19]). The failed values ranged from 1.03 to 291 microamperes and all failures were bake recoverable, indicative of a surface instability mechanism.

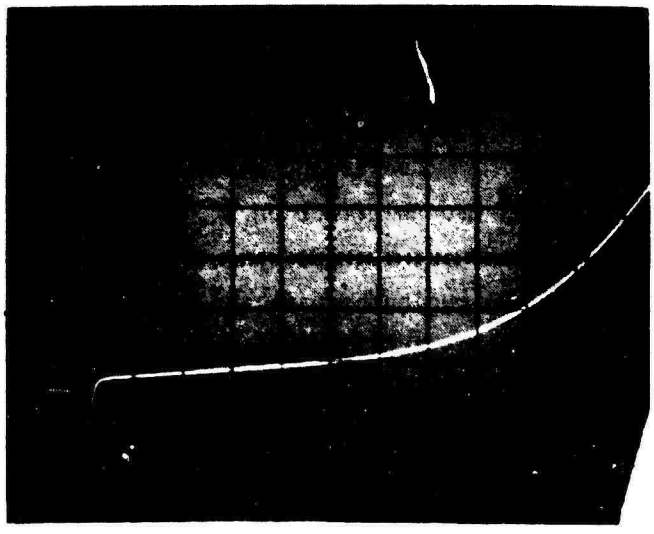
The excessive I_{SS} was traced to high I_{DSS} in two transistors of each NOR gate of the device. In each part, the N1 transistor of NOR gates A and C, the N2 transistors of NOR gates B and D, and the N4 output transistors of each NOR gate had degraded. For example, S/N A213 exhibited an I_{SS} value of 3100 nA (at V_{DD} = 15 V) after 64 hours in 250°C life, as shown in Figure D1. Each NOR gate in the part was contributing approximately 700 to 800 nA of leakage. The N1-N2 transistor pair of NOR gate A was isolated from the rest of the circuit and measured. I_{DSS} of the pair was 350 nA at V_{DS} =15V and the I_{DSS} vs. V_{DS} characteristic was channeled, as shown in Figure D2. Because the two transistors shared a common drain diffusion and because their sources were shorted together via an n+ diffusion, the individual I_{DSS}'s of each transistor could not be measured directly. However, the leakage could be isolated to a specific transistor by isolating the gate terminals and applying a negative voltage to each gate in turn. A V_{GS} of -4 VDC applied to N1 (with V_{GS} =0V on N2) pinched off the leakage to zero nanoamperes, whereas -4 VDC applied to the gate of N2 had no effect on I_{DSS} of the pair. This established that N1 of the pair was degraded and that the anomalous current was caused by inversion of the region beneath the gate stripe. Examination of the threshold voltage characteristics of each transistor, shown in Figure D3, disclosed that the threshold voltage of N1 was low compared to that of N2. This indicated that the inversion was located in the channel region of the N1 transistor. Further investigation of S/N A213 disclosed degradation in the N1 transistor of gate C, the N2 transistor of gate B, the N2 transistor of gate D, and the N4 transistor of each gate simular to that displayed by N1 of gate A. A 16 hour, 250°C bake of the part caused the degraded transistors to



I_{SS} = 500 nA/DIV.

V_{DD} = 2 VOLTS/DIV. S/N A213(64 HRS/250°C)

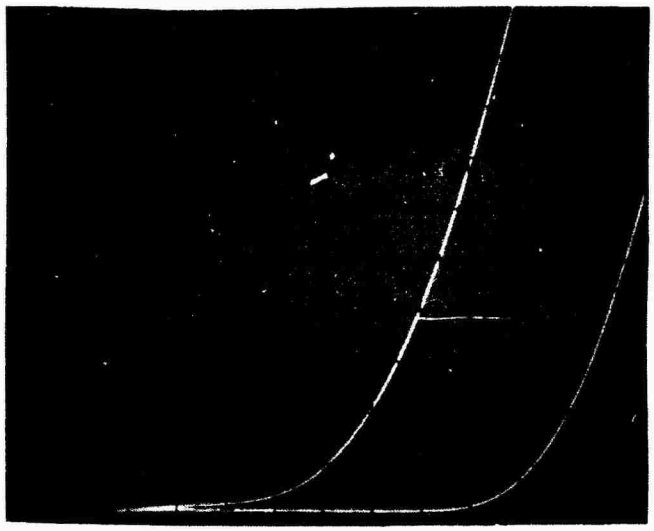
FIGURE D1 - $I_{SS[19]}$ I-V CHARACTERISTIC OF S/N A213.



I_{DSS} = 100 nA/DIV.

V_{DS} = 2 VOLTS/DIV. S/N A213(64HRS/250°C)

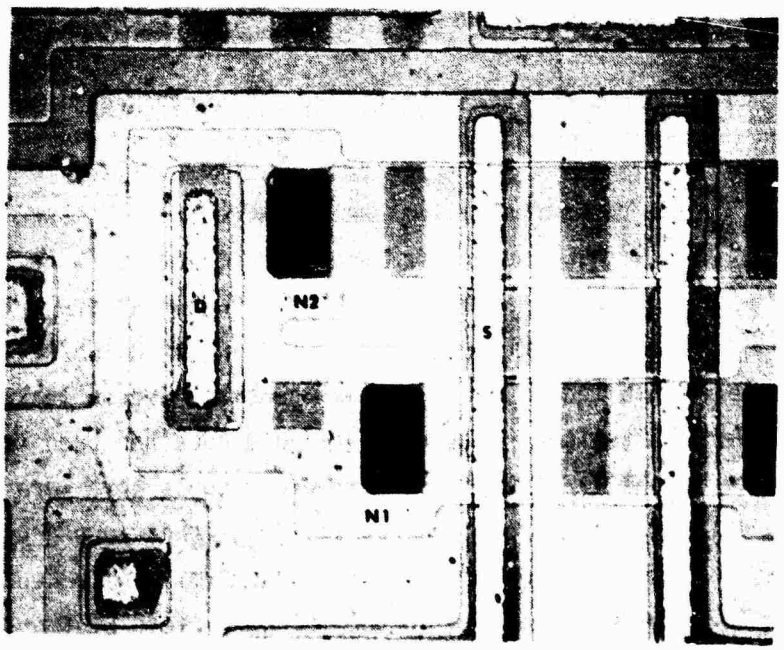
FIGURE D2 - I_{DSS} I-V CHARACTERISTIC OF THE GATE A N1-N2 TRANSISTOR PAIR OF S/N A213.



I_D = 2 μA/DIV.

V_{DS} = 0.2 VOLTS/DIV. S/N 213(64HRS/250°C)

FIGURE D3 - THRESHOLD VOLTAGE CHARACTERISTICS OF N1 (L/H) AND N2 (R/H) OF GATE A OF S/N A213. V_{TH} CHARACTERISTIC = I_{DS} VS. V_{DS} WITH V_{GS} = V_{DS}.



630X S/N B223 (16 HRS/225°C)

FIGURE D4 - EXAMPLE OF A GATE A N1 TRANSISTOR (DEGRADED) AND N2 TRANSISTOR (NORMAL) AFTER METALLIZATION REMOVAL.

recover and microscopic examination of the transistors before and after removal of the metallization disclosed no visible anomalies. A typical gate A, N1-N2 transistor pair of a failed device after removal of the metallization is shown in Figure D4.

During step-stress and life test of the 4001, input pins 1, 5, 8, and 12 were biased high and input pins 2, 6, 9, and 13 were biased low. This applied +15 VDC across the gate oxide of the N1 transistors of gates A and C and the N2 transistors of gates B and D. The output of each gate was low, thus, each N4 output transistor also had had +15 VDC across its gate oxide. Therefore, it was concluded that the gate oxide of the transistors contained cation contamination, probably sodium ions. In the transistors with a positive field across the gate oxide, the cations drifted to the Si/SiO_2 interface. The accumulation of positive charge at the interface inverted the underlying p-type channel region causing an increase in I_{DSS} and a reduction of the threshold voltage. During the I_{SS} [19] test, all eight affected n-channel transistors are in the off state, consequently, the measured value is the sum of all eight I_{DSS} currents.

3.2 I_{IH}/I_{IL} FAILURES - SURFACE INSTABILITY (CHARGE SEPARATION)

Three parts failed due to excessive I_{IH1}, one part failed due to excessive I_{IL1}, and two parts failed due to excessive I_{IH1} and I_{IL1} during accelerated life. The I_{IH} failures were traced to a degraded input-to-V_{SS} protection diode (D3 or D6) and the I_{IL} failures were traced to a degraded input-to-V_{DD} protection network (D1/D2/R1 or D4/D5/R2). The degraded diodes exhibited channeled or exponential reverse leakage and the leakage recovered after baking. The degraded diodes had been reverse biased during life test (the I_{IH} failures occurred at inputs that were connected to +15 volts and the I_{IL} failures occurred at inputs that were grounded during life). Thus, the degradation probably was caused by mobile ions in or on a passivation layer which separated in the fringing field of the reverse biased junction and inverted the underlying silicon.

3.3 $I_{IH}/I_{IL}/I_{SS}$ FAILURES - PIN-PIN SHORTS (LEAD PRECIPITATION)

Eleven parts (6 Lot A and 5 Lot B) failed I_{IH}, I_{IL}, and I_{SS} [17] or I_{SS}[18] during accelerated life. Each failure was caused by a high resistance (kilohm) short between one input pin and its respective output pin. Due to the short, the input pin was connected to an "on" transistor of the output stage during measurement of I_{IL1}, I_{IH1}, or I_{SS} [17] or I_{SS} [18]. This resulted in excessive I_{IH} and I_{IL} current at the input, as shown in Figure D5a and D5b and excessive I_{SS} [17] or I_{SS} [18] current (depending on which input was shorted) as shown in Figures D5c and D5d. Two parts contained a short between pin 2 (input) and pin 3 (output), two parts contained a short between pin 5 (input) and pin 4 (output), one part contained a short between pin 12 (input) and pin 11 (output), and three parts contained a short between pin 13 (input) and pin 11. The exact location of the short in three parts was unknown because the short had cleared prior to analysis.

The shorts were traced to conductive paths in the glass frit used to seal the package. Each part contained grey deposits on the exterior of the glass seal and discoloration of the tin-plated external leads, as illustrated in Figure D6. These conditions were not present in unstressed parts, but removal of the grey deposits did not cure the shorts. Cross-sections of the packages revealed dark stains in the glass emanating from the internal lead frame members, as illustrated in Figure D7. The leads that were shorted together always contained a bridging trail of stain between the leads. Under SEM examination, the stain appeared to be a dendrite growth, as shown in Figure D8. The largest concentration of growth always occurred at the package leads that were most negatively biased (grounded inputs or low outputs) indicating a probable electrolytic reaction. SEM X-ray analysis of the glass disclosed that it contained lead (Pb) and zinc (Zn) indicating that it probably was a PbO - ZnO- B_2O_3 glass. These findings indicate that the growth most likely was caused by reduction of lead-oxide in the glass and precipitation of Pb (a positive ion) in the vicinity of the negatively biased package leads. The package contains two lead (Pb) reducing agents, the aluminum plating on the internal portion of the lead frame and the tin plating on the external

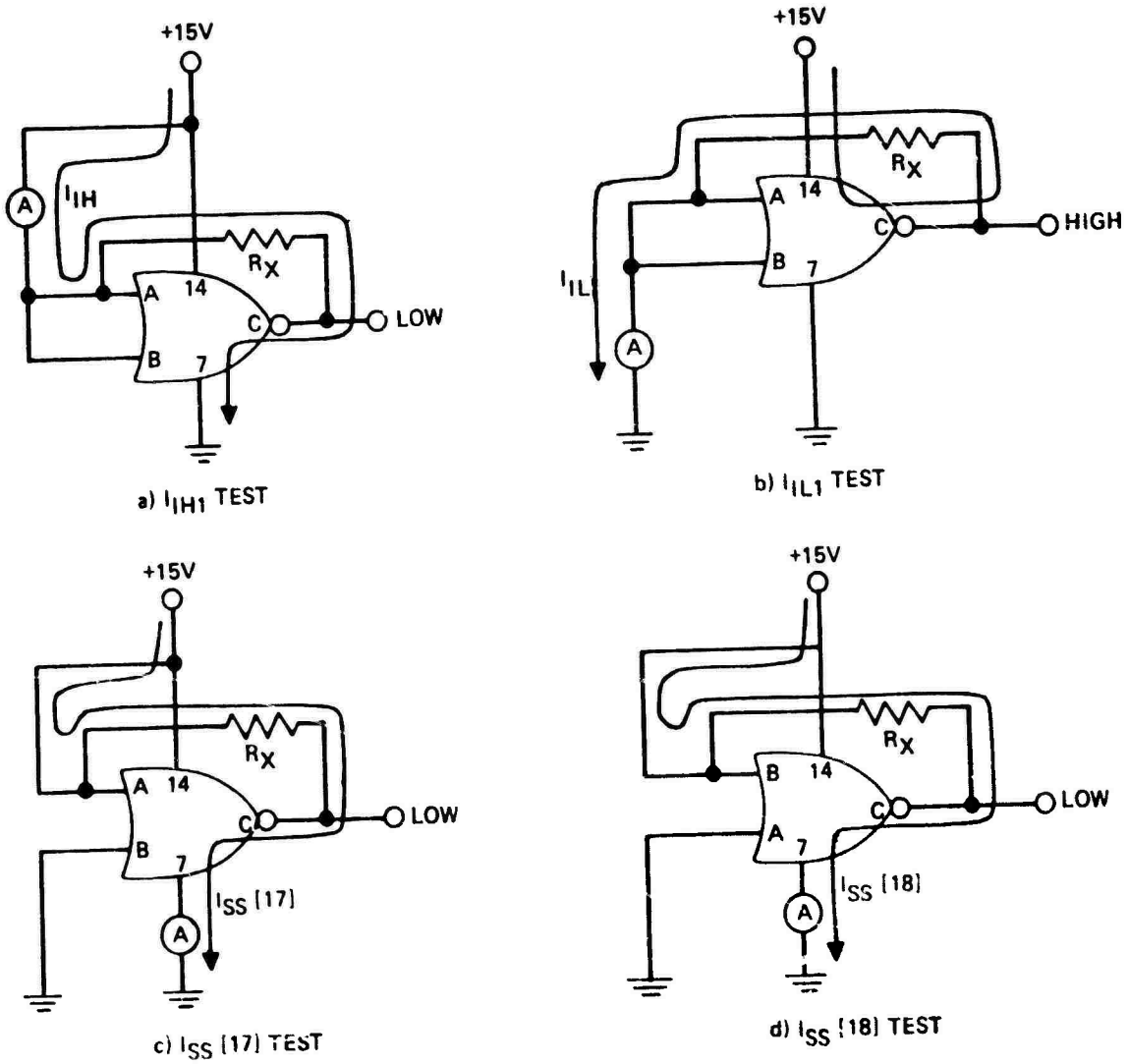
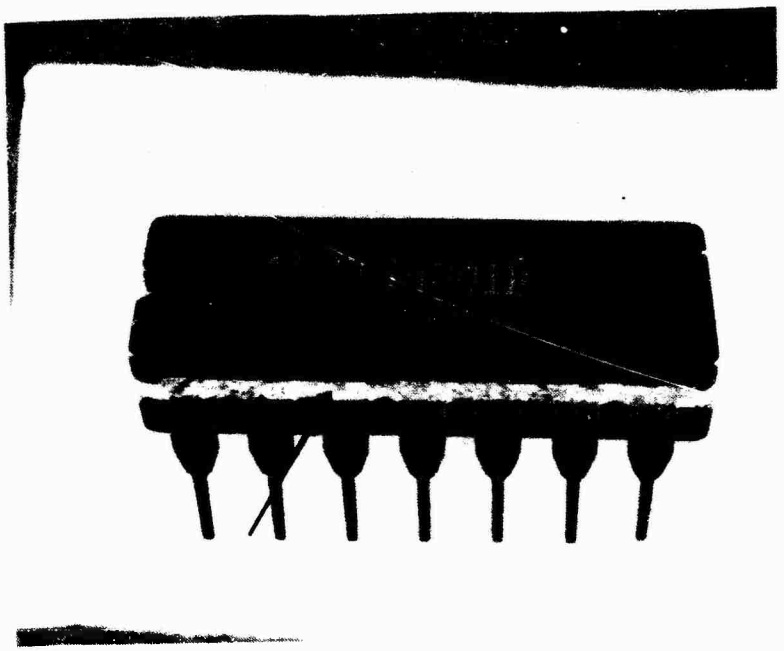
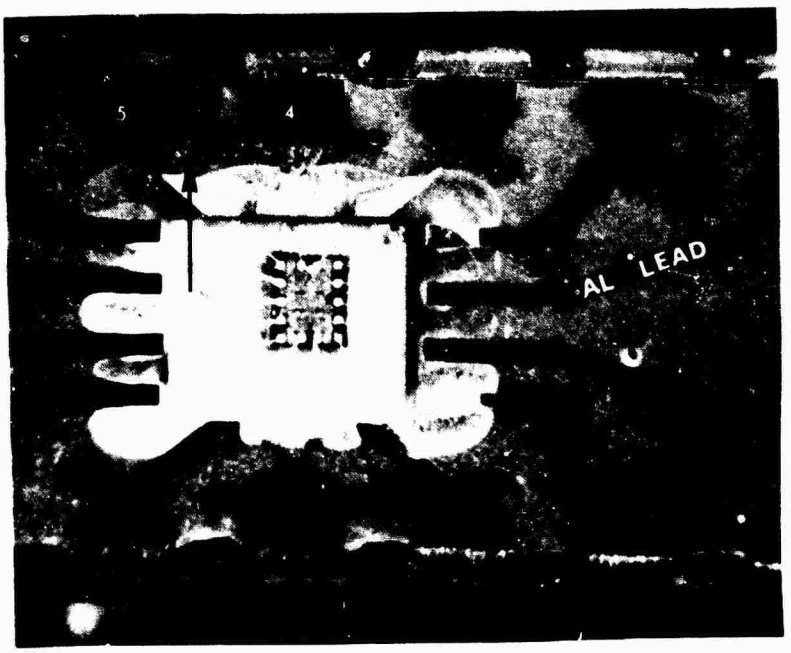


FIGURE D5. DIAGRAM OF ONE GATE SHOWING THE PATH OF THE EXCESSIVE CURRENT DURING EACH LEAKAGE CURRENT TEST AFFECTED BY AN INPUT TO OUTPUT SHORT (R_X)



4X S/N A242 (2000 HRS/250°C)

FIGURE D6 - GREY DEPOSITS (ARROW) ON THE GLASS FRIT AND DISCOLORED LEADS TYPICAL OF THE PARTS WITH SHORTED PINS.



10X S/N A242 (2000 HRS/250°C)

FIGURE D7 - CROSS-SECTION OF THE PACKAGE SHOWING DARK STAIN AROUND THE LEADS. THIS PART CONTAINED A SHORT BETWEEN PINS 4 AND 5 AND HAS A BRIDGING STAIN (ARROW) BETWEEN PINS 4 AND 5.

24X S/N A135 (4000 HRS/225°C)

FIGURE D8 - SEM PHOTO OF THE STAIN.

250X (SEM-1.3 K.V.) S/N A225 (4 HRS/250°C)

FIGURE D9 - EXAMPLE OF SILICON LASER SCRIBE HILLOCK (ARROW) AT THE FAILURE SITE EXPOSED BY LIFTING THE ALUMINUM WIRE.

portion of the lead frame; however, no obvious reducing medium (electrolyte) was found. The electrolyte may have been simply trace amounts of moisture entrapped in the glass.

3.4 I_{IL} FAILURES - WIRE-TO-DIE SHORTS

Two Lot A and three Lot B parts failed due to excessive I_{IL1} ranging from 350 nA to 1400 nA (maximum measurement capability) during accelerated life test. In each instance, the leakage was caused by a high resistance short (0.5 to 43 megohms) between an input pin and V_{DD}. The shorts were traced to contact between the aluminum interconnect wire and the edge of the silicon die (which is connected to V_{DD}).

In four of these parts, the aluminum wire shorted to a hillock of melted silicon from the laser scribe operation. Figure D9 shows an example of a hillock, exposed by bending back the aluminum wire. This hillock protruded eight microns above the die surface. Figure D10 shows the hillock from another view and indicates the point of contact on the wire.

In one part, the wire was shorted to the unpassivated kerf area of the die. Lifting the wire cleared the short and exposed a residue at the point of contact in the kerf, as shown in Figure D11. This indicated that the wire had shorted to some entrapped particulate matter.

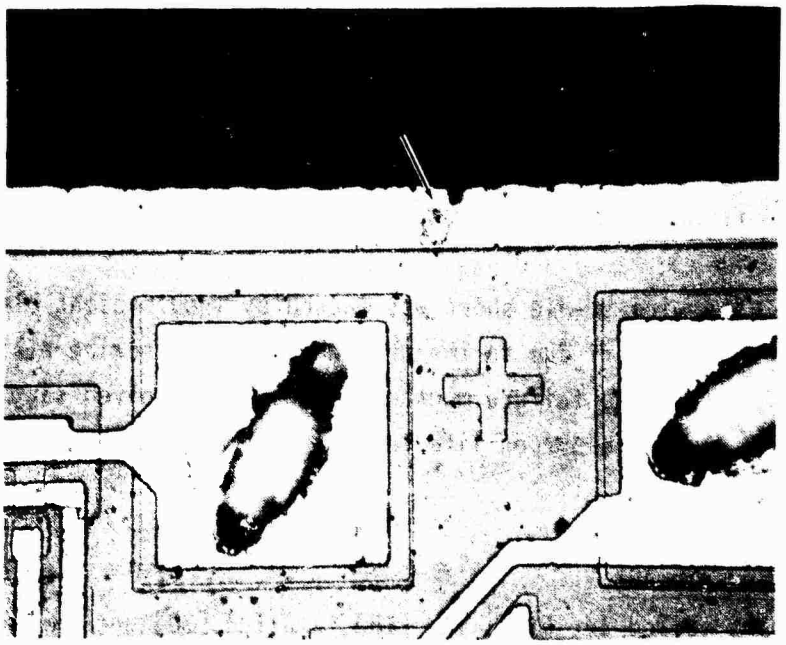
In each case, the wire-to-die short was caused by insufficient clearance between the wire and the kerf due to the presence of laser-scribe hillocks or a contaminant particle. The failure mechanism probably involved sagging or flexing of the aluminum wire during life test until the wire contacted the hillock or particle.

3.5 MISCELLANEOUS FAILURES

One Lot A part failed I_{SS} [17], I_{SS} [18], and I_{SS} [19] and V_{OL}'s and V_{OH}'s at pin 4 after the 16 hour, 175°C step during step-stress. The failures were caused by a condition in gate A that caused the n-channel and

850X (SEM-1.3 K.V.) S/N A225 (4 HRS/250°C)

FIGURE D10 - CONTACT SITE (AFTER LIFTING THE WIRE) SHOWING THE SILICON LASER SCRIBE HILLOCK (ARROW #1) AND Si-Al RESIDUE ON THE WIRE (ARROW #2).



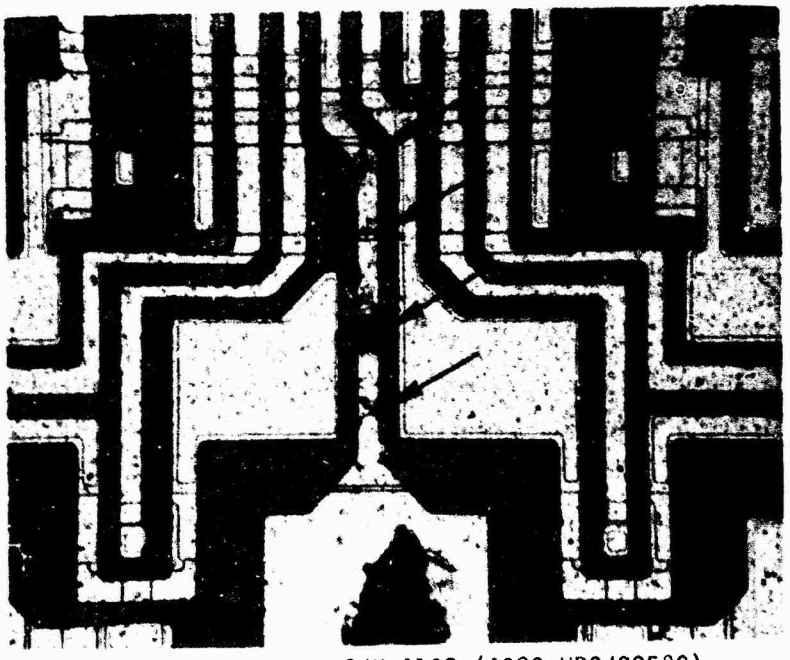
256X S/N B251 (4000 HRS/225°C)

FIGURE D11 - RESIDUE IN THE KERF (ARROW) AT THE POINT OF THE SHORT (AFTER REMOVING THE WIRE).

the p-channel transistor of the output stage (N4 and P4) to both conduct simultaneously during the parameter measurements. A 16 hour, 250°C bake did not improve the condition. Delidding the part and removal of the glassivation did not affect the failure mode, but when the output stage was probed, the part completely recovered. Examinations of the output stage disclosed no explanation for the failure and the failure could not be re-induced. No similar failure occurred during accelerated life. Consequently, the cause of this failure was not determined.

One Lot A part failed due to an open pin 7 (V_{SS}) after 4,000 hours at 225°C. Examination of the part disclosed that the pin 7 aluminum stripe had migrated open, as shown in Figure D12. The stripe contained migration voids in several areas and no other part examined displayed this condition after accelerated life indicating that the electromigration probably was caused by excessive I_{SS} current in this part rather than any stripe deficiency. Examination of the life test monitor reading disclosed that the part was drawing 276 mA after reaching temperature at the start of the final 2000 hour period (2000 hours - 4000 hours). Nominal current is about 0.2 mA. After 4000 hours, the current had dropped to 13 mA at temperature which was still excessive. Examination of the part had disclosed no deficiency which could account for the excessive current. Possibly, the excessive currect was caused by an intermittent external pin 7 (V_{SS}) chassis solder joint which allowed a pair of complementary transistors to conduct simultaneously as described in Section 4.3 of this appendix.

Four Lot C parts failed I_{IH2} at pin 1 or pin 2 at +125°C only. Two of these parts also failed V_{OH} at pin 11 at +125°C only. All four parts failed at 120 hours during Lot C acceptance testing. All four parts were left on test to 250 hours. As shown in Table D9, the failed parameters in each part returned to their pre-stress values at 250 hours. The complete recovery indicates that the failures were probably caused by a test set malfunction rather than by any part deficiency.



256X S/N A102 (4000 HRS/225°C)

FIGURE D12 - ELECTROMIGRATION VOIDS (ARROWS) IN THE PIN 7 STRIPE.

TABLE D9. PARAMETER HISTORY OF THE LOT C 120 HOUR FAILURES AT +125°C ONLY

S/N	PARAMETER	SPECIFIED LIMIT	MEASURED VALUES (+125°C) PRE-TEST	120 HOUR	250 HOUR
C35	I_{IH2} (2)	1.0 µA MAX	0.001 µA	63.102 µA	0.006 µA
	V_{OH1} (11)	4.6V MIN	4.933 V	3.421 V	4.933 V
C42	I_{IH2} (1)	1.0 µA MAX	0.036 µA	8.490 µA	0.031 µA
	V_{OH1} (11)	4.6V MIN	4.934 V	3.506 V	4.933 V
C43	I_{IH2} (1)	1.0 µA MAX	0.036 µA	8.998 µA	0.031 µA
C52	I_{IH2} (1)	1.0 µA MAX	0.033 µA	6.898 µA	0.032 µA

3.6 TEST ERRORS

Two Lot B parts were removed from test because one or two of their package leads were accidently broken off during parametric testing.

One unfailed Lot A part was inadvertently removed from test after 32 hours. The error was discovered too late to return the part to life test.

One Lot A part failed V_{OL3} at pin 10 and at pin 11 after 500 hours at 225°C. The measured values were 14.232 to 14.399 volts (specified limit = 1.5 volts maximum). A bench test of the part disclosed that V_{OL3} at pin 10 and at pin 11 was 0.00 volts (nominal). Further electrical tests and examination of the part disclosed no sign of an intermittency which could account for the failures. Consequently, this failure was probably caused by a faulty test socket or a test set malfunction.

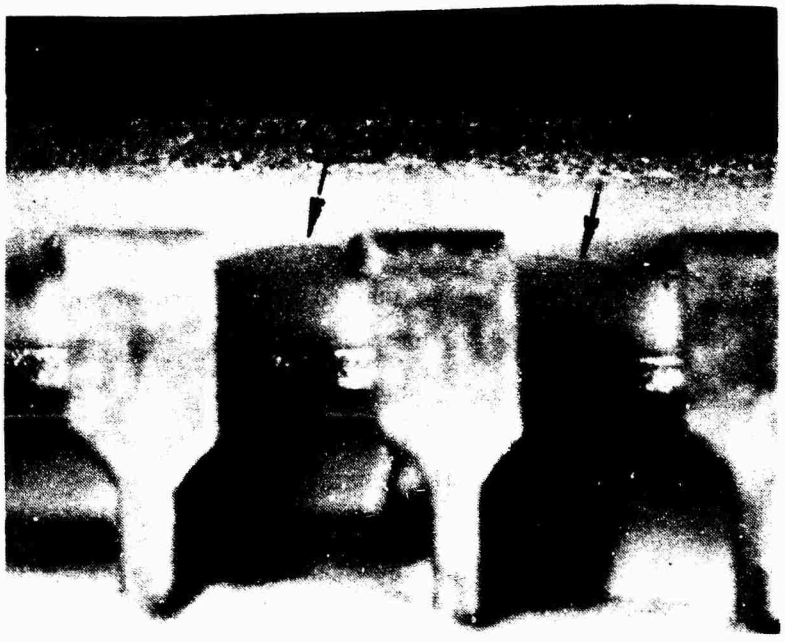
4.0 4001 QUAD TWO-INPUT NOR GATE - MANUFACTURER B

4.1 I_{SS}, I_{IH}, I_{IL}, AND V_{IC} FAILURES - NONHERMETIC PACKAGE

Forty-six parts (17 Lot A, 27 Lot B, and 2 Lot C) failed during life test because they contained or developed leaks in the package seal which allowed moisture to enter the package. Forty-four parts were gross leakers and two parts exhibited only a fine leak. One part contained no visible leak path, but in the other 45 parts the leaks were traced to:

1) cracks in the glass seal (27 parts), as illustrated in Figure D13, due to thermal expansions and contractions of the package during insertion and removal of the parts from elevated temperature (all 27 parts failed at or after the 250 hour test point or 7 cycles).
2) gaps along the interface of the glass seal and the lead (10 parts), as illustrated in Figure D14, due to fracturing of the glass meniscus during lead forming (all 28 parts failed at or before the 250 hour test point) and probably propagation of cracks into the packages.
3) voids in the lid seal (8 parts), as illustrated in Figure D15, due to deficiencies in the lid seal operation.

The moisture that entered the package caused three types of failure modes/mechanisms. Thirty-four parts failed due to excessive I_{SS} [17] and/or I_{SS} [18] and/or I_{SS} [19]. All 34 parts recoverd when baked, thus, the ultimate mechanism in these parts probably involved charge separation or drift of mobile ions brought in by or accelerated by the moisture. Ten parts failed due to excessive I_{IL1} and/or I_{IH1} caused by inversion of an input protection network and moisture trails across the networks. These parts recovered when baked or delidded. One part failed due to an open pin 13 and one part failed due to an open pin 7 and pin 9. The opens were traced to wire bonds at the lead frame that had corroded open in the presence of the moisture, as illustrated in Figure D16.

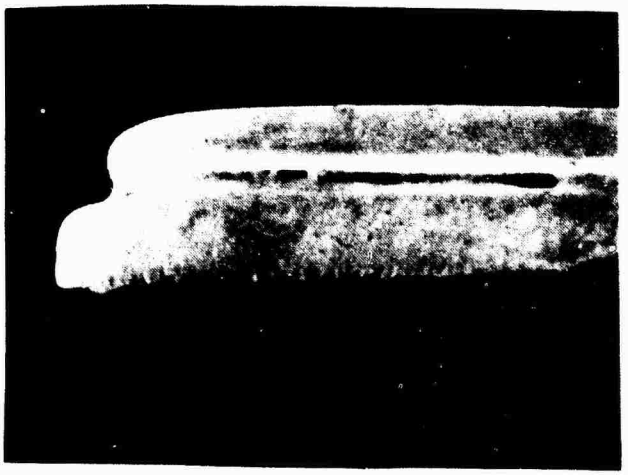


17X S/N B143 (2000 HRS/250°C)

FIGURE D13 - EXAMPLE OF CRACKS (ARROWS) IN THE GLASS SEAL.

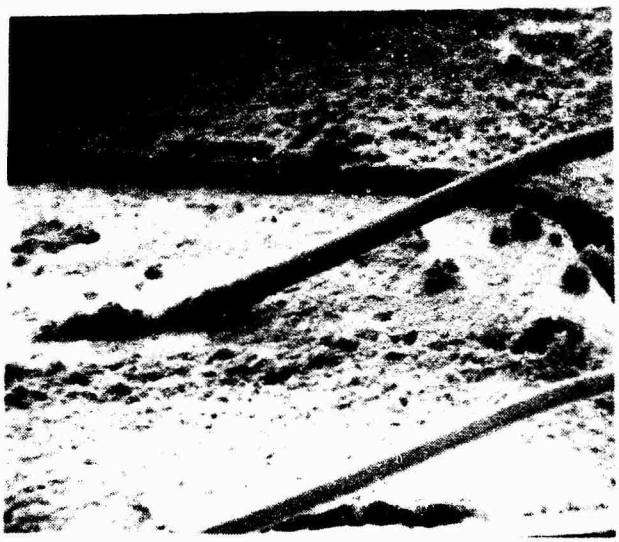
10X (SEM) S/N A91 (250 HRS/250°C)

FIGURE D14 - EXAMPLE OF GAPS AT THE GLASS SEAL MENISCUS.



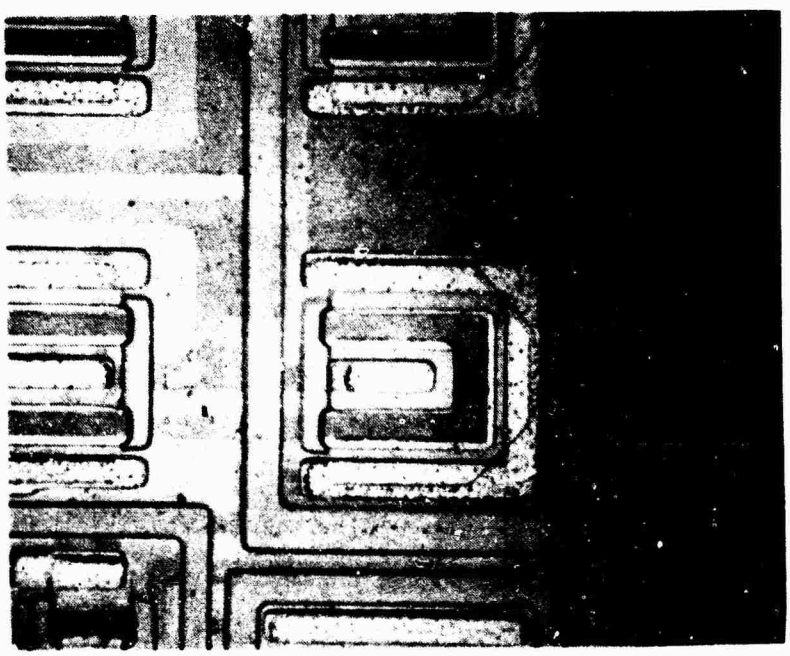
37X (SEM) S/N B154 (1000 HRS/250°C)

FIGURE D15 - EXAMPLE OF SOLDER VOIDS IN THE LID SEAL.



150X (SEM) S/N B175 (6000 HRS/225°C)

FIGURE D16 - CORRODED OPEN PIN 13 WIRE BOND AT THE LEAD FRAME.



400X S/N B53 (2000 HRS/125°C)

FIGURE D17 - EXAMPLE OF A DEGRADED N-CHANNEL "ON" TRANSISTOR (N4 OF GATE B) AFTER METAL REMOVAL.

4.2 I_{SS} FAILURE - SURFACE INSTABILITY

Sixty-five parts (58 Lot A and 7 Lot B) failed during step-stress and accelerated life due to excessive I_{SS} current(s). One part failed I_{SS} [17] only, five parts failed I_{SS} [18] only, 13 parts failed I_{SS} [19] only, seven parts failed I_{SS} [17] and I_{SS} [18], 19 parts failed I_{SS} [18] and I_{SS} [19], and 20 parts failed I_{SS} [17], I_{SS} [18] and I_{SS} [19]. The failed values ranged from 1.01 to 848 microamperes. All the failures were reversible, indicative of a surface related mechanism.

Some major obstacles were encountered during analysis of these parts. The unfailed I_{SS} currents in most of the parts were quite high and often approached the value of the failed I_{SS} currents. In all, 46 parts exhibited high or failed values for all three I_{SS} parameters. Consequently, the I_{SS} tests were, in general, of no use in troubleshooting the parts externally (at least one I_{SS} parameter must be zero or substantially lower than all others in order to externally isolate the leakage to a specific gate or transistor in the device) to classify the parts into failure mode categories. Failure mode/mechanism classification could only be achieved by systematic die level stripe severing and probing of each part. This would be much too time consuming and impractical. Furthermore, bench tests of the failed parts disclosed that many had recovered while awaiting analysis, and preliminary analysis of representative parts disclosed many would recover during analysis. Consequently, it was decided, in agreement with the RADC project engineer, that only as many parts would be analyzed in detail, as necessary to determine what different failure modes existed in these parts.

Fifteen parts had been delidded for analysis without leak testing (to avoid affecting their leakage currents) as part of the preliminary analysis. Consequently, these 15 parts are segregated from the other 49 parts (which were leak tested and found to be hermetic) in the analysis summaries since it is uncertain whether these failures should be classified as hermetic or non-hermetic. In addition to these 15 parts, ten of the hermetic parts were analyzed in detail; thus, in all, 25 of the 64 parts were analyzed in detail.

In nine parts, the leakage either recovered during the analysis or changed to the extent that it was not possible to pin-point the location of the leakage. Analysis of the other 16 parts disclosed three types of failure modes: 1) excessive I_{DSS} in an n-channel transistor that had been "on" during life test, 2) excessive I_{DSS} in a p-channel or an n-channel transistor that had been "off" during life test, and 3) a channeled p-well junction. Each failure mode is discussed below. In general, most of the parts exhibited more than one failure mode and most exhibited p-well junction leakage to some degree which is the reason most of the parts exhibited high or failed values for all three I_{SS} parameters.

1) Excessive I_{DSS} in an "on" n-channel transistor. In three parts the principal cause of the I_{SS} leakage was traced to excessive I_{DSS} in n-channel transistors N2 of gate C (one part) and N4 of gate A or B (two parts). The degraded transistors exhibited a channeled I_{DSS} characteristic and relatively low threshold voltage. The excessive I_{DSS} could be pinched off by applying negative voltage to the gate. This indicated that the excessive I_{DSS} was caused by inversion of the channel region due to the acumulation of a net positive charge at the SiO_2/Si interface. The degraded transistors recovered after a 16 hour, 250°C bake. Examination of the transistors before and after removal of the metallization disclosed no anomaly. A typical degraded transistor is shown after metal removal in Figure D17.

During the life test, +18 VDC had been applied across the gate oxide of the degraded transistors (biased "on"). Therefore, their failure mode indicated that the gate oxide of the transistors contained cation contamination, probably sodium ions. Under the influence of the positive gate bias, the cations drifted to the interface and inverted the underlying p-type channel region.

2) Excessive I_{DSS} in an "off" transistor. In four parts the principal cause of the I_{SS} leakage was traced to excessive I_{DSS} in N4 of each gate (one part), P1 of gate B (one part), or P4 of each gate (two parts). The

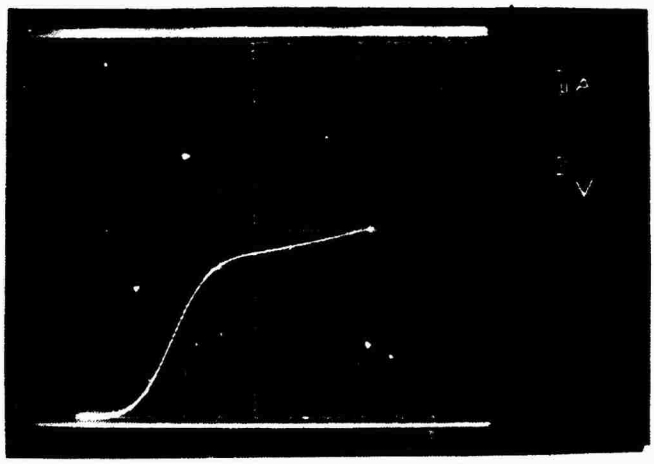
degraded transistor exhibited a channeled I_{DSS} characteristic, no threshold voltage shift and the excessive leakage could not be pinched off with reverse gate voltage. This indicated that the transistors contained a degraded drain junction. The degraded transistors recovered after a 16 hour, 250°C bake.

During life test, the drain junctions of P1 of gate B, N4, and P4 were reverse biased (the transistors were off). Thus, the degradation probably was caused by mobile ions in or on a passivation layer which separated in the fringing field of the reverse biased junction and inverted the underlying silicon.

3) Channeled p-well junction. In nine parts, the principal cause of the I_{DSS} leakage was traced to a leaky p-well junction. The reverse I-V characteristic of the degraded junction was channeled, as shown in Figure D18, and the leakage recovered after a 16 hour, 250°C bake. The p-well junctions were reverse biased during life test, thus, the degradation probably was caused by mobile ions in or on a passivation layer which separated in the fringing field of the reverse biased junction and inverted the underlying silicon.

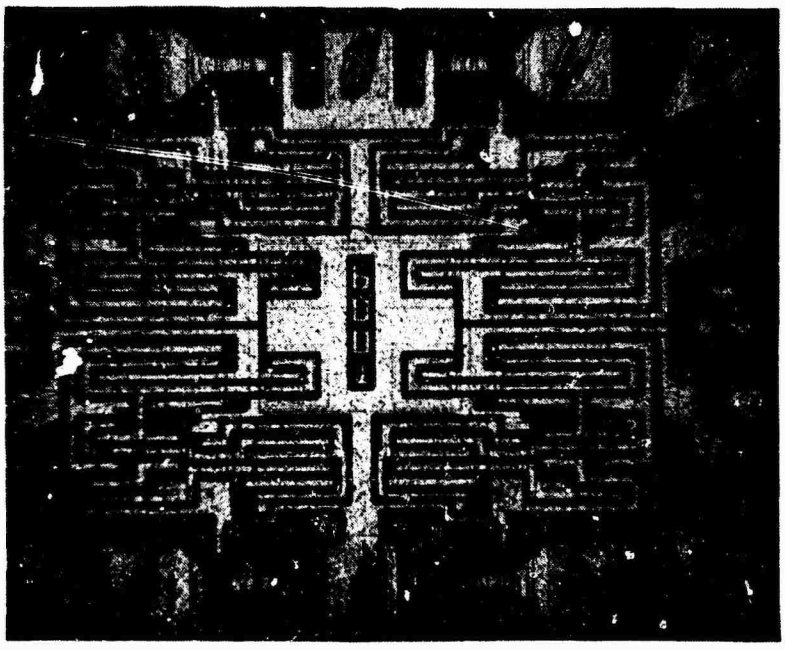
4.3 TEST ANOMALIES

Fifteen parts (1 Lot A, 8 Lot B, and 6 Lot C) failed during the tests due to open, resistive, or shorted pins. During step stress one Lot A part, S/N A42, failed at the 64 hour/250°C step due to an open pin 12 and one Lot C part, S/N C104, failed at the 80 hour/275°C step due to an open pin 6 and a shorted pin 13. Examination of these parts disclosed aluminum electromigration at the ohmic contacts of the input protection networks. For example, S/N A42 contained depleted aluminum at the pin 5, pin 8, and pin 12 (open) ohmic contacts and aluminum accumulation at the pin 6 and pin 13 ohmic contacts where shown in Figure D19. During step-stress inputs 1, 5, 8, and 12 were high (+18 VDC) and inputs 2, 6, 9, and 13 were low (ground). The depleted aluminum at the inputs biased high and the accumulation of aluminum at the inputs biased low indicated that sustained high current flowed into each high



S/N A234 (64 HRS/225°C)

FIGURE D18 - REVERSE I-V CHARACTERISTIC OF THE GATE A P-WELL JUNCTION.

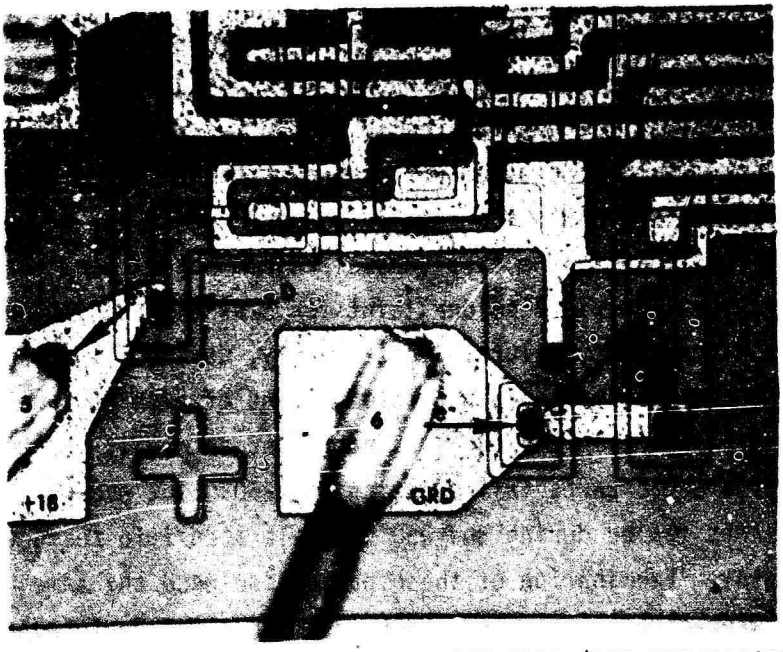


105X S/N A42 (250°C STEP)

FIGURE D19 - DIE PHOTO OF S/N A42 SHOWING THE LOCATION OF THE DEPLETED ALUMINUM (D) AND THE ALUMINUM ACCUMULATION (A).

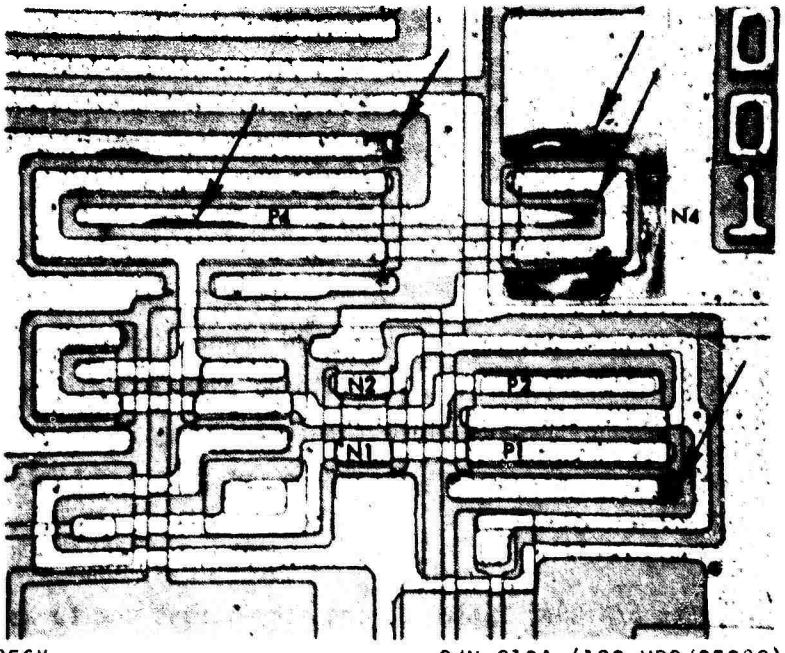
input and out each corresponding low input probably due to a latch-up condition. Special tests of sample parts showed that no latch-up would occur under normal bias conditions at temperatures up to 300°C. However, it was found that if the pin 7 (V_{SS}) connection was opened at temperatures above 250°C, excessive current flowed into the high inputs and out of the grounded inputs. In view of these findings, the step-stress program boards were examined and it was discovered that the pin 7 solder joint for S/Ns A42 and C104 were open which accounted for their failure. Consequently, during all subsequent testing, the continuity of the pin 7 solder joint of each part was checked before placing the part in the ovens at each test interval. Despite this precaution, five Lot C parts failed during the 250°C lot acceptance test and eight Lot B parts failed during the 250°C accelerated life test due to open and shorted pins. Examination of these parts disclosed the same conditions found in the step-stress failures. Each part contained depleted aluminum at the ohmic contacts of the input pins that had been biased high and accumulation of aluminum at the ohmic contacts of the inputs that were grounded, as illustrated in Figure D20. In addition, all of the parts showed evidence of electromigration at the ohmic contacts of complementary pairs of p-channel/n-channel transistors, as illustrated in Figure D21. This type of damage coincided with a migrated open on an input line that had been biased high. When the high input opened, the p-channel input transistor that was biased off by the +18 VDC (P1 or P2) apparently switched on causing excessive current to flow in the complementary transistor pairs from V_{DD} to ground through the grounded inputs. Many of the parts contained electromigration damage at the pin 7 pad, as illustrated in Figure D22. For this to happen, the external pin 7 solder joint must have been intermittent and opened long enough at temperature to induce a latch-up condition, then closed and allowed the excessive current to flow to ground through pin 7. Intermittency at temperature would explain why the faulty solder connections were not detected by the room temperature continuity checks.

One Lot C part, S/N C95, failed during step-stress due to an open drain in the pin 4 and the pin 11 n-channel output transistor, N4. Examination of the transistors disclosed that in each instance the drain stripe had melted



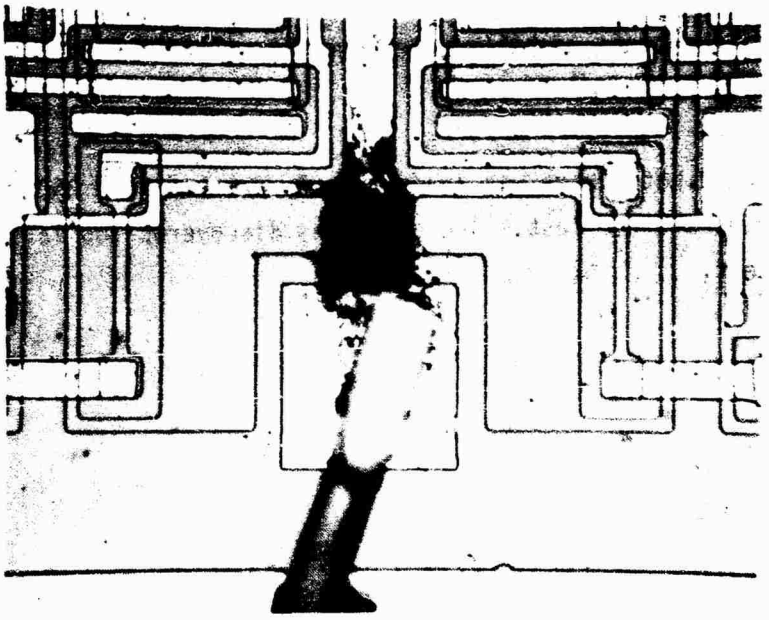
256X S/N C134 (120 HRS/250°C)

FIGURE D20 - PIN 5 AND PIN 6 INPUTS OF A 120 HOUR/250°C LOT C FAILURE SHOWING ALUMINUM DEPLETION (D) AT THE HIGH INPUT AND HILLOCK GROWTH OR ACCUMULATION (A) AT THE GROUNDED INPUT.



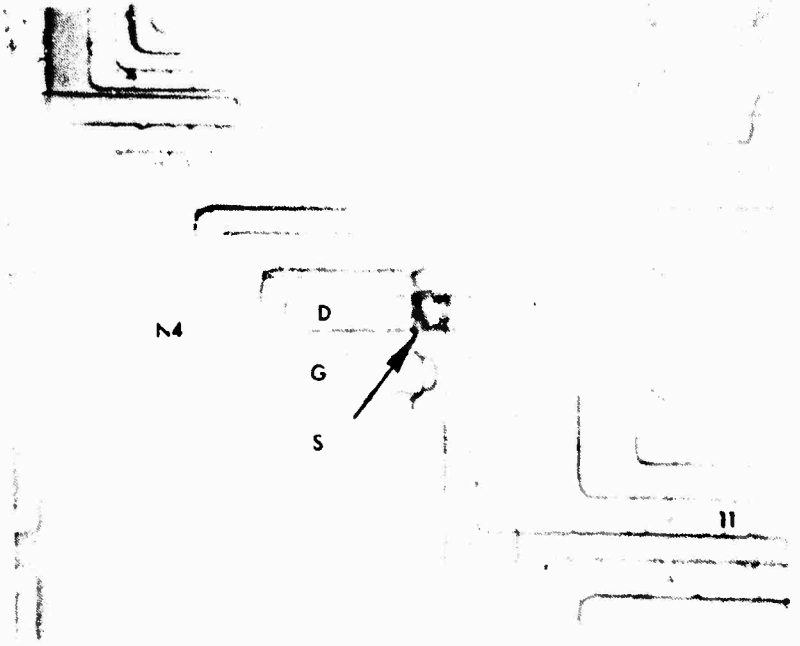
256X S/N C134 (120 HRS/250°C)

FIGURE D21 - EXAMPLE OF ALUMINUM ELECTROMIGRATION (ARROWS) AT THE TRANSISTOR CONTACTS OF GATE B.



256X S/N B124 (4000 HRS/250°C)

FIGURE D22 - EXAMPLE OF ALUMINUM DAMAGE AT THE PIN 7 PAD.



491X S/N C95 (275°C STEP)

FIGURE D23 - MELTED OPEN DRAIN STRIPE ON THE PIN 11 OUTPUT TRANSISTOR.

open, as illustrated in Figue D23. No deficiency and no other damage was present, thus, the opens probably were caused by electrical overstress of the two outputs.

One unfailed Lot A part was inadvertently removed from 250°C life after the four hour parametric test. The error was discovered too late to return the part to test.

5.0 4013 DUAL FLIP-FLOP - MANUFACTURER C

5.1 I_{SS} FAILURE - SURFACE INSTABILITY

Seventy-five parts (16 Lot A, 53 Lot B, and 6 Lot C) failed during the tests due to excessive I_{SS} [17] and/or I_{SS} [18] and/or I_{SS} [19]. Five parts failed I_{SS} [17] only, 21 failed I_{SS} [18] only, eight failed I_{SS} [19] only, three failed I_{SS} [17] and I_{SS} [19], 32 failed I_{SS} [18] and I_{SS} [19], and six failed I_{SS} [17], I_{SS} [18], and I_{SS} [19]. All failures were reversible, indicative of a surface-related mechanism. The variety of failure symptoms indicated that this group of failures probably contained several different failure modes. Preliminary analysis of these failures indicated that parts with the same failure symptoms contained different failure modes or mechanisms. This meant that the parts could not be classified into failure categories on the basis of their failure symptom, i.e., on the basis of which of the three I_{SS} tests the part had failed. The Manufacturer C 4013 contains 48 transistors and eight transmission gates, thus, random or even systematic die level probing of every failed part to determine the degraded transistor(s) for purposes of classification was impractical. The preliminary investigation had indicated that the excessive I_{SS} was due to high leakage current in a transistor or transistors that were "off" during the I_{SS} test. Because each half of the 4013 contains three inputs, it is possible to obtain eight (2^3) unique sets of different logic levels on the internal transistors of each half with the clocks low. Thus, the I_{SS} tests can be expanded to eight tests (I_{SS1} through I_{SS8}), as shown in Table D10. Furthermore, during the I_{SS7} and I_{SS8} tests the output states can be switched either high or low, which adds two additional sets of information. From these ten tests and a knowledge of the logic state of each transistor during each test, the leaky transistor (or transistors) can be reasonably pin-pointed externally. To aid in interpreting the results of the ten tests, the matrix column in Figure D24 was developed. The first ten vertical columns represent the ten I_{SS} tests and the horizontal rows represent each suspect transistor or combination of transistors. A shaded square is placed in each row in the appropriate column if the particular transistor is off during the particular I_{SS} test and can contribute leakage to the I_{SS} test.

TABLE D10. INPUT LOGIC CONDITIONS FOR THE EIGHT POSSIBLE I_{SS} TESTS

	INPUT LOGIC LEVEL (CLOCK = LOW)		
Iss TEST	SET	DATA	RESET
I_{SS1} *	LOW	LOW	HI
I_{SS2} *	HI	LOW	LOW
I_{SS3} *	HI	LOW	HI
I_{SS4}	LOW	HI	HI
I_{SS5}	HI	HI	LOW
I_{SS6}	HI	HI	HI
I_{SS7} (Q High or Low)	LOW	LOW	LOW
I_{SS8} (Q High or Low)	LOW	HI	LOW

* Standard Specified Tests

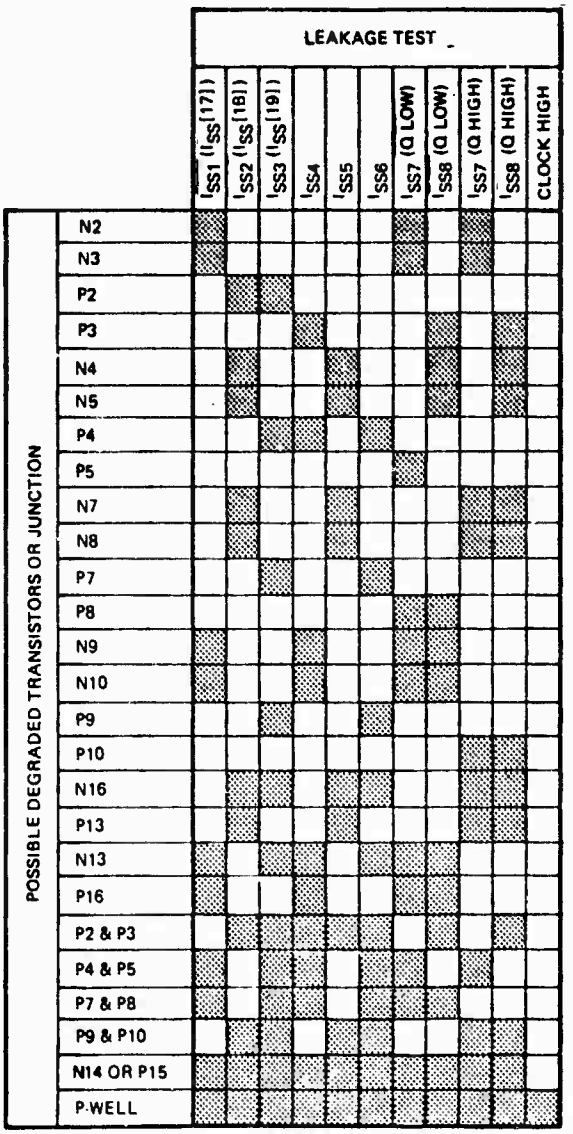


FIGURE D24. MANUFACTURER C 4013 I_{SS} DIAGNOSTIC MATRIX

A blank square means that the transistor is on during the particular I_{SS} test or, in the case of certain individual p-channel transistors, that the transistor is off, but in series with another transistor which is also off during that test. The possibility that two series p-channel transistors are both leaky is taken into account by the 21st through the 24th rows. If one or both of the off transistors of the clock circuit (N14 and P15) are leaky or if a p-well junction is leaky, the part will exhibit the same high leakage during all ten tests. By raising the clock input from low to high these two failure modes can be separated, and this is the reason for the final two rows and the eleventh column.

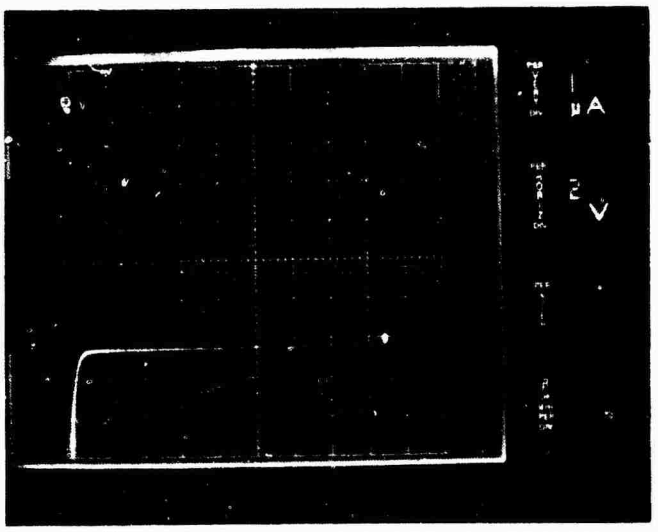
All ten I_{SS} values were then measured on a curve tracer for each flip-flop of each failed device and, using the matrix, the leaky transistor or transistors were determined. Then, the parts were classified into failure categories and representative samples of each category were analyzed in detail. Many of the parts contained more than one failure mode or had completely recovered before the analysis proceeded or during the analysis. In the case of a part with more than one failure mode, the part was classified according to the worst case (in terms of leakage current) failure mode. If the part had recovered and could not be classified on the basis of its symptoms, its failure mode was classified as not determined. The details of each category of failure mode are given in the following sections.

5.1.1 Excessive I_{DSS} in an "On" N-Channel Transistor - In 39 parts (1 Lot A, 32 Lot B, and 6 Lot C), the high I_{SS} was attributed to excessive I_{DSS} in one or more of the following transistors: N4, N5, N7, N8, or N16. Parts with a degraded N4, N5, N7, or N8 transistor had failed I_{SS} [18] and parts with a degraded N16 transistor had failed I_{SS} [18] and I_{SS} [19]. For example, S/N B95 exhibited I_{SS} [18] and I_{SS} [19] values of 3 μA after 4 hours in 250°C life. Curve tracer tests established that I_{SS2}, I_{SS3}, I_{SS5}, I_{SS6}, I_{SS7} (Q high), and I_{SS8} (Q high) of flip/flop 1 (F/F1) were each 3 μA, whereas I_{SS1}, I_{SS4}, I_{SS7} (Q low), and I_{SS8} (Q low) were zero. No leakage existed in F/F2. The matrix indicated that N16 was the only single transistor that could give

these symptoms, therefore N16 of F/F1 was isolated and measured. I_{DSS} of N16 was about 3 μA at V_{DS} = 15V and the I_{DSS} vs. V_{DS} characteristic was channeled, as shown in Figure D25. The excessive I_{DSS} could be pinched off by applying a -0.8 volt from gate to source and V_{TH} of N16 was lower than that of a typical transistor (N13) in the same part, as shown in Figure D26. This indicated that the anomalous current was caused by inversion of the channel region. A 16 hour, 250°C bake caused the degraded transistor to recover and examination of the transistor before and after removal of the metallization disclosed no visible anomaly. A typical failed N16 transistor after removal of metallization is shown in Figure D27. Many devices contained more than one degraded transistor. For example, S/N C52 exhibited an I_{SS} [18] value of 28 μA and an I_{SS} [19] value of 2 μA after 120 hours at 250°C. Curve tracer tests of F/F1 disclosed that I_{SS2}, I_{SS5}, and I_{SS8} (Q high) were 14 μA, I_{SS3} and I_{SS6} were 1 μA, I_{SS8} (Q low) was 2 μA, I_{SS7} (Q high) was 12 μA, and I_{SS1}, I_{SS4}, and I_{SS7} (Q low) were zero. Similar I_{SS} values were found in F/F2. The matrix indicated that these values were probably caused by various levels of leakage in transistors N4-N5, N7-N8, and N16 in each flip-flop. The suspect transistors were isolated and measured disclosing the following values of I_{DSS} at V_{DS} = 15 volts: in F/F1 N16 = 1 μA, N4-N5 = 2 μA and in F/F2 N16 = 1 μA, N4-N5 = 9 μA, and N7-N8 = 4 μA. In each transistor the I_{DSS} vs. V_{DS} characteristic was channeled and the excessive leakage could be pinched off by applying negative voltage from gate to source.

During the life test of the 4013, the set, data, and clock inputs were biased low and the reset inputs were biased high. This applied +15 volts across the gate oxide of transistors N4-N5, N7-N8, and N16. Therefore, it was concluded that the gate oxide of the transistors contained cation contamination, probably sodium ions. The cations drifted to the Si/SiO_2 interface under the influence of the positive field and inverted the underlying p-type channel region causing an increase in I_{DSS} and a reduction of V_{TH}.

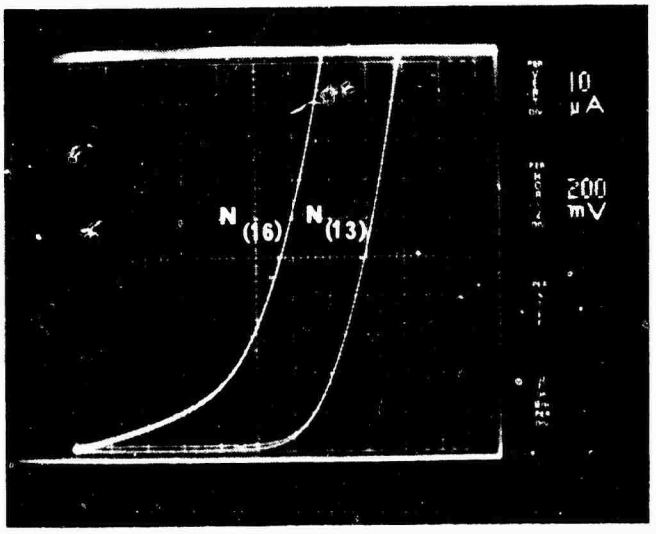
5.1.2 Excessive I_{DSS} in an "On" P-Channel Transistor - In 13 parts (three Lot A and ten Lot B), the high I_{SS} was attributed to excessive I_{DSS} in one or more of the following transistors: P2, P3, P9, or P10. Parts with a degraded



I_{DSS}

V_{DS} S/N B95 (4 HRS/250°C)

FIGURE D25 - I_{DSS} CHARACTERISTIC OF N16 OF F/F1.



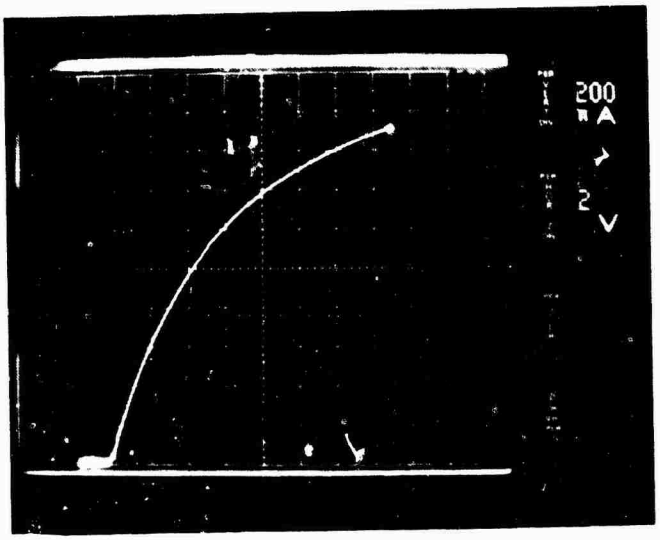
I_{DSS}

V_{GD-S} S/N B95 (4 HRS/250°C)

FIGURE D26 - THRESHOLD VOLTAGE CHARACTERISTIC OF N16 OF F/F1 (L/H TRACE) COMPARED TO THAT OF A NORMAL N-CHANNEL TRANSISTOR (N13) IN F/F1 (R/H TRACE). V_{TH} CHARACTERISTIC = V_{DS} VS. I_{DS} WITH $V_{GS} = V_{DS}$.

247X S/N B162 (8 HRS/250°C)

FIGURE D27 - TYPICAL FAILED N16 TRANSISTOR AFTER METALLIZATION REMOVAL.



I_{DSS}

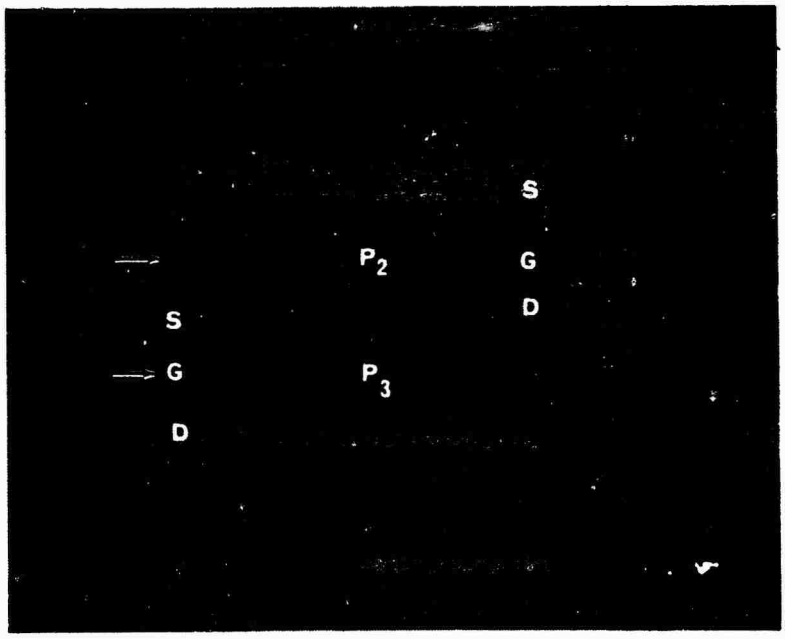
V_{DS} S/N B101 (4 HRS/250 C)

FIGURE D28 - I_{DSS} CHARACTERISTIC OF P9 OF F/F2.

P2, P3, or P9 and P10 had failed I_{SS} [18] and I_{SS} [19] and parts with a degraded P9 had failed I_{SS} [19]. In each part examined, the degraded transistor exhibited a channeled I_{DSS} characteristic, but nominal threshold voltage, and the excessive I_{DSS} was reversible. For example, S/N B101 contained a degraded P9 transistor in F/F2 after 4 hours at 250°C. I_{DSS} at V_{DS} = 15V of P9 was about 1.6 μA and the characteristic was channeled as shown in Figure D28. The excessive leakage could be pinched off by applying +5 volts from gate to source. V_{TH} of P9 was -2.21 volts, which was nominal. After recovery I_{DSS} of P9 was 132 nA, but V_{TH} had not changed significantly (-2.27V).

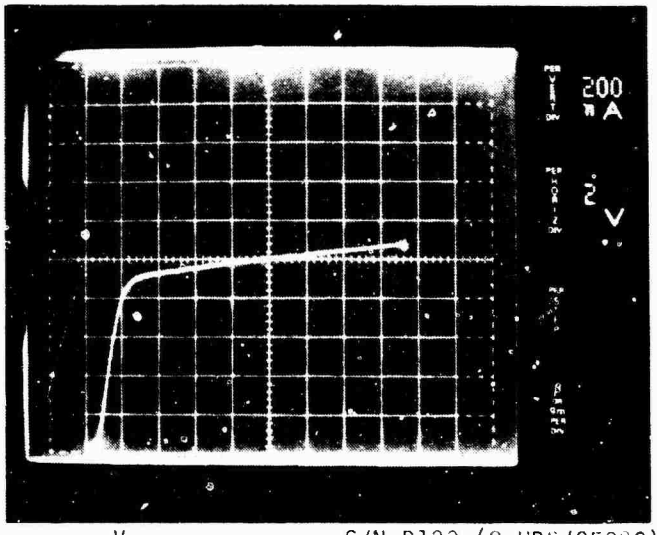
The high I_{DSS} and the fact that the leakage could be pinched off with positive gate bias indicated that the degradation in these transistors was due to inversion of the n-type substrate beneath the gate metal caused by the accumulation of a net negative charge at the SiO_2/Si interface. Since the threshold voltage of the transistors was not affected, the inversion probably was not located in the channel region or at least not along its entire width. Each of the failed transistors contained a strip of thick field oxide, covered by gate metal, between the source and drain at the sides of the channel, as illustrated in Figure D29. This might be the possible location of the inversion. During the life tests, -18 volts was applied across the gate oxide of P2, P3, P9, and P10 (these transistors were "on" during life). Inward drift of mobile negative ions in the oxide beneath the gate metal would account for the accumulation of negative charge at the interface. However, mobile anions do not ordinarily exist in normal oxides. It is more probable that the oxide contained a distributed mobile positive species in conjunction with an immobile negative species (outward drift of the cations in the negative field would expose a layer of negative charge at the interface) or that the oxide was phosphorous doped and the negative field polarized the phosphorous dipoles.

5.1.3 Degraded P-Well or Drain Junction - In nine parts the excessive I_{SS} was traced to high I_{DSS} in N2, N14, P4, P5, or P16. Parts with a degraded N2 had failed I_{SS} [17], parts with a degraded P4 or P5 had failed I_{SS} [17] and I_{SS} [18], and parts with a degraded N14 had failed I_{SS} [17], [18], and [19]. One



400X S/N A132 (120 HRS/250°C)

FIGURE D29 - P2 AND P3 OF F/F2 AFTER METALLIZATION REMOVAL SHOWING THE STRIP OF FIELD OXIDE (ARROWS) ALONG THE SIDES OF THE CHANNELS.



I_{DSS}

V_{DS} S/N B123 (8 HRS/250°C)

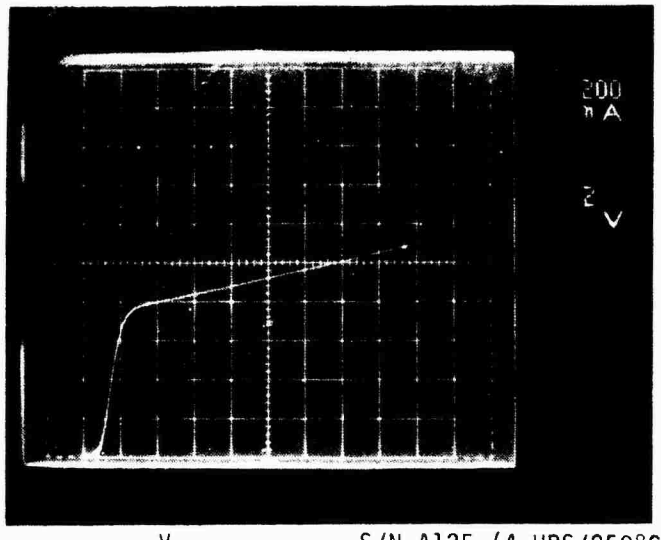
FIGURE D30 - I_{DSS} CHARACTERISTIC OF N14 OF F/F2.

of these parts had failed at +125°C only. But bench tests disclosed that I_{SS} was also failed at 25°C and analysis of the part established that the high I_{SS} was due to a degraded N14. In each case, the degraded transistor exhibited a channeled characteristic, as illustrated in Figure D30, no threshold voltage shift, and the leakage could not be pinched off by application of reverse gate voltage. This indicated that the transistors contained a degraded drain junction. In three parts the excessive I_{SS} was traced to a degraded p-well junction. These parts had failed I_{SS} [17], [18], and [19]. In each case the reverse I-V characteristic of the junction was channeled, as illustrated in Figure D31. In all cases, the leakage recovered when the part was baked.

During life test, the p-wells and the drain junctions of N2, N14, P4, P5, and P6 were reverse biased (the transistors were off). Thus, the degradation probably was caused by mobile ions in or on the passivation which separated in the fringing field of the reversed biased junctions and inverted the underlying silicon.

5.1.4 Failure Mode Not Determined - The exact failure mode of 11 parts was not determined because the excessive I_{SS} recovered before the failure mode could be established. All step stress failures were intentionally baked before analyzing and four parts recovered, indicating that their failure was caused by surface instability. The Lot A 175°C failure and one of the Lot B failures had failed I_{SS} [18] (I_{SS2}) only. The matrix indicates that the failure mode of these parts was either a degraded N4, N5, N7, or N8 (n-channel "on") or P13 (p-channel "off"); thus, their failure mode could not be established on the basis of the original symptoms. The other two parts had failed I_{SS} [19] (I_{SS3}) only. The matrix indicates that the failure mode was either a degraded P4 or P7 (p-channel "off") or P9 (p-channel "on"); thus, the failure mode of these two parts was not established.

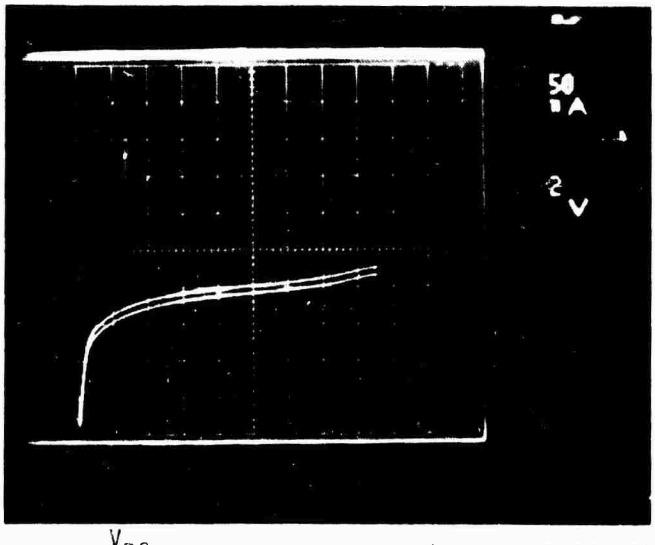
Two life test parts that had failed I_{SS} [18] only, the Lot A 16 hour failure and the Lot B 4 hour failure, recovered before the curve tracer I_{SS} tests could be performed. Two other Lot A parts had failed I_{SS} [18] and I_{SS} [19], and the matrix of I_{SS} tests indicated that the parts contained



I_R

V_R S/N A125 (4 HRS/250°C)

FIGURE D31 - REVERSE I-V CHARACTERISTIC OF THE DEGRADED P-WELL JUNCTION.



I_{DSS}

V_{DS} S/N B252 (4000 HRS/225°C)

FIGURE D32 - I_{DSS} CHARACTERISTIC OF N1 OF F/F1.

multiple failure modes. However, these parts recovered after delidding or during die level probing and the specific failure modes could not be determined. Although the failure modes were not established, the recovery of these four parts indicated that their failure probably was caused by a surface related problem. Two Lot B parts exhibited excessive I_{SS} [19] at a test temperature of +125°C at 250 hours. The two parts were left on test through 4,000 hours. They did not fail any 25°C parametric test through 4,000 hours and passed all +125°C parametric tests at 4,000 hours. One Lot A part exhibited excessive I_{SS} [18] and I_{SS} [19] at +125°C only at 4,000 hours. This part was left on test to 6,000 hours and I_{SS} had recovered at 6,000 hours. In each case the recovery indicated that the failures were probably caused by a surface-related mechanism.

5.2 I_{IH} FAILURE - SURFACE INSTABILITY

Twenty-one parts (2 Lot A, 17 Lot B, and 2 Lot C) failed due to excessive I_{IH1} (all inputs together) during life test. The failed values ranged from 117 to 384 nanoamperes (specified limit = 100 nA max). The leakages were channeled and were bake recoverable, indicative of a surface related mecnanism. In each case the excessive current was traced to one or both of the data inputs (pin 5 of F/F1, pin 9 of F/F2). In each Lot B and Lot C part examined, the leakage was caused by excessive I_{DSS} in the n-channel transistor of the input transmission gate (N1), as illustrated in Figure D32. In each Lot A part, the leakage was caused by excessive I_{DSS} in the p-channel transistor of the input transmission gate (P1). During life test, N1 and P1 were "on," thus, the failure mechanisms of N1 and P1 were probably the same as those responsible for the I_{SS} failures described in Sections 5.1.1 and 5.1.2.

5.3 I_{IL}/I_{SS} FAILURE - LEAD PRECIPITATION

Fourteen parts (12 Lot A and 2 Lot B) failed due to a pin-pin short during accelerated life. Thirteen parts exhibited excessive I_{IL1} (all inputs together). The failed values ranged from -123 to in excess of -1423 nanoamperes (specified limit = -100 nA min). The leakage was quasi-exponential and usually intermittent or erratic. In 12 of these parts the leakage

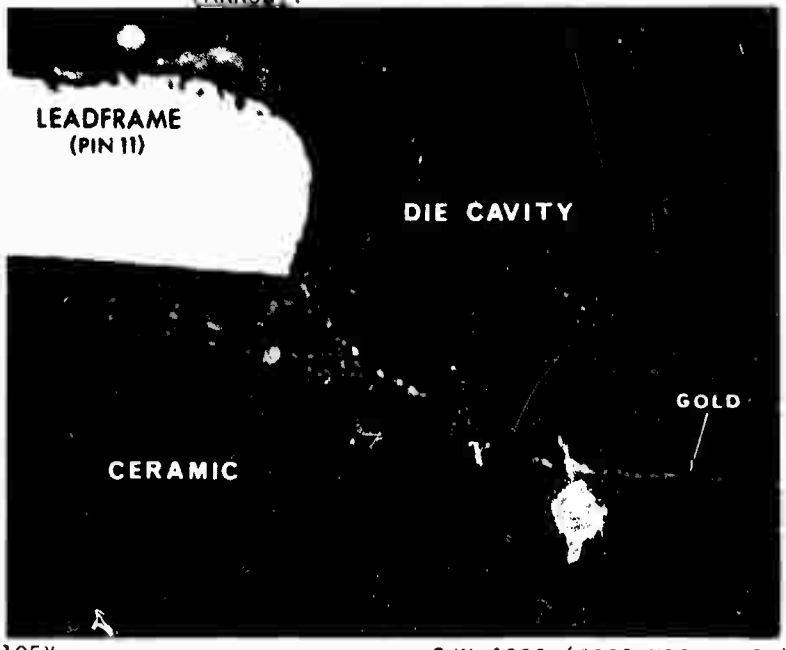
was traced to a high resistance short between pin 11 (the clock of F/F2) and pin 14 (V_{DD}) and in one part the leakage was traced to a high resistance short between pin 5 (the data input of F/F1) and pin 14. One part exhibited excessive I_{SS} [17], [18], and [19] caused by a high resistance short between pin 7 (V_{SS}) and pin 14. The shorts were isolated to a conductive path in the glass seal between the pin 11, 5, or 7 lead frame and the deposited gold header (which is connected to V_{DD}) where shown in Figure D33. The gold header extends under the glass seal beneath the tip of the lead frame, as shown in Figure D34. Cross sections of the glass seal disclosed faint traces of dark stains, similar to that found in the Manufacturer A 4001 package (Section 3.3), bridging from the lead frame to the gold header. The glass in this package is of the same composition ($PbO-ZnO-B_2O_3$) as that of the Manufacturer A package and pins 5, 7, and 11 were negatively biased with respect to pin 14 (V_{DD}) during life test. Thus, the failure of these parts was probably also caused by the same Pb reduction/precipitation mechanism responsible for the Manufacturer A 4001 failures.

5.4 I_{SS}/I_{IH} FAILURE - MASK MISALIGNMENT

Two Lot C parts, S/Ns C85 and C91, failed during step-stress after the 16 hour/175°C step due to excessive I_{SS} [17] and I_{IH1}. Also, pin 1 of S/N C85 was stuck low and pin 2 was stuck high. The failed parameters did not improve after baking. Curve tracer tests of the parts disclosed that F/F1 of each part was drawing very high current, above 1.5 volts, during the I_{SS} [17] and I_{IH1} tests. The high I_{IH1} in S/N C91 was traced to high I_{DSS} in n-channel transistor N15 of the clock circuit caused by a degraded drain junction. Figure D35 shows the I-V characteristic of the N15 drain junction of S/N C91. The excessive leakage reduced the C1 high level output voltage such that the transmission gate transistor P1 of F/F1 was not being turned off during the I_{IH1} test. This allowed excessive I_{IH} current to flow into pin 5 through P1 to V_{SS} via P11-N11 and N4 (which are on during the I_{IH1} test). Examination of N15 after removal of the aluminum metallization disclosed that its drain contact opening was misregistered, placing the contact against the drain junction, as shown in Figure D36. As a result, an aluminum alloy pit in the contact penetrated and degraded the drain junction, as shown in Figure D37.

18X S/N B224 (4000 HRS/225°C)

FIGURE D33 - INTERIOR OF THE PACKAGE (AFTER DISCONNECTING THE PIN 11 AND PIN 14 (V_{DD}) WIRES TO ISOLATE THE LEAKAGE) SHOWING THE LOCATION OF THE CONDUCTIVE PATH (ARROW).

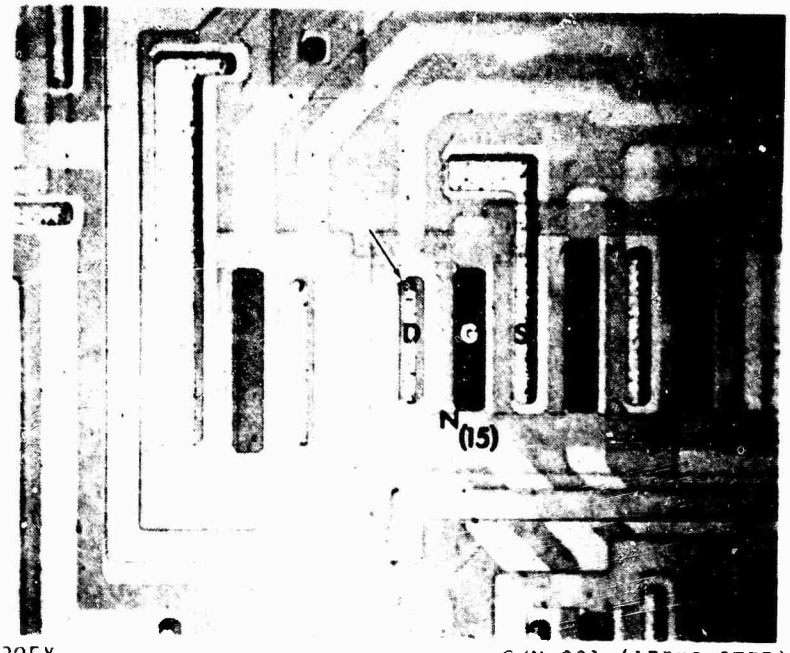


105X S/N A223 (4000 HRS/225°C)

FIGURE D34 - CROSS-SECTION OF THE PACKAGE THROUGH PIN 11 SHOWING THAT THE GOLD HEADER PLATING EXTENDS UNDER THE LEAD FRAME.

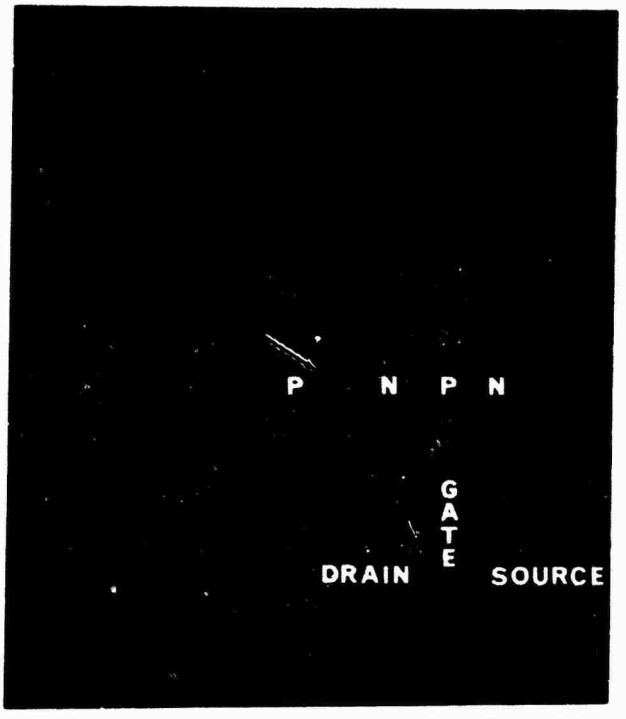
V_{DS} = 2 VOLTS/DIV. S/N C91 (175°C STEP)

FIGURE D35 - I-V CHARACTERISTIC OF THE DEGRADED DRAIN JUNCTION OF N15 (F/F1) OF S/N C91.



395X S/N C91 (175 C STEP)

FIGURE D36 - MISREGISTERED DRAIN CONTACT (ARROW) OF F/F1 N15 OF S/N C91.



780X S/N C91 (175°C STEP)

FIGURE D37 - F/F1 N15 DRAIN AFTER SILICON ETCH SHOWING AN ALLOY PIT (ARROW) THAT PENETRATED THE DRAIN JUNCTION.

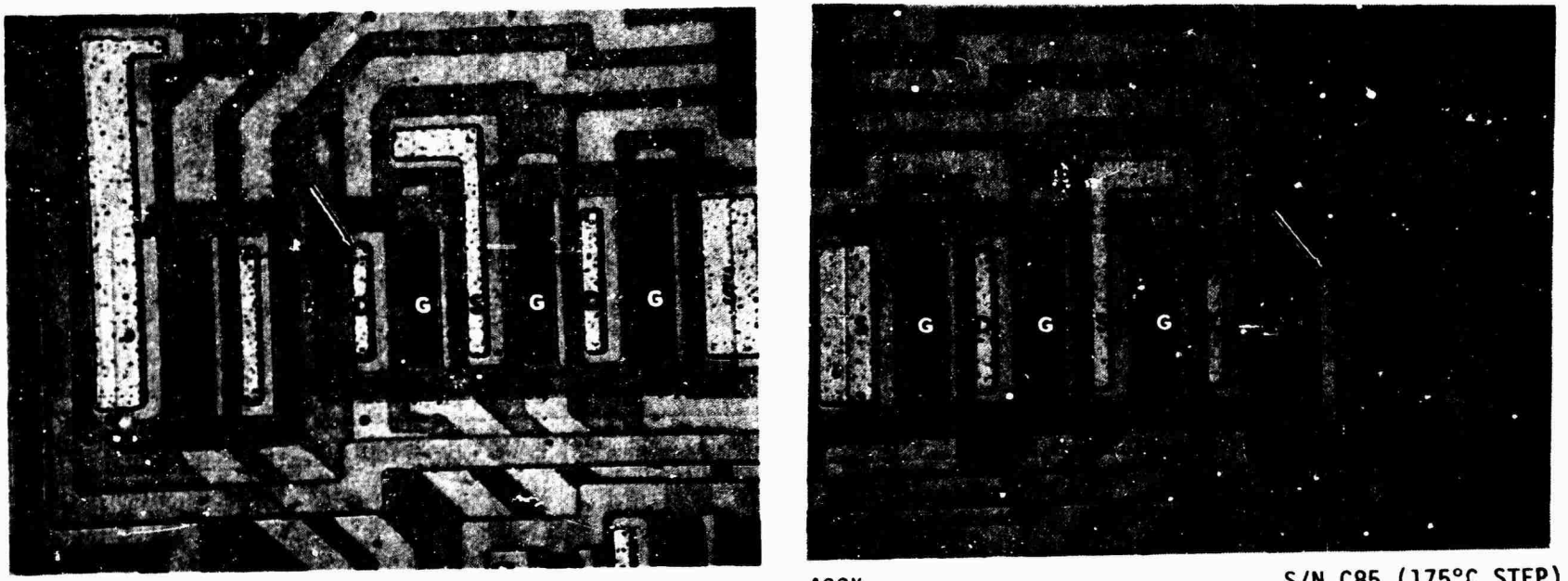
Similarly, the failure of S/N C85 was traced to misregistration of the N15 drain ohmic contact. Figure D38 shows the N15 transistors of F/F1 and F/F2 of S/N C85 aligned as they are oriented on the die. The ohmic contacts are displaced to the left in the photos and this placed the drain ohmic contact of N15 of F/F1 (and N14 of F/F2) over the junction. Note also the misregistration of the thin gate oxide which left a strip of thick field oxide along one end of each channel. The exact cause of the I_{SS} [17] failure in each part was not determined, but the curve tracer tests had indicated that the I_{SS} [17] failure was probably caused by the same type of defect responsible for the I_{IH1} failure.

The misregistration problem would likely be lot dependent but strangely no Lot C part failed due to this problem during the Lot C acceptance test even though this test was performed at 250°C. Five parts that survived the Lot C life test were delidded and examined. All five contained misregistered ohmic contacts. The worst case example is shown in Figure D39. This suggests that the mechanism that caused the contact to progress to failure may not have been time-temperature dependent, but rather was induced by random stress such as an electrical transient.

5.5 MISCELLANEOUS $I_{IH}/I_{IL}/V_{IC+}$ FAILURES

One Lot A part failed due to excessive I_{IL1} (113 nA) which was traced to pin 5, the data input of F/F1. The leakage was channeled and recovered after baking, indicative of a surface related mechanism. Pin 5 was grounded during life test, reverse biasing the input protection diodes to V_{DD}. Thus, the channel was probably caused by charge separation in the fringing field of the reverse biased junctions.

One Lot A part failed I_{IH1} (120 nA) which was traced to pin 8, the set input of F/F2. The leakage was resistive and intermittent, indicative of a mechanical problem, but the package was destroyed during delidding and the cause of the leakage was not determined.



056

400X

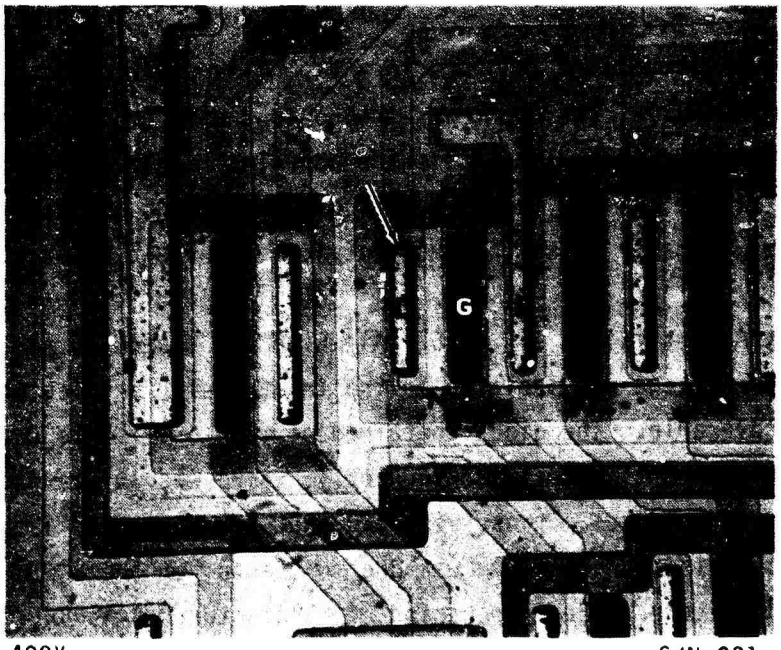
a) F/F1

400X

S/N C85 (175°C STEP)

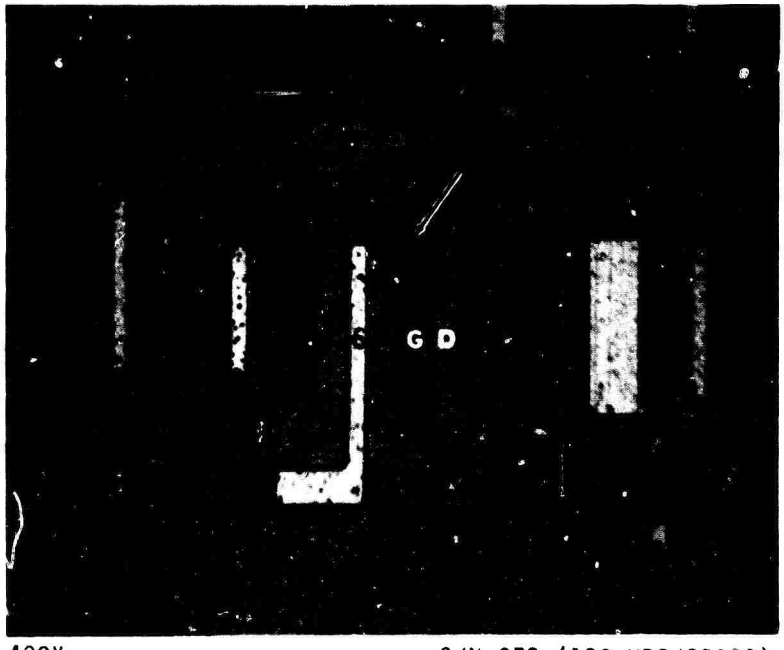
b) F/F2

FIGURE D38 - N14-N15-N4-N5 OF F/F1 AND F/F2 (METAL REMOVED) SHOWING THE MISPLACED OHMIC CONTACTS THAT OVERLAPPED THE DRAIN JUNCTIONS (ARROWS).



400X S/N C31

FIGURE D39 - F/F1 N15 OF A LOT ACCEPTANCE TEST SURVIVOR SHOWING THE DRAIN CONTACT (ARROW) OVERLAPPING THE JUNCTION.



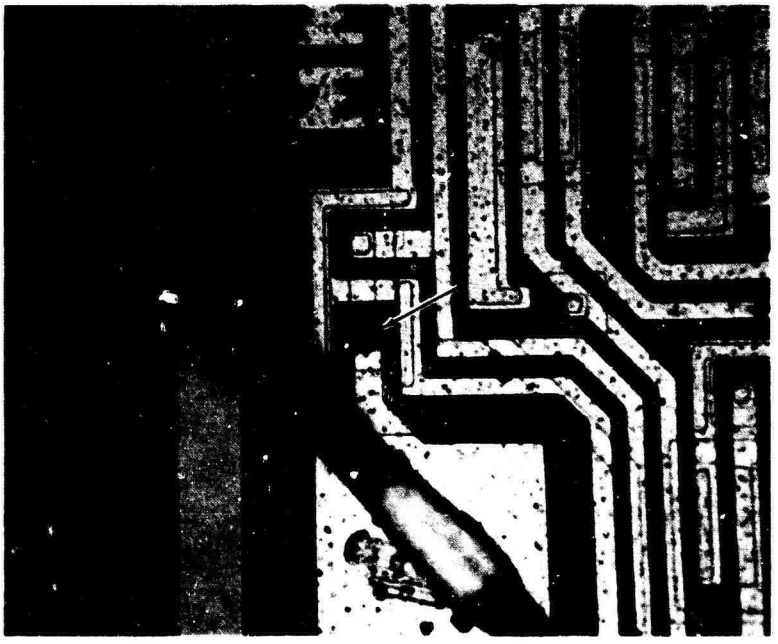
400X S/N C72 (120 HRS/250°C)

FIGURE D40 - DIELECTRIC BREAKDOWN SITE (ARROW) IN THE GATE OXIDE OF N4 OF F/F2.

One Lot C part failed I_{IH1} due to a 3K ohm short from pin 10 (reset of F/F2) to pin 7 (V_{SS}). The short was traced to a gate to body short in n-channel transistor N4. The gate oxide contained a dielectric breakdown site as shown in Figure D40 and the amount of damage present indicated that the breakdown was probably caused by an electrical transient or static discharge.

One Lot A part failed I_{IH1} (167 nA) which was traced to pin 3, the clock of F/F1. The leakage was isolated to the input-to-V_{SS} protect diode and was not bake recoverable. The diode contained no flaw or visible damage. Pin 3 was grounded during life test; consequently, there was no bias applied to the diode during life. Thus, it is suspected that the diode was damaged by an electrical transient or possibly was due to opening of the V_{SS} connection at elevated temperature. (See discussion of Manufacturer D 4008 I_{IH} failures, Section 9.2, for explanation of this failure mechanism.)

One Lot A part failed V_{IC+} at pin 10 (1.6 volts) and at pin 4 (2.0 volts). The high forward voltage was traced to damage at the ohmic contact between the input stripe and the input to V_{DD} protection network. The aluminum was melted and swollen from overheating at the contacts, as illustrated in Figure D41. This indicated that pins 4 and 10 probably had been electrically overstressed.



256X S/N A144 (2000 HRS/250°C)

FIGURE D41 - MELTED/SWOLLEN ALUMINUM (ARROW) AT THE PIN 10 OHMIC CONTACT.

6.0 4013 DUAL FLIP-FLOP - MANUFACTURER B

6.1 I_{SS} FAILURES

Thirty-eight parts (3 Lot A, 22 Lot B, 13 Lot C) failed during step-stress and accelerated life due to excessive $I_{SS}[17]$ and/or $I_{SS}[18]$ and/or $I_{SS}[19]$ at 25°C. Two parts failed $I_{SS}[17]$, eight failed $I_{SS}[18]$, two failed $I_{SS}[19]$, one failed $I_{SS}[17]$ and $I_{SS}[18]$, three failed $I_{SS}[17]$ and $I_{SS}[19]$, four failed $I_{SS}[18]$ and $I_{SS}[19]$, and 18 failed $I_{SS}[17]$, $I_{SS}[18]$, and $I_{SS}[19]$.

The three step-stress failures had been baked and had recovered. The other 35 failures were examined on the curve tracer. The ten diagnostic I_{SS} parameters developed for the Manufacturer C 4013 shown in Table D10 were measured. Four parts showed no parameter out of tolerance which indicated that the parts had recovered while awaiting analysis. Twelve parts (eight Lot C and four Lot B) exhibited excessive leakage for all ten tests with the clocks low and no leakage for all ten tests with the clocks high. This indicated that the degraded transistor was located in a clock circuit (N20, N22, or P21). The remaining 19 parts displayed ten different patterns of failure, as shown in Table D11. These parts would required a diagnostic matrix to analyze. The matrix developed for the Manufacturer C 4013, Figure D24, could not be used for the Manufacturer B 4013 because the circuit designs are completely different. Since there were too few parts per lot/per failure pattern and since some of the parameters in six of the parts had recovered, it was decided not to develop a diagnostic matrix for these random failures. Consequently, only the 12 parts with a degraded clock transistor were analyzed in detail. All other parts were leak tested, baked, and delidded for examination only.

6.1.1 I_{SS} Failures Degraded Clock Transistor - I_{SS} of the 12 parts with a degraded clock transistor ranged from 1 to 300 μA. In all eight Lot C parts and in two of the Lot B parts the leakage was associated with F/F2. In the other two Lot B parts, the leakage was

TABLE D11 - PATTERNS OF I_{SS} FAILURE BASED ON CURVE TRACER TESTS

LOT-TEMP	TIME OF FAILURE	S/N	FLIP-FLOP	I_{SS} TEST NUMBER 1	2	3	4	5	6	7L	7H	8L	8H
A-250°	250	A133	1		[X]			X			X		X
B-250°	1K	B135	1		[X]			X			X		X
	4K	B105	1		[X]			X			X		X
		B121	2		[X]			X			X		X
C-250°	120	C104	1		[X]			X			X		X
	250	C113	1+2		[X]	[ ]		X			X		X
A-225°	2K	A225	1+2	[X]	[X]	[X]	X	X	X	X	X	X	X
	6K	A183	1+2	[X]	[X]	[X]	X	X	X	X	X	X	X
B-250°	2K	B91	1+2	[X]	[X]	[X]	X	X	X	X	X	X	X
B-250°	4	B94	1		[X]	[X]		X	X		X		X
		B142	2		[X]	[X]		X	X		X		X
B-250°	2K	B154	1	[X]	[ ]	[X]	X		X	X	X		
C-250°	120	C75	1	[X]						X			
B-225°	64	B201	1	[X]	[X]	[X]				X	X		
B-250°	4K	B124	2			[ ]				X	X		
B-250°	4	B141	2		[X]		X			X	X	X	X
B-250°	6K	B101	1	[ ]	[ ]	[X]			X				
B-250°	4	B153	1			X	X		X				
	6K	B103	1	[ ]	[ ]	[X]	X		X				
			2				X			X	X	X	X
B-250°	4K	B114 and B122											
	6K	B151	RECOVERED										
C-250°	120	CB5											

NOTES:
X = IN EXCESS OF 1μA DURING THE CURVE TRACER BENCH TEST.
[ ] = STANDARD SPECIFIED TEST (I_{SS} [17],[18],[19]) IN EXCESS OF 1μA DURING ELECTRICAL PARAMETER MEASUREMENT.

traced to excessive I_{DSS} in n-channel transistor N20 or N22 of the clock circuit. I_{DSS} was channeled, as illustrated in Figure D42, and the drain-to-source leakage could be pinched off by applying a negative voltage from gate to source. The leakage would drift at room temperature. Application of a positive gate voltage for a few minutes would cause I_{DSS} to increase about one order or magnitude and negative gate voltage stress would cause I_{DSS} to decrease to within specification. These findings indicate that the gate oxide contained highly mobile positive charges. During life test, zero volts had been applied across the gate oxide of N20 and N22 (their body, source, and gates were grounded). Thus, it does not appear that the charge accumulation resulted from conventional charge migration through the gate oxide. This n-channel transistor failure mode has been observed and investigated during previous high-temperature accelerated life tests conducted by this laboratory for NASA and for RADC. In both instances, the instability was attributed to moisture that had accumulated in the package due to cracked glass seals [1] or due to outgassing of epoxy die attach material [2]. However, the Manufacturer B 4013 utilizes eutectic die attach and leak tests of the 12 parts disclosed that all but two were hermetic. Possibly, the Manufacturer B 4013 had developed the onset of cracks such as those that had occurred in the Manufacturer B 4001 and moisture was drawn into the cavity by a package breathing phenomenon.

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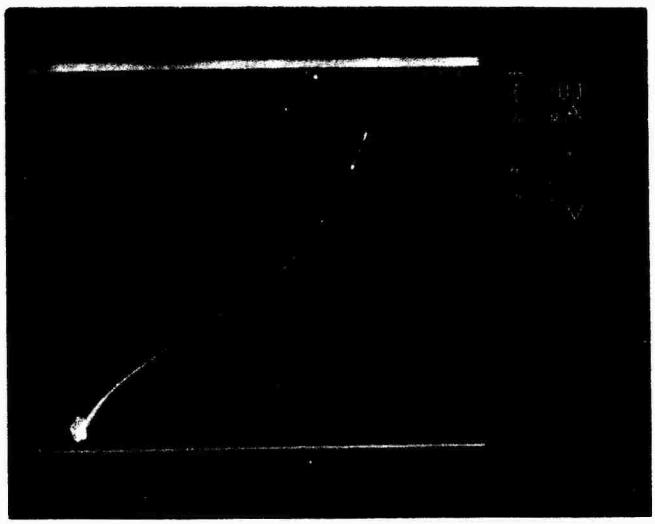
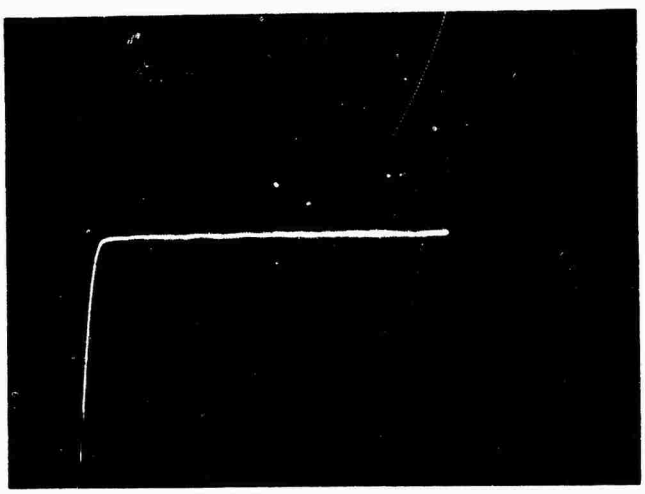
[1] G. M. Johnson, "Voltage Stress Effects On Microcircuit Accelerated Life Test Failure Rates", NASA Contract NAS8-31177, July, 1976.

[2] G. M. Johnson, "Evaluation of Microcircuit Accelerated Test Techniques", RADC-TR-76-218, July, 1976, A029757.



S/N C54 (250 HRS/250°C)

FIGURE D42 - I_{DSS} CHARACTERISTIC OF N20 OF F/F2.



V_R = 2 VOLTS/DIV. S/N A185 (6000 HRS/225°C)

FIGURE D43 - REVERSE I-V CHARACTERISTIC OF D3 OF PIN 5.

6.1.2 Random and Recovered I_{SS} Failures - The remaining 26 parts were leak tested and baked as necessary. The results of these tests are shown in Table D12. The parts were baked for 24 hours at 250°C, then retested. Any part that failed after this bake was delidded and baked for 72 more hours at 250°C. The table shows the final results after all bakes. Each part was delidded and microscopic examination of the interior and the die disclosed no visible anomaly in any part. The results of the bakes indicated that there were possibly 14 different failure patterns in the 19 failed parts rather than the original suspected ten categories. However, since the 19 parts were not analyzed in detail, all parts are shown in only two failure categories, bake recoverable (surface instability) and non-bake recoverable, on the failure summary tables.

6.2 I_{IL} FAILURE

One Lot A part exhibited excessive (285 nA) I_{IL1} (all inputs together) that was traced to pin 5, the data input of F/F1. The leakage was caused by a degraded input to V_{DD} protection diode, D3. D3 displayed a channeled reverse characteristic, as shown in Figure D43, and the leakage was recoverable. Pin 5 had been grounded during life test, thus, D3 had been reverse biased. Therefore, the degradation was attributed to a charge separation mechanism in the fringing field of the junction caused by ionic contamination in or on the passivation layers.

TABLE D12 - RESULTS OF THE LEAK TESTS AND BAKES OF THE 26 PARTS NOT ANALYZED IN DETAIL

S/N	LEAK TEST RESULTS (P=PASSED, F=FAILED) FINE	GROSS	RESULTS OF UNPOWERED BAKES
A133	P	P	WORSE
B135	P	F	RECOVERED
B105	P	P	↓
B121	P	F	
C104	P	P	
C113	P	P	
A225	P	P	RECOVERED
A183	P	P	WORSE
B91	P	P	RECOVERED
B94	F	P	NO CHANGE
B142	P	P	RECOVERED
B154	P	P	RECOVERED
C75	P	P	NO CHANGE
B201	P	P	NO CHANGE
B124	P	P	RECOVERED
B141	P	P	NO CHANGE
B101	P	F	RECOVERED
B153	P	P	WORSE
B103	P	F	RECOVERED
B114	P	P	(RECOVERED AWAITING ANALYSIS)
B122	P	P	↓
B151	P	F	
C85	P	P	
B45	P	P	(BAKED AND RECOVERED AFTER STEP STRESS)
B34	P	P	↓
C35	P	F	

7.0 4017 DECADE COUNTER/DIVIDER - MANUFACTURER D

7.1 I_{SS} FAILURES

One hundred seventy-nine (179) parts (72 Lot A, 59 Lot B, and 48 Lot C) failed I_{SS} [14] (inputs low) and/or I_{SS} [15] (inputs high) during step-stress and accelerated life. Of these, twenty-eight (28) parts had first failed I_{SS}, V_{OH2}, or V_{OL2}, at +125°C or -55°C only, were left on test, and eventually failed I_{SS} at 25°C. Therefore, for purposes of statistical analysis and failure categorization these parts were considered as 25°C I_{SS} failures at the time of the 25°C failure.

Because the two specified I_{SS} tests do not give sufficient information about the part to troubleshoot or even categorize these failures, the I_{SS} leakage of each part was examined on a curve tracer while applying all combinations of inputs and while manually stepping through a counting sequence. The results of these tests, shown in Table D13, disclosed that there were 15 types of failures (the table lists only 166 parts because 9 Lot C step-stress failures had been baked and had recovered and because 4 life test failures had recovered while awaiting analysis). These patterns were not always clear cut since many of the parts displayed varying amounts of leakage during the majority of combinations of input conditions and counts. Such parts were listed according to the pattern which showed the greatest amount of constant leakage. Because of the complexity of the device, it was evident that all 15 failure types could not be fully investigated within the scope of this program. Consequently only the first six types of failure, representing 83% of the total I_{SS} failures, were investigated in detail.

The 4017 consists of five master/slave flip-flops (F/F0 through F/F4) connected as a Johnson counter through transmission gates. It also contains a gating circuit between F/F1 and F/F2, a carry-out inverter, and ten output NOR gates. The type 6 failures showed excessive current only when outputs "0" and "1" were high, which indicated that the problem was located at the "0" and "1"

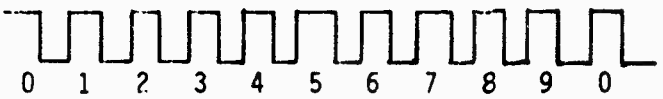
TABLE D13 - RESULTS OF CURVE TRACER TROUBLESHOOTING OF THE I_{SS} FAILURES

FAILURE TYPE	FAILURE PATTERN	QUANTITY OF PARTS Lot A	Lot B	Lot C
1	I_{SS} GREATEST WITH 0, 1, 2, 3, 4 HIGH (C_{OUT} HIGH)	0	5	39
2	I_{SS} GREATEST WITH 7, 8, 9, 0, 1 HIGH	37	13	0
3	I_{SS} GREATEST WITH 9, 0, 1, 2, 3 HIGH	5	1	0
4	I_{SS} GREATEST WITH 6, 7, 8, 9, 0 HIGH	2	15	0
5	I_{SS} GREATEST WITH 8, 9, 0, 1, 2 HIGH	4	5	0
6	I_{SS} GREATEST WITH 0 AND 1 HIGH	12	11	0
7	I_{SS} GREATEST WITH 5, 6, 7, 8, 9 HIGH (C_{OUT} LOW)	3	0	0
8	I_{SS} GREATEST WITH 1, 2, 3, 4, 5 HIGH	0	1	0
9	I_{SS} GREATEST WITH 1 HIGH	1	0	0
10	I_{SS} GREATEST WITH RESET HIGH	1	0	0
11	I_{SS} GREATEST WITH CLOCK HIGH	1	1	0
12	I_{SS} GREATEST WITH ALL COMBINATIONS OF INPUTS	0	1	0
13	OUTPUTS 3 AND 7 DON'T SWITCH	0	1	0
14	COUNT STOPS AT 4	1	0	0
15	RANDOM PATTERNS	2	4	0
		69	58	39

output pins or in their NOR gates. The other five types of failure occurred only during a specific counting sequence. The possible locations of the leakage were determined from the diagnostic diagram shown in Figure D44. The diagram contains the states of the outputs of the master and the slave sections of each flip-flop, the output of the C_{OUT} inverter, and the output of the gating circuit during the counting sequence. By comparing the pattern of I_{SS} during counting to the pattern of logic states in the diagram, the suspect stages could be pin-pointed. The type 1 failures showed the greatest leakage when "0" through "4" were high, specifically during transitions listed in Figure D44 beneath the diagnostic diagram. The pattern indicated that the leakage was located in the C_{OUT} inverter or the slave of F/F4. The type 2 failures displayed the most leakage when "7" through "1" were high as shown in Figure D44, indicating that the leakage was located in the gating circuit or the slave of F/F1. Likewise, the types 3, 4 and 5 failures were indicative of leakage in the slave of F/F3, the slave of F/F0, and the slave of F/F2, respectively.

7.1.1 Type 1 Failures - Every Lot C part that failed during lot acceptance (39 parts) and five Lot B parts exhibited excessive I_{SS} due to leakage in the C_{OUT} inverter or the slave of F/F4. The leakage was very high, ranging into the tens of milliamperes. All of the Lot C parts had exhibited V_{OH1} and V_{OH2} parametric failures at pin 12 (C_{OUT}) due to the high leakage and this indicated that the leakage was located in the C_{OUT} stage rather than the F/F4 slave. Also, all of the Lot C parts exhibited V_{OH1} and V_{OH2} parametric failures at pin 11 ("9") and many of the parts also exhibited excessive leakage during count "9", which indicated that the Lot C parts also contained leakage in the pin 11 output NOR gate.

OUTPUT STATE OF EACH STAGE (H=HIGH, L=LOW)



STAGE																						
F/F0 - MASTER	H	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	L
- SLAVE	H	H	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H
F/F1 - MASTER	H	H	H	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H
- SLAVE	H	H	H	H	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H
F/F2 - MASTER	H	H	H	H	H	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H
- SLAVE	H	H	H	H	H	H	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H
F/F3 - MASTER	H	H	H	H	H	H	H	L	L	L	L	L	L	L	L	L	H	H	H	H	H
- SLAVE	H	H	H	H	H	H	H	H	L	L	L	L	L	L	L	L	L	H	H	H	H
F/F4 - MASTER	H	H	H	H	H	H	H	H	H	L	L	L	L	L	L	L	L	L	H	H	H
- SLAVE	H	H	H	H	H	H	H	H	H	H	L	L	L	L	L	L	L	L	L	H	H
C_{OUT} INVERTER	H	H	H	H	H	H	H	H	H	H	L	L	L	L	L	L	L	L	L	H	H
GATING CIRCUIT	H	H	H	H	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H

FAILURE TYPE																						
FAILURE SYMPTOMS	TYPE 1:	X	X	X	X	X	X	X	X	X	X										X	X
	TYPE 2:	X	X	X	X									X	X	X	X	X	X	X	X	X
	TYPE 3:	X	X	X	X	X	X	X	X										X	X	X	X
	TYPE 4:	X	X									X	X	X	X	X	X	X	X	X	X	X
	TYPE 5:	X	X	X	X	X	X										X	X	X	X	X	X

X=I_{SS} GREATEST DURING THESE TRANSITIONS

FIGURE D44-I_{SS} DIAGNOSTIC DIAGRAM FOR THE MANUFACTURER D 4017

Analysis of these parts established that the high leakage was due to excessive I_{DSS} in N-channel transistor N17 of the C_{OUT} inverter (all parts) and N-channel transistor N20 of the "9" NOR gate (most of the parts). I_{DSS} of N17 and N20 were channeled, as illustrated in Figures D45 and D46, and the drain to source leakage could be pinched off by applying a negative voltage from gate to source. In each case, the leakages were bake recoverable. These findings indicated that the high I_{DSS} was due to inversion of the channel region caused by the accumulation of a net positive charge at the gate oxide/silicon interface. During life test, the gate, drain, and source-body of N20 were low and the gate and source-body of N17 were low. Since there was no applied field across the gate oxides of N20 or N17, the charge accumulation could not have resulted from conventional cation drift through the gate oxide. An identical n-channel transistor failure mode in a Manufacturer D CMOS device has been observed and investigated during a previous high temperature accelerated life test conducted for RADC by this laboratory [1]. In this instance, the instability was attributed to moisture that had accumulated in the package due to outgassing of the epoxy die attach material used by Manufacturer D. Since the Manufacturer D 4017 also uses epoxy die attach, it is suspected that these failures may also have been caused by outgassing.

7.1.2 Type 2 Failures - Thirty-seven (37) Lot A parts and thirteen (13) Lot B parts showed greatest leakage during counts "7" through "1" indicating that the leakage was located in the F/F2 input gating circuit or the slave of F/F1. Analysis of these parts established that the leakage was due to excessive I_{DSS} in p-channel transistor P26 of the gating circuit. P26 exhibited a channeled reverse characteristic, as illustrated in Figure D47, nominal threshold voltage, and the drain-source leakage could not be pinched off with positive gate-source voltage. These findings indicated that P26 contained a degraded drain junction. The degradation was bake reversible indicating a

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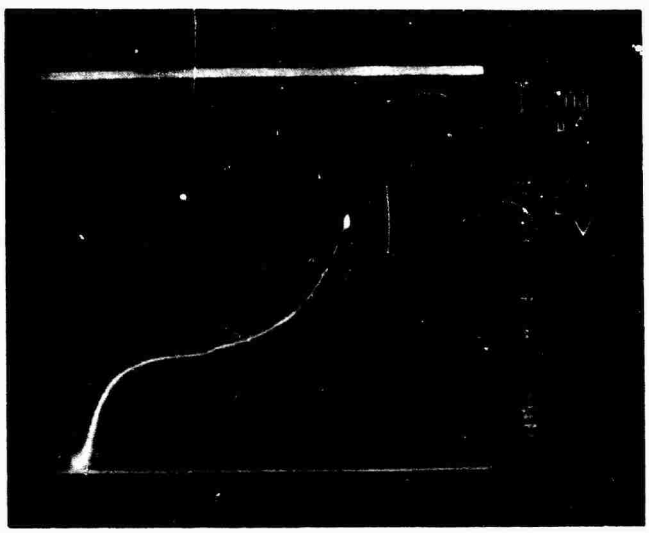
[1] G. M. Johnson, "Voltage Stress Effects on Microcircuit Accelerated Life Test Failure Rates", NASA Contract NAS8-31177, July 1976.

I_{DSS}

V_{D-S} S/N C82 (120 HRS/250°C)

FIGURE D45 - I_{DSS} C_{OUT} CHARACTERISTIC OF N17 OF THE INVERTER.

I_{DSS}



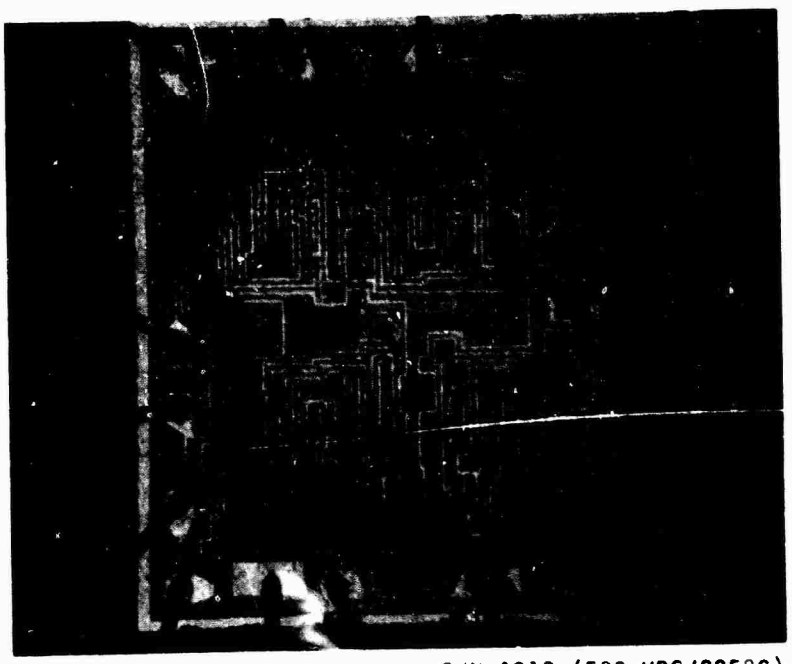
V_{D-S} S/N C82 (120 HRS/250°C)

FIGURE D46 - I_{DSS} CHARACTERISTIC OF N20 OF THE "9" OUTPUT STAGE.

I_{DSS}

V_{D-S} S/N A193 (1000 HRS/225°C)

FIGURE D47 - I_{DSS} CHARACTERISTIC OF P26.



40X S/N A212 (500 HRS/225°C)

FIGURE D48 - EXAMPLE OF THE CONDITION OF THE DIE AFTER PARTIAL GLASSIVATION ETCH.

surface related mechanism. During life test, the drain junction of P26 was reverse biased (P26 was "off"), thus the degradation was probably caused by mobile ions in the passivation which separated in the fringing field of the reverse biased junction.

7.1.3 Type 3,4 and 5 Failures - Eleven (11) Lot A parts and twenty-one (21) Lot B parts exhibited I_{SS} patterns that, in terms of greatest leakage, indicated that the leakage was located in the slave section of F/F0, F/F2, or F/F3. However, the patterns in these parts were almost always ambiguous due to overlapping of patterns, and due to the presence of other leakages within the part. For example, S/N221 exhibited the pattern shown in Table D14 in the "initial test" column. I_{SS} was a constant (30 μA) during counts "6" through "0", indicative of leakage in the slave of F/F0. I_{SS} also was appreciable and was fluctuating during counts "1" through "5", indicating that there were several other leakage sites within the circuit. Also, the I_{SS} values drifted with time and applied bias of room temperature. The second and third columns (1st retest and 2nd retest) of Table D14 shows the values of I_{SS} of S/N B221 after two one-minute intervals of applied bias. Because the patterns were ambiguous and because they were not repeatable, it was not possible to externally pin-point the leaky transistors or to establish the component values of the leakages with any certainty. Die level probing of representative samples of these type failures to isolate the leakages was unsuccessful. The glassivation layer on these parts would etch unevenly, as illustrated in Figure D48, and as a result the glassivation on the interior of the die was removed before the glass on the periphery of the die. The transistors of interest were located close to the periphery, but before they could be completely exposed for probing the interior transistors were undercut and severely degraded making quantitative and qualitative investigation of I_{SS} impossible. It was suspected that the uneven etching was caused by uneven distribution of phosphorous in the glassivation, but it is not known whether the glassivation problem had contributed to the failure of these devices. Because of the difficulties encountered, this group of failures was not investigated further.

TABLE D14 - I_{SS} VALUES OBTAINED DURING CURVE TRACER TESTS OF S/N B221

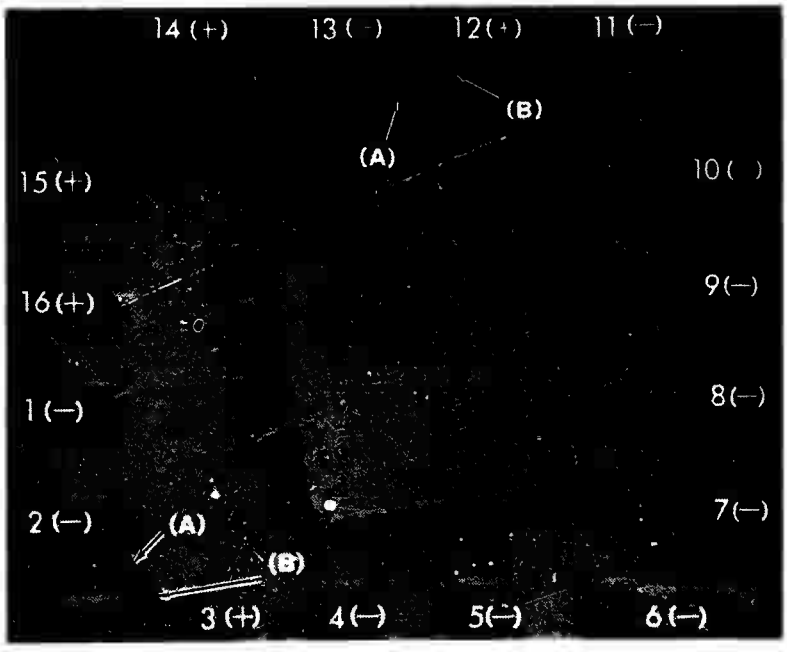
COUNT	CLOCK STATE	I_{SS} (microamperes)		
		INITIAL TEST	1st RETEST	2nd RETEST
0	H	30	-	-
	L	30	-	-
1	H	20	200	250
	L	8	150	200
2	H	18	160	210
	L	5	110	150
3	H	18	150	180
	L	5	100	130
4	H	18	130	150
	L	4	80	100
5	H	15	50	70
	L	2	10	20
6	H	30	160	180
	L	30	130	140
7	H	30	200	220
	L	30	180	200
8	H	30	240	250
	L	30	200	230
9	H	30	250	280
	L	30	230	260
0	H	30	300	300
	L	30	300	340

All remaining parts were baked and recovered, thus these failures could be at least categorized as surface related failures.

7.1.4 Type 6 Failures - Twelve (12) Lot A and eleven (11) Lot B parts exhibited excessive I_{SS} whenever "0" and "1" were high. Also, most of these parts exhibited V_{OL} and V_{OH} high failures and timing errors associated with these two outputs and other outputs as well. The failures were traced to high resistance shorts between adjacent pins. Each part contained a resistive short (ranging from 2K ohms to 100K ohms) between pin 3 ("0") and pin 2 ("1"). Some parts also contained a short between pins 12 (C_{OUT}) and 13 (Inhibit) or pins 11 ("9") and 12 or pins 16 (V_{DD}) and 1("5").

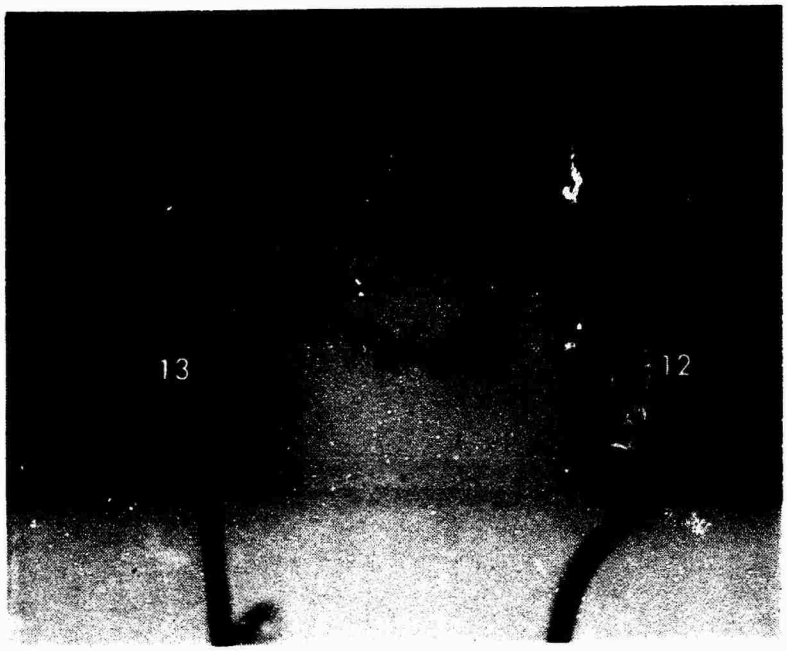
The shorts were caused by a trail of conductive dendritic growth bridging between the internal deposited package lead frames as illustrated in Figures D49 through D51. The growth was located on the surface of the ceramic and usually emanated from an obvious residue on the edge of the frame. The growth always occurred between a pin that had been positively biased and a pin that had been grounded during life test indicative of electrolytic reaction. SEM x-ray analysis of a failure site, Figure D52, disclosed that the growth was composed of nickel (from the lead frame), as shown in Figure D53, and that the residue contained phosphorous and chlorine as shown in Figure D54. These findings indicated that a chemical residue had been left in the package during manufacturing and this, combined with the applied bias (and possible moisture from outgassing of the die attach epoxy), caused an electrolytic reaction to occur that resulted in migration of nickel across the surface of the ceramic.

7.1.5 Type 7 Through 15 Failures (Not Analyzed in Detail) - These 17 parts were baked and I_{SS} of all but one part recovered. Fine and gross leak tests of the parts disclosed no loss of hermeticity in any part. These 17 bake recoverable parts, along with the 4 life test failures that had recovered while awaiting analysis, are listed together as surface-related failures on the analysis summaries.



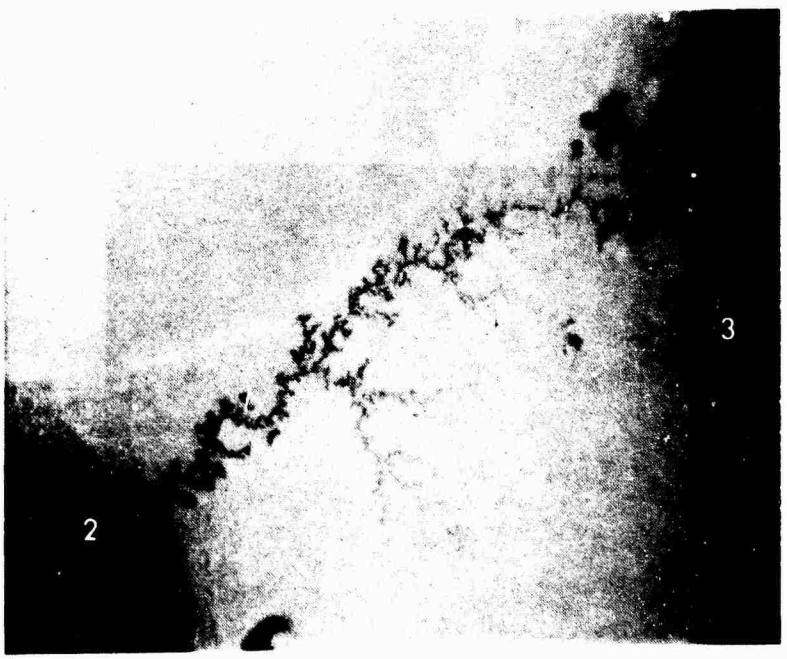
19X S/N A72 (500 HRS/250°C)

FIGURE D49 - INTERIOR OF THE PACKAGE SHOWING DENDRITE GROWTH (A) BETWEEN PINS 2 AND 3 AND BETWEEN PINS 12 AND 13, THE RESIDUE ON PINS 3 AND 12 (B), AND THE BIAS ON EACH PIN DURING LIFE TEST. (+ = +15 VOLTS, - = GROUND).



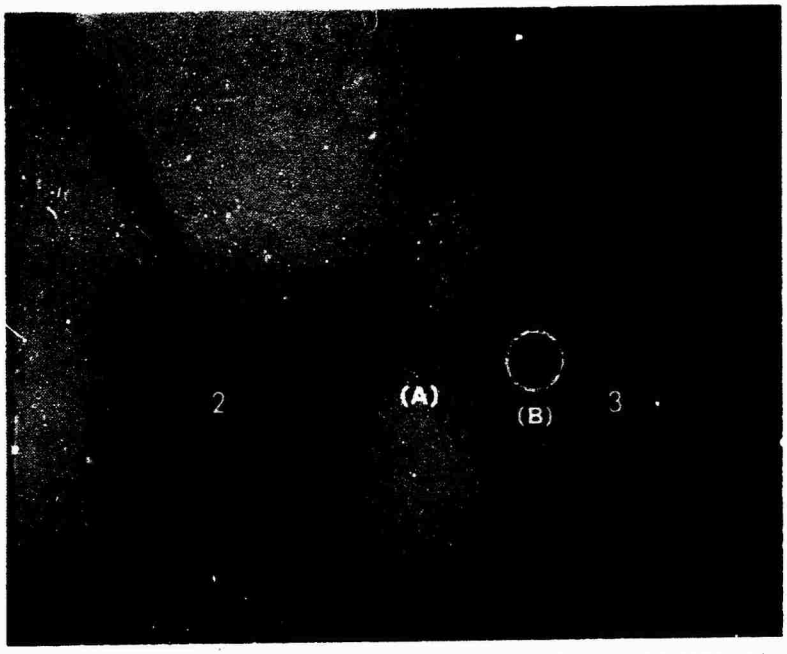
80X S/N A72 (500 HRS/250°C)

FIGURE D50 - CLOSE-UP OF THE GROWTH BETWEEN PINS 12 AND 13.



256X S/N A72 (500 HRS/250°C)

FIGURE D51 - CLOSE-UP OF THE GROWTH BETWEEN PINS 2 AND 3.



80X S/N A112 (500 HRS/250°C)

FIGURE D52 - CLOSE-UP OF THE GROWTH AND RESIDUE IN THE PART EXAMINED USING SEM X-RAY ANALYSIS SHOWING THE AREAS SCANNED (ENCIRCLED).

FIGURE D53 - X-RAY SPECTRUM OF THE DENDRITE GROWTH (AREA "A" OF FIGURE D52).

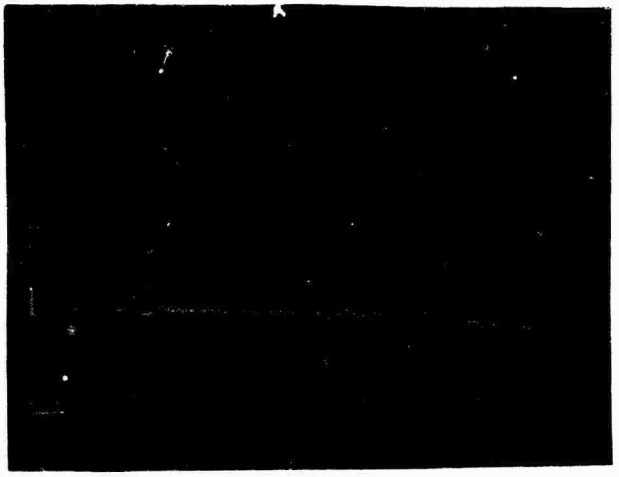


FIGURE D54 - X-RAY SPECTRUM OF THE RESIDUE (AREA "B" OF FIGURE D52).

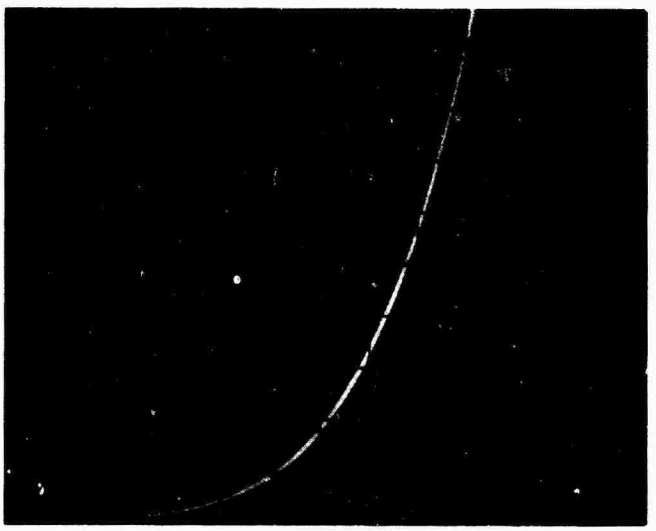
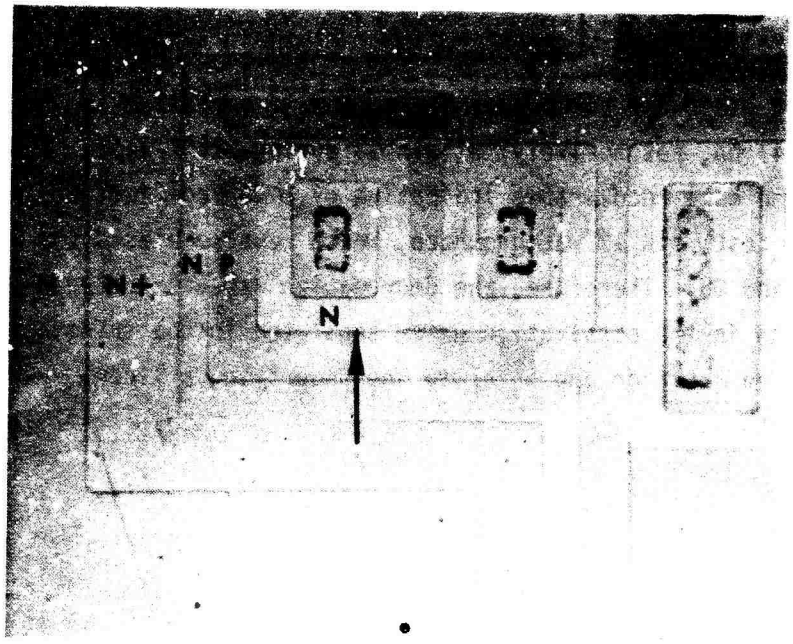


FIGURE D55 - EXAMPLE OF PIN 13 I_{IH} I-V CHARACTERISTIC.

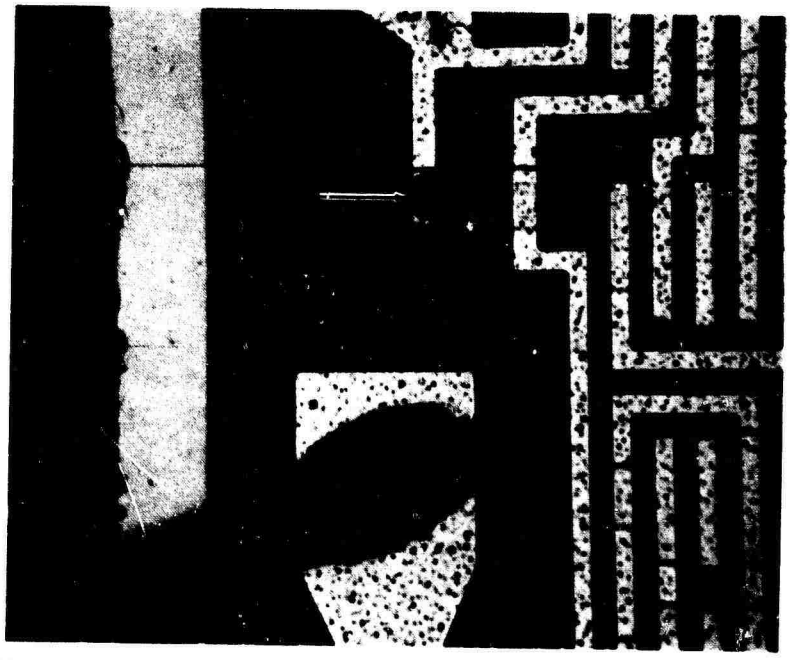
7.2 I_{IH} [1] FAILURES - DAMAGED INPUT DIODE

Eight (8) Lot A parts and fourteen (14) Lot B parts failed due to excessive I_{IH} [1] current at pin 13, the clock inhibit, during step-stress and accelerated life. The failed values ranged from 17 nA to 13 μA. The leakage was always exponential, as illustrated in Figure D55, and was not bake recoverable, which was indicative of a bulk-related mechanism. The leakage was traced to a degraded input protection diode, D6, between pin 13 and V_{SS}. In instances where the leakage was in the nanoampere range, the diode contained no discernible damage or defect as illustrated in Figure D56. In instances where the leakage was in the microampere range, the diode contained visibly burned or swollen metallization at the cathode ohmic contact as illustrated in Figure D57. The damage indicated that the degradation was caused by excessive current through D6. During life test, pin 13 and V_{SS} were connected to ground, thus no current should have flowed through D6 at elevated temperature. However, the other two inputs, pins 14 and 15, were connected to V_{DD} (+15 volts) during life test and in no instance did a pin 14 or a pin 15 sustain any damage. This suggested that the damage was related to life test conditions and not the result of an external overstress that occurred during handling or testing of the parts. A possible explanation was that the external connection between the V_{SS} lead and ground opened at elevated termperature. With V_{SS} open, the entire device current would flow to ground via D6 and pin 13. Experiments disclosed that the device current under these conditions (open V_{SS} and elevated temperature) was excessive (due to a latch-up effect) and of sufficient magnitude to damage D6. Continuity checks of the life test chassis disclosed open V_{SS} solder joints associated with the parts that had failed I_{IH} [1], thus confirming the suspected cause of failure.



490X S/N A273 (260°C STEP)

FIGURE D56 - DIODE D6 (ARROW) AFTER SILICON ETCH.



256X S/N B162 (250 HRS/225°C)

FIGURE D57 - EXAMPLE OF DAMAGED D6 CATHODE OHMIC CONTACT (ARROW).

7.3 I_{IL} [4] FAILURES - CHANNELED INPUT DIODE

One Lot A and one Lot B part failed due to excessive I_{IL} [4] current (22 nA and 47 nA, respectively) at pin 13 during 225°C life. The leakage was channeled and bake recoverable indicative of a surface instability mechanism. During life test, pin 13 was grounded, which reverse biased the input diodes to V_{DD}, D4 and D5. Therefore, the degradation was attributed to ionic contamination in the passivation which separated in the fringing field of the reverse biased junction and inverted the underlying silicon.

8.0 4017 DECADE COUNTER/DIVIDER - MANUFACTURER A

8.1 I_{SS}, I_{IH}, OR V_{OH2} FAILURES - PIN-PIN SHORTS (Pb PRECIPITATION)

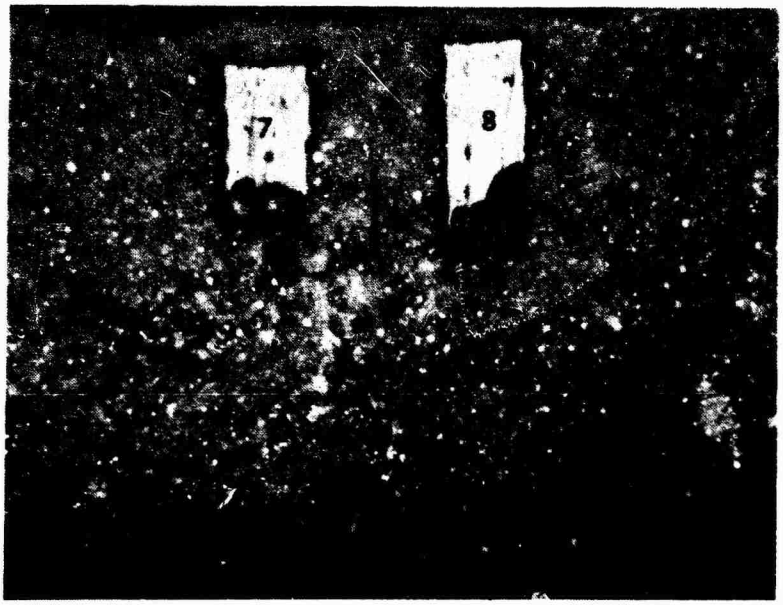
During accelerated life, thirteen (13) Lot A and ten (10) Lot B parts failed I_{SS}, I_{IH}, I_{IL}, or V_{OH2} due to high resistance (kilohn to megohm), sometimes intermittent, shorts between adjacent package leads. A complete summary of the location of the short in each part and the resultant parametric failures is presented in Table D15. Eleven parts contained a short between pin 13 (clock enable) and pin 14 (clock). The pins 13-14 shorts resulted in I_{IH} [1] and I_{IH} [2] failures, ranging from 33 nA to 1 mA, since one pin is connected to V_{DD} and the other to V_{SS} during measurement of I_{IH}. Two parts contained a short between pin 12 (C_{OUT}) and pin 13. The pins 12-13 shorts resulted in I_{IL} [4] failures, 14 and 39 nA, since pin 13 is connected to V_{SS} and pin 12 is high during measurement of I_{IL} [4]. Ten parts contained a short between pin 9 (count "8") and pin 8 (V_{SS}). The pins 9-8 shorts resulted in V_{OH2} failures at pin 9, ranging from 14.977 to 14.642 volts, because the short loaded the output during measurement of V_{OH2}. The shorts resulted in I_{SS} [14] (all inputs low) failures, ranging from 25 to 469 nA, because pin 9 may be high during measurement of I_{SS} [14] (low). The shorts were traced to lateral trails of conductive dendrite growth in the glass seal, bridging between adjacent package pins as illustrated in Figure D58. The growth was identical to that which occurred in the Manufacturer A 4001 package and was attributed to Pb reduction and precipitation as described in Section 3.3. The Manufacturer A 4017 package is identical to the 4001 package; therefore, the 4017 failures were likewise attributed to Pb dendrite growth.

8.2 V_{OH2} FAILURES - CATION DRIFT

Seven (7) Lot A parts and one (1) Lot B part failed V_{OH2} at pin 1 (3 parts), pin 3 (1 part), pin 6 (3 parts), or pin 7 (1 part) during accelerated

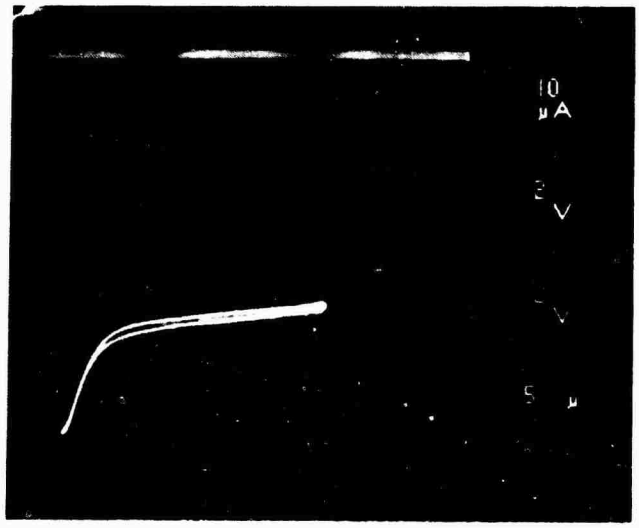
TABLE D15 - SUMMARY OF FAILURES DUE TO PIN-PIN SHORTS

LOT/TEMP	S/N	TIME OF FAILURE	FAILED PARAMETERS	LOCATION OF SHORT
A-225°C	A233	250	I_{IH} [1] AND I_{IH} [2]	PIN 13 TO PIN 14
	A221	500		
	A213	4000		
	A223	4000		
B-250°C	B34	3000		
B-225°C	B234	1000		
	B204	2000		
	B244	2000	I_{IH} [1]	
	B211	4000	I_{IH} [2]	
	B231			
	B232			
B-250°C	B124	3000	I_{IL} [4]	PIN 13 TO PIN 12
B-225°C	B241	2000		
A-250°C	A33	2000	V_{OH2}(PIN 9) AND I_{SS} [14]	PIN 9 TO PIN 8
	A71	3000	V_{OH2}(PIN 9)	
	A91			
	A92			
	A122			
A-225°C	A203	2000		
	A231		V_{OH2}(PIN 9) and I_{SS} [14] (INPUTS LOW)	
B-250°C	B131	3000	V_{OH2}(PIN 9)	
A-250°C	A43	1000	I_{SS} [14] and I_{SS} [15]	PIN 9 TO PIN 8
	A93	2000	I_{SS} [14]	



40X S/N A203 (2000 HRS/225°C)

FIGURE D58 - CROSS-SECTION OF THE PACKAGE SHOWING THE DENDRITE GROWTH (ARROW) BETWEEN PINS 8 AND 9.



I_{DRAIN}

$V_{DRAIN-SOURCE}$ (V_{GS} = 0V) S/N A141 (500 HRS/250°C)

FIGURE D59 - EXAMPLE OF A CHANNELED I_{DSS} CHARACTERISTIC OF N19 OF PIN 1.

life. The failed values ranged from 14.987 to 14.120 volts. The low V_{OH2} was traced to loading of the output caused by excessive leakage (7 μA to 2.3 mA) in the n-channel output transistor, N19, that is off during the V_{OH2} test. N19 displayed a channeled I_{DSS} characteristic, as illustrated in Figure D59, and the leakage was bake recoverable, indicative of a surface related mechanism. In most instances, the drain-source leakage could be pinched off by the application of negative gate-source voltage. This indicated that the leakage was due to inversion of the channel caused by the accumulation of a net positive charge at the gate oxide/silicon interface. During life test the pins 1, 6, and 7 N19 transistors were "on" ("5", "7", and "3" were low), thus the charge accumulation in these transistors was probably caused by cation drift through the gate oxides. The pin 3 N19 transistor was "off" during life test ("0" was high), thus the failure of this transistor was probably caused by charge separation in the fringing field of the reverse biased drain junction.

8.3 MISCELLANEOUS I_{SS} FAILURES - SURFACE INSTABILITY

Twelve (12) Lot A, one (1) Lot B, and one (1) Lot C parts failed I_{SS} [14] and/or [15] during step-stress or life test due to surface related mechanisms. The results of curve tracer troubleshooting of these 14 parts, in the manner described in Section 8.1.0, is presented in Table D16. The step-stress failure had been baked and had recovered, and 4 parts had recovered while awaiting analysis. The other 9 parts exhibited 8 different types of failures; consequently, these 9 random failures were not analyzed in detail. All 9 parts were baked and every part recovered. Fine and gross leak tests of these parts disclosed no loss of hermeticity and microscopic examination of their interiors revealed no discrepancy. Thus, these 14 failures were classified as surface related and the exact failure mode, mechanism and cause was not established.

TABLE D16 - RESULTS OF CURVE TRACER TROUBLESHOOTING OF THE I_{SS} FAILURES

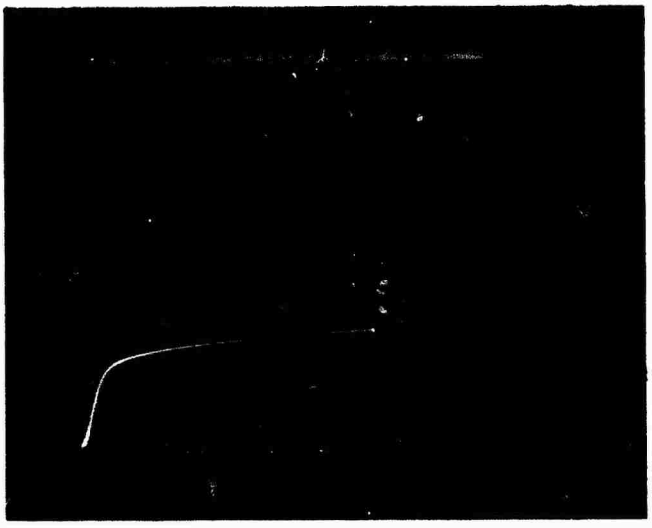
FAILURE PATTERN	QUANTITY OF PARTS					
	LOT A				LOT B	LOT C
	STEP-STRESS	250°C	225°C	125°C	250°C	250°C
I_{SS} GREATEST WITH 7, 8, 9, 0, OR 1 HIGH	0	0	0	1	0	0
2, 3, 4, 5, OR 6 HIGH	0	0	0	0	0	1
5, 6, 7, 8, 9, OR 0 HIGH	0	1	0	0	0	0
0, 1, 2, 3, 4, 6, 7, 8, OR 9 HIGH	0	0	0	0	1	0
9, 0, 1, OR 2 HIGH*	0	1	0	0	0	0
ANY OUTPUT HIGH	0	1	1	0	0	0
RESET HIGH	0	0	1	0	0	0
RESET LOW	0	1	0	0	0	
I_{SS} RECOVERED WHILE AWAITING ANALYSIS	0	1	3	0	0	0
I_{SS} RECOVERED AFTER BAKING	1	0	0	0	0	0
	1	5	5	1	1	1

*COUNT 8 IS STUCK HIGH DURING THESE COUNTS.

9.0 4008 FOUR BIT FULL ADDER - MANUFACTURER D

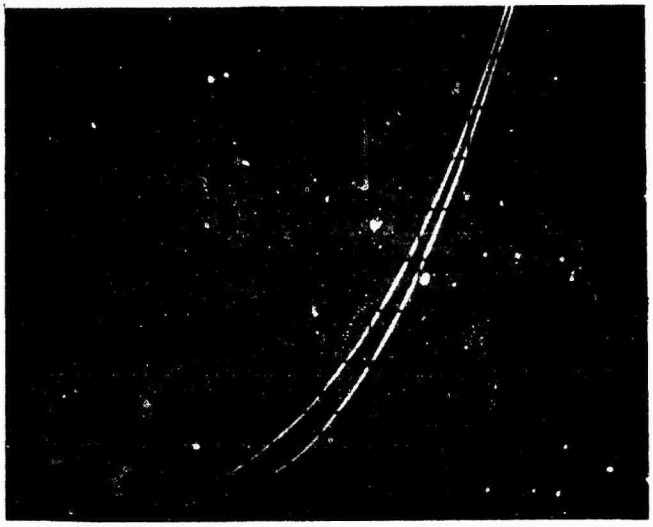
9.1 I_{SS} FAILURES

One hundred-fourteen (114) parts (58 Lot A, 54 Lot B, and 2 Lot C) failed due to excessive I_{SS} during accelerated life and lot acceptance. Each part failed from 2 to 28 of the specified 28 I_{SS} tests, and there were no distinct patterns by which to categorize the failures. The 28 I_{SS} tests were of no use in troubleshooting the parts to isolate the leakage to a specific transistor(s) within the part. This was because the 4008 contains nine inputs and therefore a total of 512 (2^9) combinations of inputs conditions would be necessary to completely isolate any leakage in the part. The specified I_{SS} tests represent only a random selection of 28 of these combinations. Examination of all 28 I_{SS} values (both failed and unfailed) of each part revealed that all 28 values were either failed or high in 91% (104/114) of the parts. This meant that most of the parts either contained a leaky p-well junction or contained multiple leaky transistors (or both). To determine if the parts could possibly contain a single common failure mode, five parts failing all 28 I_{SS} tests were selected and their p-well junctions were evaluated. The Manufacturer D 4008 contains three p-well diffusions. The diffusions were isolated, probed, and measured in each part. Two of the parts each contained one degraded p-well that accounted for the I_{SS} failures displayed by each part. The reverse I-V characteristic of the p-wells was channeled, as illustrated in Figure D60, and was bake recoverable indicative of a surface related mechanism. The other three parts contained no p-well leakage and this indicated that the excessive I_{SS} was due to multiple leaky circuit transistors. There was no way to determine externally which of the five parts contained a leaky p-well and which did not. Consequently, the failure categorization and failure modes of these parts could only be established by die level probing of every part. This would be impractical in the case of parts with multiple leaky transistors since the Manufacturer D 4008 contains 168 transistors and external tests could not establish which transistors were leaky. Therefore, the remaining parts were not analyzed in detail. All parts



S/N A112 (64 HRS/225°C)

FIGURE D60 - EXAMPLE OF THE REVERSE I-V CHARACTERISTICS OF A DEGRADED P-WELL JUNCTION.



I_{IH} = 100nA/DIV

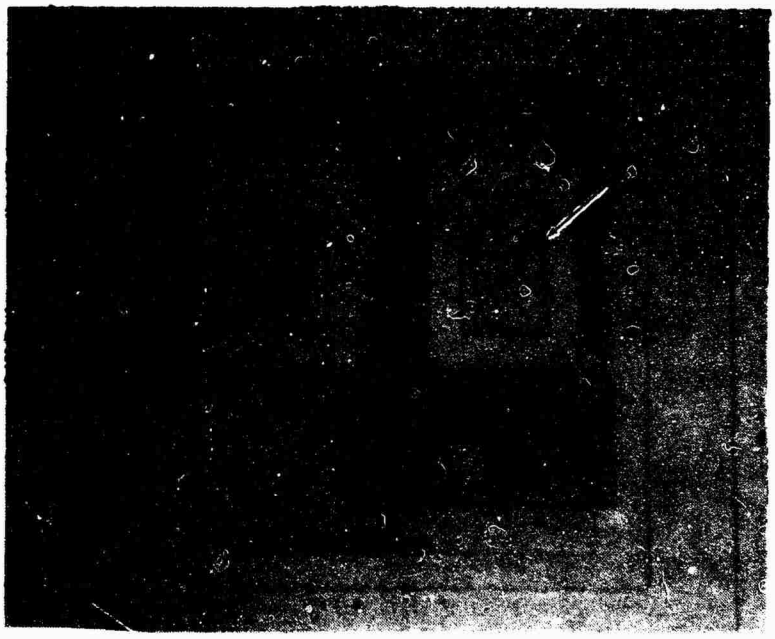
V_{IH} = 2 VOLTS/DIV S/N B33 (200°C STEP)

FIGURE D61 - I_{IH} I-V CHARACTERISTIC OF PIN 7 (L/H TRACE) AND PIN 15 (R/H TRACE).

were baked and I_{SS} in each part recovered, therefore all 114 I_{SS} failures were classified as surface instability failures.

9.2 I_{IH1} FAILURES - DAMAGED INPUT DIODE

During the tests 17 parts (7 Lot A, 9 Lot B, and 1 Lot C) failed due to excessive I_{IH1} (all inputs together) that was not bake reversible. Troubleshooting disclosed that each part contained one to three degraded inputs. One part contained a degraded pin 5, six a degraded pin 6, seventeen a degraded pin 7, and four a degraded pin 15. The leakage was always exponential, as illustrated in Figure D61, and ranged from 15 to 6500 nanoamperes. The leakage was traced to a degraded input-to-V_{SS} protection diode. Each input of the Manufacturer D 4008 device contains two input-to-V_{SS} diodes, one on either side of the input series resistor. In each instance, only the diode connected directly to the input pin (D18, D21, D24 or D3) was degraded. Examinations of the diodes disclosed no bulk damage, as illustrated in Figure D62. During life test, pins 5, 6, 7, 15, and V_{SS} were connected to ground, consequently no bias was applied across the diodes which had degraded and no current should have flowed through the diodes at elevated temperature. The absence of obvious damage and the fact that the diodes which had failed had had zero applied bias suggested that the degradation might have been due to static discharge during handling or electrical transients during testing. However, the other five inputs of the device, pins 1, 2, 3, 4 and 9 were connected to V_{DD} (+15 volts) during life test and no instance of this type of degradation occurred at one of these inputs. This indicated that the degradation was related to the life test conditions and not the result of an external overstress. A possible explanation was that the external connection between the V_{SS} lead and ground had opened at elevated temperature. With V_{SS} open, the entire device current would flow to ground by forward biasing the input diodes of the grounded inputs. Experiments showed that the device current at elevated temperature was excessive with V_{SS} open (due to a latch-up effect) and of sufficient magnitude to degrade the input diodes not protected by the series resistor (those connected directly to the input).



490X S/N B114 (250 HRS/225°C)

FIGURE D62 - P-N JUNCTION (ARROW) OF THE DEGRADED PIN 7-TO-VSS INPUT DIODE (DELINEATED BY SILICON ETCH).

Continuity checks of the life test chassis disclosed instances of open V_{SS} solder joints associated with the parts that contained a degraded pin 5, 6, 7 or 15 input, which substantiated the hypothesis.

9.3 I_{IH1} OR I_{IL1} FAILURE - CHANNELED INPUT DIODE

During accelerated life and lot acceptance, 11 parts (4 lot A, 4 Lot B, and 3 Lot C) failed due to excessive I_{IH1} (all inputs together) and 2 parts (1 Lot B and 1 Lot C) failed due to excessive I_{IL1} (all inputs together) that were bake reversible. Troubleshooting established that each part failing I_{IH1} contained one degraded input. One part contained a degraded pin 1, three contained a degraded pin 2, two contained a degraded pin 3, two contained a degraded pin 4, and one contained a degraded pin 9 (two parts had recovered while awaiting analysis). Of the parts failing I_{IL1}, one contained a degraded pin 6, the other a degraded pin 7. The leakage was always channeled and ranged from 10 to 370 nanoamperes. The leakage was traced to channeled input protection diodes between the input and V_{SS} in the I_{IH} failures and between the input and V_{DD} in the I_{IL} failures. During life, pins 1, 2, 3, 4 and 9 were connected to V_{DD} which reverse biased the input-to-V_{SS} diodes. Pins 5 and 6 were grounded which reverse biased the input-to-V_{DD} diodes. Therefore the reversible degradation was attributed to charge separation in the fringing field of the reverse biased junctions caused by the presence of ionic contamination in or on the passivation layers.

10.0 4008 FOUR BIT FULL ADDER - MANUFACATURER C

10.1 I_{SS} FAILURES - SURFACE INSTABILITY

During accelerated life and lot acceptance, thirty-five (35) parts (26 Lot A, 8 Lot B, and 1 Lot C) failed due to excessive I_{SS}. Each part failed 3 to 28 of the 28 specified I_{SS} parametric tests. The 28 specified tests were of no use in troubleshooting or categorizing these failures, but the pattern of failure in each part did indicate that it would be possible to troubleshoot these failures to some extent if an appropriate method were developed.

The 4008 contains four full adder stages (F.A. 1 through F.A. 4) and a high speed parallel carry-out circuit. By evaluating the leakage of each part on a curve tracer using the sequence shown in Table D17, the leakage could be isolated to a particular stage of the device and then narrowed down to a few suspect transistors when the device contained a single leaky transistor or contained one transistor with leakage appreciably greater than the leakage of any other transistor. Tests 1 through 26 were used to determine if the leakage was located in one of the full adders. If the leakage was located in a full adder the suspect transistor(s) could be determined by evaluating the pattern of leakage using the diagnostic matrix shown in Figure D63. The explanation of the diagnostic matrix is similar to that for the 4013 matrix discussed in section 5.1. If a failure, originally detected in a full adder, did not match a pattern shown in the matrix or if no leakage were detected in any full adder the high speed parallel carry circuit was investigated. Tests 27 through 40 were performed to determine the location of leakage in the high speed parallel carry circuit.

The results of curve tracer diagnostic tests of the 35 parts are shown in Table D18. Seven parts had recovered while awaiting analysis and two parts contained multiple random leakages, all of similar value, which could not be deciphered. The other 26 parts exhibited ten types of failure indicating a variety of possible problems. To completely categorize these failures most of

TABLE D17 INPUT LOGIC STATES FOR THE I_{SS} DIAGNOSTIC TESTS

	INPUT LOGIC STATES									
	A_4	B_4	A_3	B_3	A_2	B_2	A_1	B_1	C_{1N}	
TEST NO.										POSSIBLE LEAKY TRANSISTORS OR STAGES
1	0	0	0	0	0	0	0	0	0	
2	0	0	0	0	0	0	0	0	1	
3	0	0	0	0	0	0	0	1	0	
4	0	0	0	0	0	0	0	1	1	F. A. #1
5	0	0	0	0	0	0	1	0	0	
6	0	0	0	0	0	0	1	0	1	
7	0	0	0	0	0	0	1	1	0	
8	0	0	0	0	0	0	1	1	1	
9	0	0	0	0	0	1	0	0	0	
10	0	0	0	0	0	1	1	1	0	
11	0	0	0	0	1	0	0	0	0	
12	0	0	0	0	1	0	1	1	0	F. A. #2
13	0	0	0	0	1	1	0	0	0	
14	0	0	0	0	1	1	1	1	0	
15	0	0	0	1	0	0	0	0	0	
16	0	0	0	1	1	1	0	0	0	
17	0	0	1	0	0	0	0	0	0	
18	0	0	1	0	1	1	0	0	0	F. A. #3
19	0	0	1	1	0	0	0	0	0	
20	0	0	1	1	1	1	0	0	0	
21	0	1	0	0	0	0	0	0	0	
22	0	1	1	1	0	0	0	0	0	
23	1	0	0	0	0	0	0	0	0	
24	1	0	1	1	0	0	0	0	0	F. A. #4
25	1	1	0	0	0	0	0	0	0	
26	1	1	1	1	0	0	0	0	0	
27	1	0	1	0	1	0	1	1	0	N20+N21+N22+N23+N24+N26+N27+N28
28	1	0	1	0	1	0	1	0	0	N18+N19+N20+N21+N22+N23+P24+P25+P26+P27
29	1	0	1	0	1	1	1	1	1	N24+N26+N20+N21+N22+N23+P18•(P17+P19)
30	1	0	1	0	1	1	0	0	0	N24+N26+N27•N29+P18+P20
31	1	0	1	1	0	0	0	0	0	N24+N30•N26+P18
32	1	0	1	1	1	1	0	0	0	N24+N30•(N26+N29•N27)+P20+P18
33	1	1	0	0	0	0	0	0	0	N25+P18
34	1	0	1	0	1	0	0	0	0	P20+P25+P30+P29+P28+N18
35	1	0	1	0	0	0	1	0	0	P21+P25+P30+P29+P27•P28+N18
36	1	0	0	0	1	0	1	0	0	P22+P25+P20•(P29+P28)+N18
37	0	0	1	0	1	0	1	0	0	P23+P25+P24•(P30+P29+P28)+N18
38	0	0	0	0	0	0	1	0	1	P25+P26•P30+N17+N18
39	1	0	1	0	0	0	0	0	1	P25+P30+P29+P27•P28+P23+P21+N18+N17
40	0	0	1	1	1	1	1	1	1	P24+P25+P23+N17+N18

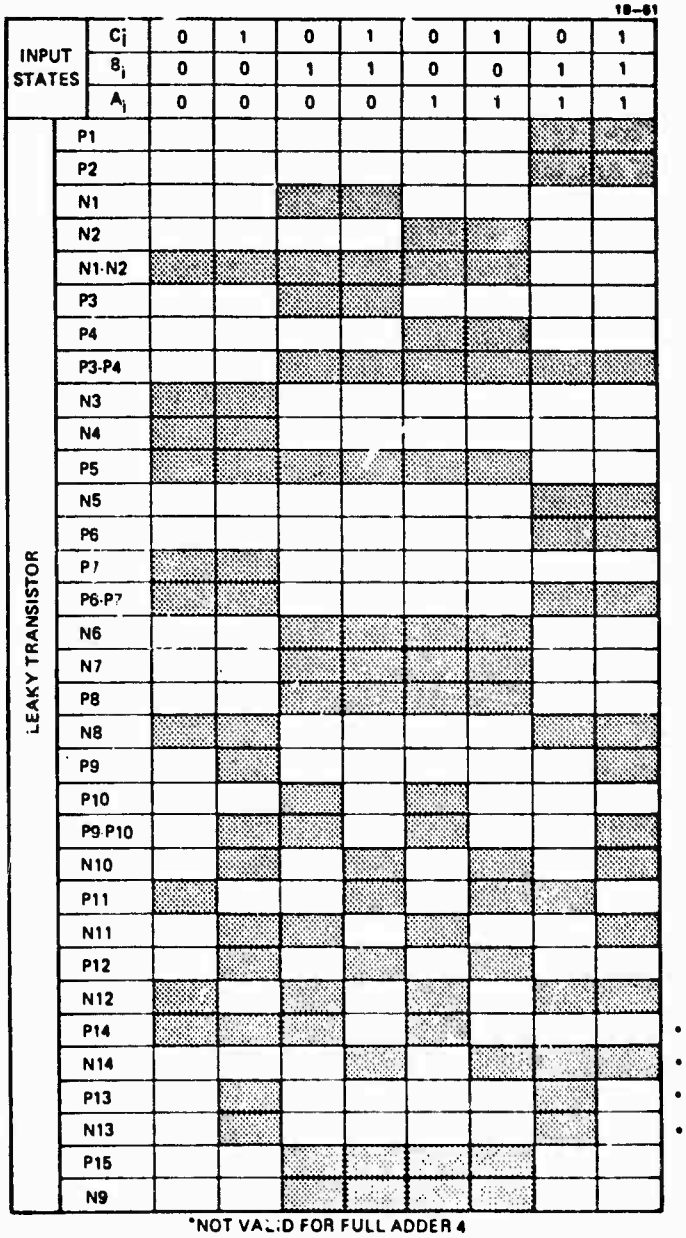


FIGURE D63. I_{SS} DIAGNOSTIC MATRIX FOR A FULL ADDER

TABLE D18 - RESULTS OF THE CURVE TRACER DIAGNOSTIC TESTS

POSSIBLE LEAKY TRANSISTORS	LOCATION OF LEAKY TRANSISTORS	QUANTITY OF PARTS		
		LOT A	LOT B	LOT C
N6, N7, N9, P8, OR P15	F. A. 1	1	0	0
	F. A. 2	1	0	0
	F. A. 3	1	0	0
N14	F. A. 2	0	1	0
	F. A. 3	1	0	0
P11	F. A. 1	0	1	0
P9, P19 or N11	F. A. 1	5	0	0
N3, N4, or P7	F. A. 4	2	0	0
N1 or P3	F. A. 1	1	0	0
P14	F. A. 2	1	0	0
N20, N21, N22, or N23	PARALLEL CARRY	4	1	0
N24 and/or N27	PARALLEL CARRY	3	1	0
N17	PARALLEL CARRY	1	0	0
P-WELL JUNCTION	-	0	0	1
MULTIPLE RANDOM	-	2	0	0
RECOVERED	-	3	4	0
		26	8	1

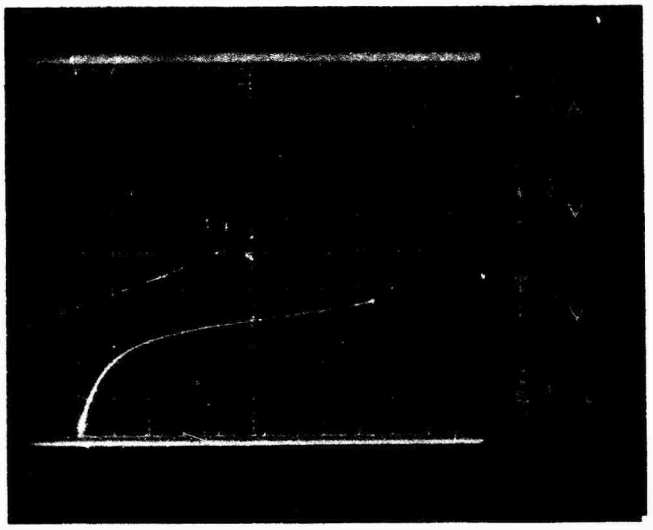
the parts would have to be individually probed and analyzed which was impractical. Consequently only representative examples were analyzed in detail. All other parts were baked and recovered. Analysis of the representative samples disclosed that the most common cause of the high I_{SS} was excessive I_{DSS} in an n-channel transistor that was "off" during life test. Five of eight parts investigated contained this failure mode. For example, S/N A234 failed 14 of the 28 specified I_{SS} parametric tests (about 80 μA each) after 1000 hours at 250°C. Curve tracer tests disclosed a leakage of 36 μA (partial recovery had ocurred) and external troubleshooting indicated that the leakage was caused by a leaky P9, P10, or N11 in F.A. 1. Die level probing of these transistors established that all of the leakage was confined to N11, the n-channel output transistor of F.A. 1. I_{DSS} of N11 was channeled, as shown in Figure D64, and recovered when the part was baked. During life test N11 was off (the output of F.A. 1 was high) which reverse biased the drain junction of N11. Therefore, the degradation was probably due to charge separation in the fringing field of the reverse biased junctions caused by ionic contaminaton in or on the passivation. Of the other three parts investigated, one contained excessive I_{DSS} in an n-channel transistor that had been "on" during life test, one containd a degraded p-well junction, and one recovered upon delidding.

10.2 I_{SS} OR I_{IL1} FAILURES - PIN-HEADER SHORTS (Pb Precipitation)

During accelerated life, 8 Lot A and 7 Lot B parts failed I_{SS}, V_{OH2}, I_{IH1}, or I_{IL1} due to high resistance shorts (kilohm to megohm) between pins or between a pin and the header (V_{SS}). A complete summary of the location of the short in each part and the resultant parametric failure is presented in Table D19. The shorts were traced to trails of Pb dendrite growth in the glass seal bridging between adjacent package leads or between a package lead and the header. This is the same mechanism that occurred in the Manufacturer A 4001 and 4017 and the Manufacturer C 4013 packages.

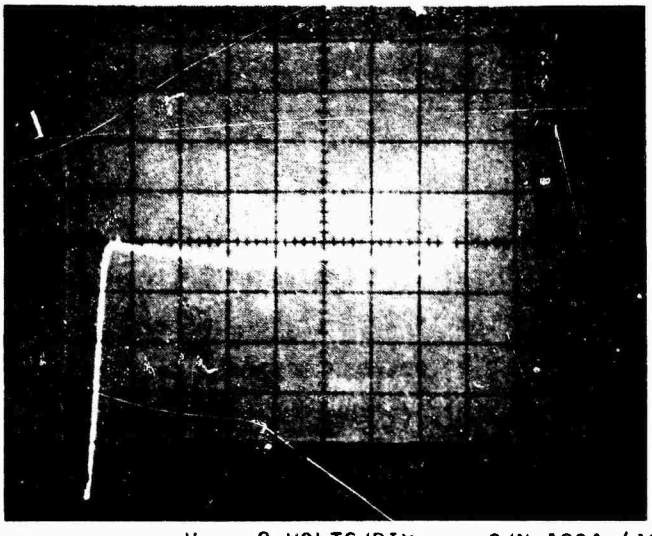
10.3 I_{IH1} OR I_{IL1} FAILURE - CHANNELED INPUT DIODE

During 125°C life, one Lot A part failed I_{IL1} (38 nA) and one Lot B part failed I_{IH1} (29 nA) traced to a degraded input diode. The Lot A part contained a degraded pin 5 input-to-V_{DD} diode (D3) and the Lot B part



$V_{DRAIN-SOURCE}$ S/N A234 (1000 HRS/250°C)

FIGURE D64 - I_{DSS} I-V CHARACTERISTIC OF N11.



V_R = 2 VOLTS/DIV S/N A294 (4000 HRS/125°C)

FIGURE D65 - REVERSE I-V CHARACTERISTIC OF THE PIN 5 INPUT-TO-V_{DD} DIODE (D3).

TABLE D19 - SUMMARY OF FAILURE DUE TO PIN-HEADER SHORTS

CELL	S/N	TIME OF FAILURE	FAILED PARAMETER(S)	LOCATION OF SHORT
A-250°C	A163	500 HRS	I_{IL1}	PIN 5 TO HEADER
A-225°C	A71	2000	I_{IL1}	PIN 15 TO HEADER
	A73	↓	↓	PIN 15
	A141	↓	↓	PIN 5
	A81	↓	↓	PIN 5
	A63	4000	↓	PIN 15
	A83	↓	↓	PIN 5
	A142	↓	↓	PIN 6
B-250°C	B211	250	I_{IL1}	PIN 15 TO HEADER
B-225°C	B103	4000	I_{IL1}	PIN 15 TO HEADER
B-250°C	B171	4000	I_{SS} & I_{IH1}	PIN 7 TO HEADER
	B151	↓	I_{SS}, I_{IH1}, & V_{OH2}	PINS 13 & 15 TO PIN 14
B-225°C	B63	1000	I_{SS} & I_{IH1}	PIN 7 TO HEADER
	B93	2000	I_{SS} & V_{OH2}	PINS 13 & 15 TO PIN 14
	B34	4000	I_{SS}, V_{OH2}, I_{IH1} & I_{IL1}	↓

contained a degraded pin 9 input-to-V_{SS} diode (D18). In each instance the leakage was channeled, as illustrated in Figure D65, and bake recoverable. During life testing, pin 5 was grounded which reverse biased D3, and pin 9 was connected to V_{DD} which reverse biased D18. Therefore, the degradation was attributed to charge separation in the fringing field of the reverse biased junction caused by ionic contamination in or on the passivation layers.

MANUFACTURER CODES

Manufacturer	Code
Motorola	A
Solid State Scientific	B
National	C
RCA	D

MISSION
of
Rome Air Development Center

RADC plans and executes research, development, test and selected acquisition programs in support of Command, Control Communications and Intelligence (C^3I) activities. Technical and engineering support within areas of technical competence is provided to ESD Program Offices (POs) and other ESD elements. The principal technical mission areas are communications, electromagnetic guidance and control, surveillance of ground and aerospace objects, intelligence data collection and handling, information system technology, ionospheric propagation, solid state sciences, microwave physics and electronic reliability, maintainability and compatibility.