AD NUMBER

ADB019981

LIMITATION CHANGES

TO:

Approved for public release; distribution is unlimited.

FROM:

Distribution authorized to U.S. Gov't. agencies only; Test and Evaluation; APR 1977. Other requests shall be referred to Air Force Weapons Laboratory, Attn: DYX, Kirtland AFB, NW 87117.

AUTHORITY

AFWL ltr, 7 Nov 1986

AD Bo 19981

AUTHORITY:
AFWL etc,
7 NOV 86

AFWL-TR-
76-286

GENERAL TEST PLAN, PULSED VOLTAGE FAILURE LEVELS OF CAPACITORS

General Electric Company
Space Division
PO Box 8555
Philadelphia, PA 19101

April 1977

Final Report

This research was sponsored by the Defense Nuclear Agency under Subtask R99QAXEB097, Work Unit 52, Nonsemiconductor Component Damage and Hardening Studies Related to EMP Phenomena.

Prepared for
Director
DEFENSE NUCLEAR AGENCY
Washington, DC 20305

AIR FORCE WEAPONS LABORATORY
Air Force Systems Command
Kirtland Air Force Base, NM 87117

AFWL-TR-76-286

This final report was prepared by the General Electric Company, Space Division, Philadelphia, Pennsylvania, under Contract F29601-75-C-0130, Job Order WDNE 1407 with the Air Force Weapons Laboratory, Kirtland Air Force Base, New Mexico. Dr Donald C. Wunsch (DYX) was the Laboratory Project Officer-in-Charge.

When US Government drawings, specifications, or other data are used for any purpose other than a definitely related Government procurement operation, the Government thereby incurs no responsibility nor any obligation whatsoever, and the fact that the Government may have formulated, furnished or in any way supplied the said drawings, specifications, or other data is not to be regarded by implication or otherwise as in any manner licensing the holder or any other person or corporation or conveying any rights or permission to manufacturer, use, or sell any patented invention that may in any way be related thereto.

This technical report has been reviewed and is approved for publication.

FOR THE COMMANDER

Donald C. Wunsch
DONALD C. WUNSCH
Project Officer

Paul J. Daily
PAUL J. DAILY
Colonel, USAF
Chief, Technology & Analysis Division

DO NOT RETURN THIS COPY. RETAIN OR DESTROY.

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE *(When Data Entered)*

REPORT DOCUMENTATION PAGE

READ INSTRUCTIONS BEFORE COMPLETING FORM

1. REPORT NUMBER: AFWL-TR-76-286	2. GOVT ACCESSION NO.
3. RECIPIENT'S CATALOG NUMBER	
4. TITLE *(and Subtitle)*: GENERAL TEST PLAN, PULSED VOLTAGE FAILURE LEVELS OF CAPACITORS	5. TYPE OF REPORT & PERIOD COVERED: Final Report
	6. PERFORMING ORG. REPORT NUMBER
7. AUTHOR(s): Dante M. Tasca	8. CONTRACT OR GRANT NUMBER(s): F29601-75-C-0130
9. PERFORMING ORGANIZATION NAME AND ADDRESS: General Electric Co., Space Division, PO Box 8555, Philadelphia, PA 19101	10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS: 62601F/~~NWNE 1407/Subtask~~ R99QAXEB097/52
11. CONTROLLING OFFICE NAME AND ADDRESS: Director, Defense Nuclear Agency, Washington, DC 20305	12. REPORT DATE: April 1977
	13. NUMBER OF PAGES: 68
14. MONITORING AGENCY NAME & ADDRESS *(if different from Controlling Office)*: Air Force Weapons Laboratory (DYX), Kirtland Air Force Base, NM 87117	15. SECURITY CLASS. *(of this report)*: UNCLASSIFIED
	15a. DECLASSIFICATION/DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT *(of this Report)*

Distribution limited to US Government agencies only because of test and evaluation of military systems/equipment (April 1977). Other requests for this document must be referred to AFWL/DYX/Kirtland AFB, NM 87117.

17. DISTRIBUTION STATEMENT *(of the abstract entered in Block 20, if different from Report)*

18. SUPPLEMENTARY NOTES

This research was sponsored by the Defense Nuclear Agency under Subtask R99QAXEB097, Work Unit 52, Nonsemiconductor Component Damage and Hardening Studies Related to EMP Phenomena.

19. KEY WORDS *(Continue on reverse side if necessary and identify by block number)*

Capacitor Damage; EMP (Electromagnetic Pulse); EMP Device Damage

20. ABSTRACT *(Continue on reverse side if necessary and identify by block number)*

The test plan of this program is to determine (1) pulsed voltage/power failure levels and (2) failure mechanisms for selected capacitors typical of those used in military electronic systems. The pulsed voltage/power levels of concern are those levels, with some safety margin, that could be induced in electronic components by electromagnetic pulse from nuclear weapons. Sufficient failure data are to be obtained so that device failure predictions are typical for each device; although statistical data collection is not required.

DD FORM 1 JAN 73 1473 EDITION OF 1 NOV 65 IS OBSOLETE

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE *(When Data Entered)*

405 025

4B

PREFACE

This General Test Plan was prepared by the General Electric Company, Space Division, Philadelphia, Pennsylvania, under Air Force Contract F29601-75-C-0130 from the Air Force Weapons Laboratory, Air Force Systems Command, United States Air Force, Kirtland Air Force Base, New Mexico, 87117. This project is sponsored by the Defense Nuclear Agency (DNA) under subtask R99QAXEB097, DNA MIPR 75-587. Technical Monitor at the AFWL is Dr. Donald C. Wunsch. The Program Manager and principal investigator at General Electric is Dante M. Tasca. The DNA Task Manager was Capt D. Wilson.

CONTENTS

SECTION I

BACKGROUND

This document defines the general test plan for Air Force Contract No. F29601-75-C-0130. The purpose of this program is to develop a data base for predicting capacitor failure levels and failure mechanisms when electronic systems are subjected to indirect EMP. Typical Air Force systems utilizing those components to be tested are the B-1, Advanced Airborne Command Post, EC135, and F-111. The data produced will be applicable to any electronic system that would be required to function in a nuclear environment.

SECTION II

OBJECTIVES

The objective of this program is to determine (1) pulsed voltage/power failure levels and (2) failure mechanisms for selected capacitors typical of those utilized in military electronic systems. The pulsed voltage/power levels of concern are those levels, with some safety margin, that could be induced in electronic components by an electromagnetic pulse from a nuclear weapon. Sufficient failure data are to be obtained so that device failure predictions are typical for each device; although statistical data collection is not required.

Specifically, the experimental program should provide a broad data base to define the damage mechanisms and permanent damage changes in capacitance, loss, and leakage current characteristics versus pulse power level as a function of at least the following variables:

(a) square wave pulse width over the range of 500 nanoseconds to 20 microseconds.

(b) nominal capacitance value

(c) capacitor voltage rating

(d) capacitor construction (such as paper, glass, mylar, mica, tantulum foil, etc.)

(e) capacitor manufacturer

The ultimate objective would be to determine if an experimental correlation can be developed on a per microfarad (nominal capacitance value) per volt (working voltage rating) basis defining the amount of damage versus pulse power level for each capacitor construction and manufacturer type. In this way the experimental results could be used to define the vulnerability levels of other capacitor types not characterized during the program. It should be noted that in carrying out the experimental evaluation, the damage criterion will not be restricted to only a single level of device damage but rather will define the range and extent of induced change in capacitor characteristics at various pulse power levels.

SECTION III

EXPERIMENTAL PROGRAM

1. GENERAL DESCRIPTION

All damage experiments will be performed using unipolarity, single square wave power pulses of 500 nanoseconds, 3 microseconds, and 20 microseconds pulse duration. Unlike the popular method of step stressing to the point of damage threshold (as determined from a minimum discernable change in device operating parameters) employed in the pulse testing of semiconductor devices, the capacitor pulse damage experiments are designed to evaluate the resultant change in device electrical characteristics when exposed to various pulse power levels. The range of interest for this induced change in the present study will be from at least 1% to 100% change in initial parameter values. The experiments themselves are configured to be relatively straightforward in that they will be performed under ambient temperature and pressure conditions and under free air conditions.

The primary failure response in the majority of capacitor units is anticipated to be associated with voltage breakdown effects. Here, for example, if a square wave current pulse is used as the stimulus, the voltage developed across the capacitor will increase linearly with time until dielectric punch through

or electrode arc over occurs. The voltage level for this to be initiated would be somewhat independent of pulse duration. At this point, though, the device current would be channeled through the breakdown point and the extent of permanent damage in capacitance, loss and leakage current would be dependent on the post breakdown current amplitude and duration. However, the breakdown voltage withstanding capability of the capacitor after the initial excursion into breakdown is generally reduced from its original value when exposed to subsequent power pulses.

A possible exception to this is the dynamic response exhibited by tantalum capacitors. The rectifier action of polar units and the back to back rectifier action of nonpolar units is expected to yield a pulse response similar to that observed when pulsing semiconductor diodes. However, capacitor damage would still be expected to be dependent on pulse current amplitude and duration. Polarized units are generally expected to be more susceptible in the "reverse" polarity direction of pulsing as compared to the "forward" polarity. The extent of this difference, though, is no doubt dependent on capacitor type and manufacturer and will be evaluated in the experimental program. Open foil burnout would be more prevalent in metallized dielectric units where electrode thicknesses of a few thousand angstroms are employed. The damage current for this effect, however, would also be dependent on current amplitude and duration.

In view of this, the pulse power damage experiments are configured to evaluate the extent of capacitor damage due to square wave pulse current amplitude and duration. In order to provide a large enough data base within a reasonable test sample size, the damage experiments will consist of two different types. The first will be a multiple exposure type, while the latter will be a single exposure type. The multiple exposure experiments are designed to yield a maximum amount of damage data, with the minimum consumption of prime components. The single-pulse experiments are designed to yield device damage data which are not biased by prior conditions of permanent damage within the device.

The rationale for selecting the exact mix of single pulse and cumulative pulse experiments, as well as the specific levels of the power pulses applied to the various capacitor units to adequately cover the damage range of interest, is discussed in the following sections.

2. TEST RATIONALE

As previously indicated, the majority of capacitor classes are expected to fail by a voltage breakdown in either the dielectric (dielectric punch through) or electrode edge (surface arcover). This is characterized by a rapid decrease in capacitor voltage, and an increase in capacitor current which is dependent on the source impedance of the pulser. This break-

down will occur when the voltage stress across the capacitor reaches a particular value which is dependent on capacitor class and construction peculiarities such as dielectric thickness, electrode edge separation, etc. Furthermore, for a given capacitor type, the critical value of capacitor voltage for breakdown to be initiated may be dependent on the rate of increase of capacitor voltage with time, such that somewhat higher voltage levels might be required in shorter time periods. In any event, though, even if breakdown is initiated, the amount of damage induced in the capacitor is dependent on the current level that flows after breakdown as well as it's time duration. In other words, a breakdown does not necessarily insure that damage will be produced and if damage does occur, it is by no means always manifested as a complete short but rather as some degree of degradation in capacitor characteristics. One consequence of a voltage breakdown, however, is that the breakdown voltage level of the capacitor when exposed to a similar subsequent pulse is generally reduced from the value required for the initial breakdown.

Some capacitor classes may fail due to a foil burnout mechanism. This would be more prevalent in capacitor classes using metallized dielectrics where electrode thicknesses of a few thousand angstroms are employed. This type of failure is anticipated to be characterized by an increase in capacitor

voltage, and a decrease in capacitor current which is also dependent on pulser source impedance. If complete foil burnout occurs, the capacitor voltage would increase to the pulser source voltage and the current would decrease to zero. The first level of capacitor damage is anticipated to be associated with a partial foil burnout rather than a complete one. As such, the damage response would be characterized by a moderate increase in capacitor voltage and a moderate decrease in capacitor current. In any event, the amount of foil burned out will depend on the current level flowing in the electrode and it's time duration. A partial foil burnout is by no means always manifested as a complete open but rather as some degree of degradation in capacitor characteristics.

The polar and nonpolar tantalum units are expected to fail by a burnout of the dielectric oxide when pulsed into conduction through the rectifying action of the electrolyte which is shown schematically in Figure 1.
In the reverse rectifier direction a "second breakdown" response is expected to occur, while in the forward rectifier direction a normal I^2R burnout similar to forward semiconductor diode pulsing would be expected. In any event, though, the amount of damage induced in the capacitor is expected to be dependent on the current level that flows as well as it's time duration. Furthermore, if damage does occur, it is by no means always manifested as a complete short but rather as some degree of degradation in capacitor characteristics.

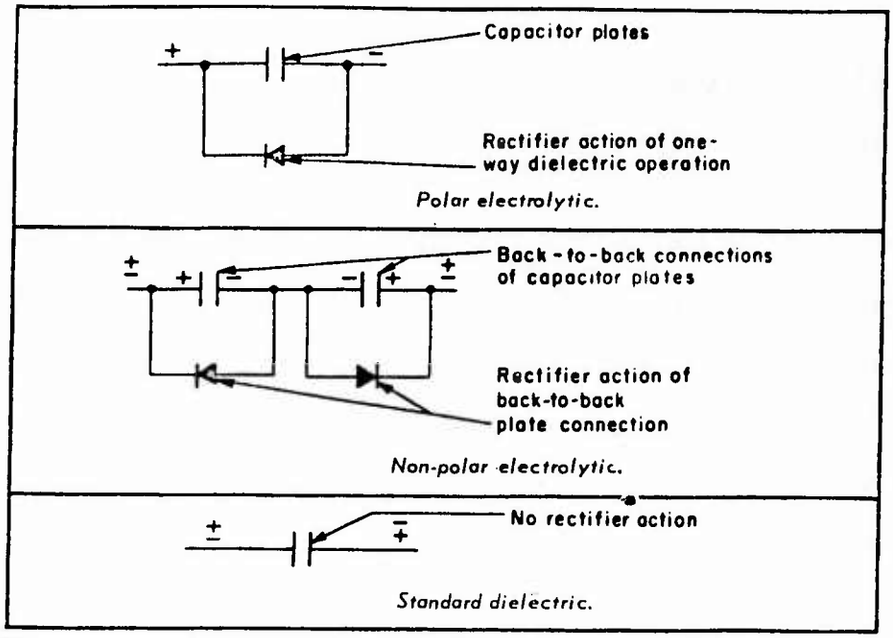


Figure 1. Circuit Configuration of Tantalum and Standard Dielectric Type Capacitors.

In performing square wave pulse testing on capacitors, one has a choice of either keeping the voltage stress or the current stress a square wave. Since a square voltage stress across the capacitor would require an extremely large impulse of current to be driven into the capacitor from an extremely small source impedance pulser and then discharged at the same rate at the pulse end, the use of a square wave current stress is actually the better choice for reasons other than just the ease and practicality of generating such a stress. For instance, under a square wave current stress the voltage developed across the capacitor would increase linearly with

time until a voltage breakdown occurred, a foil burnout occurred, or an oxide burnout occurred.

If a voltage breakdown occurs, the capacitor voltage level to initiate breakdown and its associated voltage rate of rise can be clearly observed from the pulse trace by observing the point at which the capacitor voltage decreases sharply. Similarly, the square wave current pulse provides a controlled post breakdown stress which can be completely observed during the total pulse without the frequent nuisance of post breakdown data loss due to traces going off scale. At a given pulse width, by charging the capacitors at various levels of constant current, breakdown can be initiated from the very end of the pulse to the very beginning of the pulse, thus a convenient method of generating various constant amplitudes of post breakdown current at approximately the same pulse width can be obtained. By performing these experiments at the three pulse widths planned, a body of data defining capacitor damage extent as a function of post breakdown current amplitude and duration can be generated. Furthermore, the use of a square current pulse which, by its nature, produces a linear increase in capacitor voltage will generate the proper data to characterize the dependence of capacitor breakdown voltage level on the rate of rise of capacitor voltage. Similarly, by performing the experiments at the planned pulse widths, the proper data body to completely characterize the time dependence of capacitor

breakdown voltage level can be generated.

The same rationale for using a square wave current stress would also apply if a foil burnout occurs. Here, if a foil burnout occurs, the capacitor current level to cause this and its associated pulse duration can also be clearly observed from the pulse trace by observing the point at which the capacitor voltage increases over and above its prior established linear time increase due to the current stress. The key stress parameter for a foil burnout is the pulse current, since the voltage one observes when a capacitor is pulsed is the dielectric stress and not the IR drop in the foil. Previous experimental data in pulse testing thin metal foils and thin semiconductor metallization strips have shown that the damage current to cause various degrees of metal burnout follows a well behaved time dependent function. As such, the constant current pulse provides a controlled stress which can be completely observed during the total pulse. At a given pulse width, by charging the capacitors at various levels of constant current, various degrees of foil burnout can be produced. By performing the experiments at the planned pulse widths, a body of data defining capacitor damage extent as a function of current amplitude and duration can be generated.

The rationale for using the square wave current pulse in

testing the polar and nonpolar tantalum units would be similar to that employed in testing semiconductor diodes. Here, the constant current pulse provides a controlled stress which can be completely observed during the total pulse and is a generally accepted method used to determine not only the damage characteristics but the V-I response of the devices.

3. TEST CONDITIONS

The scope of the experimental effort is, of course, closely tied to the overall objective of the program. This requires an extensive experimental effort in order to develop the proper data base by which the desired damage characteristics, over a wide range of induced damage level can be evaluated. Clearly, there are many approaches that would have potential interest in carrying out such a comprehensive program. However, in order to limit the magnitude of the test effort to a tractable level, only the most efficient approaches to satisfying the program objectives should be adopted. The following test procedure is considered to be an optimum test methodology which will yield a maximum amount of damage data over the damage range of interest within the overall scope of the program.

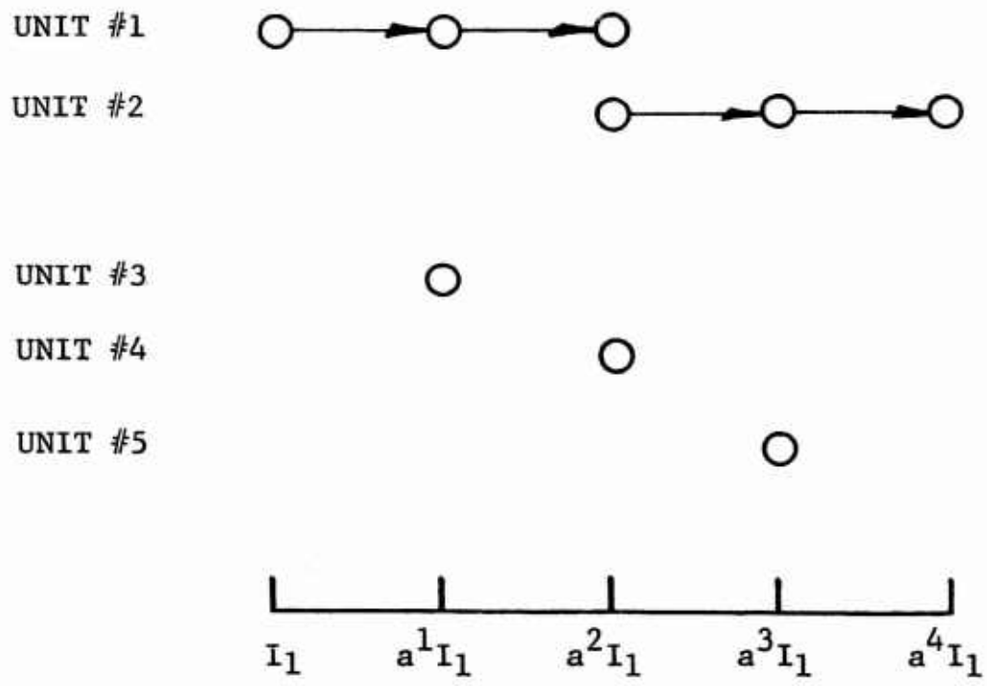
Damage testing at any given pulse width for each unique device type (i.e., construction, manufacturer, working voltage rating, initial capacitance value and polarity direction)

will be performed in a group of at least five units with an overall average of at least 1.8 power pulses per unit being expended within each group. The allocation of power pulses within the group will be as follows. Two units within the group will be subjected to step stress pulsing (monotonically increasing) with three pulses applied to each unit, resulting in a subtotal of two units and six power pulses. The remaining three units within the group will be each subjected to single power pulses, resulting in a subtotal of three units and three power pulses. The overall total will then be five units and nine power pulses per group.

In this case, the pulse current levels which result in less than 1% damage (I_{min}) and greater than 100% damage I (I_{max}) will be used to define the nominal pulse current range over which the prime units will be evaluated. However, as a precautionary measure in anticipation of possible unit to unit variations, the pulse testing on the prime units within the group of five will actually be performed over a pulse current range of $I_{min}/3$ to $3I_{max}$. Here, the pulse current range from $I_{min}/3$ to $3I_{max}$ will be divided into four increments such that the ratio of current level at one increment to its preceding level is constant.

An illustration of the planned allocation scheme for specific pulse current levels applied to each unit within the five unit group to maximize the amount of single and multiple pulse damage data is shown in Figure 2. As seen, the pulses are strategically placed such that, with the exception of the extremes, each pulse current level contains both a single and cumulative pulse damage point. As such, damage data for both single and cumulative pulse vulnerability at various levels of device damage over the complete range of interest can be obtained by this approach with an economic expenditure of prime units. Here, for example, the effects of cumulative pulsing, if any, can be observed by examining the damage characteristics exhibited by each unit as it is progressively pulsed at small increasing pulse current levels. This is further complemented by comparing the first pulse damage characteristics of the other units to the various cumulative pulse levels over the damage range of interest. The pulse damage data so obtained for each group of five units will, of course, be examined to insure that the complete device damage characteristics are adequately identified during this procedure. Additional pulse testing at other selected pulse current levels will subsequently be performed in those cases where additional damage data are deemed desirable.

The problem of properly selecting the lowest pulse current level (I_{min}) and the maximum pulse current level (I_{max})



$$I_1 = \frac{\text{I MIN}}{3} \quad \text{, AT I MIN DAMAGE IS} < 1\%$$

$$a^4 I_1 = 3 \text{ I MAX, AT I MAX DAMAGE IS} > 100\%$$

$$a = \left(\frac{9 \text{ I MAX}}{\text{I MIN}}\right)^{1/4}$$

Figure 2. Pulse Current Allocation Procedure Planned for the Capacitor Damage Experiments

to be used in the above approach can be solved quite easily for capacitor types in which many samples are available (which is the case with the majority of the capacitor types to be tested). Here, at each given pulse width, each unique device type (i.e., capacitance value, working voltage rating, polarity direction, construction and manufacturer) will have a single unit initially characterized using step stress testing. Here, the unit will be exposed and monitored under single pulses of increasing pulse current level with its electrical characteristics measured prior to the initial pulse and following each subsequent pulse. The increase in level from the previous pulse will be at least a factor of ten. The values of I_{min} and I_{max} will be defined from an examination of the current level-damage level data obtained with this unit. In the event that the factor of ten increases in the initial characterization is deemed too coarse, a finer level of a factor of 3 will be employed.

In those cases where only a limited number of test samples are available and pulse current damage data has already been obtained at a longer pulse width, then the range of pulse conditions to be used will be defined by assuming a $t^{1/2}$ (t being pulse duration) relationship in current amplitude-pulse duration equivalency for similar damage effects and extrapolate the longer pulse width data to the shorter pulse width requirements. The initial testing on the first unit will, or course, verify or

disprove this estimate and adjustments will be made accordingly. The minimum required pulse level to achieve a breakdown will be defined from the longer pulse width breakdown level observations and from the peak charging voltage capability of the pulser when driving the particular capacitance value device of concern.

In those limited cases where a limited number of test samples are available and no previous pulse damage data have been obtained, then a judgement estimate will be made on the amount of voltage overstress which would produce a breakdown and the starting current chosen from a similar examination of the pulser drive characteristics. Maximum pulse current level will be initially estimated at a factor of one hundred in excess of that required for breakdown threshold. The subsequent test conditions will then be adjusted accordingly based on the initial observations.

4. CAPACITOR MEASUREMENTS

The usual characteristics that are specified for a capacitor include Capacitance, Dissipation Factor or Equivalent Series Resistance, Insulation Resistance or Leakage Current and Dielectric Strength. The electrical and environmental parameters that are of most interest with respect to these four basic measurements are temperature, voltage, and test frequency. The reference temperature for most capacitor

measurements is 25°C. Voltage is dependent on the rating applied by the manufacturer and test frequency typically depends on the class of product. For example, electrolytic capacitors are ususlly measured at either 60 or 120 hertz, whereas ceramic and mica capacitors are usually measured at 1 kilohertz or 1 megahertz depending on value. Paper and film capacitors are usually measured at 1 kilohertz up to 1 mfd and 60 hertz above capacitance value.

As such, capacitor degradation resulting from the direct injection of the pulse power environment will be determined from capacitance, dissipation factor, and D.C. leakage current measurements obtained at room temperature. In order to provide a common reference measurement for the comparison of the pulse power damage characteristics of the various capacitor types, voltage ratings and capacitance values, a 1 kilohertz test frequency will be used. To avoid reverse biasing of the polarized units, all capacitor measurements will be obtained using a 0.2 volt oscillator level with the capacitors biased at 25% and 100% of their respective D.C. voltage rating up to a maximum of 600 volts. DC current will be limited to at least a maximum of 30 milli-amperes. Dielectric strength data will be obtained from the pulse response plots described in Section 3.7.

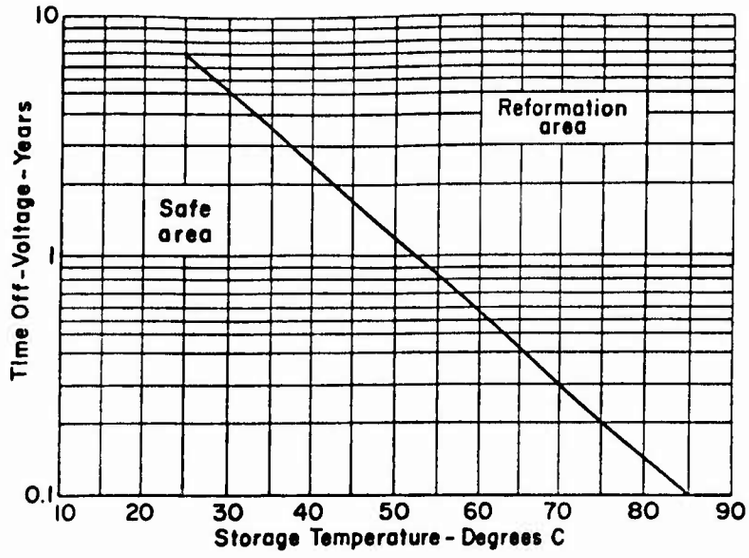


Figure 3. Storage Life Characteristics of the General Electric Type 76F Aluminum Electrolytic Capacitors

It should be noted that aluminum electrolytic capacitors are particularly susceptible to degradation due to a chemical deformation of the dielectric film resulting from exceeding the particular safe time-temperature limits of each specific type (see for example the safe storage characteristics of General Electric type 76F aluminum capacitors shown in Figure 3). As such, to preclude obtaining erroneous data on aluminum electrolytic capacitors, all units will be reformed at AFWL before testing to at least the reforming procedures defined in MIL-STD-1131.

The electrical parameter measurements will be obtained for each unit before and after each exposure to the pulse energy source. Immediately before taking every measurement on a test unit, a control unit of the identical type and capacitance value as that being pulse tested will be measured and recorded to insure that small changes in the test device capacitance, loss, and leakage are due to pulse power effects rather than instrumentation effects. Prior to any pulse testing, all device control units will be measured in the General Electric Parts Standards Laboratory to within 0.1% accuracy. The control units will also be remeasured in the Parts Standards Laboratory at the conclusion of the pulse testing phase. These measurements will represent a standard reference value for each control unit, and will be obtained using either the high speed, automatic testing equipment or single test unit equipment defined below:

General Radio Model 2990-9138 Automatic Capacitance Measurement Station

General Radio Model 2990-9139 Automatic Leakage Measurement Station

Boonton Model 75D Capacitance Bridge

Boonton Model 33A Capacitance Bridge

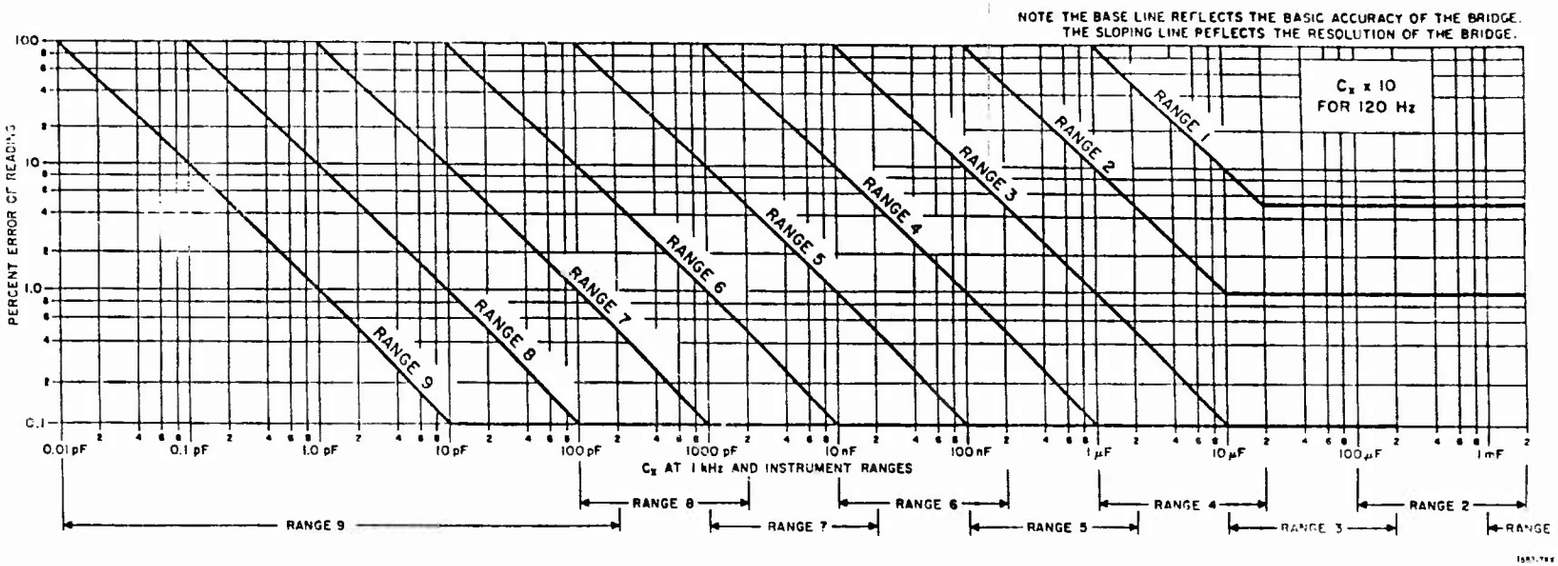
Hewlet Packard Model 425 DC Microvoltmeter-Ammeter

Keithley Model 240 Voltage Supply

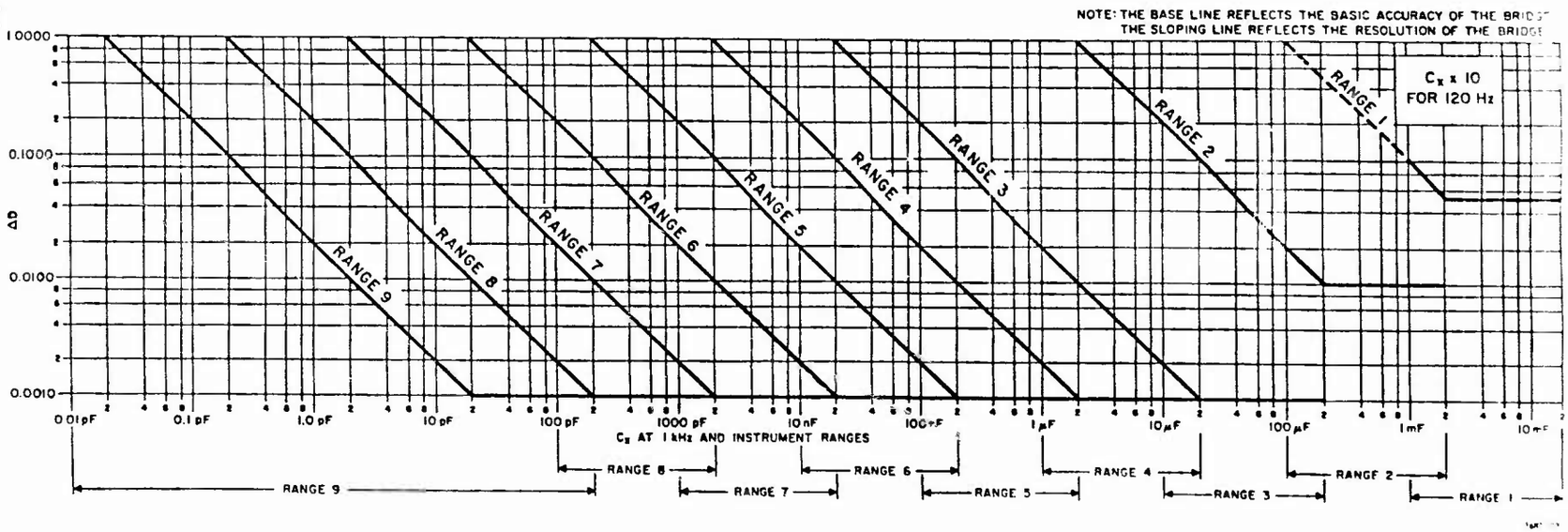
During the pulse power experiments, all devices including control units will be measured using a General Radio Model 1683 Automatic RLC Bridge for capacitance and loss measurements and Cimron Model DMM 50 Digital Multimeters and 1% precision resistors for leakage measurements. The Model 1683 Bridge is capable of obtaining capacitance readings from 0.01 picofarads to 20 millifarads at a 1 kilohertz test frequency and dissipation factor readings from 0.0001 to 2. External bias capability for capacitance-bias measurements is 600 volts maximum. The model DMM 50 multimeter can measure from 1 microvolt to 1200 volts and 1 picoamp leakage current sensitivity using a 1 megohm precision resistor.

The measurement data obtained from the Model 1683 and the Model DMM 50 instruments will be automatically recorded and stored, along with the device serial number and pulse shot number information, on magnetic tape via the computer interface described in Section 3.7. These data will then be available for automatic data reduction and analysis as required in the latter phases of the program.

The absolute accuracy obtainable with the General Radio Model 1683 RLC Bridge is shown in Figure 4. Similar information with respect to the Cimron Model DMM 50 Digital Multimeter is given in Table 1. In both cases the actual accuracy associated with a particular measurement is dependent upon the capacitance



Capacitance accuracy chart.



Dissipation-factor accuracy chart.

Figure 4. Measurement Accuracy of the General Radio Model 1683 RLC Bridge.

Table 1. Measurement Accuracy of the Cimron Model DMM 50 Digital Multimeter

RANGES	100 mv, 1V, 10V, 100V, 1000V
RESOLUTION	0.001% of range (1μV on 100 mv range)
ACCURACY	
24 HOURS	Reference Conditions: 23°C±1°C
10,100,1000V Ranges	+0.002%RDG+0.0008%FS
1V Range	±0.003%RDG±0.0008%FS
100 mv Range	±0.004%RDG±0.0016%FS
1 YEAR	Reference Conditions: 20°C to 30°C
10,100,1000V Ranges	±0.004%RDG±0.0008%FS
1V Range	±0.005%RDG±0.0008%FS
100 mv Range	±0.008%RDG±0.0016%FS
TEMPERATURE STABILITY	
10V Range	+(0.0005%RDG+0.0001%FS)/°C
1,10,100,1000V Ranges	±(0.0007%RDG±0.0002%FS)/°C
100 mv Ranges	±(0.001%RDG±0.0005%FS)/°C
INPUT RESISTANCE	
100mv + 1V Range	1000 MΩ
10V Range	10,000 MΩ
100, 1000V Ranges	10 MΩ
COMMON MODE REJECTION	1 kΩ Imbalance
DC	140 dB
AC (60 Hz and above)	120 dB
NORMAL MODE REJECTION	60 Hz or 50 Hz with 50Hz line option
FILTER OUT	60 dB
FILTER IN	100 dB

or bias voltage value of the device and the instrument scale selected. The primary objective of the experimental work, however, is to determine the pulse power induced change in capacitor characteristics for the various types to be tested. As such, instrument measurement repeatability is more of concern. Through the use of simultaneous control unit measurements during every experimental measurement, the recorded damage changes can be obtained to a much better accuracy than that on an equivalent absolute value basis.

The final aspect of the capacitor measurements is associated with evaluating and defining the effects of "time after power pulse" on device capacitance, loss, and leakage value and thermal recovery, in order to establish some standard time after pulsing to obtain device characteristics. These effects have not been presently defined and may very well be dependent on device construction. The extent, if any, of thermal recovery effects will be evaluated during the initial phase of the experimentation.

5. HIGH ENERGY PULSE SOURCE

As previously indicated, all damage experiments are planned to be performed using square wave power pulses. The high energy source which will be utilized in the present study is a General Electric 4.5 megawatt square wave cable pulser with the following specifications: 1 nanosecond risetime,

300 amperes maximum into 50 ohms. The pulser is essentially an energy source with a 50 ohm internal impedance which is capable of developing a single square wave pulse across a 50 ohm load with an amplitude equal to one half the cable charging voltage. The pulser will be operated in a "constant current" mode at pulse widths of 500 nanoseconds, 3 microseconds, and 20 microseconds for the damage experiments.

In the event that the very large capacitance value units cannot be damaged at the maximum output capability of the square wave pulser, due to pulser current limitations, and damage data are still desired, then a supplemental pulse waveshape using an additional in-place, high energy pulser can be used with the concurrence of the AFWL Project Officer. This pulser, which produces a critically damped waveshape, can produce a much higher current output than that achievable with the square wave pulser, thus producing a higher voltage stress across the higher capacitance value units. The critically damped current pulse wave shape is described in time, I(t), by the following function:

$$I(t) = I_m \, (t/t_p) \exp \, (1 - t/t_p)$$

where I_m = peak output level

t_p = time to peak output level

The electrical specifications for this particular pulser are as follows:

(a) General Electric critically-damped wave-shape pulser (adaptable to damped sinusoidal wave shapes): 30 microsecond rise time to peak output, 150 microsecond pulse width, 7000 amperes maximum into 1 ohm; 3 microsecond rise time to peak output, 15 microsecond pulse width, 7000 amperes maximum into 1 ohm; 300 nanosecond rise time to peak output, 1.5 microsecond pulse width, 3500 amperes maximum into 2 ohms; 30 nanosecond rise time to peak output, 150 nanosecond pulse width, 1200 amperes maximum into 6 ohms.

Part of the rationale in selecting test unit capacitance and voltage rating values for test will be based on the maximum charging voltage capability of the particular pulse source to be used. The interrelationship of the square wave pulser to the maximum charging voltage applied to the various test capacitors and the degree of "squareness" for the pulse current stress is discussed in the following section.

6. PULSE TEST CONFIGURATION AND INSTRUMENTATION

The pulse test experiments on the capacitor units will be performed in a relatively straightforward experimental configuration in that the devices will be evaluated under ambient temperature and pressure conditions without any external bias applied; placed in a test fixture under free air conditions without heatsinking; and exposed to a high energy power pulse while monitoring the current delivered to the device and the voltage developed across the device. The text fixtures used to mount and instrument the capacitor for power pulsing will minimize, to the most practical extent, device lead and fixture inductance and capacitance to insure meaningful experimental data.

As previously indicated, the pulse damage experiments are configured to evaluate the extent of capacitor damage due to square wave pulse current amplitude and duration. To generate a square wave current it is planned to operate the pulser in the constant current mode which provides a maximum of 300 amperes square wave output. This is done quite simply by driving the capacitors through a 50 ohm series or shunt resistance and other suitable matching networks, as shown in Figure 5, with the larger capacitance value providing the flatter current-time capability. The degree of flatness of the current pulse delivered to the capacitors is determined

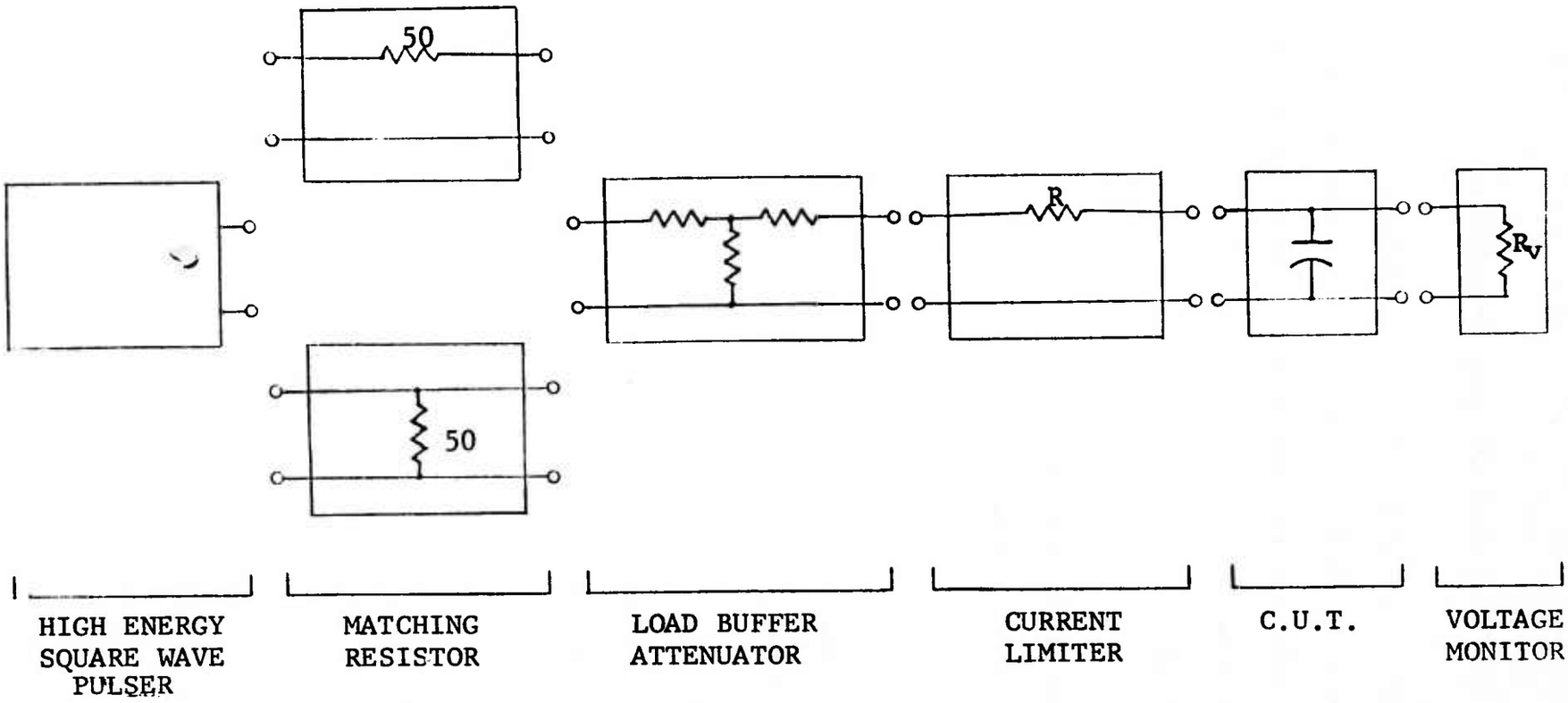
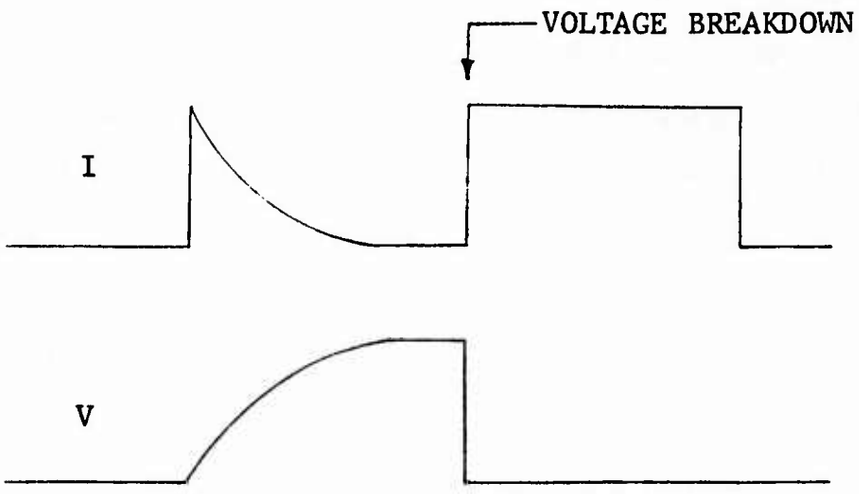


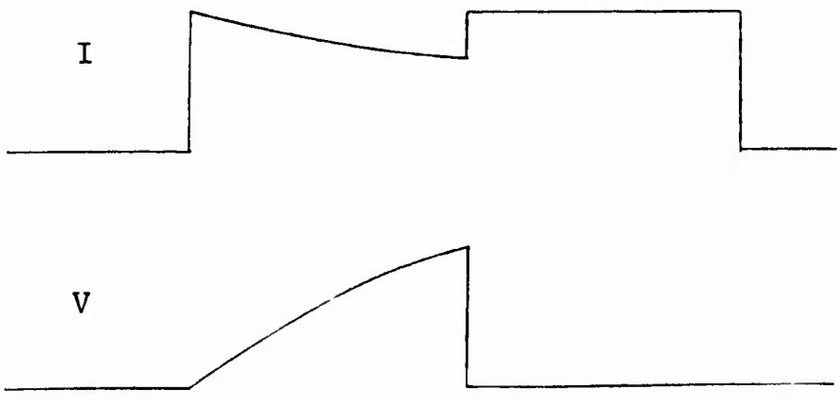
Figure 5. Square Wave Current Generator for Capacitor Pulse Damage Tests

by the total pulse width of the square wave energy source and the RC time constant of the current limiting resistor (R), voltage monitor resistor (RV), and the capacitor under test (C.U.T.). A typical wave shape which could be observed for extremely small and extremely large valued capacitance units would be as shown in Figure 6. Hence, to generate a reasonable square wave current pulse requires larger values for R and RV as the pulse width increases or the capacitance value decreases. There is, however, a practical limit to which this can be accomplished due to the inherent shunt resistance of the resistors. For Carbon composition units this value is approximately 0.5 to 2 picofarads, depending on wattage rating. The inherent shunt capacitance has the effect of lowering the effective impedance of the resistor (and hence its current limiting capability) for a few RC time constants of the resistor. As such, a 1 megohm - 1 picofarad resistor would not really present a circuit impedance of 1 megohm until 2 or 3 microseconds have passed. One can decrease this effect by building a series chain of "N" resistors which, in effect, would decrease the shunt capacitance by 1/N. There is, obviously, a practical limit to which this can be done and still maintain good pulse fidelity. These limitations have not now been established and will be identified as the testing progresses.

An indication of the maximum charging capability of the



A) LOW CAPACITANCE UNITS



B) HIGH CAPACITANCE UNITS

Figure 6. Pulse Response of Low and High Capacitance Value Units

energy source with respect to the peak voltage that the capacitors can be charged to is given in Figure 7. The charging voltage curves are shown for various matching networks and current limiter/voltage monitor combinations and are displayed parametically in terms of the capacitance-pulse width ratio of the experiment. It should be noted that these curves are idealized ones which have not factored in the aforementioned shunt capacitance characteristics of the various resistor elements. Figure 8 shows the degree of squareness of the pulse current stress which is achievable with the various resistor network-capacitor combinations. These characteristics are given in terms of the ratio of the capacitor current at the pulse end to that at the pulse start. A ratio of "1" would indicate a perfect square wave while a ratio of "0" would indicate complete capacitor charging.

The pulse voltage instrumentation planned is to utilize high frequency carbon composition resistors for device voltage monitors. For test devices with a relatively low pulse impedance (at pulse end), the voltage monitor resistance will be chosen to be at least 100 times greater than the maximum exhibited by the device under test. Electrical connection to the device under test is made as close as physically possible to the device package and the voltage monitor ground is kept

1: 50 SERIES, Rv = 10K
2: 50 SERIES,2X ATTENUATOR, Rv = 10K
3: 50 SHUNT, R = 1K, Rv = 10K
4: 50 SHUNT,2X ATTENUATOR, R = 1K, Rv = 10K
5: 50 SHUNT, R = 10K, Rv = 100K
6: 50 SHUNT, R = 100K, Rv = 1M
7: 50 SHUNT, R = 1M, Rv = 10M

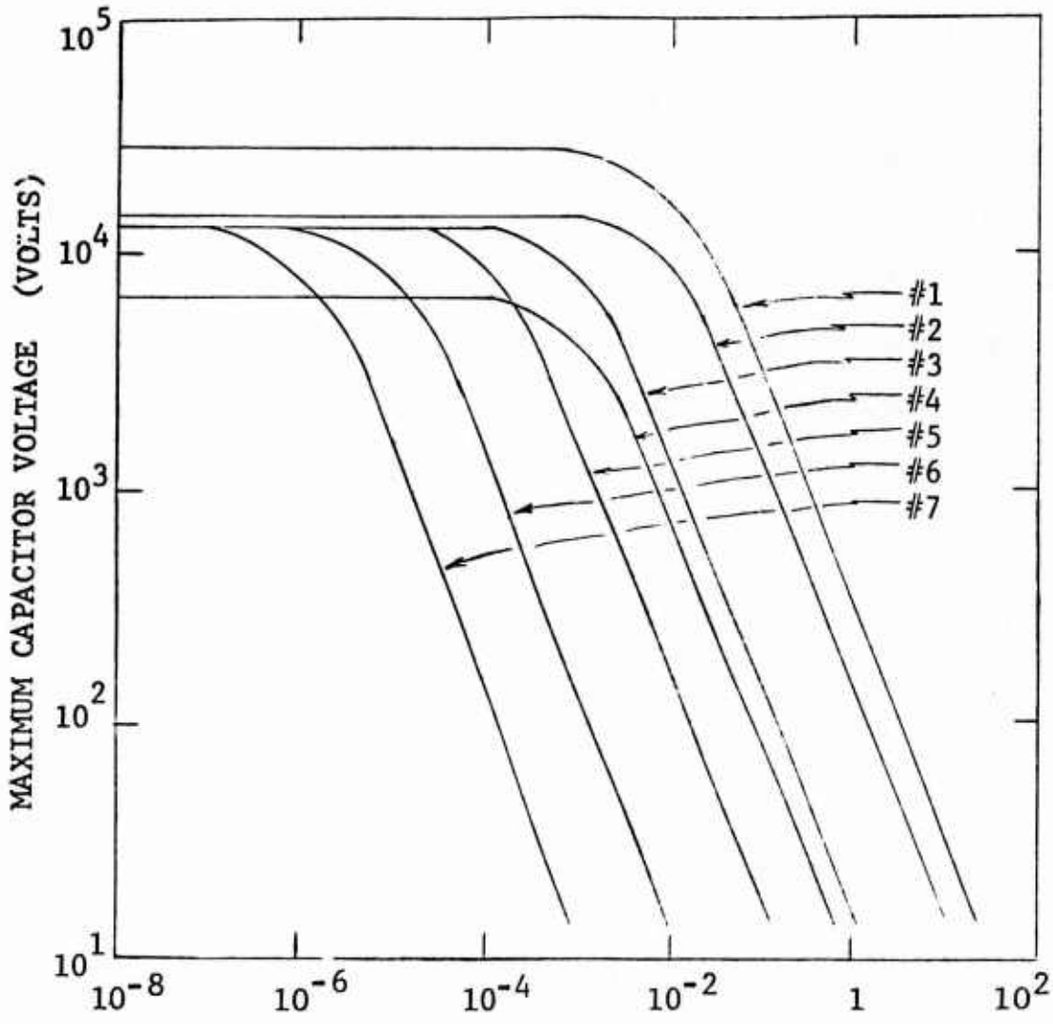


Figure 7. Maximum Capacitor Charge Voltage Capability of the Square Wave Energy Source

1: 50 SERIES, Rv = 10K
2: 50 SERIES,2X ATTENUATOR, Rv = 10K
3: 50 SHUNT, R = 1K, Rv = 10K
4: 50 SHUNT,2X ATTENUATOR, R = 1K, Rv = 10K
5: 50 SHUNT, R = 10K, Rv = 100K
6: 50 SHUNT, R = 100K, Rv = 1M
7: 50 SHUNT, R = 1M, Rv = 10M

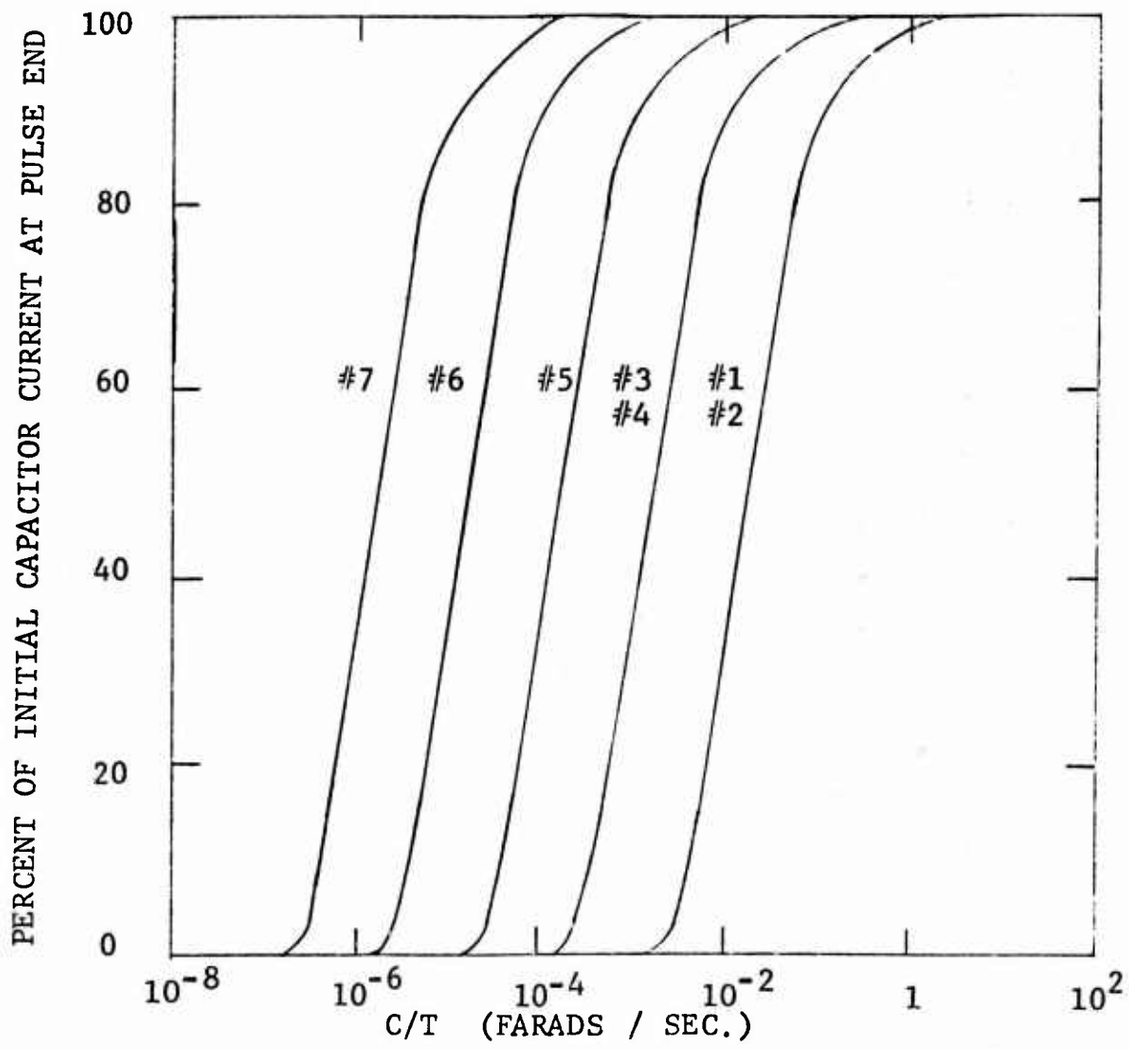
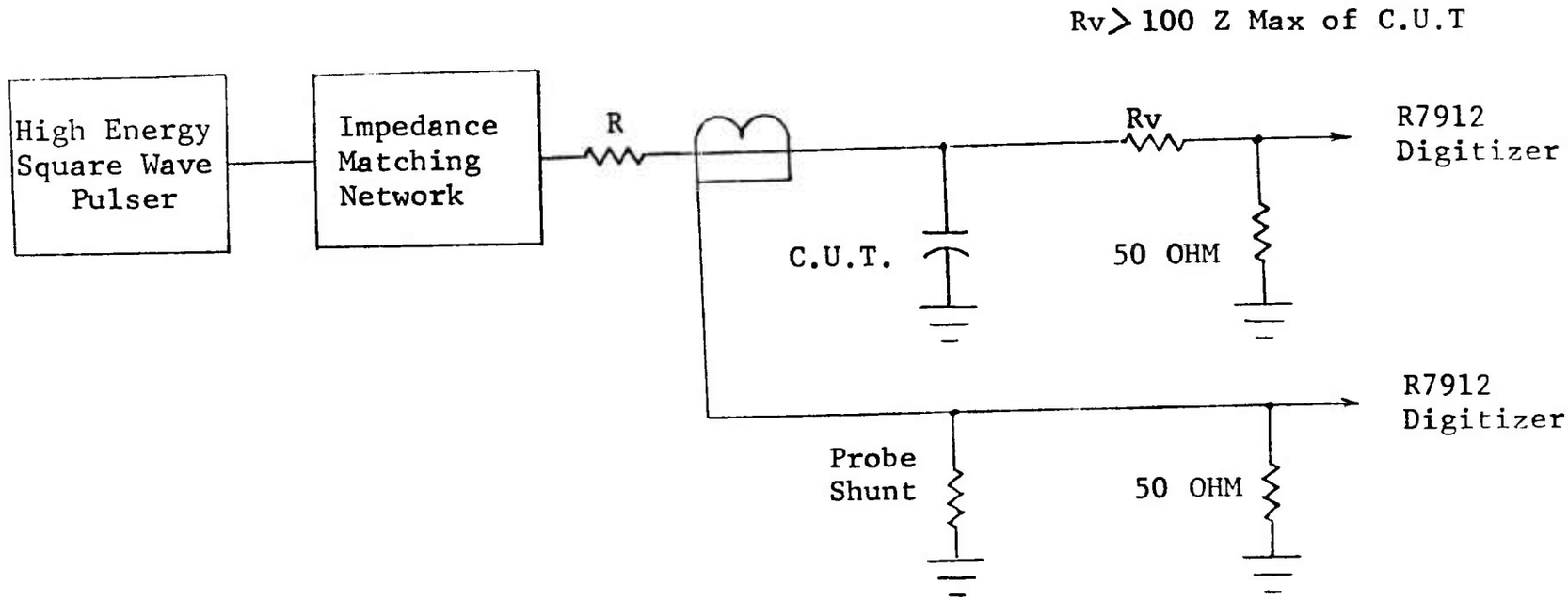


Figure 8. Square Wave Capacitor Current Capability of the Square Wave Energy Source

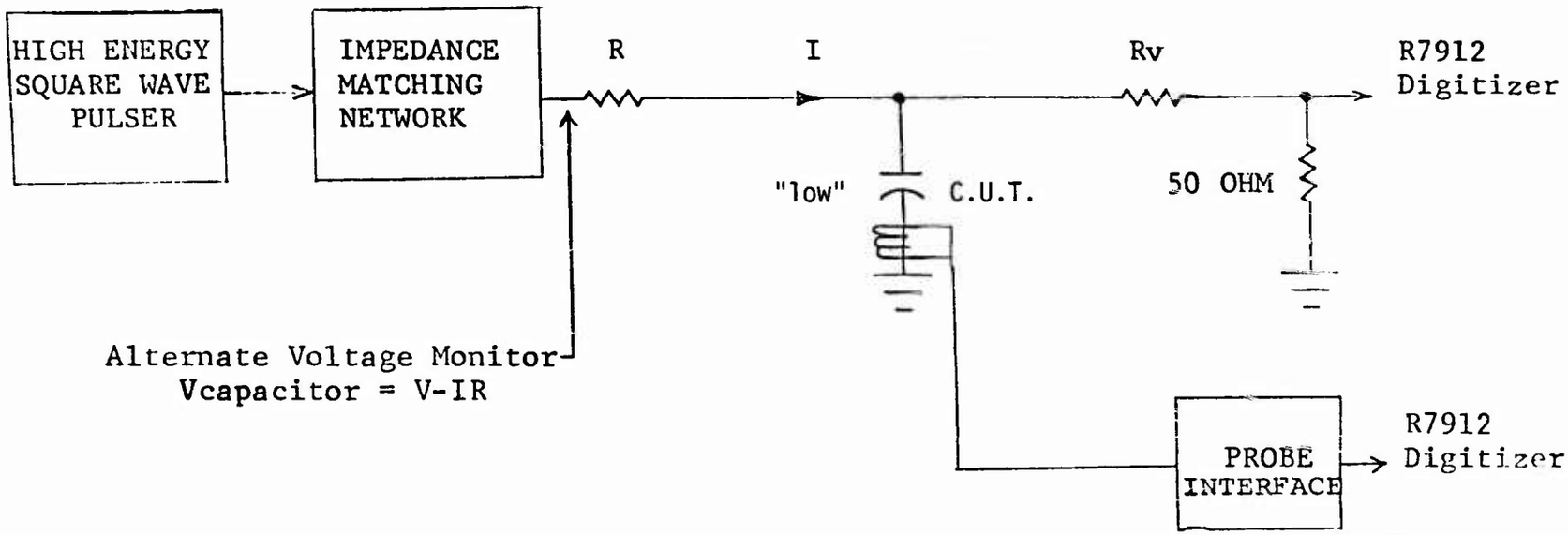
as close as physically possible to the test device ground. The pulse current instrumentation will consist of current probes which are capable of directly measuring the maximum peak currents anticipated without resorting to current dividers. The risetime capability of the probes is generally kept to less than 1% of the total pulse width being measured. For maximum noise immunity, a current probe with the maximum transfer impedance for the maximum pulse width and amplitude conditions expected is used. For the low pulse impedance devices (large capacitance units) the current probe and voltage monitor configuration will be as shown in Figure 9. Here, since the voltage monitor resistance is 100 times greater than the capacitor pulse impedance, the current probe measures the actual capacitor current to within 1%. The Stoddard current probes shown have a maximum linearity of $\pm$3% for pulse currents of up to 350 amperes. Large current levels such as these would generally be required to damage the higher capacitance value devices.

For capacitors with a relatively high pulse impedance at pulse end (such as units of a few picofarads) the instrumentation will be as shown in Figure 10. Here, smaller current probes are used which will minimize the lead length from capacitor "lo" to ground. The restriction in their use is that they can not be employed to measure extremely large current levels. For the small value capacitor units, though, large currents are not



CURRENT PROBE	PROBE SHUNT	RISE TIME	Pulse Width
Stoddard 91197-1	12.5 OHM	100 nsec	20 usec
Stoddard 91550-3	None	3 nsec	0.5&3 usec

Figure 9. Schematic of the Pulse Test Instrumentation for Large Capacitance Units



Current Probe	Rise Time	Pulse Width
Tektronix P6021	6.7 nsec	3 & 20 usec
Tektronix CT2	0.7 nsec	0.5 usec

Figure 10. Schematic of the Pulse Test Instrumentation for Small Capacitance Units

required to completely charge them. The Tektronix P6021 probe is flat to within ±3% for pulse currents up to 60 amperes and 20 microseconds duration. The CT-2 probe is flat to within ± 3% for pulse currents up to 100 amperes and 1 microsecond duration. There may be some restrictions on the maximum magnitude of the voltage monitor resistor due to the risetime effects associated with the resistor shunt capacitance. The smaller this resistance value the less the effect. However, by lowering this resistor the maximum pulse voltage that the capacitors can be charged to is also lowered. One could alleviate this problem by using a 50 ohm attenuator in a tee connection between the "load buffer attenuator" and "current limiter" interface shown in Figure 5. Here, though, one must resort to obtaining two separate signals and performing a subtraction in order to determine the capacitor voltage. This, in general, is less desirable then a direct measurement. At present, the optimum instrumentation to be used has not yet been defined with the critical aspect being the capability to obtain a low capacitance resistance string.

The pulse voltage and current delivered to the capacitors under test will be recorded using Tektronix R7912 Transient Digitizers and appropriate plug-ins and stored on magnetic tape for data processing. The vertical preamplifiers have a flat response of DC to 225 MHz for the 7A16A and DC to 500 MHz

for the 7A19. The time base units are capable of 5 seconds per division to 5 nanoseconds per division for the 7B50 and 0.2 seconds per division to 0.5 nanoseconds per division for the 7B92. As such, all anticipated waveshapes can be accurately recorded.

All voltage and current probes will, of course, be calibrated before use. Periodic calibration shots using high frequency carbon composition resistors as a test device will be obtained to insure the integrity of the pulse instrumentation. The device pulse test fixture will be proof tested for voltage breakdown at the maximum pulser output voltage level to insure the absence of fixture breakdowns which could erroneously be interpreted as device breakdown in the subsequent data analysis phase. The high energy pulse source will be buffered from the capacitor under test by the suitable output attenuators and matching networks previously described to minimize the voltage reflection coefficient across the test unit, thus insuring that the capacitor damage observed is a result of the primary power pulse applied to the unit.

7. DATA ACQUISITION AND REDUCTION

All pulse power data (current and voltage) and capacitor parameter data (capacitance, dissipation factor, and DC leakage current) for both the control and test units will be obtained using an automated computer controlled test system. This system has the capability of automatically obtaining the data together with the proper test condition identification and serialization, processing it, and storing it on magnetic tape for batch reduction on the H6060 computer system. The principle components of the system are as follows:

Tektronix R7912 Transient Digitizer (2)

- 7B50 Time Base Unit (2)
- 7B92 Time Base Unit (2)
- 7A16A Amplifier (2)
- 7A19 Amplifier (2)

Tektronix 632 TV Monitor

General Radio 1683 Automatic RLC Bridge

Cimron DMM50 Digital Multimeter (2)

Fluke 415A High Voltage Supply

DEC PDP 11/40 Computer

Tektronix 4010 Computer Terminal

Tektronix 4610 Hard Copy Unit

Datum 7 Track Magnetic Tape System

The pulse power data are acquired by the R7912 Digitizers, automatically processed by the PDP 11/40 Computer and stored on magnetic tape. Capacitor parameter data are acquired by the 1683 Bridge and DMM 50 Multimeters, automatically processed by the PDP 11/40 Computer and also stored on magnetic tape. Data identification is accomplished through the 4010 Computer Terminal.

The data reduction of the pulse power information will be provided in the form of a plot generated on the Calcomp 936 showing the actual pulse voltage and current levels developed across the capacitor test unit together with the average power delivered to the test unit throughout the pulse. The reduced capacitor parameter data will be provided in the form of a computer printout defining the complete pulse power-damage history of each device tested during the program from pretest to various levels of device damage. This information will include pertinent pulse parameters (such as pulse current and voltage and average power before and after voltage breakdowns) as well as the resulting damage effects, if any, on specific capacitor parameters (such as capacitance, loss, leakage and dielectric withstanding voltage.) Pulse polarity, where appropriate for polarized capacitors, will also be defined as well as any observations concerning mechanical damage or fracture. The data will be presented in a logical, systematic manner in the order of capacitor type and manufacturer, voltage

rating, pulse width, capacitance value and unit serial number. Pulse data for units which are pulsed more than one time would be printed out in the order of the test unit's exposure to the high energy pulse source.

The specific format and information content of the computer printout will depend on the damage responses exhibited by the capacitor types evaluated and will be defined in concurrence with the AFWL Project Officer.

8. FAILURE ANALYSIS

The depth of failure analysis consistent with the Program Scope can primarily be accomplished using straightforward optical microscopy techniques. This is particularly true in capacitor classes employing a foil type structure, although other classes are also amendable to this approach. By observing the relative position of the damage site (electrode center or edge) and its form (puncture, surface scorch, vaporized electrode), one can evaluate the type of failure mechanism associated with the unit (dielectric punch through, surface arc over, electrode burn out). The capacitor damage resulting from the pulse power stressing is anticipated to be generally manifested by these physical appearances. For capacitor classes which are more difficult to unencapsulate, X-ray - Vidicon techniques would be more appropriate. Some cross sectioning and optical microscopy evaluations of these classes might be

performed, although this would involve a very minimal effort.

It is planned to subject a minimum of 100 units to at least an optical microscopy failure analysis. It is felt that this quantity represents the anticipated number of units which will give an adequate representation of the various capacitor classes and manufacturers encountered. The exact mix of capacitor class, manufacturer, capacitance and working voltage ratings will depend on which types exhibit damage and their respective damage severity.

9. DATA ANALYSIS

As indicated previously, the overall objective of the program is to provide a broad experimental data base for predicting capacitor failure levels and failure mechanisms when exposed to pulse power environments. To meet this objective, the extensive test data obtained during the program will be displayed in a convenient and compact format to show the logical development of any damage prediction methodology concluded from the program work.

The first level of the data analysis has been previously described in Section 3.7 and is in the form of a computerized printout defining the complete pulse power-damage history of each unit tested. The next level of summarization planned is to provide graphical displays of capacitor electrical parameter

damage versus pulse current (or power) as a function of pulse width for each capacitor class, manufacturer, capacitance value and working voltage rating. These will be provided in the form of computer generated plots using the Calcomp 936 plotter. These plots can be readily generated since the entire experimental data bank (pulse damage levels and capacitor electrical parameters) will be stored on magnetic tape and readily accessable through the use of a systematic serialization system identifying capacitor class, capacitance, working voltage, pulse width, shot number, etc.

These data consolidation displays will be used in conjunction with the failure analysis results to formulate the primary failure mechanisms associated with the capacitors. The data obtained from these displays will be used to obtain the next level of summarization which is an intercomparison of failure levels for various capacitance and working voltage ratings within a device class as well as an intercomparison of failure levels for various capacitor classes. This intercomparison will be established as a function of pulse width and capacitor parameters. It is currently envisioned that the format for this will be in the form of a compact functional relationship defining capacitor parameter damage extent as a function of pulse level, pulse width, and initial capacitor characteristics. This will be accomplished by performing a multifunction regression analysis of the experimental data

using in place computer curve fitting routines. The results of this will define the average failure levels and failure level bounds as well as failure trends for the various capacitor classes.

10. COMPONENT SELECTION AND TEST MATRIX

The test matrix defining the device selection and experimental conditions is of prime importance since this forms the foundation for the entire program. Through proper and judicious selection, maximum application of program results to various military systems of concern can be obtained from the available device inventory. Here, such aspects as evaluating a large enough spread in nominal capacitance value, working voltage rating, and capacitor type in order to extend the experimental results to be applicable to a broad range of device values was considered in defining the text matrix. A suitably defined large range in device characteristics is also desirous in order to evaluate possible damage correlation on a per working volt rating/microfarad capacitance basis. Other more subtle considerations were with respect to correlating different manufacturers' parts to particular part standards which, when procured to a certain MIL specification designation, could result in a large variety of manufacturers' and construction peculiarities being supplied as the same part. Here, selection will be based on testing, if possible, similar MIL

specification part types from various manufacturers in order to determine their relative susceptibility. It is anticipated that less emphasis will be placed on the larger capacitance and voltage rated devices at the shorter pulse widths, due to the possible limitations of the pulsing equipment to inflict significant damage. Additional considerations would be in the area of duplicity of data. Obviously, devices and experimental conditions defined for test should be only those for which adequate test data are nonexistent and for which an adequate supply of test samples is available.

Close coordination with the AFWL Project Officer was maintained during the development of the test matrix. The Project Officer supplied a parts list of various manufacturers and construction types available for test. Table 2 shows an overview of the various capacitor types and manufacturers which are contained in the available parts list. The parts list provided was in terms of part number designations which were used in procuring the respective parts. The part number designations were a mix of individual manufacturer's designations and MIL specification designations; in many cases the manufacturer's designation corresponded to a part which met the MIL specification designation for another manufacturer. In some cases the part types represented commercial units which did not meet any particular MIL specification.

Table 2. Available Capacitor Types and Manufacturers.

DIELECTRIC \ MANUFACTURER	AEROVOX	ARCO	CORNELL-DUBILIER	CORNING	DUCATI	EL-MENCO	ERIE	GENERAL ELECTRIC	GENERAL INSTRUMENTS	GUDEMAN	IEC	KEMET	MALLORY	MICAMOLD	SPRAGUE	TANSITOR	TRW	WEST-CAP	VITRAMON
GLASS				X															X
MICA			X			X			X										
CERAMIC	X						X					X			X			X	
PLASTIC: METALLIZED POLYCARBONATE																	X		
PLASTIC: METALLIZED POLYESTER								X											
PLASTIC: MYLAR																	X		
PLASTIC: POLYCARBONATE								X									X		
PLASTIC: POLYESTER								X											
PAPER	X								X	X				X				X	
TANTALUM: SOLID, POLARIZED				X								X			X				
TANTALUM: WET SLUG, POLARIZED								X					X		X				
TANTALUM: PLAIN FOIL, POLARIZED								X							X				
TANTALUM: PLAIN FOIL, NON POLARIZED								X											
TANTALUM: ETCHED FOIL, POLARIZED								X					X		X	X			
TANTALUM: ETCHED FOIL, NON POLARIZED								X							X				
ALUMINUM		X			X			X			X		X		X				

This information, together with various manufacturers' catalogs, contacts, and MIL specifications, was used to define a common base or reference point for comparison of the various capacitor types. The essential results of this correlation are given in Table 3. Shown here is the number of available units within various capacitance values for each of the capacitor dielectric types as well as the relationship of the various capacitor types to appropriate MIL specifications and a definition of their various voltage-ambient temperature ratings. It is interesting to note that, in some cases, the voltage rating for some tantalum MIL specification types will vary depending upon the capacitor operating temperature.

The broad objective of the Program is to obtain EMP damage data on electrical capacitors applicable in the pulse-width range of 500 nanoseconds to 20 microseconds. As previously indicated the pulse damage testing will be performed at 500 nanosecond, 3 microsecond, and 20 microsecond pulse widths. In many cases, however, testing at a 500 nanosecond pulse width would be uninformative if the 3 or 20 microsecond pulse testing did not produce any device damage. In view of this, a logical three phase Test Matrix development program is planned which will maximize the informative data output of the program while being flexible enough to provide for

Table 3. Inventory of Available Capacitor Types.

CAPACITOR TYPE	MANUFACTURER	MFR TYPE	MIL TYPE	VOLTAGE RATING	AVAILABLE UNITS AT INDICATED CAPACITANCE VALUE																		
					PICOFARADS						NANOFARADS						MICROFARADS						
					1	3.4	11	34	110	340	1.1	3.4	11	34	110	340	1.1	3.4	11	34	110	340	1.1K
					3.3	10	33	100	330	1K	3.3	10	33	100	330	1K	3.3	10	33	100	330	1K	3.3K
GLASS	CORNING	CYR	CYR 53	300 @ 125°C							20												
		TYO	CY06	300 @125°C	20	20			20														
		CYFM	CY10	300 @125°C					20														
		CYFM	CY30	300 @125°C								20											
		CYFM	CY13	500 @125°C					20														
		CYFR	AFJ950 (10)	300 @125°C					20														
		CYFR	AFJ950 (15)	300 @125°C							20												
		CYFR	AFJ950 (20)	300 @125°C								20											
		CYFR	AFJ950 (10)	500 @125°C	23		6	40															
		CYFR	AFJ950 (20)	500 @125°C							20												
	VITRAMON	HRCY13		300 @125°C					20														
		VY	CY22	300 @125°C							20												
		VY	CY12	500 @125°C				20															
		VY	CY13	500 @125°C			20																
MICA	CORNELL-DUBILIER	CD6		100 @125°C				20															
		CD6		500 @125°C		20		20															
	EL-MENCO	DM10					60		89														
		DM10	CM04	500 @125°C					30														
		DM15	CM05	500 @125°C		20	49		15	50													
	GENERAL INSTRUMENTS	RDM	CM06	500 @125°C							20												
CERAMIC	AEROVOX	MC	CK06	100 @125°C										25									
			CK05	200 @125°C				25			25												
	ERIE	8123/27	CK05	50 @125°C										30									
		8123/27	CK05	100 @125°C							12												
		8123/27	CK05	200 @125°C				50															
		8133/37	CK06	200 @125°C								30											
		CK62	CK62	500 @125°C							25												
	KEMET	CK	CK12	100 @125°C				20		20													
		CK	CK05	200 @125°C				25															
		CK	CK06	200 @125°C							25	25											
	SPRAGUE	5GA		1000 @85°C				25															
	WEST-CAP		CKR11	100 @125°C				25		25		25											
			CK06	100 @125°C										25									
			CK12	100 @125°C								25											
			CK05	200 @125°C					25	25													
			CK06	200 @125°C							25	25											

Table 3. (continued)

CAPACITOR TYPE	MANUFACTURER	MFR TYPE	MIL TYPE	VOLTAGE RATING	AVAILABLE UNITS AT INDICATED CAPACITANCE VALUE																		
					PICOFARADS						NANOFARADS						MICROFARADS						
					1	3.4	11	110	110	340	1.1	3.4	11	34	110	340	1.1	3.4	11	34	110	340	1.1K
					3.3	10	33	100	330	1K	3.3	10	33	100	330	1K	3.3	10	33	100	330	1K	3K
PLASTIC: MYLAR	TRW	601PE		50 @ 85°C									20		20								
		608		50 @ 85°C									20	20									
PLASTIC: POLYCARBONATE	GENERAL ELECTRIC	74F51		100 @ 85°C								20			20	20							
		74F51		200 @ 85°C										20									
	TRW	463UW		50 @ 125°C								20			20								
PLASTIC: METALLIZED POLYCARB.	TRW	X440		50 @ 125°C							20		20	20									
PLASTIC: POLYESTER	GENERAL ELECTRIC	63F	CTM	50 @ 125°C						20	20	20		20		20							
PLASTIC: METALLIZED POLYEST.	GENERAL ELECTRIC	BA		100 @ 85°C										20		20							
		BA		200 @ 85°C										20									
PAPER	AEROVOX	P123ZN		200 @ 125°C						20													
		P123ZN		400 @ 125°C							20												
		P3235XP		600 @						5													
	GENERAL INSTRUMENTS		CP04	200 @ 85°C										20									
			CP04	400 @ 85°C								20		20									
	GUDEMAN		CP04	100 @ 85°C										20									
	MICAMOLD		CP04	600 @ 85°C								20											
			CP08	1000 @								20											
	WEST-CAP		CP04	400 @ 85°C						8													
			CP04	600 @ 85°C						20				20									
			CP04	100 @ 85°C								20											
ALUMINUM: POLAR	ARCO			3 @																	25		
				150 @												25							
	DUCATI			3 @															25				
				100 @												25							
	GENERAL ELECTRIC	76F		12 @ 85°C												20		20					
		76F		15 @ 85°C												20		20		20			
		76F		25 @ 85°C												20		20		20			
		76F		50 @ 85°C												20		20		20			
	IEC			3 @												25							
				25 @												25							
				50 @												25							
	MALLORY	MTA		3 @ 65°C																25			
		TT		250 @ 85°C												25							
	SPRAGUE			3 @																25			
		39D		3 @ 85°C																			15
		TE		10 @ 85°C															25				

Table 3. (continued)

CAPACITOR TYPE	MANUFACTURER	MFR TYPE	MIL TYPE	VOLTAGE RATING	AVAILABLE UNITS AT INDICATED CAPACITANCE VALUE																		
					PICOFARADS						NANOFARADS						MICROFARADS						
					1	3.4	11	34	110	340	1.1	3.4	11	34	110	340	1.1	3.4	11	34	110	340	1.1K
					3.3	10	33	100	330	1K	3.3	10	33	100	330	1K	3.3	10	33	100	330	1K	3K
TANTALUM: SOLID, POLAR	CORNING	TS	CS13	35 @ 85°C								20		20		20							
	KEMET	T110	CSR13	6 @ 85°C													30	30		20			
		T110	CSR13	10 @ 85°C																20			
		T110	CSR13	15 @ 85°C											20		30		20				
		T110	CSR13	20 @ 85°C										20		20		20	20				
		T110	CSR13	35 @ 85°C								6		40		20		20					
		T110	CSR13	50 @ 85°C								40		20		20			20				
		T110	CSR13	60 @ 85°C								20		20									
		T110	CSR13	75 @ 85°C								20											
		T110	CSR13	100 @ 85°C								20											
	SPRAGUE	150D		35 @ 85°C												20							
TANTALUM: WET SLUG, POLAR	GENERAL ELECTRIC	69F	CL64	25 @ 85°C														25					
		69F	CL64	50 @ 85°C														25					
	MALLORY	TLS	CL64	25 @ 85°C														20					
	SPRAGUE	CL64	CL64	50 @ 85°C														17					
TANTALUM: PLAIN FOIL, POLAR	GENERAL ELECTRIC	29F	CL34	15 @ 85°C														20					
		29F	CL34	75 @ 85°C												40							
		29F	CL34	150 @ 85°C													3						
	SPRAGUE	120D		15 @ 125°C															10				
TANTALUM: PLAIN FOIL	GENERAL ELECTRIC	29F	CL36	15 @ 85°C														20					
		29F	CL36	50 @ 85°C												20							
TANTALUM: ETCHED FOIL, POLAR	GENERAL ELECTRIC	29F	CL24	50 @ 85°C														20					
		29F	CL24	100 @ 85°C													3						
		29F	CL24	150 @ 85°C												20							
	MALLORY	TBF	CL24	15 @ 85°C																	2		
	SPRAGUE	CL24	CL24	15 @ 85°C															3				
		CL24	CL24	25 @ 85°C															20				
		112D		30 @ 85°C														20					
	TANSITOR	TEF	CL24	15 @ 85°C																	1		
		TEF	CL24	150 @ 85°C														3	3				
TANTALUM: ETCHED FOIL	GENERAL ELECTRIC	29F	CL26	100 @ 85°C												20							
	SPRAGUE	CL22	CL22	10 @ 85°C														7					

alternate approaches which would be identified from the initial experimental data results.

The first phase would be associated with the longest pulse width damage testing at 20 microseconds since this represents the maximum pulser capability to reach capacitor breakdown overstress conditions in the largest range of capacitance and working voltage values. Heavier emphasis would be placed on evaluating the lower capacitance and working voltage rating devices within each capacitor class since they can be charged to a higher critical overstress level. Polarized units would be evaluated for damage in both the positive and negative directions of polarization. For the purposes of the Test Matrix they would be considered as separate entities for testing, for at least during the first phase, until their relative susceptibilities could be established.

Once the 20 microsecond tests have been performed and the damage levels of various device classes, capacitance and voltage ratings established, then the parts test matrix for the second phase testing at 3 microseconds can be intelligently defined. A similar procedure would be used in defining the 500 nanosecond parts test matrix (third phase) from the 3 microsecond test results. In this way only those capacitor types which could be damaged at the longer pulse widths would

be considered for shorter pulse width testing, thus resulting in the maximum amount of damage data while avoiding extensive uninformative nondamage testing.

The actual part types and capacitance/voltage values to be tested will be selected in concurrence with the AFWL Project Officer and will be chosen from the candidates shown in Table 3. A minimum of 2000 devices will be tested during the Program.

SECTION IV

PROGRAM SCHEDULE AND DOCUMENTATION

In order to accomplish the proposed work in a timely manner such that the overall program objectives are best satisfied, close liaison and technical interfaces with the AFWL Project Officer will be maintained. The time schedule presented below shows the key program milestones and program documentation as related to the program schedule and CDRL portions of the test program.

Contract Authorization	July 14, 1975
Test Plan Submittal	August 25, 1975
Phase 1 Test Matrix Submittal	August 25, 1975
Test Plan Review	September 3, 1975
Test Plan Approval	September 9, 1975
Program Review Meeting (@GE)	September 9, 1975
Begin Phase 1 Testing	September 10, 1975
Program Review Meeting (@AFWL)	November 7, 1975
Phase 2 Test Matrix Submittal	November 7, 1975
Begin Phase 2 Testing	November 10, 1975
Begin Data analysis & Documentation	November 24, 1975
Begin Failure Analysis	November 24, 1975
Program Review Meeting (@AFWL)	December 9, 1975
Phase 3 Test Matrix Submittal	December 9, 1975

Begin Phase 3 Testing	December 10, 1975
Program Review Meeting (@AFWL)	January 6, 1976
End Technical Effort	January 14, 1976
Draft Final Report Submittal	February 13, 1976
Draft Final Report Approval	March 12, 1976
Final Technical Report	April 14, 1976

DISTRIBUTION

No. cys	
1	Cdr, Picatinny Arsenal (Tech Lib), Dover, NJ 07801
1	Cdr, NESC (Tech Lib), Wash, DC 20360
1	Maxwell Lab (Tech Lib), 9244 Balboa Ave, San Diego, CA 92123
1	DCEC (R124C), 1860 Wiehle Ave, Reston, VA 22090
2	DDC (TCA), Cameron Sta, Alexandria, VA 22314
1	Cdr, DESC (ECS/Tech Lib), 1507 Wilmington Pike, Dayton OH 45401
3	DDR&E (Dep Dir, Strat/Sp Sys; DAD SK, G. Barse; S&SS (OS)), Wash, DC 20301
2	Cdr, FC DNA (FCPS; FCPR), Stop 44
1	JSTPS (Tech Lib), Offutt AFB, NE 68113
1	Dir, NSA (Tech Lib), Ft Meade, MD 20755
2	Dir, BMDATC (Tech Lib; SSC-TEN, N. Hurst), POB 1500, Huntsville, AL 35807
1	Ch, R&D, Dept Army (DARD-DDM-N, LtC Goncz), Wash, DC 20310
1	Cdr, USAMC, RSIC (Ch, Doc Sec), Redstone Arsenal, AL 35809
1	Cdr, SCA (ACCX-SAT-EMP), Ft Huachuca, AZ 85613

No. cys	
1	Cdr, SSSAC (Ch, Act Div), POB 631, Langdon, ND 58249
1	Cdr, USA-A (NBC DIV AFZT-PTS-C, Maj Dean), APO Seattle, WA 98749
1	Cdr, USAEC (AMSEL-TL-IR, Dr. Hunter), Ft Monmouth, NJ 07703
1	Cdr, ASD (Tech Lib), WPAFB, OH 45433
1	Sim Phys (J. Uglum), POB 974, Boxborough, MA 07120
1	CICCADC (DCS/C&E, CESA), Ent AFB, CO 80912
1	Cdr, DCA, Nat Mil Cmd Sys Spt Ctr (Tech Lib), Wash, DC 20305
1	Dir, DIA (Tech Lib), Wash, DC 20301
	Dir, DNA, Wash, DC 20305
2	(STTL)
4	(RAEV)
3	(STSI; STVL; DDST, P. Haas)
1	Intsvc Nuc Wpn Sch (Doc Cont), Stop 9
1	Ch, FC DNA, LLL (L-395), POB 808, Livermore, CA 94550
1	Ofc JCS (Tech Lib), Wash, DC 20301
1	Asst CS, Com/Elc (CEED-7, W. Heath), Dept Army, Wash, DC 20314
1	CE, Dept Army (DAEN-MCE-D, Mr. McCauley), Wash, DC 20310
1	Dept Army, FESA (Ch, R&T Div), Ft Belvoir, VA 22060

No. cys	
	Cdr, Diamond Lab (AMXDO), 2800 Powder Mill Rd, Adelphi, MD 20783
5	(EM, A. Renner; J. Klebers; R. Bostak; R. Wong; R. Gray)
1	(RB, J. Miletta;
2	(NP, S. Marcus; F. Wimenitz)
3	(RBF, J. Tompkins; RC, Dr. Oswald; TI)
1	Cdr, TRASANA (SSEA-EAB, F. Winans), WSMR, White Sands, NM 88002
1	Cdr, USACSC (Tech Lib), Ft Belvoir, VA 22060
2	Ch, USACSA (S. Krevsky, DD Eng; Tech Lib), Ft Monmouth, NJ 07703
1	Cdr, USAMER&DC (Tech Lib), Ft Belvoir, VA 22060
1	Cdr, USANA (Tech Lib), Ft Bliss, TX 79916
2	Ch, USAN&CSGp (MOSG-NO, Maj Winslow; Tech Lib), Bldg 2073, No Area, Ft Belvoir, VA 22060
1	Cdr, WSMR (STEWS-TE-NT, M. Squires), White Sands, NM 88002
1	OIC, CEL, NCBC (Tech Lib), Pt Hueneme, CA 93041
1	CO, NAD (Tech Lib), Crane, IN 47522
1	Cdr, NELC (Tech Lib), San Diego, CA 92152
1	Supt, NPS (2124), Monterey, CA 93940
5	Cdr, NSWC (431, Dr. Malloy; E. Dean; M. Petree; 130-215, E. Rathbun; Tech Lib/Info Svc Div), White Oak, Silver Spring, MD 20910
1	Cdr, NWC (753), China Lake, CA 93555
1	CO, NWEF (ADS), Stop 40

No. cys	
1	Cdr, ASD (YHEX, Maj Leverette), WPAFB, OH 45433
1	AFATL (DLOSL), Eglin AFB, FL 32542
1	Cdr, FTD (PQAL), WPAFB, OH 45433
1	SAMSO (MN), Norton AFB, CA 92409
2	CICSAC (NRI/STINFO; XPFS, Maj Stephan), Offutt AFB, NE 68113
2	USAEC NVL (Capt Parker; Tech Lib), Ft Belvoir, VA 22060
	Cdr, USAMC, Redstone Arsenal, AL 35809
2	(AMSMI/RGP, H. Green; V. Rowe)
3	(AMCPM/MD, SAM-D Proj Mgr; AMCPN/HA, HAWK Proj Mgr; Tech Lib)
1	Proj Mgr, USATDS (Tech Lib, Ft Monmouth, NJ 07703
1	Cdr, USAT&EC (Tech Lib), Abdn Pvg Gnd, MD 21005
1	Ch, NOps, Dept Navy (Tech Lib), Wash, DC 20350
1	Cdr, NASC (Tech Lib), Wash, DC 20360
1	Cdr NCC (Tech Lib), 4401 Massachusetts Av NW, Wash, DC 20390
1	Cdr, NOSC (ORD-034C, S. Barnham), Wash, DC 20360
9	Dir, NRL (4004, Dr. Brancato; 6603F, R. Statler; 2627, D. Folen; 6633, J. Ritter; Tech Lib; 7706, J. Boris; 7701, J. Brown; 464, R. Joiner; 7770, D. Levine), Wash, DC 20375
	Cdr, NSWC, Dahlgren, VA 22448
2	(W. H. Holt)
2	(FUR, Dr. Amadori; Tech Lib)

No. cys	
1	Dir, SSPO, Dept Navy (Tech Lib), Wash, DC 20376
1	ARL (Tech Lib), WPAFB, OH 45433
1	Cdt, AFFDL (R. Beavin), WPAFB, OH 45433
1	CS, USAF (RDQPN), Wash, DC 20330
1	Cdr, RADC (Tech Lib), Griffiss AFB, NY 13441
2	LASL (Rpt Lib; K. Riepe, L-1), POB 1663, Los Alamos, NM 87544
1	Sandia Lab (K. Mitchell, 8157), POB 969, Livermore, CA 94550
6	ESD (DCD/SATIN IV; DCKE, L. Staples; YWES; XRE-Surv; MCAE, LtC Sparks; XRP, Maj Gingrich), Hanscom AFB, MA 01730
7	Sandia Lab (3141; E. Hariman; A. Limieux; 5223, C. Vittitoe; 2126, J. Cooper; 1935, J. Gover; 9353, R. Parker), Stop 40
2	CIA (RD/SI, Rm 5G48, Hq Bldg; Tech Lib), Wash, DC 20505
1	NASA-Marshall SFC (ASTR-MTD, A. Coleman, Bldg 4476), Huntsville, AL 35812
1	Aerojet El-Sys (T. Hanscome, 8170/D6711), POB 296, Azusa, CA 91702
1	Avco, GPG (Rsch Lib, A830/7201), 201 Lowell St, Wilmington, MA 01887
1	BMI (Tech Lib), 505 King Ave, Columbus, OH 43201
1	BPC (Proj Mgr, Gov Proj, H. Dietze), POB 60860, LA, CA 90060
1	Bendix Aerosp Sys Div (R. Pizarek), 3300 Plymouth Rd, Ann Arbor, MI 48107

No. cys	
1	Bendix Nav/Cont Div (E. Lademann), Teterboro, NJ 07608
1	BA/H (R. Chrisner), 106 Apple St, New Shrewsbury, NJ 07724
3	BDM (D. Durgin; D. Alexander; Tech Lib), POB 8885, Sta C, Albuq, NM 87108
1	CSD Lab (Tech Lib), 68 Albany St, Cambridge, MA 02139
1	CEC (Tech Lib), 2630 Glendale/Milford Rd, Cincinnati, OH 45241
8	SAMSO (SKT, P. Stadler; RSP, LtC Gilbert; DYS, Maj Heilman; SZH, Maj Schneider; SKD; IND, I. Judy; DYJB, Capt Ingram; SZJ, Capt Dejonckheere), POB 92960, WWPC, LA, CA 90009
2	UCC, Holifiend Nat Lab (Dr. D. Nelson; Tech Lib), POB X, Oak Ridge, TN 37830
1	UC, LLL (Tech Lib), POB 808, Livermore, CA 94550
1	Dept Commerce, NBS (J. French, Elc Tech Div), Wash, DC 20234
1	NASA-Lewis RC (Lib), 21000 Brookpark Rd, Cleveland, OH 44135
13	Aerosp Corp (Lib; S. Bower; Dr. Pearlston, A2/220; R. Murtensen, Hard Reent Sys; J. Benveniste; Dr. Comisar; Dr. Reinheimer; I. Garfunkel, 115/2076; R. Crolius, A2/1027; N. Stockwell, N&E Stf; L. Aukerman, 120/2841; V. Josephson, D&S Dir; D. McPherson, Tech Surv Dir), POB 92957, LA, CA 90009
1	Bell Aerosp (Tech Lib), POB 1, Buffalo, NY 14240
1	Bell Tel Lab (Tech Lib), Mountain Ave, Murray Hill, NJ 07974
1	Bendix RLD (D. Niehaus, Mgr, Pgm Dev), Bendix Cen, Southfield, MI 48075

No. cys	
8	Boeing Co (R. Caldwell; D. Isbell; D. Egelkrout; Lib; Dr. Dye, 2-6005, 45-21; H. Wicklein, 17-11; A. Lowrey, 2R-00; D. Kemle), POB 3707, Seattle, WA 98124
1	Brn Eng (Tech Lib), Cummings Rsch Pk, Huntsville, AL 35807
1	Burroughs Fed/Spec Sys (Tech Lib), Central Ave/Rte 252, Paoli, PA 29301
1	CRC (M. Lahr, Lib, 106-216), 5225 C Ave NE, Cedar Rapids, IA 52406
1	CSC (P. Carleston), POB 530, Falls Church, VA 22046
1	EG&G (Tech Lib), POB 10218, Albuq, NM 87114
2	FC&IC (D. Myers, 2-233; Tech Lib), 464 Ellis St, Mountain View, CA 94040
2	Franklin Inst (R. Thompson; Tech Lib), 20 St/Pkwy, Phila, PA 19103
1	Gen Dyn Corp, Elc Div (Tech Lib), POB 81127, San Diego, CA 92138
6	GE Co, Sp Div, VFSC (L. Chasen; J. Peden, CCF 8301; D. Tasca, 8301-C8; J. Spratt, M9549 J. Andrews, Rad Eff Lab; TIC), POB 8555, Phila, PA 19101
1	GE Co (B. Showalter, 160), POB 5000, Binghampton, NY 13902
1	GE Co (Tech Lib), POB 1122, Syracuse, NY 13201
1	GRC (Dr. Johnson), 1501 Wilson Blvd, Suite 700, Arlington, VA 22209
1	Goodyear Aerosp Corp (B. Manning), Litchfield Park, AZ 85340
1	GTE Sylv, ESGp (Tech Lib), 77 A St, Needham, MA 02194

No. cys	
1	Harris Semicond (C. Davis), POB 883, Melbourne, FL 32901
2	Hercules Bacchus Plt (R. Woodruff, 100K-26-W; Tech Lib), POB 98, Magna, UT 84044
2	Honeywell Aerosp (H. Noble, Stf Eng, 725-5A; Tech Lib), 13350 US Hwy, St Pettersburg, FL 33733
4	Hughes Acft, ASD (A1080, W. Scott; C624, E. Smith; A1080, H. Boyte; Tech Lib), POB 92919, LA, CA 90009
1	Dikewood (Tech Lib), 1009 Bradbury Dr SE, Univ Rsch Pk, Albuq, NM 87106
1	Elc Com (J. Daniel, 9), POB 12248, St Petersburg, FL 33733
2	Fairchild Ind, SFTC (Mgr, CD&S; Tech Lib), 20301 Century Blvd, Germantown, MD 20767
2	Garrett Corp (R. Weir, 93-9; Tech Lib), 9851 Sepulveda Blvd, LA, CA 90009
1	GE Co, Ord Sys (D. Corman, 2171), 100 Plastics Ave, Pittsfield, MA 01201
1	GE Co, RESD (Tech Lib), POB 7722, Phila, PA 19101
1	GE Co, AES (Tech Lib), French Rd, Utica, NY 13503
2	GE Co, TEMPO-Cen Adv Stud (Dr. Rutherford; DASIAC), PODwr QQ, Santa Barbara, CA 93102
1	GE Co, AEG-TIC (J. Ellerhorst, E2), Evendale Plt, Cincinnati, OH 45215
3	GRC (Dr. Hill; J. Ise; TIO), POB 3587, Santa Barbara, CA 93105
2	Grumman Aerosp Corp (J. Rogers, 533, Pt 35; Tech Lib), S. Oyster Bay Rd, Bethpage, NY 11714
1	GTE Sylv (Tech Lib), 189 B St, Needham Heights, MA 02194

No. cys	
2	Hazeltine Corp (M. Waite, TL; J. Colombo), Pulaski Rd, Green Lawn, NY 11740
2	Honeywell GAPD (Tech Lib; R. Johnson, A1391), 1625 Zarthan Ave, Minneapolis, MN 55416
1	Honeywell RC (Tech Lib), 2 Forbes Rd, Lexington, MA 02173
1	Hughes Acft, GSGp (Lib, 600, C-222), 1901 W. Malvern Ave, Fullerton, CA 92634
3	IITRI (I. Mindel; J. Bridges; Tech Lib), 10 W. 35 St, Chicago, IL 60616
6	Hughes Acft (K. Walker, D157; B. Campbell, 6-E110; W. McDowell, R&D; Dr. Binder, 6-D147; Dr. Singletary, D157; Tech Lib), Centinela/Teale Sts, Culver City, CA 90230
1	ITT (Tech Lib), 500 Washington Ave, Nutley, NJ 07110
1	ITT Cannon Elc (D. Shaff), 2801 Air Lane, Phoenix, AZ 85034
1	Litton Sys, Elc Tube Div (F. McCarthy), 1035 Westminster Dr, Williamsport, PA 17701
1	LTV Aerosp, VSD (TDC), POB 6267, Dallas, TX 75222
2	LTV Aerosp (T. Rozelle; Tech Lib), POB 909, Warren, MI 48090
1	MM Aerosp (Tech Lib), POB 5837, Orlando, FL 32805
2	McDon Doug (Dr. Ender, 313, 33; Tech Lib), POB 516, St Louis, MO 63166
1	McDon Doug (T. Lundregan), POB 1850, Albuq, NM 87103
1	MRC (Dr. Van Lint), 7650 Convoy Ct, San Diego, CA 92111
1	Mitre Corp (Tech Lib), POB 208, Bedford, MA 01730

No. cys	
1	Northrop Elc Div (Tech Lib), 1 Rsch Pk, Palos Verdes Peninsula, CA 90274
1	Northrop Elc Div (Tech Lib), 2301 W. 120 St, Hawthorne, CA 90250
1	Philco-Ford WDLD (Tech Lib), 3939 Fabian Way, Palo Alto, CA 94303
1	Pulsar Assoc (C. Jones), 7911 Herschel Ave, La Jolla, CA 92037
1	Rand Corp (Tech Lib), 1700 Main St, Santa Monica, CA 90406
1	IITRI, ECAC (Tech Lib), North Severn, Anapolis, MD 21402
1	IRT (Tech Lib), POB 81087, San Diego, CA 92138
1	IBM (Tech Lib), Rte 17C, Owego, NY 13827
1	Ion Phys (Tech Lib), S. Bedford St, Burlington, MA 01803
1	Kaman Sci (Tech Lib), POB 7463, Colorado Springs, CO 80933
2	Litton Sys, Data Sys (S. Sternbach; Tech Lib), 8000 Woodley Ave, Van Nuys, CA 91406
1	Lockheed M/S (TIC, G. Evans, 0-52-52), 3251 Hanover St, Palo Alto, CA 94304
2	MIT, Linc Lab (A. Stanley; L. Loughlin, Lib), POB 73, Lexington, MA 02173
1	MM Corp (Tech Lib), POB 179, Denver, CO 80201
1	McDon Doug (Tech Lib), 5301 Bolsa, Huntington Beach, CA 92647
1	MRC (Tech Lib), 325 State St, Santa Barbara, CA 93101
2	MRC (D. Merewether; Tech Lib), POB 8693, Sta C, Albuq, NM 87108

No. cys	
2	NAS (Dr. Shane, Nat Mtls Adv Bd; Tech Lib), 2101 Constitution Ave NW, Wash, DC 20418
1	Northrop R&TC (Tech Lib), 3401 W. Broadway, Hawthorne, CA 90250
1	Philco-Ford, A&COps, Aeronut (Tech Lib), Ford/Jamboree Rds, Newport Beach, CA 92663
2	Phys Int (TechLib; I. Smith), 2700 Merced St, San Leandro, CA 94577
1	R&D Assoc (Dr. W. Graham), POB 3580, Santa Monica, CA 90403
1	Raytheon (Tech Lib), 528 Boston Post Rd, Sudbury, MA 01776
2	Raytheon (G. Joshi, Rad Sys Lab; Tech Lib), Hartwell Rd, Bedford, MA 01730
2	RCA G&S Sys, AED (Dr. Brucker; Tech Lib), POB 800, Locust Corner, Princeton, NJ 08540
5	Rockwell Int (G. Messenger, FB61; R. Hubbs, FB46; J. Bell, HA 10; J. Sexton, CA 31; Tech Lib), 3370 Miraloma Ave, Anaheim, CA 92803
1	Sperry Rand Gyro Mgt Div (Tech Lib), Marcus Ave, Great Neck, NY 11020
1	Sperry Rand Univac Def Sys (Tech Lib), POB 3525, MS 1931, St Paul, MN 55101
1	Texas Instru (Tech Lib), POB 5474, Dallas, TX 75222
1	BDM (Dr. Neighbors), 7915 Jones Branch Drive, McLean, VA 22101
11	TRW Sys Gp (A. Liebschutz, R1-2154; J. Lubell; A. Narevsky, R1-2144; R. Whitmer; R. Kingsland, R1-2154; R. Webb, R1-1071; F. Holmquist, R1-1070; Dr. Sussholtz; TIC, S1930; Dr. Jortner; W. Robinette), 1 Sp Pk, Redondo Beach, CA 90278

No. cys	
2	UAC Ham Std (R. Gignere; Tech Lib), Bradley Int Aprt, Windsor Locks, CT 06069
2	Westinghouse D&ESC (H. Kalapaca, 3525; Tech Lib), POB 1693, Fndsp Int Aprt, Baltimore, MD 21203
2	Cdr, USAR&DCtr (AMXRD-BVL, J. McNeilly; Tech Lib), Abdn Pvg Gnd, MD 21005
2	Cdr, USASA (IARD-T, Dr. Burkhardt; Tech Lib), 4000 Arlington Blvd, Arlington, VA 22212
1	Litton Sys G&CSD (Tech Lib), 5500 Canoga Ave, Woodland Hills, CA 91364
1	RCA G&C Sys, M&S Rad (Tech Lib), Marne Hwy/Borton Ldg, Moorestown, NJ 08057
1	RTI (Dr. M. Simons, Eng Div), POB 12194, Research Triangle Park, NC 27709
1	Rockwell Int (Tech Lib), 5701 W. Imperial Hwy, LA, CA 90009
1	Sci Appl (Tech Lib), POB 2351, La Jolla, CA 92038
2	Sperry Rand Flt Sys Div (Tech Lib; D. Schow, 104C), POB 21111, Phoenix, AZ 85036
1	SRI (Tech Lib), 306 Wynn NW, Huntsville, AL 35805
1	SRI (Tech Lib), 333 Ravenswood, Menlo Park, CA 94025
2	Texas Tech Univ (T. Simpson; Tech Lib), POB 5404, N Col Sta, Lubbock, TX 79417
2	TRW Semicond (R. Clarke, Tech Stf; Tech Lib), 14520 Aviation Blvd, Lawndale, CA 90260
1	TRW Sys Gp (Tech Lib), POB 1310, San Bernardino, CA 92402
2	TRW Sys Gp (D. Pubsley; Tech Lib), POB 368, Clearfield, UT 84015

No. cys	
1	UAC Norden (C. Corda), Helen St, Norwalk, CT 06851
1	Univ Denver CO Sem, DRI (Tech Lib), Univ Pk, Denver, CO 80210
1	Westinghouse RL (R. Wootton 301-2B3), Pittsburgh, PA 15235
1	Cdr, USAADC (Tech Lib), Ent AFB, CO 80912
2	Cdr, USAMC (A. Nichols, NDB 300, 95; Tech Lib), Picatinny Arsenal, Dover, NJ 07801
2	Ch, NR, Dept Navy (R. Joiner, 464; Tech Lib), Arlington, VA 22217
1	CO, Diamond Lab (Lib), Wash, DC 20438
1	Hq USAF (XOOWD), Wash, DC 20330
2	AFSC (DLCAW; XRP), Andrews AFB, Wash, DC 20334
1	USAFA (FJSRL, CC), CO 80840
1	AFIT (Tech Lib, 640, B), WPAFB, OH 45433
2	CO, USAEC (AMSEL-10-T; Tech Lib), Ft Monmouth, NJ 07703
1	Dir Ofc, LLL (TID), POB 808, Livermore, CA 94550
1	Hq USAF (RDQPN, 1D425), Wash DC 20330
1	Dir, BMD Prog Off, (Tech Lib) 1300 Wilson Blvd, Arlington, VA 22209
1	Hq USAF, AFTAC, Patrick AFB, FL 32925
1	ADC (DPQY), Ent AFB, CO 80912
1	AUL (LDE), Maxwell AFB, AL 36112

No. cys	
	AFWL, KAFB, NM 87117
1	(HO, Dr. Minge)
2	(SUL)
5	(DYX: Dr. Wunsch)
5	(EL, J. Darrah; ELA, L. Eichwald, J. O'Donnell, R. Hays, D. Lawry)
5	(ELA)
1	Official Record Copy (Maj Nielsen, AFWL/ELA)
1	Lockheed M&S Co, (Tech Lib) POB 504, Sunnyvale, CA 94038
1	Dr P. P. Budenstein Physics Department Auburn, Alabama 36830
2	Lawrence Livermore Laboratory P.O. Box 808 Livermore, CA 94550 Dr L. C. Martin L-156; Dr J. Candy L-156
1	State University of NY at Buffalo 4232 Ridge Lea Road Amherst, NY 14226 Dr J. J. Whalen
2	U.S. Army Missile Command G Directorate Redstone Arsenal, Alabama 35809 D. Mathews - DRSMI-RGP

Official Record Copy (Maj Nielsen, AFWL/ELA)