AD NUMBER
ADB017987
LIMITATION CHANGES
TO: **Approved for public release; distribution is unlimited.**
FROM: **Distribution authorized to U.S. Gov't. agencies only; Test and Evaluation; MAR 1977. Other requests shall be referred to Rome Air Development Center, Griffiss AFB, NY 13441.**
AUTHORITY
RADC ltr 3 Dec 1979

RADC-TR-77-111
Final Technical Report
March 1977

A RELIABILITY STUDY AND INVESTIGATION OF COMPLEMENTARY MOS/SOS INTEGRATED-CIRCUIT TECHNOLOGY

RCA Solid State Technology Center

ROME AIR DEVELOPMENT CENTER
AIR FORCE SYSTEMS COMMAND
GRIFFISS AIR FORCE BASE, NEW YORK 13441

A RELIABILITY STUDY AND INVESTIGATION OF COMPLEMENTARY MOS/SOS INTEGRATED-CIRCUIT TECHNOLOGY

This report has been reviewed and is approved for publication.

APPROVED: R. Alan Blore

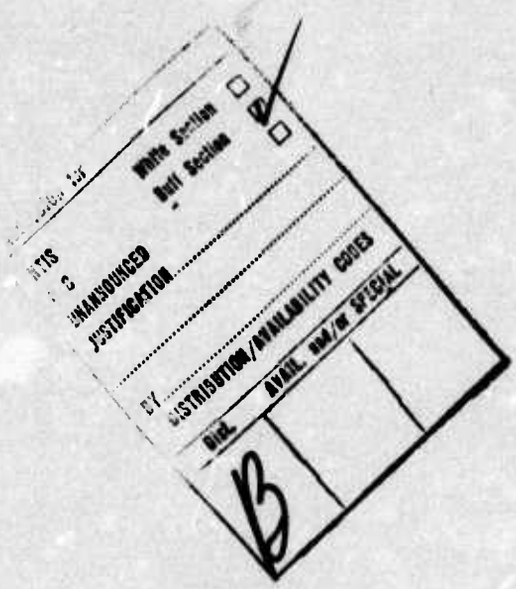
R. ALAN BLORE
Project Engineer

APPROVED: Joseph J. Naresky

JOSEPH J. NARESKY
Chief, Reliability & Compatibility Division

FOR THE COMMANDER: John P. Huss

JOHN P. HUSS
Acting Chief, Plans Office



Do not return this copy. Retain or destroy.

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE *(When Data Entered)*

REPORT DOCUMENTATION PAGE

READ INSTRUCTIONS BEFORE COMPLETING FORM

1. REPORT NUMBER: RADC-TR-77-111
2. GOVT ACCESSION NO.:
3. RECIPIENT'S CATALOG NUMBER:

4. TITLE *(and Subtitle)*: A RELIABILITY STUDY AND INVESTIGATION OF COMPLEMENTARY MOS/SOS INTEGRATED-CIRCUIT TECHNOLOGY

5. TYPE OF REPORT & PERIOD COVERED: Final Technical Report, 1 Apr 75 - 30 May 76

6. PERFORMING ORG. REPORT NUMBER: PRRL-76-CR-40

7. AUTHOR(s): G. Caswell, S. Cohen

8. CONTRACT OR GRANT NUMBER(s): F30602-75-C-0163

9. PERFORMING ORGANIZATION NAME AND ADDRESS: RCA Solid State Technology Center, Somerville NJ 08869

10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS: 61101F, 55190653

11. CONTROLLING OFFICE NAME AND ADDRESS: Rome Air Development Center (RBRP), Griffiss AFB NY 13441

12. REPORT DATE: March 1977

13. NUMBER OF PAGES: 130

14. MONITORING AGENCY NAME & ADDRESS *(if different from Controlling Office)*: Same

15. SECURITY CLASS. *(of this report)*: UNCLASSIFIED

15a. DECLASSIFICATION/DOWNGRADING SCHEDULE: N/A

16. DISTRIBUTION STATEMENT *(of this Report)*:
Distribution limited to U. S. Gov't agencies only; test and evaluation; March 1977. Other requests for this document must be referred to RADC (RBRP), Griffiss AFB NY 13441.

17. DISTRIBUTION STATEMENT *(of the abstract entered in Block 20, if different from Report)*:
Same

18. SUPPLEMENTARY NOTES:
RADC Project Engineer: R. Alan Blore (RBRP)

19. KEY WORDS *(Continue on reverse side if necessary and identify by block number)*:

CMOS/SOS	Silicon gate transistor
Enhancement-mode MOS transistors	Aluminum gate transistor
Reliability	Failure analysis
Stress tests	Screening
	Edge transistor

20. ABSTRACT *(Continue on reverse side if necessary and identify by block number)*:
The objective of this study was an evaluation of the reliability and associated failure mechanisms of complementary MOS integrated circuits using silicon-on-sapphire technology. The results of this investigation indicate that, with appropriate screening, the self-aligned Si-gate CMOS/SOS technology can provide reliability equivalent to that of the Al-gate, bulk-silicon CMOS technology.

The tests were conducted on CD4007 type inverter circuits processed in two

DD FORM 1 JAN 73 1473 EDITION OF 1 NOV 65 IS OBSOLETE

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE *(When Data Entered)*

405 931

different CMOS/SOS technologies: Al-gate and self-aligned Si-gate. The test program consisted of various combinations of electrical, thermal, and mechanical stresses designed to accelerate failure mechanisms. Extensive analysis was performed on the failed arrays, and predominant failure modes were determined. Activation energies for the predominant failure mechanisms were obtained, and results used for reliability predictions for both the Al-gate and the self-aligned Si-gate technologies. Recommendations for screening procedures for CMOS/SOS devices are also included.

It must be pointed out that the statistics resulting from this investigation apply only to the processes used by the manufacturers, A & B, whose parts were used for the stress-testing program. There is no intent to imply that the statistical results of this program apply to devices made by other manufacturers with similar technologies.

PREFACE

This Final Technical Report was prepared by RCA Solid State Technology Center, Somerville, New Jersey, under Air Force Contract F30602-75-C-0163. The contract was administered under the technical direction of Mr. R. A. Blore of the Rome Air Development Center, Griffiss Air Force Base, New York.

This report covers the work performed from 1 April 1975 to 30 May 1976. S. Cohen, Engineering Leader, Custom Monolithics Department, RCA Solid State Technology Center, had overall technical responsibility, under the direction of H. Borkan, Manager of Custom Monolithics, RCA Solid State Technology Center.

The authors wish to thank J. J. Fabula, D. S. Woo, and W. Ham for many helpful technical discussions; the RCA/SSTC Design Automation group, especially C. Lewin and H. Lambert for computer programming assistance; K. Long and H. Riehman for the electrical testing; and D. Brown, C. Grieff, and D. Woronka for their invaluable assistance throughout the entire program. The technical guidance of R. A. Blore and C. Salvo of the Rome Air Development Center is also gratefully acknowledged.

TABLE OF CONTENTS

TABLE OF CONTENTS (Continued)

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS (Continued)

LIST OF ILLUSTRATIONS (Continued)

LIST OF ILLUSTRATIONS (Continued)

LIST OF TABLES

EVALUATION

This report covers one of a series of efforts administered by the Reliability Branch of RADC, both in-house and contractually, to assess the reliability of the CMOS technology. RADC/RB has in the past and is continuing to study both bulk and sapphire CMOS approaches.

Silicon-on-sapphire (SOS) construction adds to the benefits of bulk CMOS in the areas of circuit density and radiation hardness. These are, of course, of interest to the Air Force and the other branches of the Department of Defense. This effort was intended to study the inherent reliability factors introduced by SOS processing. CD4007 type circuits were used. Three hundred parts were silicon gate and three hundred parts were aluminum gate. The silicon gate study was supplemented by the use of test insert chips to monitor various processing sensitive parameters.

The results of this study indicate that the major weakness in the aluminum gate process is the silicon island edge. The silicon gate process showed significant P-channel threshold drift, but achieved an extrapolated 72,000 hours median time to failure at 125°C. This is similar to bulk CMOS accelerated test results.

Results also indicate that high temperature storage was not a useful screen test, and both thermal shock and temperature cycling with intermittent bias were effective and practical screens.

Processing and design recommendations are presented for overcoming the weaknesses observed.

RADC/RB is planning continued CMOS reliability studies.

R. Alan Blore

R. ALAN BLORE
Project Engineer

I. DEVICE SELECTION AND RATIONALE

The circuit type selected for this program was the CMOS/SOS equivalent of the CMOS CD4007. This circuit consists of three n-channel and three p-channel enhancement-mode MOS transistors. The transistor elements are accessible through the package terminals and provide a convenient means for constructing inverters, 3-input NOR and 3-input NAND gates, high-current drivers, or dual bi-directional transmission gates. The complementary n- and p-transistor pairs, when connected as inverters, provided a convenient test vehicle for the stress test program.

A total of 600 CMOS/SOS arrays were used for this program, distributed by type and process as follows:

TYPE	DATE CODE	PROCESS	MANUFACTURER	QUANTITY
TCS056	7524	Si-gate	A	150
TC1092	7518	Si-gate	A	150
4007S	7349	Al-gate	B	300

Vendor A (Si-gate) parts were manufactured in accordance with MIL-STD-883A Method 5004.2 requirements for Class "B" devices. The Vendor B (Al-gate) arrays were ordered with a 100-nA maximum quiescent leakage current specification. No prior screening to MIL-STD-883A Method 5004.2 requirements had been performed. All Vendor B devices were subjected to the remaining applicable Method 5004.2 screening procedures prior to starting the test program (described in Section II). Due to the vendor withdrawing from the market, the parts received constituted the vendor's entire remaining inventory. Because of the quality difference in the procured parts, statistical comparison of the two technologies cannot be made. However, the failure mode and mechanisms are considered indicative of their respective technologies at the time of manufacture.

II. INITIAL SCREENING

A. INCOMING ELECTRICAL INSPECTION

The Al-gate arrays purchased from Vendor B exhibited a high failure rate during the incoming electrical tests. The predominant failure mode was high leakage current caused by low (<10 V) source-drain voltage breakdown levels. The 17-V V_{DD} test level was reduced to 10 V to prevent catastrophic failures during the test program. Analysis of the arrays passing the reduced level tests showed typical values for source-drain breakdown of 12 to 14 V, as compared with the 20- to 22-V levels observed on the Si-gate arrays. The inspection results are summarized in Table 1.

TABLE 1. INCOMING ELECTRICAL TESTS, VENDOR B, TYPE 4007S

Total tested	702
Total accepted*	447
Total failed	255
Leakage (I_{DSS})	238
Noise immunity (30%)	12
Functional	5

*V_{DD} reduced to 10 V for this test

B. MIL-STD-883A SCREENING

All devices used for the stress-test program were subjected to MIL-STD-883A, Method 5004.2, Class B screening. The tests and their respective MIL-STD-883A methods are listed in Table 2. The results of the tests are shown in Table 3.

Of the 447 4007S arrays subjected to the screening only 309 survived. The reasons for failure are shown in Table 4.

The bias burn-in at 125°C caused several additional failures for excessive current. These units were analyzed and the source-drain breakdown levels were all $\sim$10 V.

TABLE 2. SCREENING PROCEDURE: MIL-STD-883A, METHOD 5004.2, CLASS B

Screen	Method	Requirement
Internal Visual	2010.2	100%*
Stabilization Bake	1008.1C (24 h minimum)	100%*
Temperature Cycling	1010.1C (10 cycles) -65° to +150°C	100%
Constant Acceleration	2001.1E (Y1-plane)	100%
Hermeticity	1014.1 (A_1, C_1, and C_2)	100%
Burn-in	1015.1A (168 h at 125°C with bias)	100%
Post-Burn-In Electrical Test**	Per TCS056 test program	100%

*Not perfomed on 4007S.
**25°C data only. Separate pre-stress electrical tests were performed at 25°, -55°, and 125°C to establish the initial (0 hour) data base.

TABLE 3. SCREENING RESULTS

Type	Vendor	Received Incoming Electrical Test	Passed Incoming Electrical	Passed Post Screen Electrical	Used for Program
4007S	B	702	447	309*	300
TC1092	A	209	206	204	150
TCS056	A	226	224	222	150

*17-V functional test deleted.
This test was destructive for the Al-gate type.

TABLE 4. POST-SCREEN ELECTRICAL TESTS, VENDOR B, TYPE 4007S

Acceptable	309
Noise Immunity	10
Catastrophic Leakage (I_{DSS} >1 mA)	128

Incoming inspection electrical testing and post-screen electrical testing were performed on a Datatron Hustler 44 Test System. A program was created to analyze completely several key test parameters and "datalog" the results for statistical analysis on an IBM-370 system. The complete test program with the pinning configurations used for each test is shown in Table 5.

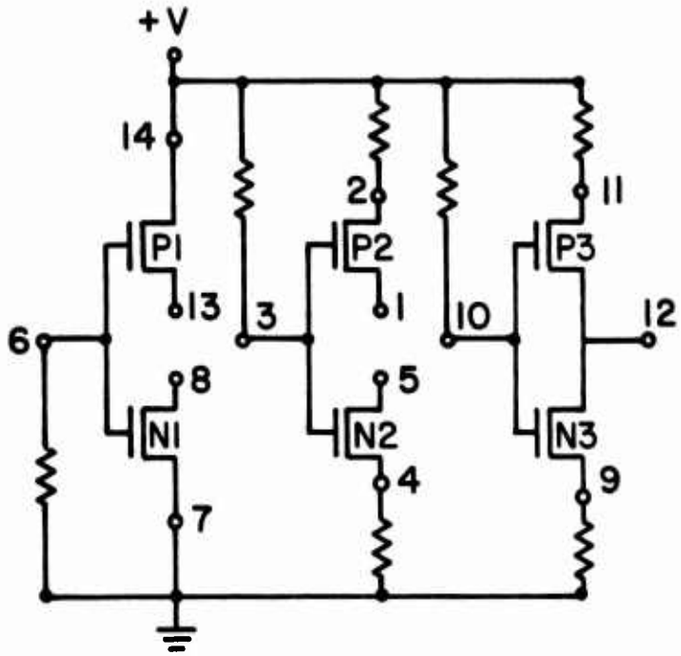
To simplify Datatron programming, the threshold voltage measurement procedure was modified. Normally, threshold voltages are measured by forcing the test current into the source while short-circuiting the gate and drain electrodes. The Datatron test program simply reverses the source and drain for measuring threshold voltages. This mode of testing can cause measurement error if source-drain interchangeability is not possible. For this program, threshold voltages were obtained from "Square Rooter" (see Appendix C) plots on numerous units before and after stress-testing and compared with Datatron readings (for the same currents). In all cases the threshold data obtained from either procedure checked within ±0.1 V. It should also be noted that both the TC1092 and TCS056 input protection networks were not fully characterized by this test program. Specifically, the upper (to V_{DD}) protective network was not tested.

A 168-h bias burn-in at 125°C was performed on all devices as part of the initial screening procedure. The circuit is the standard RCA high-reliability bias-life test configuration established for the bulk COS/MOS CD4007 type. This circuit biases one "p" device and two "n" devices ON with a V_{DD} level of +10 V. Figure 1 is the schematic for the burn-in.

TABLE 5. TCS056 TEST PROGRAM WITH PINNING CONFIGURATION

Test	Symbol	Test Method	Test #	PACKAGE PINS 1	2	3 Inp. 2	4	5	6 Inp. 1	7 V_{SS} (V)	8	9	10 Inp. 3	11	12 Outp. 3	13	14 V_{DD} (V)	Measured Terminal	Min	Max	Units	DATATRON DATA LOG Address	Step
17 V Functional	V_{OL2}	3007.1	1	m	+12	+12	-5	m	-5	-5		-5	-5	+12			+12	(1-5)	-5.0	-4.7	Volts	10	2
	V_{OH1}	3006.1	2		+12	+12	-5		-5	-5	m	-5	-5	+12		m	+12	(8-13)	11.7	12.0	Volts	10	2
	V_{OH3}	3006.1	3		+12	+12	-5		-5	-5		-5	-5	+12	m		+12	12	11.7	12.0	Volts	10	2
	V_{OH2}	3006.1	4	m	+12	-5	-5	m	+12	-5		-5	-5	+12			+12	(1-5)	11.7	12.0	Volts	10	4
	V_{OL1}	3007.1	5		+12	-5	-5		+12	-5	m	-5	-5	+12		m	+12	(8-13)	-5.0	-4.7	Volts	10	4
	V_{OL3}	3007.1	6		+12	-5	-5		-5	-5		-5	+12	+12	m		+12	(12)	-5.0	-4.7	Volts	10	6
10 V Functional	V_{OL2L}	3007.1	7	+1.3mA m	+10	+10	GND	m	GND	GND		GND	GND	+10			+10	(1-5)	0	+.65	Volts	22	2
-1.1mA load on a "1"	V_{OH1L}	3006.1	8		+10	+10	GND		GND	GND	-1.1mA m	GND	GND	+10		m	+10	(8-13)	9.35	10.0	Volts	22	2
+1.3mA load on a "0"	V_{OH3L}	3006.1	9		+10	+10	GND		GND	GND		GND	GND	+10	-1.1mA m		+10	12	9.35	10.0	Volts	22	2
	V_{OH2L}	3006.1	10	-1.1mA m	+10	GND	GND	m	+10	GND		GND	GND	+10			+10	(1-5)	9.35	10.0	Volts	22	4
	V_{OL1L}	3007.1	11		+10	GND	GND		+10	GND	+1.3mA m	GND	GND	+10		m	+10	(8-13)	0	+.65	Volts	22	4
	V_{OL3L}	3007.1	12		+10	GND	GND		GND	GND		GND	+10	+10	+1.3mA m		+10	12	0	+.65	Volts	22	6
10 V Functional	V_{OL2N}	3007.1	13	m	+10	+8	GND	m	+2	GND		GND	+2	+10			+10	(1-5)	0	+.5	Volts	28	2
20% Noise	V_{OH1N}	3006.1	14		+10	+8	GND		+2	GND	m	GND	+2	+10		m	+10	(8-13)	9.5	10.0	Volts	28	2
	V_{OH3N}	3006.1	15		+10	+8	GND		+2	GND		GND	+2	+10	m		+10	12	9.5	10.0	Volts	28	2
	V_{OH2N}	3006.1	16	m	+10	+2	GND	m	+8	GND		GND	+2	+10			+10	1-5	9.5	10.0	Volts	28	4
	V_{OL1N}	3007.1	17		+10	+2	GND		+8	GND	m	GND	+2	+10		m	+10	8-13	0	+.5	Volts	28	4
	V_{OL3N}	3007.1	18		+10	+2	GND		+2	GND		GND	+8	+10	m		+10	12	0	+.5	Volts	28	6
5 V Functional	V_{OL2N}	3007.1	19	m	+5	+4	GND	m	+1	GND		GND	+1	+5			+5	1-5	0	+.2	Volts	38	2
20% Noise	V_{OH1N}	3006.1	20		+5	+4	GND		+1	GND	m	GND	+1	+5		m	+5	8-13	4.8	5.0	Volts	38	2
	V_{OH3N}	3006.1	21		+5	+4	GND		+1	GND		GND	+1	+5	m		+5	12	4.8	5.0	Volts	38	2
	V_{OH2N}	3006.1	22	m	+5	+1	GND	m	+4	GND		GND	+1	+5			+5	1-5	4.8	5.0	Volts	38	4
	V_{OL1N}	3007.1	23		+5	+1	GND		+4	GND	m	GND	+1	+5		m	+5	8-13	0	+.2	Volts	38	4
	V_{OL3N}	3007.1	24		+5	+1	GND		+1	GND		GND	+4	+5	m		+5	12	0	+.2	Volts	38	6
Input Terminal 10 V, 10 μA	I_{IH}	3010.1	25		+10	+10 m	GND		GND	GND		GND	GND	+10			+10	3	0	10	μA	48	2
	I_{IH}	3010.1	26		+10	GND	GND		+10 m	GND		GND	GND	+10			+10	6	0	10	μA	48	4
	I_{IH}	3010.1	27		+10	GND	GND		GND	GND		GND	+10 m	+10			+10	10	0	10	μA	48	6
Leakage 10 V, 10 μA	I_{SS}	3005.1	28		+10	+10	m		+10	m		m	+10	+10			+10	4,7,9	0	10	μA	57	2
	I_{SS}	3005.1	29		+10	GND	m		GND	m		m	GND	+10			+10	4,7,9	0	10	μA	57	4
Output Drive Current N_2	I_{DN}		30	+3 m		+10	GND	+3 m		GND		GND						1-5	–	–	mA	67	2
Output Drive Current P_2	I_{DP}		31	+7 m	+10	GND		+7 m						+10			+10	1-5	–	–	mA	75	2
Threshold N_2	V_T		32	-10μA m		+10	+10	-10μA m		+10		+10						1-5	+7.4	+9.4	Volts	88	2
N_1	V_T		33				+10		+10	+10	-10μA m	+10				-10μA m		8-13	+7.4	+9.4	Volts	95	2
N_3	V_T		34				+10			+10		+10	+10		-10μA m			12	+7.4	+9.4	Volts	102	2
P_2	V_T		35	+10μA m	-10	-10		+10μA m						-10			-10	1-5	-9.4	-7.4	Volts	112	2
P_1	V_T		36		-10				-10		+10μA m			-10		+10μA	-10	8-13	-9.4	-7.4	Volts	119	2
P_3	V_T		37		-10								-10	-10	+10μA m		-10	12	-9.4	-7.4	Volts	126	2

NOTE: PINS 1 + 5, 8 + 13, 2, 11 + 14, 4, 7 + 9 are connected externally



$R = 47{,}000\Omega$

$V_{DD} = +10\,V$

Figure 1. Schematic of burn-in circuit.

III. STRESS TEST PROGRAM

After the screening tests, 600 units (300 from each technology) were tested and data-logged at 25°, +125°, and -55°C on the Datatron test system. The data obtained were used as the "0 hour" base-line comparison with post-stress test data. The arrays were then separated into six subgroups for the stress test program (see Table 6). The stress tests were selected so that failure mechanisms associated with either mechanical or electrical problems would be quickly detected.

A. STATIC BIAS-TEMPERATURE STRESS TEST

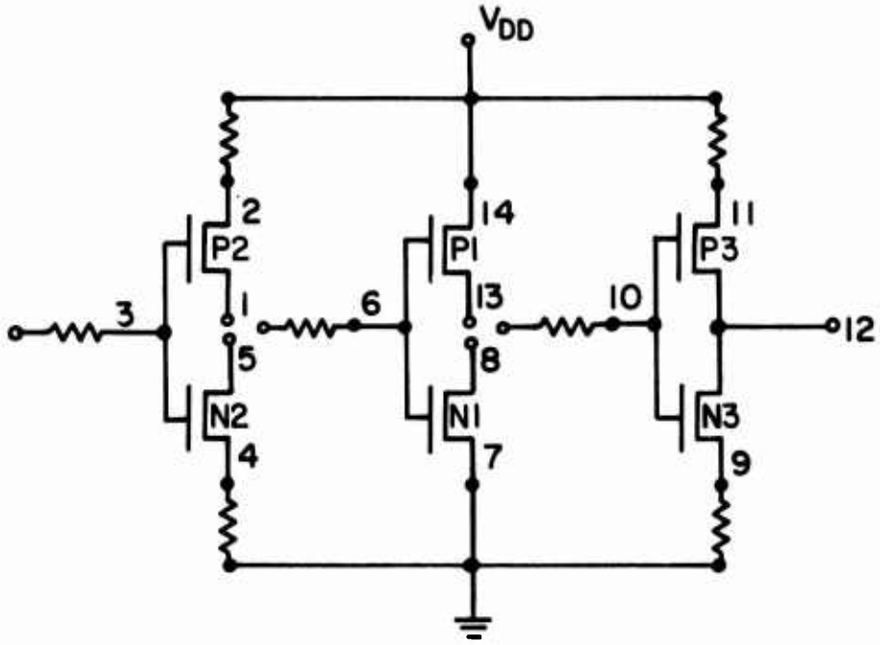
For this test 125 arrays were divided into five temperature subgroups from 150° to 250°C in 25°C increments. Each subgroup remained on test until median failure was achieved, for each of the three circuit types. These median failure points were then used for the generation of an Arrhenius plot for reliability predictions. The test circuit designed for this test is shown in Fig. 2. One-half of the sockets had the gates connected high and one-half low. This allowed for optimum stress to be applied to an equal number of n-and p-transistors. Testing was initiated on the 250° and 225°C subgroups and monitored at 2-h intervals until median failure was reached. These median failure points were then used to project median failure in the lower temperature cells and to calculate the activation energies for the various failure mechanisms.

B. BIAS-POWER TEMPERATURE STRESS TEST

For this test, 125 arrays were subdivided in the same manner as for the static bias-temperature test. The temperature range was 85° to 175°C. Each device was configured as a 3-input NOR gate with a 25-mW output load. This load was selected because it is the typical load specified for bulk COS/MOS at 25°C. The circuit used for this test is shown in Fig. 3. These subgroups were also tested to median failure.

TABLE 6. STRESS PROGRAM SUMMARY

Test	# of Cells	Quant/Cell			Total Qty	Stress Test Levels		
		4007S	TCS056	TC1092		Temperature (°C)	Voltage	Time
Static Bias-Temperature Stress (No Load)	5	12	7	6	125	150 175 200 225 250	V_{DD} = 10 V	To median failure
Bias-Power Temperature Stress (Loaded)	5	12	7	6	125	175 150 125 105 85	V_{DD} = 10 V Load = 2.5 mA per array	To median failure
Temperature Cycling with Intermittent Bias	-	50	25	25	100	-55 to 125	+10 V 15 min on, 15 min off	1000 cycles
Operational Life	-	50	25	25	100	125	V_{DD} = +10 V 50-kHz clock	5000 h
Thermal Shock	-	25	13	12	50	-65 to 150	-	500 cycles
High-Temperature Storage (Stepped)	-	50	25	25	100	150 200 250 300	- - - -	1000 h 1000 h 1000 h 1000 h



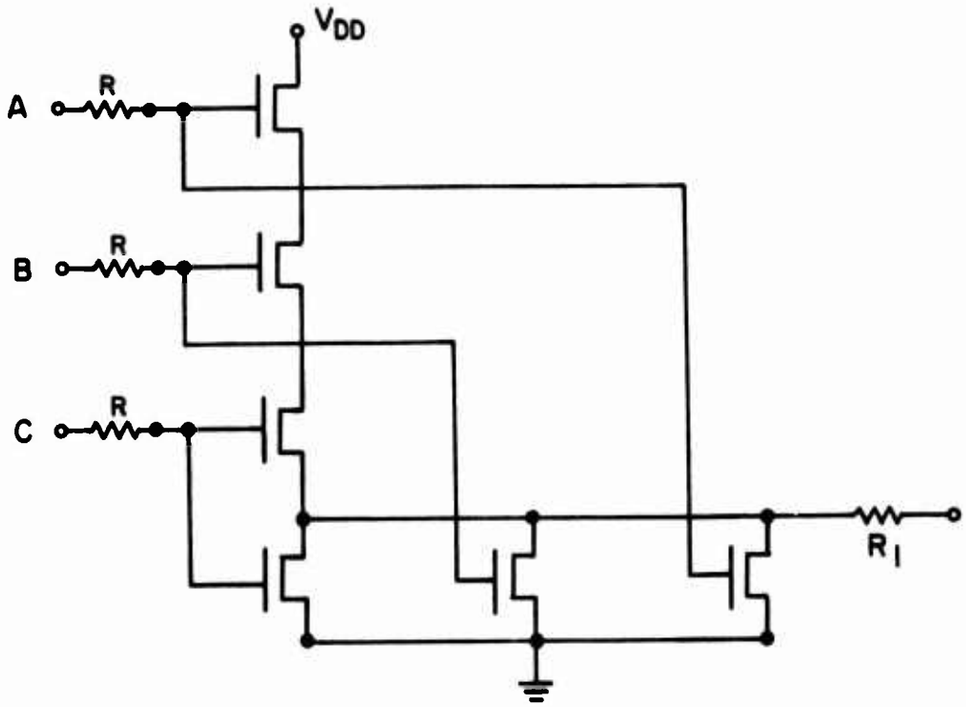
R = 47,000 Ω

V_{DD} = +10 V

Half of the test sockets connect all three inputs to V_{DD} ; the other half connect all the three inputs to GND.

* This is the same circuit used for the temperature cycling with intermittent bias.

Figure 2. Static bias-temperature stress test circuit.



$R = 47{,}000\ \Omega$

$R_1 = 4{,}000\ \Omega$

$V_{DD} = +10\ V$

CURRENT DRAWN PER PACKAGE = 2.5 mA

ONE-HALF OF THE TEST SOCKETS CONNECTED WITH ALL INPUTS AND THE OUTPUT CONNECTED TO V_{DD}, AND ONE-HALF OF THE TEST SOCKETS CONNECTED WITH ALL INPUTS AND THE OUTPUT CONNECTED TO GND.

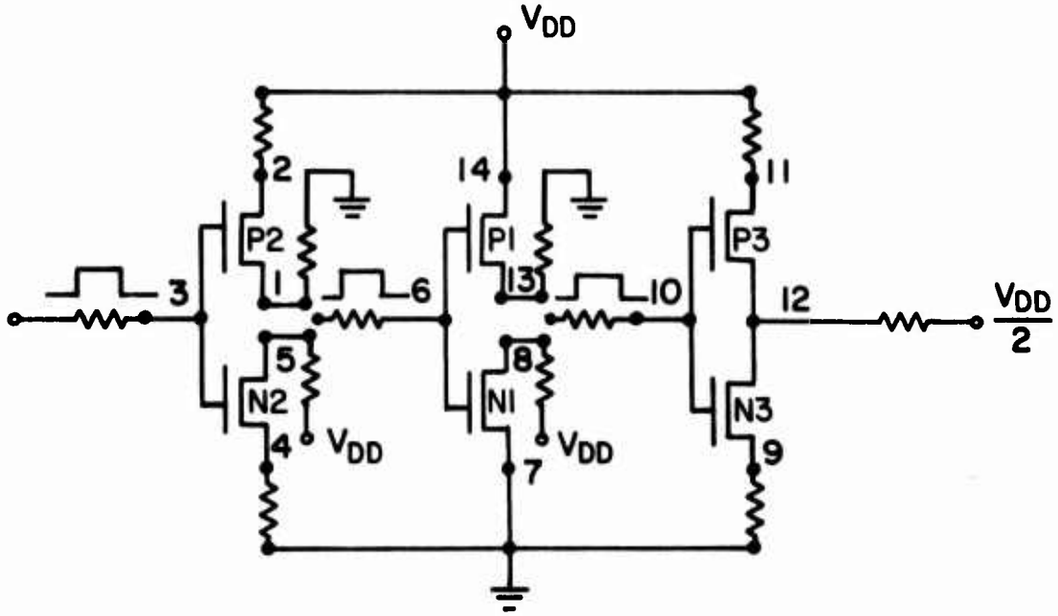
Figure 3. Bias power temperature stress test circuit connected as a 3-input NOR gate.

C. TEMPERATURE CYCLING WITH INTERMITTENT BIAS

For this stress test, 100 units were selected; the circuit was the same as the static bias-temperature test. The units were stressed for 1000 one-hour cycles with the bias on for 15 minutes, then off for 15 minutes at each temperature extreme.

D. OPERATION LIFE

A total of 100 units were subjected to the operational life test at 125°C. The test frequency, as shown in Fig. 4, was 50 kHz with a 50% duty cycle. This test was continued for 5000 h because no failures occurred during the first 2000 h. The results of this test were used to suggest an effective burn-in schedule and an estimation of failure rates.



R = 47,000 Ω

CLOCK PULSE = 10-V amplitude
50-kHz repetition rate
50 % duty cycle

V_{DD} = +10V

Figure 4. Operational life test circuit.

E. THERMAL SHOCK

To obtain thermal shock data 50 units were subjected to the -65° to +150°C (liquid-liquid) stress test. The major purpose of this test was to evaluate failure mechanisms associated with thermal expansion mismatch characteristics. The test was continued to 500 cycles to test device durability and to determine any end-of-life mechanisms.

F. HIGH-TEMPERATURE STORAGE STRESS (STEPPED)

Finally, 100 units were subjected to sequential storage tests of 1000 hours at 150°, 200°, 250° and 300°C. The results of this test were used to suggest an effective storage screen. Package gas analysis results were also closely monitored as the 300°C cell was above the epoxy cure temperature for the Si-gate array types.

IV. TCS010 TEST INSERT CHIP

In addition to the units subjected to the stress test program, 25 TCS010 test-insert chips were subjected to a 125°C operational life test for 3000 hours. These units were from wafers processed concurrently with the TCS056 and TC1092 runs used for this program. This test chip is used as a process control monitor and is on every CMOS/SOS wafer made by Manufacturer A. A photomicrograph of the test chip is shown in Fig. 5. The parameters monitored and the test conditions are given in Table 7. The TCS010 life test bias configuration is shown in Fig. 6.

TABLE 7. TCS010 TESTS

Test	Conditions
n-Channel	
I_{DSS}	V_{DD} = 10 V
V_{th}	I_D = 10, 40, 100 μA
BV_{SD}	Same as I_{DSS} test, I_{DSS} = 10 μA
p-Channel	Identical to n-channel, with voltages reversed
n+ (p-epi) Diffusion	Resistance measurement
p+ (n-epi) Diffusion	Resistance measurement
n+ (Polysilicon)	Resistance measurement
p+ (Polysilicon)	Resistance measurement
Metallization Continuity (100 x R_s 44 metal steps)	Resistance measurement
Contact + Polysilicon (66 contacts + 56 poly)	Resistance measurement
BV, Zener	I_D = 10 μA, 100 μA
Ring Oscillator Frequency, Stage Delay	V = 10 V

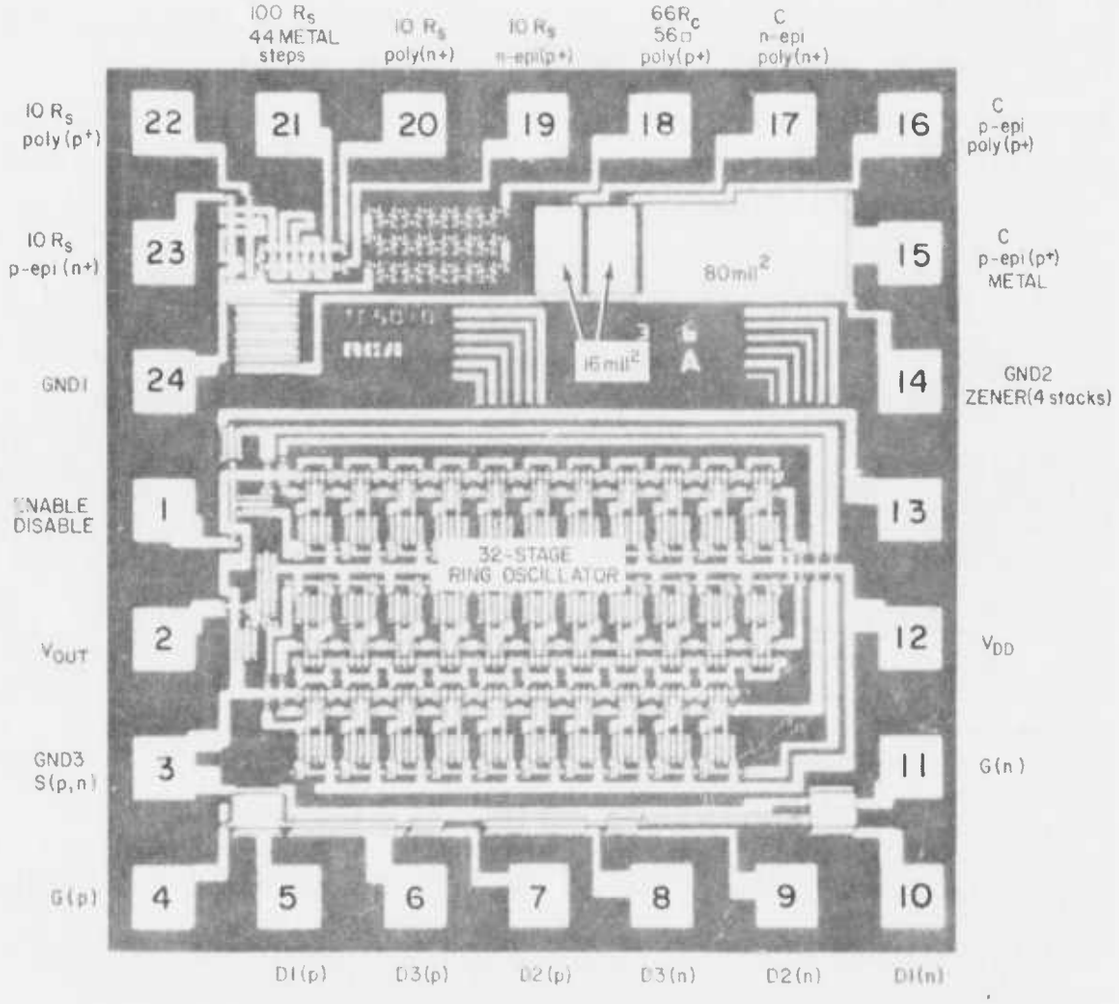


Figure 5. TCS010, test insert chip.

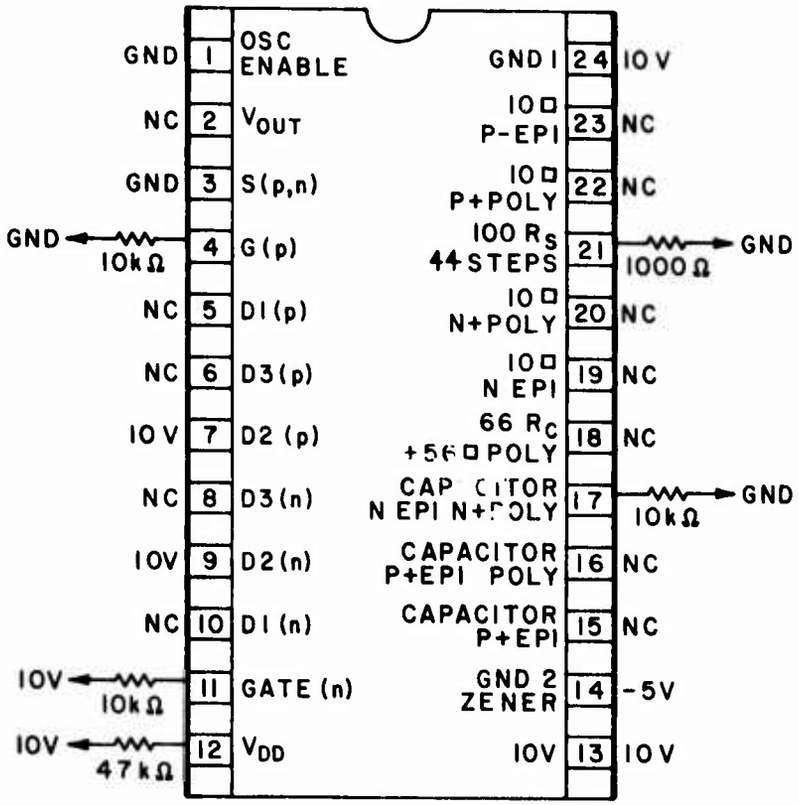


Figure 6. Pin connections for TCS010 life test at 125°C

Several different test conditions were established by the bias configuration shown in Fig. 6, permitting the process monitors (resistors, transistors, capacitors) to be stressed:

(1) The P1 and P3 transistors were subjected to 125°C storage.

(2) The P2 and N2 transistors experienced maximum channel current and oxide stress.

(3) The N1 and N3 transistors experienced just oxide stress (no current flow).

(4) Grounding pin 1 "enabled" the ring oscillator.

(5) 15 V was applied to the 4-stack Zener.

(6) The p-epi and p-epi + poly capacitors were subjected to 125°C storage

(7) 5 V was applied to the n-epi + n+ poly capacitor.

(8) All process monitor resistors (pins 18, 19, 20, 22, 23) subjected to a storage test at 125°C.

(9) 10 mA was drawn through the 44-aluminum-steps path to test metal integrity.

The purpose of this test was to compare the results with those obtained from the operational life test of the TCS056 and TC1092 arrays. There were no device (ring oscillator, transistor) failures or significant parametric drift observed in the 25 TCS010 arrays subjected to the 3000-h 125°C life test.

The process monitors (resistors, capacitors, metallization, and Zener diodes) all remained stable during the 3000-h test. The "p" transistor threshold increase phenomenon observed on the TCS056 and TC1052 Si-gate arrays also existed on the TCS010's but to a lesser degree (Δ's < 0.5 V). BV_{DS} measurements taken on the six test transistors also remained stable (> 20 V), as did the ring oscillator speed (3.3 MHz).

V. DEVICE CHARACTERISTICS

A complete mechanical and electrical device characterization was performed on the arrays. This information created the necessary initial data base for comparison with post-stress test data. Representative samples of each array type were subjected to scanning-electron microscopy, hermeticity test (leak rate), and package dimensioning. Cross-sectional views of a typical complementary pair for each technology are shown in Figs. 7 and 8, with typical thicknesses defined. The process flow-charts for each technology are shown in Figs. 9 and 10. (In Figs. 7 through 10, the silane overcoat is not shown.) Schematic diagrams and photographs of the three circuit types are shown in Figs. 11, 12, and 13.

A. PACKAGING

The package configuration used by both manufacturers was a 14-lead side-brazed ceramic package. Figure 14 is a cross-sectional view representative of the assembly. Both manufacturers used epoxy to attach the chip. Manufacturer A used Dupont 5504 epoxy for this purpose. The cure cycle was 1 h at 160°C plus 1 h at 260°C. Manufacturer B's epoxy type and cure cycle were not determined.

A braze-sealing technique was used by both manufacturers. Manufacturer A used a three-zone belt sealer with the following characteristics:

Pre-seal vacuum bake	=	2 h at 200°C
Nitrogen flow	=	45 ft^3/h
Control temperature	=	320°C
Sealing time	=	8.5 min at $T \geq 280°C$
Belt speed	=	2.5 in./min

Manufacturer B's sealing cycle was not determined.

During the entire stress test program only one mechanical failure was encountered (one Kovar lead was damaged). This was attributed to a handling problem. No other failure mechanisms observed were attributed to a package defect.

EVEL	THICKNESS	LEGEND
SOS epi...	6000 Å	
Channel oxide	1100 Å	
Polycrystalline silicon	5000 Å	
Phosphorus-doped glass	700 Å + 700 Å Boron-doped glass CAP	
Boron-doped glass	700 Å + 5000 Å Undoped CAP	
Aluminum	12,000 Å	

Figure 7. Cross-sectional view of CMOS/SOS Si-gate process (self-aligned).

LEVEL	THICKNESS	LEGEND
SOS epitaxy	6000Å	
Channel oxide	1200Å	
Aluminum	10-13,000Å	

Figure 8. Cross-sectional view of CMOS/SOS Al-gate process.

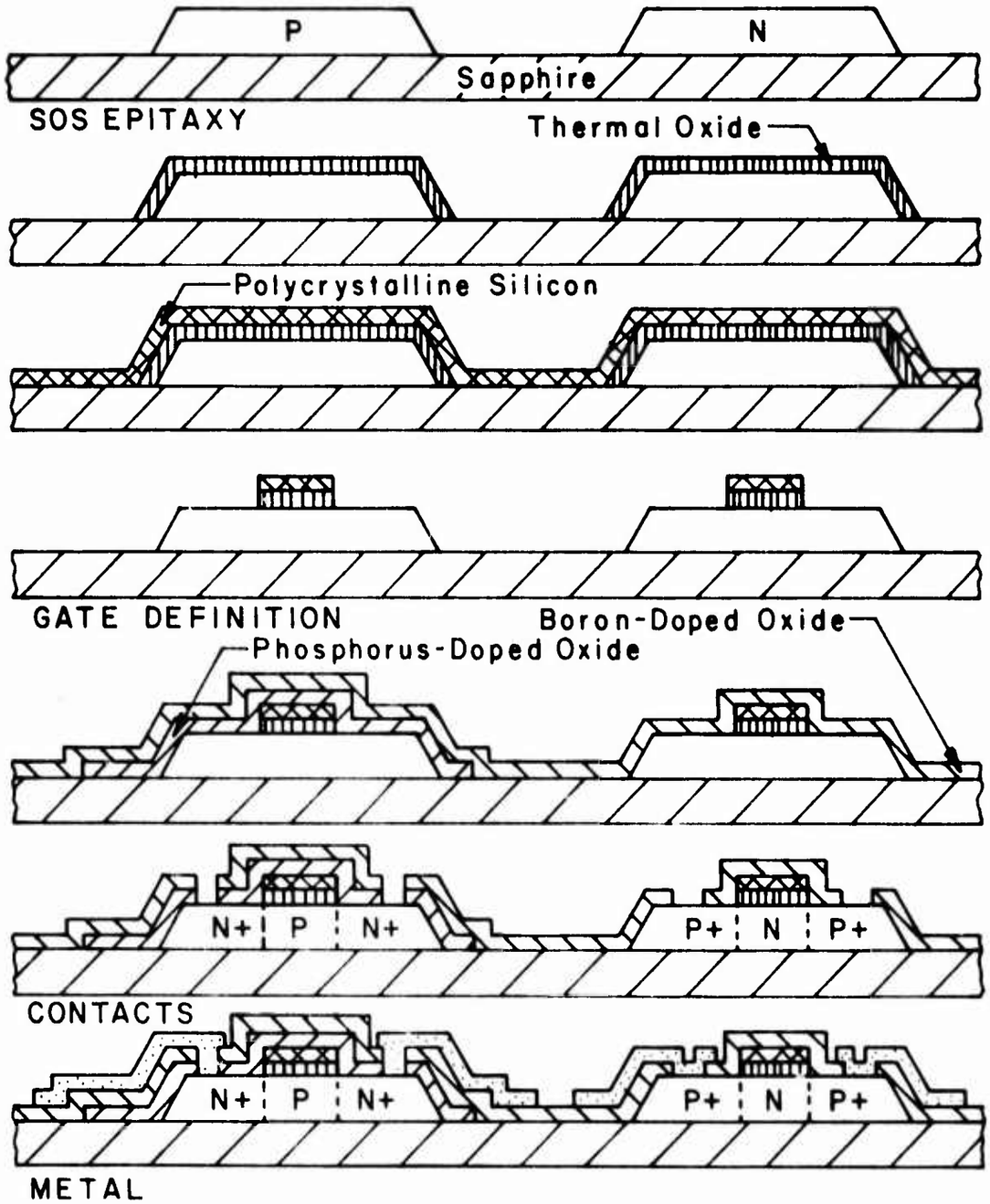
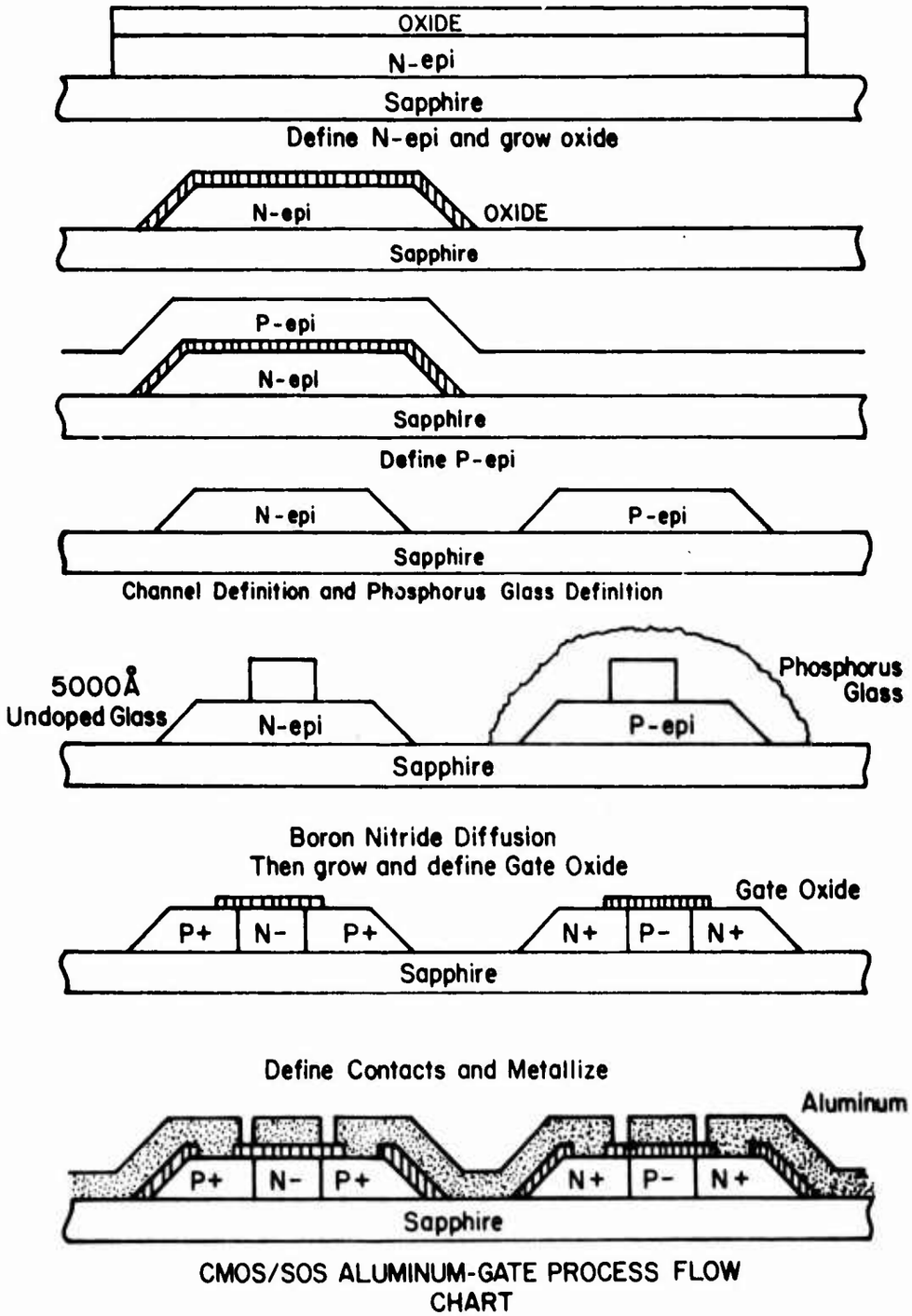


Figure 9. CMOS/SOS Si-gate process flow chart.



CMOS/SOS ALUMINUM-GATE PROCESS FLOW CHART

Figure 10. CMOS/SOS Al-gate process flow chart.

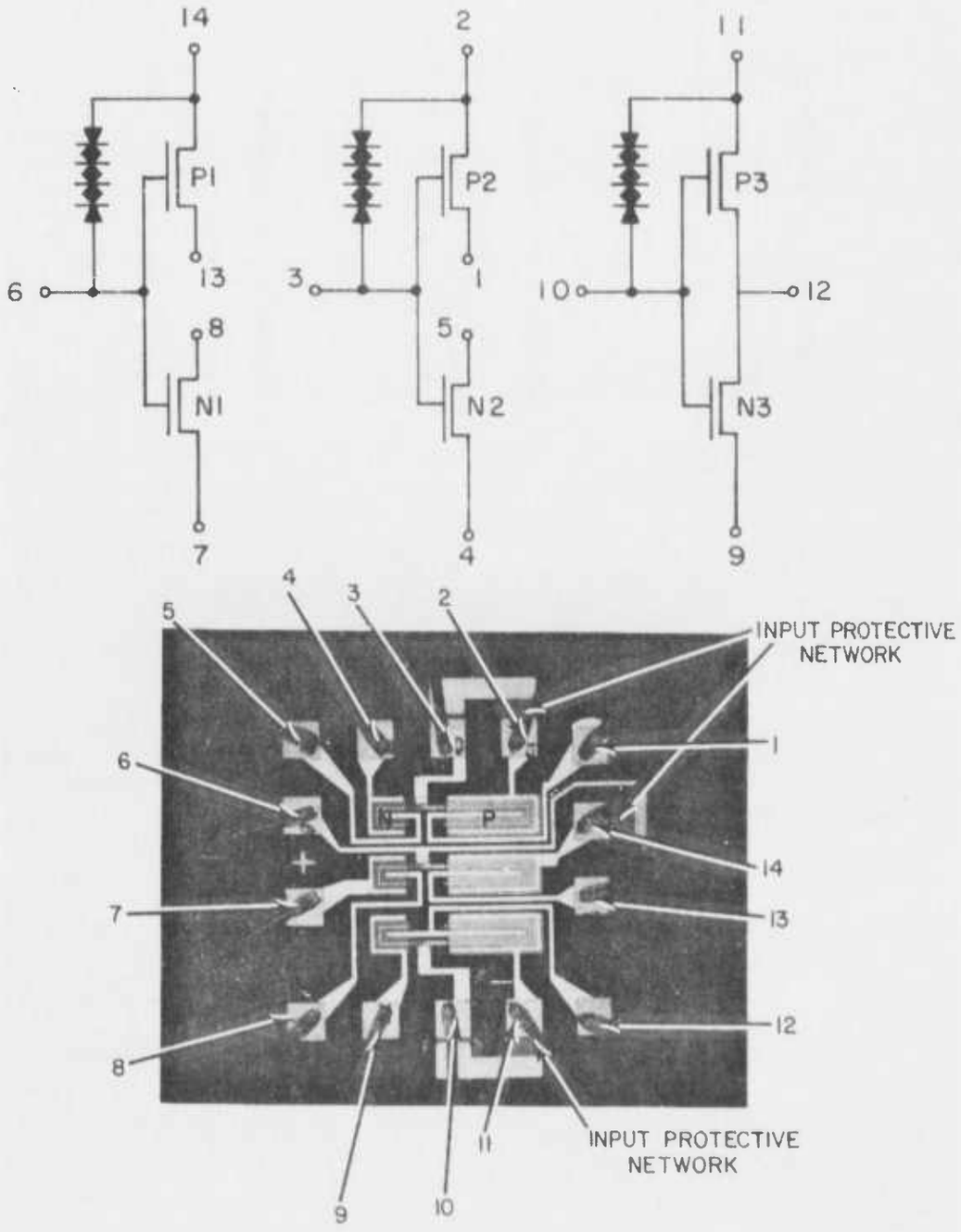


Figure 11. Si-gate CMOS/SOS CD4007 type (TCS056).

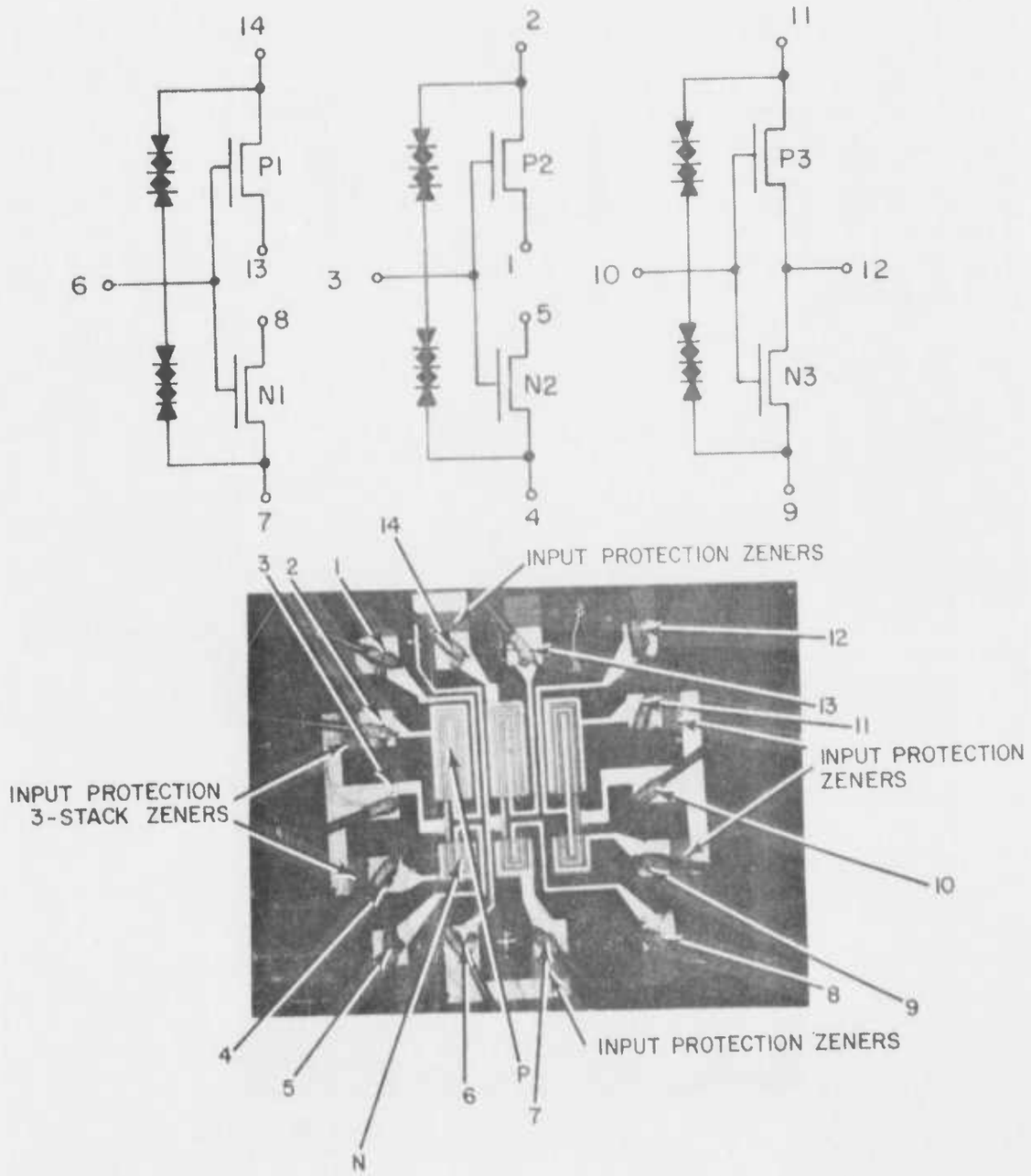


Figure 12. Si-gate CMOS/SOS CD4007 type (TC1092).

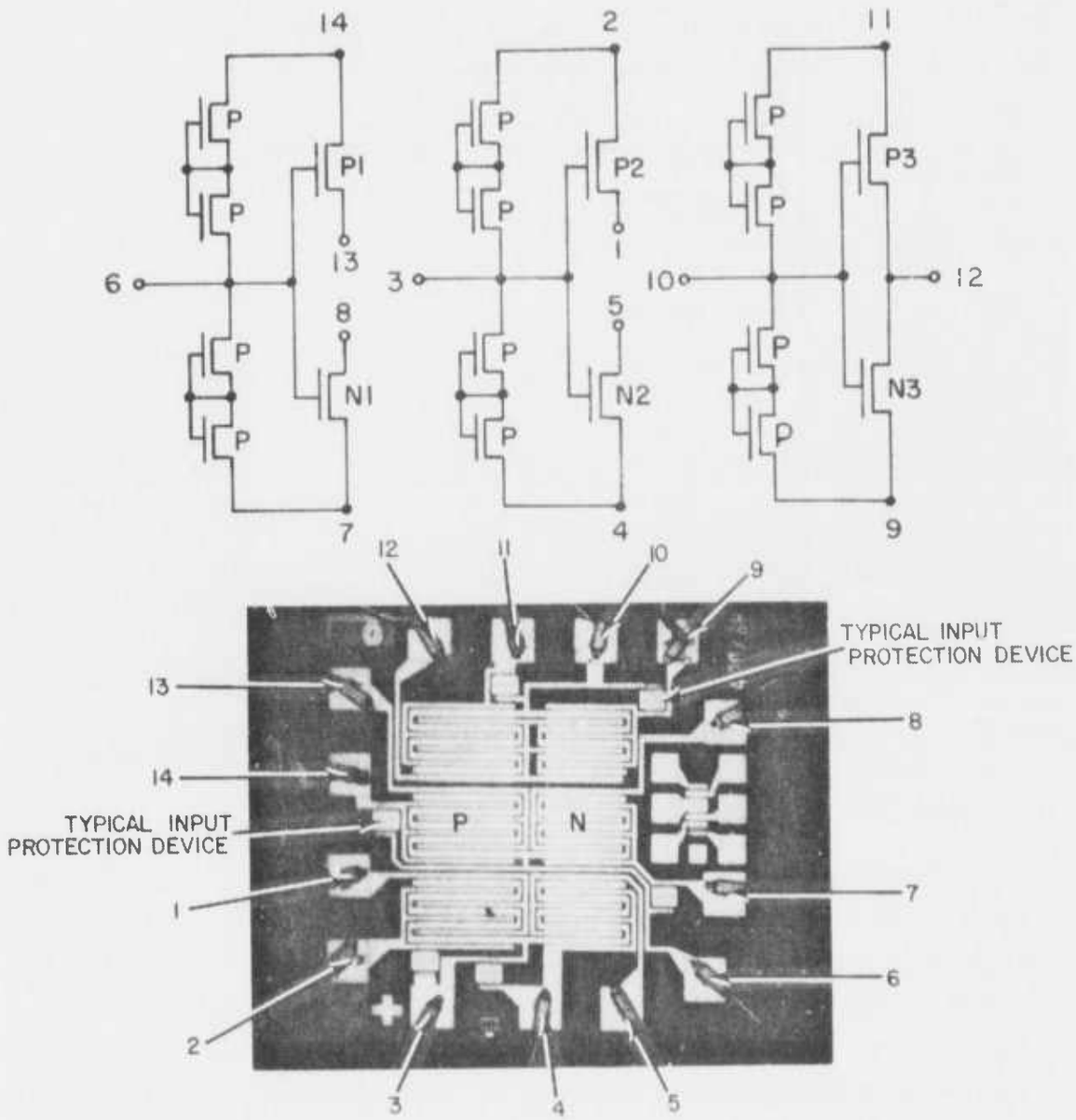


Figure 13. Al-gate CMOS/SOS CD4007 type (4007S).

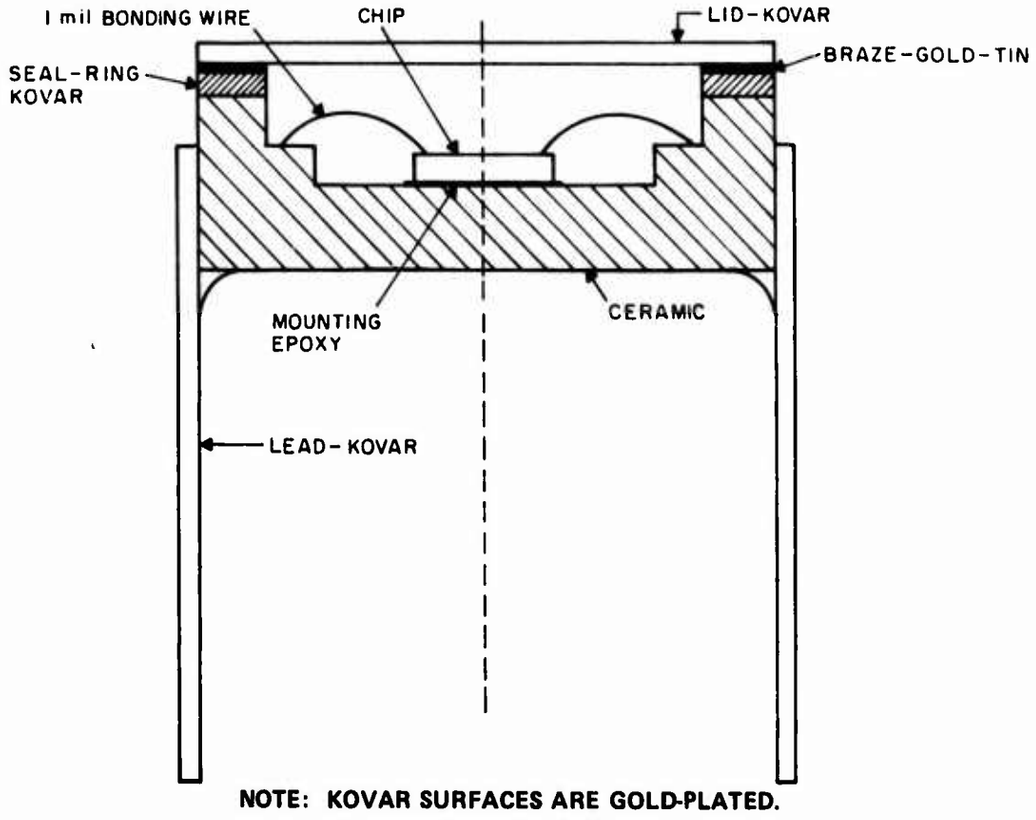


Figure 14. Typical package cross-sectional view.

B. PROTECTIVE NETWORKS

The arrays in the test program had three different input protective circuits. The Al-gate transistor protection network is shown in Fig. 15. The Si-gate configuration for the TC1092 and TCS056 is shown in Fig. 16. The TC1092 Si-gate array uses two 3-stack Zener networks instead of the one 4-stack incorporated in the TSC056 design. The trend plots in the analysis section of this report show that both the 4-stack and transistor configurations have input leakage levels, with the gate biased high, in the nanoampere region, while the 3-stack diode structure had typical input leakage levels around 10 μA. Figure 17 shows photographs of the typical curves obtained on one input protection network for the three array types. The 4007S type exhibited the lowest leakage levels of the three. The difference between the two Si-gate types is the addition of one more Zener (to increase the breakdown level) and the elimination of the stack Zener connected from the input

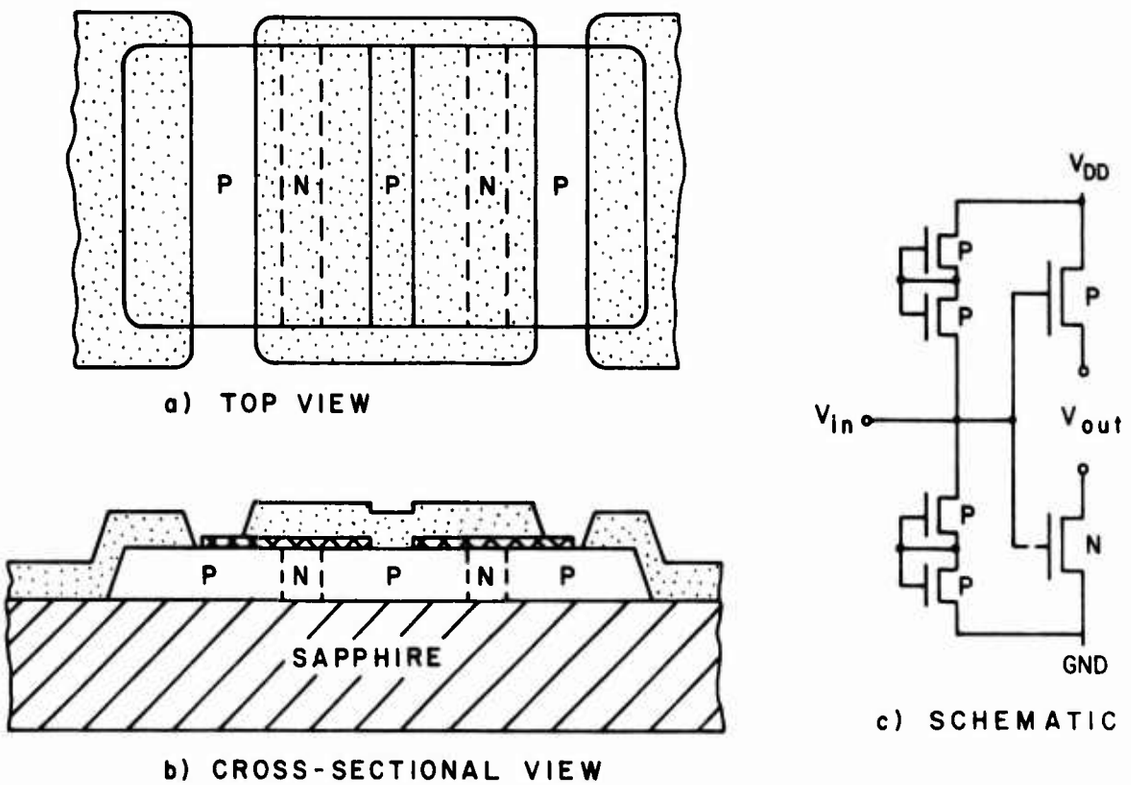


Figure 15. Input protection device (4007S).

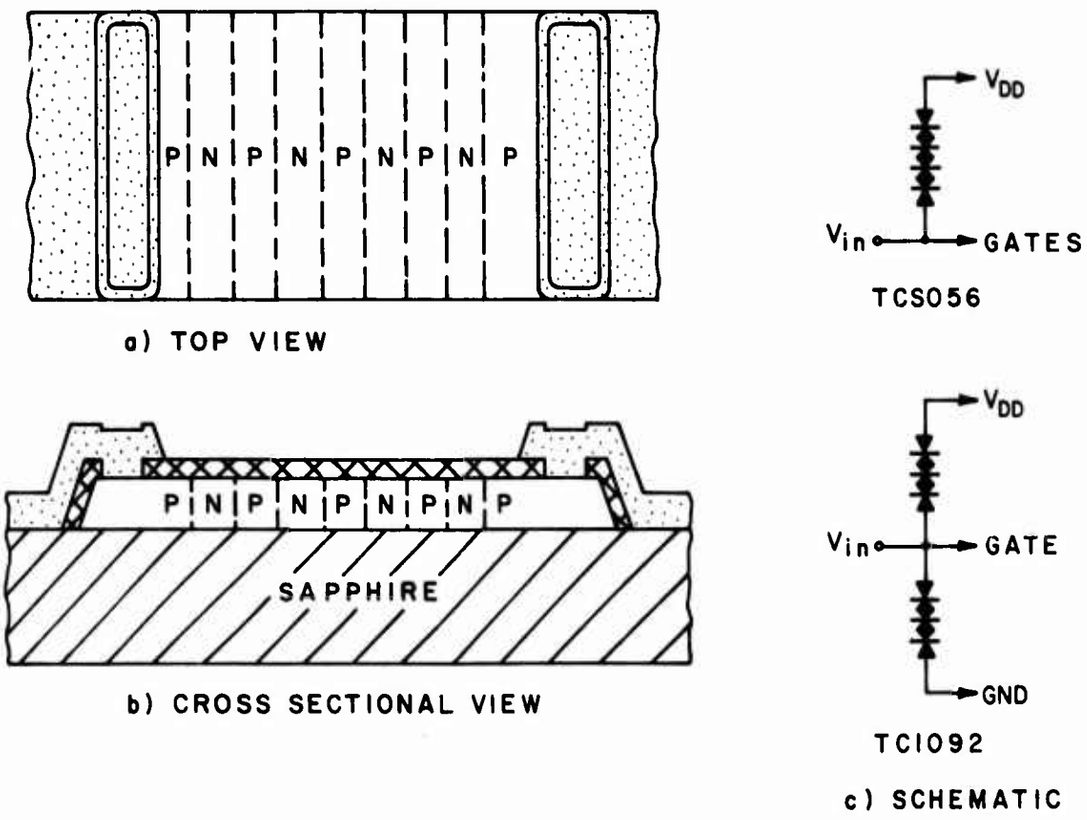
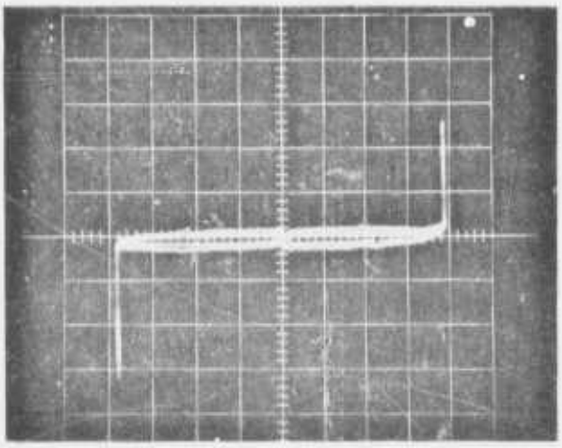
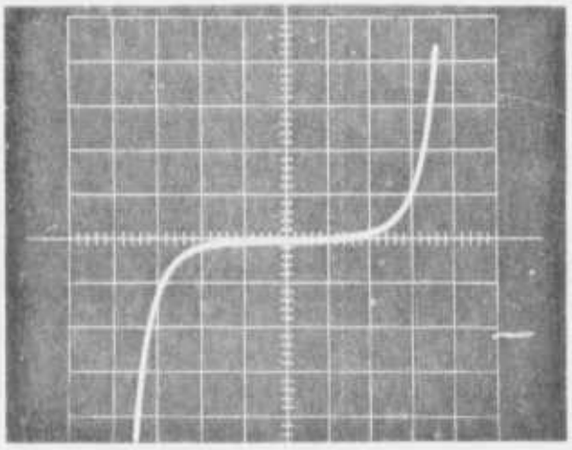


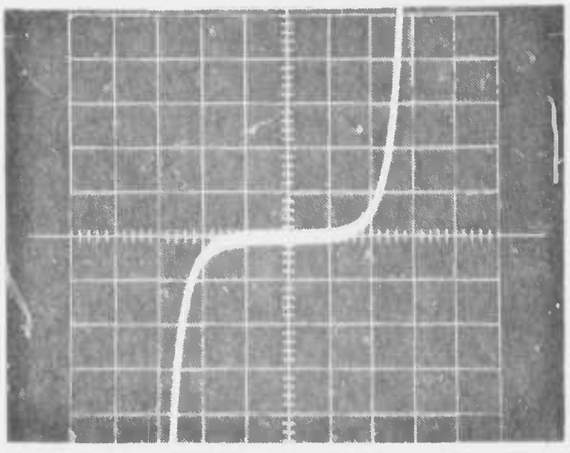
Figure 16. Input protection device (TCS056, TC1092).



TYPE = 4007S
HORIZ. = 5V/div
VERT. = 10μA/div
BREAKDOWN = ≈ 19 V at 10μA
LEAKAGE = < 100 nA at 10V



TYPE = TCS056
HORIZ. = 5 V/div
VERT. = 10μA/div
BREAKDOWN = 14 V at 10μA
LEAKAGE = < 1μA at 10V



TYPE = TC1092
HORIZ. = 5 V/ div
VERT. = 10μA/div
BREAKDOWN = 11 V at 10μA
LEAKAGE = 4 μA at 10V

Figure 17. Typical protective network characteristics at 25°C.

to V_{SS}. The soft knee observed on both Si-gate types can be caused by high dislocation density at the epitaxial Si-sapphire interface or at the surface field-oxide interface.

No failures attributable to static discharge were observed during the stress test program on any of the array types.

VI. TEST RESULTS

A. STATIC BIAS-TEMPERATURE STRESS TEST

Observations were made during the static-bias step-stress tests to determine the median-failure points at each test temperature. For the lower test temperatures (150°, 175°C), time to median failure was not achieved during the program. The Arrhenius plot (Fig. 18) of the median failure points obtained during the static-bias test shows activation energies of 1.1 eV for both Al-gate and TCS056 self-aligned Si-gate failure mechanisms. The projected median life expectancy at 125°C was 72,000 h for the TCS056 Si-gate technology and 7500 h for the 4007S Al-gate technology.

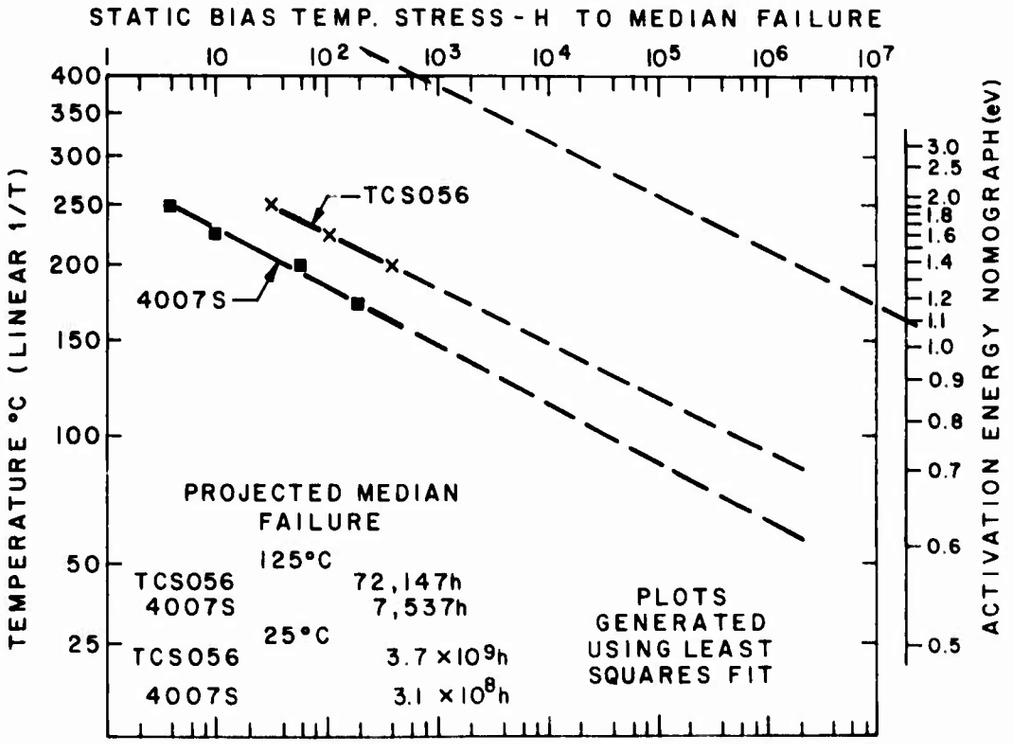


Figure 18. Arrhenius plot, static bias-temperature stress.

The TC1092 Si-gate arrays had a lower median failure time than the TCS056 arrays during the static-bias stress test. Both Si-gate types had identical processing. The higher failure rate of the TC1092 arrays was attributed to the leakage current through the protective networks at the

200° to 250°C test temperatures, causing the gate of the P3 transistor (pin 10) to be positively biased with respect to the p source (pin 11) on units whose inputs were biased high. Units with inputs biased low had the expected p transistor stress. Both conditions produced p transistor threshold shifts.

Figure 19 shows the 15% and 50% failure points observed on the TC1092 cells for the static-bias test. It shows two parallel sets of data both having ≈1.1-eV activation energies for the 15% data. The plot shows the reduction in time to the 15% failure point at temperatures above 200°C, yet the activation energy remained constant. These results are further confirmed by the fact that at the 125°C operational life test temperature both the TC1092 and TCS056 types had similar test results.

The 50% data shows the effect of additional time at elevated temperature. Since inverter three for each array exhibited different leakage and bias characteristics (typically 1.0 V at 200°C, 1.6 V at 225°C, and 2.2 V at 250°C), the inconsistent bias conditions for each cell did not permit reliability predictions for the silicon gate TC1092 to be generated.

The point that should be made is that at test temperatures in excess of 200°C, one must be extremely careful that the bias levels on the devices are what they were originally designed to be.

B. BIAS-POWER TEMPERATURE STRESS TEST

The results of the bias-power step-stress tests for the Al-gate array show the median failure to be 168 h at 125°C. The projected median failure time for the TCS056 Si-gate was 70,000 h, which was determined by taking the 1.1-eV activation energy result from the static-bias test and applying it to the 2,168-h median failure point obtained in the 175°C cell.

C. OPERATIONAL LIFE TEST AT 125°C

The failures resulting from the 50-kHz operational life-testing at 125°C exhibited characteristics similar to those observed during the static-bias and bias-power stress tests. However, the median failure time of 4000 h for the life test is lower for the Al-gate devices than that predicted by the static stresses. The Si-gate devices had no failures prior to the 3000-h test point, and 8% failed during the next 2000h. The reliability of the

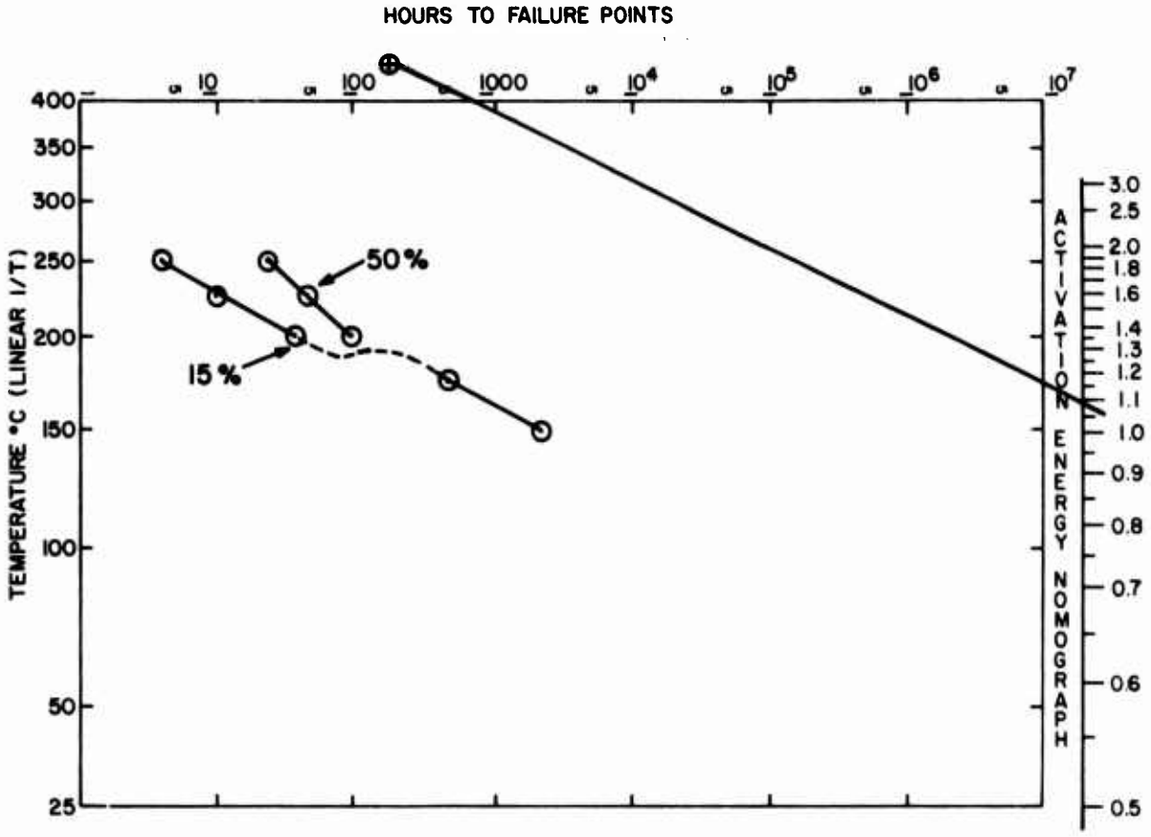


Figure 19. Si-gate TC1092 15% and 50% failure points.

TC1092 in this test is considerably greater than that projected from the static-bias stress test. At the 125°C test temperature the differences in the protective network designs of the two Si-gate array types had no effect on the device reliability. The Weibull Probability Chart shown in Fig. 20 plots the results obtained for this test. Since no failures occurred during the initial 2000h of test, the 168-h bias burn-in performed during the screening procedure appears to be an effective screen for eliminating "early life" failures.

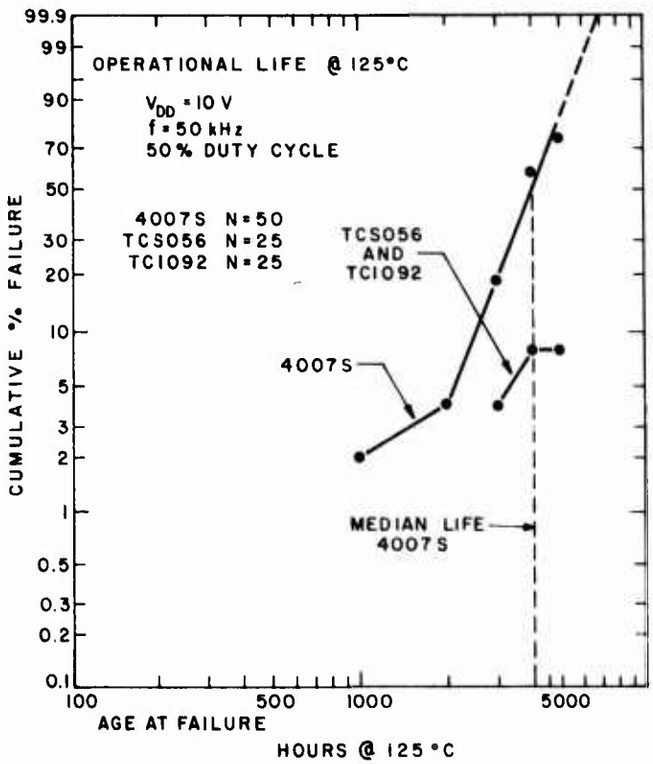


Figure 20. Weibull Probability Chart plot of operational life for 4007S, TCS056, and TC1092.

D. HIGH-TEMPERATURE STORAGE STRESS

The results of the high-temperature storage test (50 units from each technology, sequentially subjected to 1000 h at each of four temperatures: 150°, 200°, 250°, and 300°C) indicate that this stress is ineffective as a screen for eliminating potential early-life failures. However, as the test temperature was increased, the edge-leakage failure rate for the Al-gate

arrays was greatly accelerated. No failures occurred below 250°C for the Al-gate or the Si-gate devices. All but one of the Si-gate failures noted at 300°C were caused by a failure mechanism (e.g., depletion mode operation of the N-transistor) different from that associated with the previous stresses. Gas analysis of the Si-gate failures indicated an increase in H_2, CO_2, and moisture constituents that were attributable to additional curing of the chip-mounting epoxy. The 300°C storage temperature exceeded the curing temperature of 260°C used for the chip-mounting operation of the Si-gate devices. Figure 21 is a Weibull Probability Chart showing these test results.

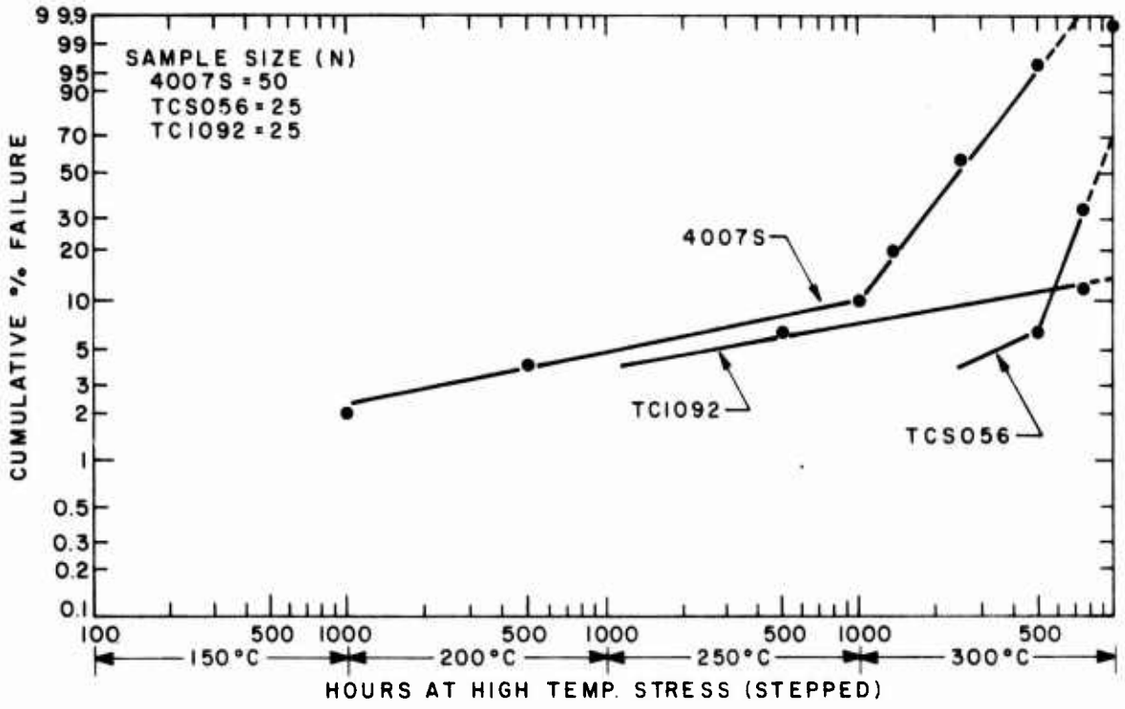


Figure 21. Weibull Probability Chart plot of high-temperature storage stress (stepped).

E. THERMAL SHOCK AND TEMPERATURE CYCLING WITH INTERMITTENT BIAS

All failures encountered during the temperature cycling stress test occurred during the first 50 of the total 1000 cycles. All failures were catastrophic in nature and were the result of process-related defects (e.g.,

oxide pinholes, epitaxial silicon defects). The 500-cycle thermal shock test had two process-related failures in the initial 10 cycles (e.g., oxide pinholes, metal discontinuity) and no other failures to 300 cycles. Beyond 300 cycles seven edge-related gate-to-source breakdowns were observed, indicating an "end-of-life" characteristic related to excessive thermal-mechanical stressing of the Si-sapphire interface.

Detailed results for the six stress tests are shown in Tables 8 to 10.

TABLE 8. STATIC BIAS-TEMPERATURE STRESS

CELL TEMP	STATUS	QUANTITY	RESULTS	TEST CONDITIONS	MEDIAN FAILURE
250°C	Completed	12 4007S	9 Depletion mode VthN ≤ 0 V 7 Failed @ 4 h 1 Failed @ 6 h 1 Failed @ 7 h	V_{DD} = +10 V 5 arrays Vgs = + 10 V 4 arrays Vgs = 0 V	4 h
	Completed	6 TC1092	3 VthP < -2.6 V 1 Failed @ 4 h 1 Failed @ 4 h 1 Failed @ 26 h	V_{DD} = +10 V Vgs = 0 V Vgs = 10 V Vgs = 10 V	26 h
	Completed	7 TCS056	3 VthP < -2.6 V 1 Failed @ 4 h 1 Failed @ 6 h 1 Failed @ 30 h	V_{DD} = +10 V Vgs = 0 V	30 h
225°C	Completed	12 4007S	7 Depletion mode VthN ≤ 0 V 3 Failed @ 5 h 4 Failed @ 10 h	V_{DD} = +10 V 6 arrays Vgs = +10 V 1 array Vgs = 0 V	10 h
	Completed	6 TC1092	3 VthP < -2.6V 1 Failed @ 10 h 2 Failed @ 65 h	V_{DD} = +10 V Vgs = 10 V Vgs = 0 V	65 h
	Completed	7 TCS056	4 VthP < -2.6 V all at 105 h	V_{DD} = +10 V Vgs = 0 V	105 h
200°C	Completed	12 4007S	7 Depletion mode VthN ≤ 0 V 4 Failed @ 32 h 3 Failed @ 60 h	V_{DD} = +10 V 6 arrays Vgs = +10 V 1 array Vgs = 0 V	60 h
	Completed	6 TC1092	3 VthP < -2.6 V 1 Failed @ 40 h 2 Failed @ 100 h	V_{DD} = +10 V Vgs = 10 V Vgs = 0 V	100 h
	Completed	7 TCS056	4 VthP < -2.6 V 1 Failed @ 150 h 3 Failed @ 400 h	V_{DD} = +10 V Vgs = 0 V	400 h
175°C	Completed	12 4007S	6 Depletion mode VthN ≤ 0 V 4 Failed @ 168 h 2 Failed @ 200 h	V_{DD} = +10 V Vgs = +10 V	200 h
	Terminated @ 1000 h	6 TC1092	1 VthP < -2.6V Failed @ 500 h	V_{DD} = +10 V Vgs = 0 V	
	Terminated @ 1000 h	7 TCS056	0 Failures		
150°C	Completed	12 4007S	6 Depletion mode VthN ≤ 0 V All 6 failed @ 168 h	V_{DD} = +10 V Vgs = +10 V	168 h
	Terminated @ 2250 h	6 TC1092	1 VthP < -2.6 V 1 Input Terminal Leakage > 10 μA Both failed @ 2250 h	V_{DD} = +10 V Vgs = 0 V	
	Terminated @ 2250 h	7 TCS056	0 Failures		

TABLE 9. BIAS POWER TEMPERATURE STRESS

CELL TEMP	STATUS	QUANTITY	RESULTS	TEST CONDITIONS	MEDIAN FAILURE
175°C	Completed	12 4007S	6 Depletion mode VthN $\leq$ 0 V 3 Failed @ 35 h 3 Failed @ 100 h	V_{DD} = +10 V Inputs - high	100 h
	Completed	6 TC1092	3 VthP < -2.6 V 1 Failed @ 200 h 2 Failed @ 300 h	V_{DD} = +10 V Inputs - low	300 h
	Completed	7 TCS056	4 VthP < -2.6 V 1 Failed @ 1250 h 3 Failed @ 2168	V_{DD} = +10 V Inputs - low	2168 h
150°C	Completed	12 4007S	6 Depletion mode VthN $\leq$ 0 V 3 Failed @ 75 h 3 Failed @ 125 h	V_{DD} = +10 V Inputs - high	125 h
	Terminated @ 1000 h	6 TC1092	1 VthP < -2.6 V @ 750 h	V_{DD} = +10 V	
	Terminated @ 1000 h	7 TCS056	No failures		
125°C	Completed	12 4007S	6 Depletion mode VthN $\leq$ 0 V All 6 failures @ 168 h	V_{DD} = +10 V Inputs - high	168 h
	Terminated @ 2250 h	6 TC1092 and 7 TCS056	No failures		
105°C	Terminated @ 2000 h All types	12 4007S	1 Catastrophic failure at 750 h N_1 transistor-gate to source breakdown	V_{DD} = +10 V Inputs - high	
		6 TC1092	1 Leakage failure at 336 h	V_{DD} = +10 V Inputs - high	
		7 TCS056	No failures		
85°C	Terminated @ 2000 h All types	12 4007S	1 Failure @ 168 h Input 6 "P" device failure	V_{DD} = +10 V Inputs - high	
		6 TC1092	1 Failure VthP < -2.6 V @ 1000 h	V_{DD} = +10 V Inputs - low	
		7 TCS056	1 Failure - high leakage current N3 transistor @ 336 h	V_{DD} = +10 V Inputs - high	

TABLE 10. TEMPERATURE CYCLING WITH INTERMITTENT BIAS, OPERATIONAL LIFE, THERMAL SHOCK, AND HIGH-TEMPERATURE STORAGE STRESS TESTS

A. TEMPERATURE CYCLING WITH INTERMITTENT BIAS

Status	Quantity	Results	Test Conditions
4007S completed 1000 cycles	50 - 4007S	After 50 cycles the following 4 failures were noted: 1 mech. - pin 8 broken 3 elec. a) N1 + P1 transistors gate-to-source breakdown b) P1 gate-to-source breakdown *c) N1 gate-to-source breakdown	V_{DD} = + 10 V 3 failures - V_{gs} = 0 V 1 failure - V_{gs} = 10 V*
TC1092 & TCS056 completed 1000 cycles	25 - TC1092 25 - TCS056	No TCS056 failures 3 TC1092 elect. failures (2 at 10 cycles) (1 at 50 cycles) a) P1 transistor gate-to-drain breakdown b) P1 transistor 100-μA leakage c) N1 transistor gate-to-source breakdown	V_{DD} = + 10 V 3 failures - V_{gs} = 0 V

B. OPERATIONAL LIFE

5000 hours completed	50 - 4007S 25 - TC1092 25 - TCS056	1 TCS056 at 3000 h N1 - P1 inverter failure (gate to source leakage) 1 TCS056 at 4000 h N1 transistor, high current failure 1 TC1092 at 3000 h V_{th} "P" $\leq$ -2.6 V 1 TC1092 at 4000 h V_{th} "P" $\leq$ -2.6 V 38 4007S at 4000 h 1 N1 - P1 inverter failure (gate to-source-breakdown) N1 transistor 8 units with $V_{thn} \leq 0$ V 29 units with edge transistor leakage > 50 μA 8 4007S at 5000 h edge transistor leakage	V_{DD} = +10 V T = 125°C f = 50 kHz

C. THERMAL SHOCK

500 cycles completed	25 - 4007S 12 - TC1092 13 - TCS056	1 TC1092 failure at 10 cycles P3 transistor, open-drain-metal over epi-island 1 4007S failure at 10 cycles, N1 transistor gate-to-source breakdown (Non edge-related) 4 TCS056 failures 1 TC1092 failure 1 4007S failure All edge-related gate-to-source breakdown, at 300 cycles 1 TCS056 edge-related gate-to-source breakdown at 400 cycles	-65°C to +150°C liquid to liquid

D. HIGH-TEMPERATURE STORAGE STRESS (STEPPED)

1000 h at 150°C completed	50 - 4007S 25 - TC1092 25 - TCS056	No failures	All parts subjected sequentially to 150°, 200°, 250°, and 300°C storage tests, no bias, all terminals floating.
1000 h at 200°C completed	same	No failures	
1000 h at 250°C completed	same	2 TC1092 (1 each type failed after 24 h (gate-to-source breakdown) (1 edge related) 2 4007S (and 1 each again after 500 h (gate-to-source breakdown) (1 edge related).	
1000 h at 300°C completed	same	8 TCS056 (Depletion mode N transistors 1 TC1092 ($V_{thn} \leq 0$ V) 26 4007S Edge transistor leakage > 50 μA	

VII. PACKAGE GAS ANALYSIS

Particular attention was paid to the evaluation of the effects of the high-temperature stress testing on the ambient gas in the package cavity. Previous experience after normal 1000-h, 125°C, bias and operating life tests indicated no significant changes in the normal (N_2, trace O_2, trace CO_2) gas content. However, units subjected to the high-temperature storage tests during this program were exposed to temperatures up to 300°C for periods up to 1000 h. It should be noted that this temperature exceeds the epoxy cure (260°C) and the braze eutectic (285°C) temperatures used in the chip-mounting and package sealing operations. (The 260°C cure temperature is for Vendor A parts.)

Table 11 summarizes the data obtained initially and on post-stress test measurements. Measurements on the Si-gate arrays subjected to high-temperature storage (300°C) indicate a typical decrease in the N_2 level of 10% with substantial increase in the H_2, CO_2, and O_2 levels. These changes are attributed to additional curing of the epoxy used for chip mounting and the melting (and recrystallizing) of the braze material.

TABLE 11. PRE- AND POST-STRESS TEST - GAS ANALYSIS RESULTS

Device Type	Unit #	Stress Test	ANALYSIS														
			H_2 (%)	He	H_2O	N_2 (%)	O_2	Ar	CO_2	CH_4	C_2H_6	C_3H_6 (%)	Benzene (%)	Toluene (%)	Acetone	Acetylene	Fluorocarbons
TCS056	159	Pre-stress	0.53	-	-	98.3	0.13%	780ppm	0.68	-	-	-	-	-	0.26%	-	940ppm
	214	Pre-stress	0.96	-	-	97.5	810ppm	400ppm	0.72	0.15%	-	0.23	-	-	0.23%	-	950ppm
	9	Temp Cycling	0.95	-	-	92.1	0.10%	-	2.5	1.0%	-	0.55	0.60	-	0.75%	0.20%	-
	10	Temp Cycling	0.96	-	-	90.3	0.12%	-	4.7	1.5%	-	0.73	0.65	0.16%	0.66%	0.17%	-
	6	High-Temp Stor.	-	-	1000ppm	79.1	12.3%	.93%	7.6	-	-	-	-	-	-	-	-
	24	High-Temp Stor.	9.0	-	-	90.0	0.11%	260ppm	0.45	660ppm	-	0.14	-	-	0.13%	680ppm	-
	27	Thermal Shock	1.9	-	-	96.7	860ppm	280ppm	0.71	400ppm	-	0.20	-	-	0.22%	800ppm	760ppm
	36	Thermal Shock	1.7	-	-	97.4	0.14%	460ppm	0.37	640ppm	-	0.12	-	-	0.12%	-	-
	43	Operational Life	2.5	-	-	99.9	0.11%	140ppm	0.68	0.15%	-	-	-	-	0.26%	430ppm	900ppm
	58	Operational Life	-	Damaged during gas analysis test													
TC1092	194	Pre-stress	0.98	-	-	96.4	0.11%	560ppm	1.13	0.23%	-	0.50%	-	-	0.31%	-	0.22%
	203	Pre-stress	0.99	-	-	98.3	770ppm	280ppm	0.23	560ppm	-	0.14	-	-	770ppm	-	490ppm
	91	Temp Cycling	0.99	-	0.83%	89.1	0.10%	-	4.8	1.5%	0.71%	1.1	-	0.09%	0.59%	0.18%	-
	106	Temp Cycling	1.5	-	1.1%	87.1	870ppm	-	5.6	1.64%	0.85%	1.3	-	-	0.78%	0.18%	-
	15	High-Temp Stor.	2.0	-	-	87.8	710ppm	58ppm	6.2	1.6%	0.20%	780ppm	0.81	-	0.76%	0.50%	-
	46	High-Temp Stor.	1.5	-	-	97.0	830ppm	100ppm	0.69	-	-	0.22	-	320ppm	310ppm	450ppm	-
	52	Thermal Shock	1.0	-	-	98.0	0.10%	300ppm	0.37	750ppm	-	0.19	-	-	0.12%	-	790ppm
	61	Thermal Shock	0.90	-	-	98.3	820ppm	280ppm	0.32	700ppm	-	0.12	-	-	990ppm	-	450ppm
	68	Operational Life	2.0	-	-	96.2	360ppm	-	0.68	0.16%	-	0.33	-	-	0.33%	440ppm	0.13%
	83	Operational Life	1.7	-	-	97.0	460ppm	660ppm	0.55	0.11%	-	800ppm	-	-	0.27%	330ppm	0.11%
4007S	694	Pre-stress	7.17	-	-	90.76	0.12%	610ppm	1.0	900ppm	-	0.30	-	750ppm	0.25%	-	0.15%
	673	Pre-stress	5.0	-	-	93.7	-	0.24%	0.50	140ppm	-	240ppm	-	-	0.31%	-	0.17%
	18	Temp Cycling	1.34	-	0.11%	84.51	0.14%	0.18%	8.8	2.0%	-	0.88	0.92	0.34%	0.79%	-	-
	59	Temp Cycling	1.2	-	-	89.7	810ppm	-	5.4	1.3%	-	0.63	0.66	-	0.81%	0.19%	-
	117	High-Temp Stor.	1.6	-	-	97.3	420ppm	150ppm	0.54	660ppm	-	0.17	-	-	0.14%	-	-
	195	High-Temp Stor.	1.4	-	-	97.2	820ppm	140ppm	0.55	660ppm	-	0.25	0.11	-	0.30%	470ppm	-
	222	Thermal Shock	1.4	-	-	96.4	0.20%	390ppm	0.30	500ppm	-	720ppm	-	-	940ppm	-	-
	267	Thermal Shock	5.0	-	-	94.6	910ppm	460ppm	0.48	600ppm	-	840ppm	-	-	0.11%	490ppm	-
	385	Operational Life	6.0	-	-	93.1	700ppm	320ppm	0.45	870ppm	-	0.10%	-	-	0.11%	550ppm	-
	413	Operational Life	Non-Hermetic														

VIII. SCANNING ELECTRON MICROSCOPE INSPECTION

Initial scanning electron microscope (SEM) photographs were taken on typical units of each device type. The SEM was employed primarily for observing changes in metallization continuity that could occur due to the thermal and intermittent power stress tests. The control of metallization coverage over the polysilicon, epitaxial Si island, and contact edges is difficult because of the different etching rates of the polysilicon gates and the epitaxial Si islands. These photographs (Figs. 22, 23, and 24) are typical photographs of metallization coverage prior to the start of the stress test program. The silane overcoat was removed prior to SEM analysis. The pictures show that the TCS056 type exhibited good metallization coverage over the epitaxial islands, polysilicon, and contacts. Both the Si-gate TC1092 and the Al-gate 4007S types show a sharp slope to the epi-island, causing a thinning down of the metallization at those points in the circuit. Strict attention was paid to the units failing the stress tests to see if there was any correlation between the device reliability and the metal and polysilicon quality. Figures 25 through 28 are typical SEM photographs of devices that completed the stress test program. No evidence of degradation was observed in the polysilicon or metallization coverage over the epitaxial island edges and contacts as a result of the stress tests with the exception of one TC1092 metallization open noted in the thermal shock test.

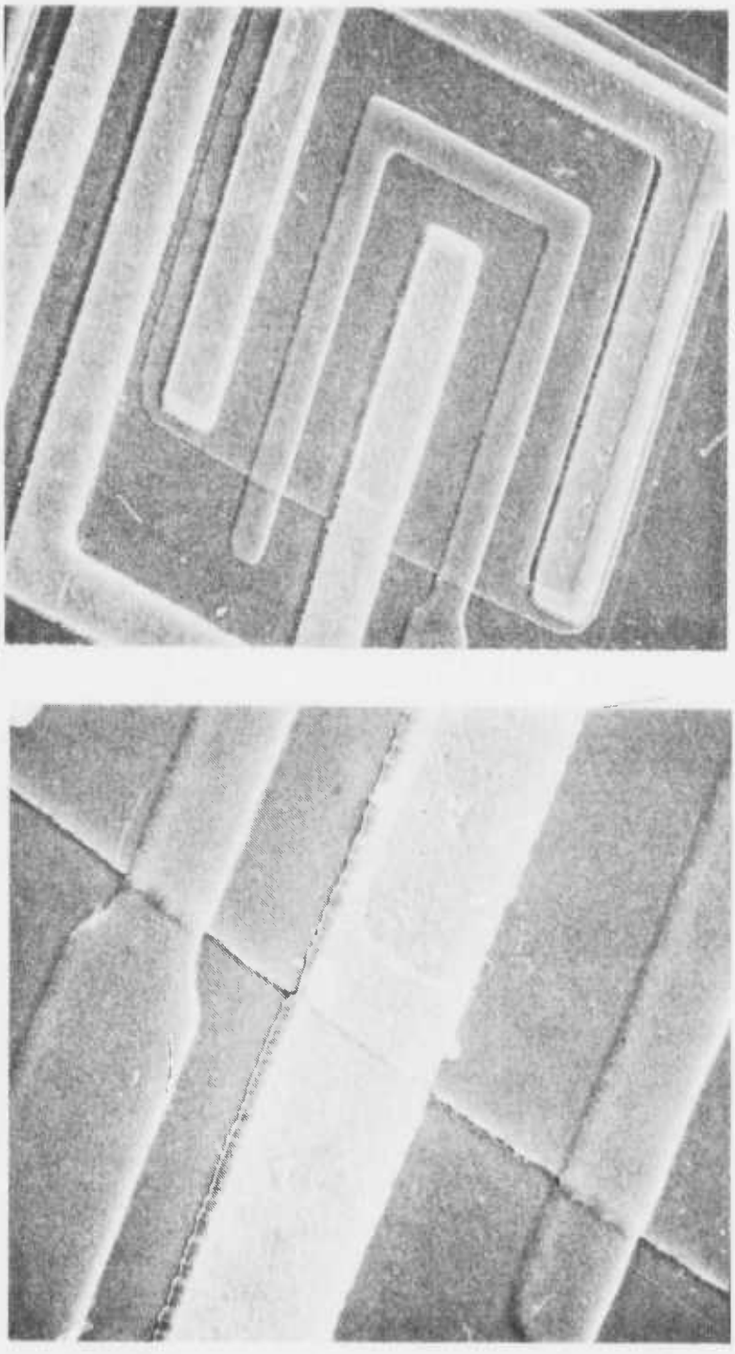
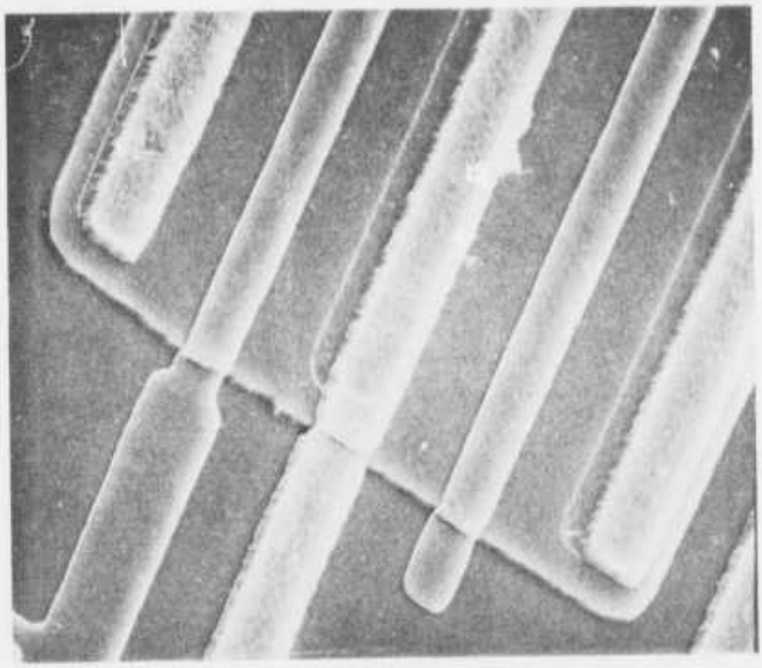
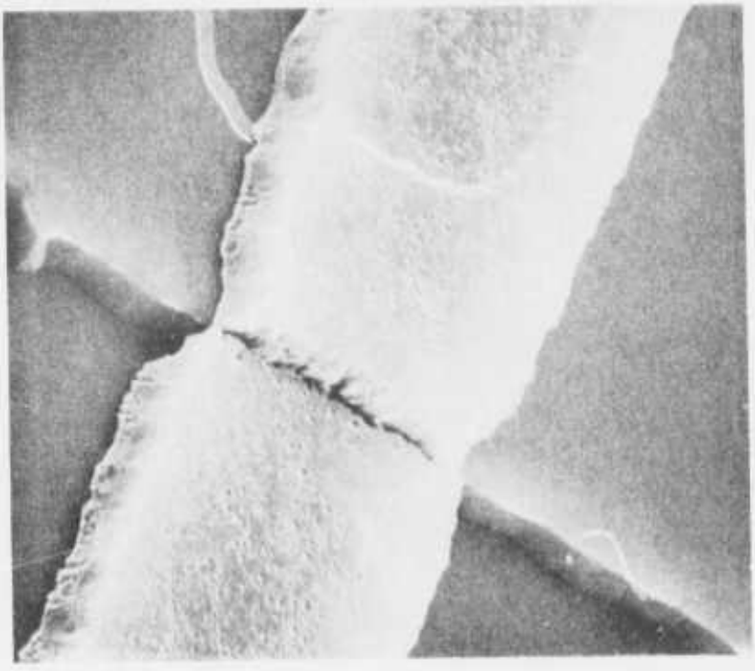


Figure 22. Pre-stress SEM photographs of TCS056, (a) 800X and (b) 2000X.



(a)



(b)

Figure 23. Pre-stress SEM photographs of TC1092, (a) 1000X and (b) 5000X.

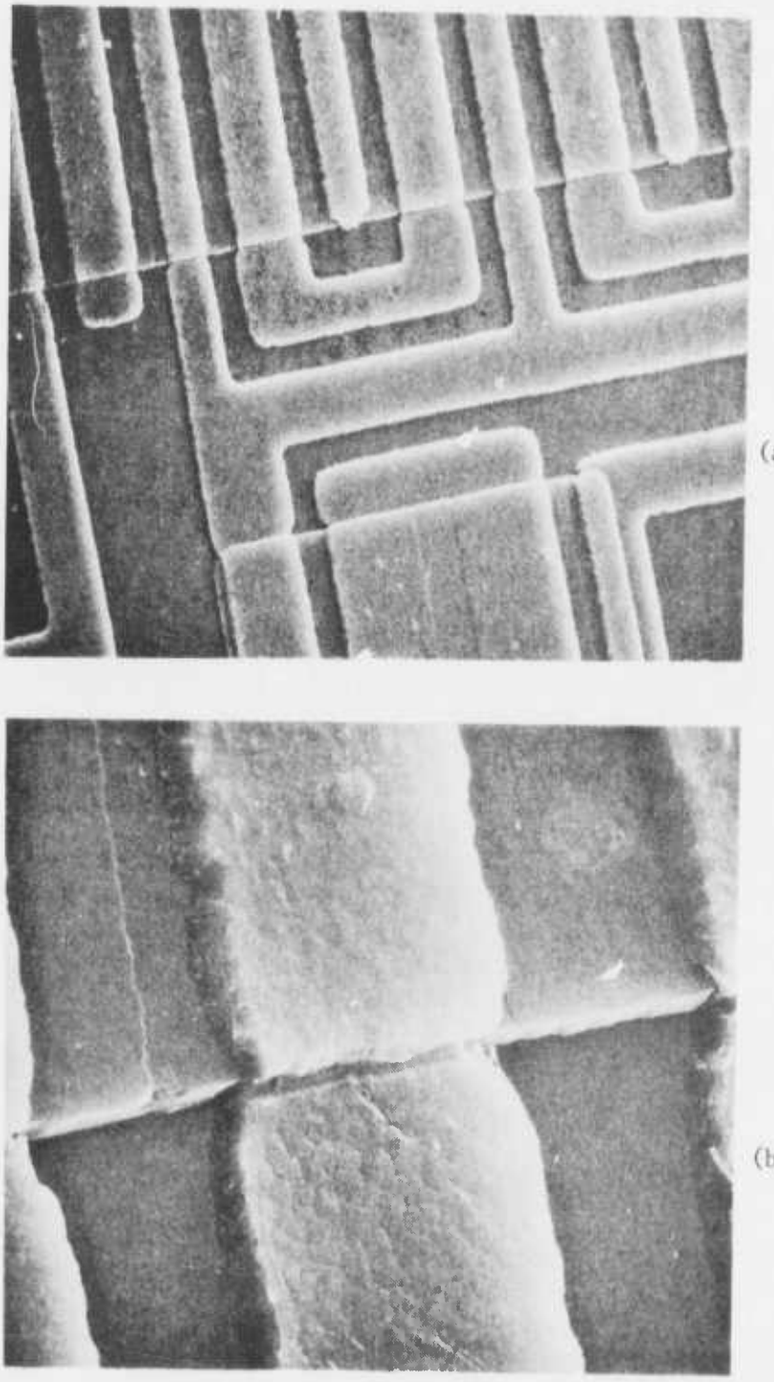


Figure 24. Pre-stress SEM photographs of 4007S, (a) 800X and (b) 5000X.

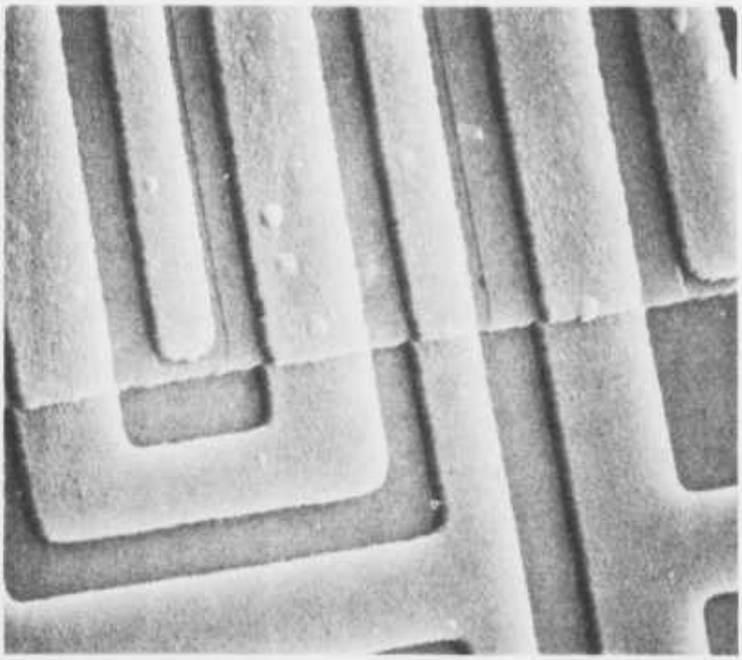


Figure 25. Al-gate 4007S (#115) after high-temperature storage stress (1000X).

Figure 26. Si-gate TCS056 (#85) after temperature cycling with intermittent bias stress test (3000X).

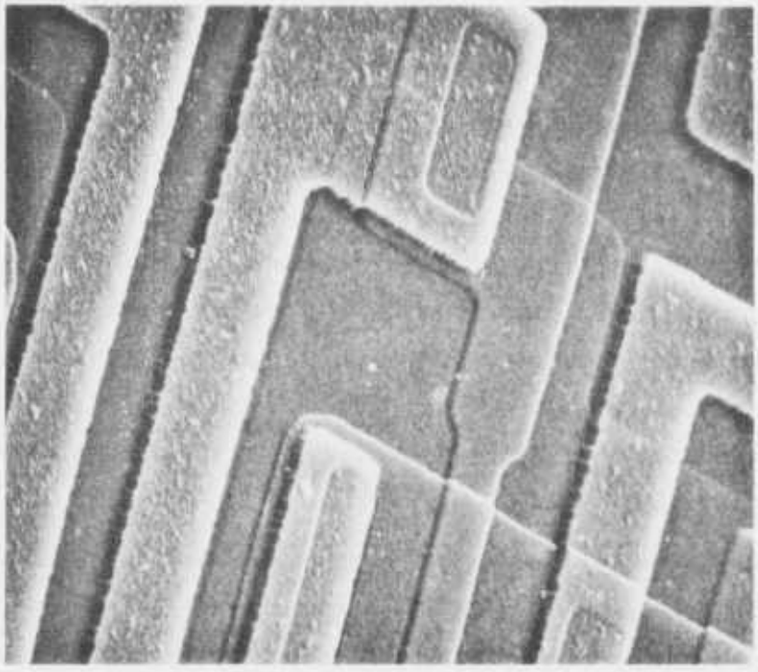


Figure 27. Si-gate TCS056 (#62) after operational life at 125°C (1000X).

Figure 28. Si-gate TC1092 (#113) after temperature cycling with intermittent bias (3000X).

IX. HIGH- AND LOW-TEMPERATURE TEST RESULTS

Pre- and post-stress testing was performed on all subgroups at 25°, -55°, and 125°C. The 25°C data are shown in the trend analysis plots. The high- and low-temperature data are summarized in Table 12.

The data indicate that if end-point testing had been performed at 125°C at each test interval, instead of at the end of the test, potential failures may have been spotted prior to the time of failure (as determined by the room temperature measurements).

Typical examples (data from Table 12) of parametric changes that may be precursors of failure are:

(1) decreasing n-transistor thresholds for the TCS056 and TC1092 devices under very high (300°C) temperature storage conditions.

(2) increasing leakage currents (I_{SS}) for the 4007S devices under all stress conditions.

(3) degradation of the output drive current for the 4007S arrays (most evident on the p transistors).

TABLE 12. PRE- AND POST-STRESS TEST - HIGH- AND LOW-TEMPERATURE DATA

Test Parameter	Stress Test	-55°C				+125°C			
		N		P		N		P	
		$\bar{X}$	Sigma	$\bar{X}$	Sigma	$\bar{X}$	Sigma	$\bar{X}$	Sigma
Threshold Voltage	Pre-Stress	1.2	0.1	1.4	0.1	1.0	0.08	1.2	0.2
TCS056	Thermal Shock	1.1	0.06	1.4	0.14	0.9	0.06	1.2	0.16
(in volts)	Temperature Cycling	1.5	0.1	1.6	0.3	1.0	0.04	1.3	0.1
	Operational Life	1.2	0.06	2.0	0.4	1.2	0.08	2.4	0.4
	High-Temp Storage	1.0	0.32	2.4	0.29	0.6	0.23	2.0	0.28
Threshold Voltage	Pre-Stress	1.5	0.1	1.5	0.1	1.3	0.1	1.3	0.1
TC1092	Thermal Shock	1.5	0.06	1.5	0.11	1.3	0.05	1.3	0.1
(in volts)	Temperature Cycling	1.6	0.1	1.5	0.1	1.4	0.1	1.4	0.1
	Operational Life	1.6	0.2	2.5	0.3	1.5	0.05	2.4	0.3
	High-Temp Storage	1.0	0.26	2.0	0.24	1.2	0.27	2.5	0.23
Threshold Voltage	Pre-Stress	1.7	0.2	2.3	0.2	1.5	0.1	2.4	0.2
4007S	Thermal Shock	1.8	0.8	2.4	0.19	1.4	0.09	2.4	0.18
(in volts)	Temperature Cycling	2.1	0.26	2.7	0.3	1.6	0.3	2.5	0.3
	Operational Life	1.7	0.13	2.4	0.18	1.3	0.14	2.6	0.17
	High-Temp Storage	1.7	0.35	2.4	0.17	1.6	0.3	2.5	0.15

TABLE 12. PRE- AND POST-STRESS TEST - HIGH- AND LOW-TEMPERATURE DATA (Continued)

Test Parameter	Stress Test	-55°C Inputs High $\bar{X}$	-55°C Inputs High Sigma	-55°C Inputs Low $\bar{X}$	-55°C Inputs Low Sigma	+125°C Inputs High $\bar{X}$	+125°C Inputs High Sigma	+125°C Inputs Low $\bar{X}$	+125°C Inputs Low Sigma
Leakage Current (I_{SS}) TCS056 (in nA)	Pre-Stress	55	15	100	20	59	10	83	21
	Thermal Shock	50	7	97	23	67	8.5	142	18
	Temperature Cycling	143	20	279	80	32	50	899	131
	Operational Life	276	86	531	362	260	35	543	87
	High-Temp Storage	434	210	866	250	454	225	2700	600
Leakage Current (I_{SS}) TC1092 (in µA)	Pre-Stress	7.2	1.0	0.22	0.27	11.2	1.0	0.3	0.27
	Thermal Shock	7.5	0.9	0.20	0.43	16.2	1.9	0.35	0.4
	Temperature Cycling	7.3	1.5	0.34	0.8	11.3	1.1	0.48	0.8
	Operational Life	7.3	1.0	0.74	0.7	13.8	1.9	0.42	0.47
	High-Temp Storage	7.2	0.75	1.8	0.6	12.6	1.2	1.7	0.5
Leakage Current (I_{SS}) 4007S (in nA)	Pre-Stress	40	8	29	5.2	210	33	109	11
	Thermal Shock	39	5	26	5	332	39	163	16
	Temperature Cycling	141	110	37	9.5	194	171	41	9.8
	Operational Life	546	100	227	47	643	153	216	90
	High-Temp Storage	212	120	90	20	212	150	95	20

TABLE 12. PRE- AND POST-STRESS TEST - HIGH- AND LOW-TEMPERATURE DATA (Continued)

		-55°C				+125°C			
		N		P		N		P	
		$\bar{X}$	Sigma	$\bar{X}$	Sigma	$\bar{X}$	Sigma	$\bar{X}$	Sigma
Output Drive Current TCS056 (in mA)	Pre-Stress	8.9	0.4	32.7	1.6	7.0	0.3	23.9	1.1
	Thermal Shock	9.8	0.35	33.1	1.9	6.9	0.3	24.8	1.2
	Temperature Cycling	8.5	1.9	31.4	1.2	6.5	0.27	22.8	0.89
	Operational Life	8.6	0.4	28.8	1.3	6.5	0.33	21.5	1.09
	High-Temp Storage	8.6	0.53	27.3	1.5	7.3	0.4	22.2	1.3
Output Drive Current TC1092 (in mA)	Pre-Stress	8.4	0.56	29.3	2.0	6.0	0.35	21.1	1.7
	Thermal Shock	8.8	0.48	29.5	2.6	6.1	0.4	20.9	1.8
	Temperature Cycling	7.6	1.9	29.0	2.7	5.8	0.3	21.2	2.0
	Operational Life	8.0	0.86	27.9	2.3	5.9	0.71	21	2.9
	High-Temp Storage	8.7	0.78	26.7	2.1	6.9	0.69	20.9	1.88
Output Drive Current 4007S (in mA)	Pre-Stress	28.2	1.9	74.9	2.6	22.0	1.3	61.4	2.0
	Thermal Shock	28.9	2.1	76.5	3.4	21.6	1.4	54.4	2.7
	Temperature Cycling	26.3	1.3	72.6	3.2	21.2	1.3	55.9	3.1
	Operational Life	27.2	1.6	75.7	3.4	21.9	1.0	56.0	2.6
	High-Temp Storage	24.0	5.5	70.0	5.7	19.5	4.5	52.9	4.7

X. HERMETICITY

Helium leak rate measurements were recorded on five units of each device type prior to the start of the stress test program and also on representative samples at the completion of each stress test. The data are summarized in Table 13. There were no significant changes in leak rates resulting from the various stresses.

TABLE 13. LEAK-RATE ANALYSIS (ATM. cm^3/s)

Circuit Type	Ser. #	Leak Rate No Stress ($\times 10^{-8}$)	Ser. #	Leak Rate High-Temp Storage ($\times 10^{-8}$)	Stress Test Ser. #	Leak Rate Thermal Shock ($\times 10^{-8}$)	Ser. #	Leak Rate Oper. Life ($\times 10^{-8}$)	Ser. #	Leak Rate Temp -Cycling Intermittent-Bias ($\times 10^{-8}$)
TCS056	143	0.1	15	4.5	32	0.02	49	0.05	71	0.04
	144	0.8	25	3.2			59	0.07	72	0.04
	145	0.6								
	146	0.5								
	147	0.1								
TC1092	166	0.2	14	1.8	54	0.04	64	0.04	110	0.05
	167	0.2	38	3.1	56	0.08	76	0.08	114	0.01
	168	0.1								
	169	0.1								
	170	0.2								
4007S	636	1.5	150	5.0	223	1.8	312	2.8	88	1.8
	642	1.3	152	3.2	225	2.5	317	1.2	89	3.2
	644	1.8								
	647	1.8								
	650	1.4								

XI. DATA ANALYSIS

A major requirement of this program was the collection and analysis of variables data recorded during the stress test period. The variables data were analyzed after several programs were generated to create computer/language compatibility. Key parameters such as output drive current, leakage current, and threshold voltages were closely monitored so that imminent device failure could be detected. These data were also used to assist in devising effective screens for the elimination of "maverick" failures, both catastrophic and parametric.

All test data were stored on Cartrifiles (magnetic tape). The data were then recompiled using a PDP-11 system and reformatted onto IBM magnetic tape reels. All statistical analysis was performed using the RAMIS (Rapid Access Management Information System) programs in the IBM-370 system. RAMIS is a general-purpose information processing system. It permits files to be created; data to be entered and maintained with any necessary changes, deletions, or additions; and comprehensive reports to be prepared upon request. The primary purpose of the RAMIS programs is to allow information to be organized easily and quickly and to be retrieved for presentation.

Key RAMIS programs utilized for both a fast data overview and in-depth statistical analysis are described below.

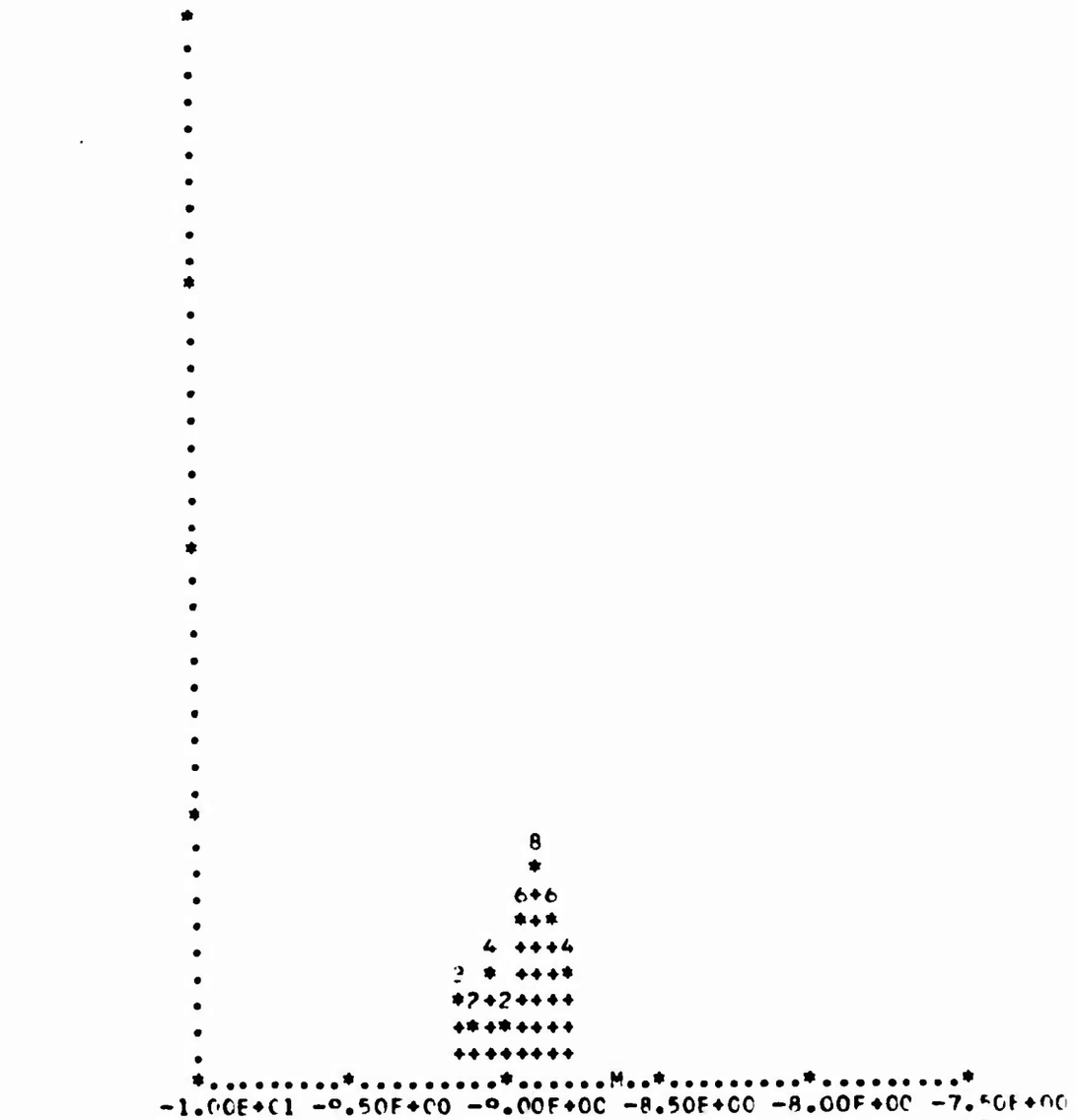
A. HISTOGRAM

Figure 29 shows a typical histogram plot for the p-threshold data for the TC1092 type after 10 cycles of thermal shock. The plot yields various pieces of data, including mean and standard deviation measurements and total population distribution. Superimposing these plots can quickly tell whether or not the cell population is stable or is shifting as each subsequent measurement is taken.

B. MATRIX

The matrix program was generated to create a quick overview of failing parameters and trends. The plot obtained (Fig. 30) graphs the test number vs

```
DATE PRINTED : 09/23/75                          TIME PRINTED : 15.16.07
HISTOGRAM FOR TYPE =1092
              LOT  =T10 (THERMAL SHOCK AFTER 10 CYCLES)
              TEST =35 OR 36 OR 37 IF SUBTEST IS V
              ULIM=-7.5   LLIM=-10.0
```




```
CELL WIDTH: 5.00E-02     COUNT: EACH + IS    1 UNIT(S)
SAMPLE SIZE:   36  PLOTTED:   35  ABOVE:    1  BELOW:     0  CLAMP:    0
SAMPLE MAX VAL: -9.040E-01      MIN VAL: -9.148E+00          UNITS: UV
SAMPLE MEAN:    -8.674E+00      SIGMA:    1.645E+00
PLOTTED MEAN:   -8.948E+00      SIGMA:    1.046E-01
```

Figure 29. Typical histogram plot for p-threshold data.

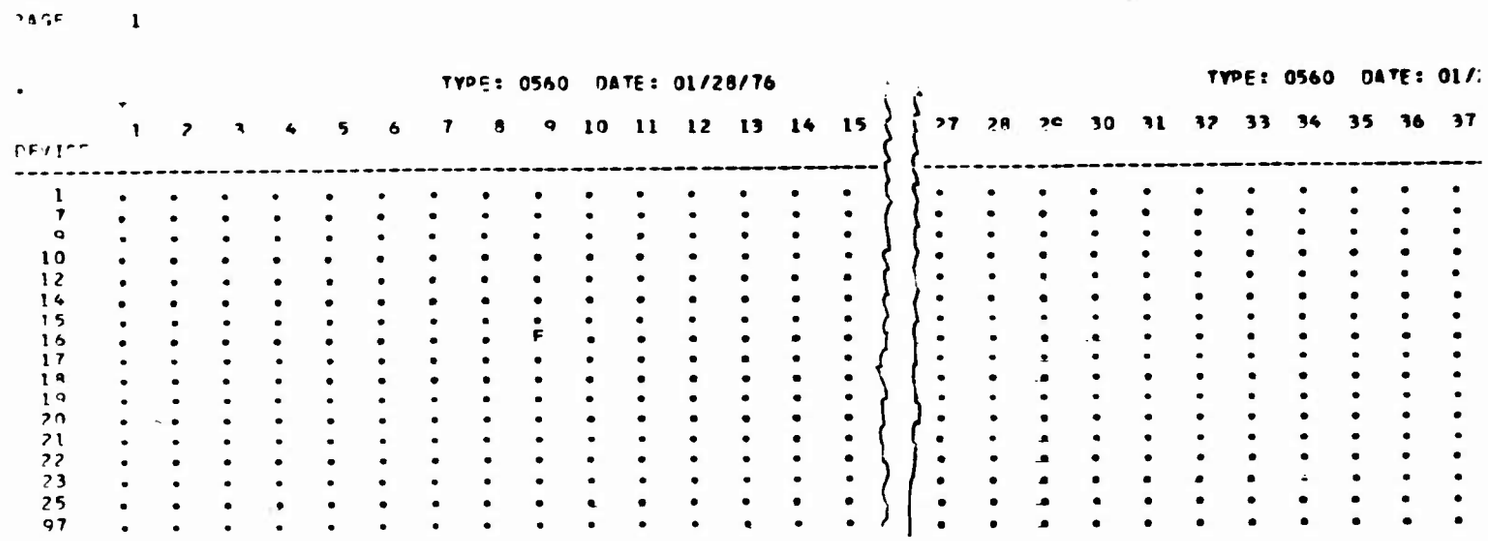


Figure 30. Matrix used to determine failure parameters and trends.

the unit number and indicates a failure with an "F". Trending, such as the edge-leakage phenomenon noted on the Al-gate arrays, was easily monitored by observing the changes in the quantity of failures observed.

Table 14 is a typical printout. The listing gives the minimum, average, maximum, and sigma values obtained for each test. These listings were used for the generation of the trend graphs, because all of the necessary data were reported in a very concise manner.

TABLE 14. TYPICAL MATRIX PROGRAM PRINTOUT

********* TCSU56 02/28/76 *********
VALUES ARE BY TEST IF LIMIT IS NOT '9'
SUBTEST IS 'V'

LOT	TEST #	MINIMUM VALUE	AVERAGE VALUE	MAXIMUM VALUE	R	U	SIGMA
HT250200	1	-4.999000	-4.992067	-4.882000	U	V	.02550336
	2	11.990000	11.994795	12.000000	U	V	.00974560
	3	10.770000	11.928389	12.000000	U	V	.25045484
	4	11.990000	11.998798	12.000000	U	V	.00539200
	5	-5.004999	-5.003716	-5.002000	U	V	.00949205
	6	-5.014999	-5.002235	-4.997999	U	V	.00812602
	7	.389000	.435880	.871000	U	V	.09041369
	8	9.636999	9.689790	9.712000	M	V	.01798379
	9	9.448999	9.662632	9.705000	M	V	.05311316
	10	9.648000	9.674312	9.695999	M	V	.01389649
	11	.406000	.434060	.462000	M	V	.01451038
	12	.385000	.423159	.495000	M	V	.02694355
	13	.026000	.074000	.138000	M	V	.02336003
	14	9.796000	9.822752	9.839999	U	V	.01143208
	15	8.622999	9.773791	9.863000	U	V	.23543859
	16	9.801000	9.824912	9.856999	U	V	.01306850
	17	.019000	.069960	.102000	U	V	.02064487
	18	.003000	.063240	.102000	U	V	.02192251
	19	-.005000	-.000160	.002000	U	V	.00195305
	20	4.990999	4.995390	4.997999	U	V	.00660282
	21	4.417999	4.974472	5.002999	U	V	.11377126
	22	4.993999	4.998031	5.002999	U	V	.00717181
	23	-.007000	-.005960	-.004000	U	V	.00072002
	24	-.011000	-.001920	.002000	U	V	.00269696
	25	-.010000	.014400	.040000	U	A	.01329058
	26	.040000	.056400	.070000	U	A	.00889103
	27	.100000	.114800	.130000	U	A	.00854227
	28	-2.569999	-.123200	.140000	U	A	.51356542
	29	-3.509999	-.328400	.090000	U	A	.96647274
	30	6.900000	8.009593	8.480000	M	A	.33400077
	31	25.059998	27.237518	28.829987	M	A	.89550120
	32	8.629000	8.809153	8.929000	M	V	.06660700
	33	8.702000	8.826592	8.938000	U	V	.05387166
	34	7.358999	8.760633	8.933000	U	V	.29135942
	35	-8.738000	-8.583713	-8.268999	U	V	.11432368
	36	-8.733999	-8.588952	-8.230000	U	V	.12541956
	37	-8.749000	-8.605392	-8.282000	U	V	.11462390

C. STRESS TEST TRENDS

Trend graphs containing the $\bar{X} \pm 1$ sigma limits for each test cell were generated from the parametric data collected. The plots presented in Figs. 31 to 42 are for threshold voltage, output drive current, and I_{SS} (test 28) and are separated into groups for thermal shock, temperature cycling with intermittent bias, high-temperature storage, and operational life. These charts were generated to show changes in parametric data both during the individual stress tests and between the stress tests. The N (quantity per test cell) was only reduced if a catastrophic failure occurred. Parametric changes beyond specification limits (not affecting functionality) were included in the data for each population.

D. TCS010 TEST INSERT CHIP LIFE TEST RESULTS

A run of TCS010 wafers was processed concurrently with the TCS056 and TC1092 Si-gate arrays. A total of 25 packaged devices from this run were then subjected to a 125°C life test under the test conditions described in Section IV. Process monitors (transistors, resistors, metallization, Zener diodes) and ring oscillators were measured for comparison with results obtained on the Si-gate TCS056's and TC1092's subjected to the stress test program. Trend plots for all test parameters are shown in Figs. 43 to 53. These charts show the same p- transistor threshold increase phenomenon noted on the other Si-gate arrays, but simultaneously show that all other process control parameters were not affected. While the TCS010 test insert chip is primarily used for "in-process" control during manufacturing, accelerated testing of packaged arrays could possibly be used as a supplementary means of monitoring a high-reliability wafer-processing facility.

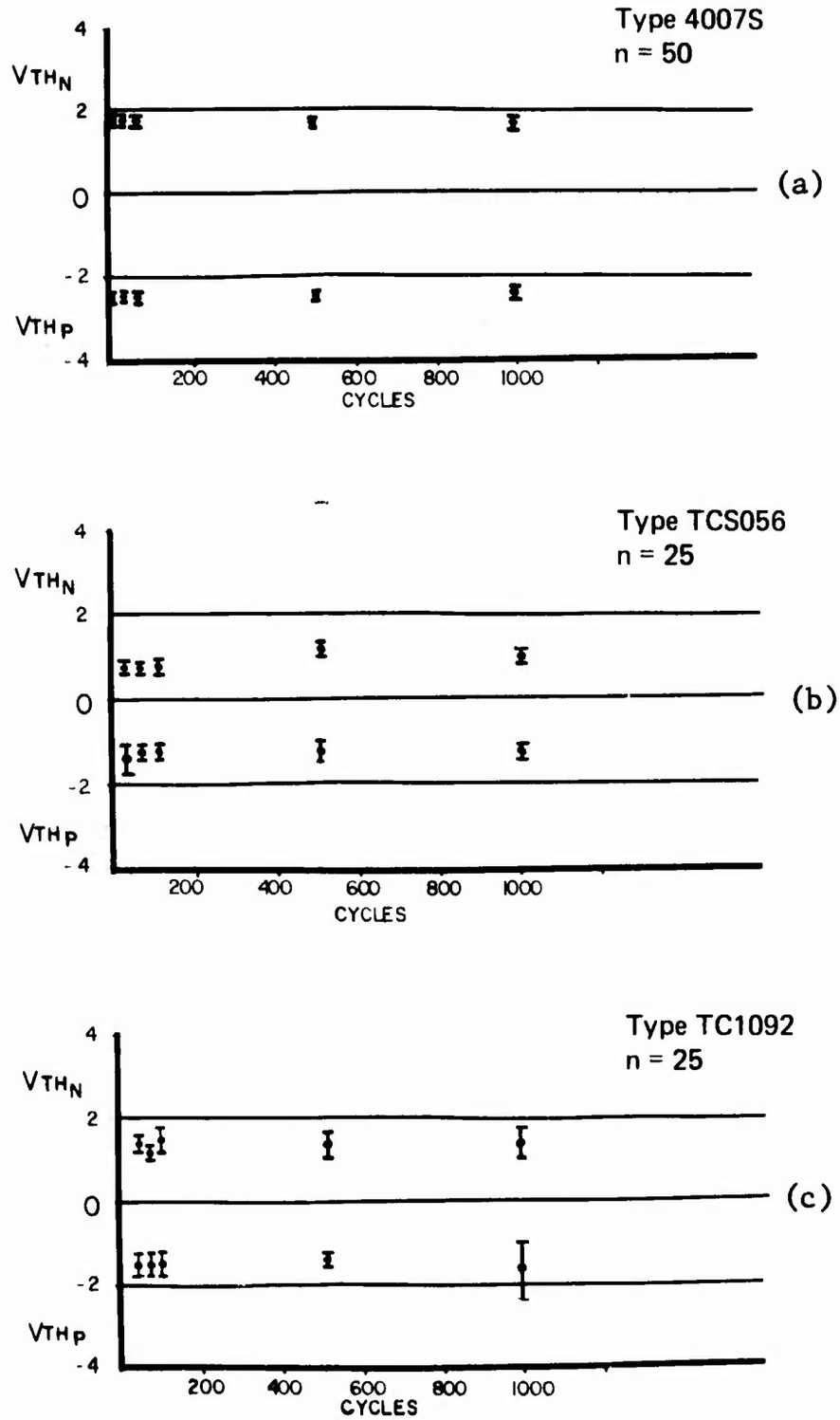


Figure 31. Threshold voltage in temperature cycling intermittent bias test: (a) 4007S, n = 50; (b) TCS056, n = 25; (c) TC1092, n = 25. $\bar{X} \pm 1$ sigma data.

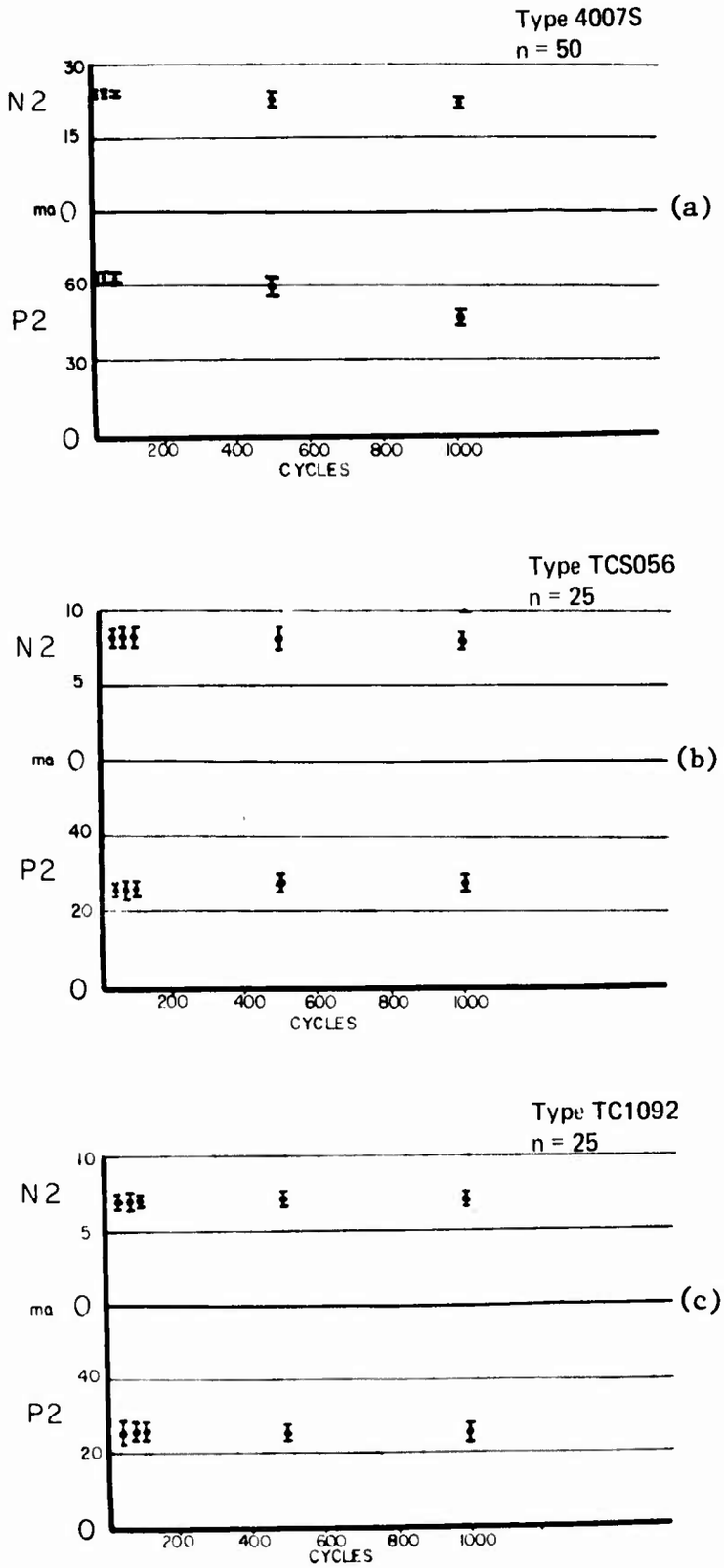
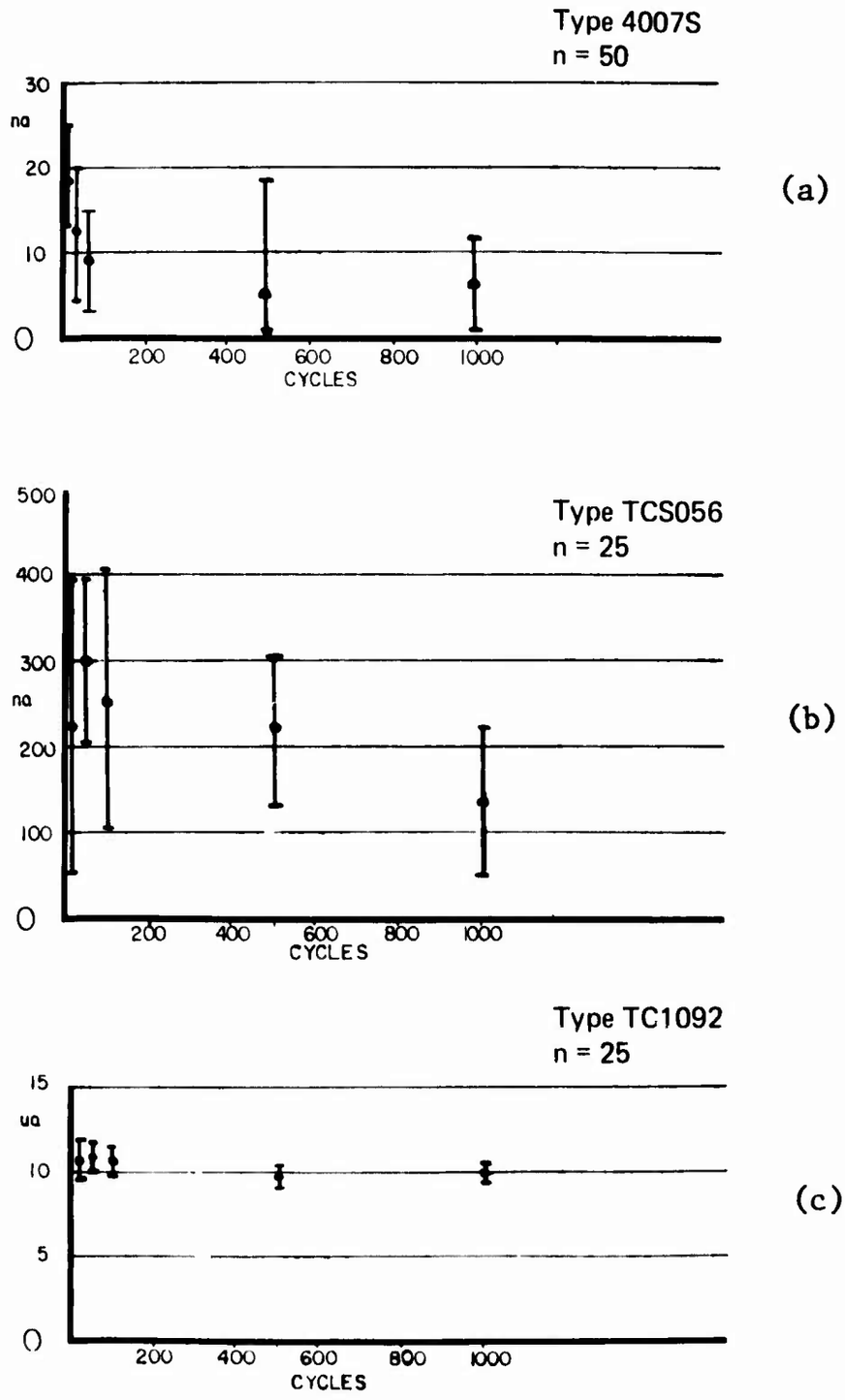


Figure 32. Output drive current in temperature cycling intermittent bias test: (a) 4007S, n = 50; (b) TCS056, n = 25; (c) TC1092, n = 25. $\bar{X} \pm 1$ sigma data.



NOTE: Nanoampere data fluctuations are due to the values approaching the reproduceability limits of the automatic tester.

Figure 33. Leakage current in temperature cycling intermittent bias test: (a) 4007S, n = 50; (b) TCS056, n = 25; (c) TC1092, n = 25 $\bar{X} \pm 1$ sigma data.

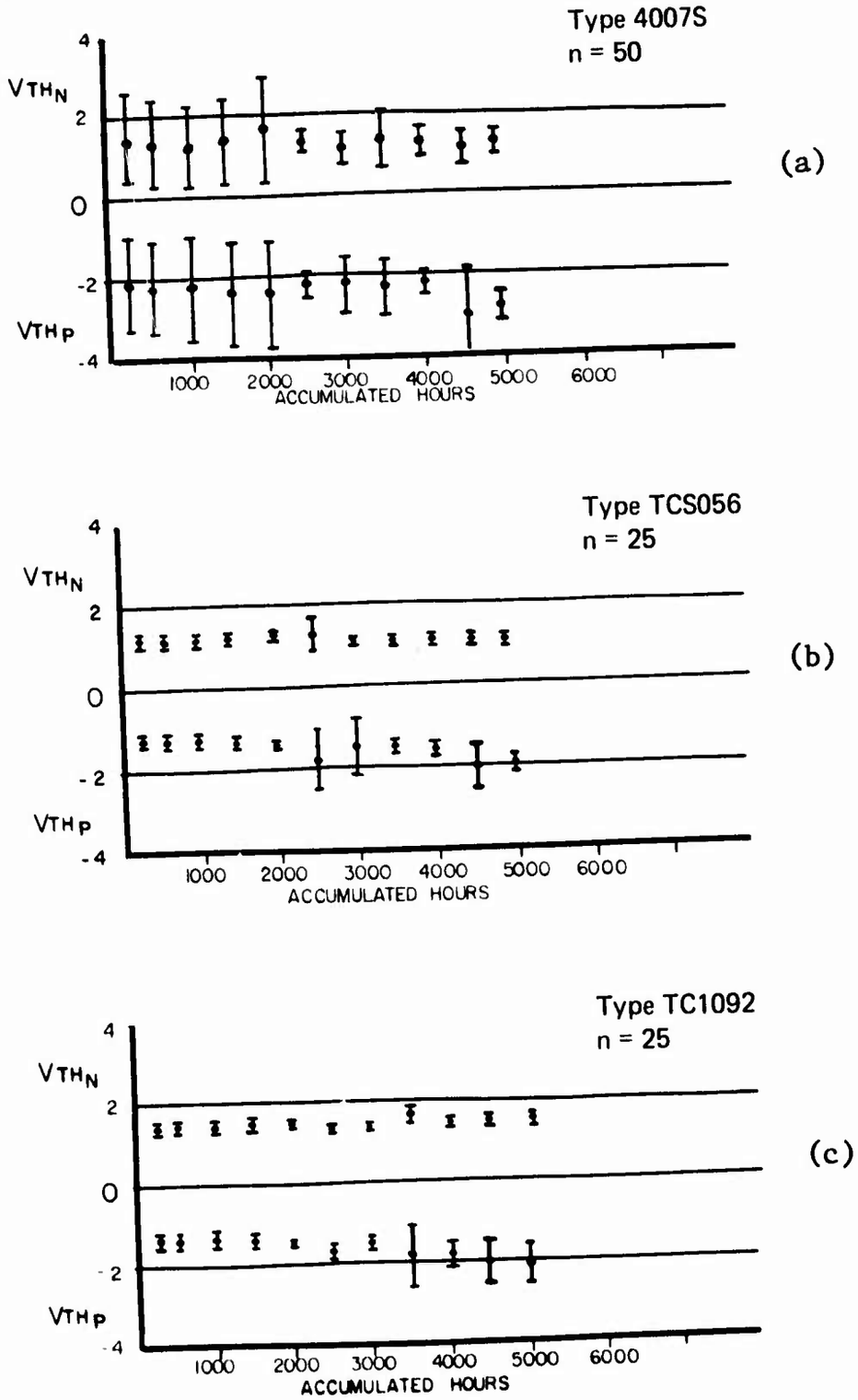


Figure 34. Threshold voltage in operational life test at 125°C: (a) 4007S, n = 50; (b) TCS056, n = 25, (c) TC1092, n =25. $\bar{X} \pm 1$ sigma data.

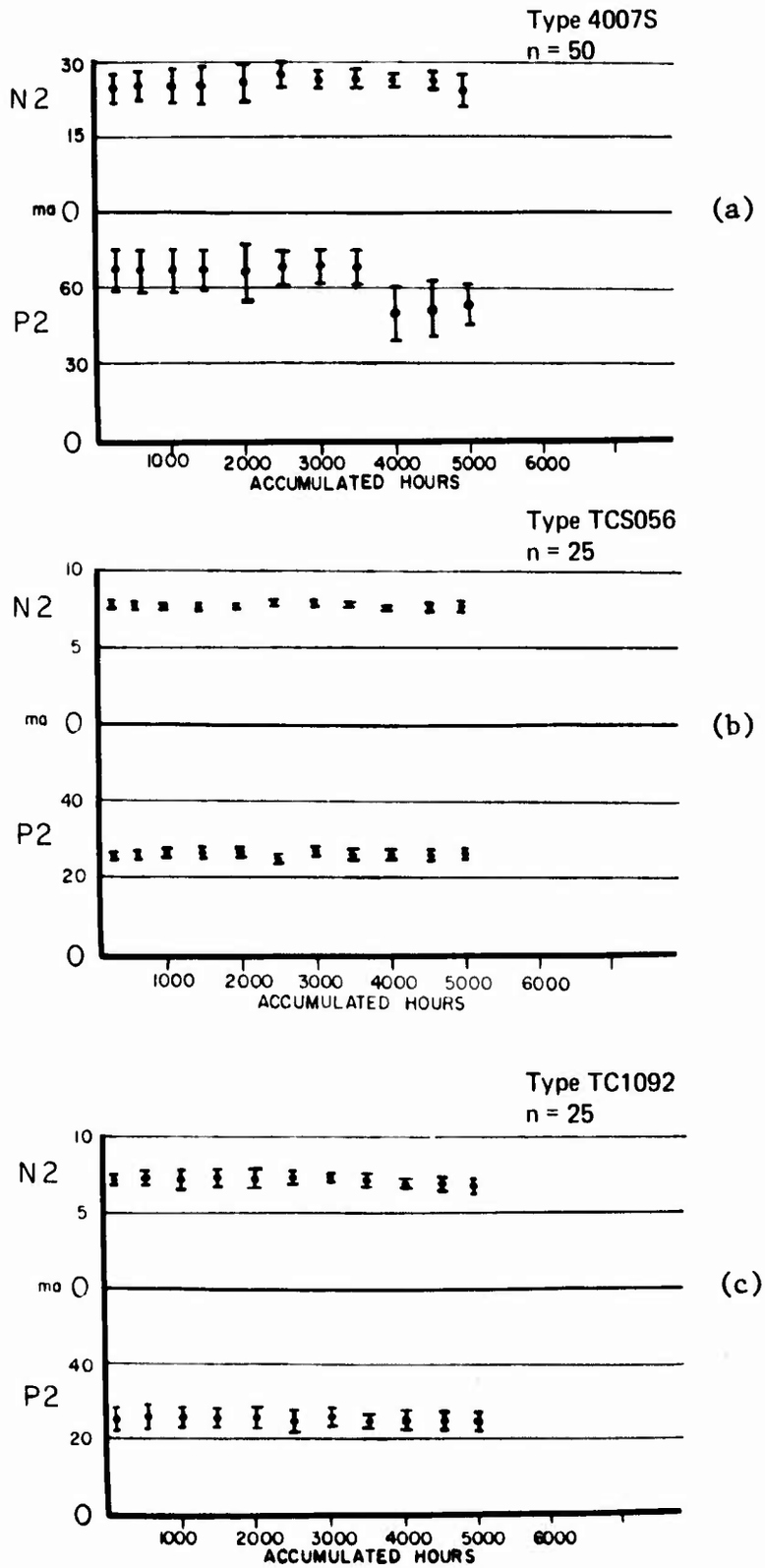
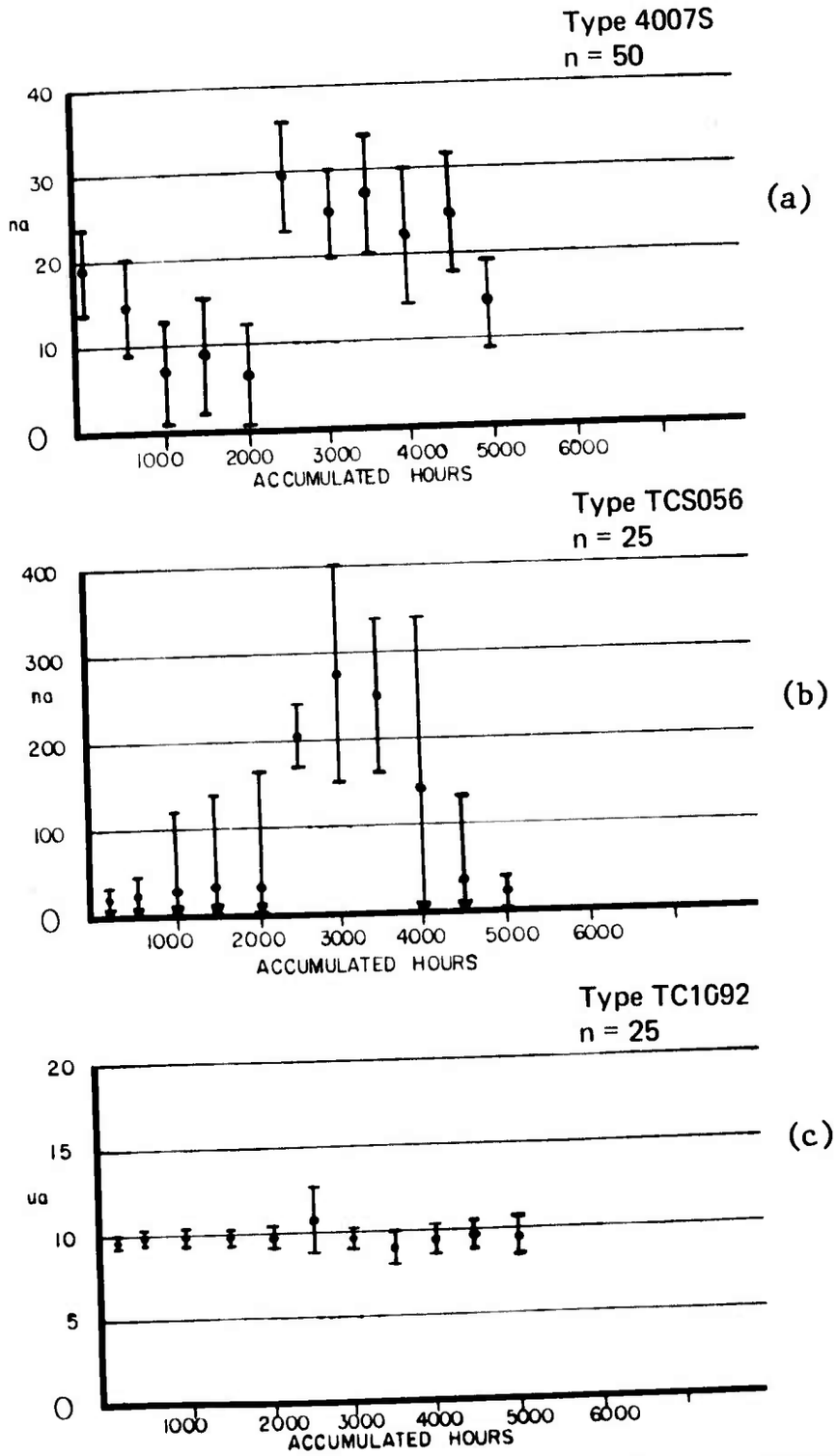


Figure 35. Output drive current in operational life test at 125°C: (a) 4007S, n = 50; (b) TCS056, n = 25, (c) TC1092, n = 25. $\bar{X} \pm 1$ sigma data.



NOTE: Nanoampere data fluctuations are due to the values approaching the reproduceability limits of the automatic tester.

Figure 36. Leakage current (I_{SS}, test 28) in operational life test at 125°C: (a) 4007S, n = 50; (b) TCS056, n = 25, (c) TC1092, n = 25. $\bar{X} \pm 1$ sigma data.

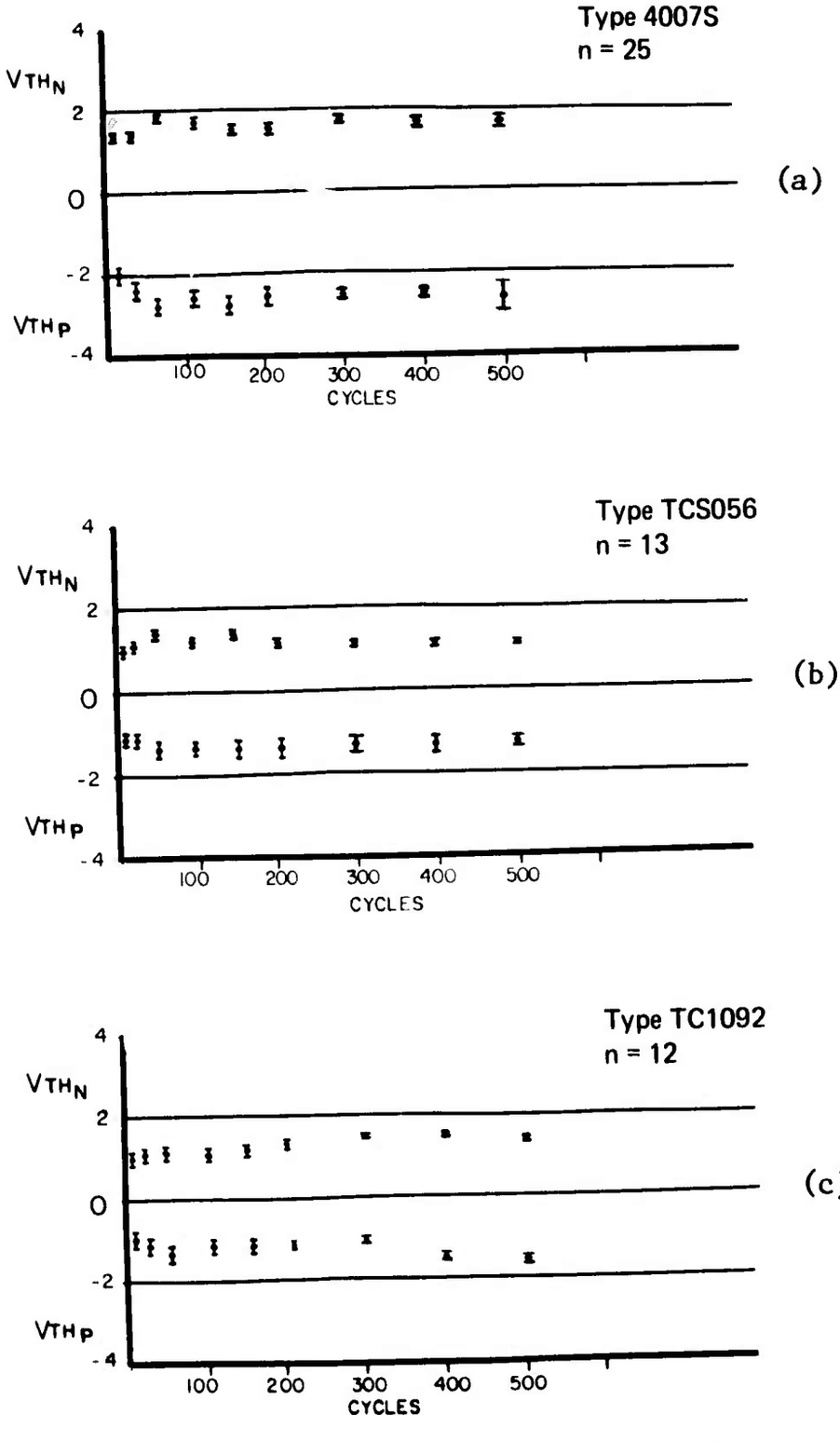


Figure 37. Threshold voltage in thermal shock test: (a) 4007S, n = 25; (b) TCS056, n = 13; (c) TC1092, n = 12. $\bar{X} \pm 1$ sigma data.

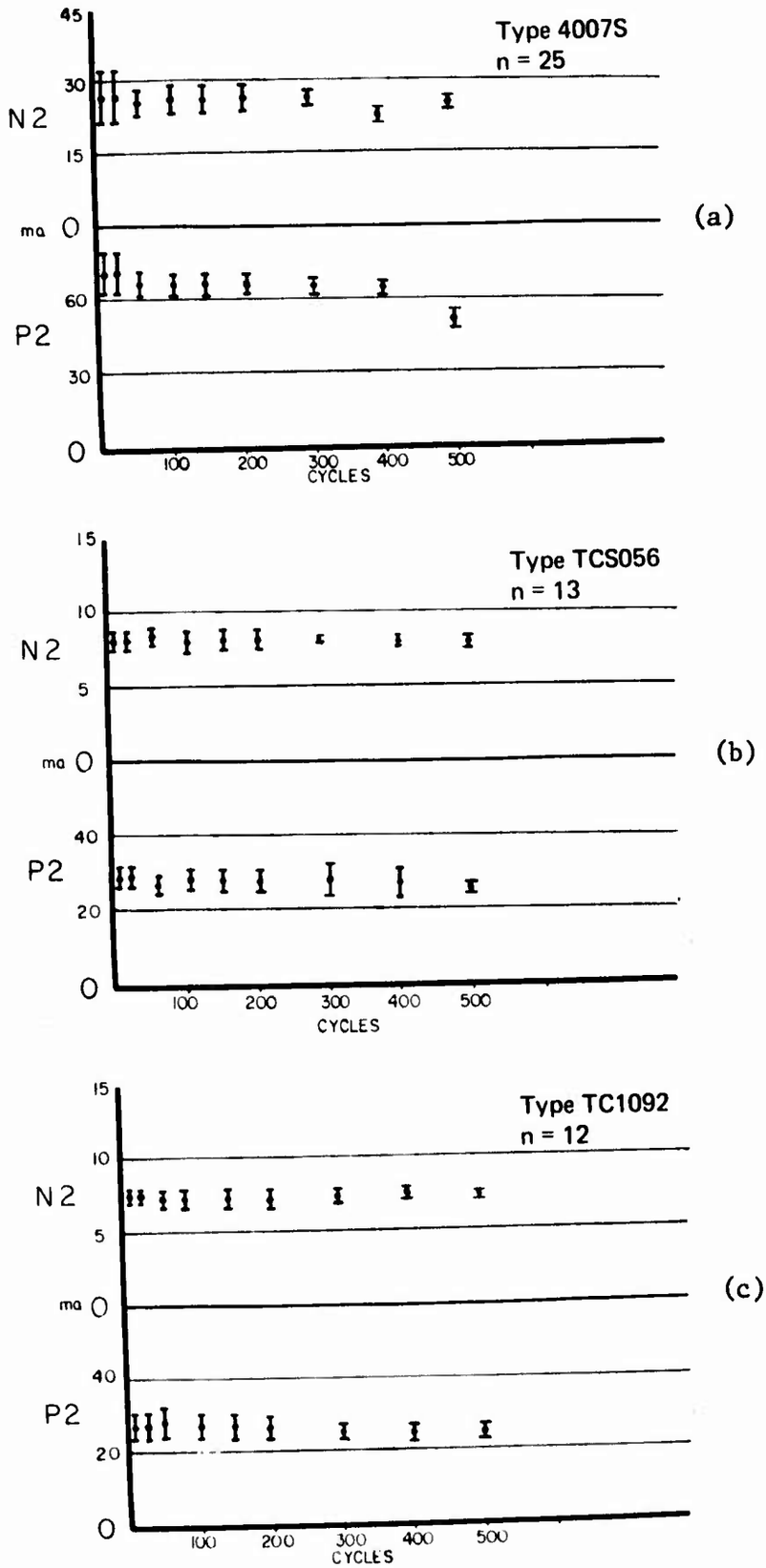
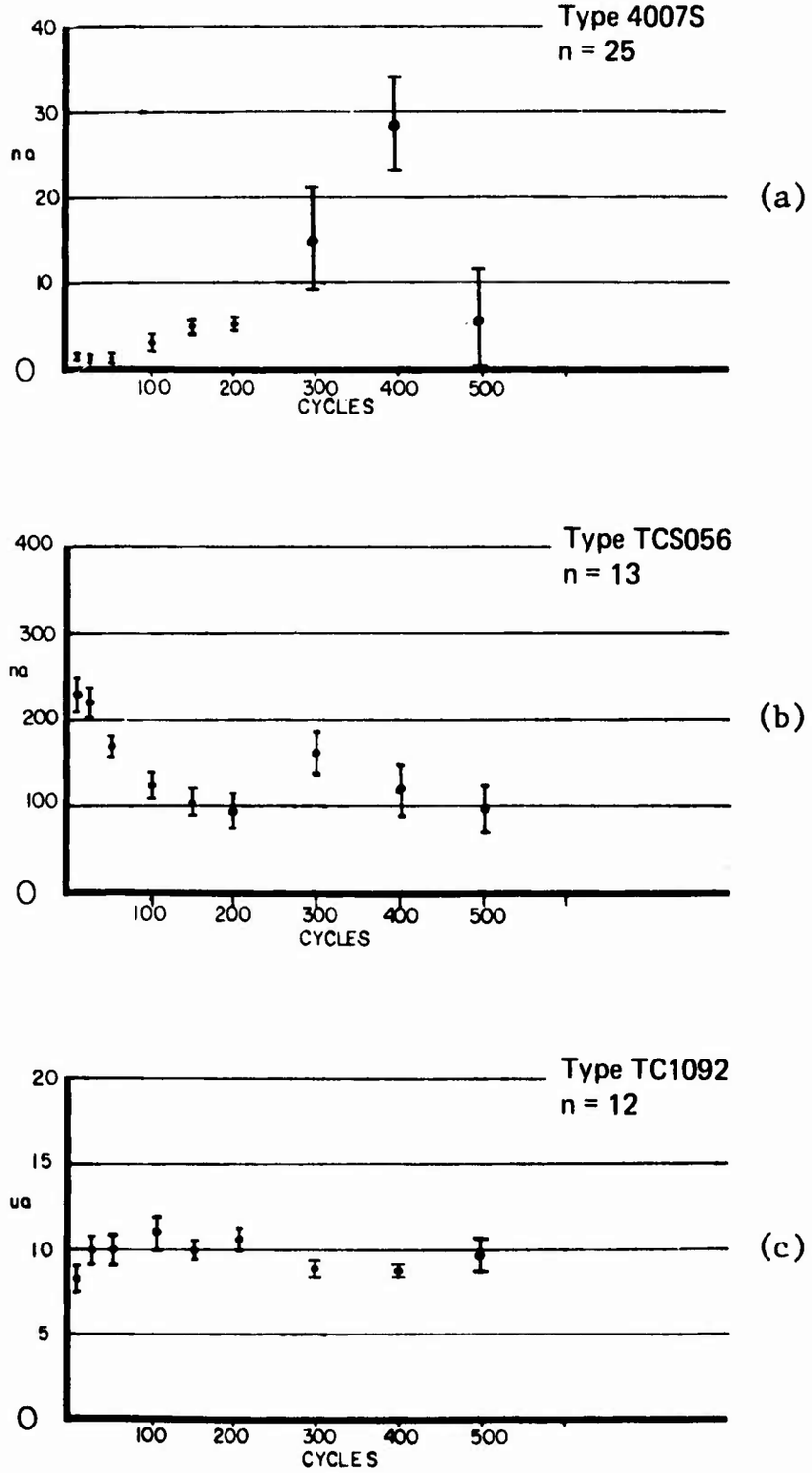


Figure 38. Output drive current in thermal shock test: (a) 4007S, n = 25, (b) TCS056, n = 13; (c) TC1092, n = 12. $\bar{X} \pm 1$ sigma data.



NOTE: Nanoampere data fluctuations are due to the values approaching the reproduceability limits of the automatic tester.

Figure 39. Leakage current in thermal shock test: (a) 4007S, n = 25; (b) TCS056, n = 13; (c) TC1092, n - 12. $\bar{X} \pm 1$ sigma data.

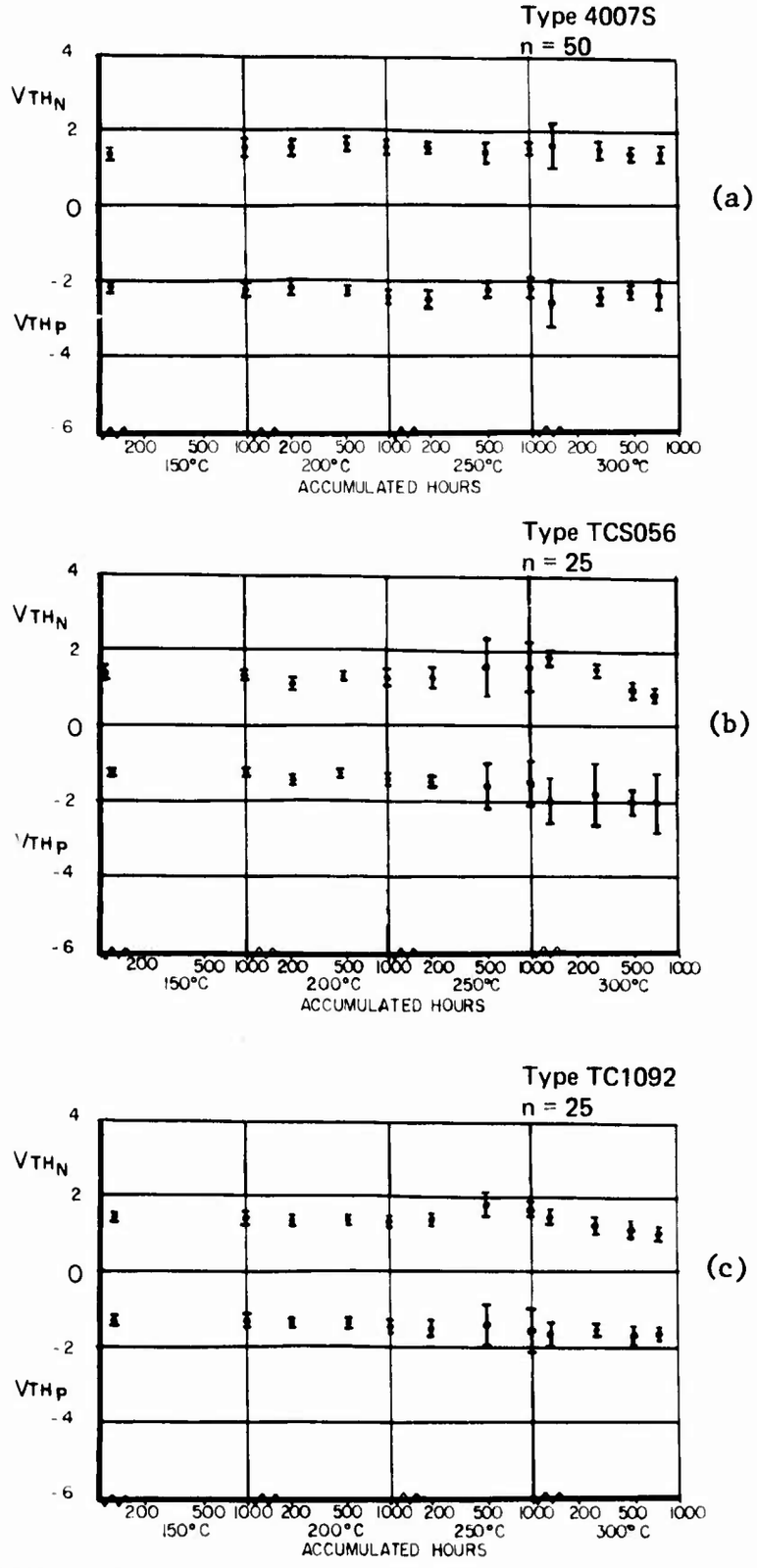


Figure 40. Threshold voltage in high-temperature storage stepped test: (a) 4007S, n = 50, (b) TCS056, n = 25, (c) TC1092, n = 25. $\bar{X} \pm 1$ sigma data.

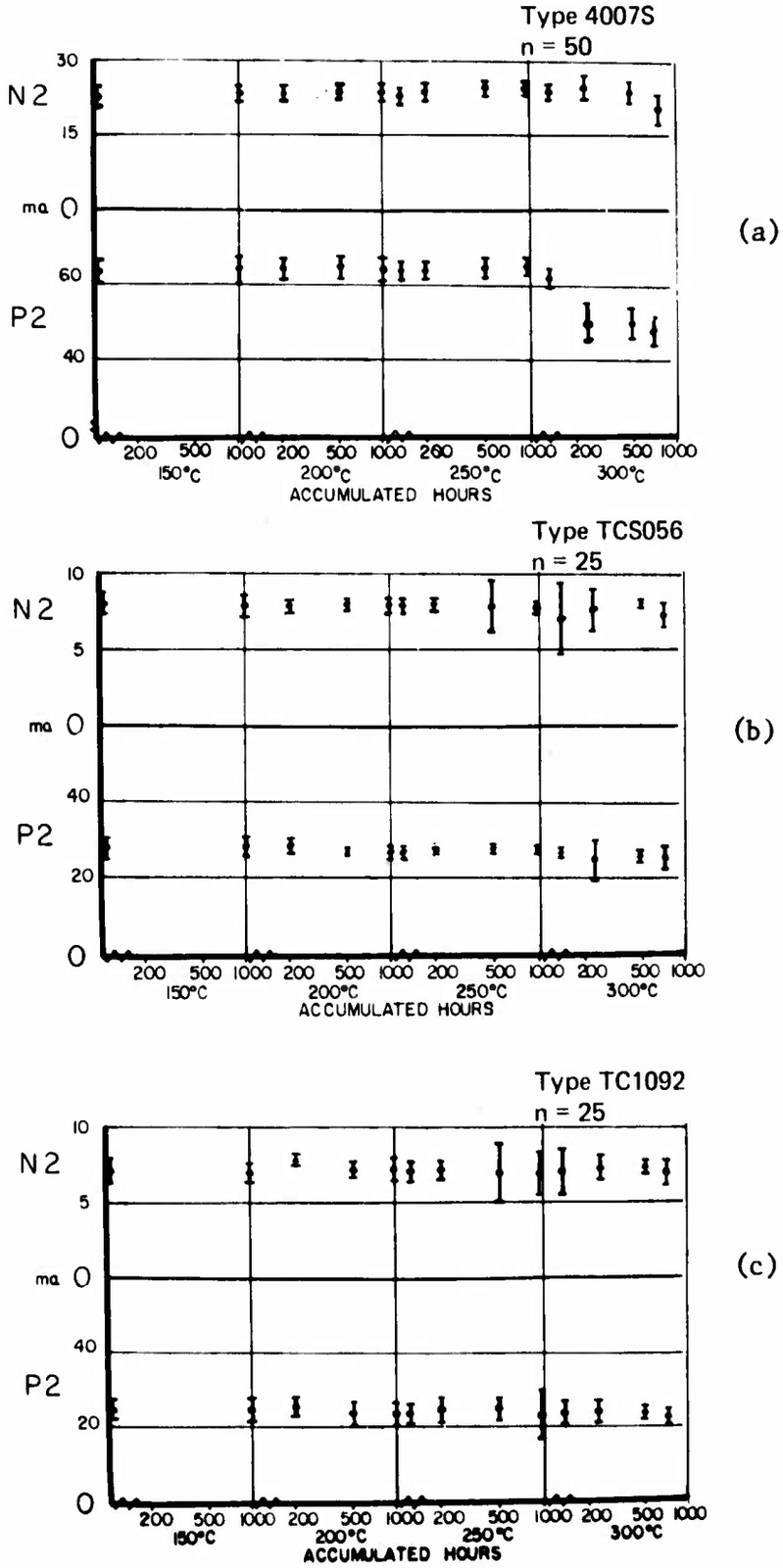
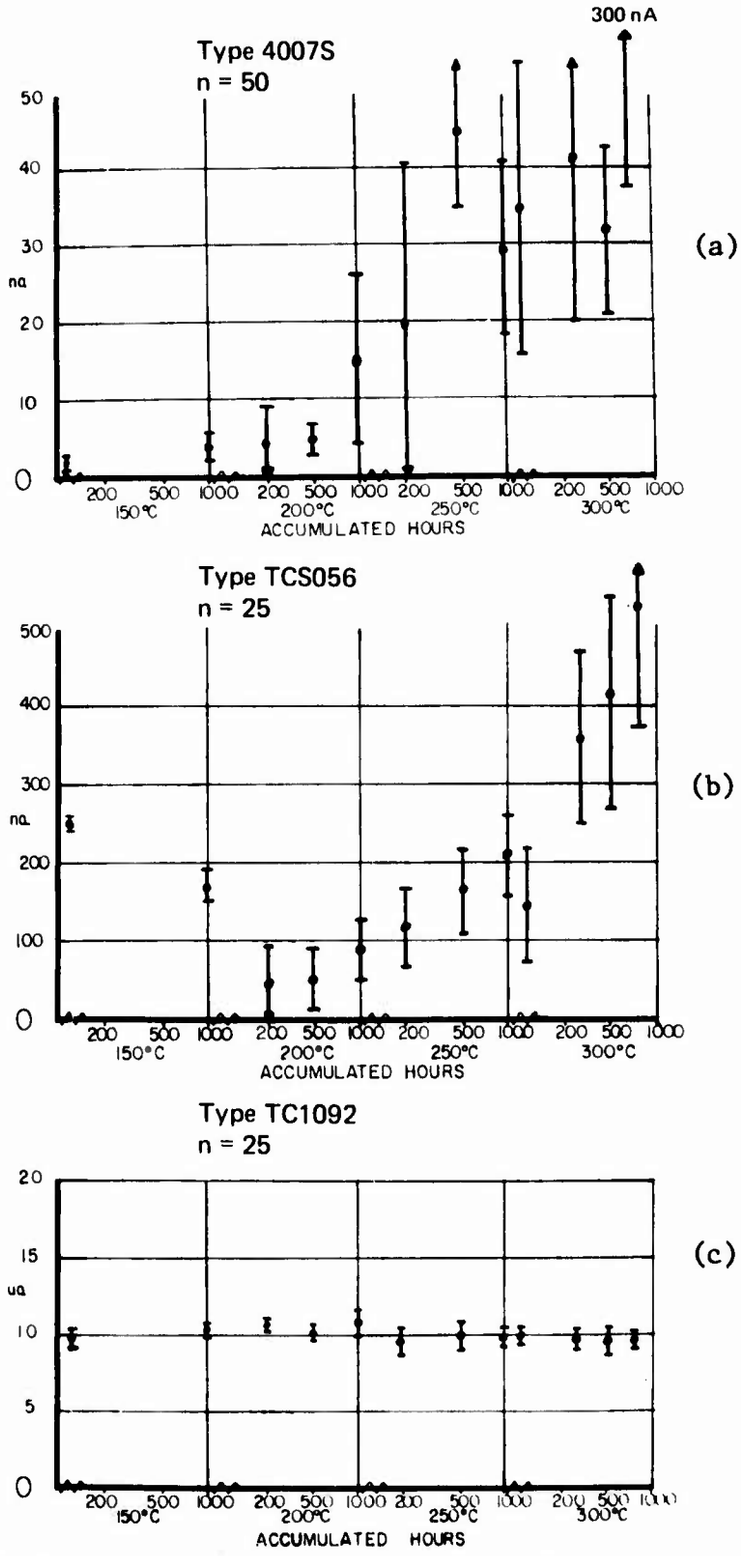
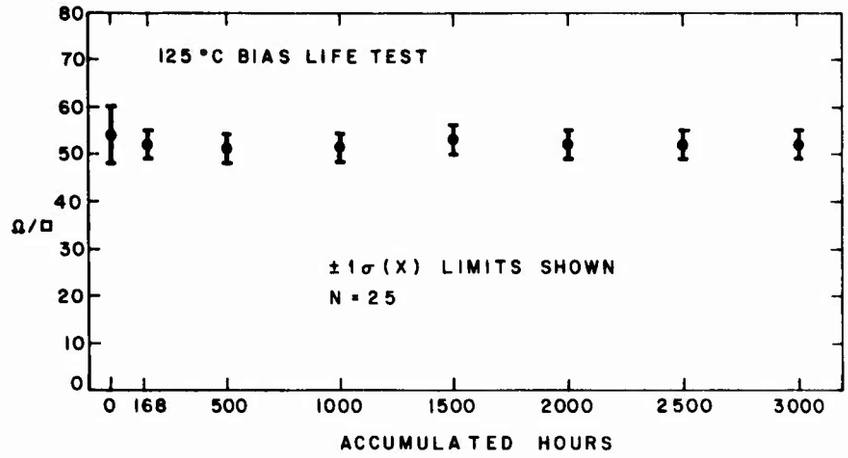


Figure 41. Output drive current in high-temperature storage stepped test: (a) 4007S, n = 50, (b) TCS056, n = 25, (c) TC1092, n = 25. $\bar{X} \pm 1$ sigma data.

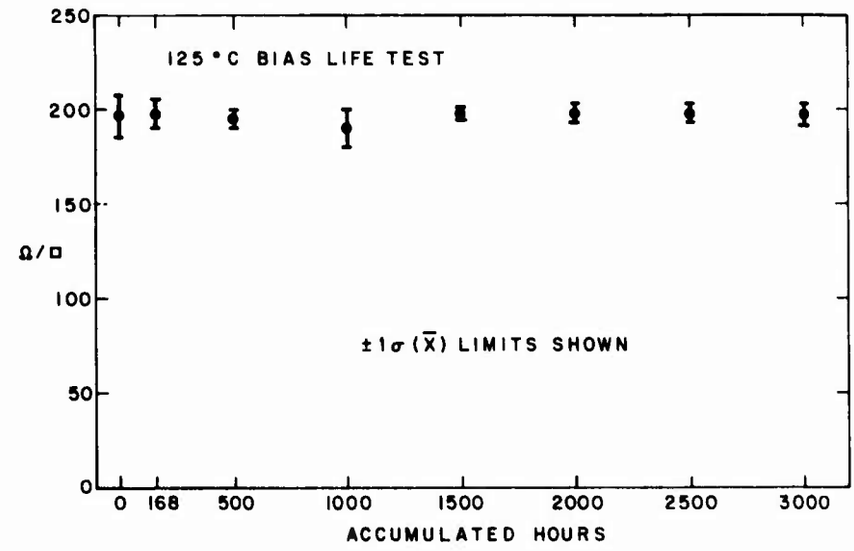


NOTE: Nanoampere data fluctuations are due to the values approaching the reproduceability limits of the automatic tester.

Figure 42. Leakage current in high-temperature storage stepped test: (a) 4007S, n = 50, (b) TCS056, n = 25, (c) TC1092, n = 25. $\bar{X} \pm 1$ sigma data.

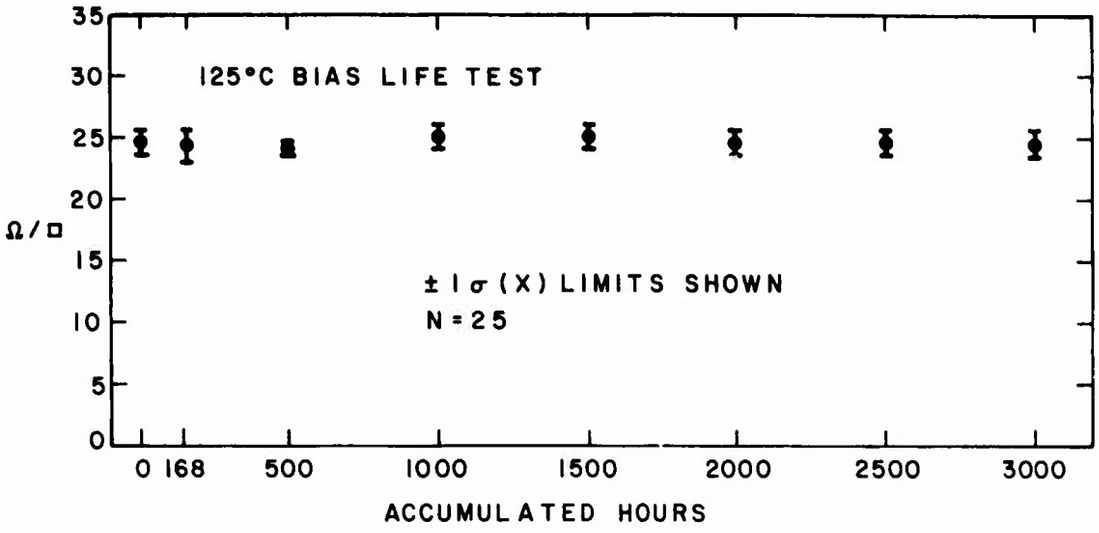


(a)

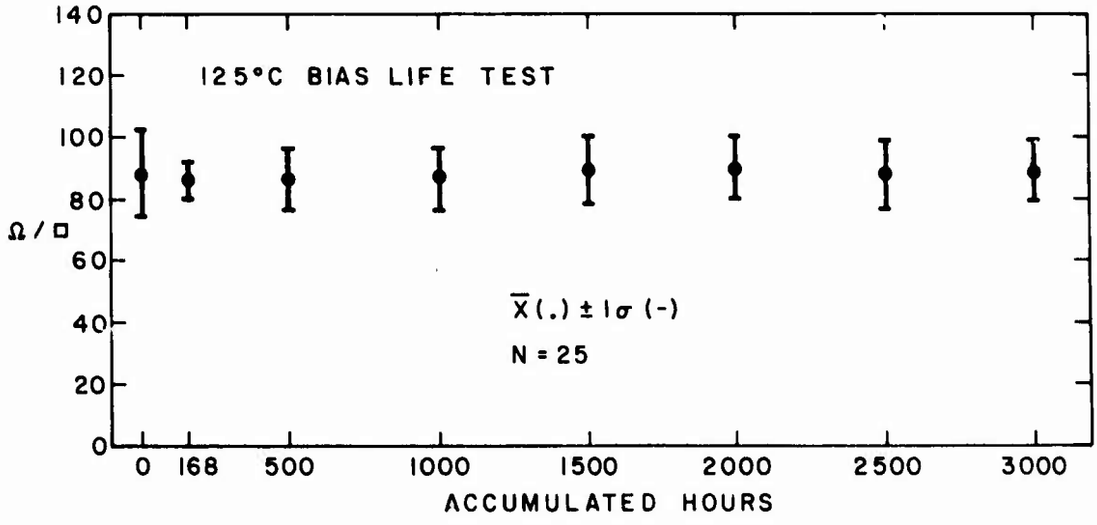


(b)

Figure 43. Bias life test at 125°C, showing $\bar{X} \pm 1$ sigma trends, for TCS010 Si-gate CMOS/SOS test array resistance (Ω/□) of (a) p^+-doped polysilicon vs time and (b) n^+-doped polysilicon vs time.

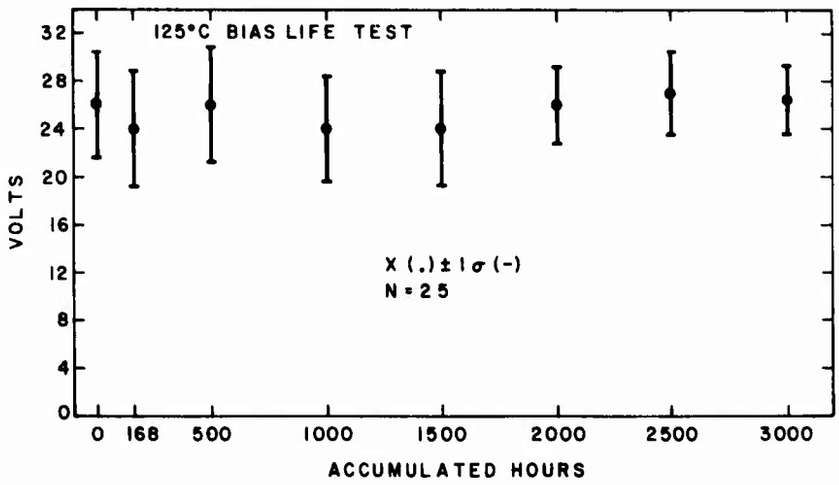


(a)

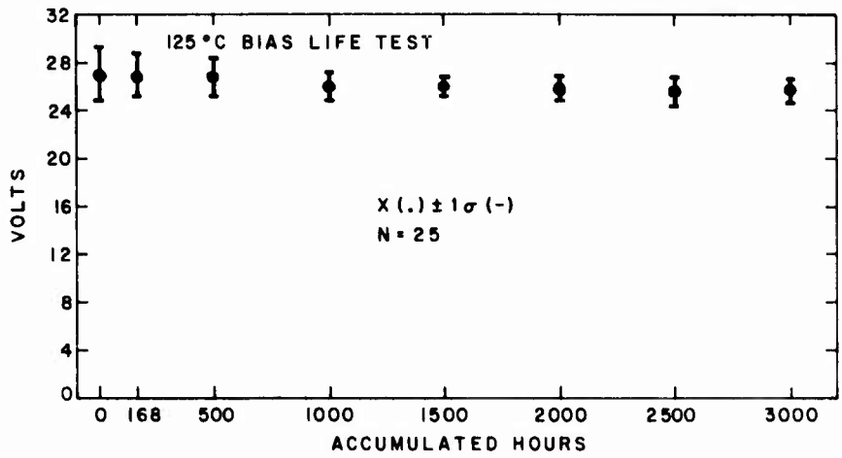


(b)

Figure 44. Bias life test at 125°C, showing $\bar{X} \pm 1$ sigma trends, for TCS010 Si-gate CMOS/SOS test array resistance (Ω/□) of (a) p^+-doped n-epitaxial silicon vs time and (b) n^+-doped p-epitaxial silicon vs time.

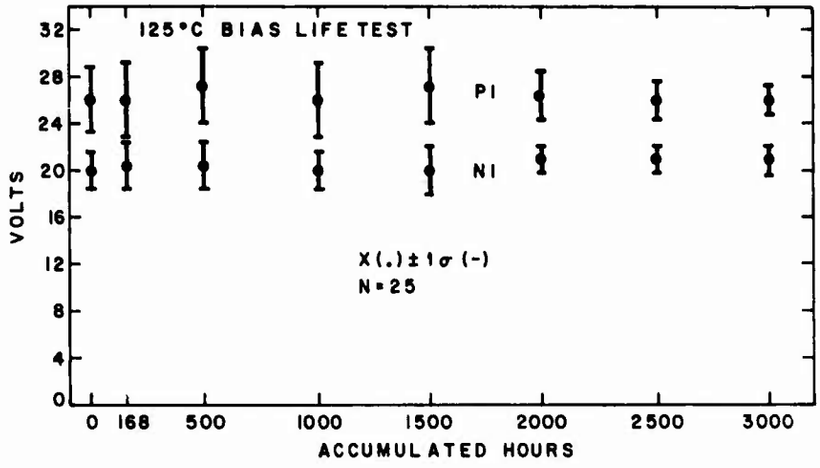


(a)

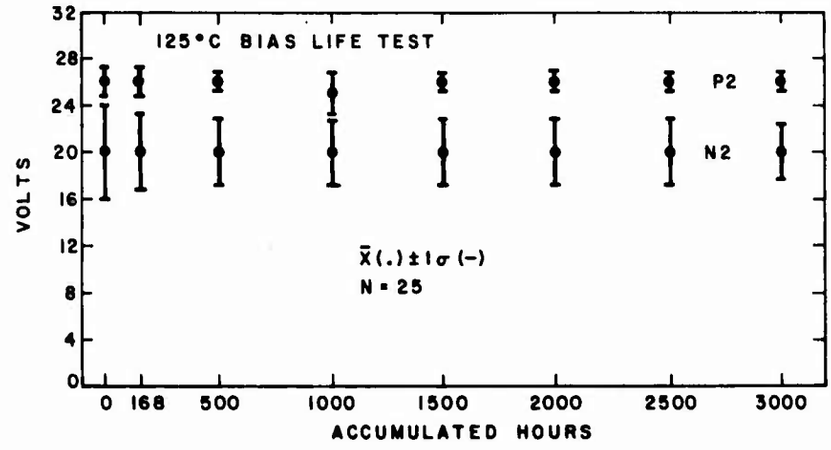


(b)

Figure 45. Bias life test at 125°C, showing $\bar{X} \pm 1$ sigma trends, for TCS010 Si-gate CMOS/SOS test array for 10-μA BV_{ds} vs time: (a) N3 transistor and (b) P3 transistor.



(a)



(b)

Figure 46. Bias life test at 125°C, showing $\overline{X} \pm 1$ sigma trends, for TCS010 Si-gate CMOS/SOS test array for 10-μA BV_{ds} vs time: (a) N1 and P1 transistors and (b) N2 and P2 transistors.

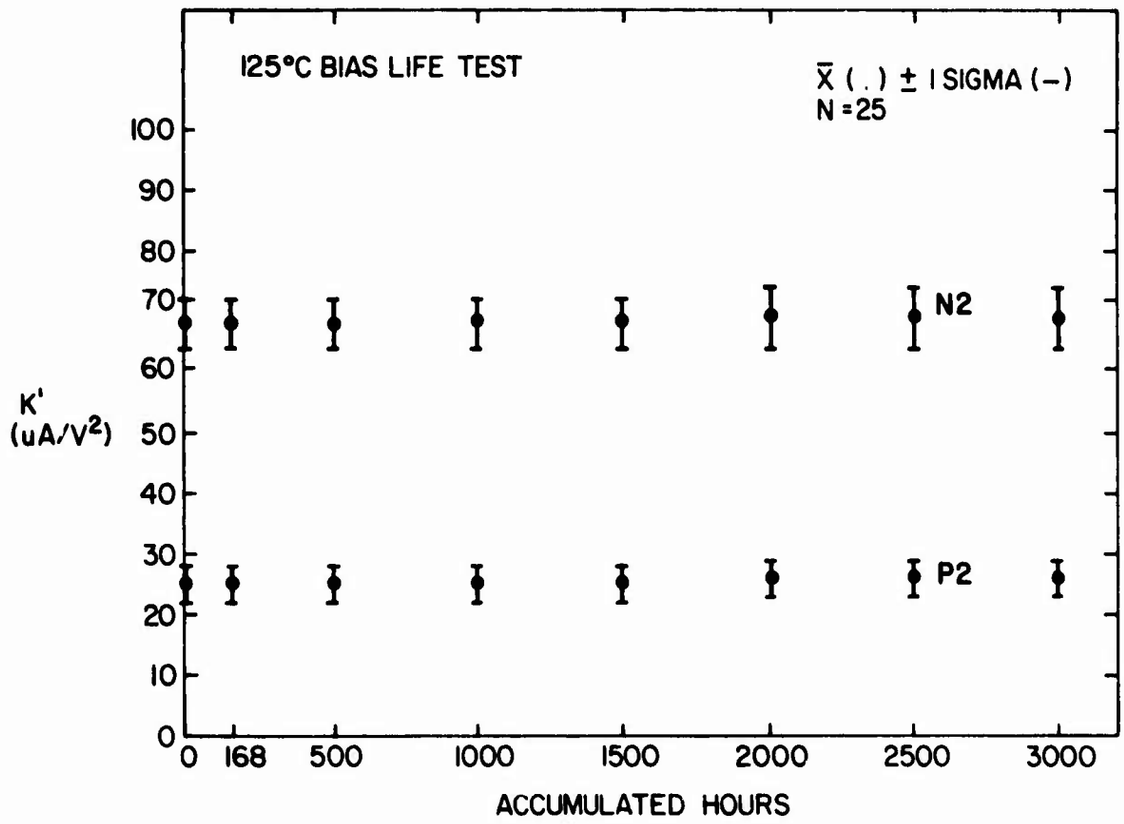


Figure 47. Bias life test at 125°C, showing $\bar{X}$ ± 1 sigma trends, for TCS010 Si-gate CMOS/SOS test array K' as a function of time for n- and p-transistor.

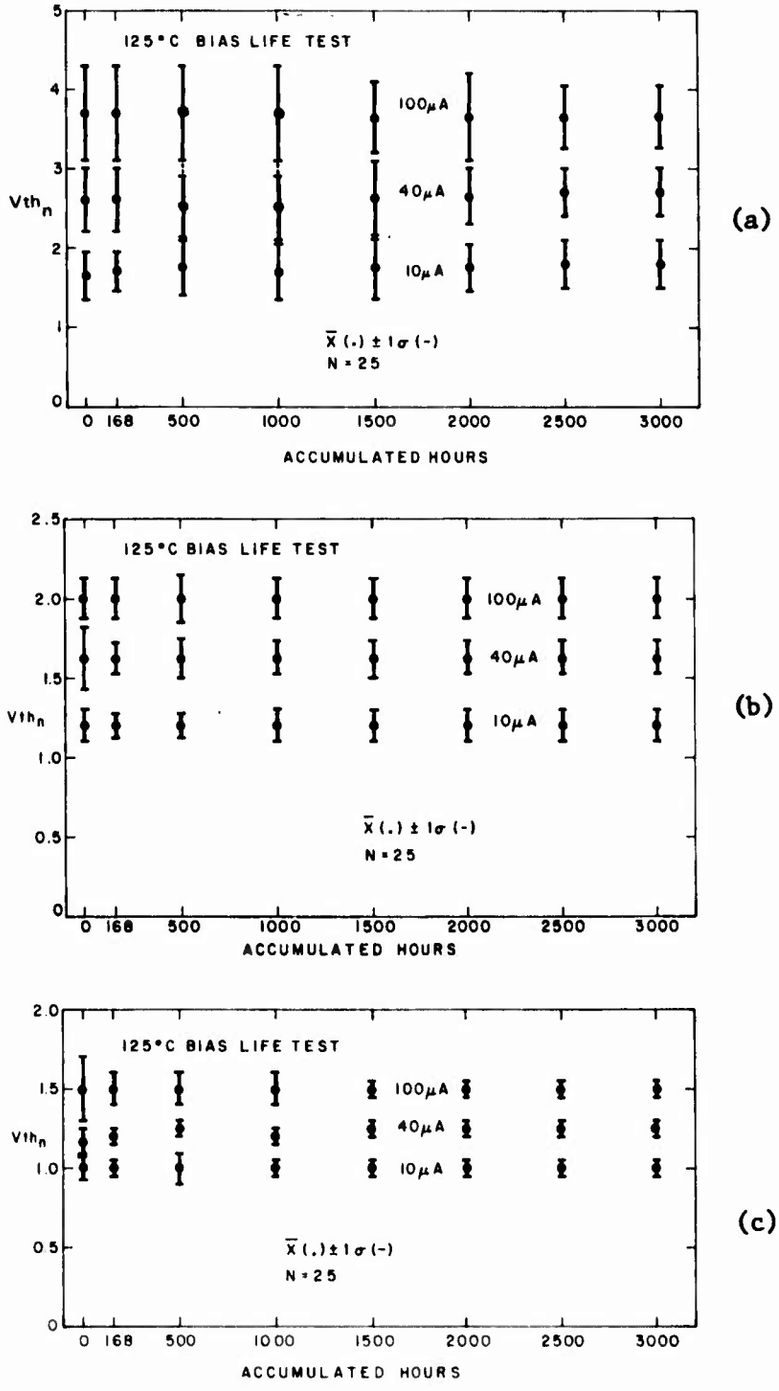
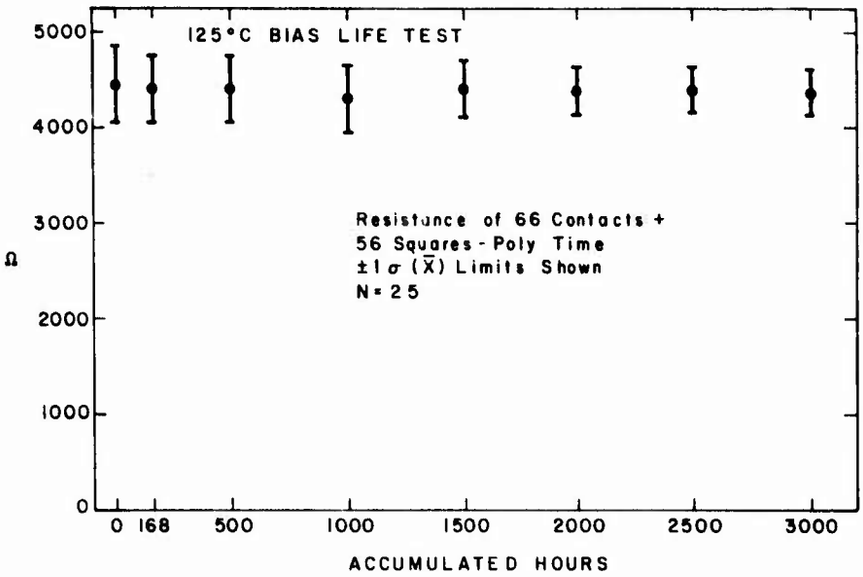
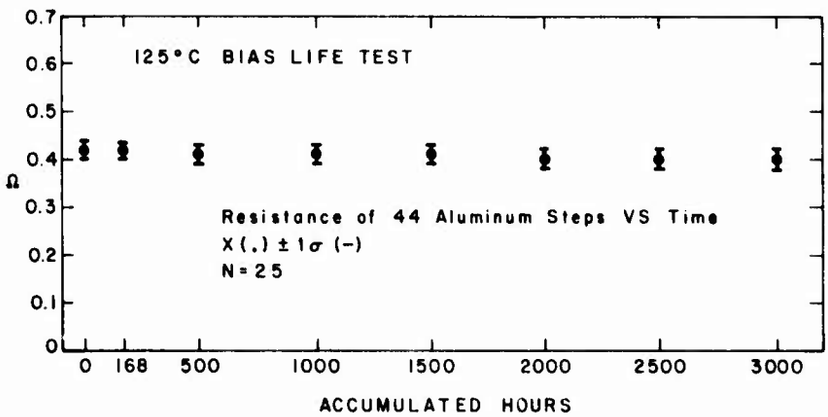


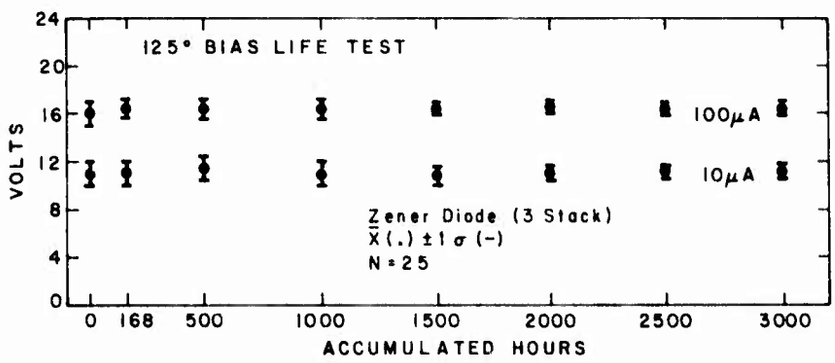
Figure 48. Bias life test at 125°C, showing $\bar{X} \pm 1$ sigma trends, for TCS010 Si-gate CMOS/SOS test array threshold vs time of (a) N1 transistor, (b) N2 transistor, and (c) N3 transistor.



(a)



(b)



(c)

Figure 49. Bias life test at 125°C, showing $\bar{X} \pm 1$ sigma trends, for TCS010 Si-gate CMOS/SOS test array resistance of (a) 66 contacts + 56 squares poly vs time and (b) 44 aluminum steps vs time (c) $\bar{X} \pm 1$ sigma trend for 3-stack Zener diode in TCS010 Si-gate CMOS/SOS test array.

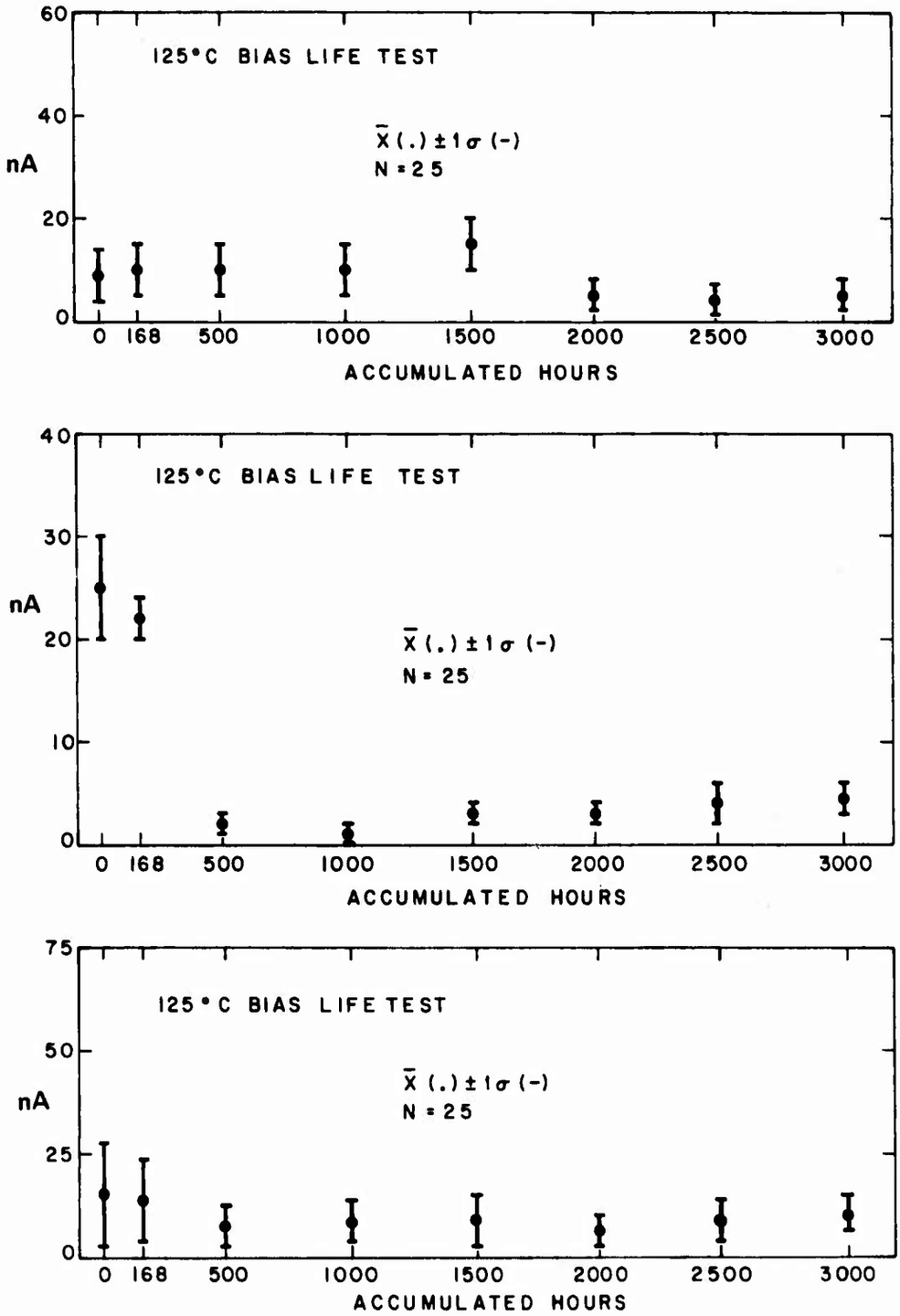


Figure 50. Bias life test at 125°C, showing $\bar{X} \pm 1$ sigma trends, for TCS010 Si-gate CMOS/SOS test array I_{DSS} at 10 V vs time: (a) N1 transistor, (b) N2 transistor, and (c) N3 transistor.

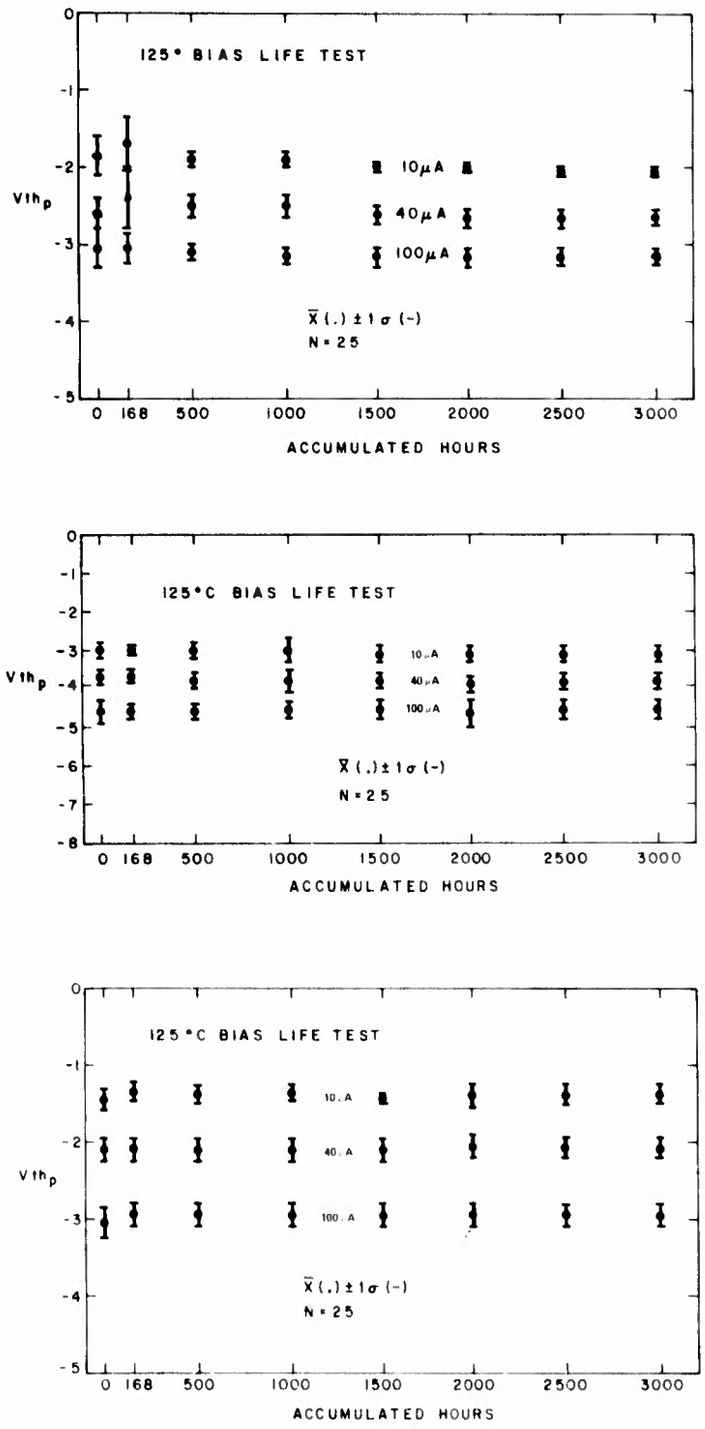
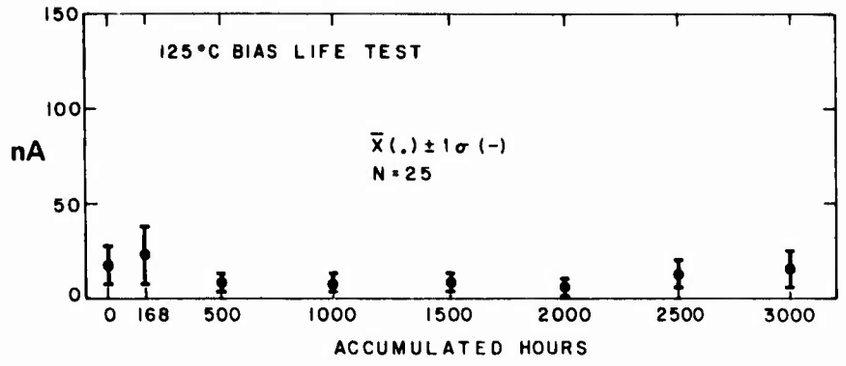
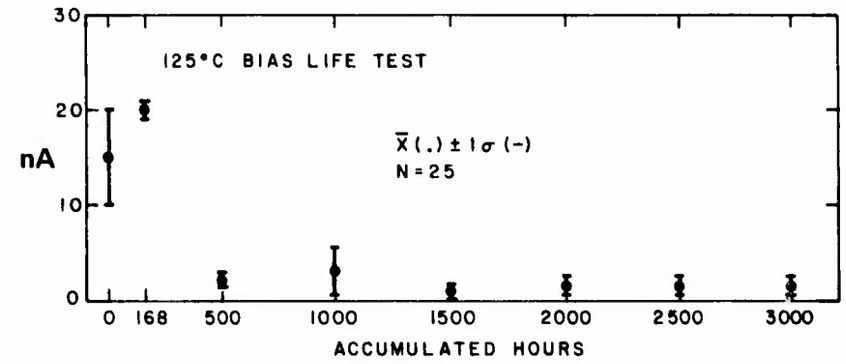


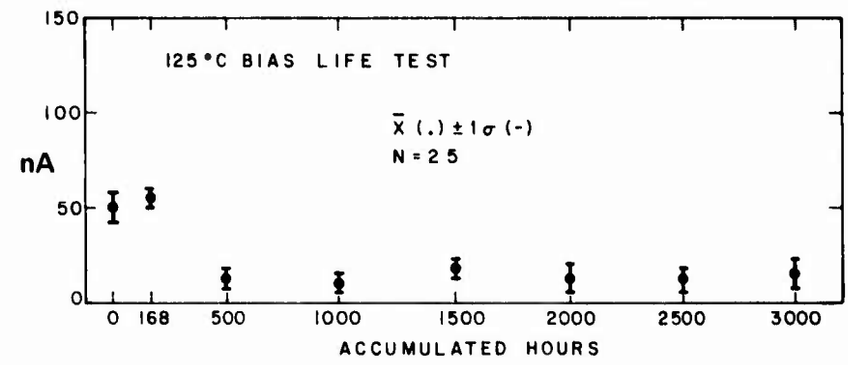
Figure 51. Bias life test at 125°C, showing $\bar{X} \pm 1$ sigma trends, for TCS010 Si-gate CMOS/SOS test array threshold vs time of (a) P1 transistor, (b) P2 transistor, and (c) P3 transistor.



(a)



(b)



(c)

Figure 52. Bias life test at 125°C, showing $\bar{X} \pm 1$ sigma trends, for TCS010 Si-gate CMOS/SOS test array I_{DSS} at 10 V vs time: (a) P1 transistor, (b) P2 transistor, and (c) P3 transistor.

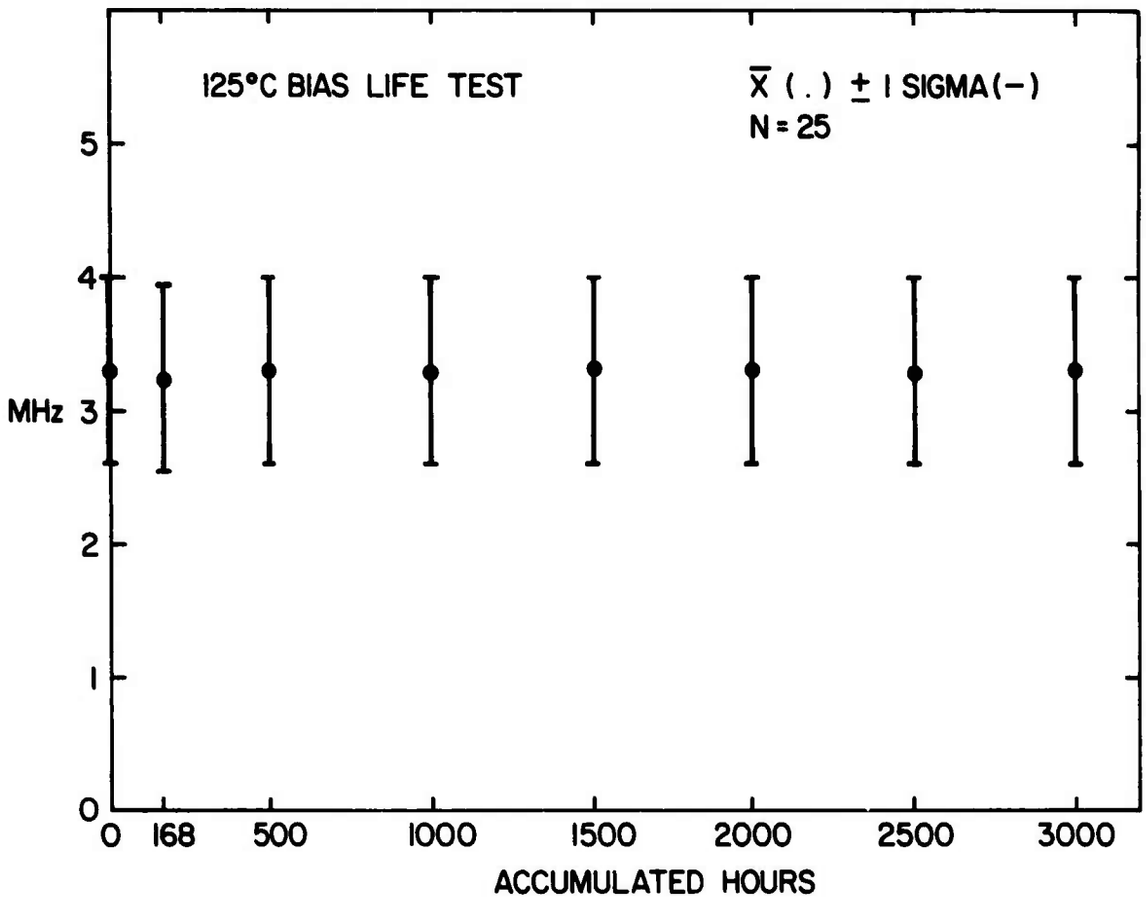


Figure 53. Bias life test at 125°C, showing $\bar{X} \pm 1$ sigma trends, for TCS010, Si-gate CMOS/SOS test array ring oscillator frequency as a function of time.

XII. FAILURE ANALYSIS

A major objective of this study was to define and identify any failure modes or mechanisms observed during the stress test program. Both catastrophic (nonfunctional) and parametric (degraded beyond specification limits) failures were identified during the failure analysis. The thermal shock and temperature cycling with intermittent bias stress tests generated catastrophic type failures associated with process-related defects as well as "end-of-life" failures caused by the weaker dielectric at the epitaxial island edge regions. The catastrophic failures caused by process-related defects all occurred during the first 10 cycles of thermal shock and 50 cycles of temperature cycling with intermittent bias, indicating clearly that these failures can be effectively screened. The edge-related failure mechanism that occurred after extended thermal shock stressing was common to both technologies. A detailed explanation of this edge-phenomenon is given in Appendix B. The remainder of this Section is devoted to failure analyses reports typifying both the process-related and "end-of-life" failure mechanisms.

A. PROCESS-RELATED FAILURES

1. Serial #51 (TC1092) Si-Gate. This unit failed the thermal shock test at 10 cycles. Its failure mode was an open N3-P3 inverter. To verify the failure, the unit was tested for hermeticity (MIL-STD-883, Method 1014 A, C_1, C_2) and found to be satisfactory. It was then "delidded" and examined on the SEM using the voltage contrast mode. Figure 54 shows the voltage on the drain terminal stopping at the epi-island edge. Figure 55 shows the cracked metal condition observed at the failure site. The failure mechanism was due to poor metal coverage over the island edge step.

2. Serial #98 (TC1092) Si-Gate. This unit failed the temperature cycling with intermittent bias test at 10 cycles. The failure mode was a gate-to-source breakdown of the P1 transistor at 8 V. In the failure verification, the unit was tested for hermeticity and found to be satisfactory. The unit

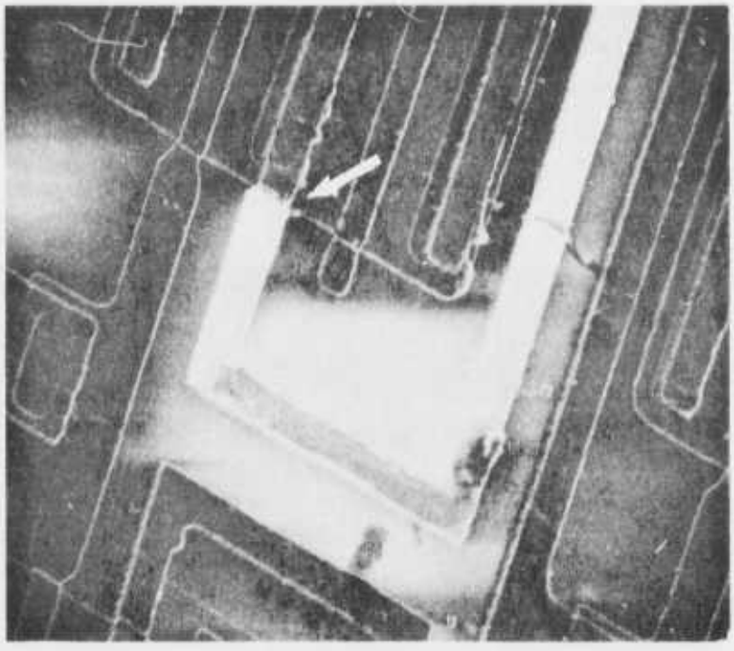


Figure 54. SEM voltage contrast mode (TC1092, #51). Pin 1 - drain terminal, open at epi-island edge.

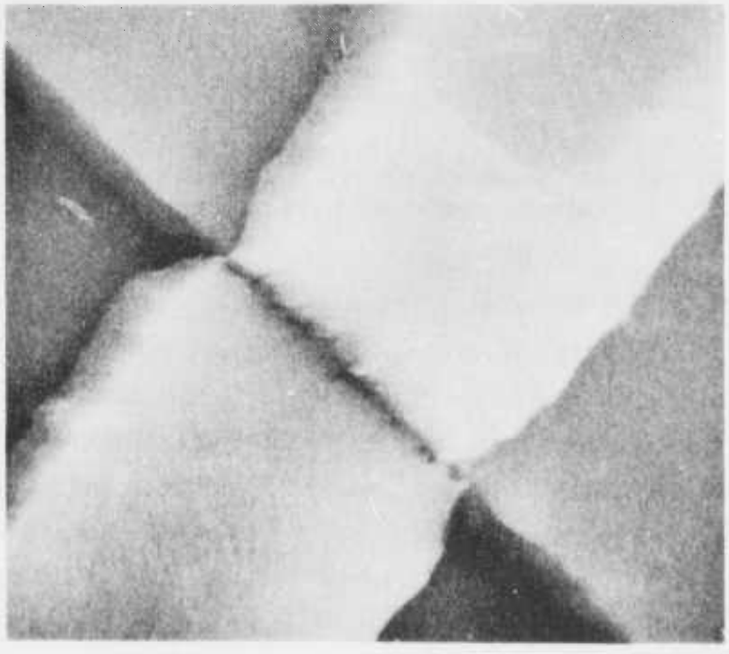


Figure 55. SEM photograph of metal discontinuity at defect site (TC1092, #51).

was then delidded and examined on the SEM using the induced current (EBIC) mode with bias applied. Figure 56 shows the induced current image obtained when the P1 and P2 gates were biased above 8 V. The arrow points to a microplasma breakdown site that is developing and increases in size as the voltage is raised. The failure mechanism is a gate oxide rupture below the polysilicon gate.

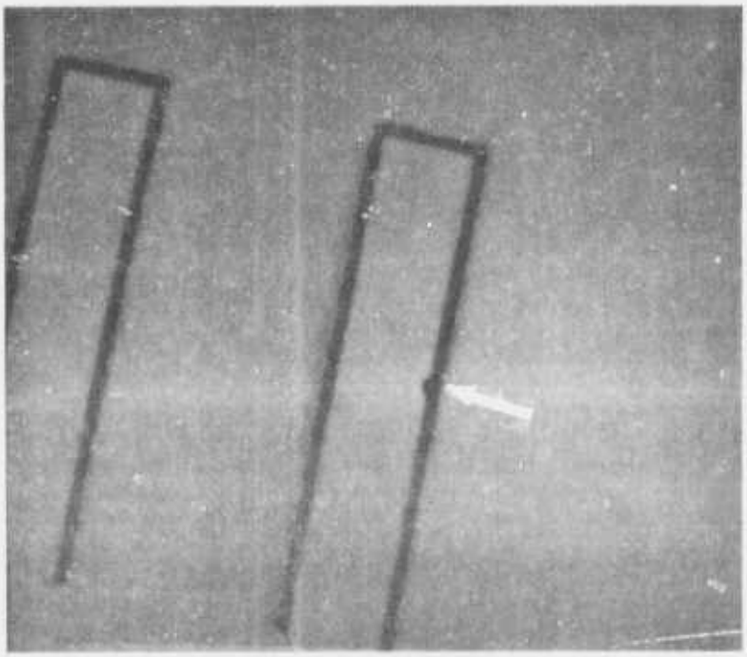


Figure 56. SEM-induced current mode with bias (TC1092, #98). Gate-so-source microplasma breakdown site.

3. Serial #6 (4007S) Al-Gate. The unit failed the temperature cycling with intermittent bias test at 50 cycles. The failure mode was a high-current breakdown gate-to-source of the P1 transistor. For failure verification the unit was tested for hermeticity (MIL-STD-883 Method 1014 A, C_1, C_2) and found to be satisfactory. The unit was then delidded and analyzed using the liquid-crystal *ac* field-effect technique. Figure 57 shows the thermal effect observed during the liquid-crystal analysis. The liquid crystal was removed, and the failure site was examined under a metallurgical microscope. Figure 58 shows a short-circuit from gate-to-source caused by a subsurface defect in the epitaxial material (Fig. 59).

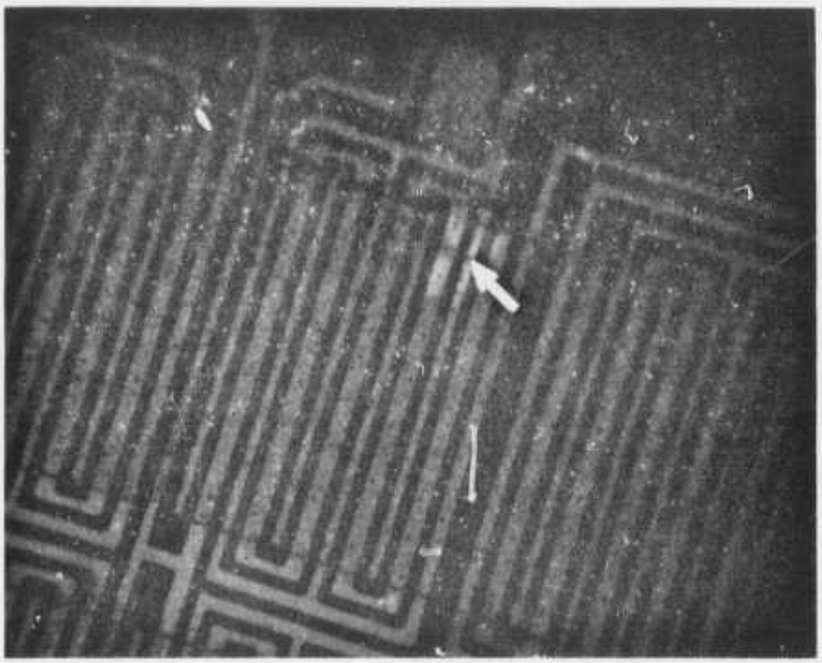


Figure 57. Liquid-crystal technique - thermal mode. P1 transistor breakdown at 0.3 V.

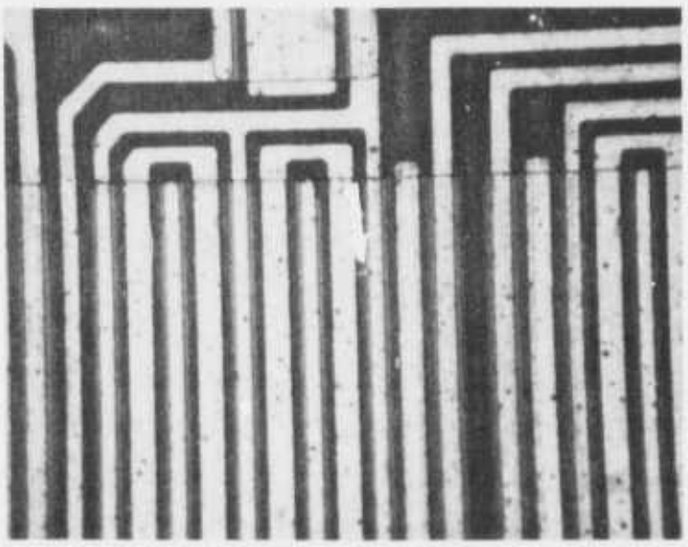


Figure 58. Short-circuit from gate-to-source metal.

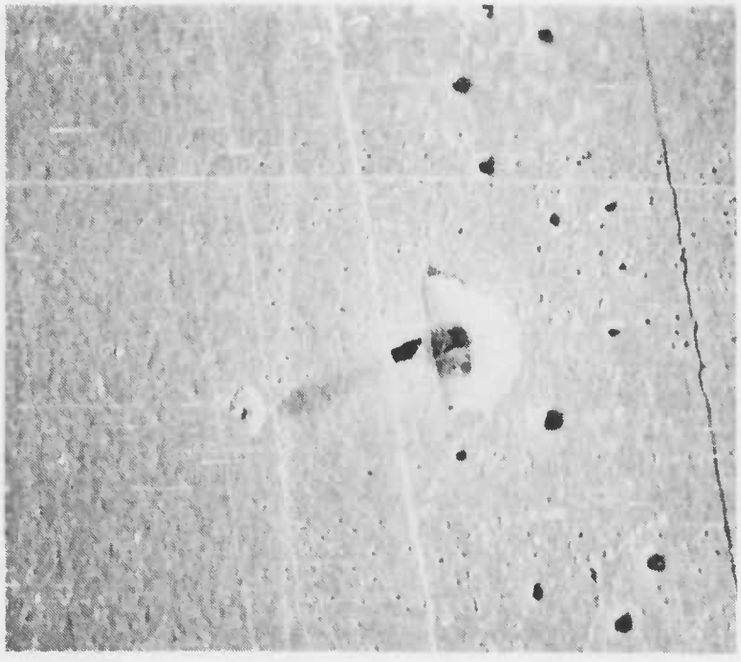


Figure 59. SEM photograph showing subsurface defect where gate-to-source short-circuit occurred.

B. "END-OF-LIFE" FAILURES

1. Serial #230 (4007S) Al-Gate. This unit failed the thermal shock test at 300 cycles. The failure mode was gate-to-source breakdown of the N1 transistor at 3 V. In failure verification, the unit passed hermeticity tests, and was then delidded and analyzed with the liquid-crystal technique. Figure 60 shows the breakdown site (thermal mode) at the epitaxial island edge.

2. Serial #33 (TCS056) Si-Gate. This unit failed the thermal shock test at 300 cycles. The failure mode was gate-to-source breakdown of the N2 transistor at 2 V.

In failure verification, the unit passed hermeticity tests, was delidded, and analyzed using the liquid-crystal *ac* field-effect technique. Figure 61 shows the breakdown site (thermal mode) at the epitaxial island edge.

Failure analysis indicated a predominance of gate-to-source short-circuits while very few gate-to-drain short-circuits were noted. This is due to the bias configurations leaving drain connections floating in most of the stress tests.

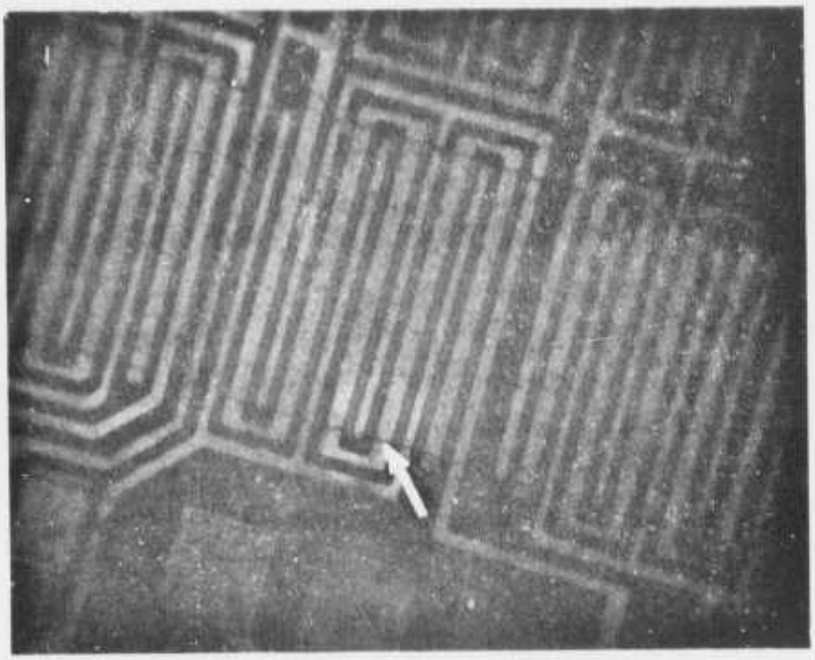


Figure 60. Gate-to-source breakdown, N1 transistor liquid-crystal technique (4007S, #230).

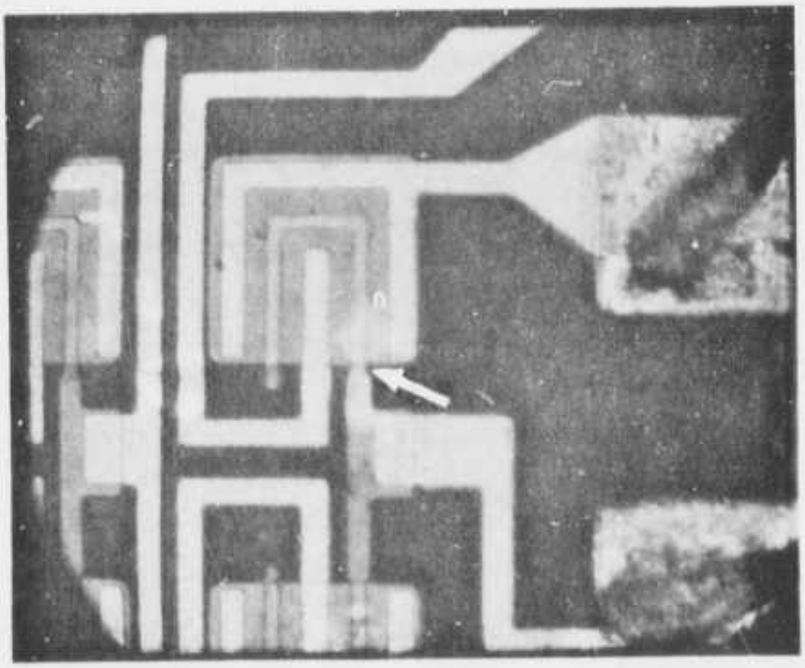


Figure 61. Edge-related gate-to-source breakdown in transistor TCS056, #33.

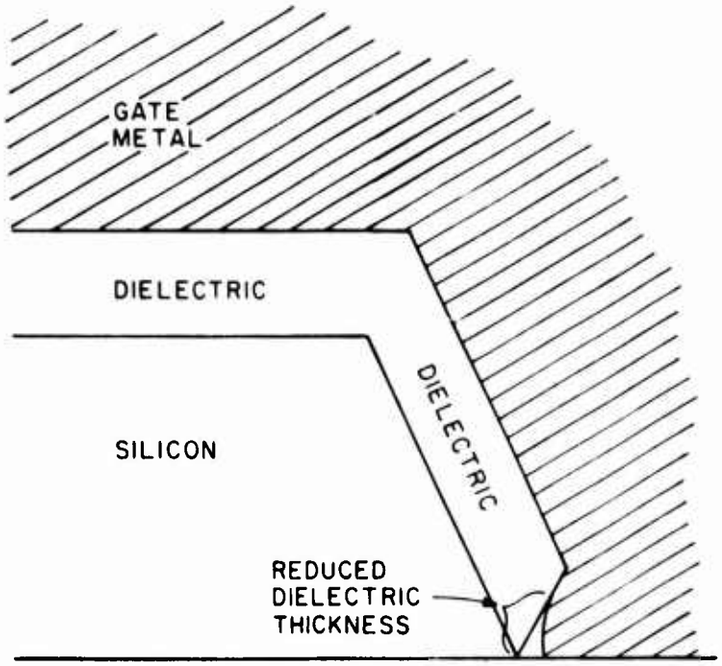
XIII. PREDOMINANT FAILURE MODES AND MECHANISMS

Different failure modes were observed during the stress test program for the two processes. The predominant failure mode for the Al-gate technology was the depletion mode operation of the n-transistor ($V_{thN} \leq 0$ V), causing high leakage current. Si-gate processed arrays failed because of p-transistor thresholds increasing in absolute value. (For this program, a p-transistor threshold failure was defined as < -2.6 V, although much greater threshold values could be tolerated before circuit function was affected.) The Si-gate threshold voltage failures were bake-recoverable (200°C, 1 h, no bias) while the Al-gate leakage failures were not. A summary of failures resulting from the stress-test program is given in Table 15. A detailed listing of all failures is given in Appendix A.

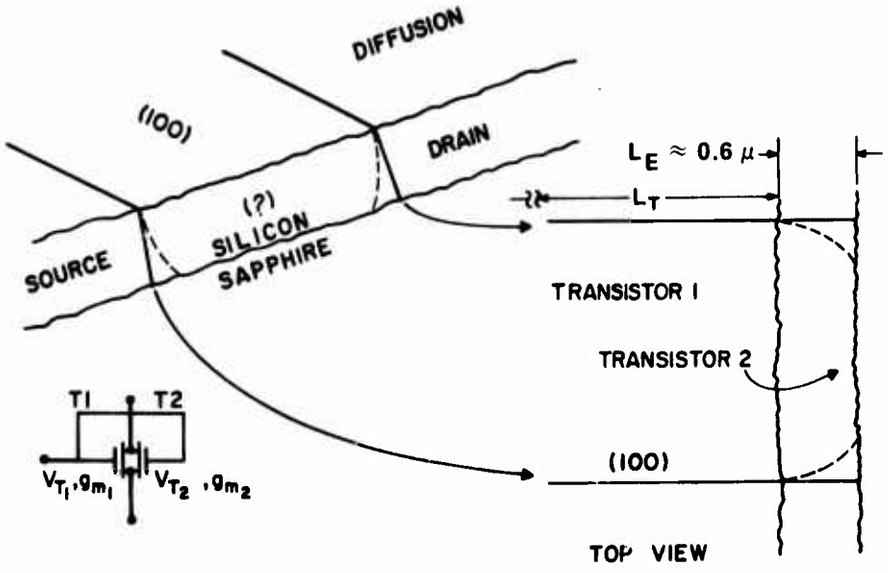
Most of the high-leakage-current failures in the Al-gate arrays were caused by a weak dielectric at the Si-sapphire interface. While both the Al-gate and the self-aligned Si-gate technologies have their n- and p-transistors defined on separate epitaxial-Si-island structures, the wafer processing involved makes the Al-gate devices more susceptible to this type of failure. During the processing of the Si-gate arrays, the polysilicon-gate is deposited immediately after the channel oxide is defined. This is the only oxidation step after the islands are defined. In contrast, the Al-gate process has three oxidation steps after the islands are defined. Each oxidation typically consumes 440 Å of Si for each 1000 Å of oxide grown. As this operation is repeated, the island-edge sapphire interface is degraded (see Fig. 62). The measured dielectric breakdown voltage of the arrays (typical values were 22 to 24 V for Al-gate and 65 to 75 V for self-aligned Si-gate arrays) confirmed the weakness of the Al-gate process. The epitaxial island edge structure comprises a separate transistor that is electrically in parallel with the primary transistor (see Fig. 62). This parasitic transistor has higher leakage, lower conductivity, and lower threshold voltage due to different mobility and crystallographic orientation. The effect of the edge transistor on device performance was studied using a logarithmic picoammeter to measure the drain current as a function of gate voltage. Figure 63 is a typical "Log-Picoammeter" plot of a good Al-gate transistor prior to the stress-test program and of a similar device after 4000 h

TABLE 15. FAILURE MODE SUMMARY

Test	Circuit Type	Principal Failure Mode
Static Bias Temp Stress (150° to 250°C) (No Load)	4007S	Depletion mode operation, n-transistor (edge-transistor leakage increases)
	TCS056 & TC1092	p-transistor threshold increases < -2.6 V.
Bias Power Temp Stress (85° to 175°C) (Loaded)	4007S	Same failure modes as static bias subgroup.
	TCS056 & TC1092	
Temp Cycling with Intermittent Bias -55° to 125°C 1000 Cycles	4007S	One gate-to-source edge-related and two gate-to-source non-edge-related breakdowns in first 50 cycles.
	TCS056	No failures.
	TC1092	Three failures - gate-to-source breakdowns.
Operational Life 125°C	4007S	Depletion mode operation, n-transistor (edge-transistor leakage increases) on 46 of 50 units subjected to test. Most failures occur after 3000 h.
	TCS056	2 Failures - both N1 transistor gate-to-source breakdowns, 1 at 3000 h and 1 at 4000 h.
	TC1092	2 Failures - both have p-transistor threshold < -2.6 V 1 at 3000 h and 1 at 4000 h.
Thermal Shock -65° to 150°C	4007S, TCS056, TC1092	Edge-related gate-to-source breakdowns (at, or beyond, 300 cycles).
High-Temp Storage Stress 150° to 300°C	4007S	26 of 50 show edge-transistor leakage current increases in the 300°C cell.
	TCS056 & TC1092	Depletion mode operation, n-transistor on 8 TCS056's and 1 TC1092.



(a)



(b)

Figure 62. (a) Degradation of island-edge sapphire interface and (b) schematic diagram of edge transistor.

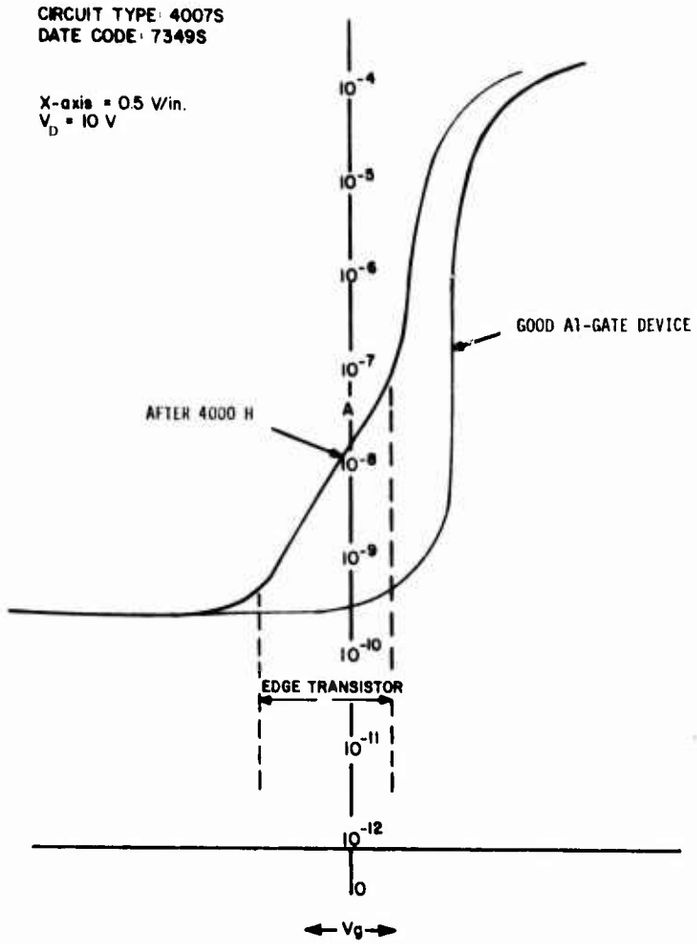


Figure 63. Log-picoammeter plot of good Al-gate transistor prior to stress-test program and after 4000-h operational life test at 125°C.

operating life test at 125°C. The plot shows that the edge transistor leakage current increased and also demonstrates the effect of the parasitic transistor threshold voltage on the overall threshold voltage.

Most of the self-aligned Si-gate device failures were due to p-transistor threshold voltage increase. Since this is a parametric rather than a catastrophic failure mechanism and was bake recoverable, the Si-gate CMOS/SOS process was analyzed to determine the cause of this type of failure. In the self-aligned Si-gate process, the n-transistor had a 700-Å layer of phosphorus-doped oxide over the polysilicon gate, followed by a 700-Å layer of boron-doped oxide and a 5000-Å undoped capping oxide. The p-transistor only had the boron-doped oxide (700 Å) and the undoped cap (5000 Å) over

the gate. These deposited oxides provide the dopants for the source-drain diffusions. When mobile ions (e.g., Na) exist in the channel, they would tend to affect both transistors. The postulated mechanism for affecting only the p-device is a "gettering" effect caused by the phosphorus-doped oxide over the n-transistor preventing mobile ions outside the channel dielectric from migrating into the active channel region. Since this phosphorus glass is not over the p-transistor, the p-transistor could exhibit threshold voltage shift independent of the n-transistor.

XIV. CONCLUSIONS AND DISCUSSION

A. CONCLUSIONS

(1) The results of this study show that the self-aligned Si-gate technology can achieve a median life of 72,000 h at 125°C.

(2) The Al-gate technology demonstrated a 7500-h median life at 125°C.

(3) The poorer reliability results for the Al-gate devices may have been due to the particular manufacturer's process that resulted in inherently weak dielectric strength of the channel oxide as it extends over the epi-island edge. The poor quality, due to the procuring circumstances, was also a cause.

(4) "Infant mortality" failures due to process-related defects are screenable.

(5) Edge-transistor related reliability problems can be minimized by using the self-aligned Si-gate technology.

(6) No electrostatic discharge failures attributable to handling were encountered during the entire test program. It must be pointed out that the results demonstrated for the TCS056 Si-gate technology were achieved on arrays that did not incorporate complete static voltage input protection.

(7) The stacked Zener-diode type of input-protection network causes increased power dissipation and should not be used for large-scale integrated (LSI) circuits.

(8) Metallization step coverage of the epitaxial islands does not appear to be a reliability problem for the simple structures evaluated in this program, but improvements are necessary in order to meet MIL-M-38510 metallization inspection requirements.

(9) The use of accelerated bias-temperature ($\geq$ 250°C) screening as an indicator of device reliability is not recommended for epoxy-mounted arrays. Catastrophic failures and variation of device parameters may result from the effects of additional epoxy curing at temperatures at or in excess of the cure temperature.

XV. RECOMMENDATIONS

Based upon the stress program results, RCA/SSTC suggests the following tests as part of a high-reliability screening procedure for CMOS/SOS:

(1) 168-h static-bias burn-in at 125°C.

Since no failures occurred during the initial 2000 h of the 125°C operational life test, it was felt that the 168-h static-bias burn-in performed during the pre-stress program screening procedure effectively eliminated all "early life" failures.

(2) Thermal shock, 10 cycles, -65° to 150°C, liquid to liquid.

(3) Temperature cycling with intermittent bias, 50 cycles, -55° to 125°C.

Based on data obtained from arrays processed with more recent RCA technology, the reliability of self-aligned Si-gate CMOS/SOS devices can be further improved by:

(1) Substitution of ion-implantation of the source-drain electrodes for the boron- and phosphorus-doped oxides, which eliminates the condition where the boron-doped oxide is in intimate contact with the channel insulator.

(2) Use of low-leakage gated-diode input-protection networks (input to V_{DD} and V_{SS}) combined with large-area V_{DD} to V_{SS} protective diodes.

(3) Use of enclosed-type transistor geometries to minimize edge transistor related failures.

BIBLIOGRAPHY

D. W. Flatley and W. E. Ham, "Edge Related Instabilities in SOS/MOS Transistors," unpublished.

W. E. Ham "Physical Structure and Radiation Behavior of the Silicon on Sapphire Island Edge," unpublished.

W. E. Ham "Leakage Current in Silicon on Sapphire Enhancement Mode Transistors," unpublished.

S. Cohen and J. J. Fabula, "Radiation Hardened CMOS Processes," paper presented at 1976 IEEE Radiation Effects Conference, San Diego, California.

D. S. Woo, S. G. Policastro, and H. Borkan, *Manufacturing Methods for Silicon Devices on Insulating Substrates, Quarterly Report III*, Technical Report #AFML-IR-516-3, April 30, 1974.

G. L. Balle, "Current Detector," unpublished.

APPENDICES

APPENDIX A

FAILURE DATA FOR STRESS-TEST PROGRAM

Stress Test Failed	Device Type	When Failure Occurred	Unit #	Transistor Failed	Failure Mode
Thermal Shock	TC1092	10 cycles	51	P2	Metal discontinuity over epitaxial island edge
	4007S	10 cycles	260	N1	Gate-to-source edge related breakdown
	TCS056	300 cycles	33	N2	Edge related gate-to-source breakdown
	TCS056	300 cycles	30	P1	Edge related gate-to-source breakdown
	TCS056	300 cycles	38	N1	Edge related gate-to-source breakdown
	TCS056	300 cycles	29	P1	Edge related gate-to-source breakdown
	TC1092	300 cycles	50	P1	Edgre related gate-to-source breakdown
	4007S	300 cycles	230	N1	Edge related gate-to-source breakdown
	TCS056	400 cycles	35	N1	Edge related gate-to-source breakdown
Temperature Cycling	TC1092	10 cycles	98	P1	Gate-to-drain breakdown
	TC1092	10 cycles	112	P1	100 μA I_L gate to source
Intermittent Bias	TC1092	50 cycles	109	N1	Gate-to-source breakdown
	4007S	50 cycles	57	Pkg. Pin 8	Broken package pin - probable handling failure
	4007S	50 cycles	9	N1 - P1	Damaged epi-gate-to-source breakdown (2 failure sites)
	4007S	50 cycles	6	P1	Defect in epi-gate-to-source breakdown
	4007S	50 cycles	98	N1	Edge related gate-to-source breakdown
High-Temperature Storage Stress (Stepped)	4007S	500 h (250°C)	134	P3	Edge related gate-to-source breakdown
	TC1092	500 h (250°C)	22	N2	Gate-to-source breakdown
	4007S	24 h (250°C)	106	N1	Gate-to-source breakdown
	TC1092	24 h (250°C)	30	P1	Edge related gate-to-source breakdown
	TC1092	250 h (300°C)	97	All "N" devices	V_{th} "N" $\leq$ 0 V
	TCS056	750 h (300°C)	19	N1	Depletion mode N device
	TCS056	750 h (300°C)	6	All "N" devices	Depletion mode N device
	TCS056	750 h (300°C)	4	All "N" devices	Depletion mode N $V_{th} \leq 0$ V
	TCS056	750 h (300°C)	7	All "N" devices	Depletion mode N $V_{th} \leq 0$ V
	TCS056	750 h (300°C)	5	N1	Depletion mode N $V_{th} \leq 0$ V
	TCS056	250 h (300°C)	21	N1	High leakage gate-to-source breakdown
	TCS056	750 h (300°C)	8	N1	Depletion mode N $V_{th} \leq 0$ V
	TCS056	1000 h (300°C)	18	All "N" devices	Depletion mode N $V_{th} \leq 0$ V
	4007S	500 h (300°C)	156	N2	Edge transistor leakage
	4007S	750 h (300°C)	170	N2	Edge transistor leakage
	4007S	500 h (300°C)	205	N2	Edge transistor leakage
	4007S	500 h (300°C)	112	N1 + N2	Edge transistor leakage

FAILURE DATA FOR STRESS-TEST PROGRAM (Continued)

Stress Test Failed	Device Type	When Failure Occurred	Unit #	Transistor Failed	Failure Mode
High-Temperature Storage Stress (Stepped)	4007S	500 h (300°C)	175	N1	Edge transistor leakage
	4007S	500 h (300°C)	148	N2	"
	4007S	500 h (300°C)	132	N1 + N2	"
	4007S	500 h (300°C)	119	N1	"
	4007S	500 h (300°C)	130	All "N" devices	"
	4007S	500 h (300°C)	123	N1 + N3	"
	4007S	500 h (300°C)	211	All "N" devices	"
	4007S	750 h (300°C)	152	N3	"
	4007S	750 h (300°C)	124	N1	"
	4007S	500 h (300°C)	204	N3	"
	4007S	500 h (300°C)	195	N3	"
	4007S	500 h (300°C)	196	N3	"
	4007S	500 h (300°C)	178	N1	"
	4007S	750 h (300°C)	164	All "N" devices	"
	4007S	1000 h (300°C)	171	All "N" devices	"
	4007S	1000 h (300°C)	150	All "N" devices	"
	4007S	1000 h (300°C)	182	All "N" devices	"
	4007S	500 h (300°C1)	104	All "N" devices	"
	4007S	500 h (300°C)	107	All "N" devices	"
	4007S	500 h (300°C)	114	All "N" devices	Edge transistor leakage "
	4007S	500 h (300°C)	133	All "N" devices	"
	4007S	500 h (300°C)	136	All "N" devices	"
Operational Life	TCS056	3000 h	56	N1,P1, P3	Breakdown P $\leq$ -2.6 V
	TCS056	4000 h	60	N1	Breakdown gate-source
	TC1092	4000 h	80	P1,P3	"P" $V_{th} \leq$ -2.6 V
	TC1092	3000 h	77	P1	"P" $V_{th} \leq$ -2.6 V
	4007S	1000 h	395	All "N" devices	Edge transistor leakage
	4007S	3000 h	392	All "N" devices	"
	4007S	4000 h	391	All "N" devices	"
	4007S	2000 h	355	All "N" devices	"
	4007S	4000 h	354	All "N" devices	"
	4007S	3000 h	351	All "N" devices	"
	4007S	4000 h	403	All "N" devices	"
	4007S	4000 h	385	All "N" devices	"
	4007S	4000 h	297	N1	Edge transistor leakage
	4007S	3000 h	372	N1,N2	"
	4007S	3000 h	386	N1,N3	"
	4007S	4000 h	420	All "N" devices	"
	4007S	4000 h	414	All "N" devices	"
	4007S	3000 h	330	All "N" devices	"
	4007S	4000 h	349	All "N" devices	"
	4007S	4000 h	342	All "N" devices	"
	4007S	4000 h	341	All "N" devices	"
	4007S	3000 h	333	All "N" devices	"
	4007S	4000 h	309	All "N" devices	"
	4007S	4000 h	350	All "N" devices	"
	4007S	4500 h	283	All "N" devices	"
	4007S	4000 h	346	All "N" devices	"
	4007S	4000 h	358	All "N" devices	"
	4007S	4000 h	360	All "N" devices	"
	4007S	4000 h	366	All "N" devices	"
	4007S	4000 h	367	All "N" devices	"
	4007S	4000 h	374	All "N" devices	"
	4007S	4000 h	375	All "N" devices	"

FAILURE DATA FOR STRESS-TEST PROGRAM (Continued)

Stress Test Failed	Device Type	When Failure Occured	Unit #	Transistor Failed	Failure Mode
Operational Life	4007S	4000 h	379	All "N" devices	Edge transistor leakage
	4007S	3000 h	387	"	"
	4007S	4000 h	294	"	"
	4007S	4500 h	296	"	"
	4007S	4500 h	317	"	"
	4007S	4500 h	321	"	"
	4007S	4500 h	324	"	"
	4007S	4500 h	373	"	"
	4007S	5000 h	382	"	"
	4007S	5000 h	312	"	"
	4007S	5000 h	337	"	"
	4007S	5000 h	359	"	"
	4007S	5000 h	397	"	"
	4007S	5000 h	402	"	"
	4007S	5000 h	409	"	"
	4007S	5000 h	412	"	"
	4007S	5000 h	423	"	"
Static Bias-Temperature Stress 250°C	4007S	4 h	455	N1	Edge transistor leakage
	4007S	4 h	438	N1,N2	"
	4007S	4 h	443	N1,N2,N3	"
	4007S	4 h	439	N1,N2	"
	4007S	4 h	450	N1,N2	"
	4007S	4 h	428	N1	"
	4007S	4 h	427	N2	"
	4007S	6 h	431	N2	"
	4007S	7 h	432	N1,N3	"
	TC1092	4 h	119	All "P" devices	V_{th} "P" $\leq$ -2.6 V
	TC1092	4 h	121	P3	"
	TC1092	26 h	120	All "P" devices	"
	TCS056	4 h	93	P2,P3	"
	TCS056	6 h	94	P2	"
	TCS056	30 h	92	P2	"
Static Bias-Temperature Stress 225°C Cell	4007S	5 h	635	All "N" devices	Edge transistor leakage
	4007S	5 h	633	All "N" devices	"
	4007S	5 h	627	N1	"
	4007S	10 h	623	All "N" devices	"
	4007S	10 h	626	All "N" devices	"
	4007S	10 h	610	N1	"
	4007S	10 h	608	N1	"
	TC1092	10 h	162	P2,P3	V_{th} "P" $\leq$ -2.6 V
	TC1092	65 h	161	P2,P3	"
	TC1092	65 h	160	P2,P3	"
	TCS056	105 h	136	P1	"
	TCS056	105 h	137	P1,P2	"
	TCS056	105 h	139	P1	"
	TCS056	105	138	P1	"
Static Bias-Temperature Stress 200°C Cell	4007S	32 h	498	N2	Edge transistor leakage
	4007S	32 h	496	All "N" devices	"
	4007S	32 h	493	All "N" devices	"
	4007S	32 h	538	All "N" devices	"
	4007S	60 h	517	All "N" devices	"
	4007S	60 h	491	N2	"
	4007S	60 h	489	All "N" devices	"
	TC1092	40 h	130	P2,P3	V_{th} "P" $\leq$ -2.6 V
	TC1092	100 h	128	All "P" devices	"
	TC1092	100 h	129	P3	"
	TCS056	150 h	106	All "P" devices	"
	TCS056	400 h	105	P3	"
	TCS056	400 h	107	P1	"

FAILURE DATA FOR STRESS-TEST PROGRAM (Continued)

Stress Test Failed	Device Type	When Failure Occured	Unit #	Transistor Failed	Failure Mode
Static Bias-Temperature Stress 175°C	4007S	168 h	352	All "N" devices	Edge transistor leakage
	4007S	168 h	399	N1	"
	4007S	168 h	687	All "N" devices	"
	4007S	200 h	664	All "N" devices	"
	4007S	200 h	683	All "N" devices	"
	TC1092	500 h	189	P3	V_{th} "P" $\leq$ -2.6 V
Static Bias-Temperature Stress 150°C Cell	4007S	168 h	578	N2,N3	Edge transistor leakage
	4007S	168 h	571	All "N" devices	"
	4007S	168 h	568	All "N" devices	"
	4007S	168 h	569	All "N" devices	"
	4007S	168 h	570	All "N" devices	"
	4007S	168 h	566	N3	"
	TC1092	2250 h	142	P2	V_{th} "P" $\leq$ -2.6 V
	TC1092	2250 h	146	P1	10-μA leakage (gate-to-source)
Bias Power Temperature Stress 175°C Cell	4007S	35 h	476	N3	Edge transistor leakage
	4007S	35 h	471	N2	"
	4007S	35 h	466	N1	"
	4007S	100 h	458	N1	"
	4007S	100 h	480	All "N" devices	"
	4007S	100 h	474	N1	"
	TC1092	200 h	123	P1,P2	V_{th} "P" $\leq$ -2.6 V (N1 leaky)
	TC1092	300 h	124	All "P" devices	"
	TC1092	300 h	126	P1, N1	"
	TCS056	1250 h	104	P2,P3	"
	TCS056	2168 h	100	P1	"
	TCS056	2168 h	99	P1,P2	"
	TCS056	2168 h	101	P3	10-μA leakage (gate-to-source)
Bias Power Temperature Stress 150°C Cell	4007S	75 h	401	N1	Edge transistor leakage
	4007S	75 h	441	N1	"
	4007S	75 h	444	N1	"
	4007S	125 h	286	N1	"
	4007S	125 h	666	All "N" devices	"
	4007S	125 h	668	All "N" devices	"
	TC1092	750 h	173	P2	V_{th} "P" $\leq$ -2.6 V
Bias Power Temperature Stress 125°C Cell	4007S'	168 h	552	All "N" devices	Edge transistor leakage
	4007S	168 h	555	All "N" devices	"
	4007S	168 h	554	All "N" devices	"
	4007S	168 h	550	All "N" devices	"
	4007S	168 h	548	All "N" devices	"
Bias Power Temperature Stress 105°C Cell	4007S	750 h	602	N1,P1	Breakdown (gate-to-source)
	TC1092	336 h	158	P3	Leakage Failure
Bias Power Temperature Stress 85°C Cell	4007S	168 h	588	P1	Breakdown (gate-to-source)
	TC1092	1000 h	147	P1, P2	V_{th} "P" $\leq$ -2.6 V
	TCS056	336 h	128	N3	Leakage current failure

APPENDIX B

PHYSICAL STRUCTURE OF THE EDGE REGION

When thin heteroepitaxial Si films are used to make CMOS/SOS devices, the usual practice is to etch the unneeded Si off the substrate, thereby leaving isolated Si islands. This process is the most common technique used for achieving dielectric isolation. The etch used is typically an anisotropic Si etch consisting of water, potassium hydroxide, and n-propanol used at an elevated temperature (∿85°C). This etch is somewhat preferential and attacks (111) planes more slowly than others. The preferential nature of this etch is not sufficient to guarantee a microscopically planar edge. Therefore, on the average, the edge surfaces are sloped toward the (111) plane but cannot really be considered to have a definite orientation. The preferential nature of the etch produces sloped edges which limit the amount of undercutting during the etch and give better step coverage with deposited metal.

Physically, the edge Si surface is different from the top Si surface. In addition to the previously mentioned orientation difference, the following points are to be considered:

(1) The edge region is not flat microscopically.
(2) The edge region has been exposed to different chemical environments.
(3) The edge surface intersects the substrate.
(4) The edge is composed of Si whose structural perfection is graded from top to bottom.

The important point to note is that there are at least five reasons to expect that the edge region and its associated interfaces will behave differently from the top Si surface and its associated interfaces. Consider what happens when the Si is constrained to retain its original shape after oxidation, as is observed. The process of thermally oxidizing a sharp corner is illustrated in Fig. B-1. During the oxidation, Si will be consumed to form the oxide. These areas are denoted 1, 2, 3, and 4. A given volume of Si will produce approximately twice that volume of SiO_2. Therefore, Si 1

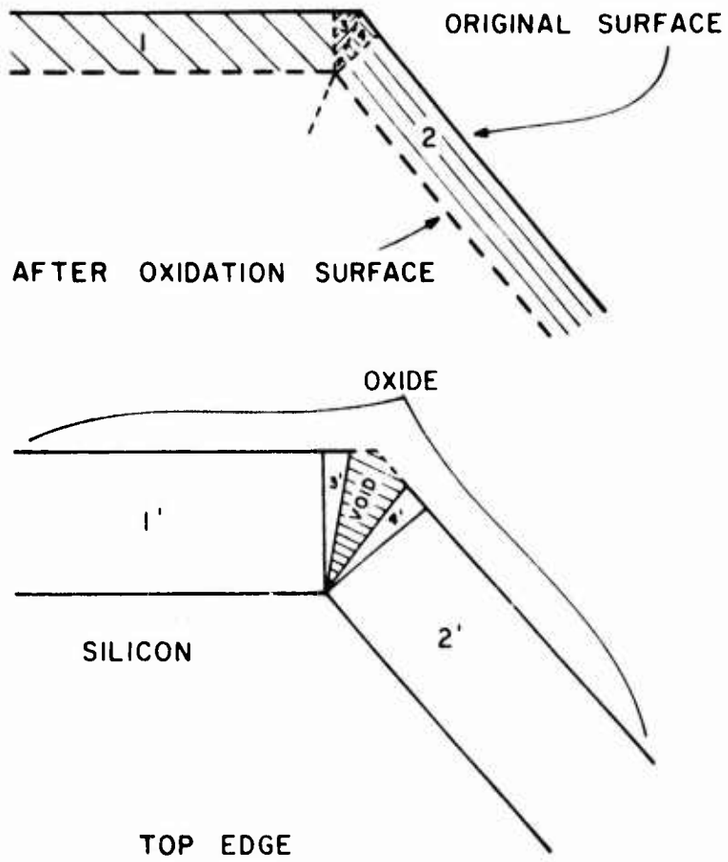


Figure B-1. Diagram that shows tendency for void creation at top of silicon edge.

produces oxide 1' and so forth. Obviously, the oxide does not have the shape shown in Fig. B-1, but it is clear that there is not enough Si available to produce enough oxide for uniform corner coverage. This means that a strong force, which is basically cohesive in nature, is pulling the edge oxide up the edge in order to fill the void. The force is not related to the thermal expansion coefficients and has its origin within the oxide itself. It is a direct consequence of the geometry of the system.

In addition to this cohesive force, the phenomenon illustrated in Fig. B-2 tends to form a void at the bottom of the edge. This phenomenon is again due to a limited supply of Si but is not a function of the Si film thickness.

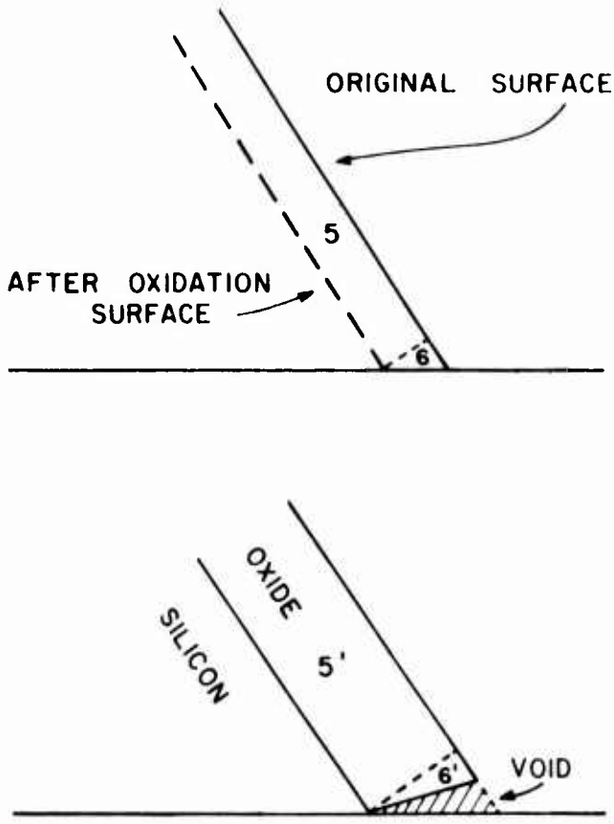


Figure B-2. Diagram that shows tendency for void creation at bottom of silicon edge.

This creation of a void at the bottom edge of the island results in a decrease in dielectric thickness. Continual thermal stressing of this region (e.g., thermal shock) has created a failure mechanism common to both Al-gate and Si-gate technologies.

This appendix was extracted from W. E. Ham, "High Speed Complementary Metal-Oxide-Semiconductor/Silicon-on-Sapphire Development," PRRL-75-CR-42; November 1975, (AD-B007 950L).

APPENDIX C

TEST TECHNIQUES

All device electrical characterization (initial, interim, and final) utilized the Datatron "Hustler 44" automatic test system. Supplemental tests performed for failure analysis used both a log-picoammeter and current analyzer. These techniques are described in this section.

1. Datatron Hustler 44

The Datatron Test System is a three-station system consisting of a two-station 50-kHz Hustler 44 and a one-station 10-MHz Hustler 45. The Hustler 44 parametric tester is capable of testing arrays of up to 75 pins and is wired to be expanded up to 100 pins and up to four stations. The central computer is a Data General Nova having 32K words of high-speed core memory. Supplementing this is a dual floppy disc with an additional 240K words of memory and a magnetic-tape Cartrifile memory for storing test programs. The system has an ASR 33 Teletype, CRT display and keyboard used to generate and edit test programs. A high-speed paper tape reader and punch is included for generating and storing hard copies of test programs. A medium-speed printer does data-logging and test pattern printouts. Additional hardware includes a system for measuring currents as low as 1 nA, two 100-V bias supplies, two clock systems, hardware masking of errors which eliminates repetition rate slow-down, and a front panel digital display for observing test patterns. An A-to-D converter is included to measure voltages and currents on any pin.

The Hustler 45 clock rate tester forms the third test station and is under the control of the Hustler 44 central computer. This system can be used for both parametric testing at rates up to 50 kHz as well as clock rate testing at rates up to 10 MHz. The system can test arrays with up to 76 pins and is wired to be expanded to 100 pins. The system has a 1024-bit high-speed ECL RAM behind each pin. The system can make rise-time, fall-time, pulse width, and propagation delay measurements to 1-ns resolution under software control. It contains a programmable pattern generator (microprocessor) to test arrays requiring repeating test patterns such as memories

and counters. The microprocessor is formated for 64 instructions of 32 bits each, and is configured for 16 address lines and 12 data lines. It can test up to 32K bits of memory at a 10-MHz rate.

Software includes executive, self-test, and calibration programs as well as datalog, software masking, delta measurements, truth table read-in from tape, bias offset, and incremental voltage testing. A translator program is provided to make test programs compatible between the new system and the existing Datatron Test System.

The entire test system will normally be set up for wafer probing at the Hustler 45 station and at one of the Hustler 44 stations. The remaining Hustler 44 station will be used for final testing packaged arrays. Any of the stations can easily be converted to final testing or wafer probing as the need arises.

2. Current Analyzer ("Square-Rooter")

In normal operation, a COS/MOS inverter input is switched rapidly between the high and low states so that the major current is due to charging and discharging of the output capacitance.

The output voltage curve shows that when the voltage at the input of the inverter is zero, the gate-to-source voltage (V_{gs}) of the p-channel device is equal to the negative of the supply voltage (V_{DD} = 10 V) and the p-channel unit is on. Under these conditions there is a low impedance path from the output to V_{DD}, and a very high impedance path to ground; therefore, the output voltage approaches V_{DD}. When the input voltage is $+V_{DD}$, the situation is reversed: the p-channel unit is cut off and the n-channel unit is on, with the result that the output voltage approaches zero. As the input voltage is swept from 0 toward V_{DD} the n-channel begins to conduct. Therefore, the left side of the current curves represents the I-V characteristic of the n-channel device. The source of the n-channel is connected to V_{SS} so that the gate-to-source voltage is $V_{gsn} = V_{in}$. When V_{in} reaches the switching voltage (approximately $V_{DD}/2$) the p-channel device begins to limit the current. The right-hand portion of the current curves represents the I-V characteristic of the p-channel unit. The source of the p-channel is connected to V_{DD} so that the p-channel gate-to-source voltage is measured $V_{gsp} = V_{in} - V_{DD}$.

The simple current equations for the n- and p-channel devices are:

$$I_{Dn} = K_n (V_{gsn} - V_{thn})^2 \qquad \text{(C-1)}$$

$$V_{gsp} < V_{tp} \quad I_{Dp} = K_p (V_{gsp} + V_{thp})^2 \qquad \text{(C-2)}$$

where K_n, K_p = gain constants depending on geometry and field effect mobility.

V_{thn}, V_{thp} = threshold voltage for n- and p-channel devices.

By analyzing the power supply current, it is possible to determine the threshold and gain factors of both the p- and n-channel devices. The task is greatly simplified by looking at the square root of the drain current since this makes Eqs. (C-1) and (C-2) linear in voltage. Figure C-1 shows that the square root of the current is composed of two straight-line segments whose intercepts are the threshold voltages and slopes are equal to the square root of the gain factor. Figure C-2 shows the schematic of the current analyzer. Typical plots obtained with the current analyzer during failure analysis are shown in Fig. C-3.

3. Log-Picoammeter

The log-picoammeter provides accurate current measurements with continuous auto-ranging from 10^{-11} to 10^{-3} A. A dual-polarity input and an output voltage of 1 V per decade provide a convenient means for recording data with either an X-Y recorder or an automated testing system. Figure C-4 shows typical plots obtained on devices during the stress test program.

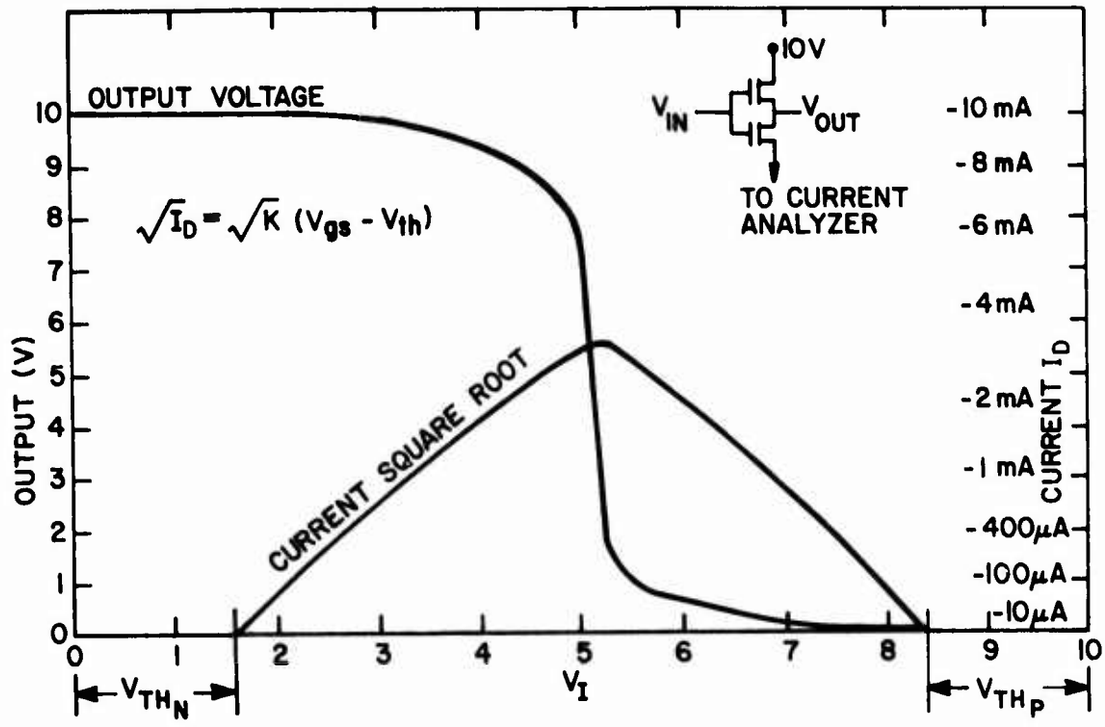


Figure C-1. Transfer characteristics, CD4007.

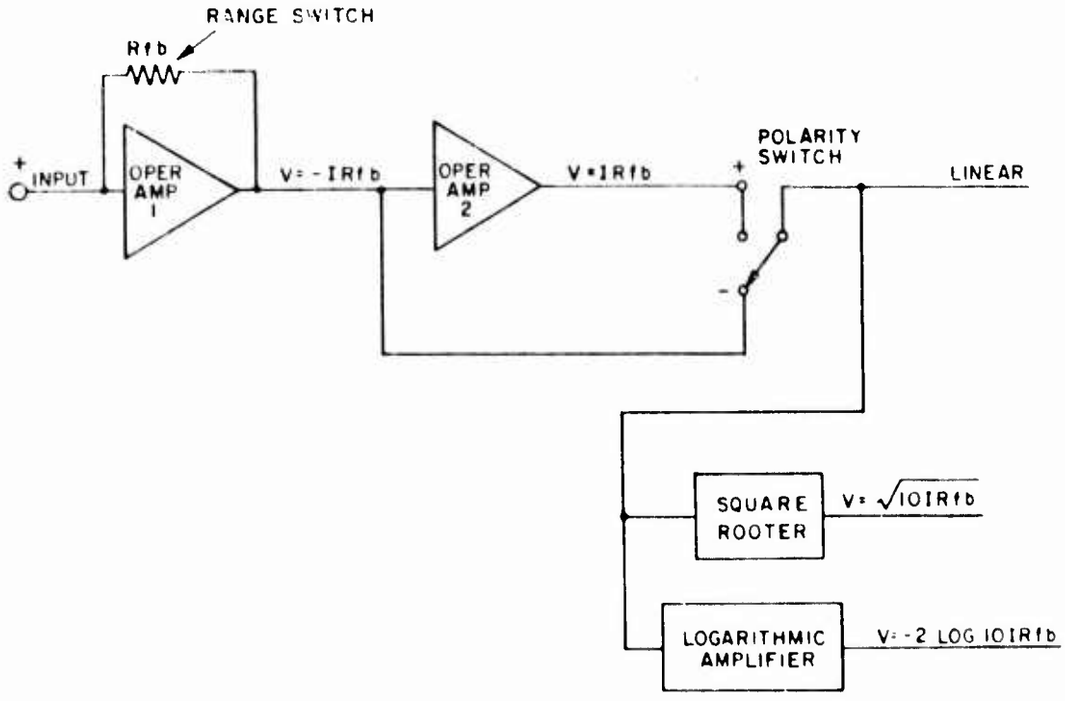
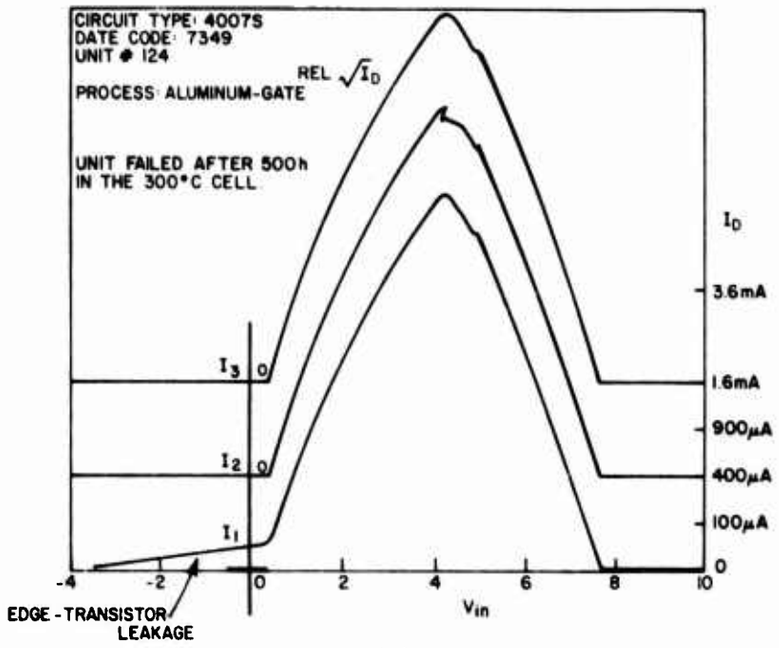
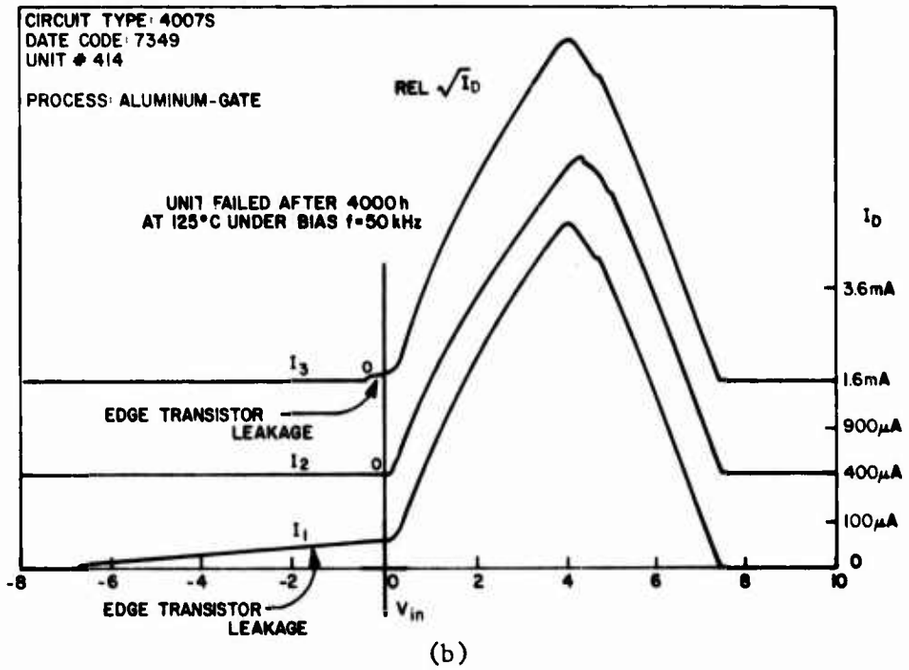


Figure C-2. Block diagram of current analyzer.



(a)



(b)

Figure C-3. Typical plots of failure analysis with current analyzer: (a) unit failed after 500 h at 300°C and (b) unit failed after 4000 h at 125°C.

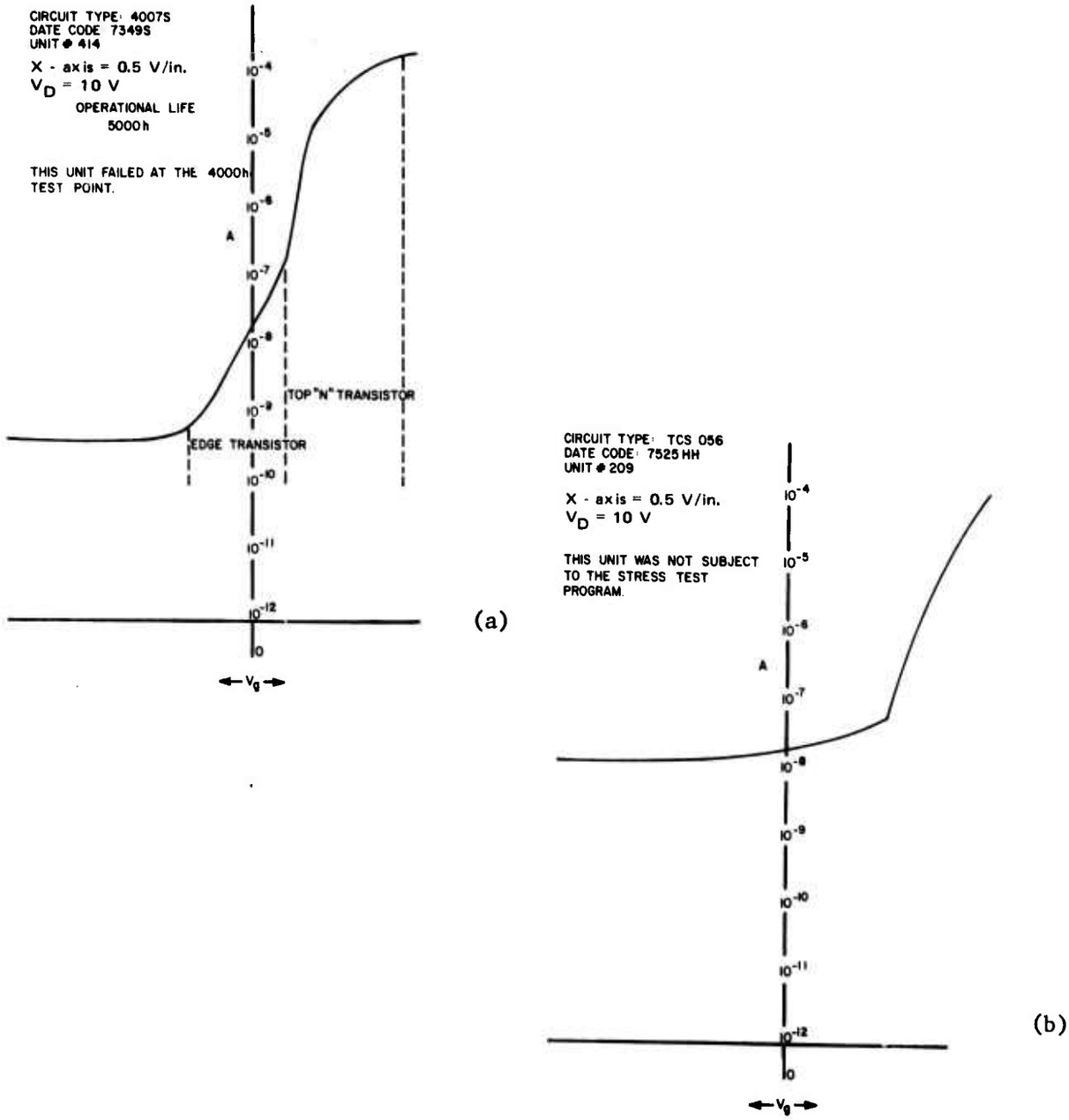
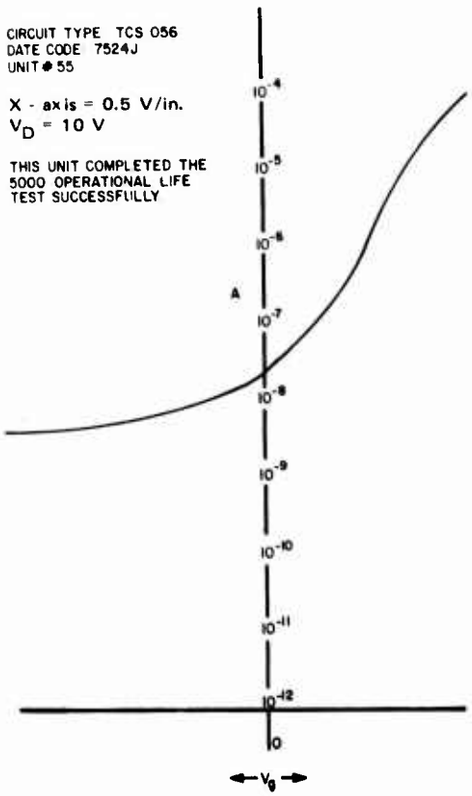
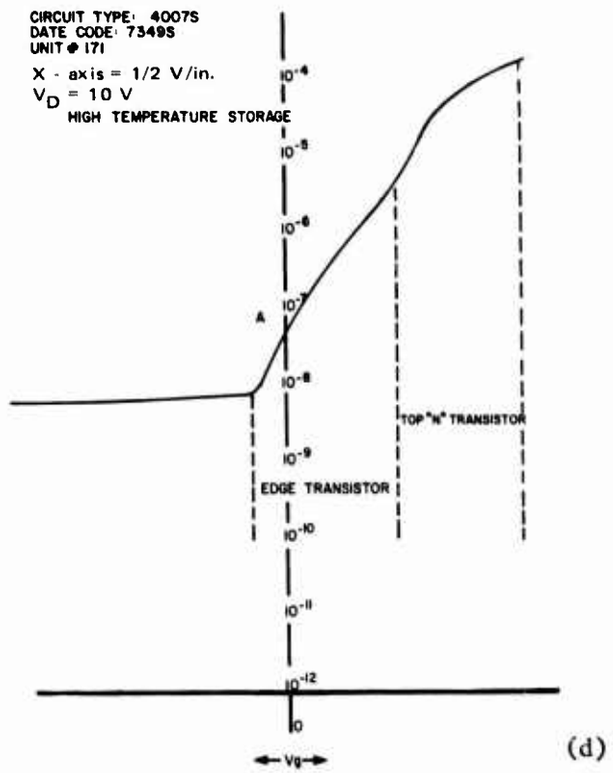


Figure C-4. Typical "log-picoammeter" plots; (a) Unit failed after 4000 h of 125°C operational life. (b) Not subjected to stress test program (TCS056).



(c)



(d)

Figure C-4. Typical "log-picoammeter" plots; continued (c) Unit completed 5000 h life test successfully (TCS056). (d) Unit failed for edge-transistor leakage after high-temperature storage (4007S).

APPENDIX D

LIQUID-CRYSTAL FAILURE ANALYSIS TECHNIQUE

A. BACKGROUND

This technique is nondestructive and allows both surface thermal effects and ac fields to be observed. A nematic liquid-crystal layer is applied to the chip, and the circuit is operated normally. The effect is observed on a standard metallurgical microscope utilizing cross-polarized lighting and optics. In pulse operation the areas of the circuit where the potentials are modulated appear bright against a dark background. By reducing the repetition rate of the clocking pulse, the propagation of the signal in a complex circuit can be followed. Localized heating effects can also be observed. When the failure mode is a region of high current density and low voltage breakdown, the crystal will respond to a temperature change when the V_{DD} voltage is swept beyond the breakdown level. By decreasing the V_{DD} level slowly, the heating is confined to a very small area and the failure location can be pinpointed.

B. LIQUID-CRYSTAL OPTICS

A nematic liquid crystal is composed of rod-like organic molecules which act on each other to force themselves to align in the same direction. If the walls bounding a thin layer are suitably treated, they will force the molecules adjacent to the walls to be aligned in a perpendicular fashion. The ordering tendency then causes the rest of the molecules to follow suit and point in the same direction.

The electro-optic and thermo-optic properties of this layer are strongly birefringent, that is, the refractive index changes with direction. When electrical fields or currents cause localized distortion of the molecular ordering the refractive index is correspondingly changed. Similarly, when localized heating occurs it causes an adjacent region of liquid crystal to pass from the nematic to the isotropic (normal liquid) state, also creating an index distortion. As a result of these properties a refractive index pattern is produced in the liquid crystal which mirrors the pattern of electric fields at the surface of the integrated circuit.

C. INTEGRATED-CIRCUIT EXAMINATION

An extremely simple preparation of the IC allows this technique to be implemented. The surface of the IC is pretreated with a surfactant solution that assists the molecular alignment. The liquid crystal is then applied to the chip. A surfactant-coated cover glass is then lowered onto the liquid crystal and the completed assembly, as shown in Fig. D-1, is ready for observation. The device is then placed into an ocular system (standard metallurgical microscope with polarized light source and eyepieces) as shown in Fig. D-2 and operated normally.

A further discussion of the liquid crystal technique may be found in D. J. Channin, "Observing Integrated Circuit Operation with Liquid Crystals," I.E.E.E. Transactions on Electron Devices, October 1974.

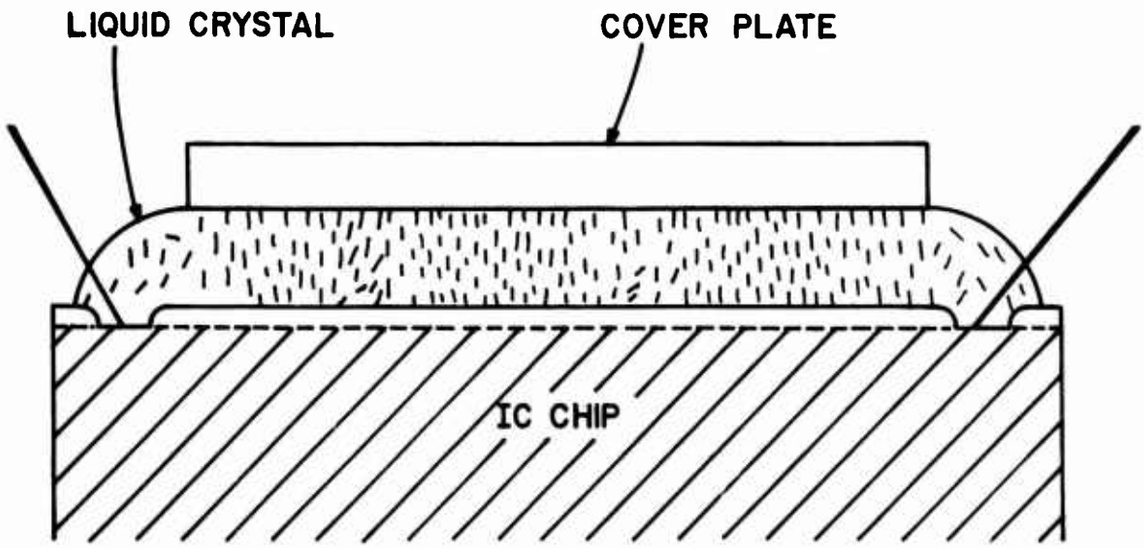


Figure D-1. Nematic liquid-crystal technique.

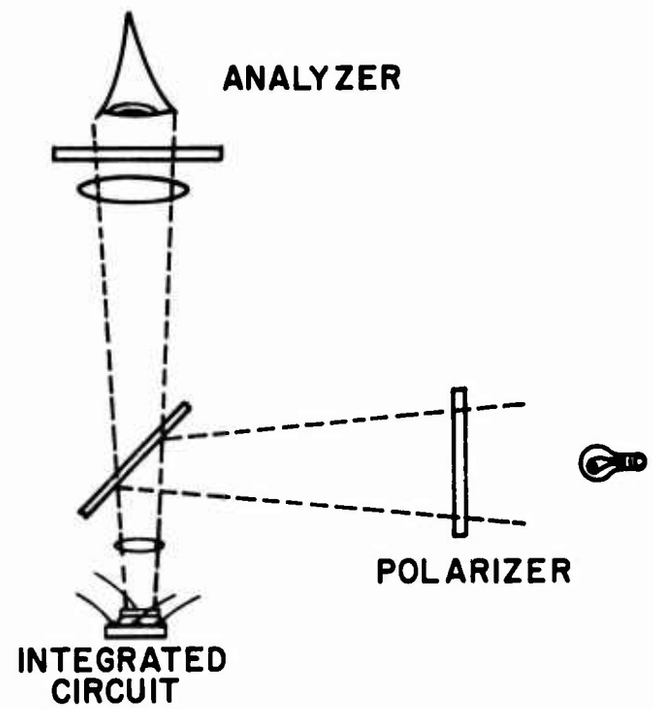


Figure D-2. Liquid-crystal ocular display system.

METRIC SYSTEM

BASE UNITS:

Quantity	Unit	SI Symbol	Formula
length	metre	m	...
mass	kilogram	kg	...
time	second	s	...
electric current	ampere	A	...
thermodynamic temperature	kelvin	K	...
amount of substance	mole	mol	...
luminous intensity	candela	cd	...

SUPPLEMENTARY UNITS:

plane angle	radian	rad	...
solid angle	steradian	sr	...

DERIVED UNITS:

Acceleration	metre per second squared	...	m/s
activity (of a radioactive source)	disintegration per second	...	(disintegration)/s
angular acceleration	radian per second squared	...	rad/s
angular velocity	radian per second	...	rad/s
area	square metre	...	m
density	kilogram per cubic metre	...	kg/m
electric capacitance	farad	F	A·s/V
electrical conductance	siemens	S	A/V
electric field strength	volt per metre	...	V/m
electric inductance	henry	H	V·s/A
electric potential difference	volt	V	W/A
electric resistance	ohm		V/A
electromotive force	volt	V	W/A
energy	joule	J	N·m
entropy	joule per kelvin	...	J/K
force	newton	N	kg·m/s
frequency	hertz	Hz	(cycle)/s
illuminance	lux	lx	lm/m
luminance	candela per square metre	...	cd/m
luminous flux	lumen	lm	cd·sr
magnetic field strength	ampere per metre	...	A/m
magnetic flux	weber	Wb	V·s
magnetic flux density	tesla	T	Wb/m
magnetomotive force	ampere	A	...
power	watt	W	J/s
pressure	pascal	Pa	N/m
quantity of electricity	coulomb	C	A·s
quantity of heat	joule	J	N·m
radiant intensity	watt per steradian	...	W/sr
specific heat	joule per kilogram-kelvin	...	J/kg·K
stress	pascal	Pa	N/m
thermal conductivity	watt per metre-kelvin	...	W/m·K
velocity	metre per second	...	m/s
viscosity, dynamic	pascal-second	...	Pa·s
viscosity, kinematic	square metre per second	...	m/s
voltage	volt	V	W/A
volume	cubic metre	...	m
wavenumber	reciprocal metre	...	(wave)/m
work	joule	J	N·m

SI PREFIXES:

Multiplication Factors	Prefix	SI Symbol
1 000 000 000 000 = 10^{12}	tera	T
1 000 000 000 = 10^{9}	giga	G
1 000 000 = 10^{6}	mega	M
1 000 = 10^{3}	kilo	k
100 = 10^{2}	hecto*	h
10 = 10^{1}	deka*	da
0.1 = 10^{-1}	deci*	d
0.01 = 10^{-2}	centi*	c
0.001 = 10^{-3}	milli	m
0.000 001 = 10^{-6}	micro	μ
0.000 000 001 = 10^{-9}	nano	n
0.000 000 000 001 = 10^{-12}	pico	p
0.000 000 000 000 001 = 10^{-15}	femto	f
0.000 000 000 000 000 001 = 10^{-18}	atto	a

* To be avoided where possible.

MISSION
of
Rome Air Development Center

RADC plans and conducts research, exploratory and advanced development programs in command, control, and communications (C^3) activities, and in the C^3 areas of information sciences and intelligence. The principal technical mission areas are communications, electromagnetic guidance and control, surveillance of ground and aerospace objects, intelligence data collection and handling, information system technology, ionospheric propagation, solid state sciences, microwave physics and electronic reliability, maintainability and compatibility.