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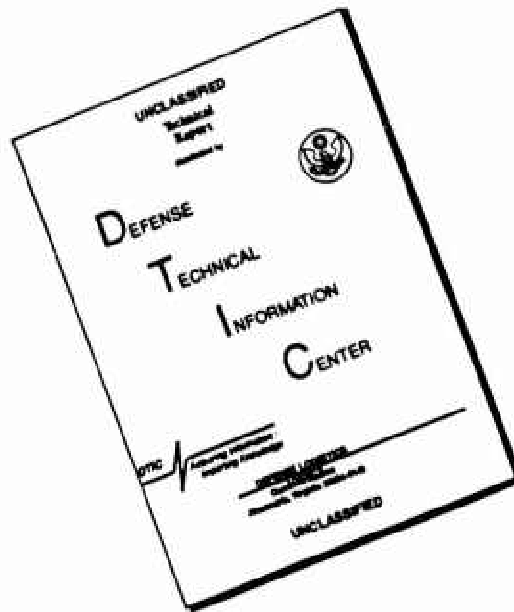

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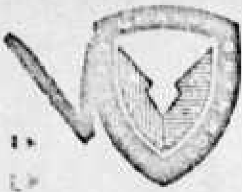

(2)

Research and Development Technical Report

ECOM-76-C-1340-I

AD B017548

SMALL SIGNAL GaAs FET PROBLEMS

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March 1977
Interim(Semi Annual) Report for Period 5 April 1976 to October 1976

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SMALL SIGNAL GA AS FET PROBLEMS

for

Electronic System Procurement Branch
Procurement and Production Directorate
U. S. Army Electronic Command
Ft. Monmouth, N. J. 07703

Contract

DAAB07-76-C-1340

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I INTRODUCTION

This program as originally set up was intended to provide a means for an in depth investigation into certain FET problems and to accomplish tasks related to GaAs FET's. The tasks/problems to be investigated were to include as a minimum the following items:

1. DC drift
2. RF drift
3. Assymetry
4. Non linear contacts
5. Epi layer, contacts and R_{con}
6. Noise mechanisms
7. Gunn mode
8. Cooled noise figure to 77°K
9. Reliability
10. Break up
11. Burn out
12. Buffer layer limitations
13. Loops
14. High G_{out} buffer

In addition to the items listed above, the effect of capacitance in FET's has also been investigated. During the first six months of the program all of the problem/tasks listed above were investigated with the exception of:

1. Noise mechanisms
2. Cooled noise figure
3. Burn out

Those items not reported on during the first six months will be investigated during the latter half of this contract.

II NARRATIVE AND DATA

1. DC and RF Drift

The work on this contract directed to investigating the origins of drift is an extension of work that had already been started at Avantek before the award of this program. Prior to this program, Avantek had ascertained the following facts regarding DC and RF drift:

A. The largest part of RF and DC drift is a surface oriented condition.

B. RF drift with the exception of the initial short term drift, can be eliminated by depositing polycrystalline gallium arsenide on the surface of the FET between the gate and source and the gate and drain.

C. All available FET's other than Avantek, also exhibit DC and RF drift to a greater or lesser degree.

During October, at the request of ECOM, the investigation on drift was re-initiated at Avantek. The purpose of this investigation will be to define as accurately as possible, the actual causes of drift and how PGA affects the cause itself. This new investigation, which has just begun, has yielded several new pieces of information regarding drift.

A. The drift characteristics of competitors' devices can also be stabilized by the application of PGA, if the device has not already been passivated with another material.

B. The application of PGA has a very minor effect on the input capacitance at the terminals of an FET. Figure 1 shows how the capacitance is changed for an FET before and after the application of PGA. The application of PGA affects transconductance and, at least dimensionally, capacitance. This means that the frequency characteristics of an FET are altered favorably by the application of PGA.

The alteration of the drift characteristics by the application of PGA is illustrated in Figure 2. Note that the initial drift which lasts up to a minute or less is not affected by the PGA but the long term drift is the portion which is actually stabilized. Transistor run, 183C, from which these transistors were taken, does not have very severe drift. While from the point of view of making driftless transistors, this is desirable, it makes testing the differences in PGA devices rather difficult. From Figure 2 it can be seen that the total drift actually amounts to only a small fraction of the operating current of the device. The differences in the RF characteristics are also not greatly different as can be seen from Tables I and II which show the S parameters of the FET's. In order to improve the accuracy of the measurement of PGA and non PGA devices it will therefore be necessary to make more FET

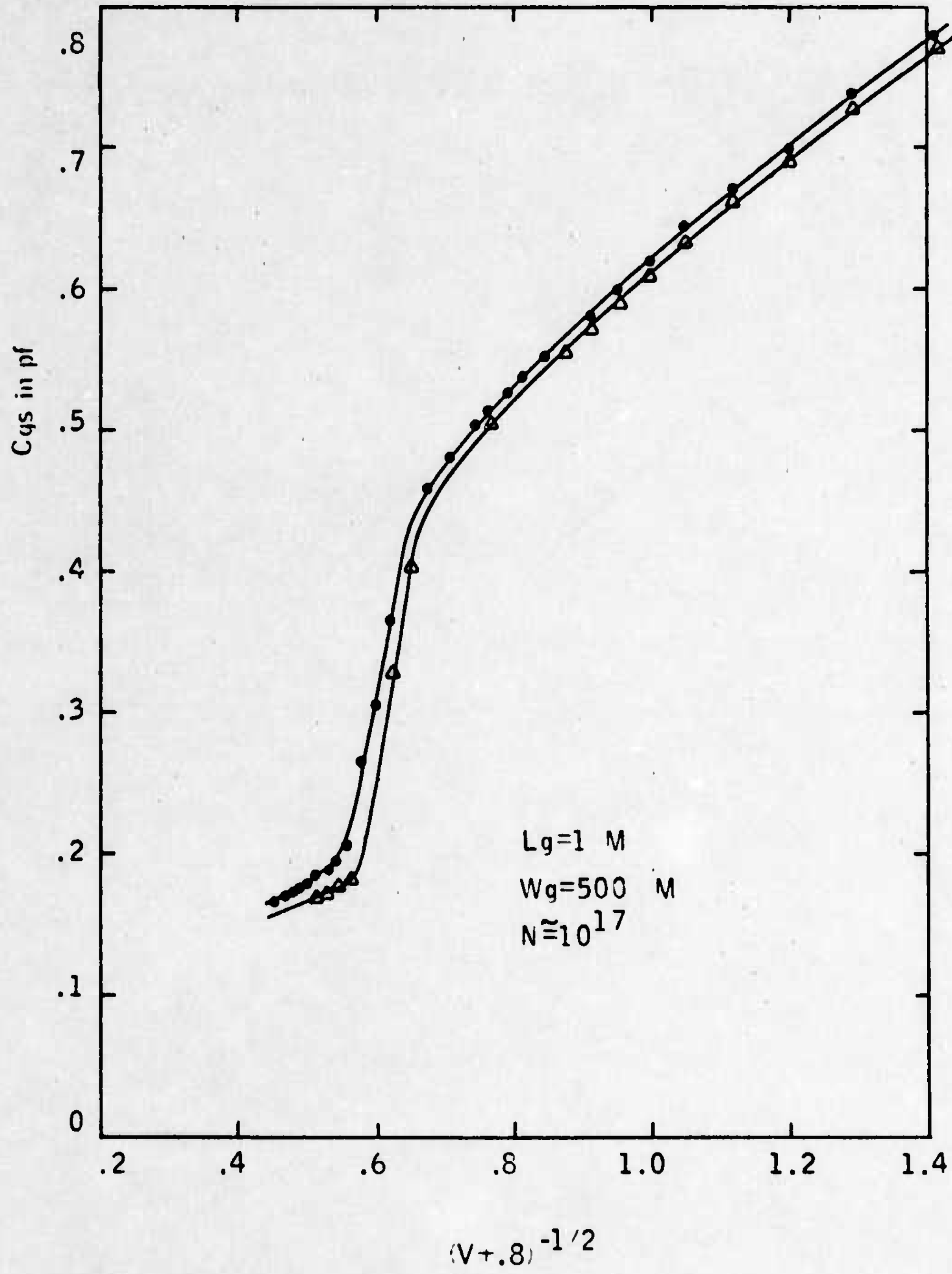
Effect of PGA on FET

Input Capacitance, Cgs

Figure 1

△ Before PGA

c After PGA



Effect of PGA on Drain Current, I_D,

Drift Vs Time

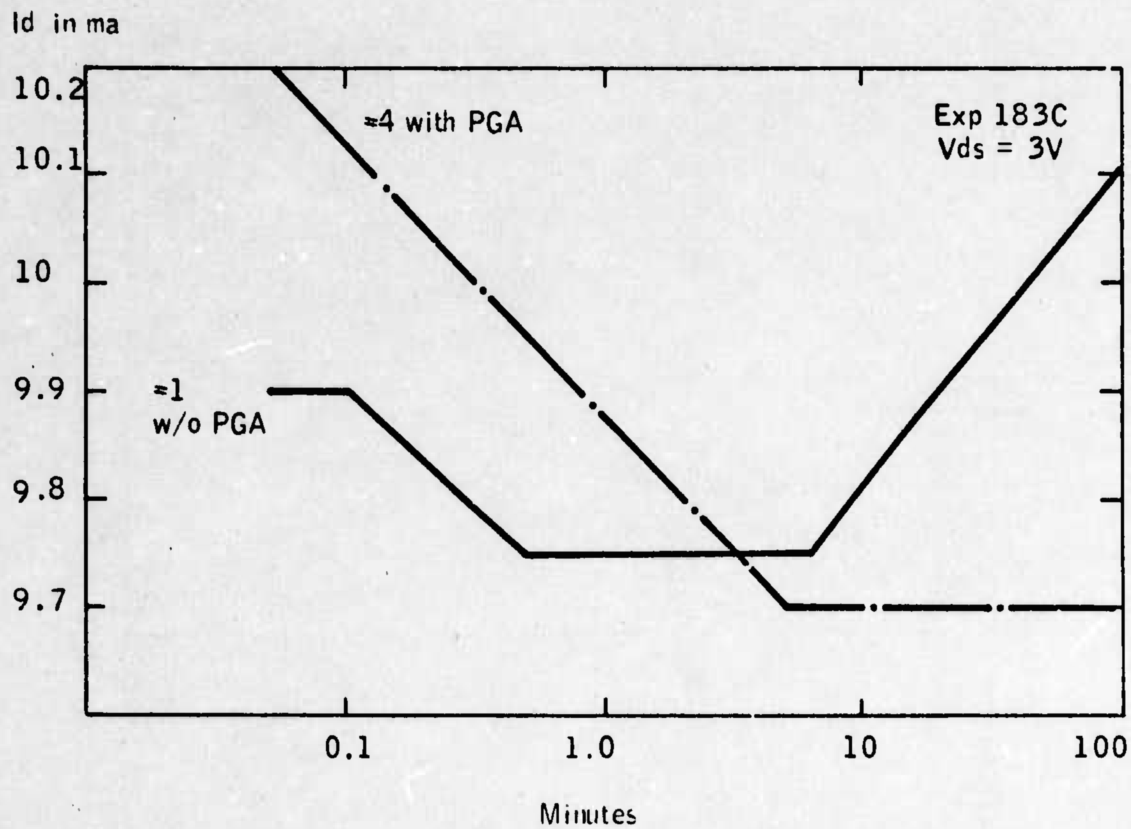


Figure 2

TABLE I A

[illegible]

[illegible]

[illegible]

SER NO. 6 W/o PGA BIAS= 3.00 VOLTS, 10.00 MA

-- MAGN AND ANGLES:

FREQ	11		21		12		22	
4000.00	.918	-82.9	1.151	91.0	.046	33.7	.726	133.2
6000.00	.863	-128.4	1.016	45.8	.042	14.7	.708	12.5
8000.00	.833	-166.2	.814	14.1	.005	15.7	.722	-107.8
10000.00	.821	[illegible]	.726	-14.6	.049	34.7	.689	136.0
12000.00	.783	154.6	.784	-42.4	.070	41.1	.657	4.8
14000.00	.719	134.6	.530	-63.8	.095	18.6	.711	-123.9
16000.00	.665	114.4	.500	-89.6	.137	-5.9	.660	87.7
17999.99	.492	103.7	.621	-122.9	.180	-41.7	.596	-65.2

REF PLANES = 2.70 2.70 5.40

FREQ MHZ	S21 DB	MSG DB	K	MAG DB	MASON U DB
4000.00	1.52	14.15	.53	$$$$$$$	$$$$$$
6000.00	.09	13.84	2.15	7.76	9.44
8000.00	-1.79	13.65	2.30	7.24	9.15
10000.00	-2.76	11.70	2.22	5.47	6.38
12000.00	-2.61	10.15	2.69	3.01	2.99
[illegible]000.00	-5.39	7.52	2.07	1.64	1.56
[illegible]000.00	-6.03	5.62	2.13	-.41	-.40
17999.99	-4.13	5.38	2.50	-1.43	-1.36

REF PLANES = 2.70 2.70 5.40

Table IA

TABLE I B

[illegible]

[illegible]

[illegible]

SER NO. [illegible] W/o PGA BIAS= 3.00 VOLTS, 20.00 MA

-- [illegible]:

FREQ	11		21		12		22	
4000.00	.915	-87.0	1.226	87.5	.042	42.3	.708	128.6
6000.00	[illegible]	-133.2	1.010	45.2	.042	29.7	.678	8.5
8000.00	[illegible]	-164.8	.889	[illegible]	.046	26.8	.691	-110.8
10000.00	.806	168.5	.733	-15.8	.067	33.3	.653	133.0
12000.00	.767	148.2	.724	-45.3	.089	33.0	.619	2.5
14000.00	.653	127.6	.553	-64.6	.114	9.4	.678	-125.6
16000.00	.478	107.4	.524	-91.5	.159	-17.9	.630	85.9
17999.99	.401	96.1	.623	-120.8	.205	-52.7	.561	-66.7

REF PLANES = 2.70 2.70 5.40

FREQ MHZ	S21 DB	MSG DB	K	MAG DB	MASON U DB
4000.00	1.77	14.67	.79	*******	21.79
6000.00	.08	13.79	2.23	7.53	9.45
8000.00	-1.84	12.48	1.89	7.05	9.37
10000.00	-2.70	10.39	1.53	4.84	5.81
12000.00	-2.81	9.11	2.46	2.39	2.45
14000.00	-5.15	6.66	2.01	1.11	1.12
16000.00	-5.62	5.17	2.07	-.71	-.71
17999.99	-4.12	4.83	2.51	-2.00	-2.01

REF PLANES = 2.70 2.70 5.40

Table IB

TABLE IIA

[illegible]

[illegible] BIAS: 3.00 VOLTS, 10.00 MA

FREQ	11		21		12		22	
4000.00	[illegible]	[illegible]	[illegible]	86.5	.051	32.9	.692	136.1
6000.00	[illegible]	[illegible]	1.171	41.4	.043	20.3	.672	16.0
8000.00	[illegible]	[illegible]	.941	10.5	[illegible]	31.5	.693	-104.4
10000.00	[illegible]	[illegible]	[illegible]	-18.7	.071	44.9	.666	[illegible]
12000.00	[illegible]	[illegible]	[illegible]	-47.9	.091	32.5	.628	7.6
14000.00	[illegible]	112.1	[illegible]	[illegible]	.140	18.3	.712	-120.1
16000.00	[illegible]	85.6	.745	-100.6	.129	-54.9	.549	94.3
17999.99	[illegible]	46.0	.805	-155.3	.182	-67.3	.575	-70.7

REF PLANES = 2.70 2.70 5.40

FREQ MHZ	S21 DB	MSG DB	K	MAG DB	MASON U DB
4000.00	3.11	14.51	.69	********	21.33
6000.00	[illegible]	14.40	2.32	7.94	9.66
8000.00	-.53	13.66	1.98	7.93	10.02
10000.00	-1.45	10.76	1.86	5.41	5.94
12000.00	-.94	9.93	2.21	3.71	3.72
14000.00	[illegible]	6.78	1.26	3.71	2.87
16000.00	[illegible]	[illegible]	1.99	.20	.34
17999.99	-1.89	6.46	2.30	-.11	-.10

REF PLANES = 2.70 2.70 5.40

Table IIA

[illegible]

[illegible] *TABLE IIB*

[illegible]

SER NO. 2 *W/PGA* [illegible] 3.00 VOLTS, 20.00 [illegible]

-- [illegible] AND ANGLES:

FREQ	11		21		12		22	
4000.00	.888	[illegible]	1.[illegible]	[illegible]	.045	43.8	.677	131.2
6000.00	.828	-140.0	1.174	37.0	[illegible]	30.2	[illegible]	17.4
8000.00	.801	178.0	[illegible]	[illegible]	[illegible]	24.0	[illegible]	-107.5
10000.00	[illegible]	155.7	[illegible]	[illegible]	[illegible]	40.3	.630	130.7
12000.00	.714	132.3	[illegible]	-50.8	.111	25.7	.594	4.7
14000.00	.612	103.[illegible]	.677	[illegible]	.154	6.5	.684	-127.[illegible]
16000.00	.545	68.3	[illegible]	[illegible]	.210	-56.6	.563	91.[illegible]
17999.99	.099	-81.0	[illegible]	[illegible]	[illegible]	-77.3	.538	-73.1

REF PLANES = 2.70 2.70 5.[illegible]

FREQ MHZ	S21 DB	MSG DB	K	MAG DB	UNCON U DB
4000.00	3.04	15.13	.53	********	20.57
6000.00	1.39	14.18	2.22	7.86	9.92
8000.00	-2.56	11.10	2.15	5.03	6.69
10000.00	-1.46	9.82	1.70	4.54	5.53
12000.00	-1.16	8.98	2.07	3.05	3.11
14000.00	-3.39	6.42	1.35	2.90	2.41
16000.00	-2.70	5.42	2.61	-.32	-.41
17999.99	-2.34	5.84	2.39	-.74	-.69

REF PLANES = 2.70 2.70 5.[illegible]

Table IIB

runs in which, it is hoped, the differences will be large enough to make them measurable. The plans for this portion of the investigation are then as follows:

(1) Build more FET's without PGA in order to find a run which exhibits fairly severe drift.

(2) Build up FET's out of this run.

(3) Test the FET's completely for RF characteristics, DC characteristics and drift.

(4) Apply PGA to the transistors tested in (3).

(5) Retest all of the transistors for drift, DC and RF characteristics.

(6) Analyze results and build a model.

(7) Apply tests to check validity of model.

At this time it is possible to speculate only as to the nature of the changes in the transistor which occur after the application of PGA. Dimensionally, it is expected that the mechanisms causing drift can be modeled like variable capacitances but will actually be time-dependent traps. It also appears that the location of these traps is near the periphery of the FET gate.

2. Backside Gating Phenomena

A number of the problems which were delineated at the time this program was started have been traced to the interface layer between the active layer and the substrate or buffer, if this is used. Most of the effects occur only in non-buffer devices. Some of these effects are:

- Assymetry
- Non linear contacts
- Break up
- Loops

A brief discussion of each one of these phenomena follows with an explanation as to how the buffer layer alleviates or eliminates the effect.

Very often when the active layer is grown directly on a tin doped substrate, a P layer is formed at the interface between the active layer and substrate. The P layer thus formed can, under certain circumstances, act as a backside gate since the P layer together with the N active layer, forma PN junction. This is shown schematically in Figure 3. If

Figure 3

FET With Backside Gating

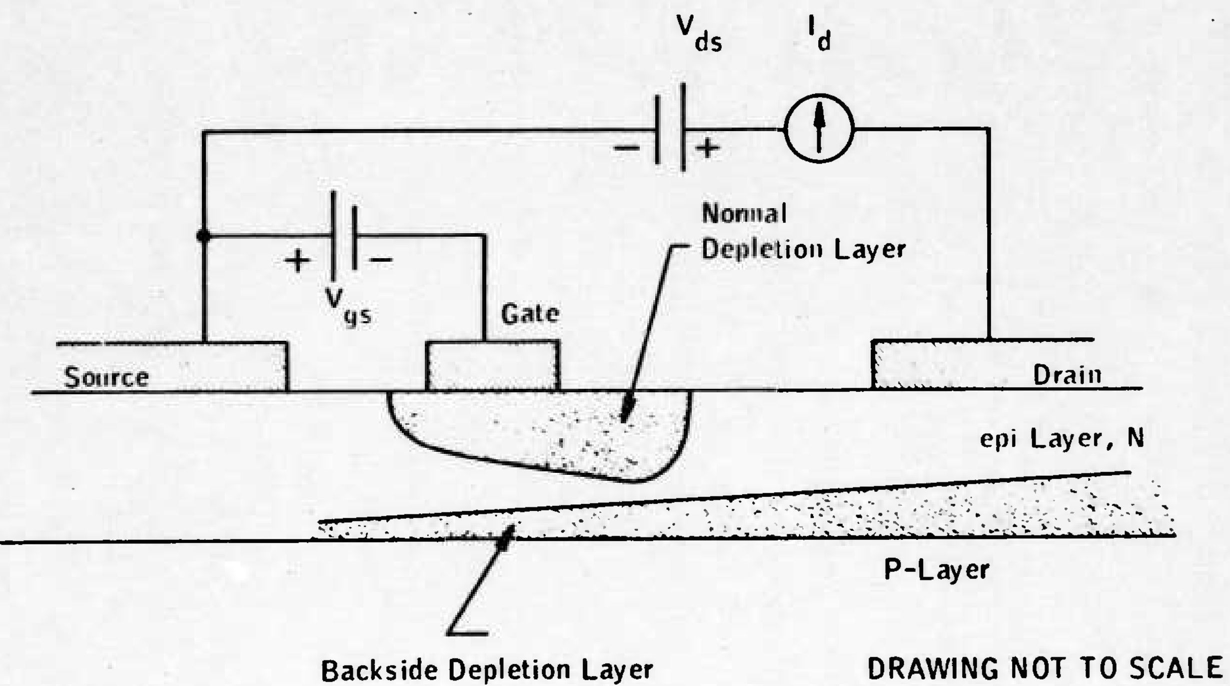


Figure 3

the drain is made positive with respect to the source while the gate is connected to the source for an Idss measurement, the "backside gate" is automatically biased in such a way so as to pinch off the active layer from the back. This is because in most transistor designs, the source is tied to the substrate while the drain remains isolated. It also means that the source and the backside PN junction are both connected together at zero potential. If an AC signal is used on the curve tracer to delineate Idss, both in the forward and reverse directions, the value for Idss in the forward direction (which is such to make backside gating possible), will show a much reduced value. Figure 4A shows this phenomenon.

The most effective solution to this problem is the application of a good buffer layer. The buffer layer, if of sufficient thickness, and low enough doping density, can prevent formation of a P layer next to the active layer. The critical minimum thickness for the buffer layer is the order of 3 to 5 microns.

If the impurities which diffuse out of the substrate and form the so called anomalous or P layer, are to be prevented, the total number of charges in the buffer layer per unit area, must exceed those in the substrate itself. Thus, the minimum requirement for the thickness on the buffer layer. Figure 5 shows the curve tracer characteristic for a buffered device. Note that it has no loops which is another characteristic of devices utilizing buffer layers.

One form of the non linear contact is just another aspect of the backside gating problem. The effect of assymetry described above can occur on devices without gates as well as those with gates. Thus the assymetry shown in Figure 4A could also be used to describe the set of contacts where backside gating was also present. Another form of non-linearity encountered in contacts is the depressed shoulder on the saturation characteristic which appears to be a form of premature saturation. It is caused by the backside gate taking on a charge which later, due to carrier accumulation or other causes, disappears allowing the transistor to reach its final and normal current saturation. A more extreme form of this defect is shown in Figure 4D. This is often called break up - where the transistor goes into what appears to be a normal saturation characteristic which is followed by a secondary saturation at a much higher current level. During the transition from the lower saturation current to the higher saturation, the device is extremely noisy and may have oscillation problems. It is easy to visualize thru the action of backside gating that the transistor saturates prematurely

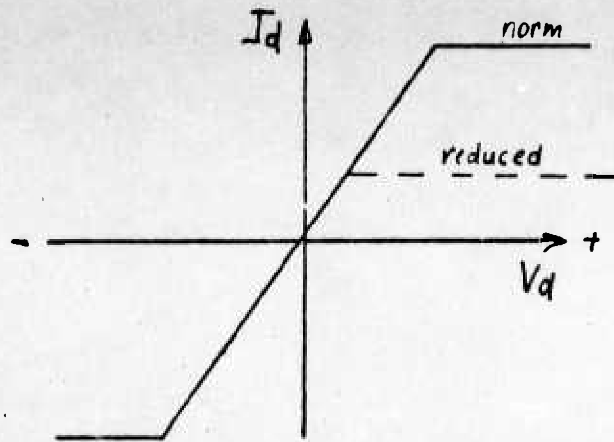
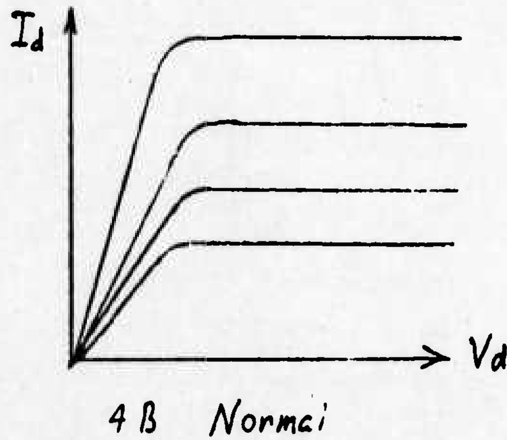
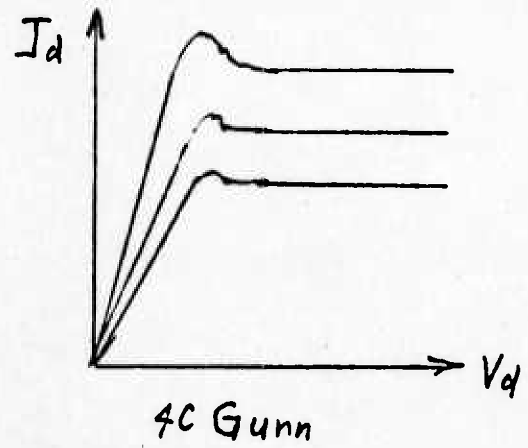


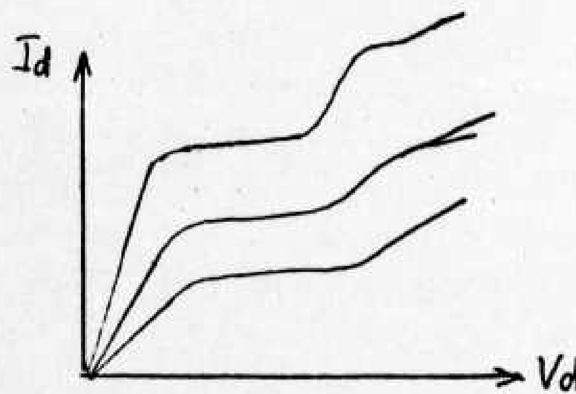
Fig 4A
Assymetry



4B Normal



4C Gunn



4D
Breakup

Figure 4
Backside Gating Phenomena

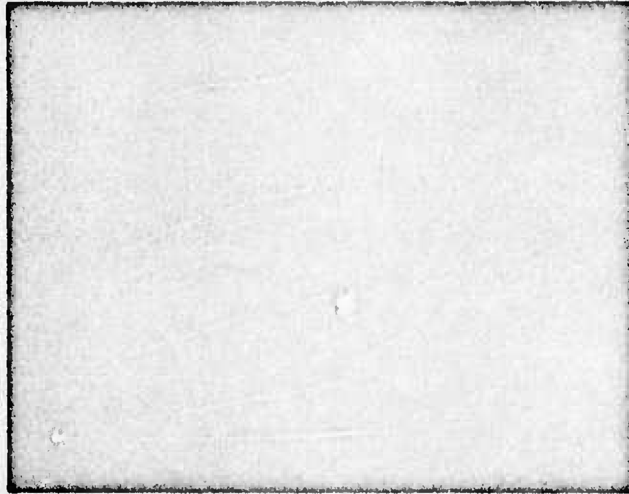


Figure 5

Curve Tracer Characteristic
FET on Buffered Material

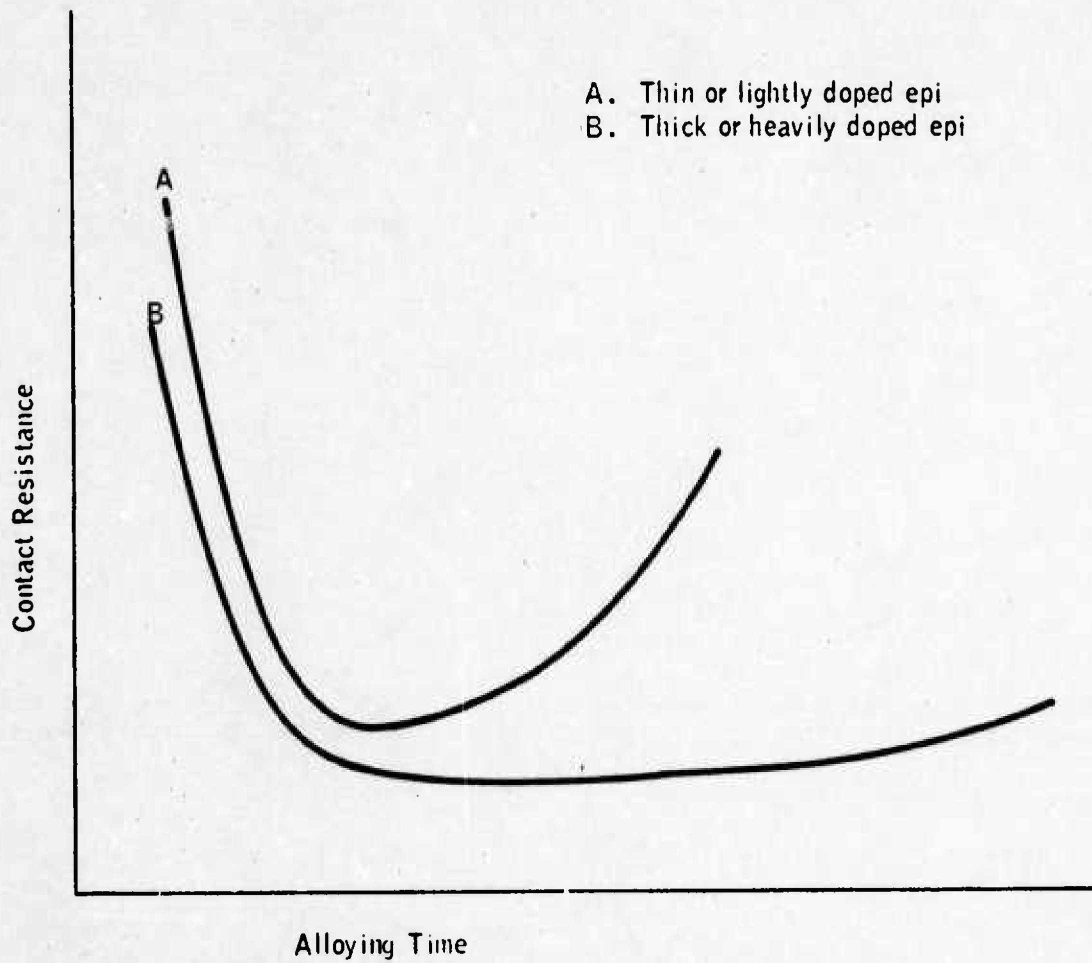
1 V/div - Horizontal
10 ma/div - Vertical
0.5 V/step

due to pinching off of the channel from the backside. However, the loss of control by the backside gate and the eventual resaturation of the transistor at a higher level is more difficult to explain. It is possible that there is an accumulation of carriers near the pinched off end of the channel, which when it becomes large enough, disperses, thus causing a high noise level and a higher current level. During this investigation it was found that two methods of controlling the backside gate phenomena were available. First of all, by doping the channel more heavily (e.g. 10^{17}) the incidence of backside gating, including break up and assymetry in the contacts, could be reduced to a very small percentage of the total transistors. However, the use of a buffer layer proved to be the most effective means of combating this problem. Providing the buffer layer is thick enough, backside gating is not present. Experimentally, it was determined that a critical value for the thickness of the buffer layer is in the order of three to four microns. For a conservative design thus, a six micron buffer layer thickness is desirable.

3. Contact Resistance and Epitaxial Layer

Sometime before this program was begun, it was noted that devices built on very lightly doped active layers or on very thin normally doped layers (e.g. $\approx 10^{17}$) were very sensitive to the alloying cycle as it affected the contact resistance. Figure 6 shows the effect observed. For devices built on very heavily doped substrates with N+ layers under the contacts the effect was negligible or not present at all. The effect was also less pronounced on transistors where the active layer was very thick where the contacts were placed, and the gate was located in an etched down region.

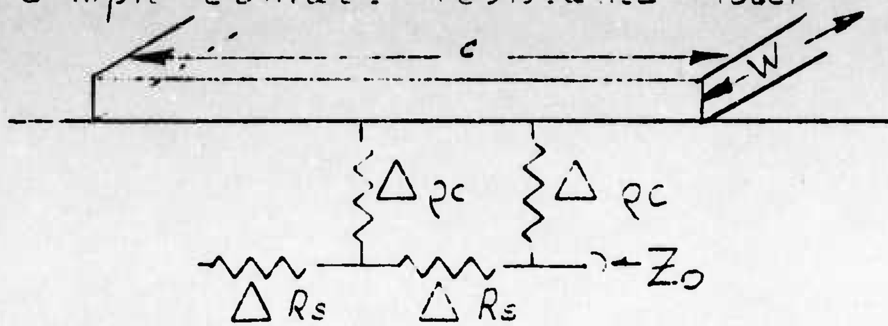
To explain these phenomenon a new model of the contact resistance for gallium arsenide FET's was needed. The usual model for contacts on semiconductors [1] is based on a transmission line as shown in Figure 7A. Among the assumptions made with this type of model is that the thickness of the epitaxial layer, or the layer upon which the contact is made, is many times thicker than the penetration of the contact itself into the layer. For very thin layers such as are used in gallium arsenide microwave FET's this assumption may not be valid. A modified transmission line model is therefore proposed which recognizes the importance of the penetration of the contact into the epitaxial layer. Figure 7B shows the model and the appropriate equations which have been developed from this model. Using this model it is now possible to calculate the contact resistance for contacts on gallium



Effect of Alloying Time on Contact Resistance

Figure 6

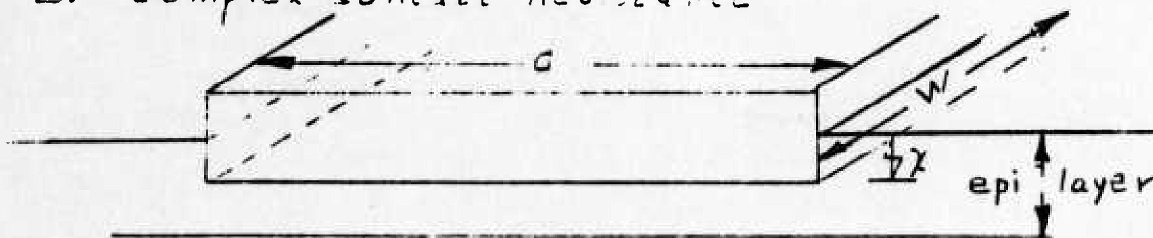
A. Simple Contact Resistance Model



$$R_{con} \doteq Z_o = \frac{1}{W}\sqrt{\rho_c R_s}\quad \coth d\sqrt{\frac{R_s}{\rho_c}}$$

Eq1 $\quad \cong \sqrt{\frac{\rho_c R_s}{W}}$, if d is large or ρ_c is small

B. Complex Contact Resistance



Eq2 $$R_{con} = \frac{\frac{\rho_c}{W}\sqrt{\rho_c \rho_B}}{\rho_c\sqrt{a-x} + x\sqrt{\rho_c \rho_B}},$$ d large or ρ_c small

d = Contact length
W = Contact Width
x = Contact Penetration
a = epi thickness

ρ_c = contact Resistivity, ρcm^2
R_s = Sheet Resistance, epi $= \frac{\rho_B}{a}$

Figure 7

arsenide for varying degrees of penetration and epitaxial layer characteristics. Figure 8 shows calculations for three types of layers. The lightly doped layer has a very steeply changing characteristic and is minimum at zero penetration. The middle curve which is for a typical FET is nowhere near as sensitive to the contact penetration whereas the bottom curve which was calculated for a relatively heavily doped layer shows that it is very insensitive to the amount of penetration of the contact.

The results of this part of the investigation have been quite useful since they have pointed out the necessity of either using N+ contact layers or using relatively thick active layers under the contacts and thinned regions under the gates.

4. Gunn Mode

For transistors that are built on semi-insulating substrates without a buffer layer there is a fairly wide transistion region between the active layer and the substrate which is capable of sustaining Gunn oscillations. Measurements taken on devices exhibiting oscillations of this type has shown that the frequency lies between 27 and 40 GHz. From a circuit viewpoint, it is impossible to suppress this type of oscillation since the electrical length within which it occurs is normally much shorter than the tuning length of the elements required for an amplifier in, say X-band. The most obvious indication of Gunn oscillations is the characteristic on the curve tracer as shown in Figure 4C.

The solution to this problem is, obviously, the elimination of the anomalous layer between the active layer and the substrate. A small percentage of all substrates are free from Gunn oscillations after the active layer has been grown. However, the selection of substrates as a solution to the Gunn oscillation problem is not considered practical from an economic viewpoint. A much better approach is simply to build in an adequate buffer layer between the substrate and active layer. In order to insure the elimination of Gunn oscillations it appears there is a minimum thickness for the buffer layer, in the order of 6-10 microns. No Gunn oscillations have been encountered in buffered devices, providing the thickness of the epi layer was adequate.

5. Reliability

The reliability of gallium arsenide FET's has been a subject of considerable interest and speculation. Of all the activities which have taken place on this particular program, reliability has by far atrracted the most interest from Avantek's customers and others interested

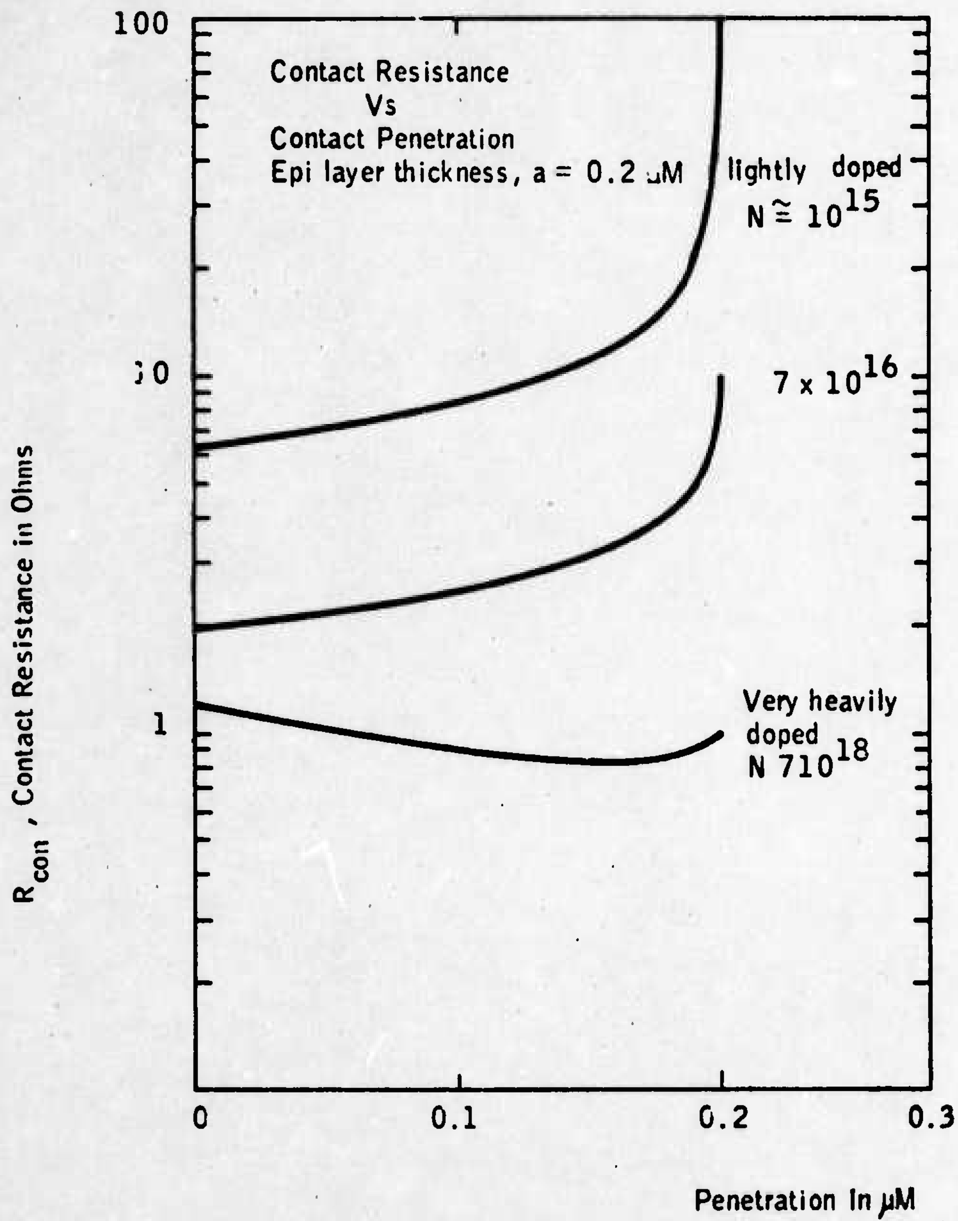


Figure 8

in gallium arsenide FET amplifiers, in general. Early Esaki and Gunn devices suffered from reliability problems associated with the material itself. As a result, some potential users of gallium arsenide FET's, were initially at least put off by this record. However, at this time, it appears that the reliability of GaAs FET's will be excellent and perhaps better than many other solid state devices. These improvements in reliability can be attributed to two factors:

- Gallium arsenide material has undergone a tremendous improvement in quality since the early days.
- The doping levels used in gallium arsenide FET material , particularly for the active layer, are such that reliability problems would be very unlikely.

The results of this program to date indicate that the reliability of gallium arsenide FET's operated at a junction temperature of 100°C should be in excess of 10^6 hours.

A brief outline of the reliability program is as follows:

Approximately two years ago Avantek made a reliability study on gallium arsenide FET's and FET amplifiers with test temperatures up to 100°C. Although the tests continued for almost two years, no failures were encountered which in itself was a very encouraging result. However, since there were no failures it was impossible to determine just what the MTBF of FET's would be. The first phase of the ECOM program was therefore dedicated to determining at what temperature FET's would start to fail. This information could then be used to make more extensive tests to find the actual MTBF. The second phase of the test would then consist of operating FET's at an elevated temperature or temperatures and recording the number of failures versus time. By doing the latter test at more than one temperature, a redundancy in the data is obtained which would give a considerably greater degree of confidence in the numbers derived. Phase II results would yield, in addition to the actual number for the MTBF, a number for the activation energy, and finally, the nature of the failure modes. Phase I has now been completed. The details of the test are as follows:

A total of fifty packaged one micron FET's were completely tested for all DC parameters and RF parameters at 6 GHz. One half of the group were mounted on test boards designed to keep the transistor under bias at the temperature of the test. The other half

of the sample of fifty were simply stored in a petri dish in the test oven. The test itself was a step stress test with 25°C increments in the test temperature and a dwell time of one week (168 hours). The initial test temperature was 125°C. As the temperature was increased the test boards holding the biased transistors failed at 150°C. Since the test boards were of epoxy fiberglas construction, the failure was not unexpected. Therefore, the transistors under bias had to be eliminated from the test at this point. The first transistor failure occurred after the devices had been aged for one week at 200°C (a failure is a device which can no longer be biased normally or has a noise figure increase of 1/2 dB). The first failure was an abnormal increase in the gate-source leakage which quickly became a gate-source short as the testing progressed. This kind of problem occurs frequently when life testing active devices: a device is degraded in doing the life test and is converted to a complete short during the actual testing of the device. The problem arises from the fact that in FET's the amount of energy to cause a massive failure is extremely small once the failure is initiated.

The test continued on until 275°C was reached, at which point a total of ten devices had failed. The results are displayed graphically in Figure 9. The results were then replotted on reliability paper (Figure 10). For a step stress test, this type of plot yields one useful piece of information, i.e., the temperature at which the average life of the device is equal to the dwell time of the test. Thus, the data shows that at 302°C the average life of the FET would be 168 hours or one week.

A step stress test carried out at only one dwell time does not yield the activation energy of the failure mode. The step stress test just described did however, indicate the types of failures to be expected with FET's operating at elevated temperatures. The two types of failures were:

- Gate degradation; gate short or high leakage
- Contact resistance increase

Both of these failures are related to the migration of gallium through the gallium arsenide. This conclusion was reached based on the fact that we were able to find local accumulations of pure gallium at the points where the gates shorted to the source in those devices which failed in that manner. For the transistors that failed through degraded noise figure, as a result of increased contact (Figure 11) resistance, the contacts themselves showed (by means of an Auger analysis) that gallium had migrated all the way through to the top layer of the metal.

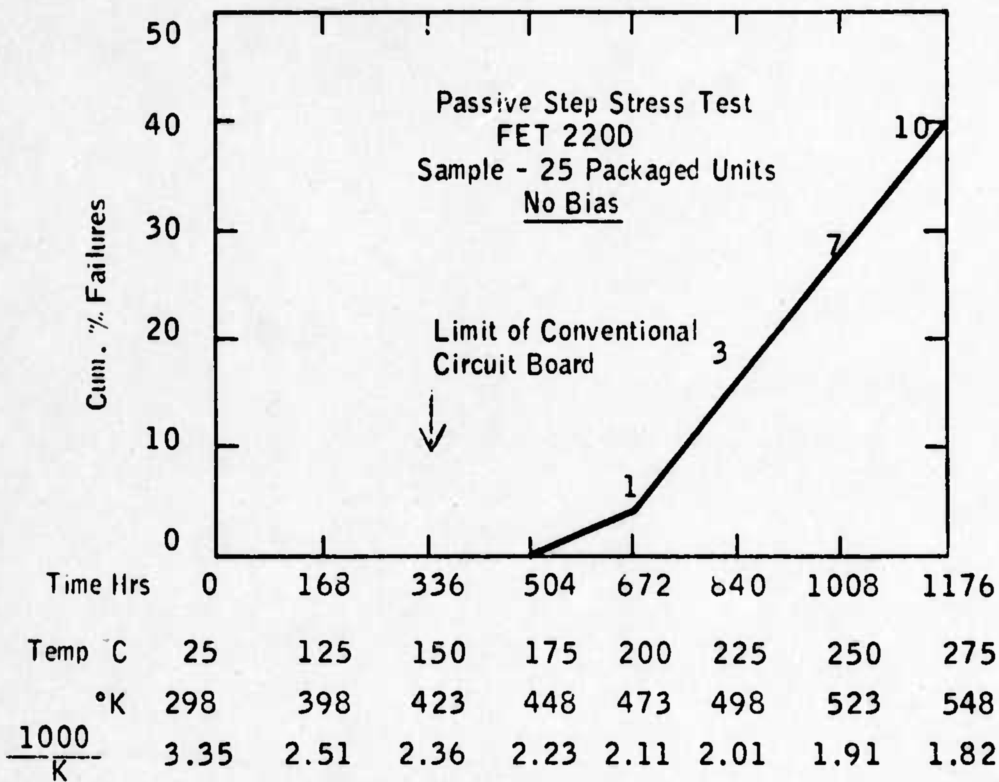
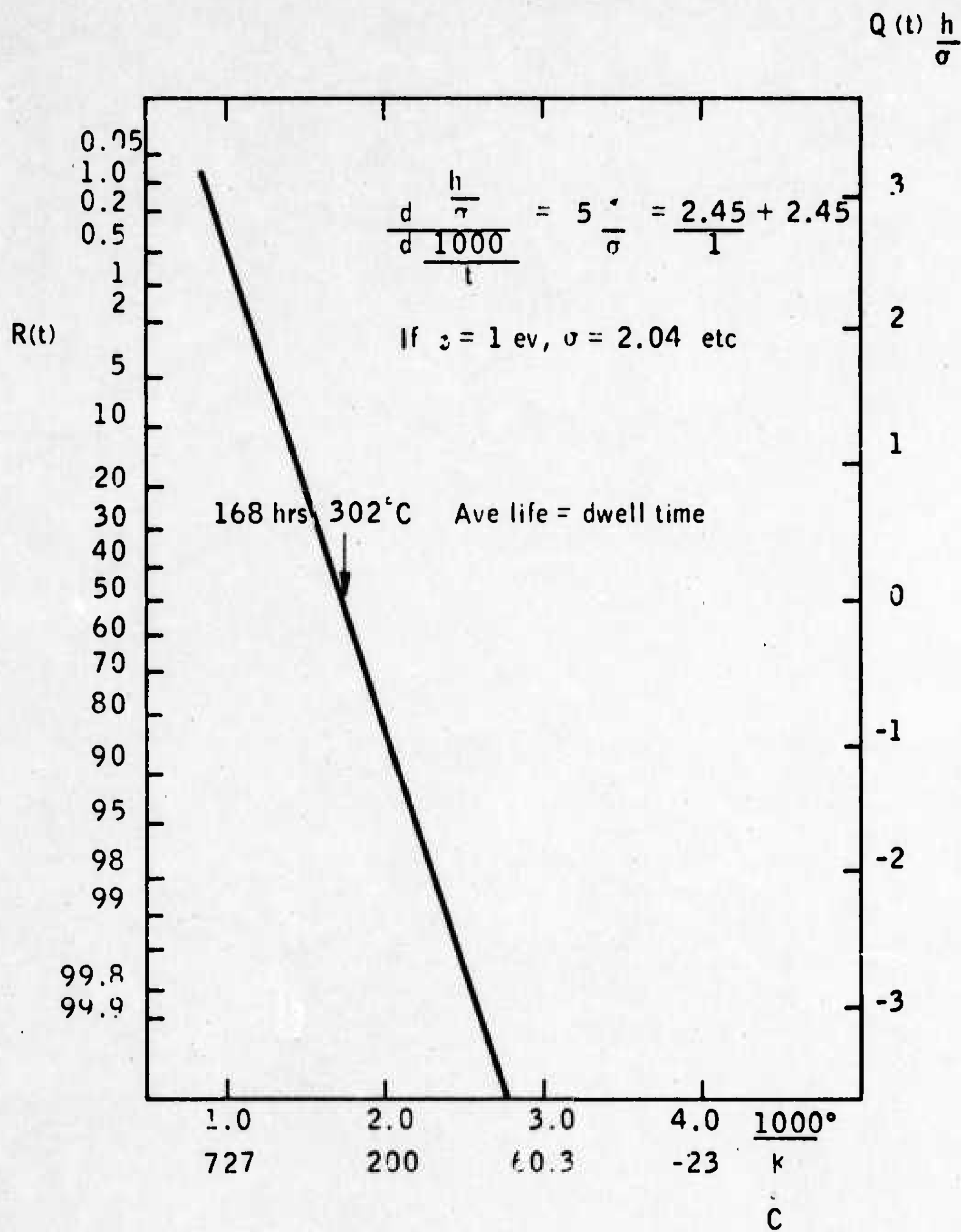


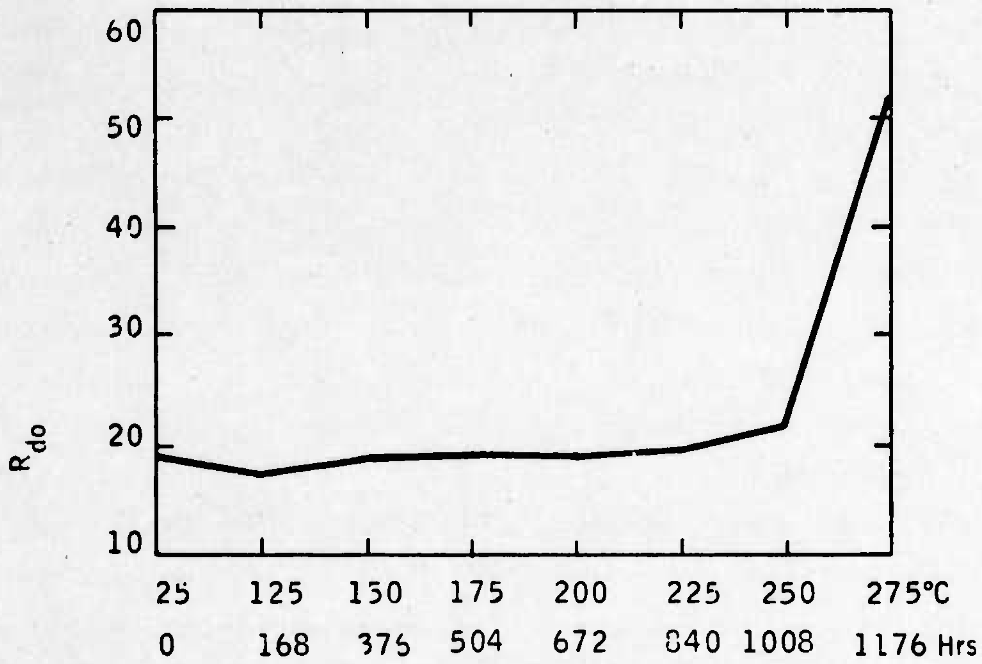
Figure 9



R(t) Versus 1000°K^{-1}

Figure 10

Low Field Drain Resistance, Rdo
Vs Time & Temp



Rdo = 2 X Contact Resistance + r_{ds} + r_{gd}

Figure 11

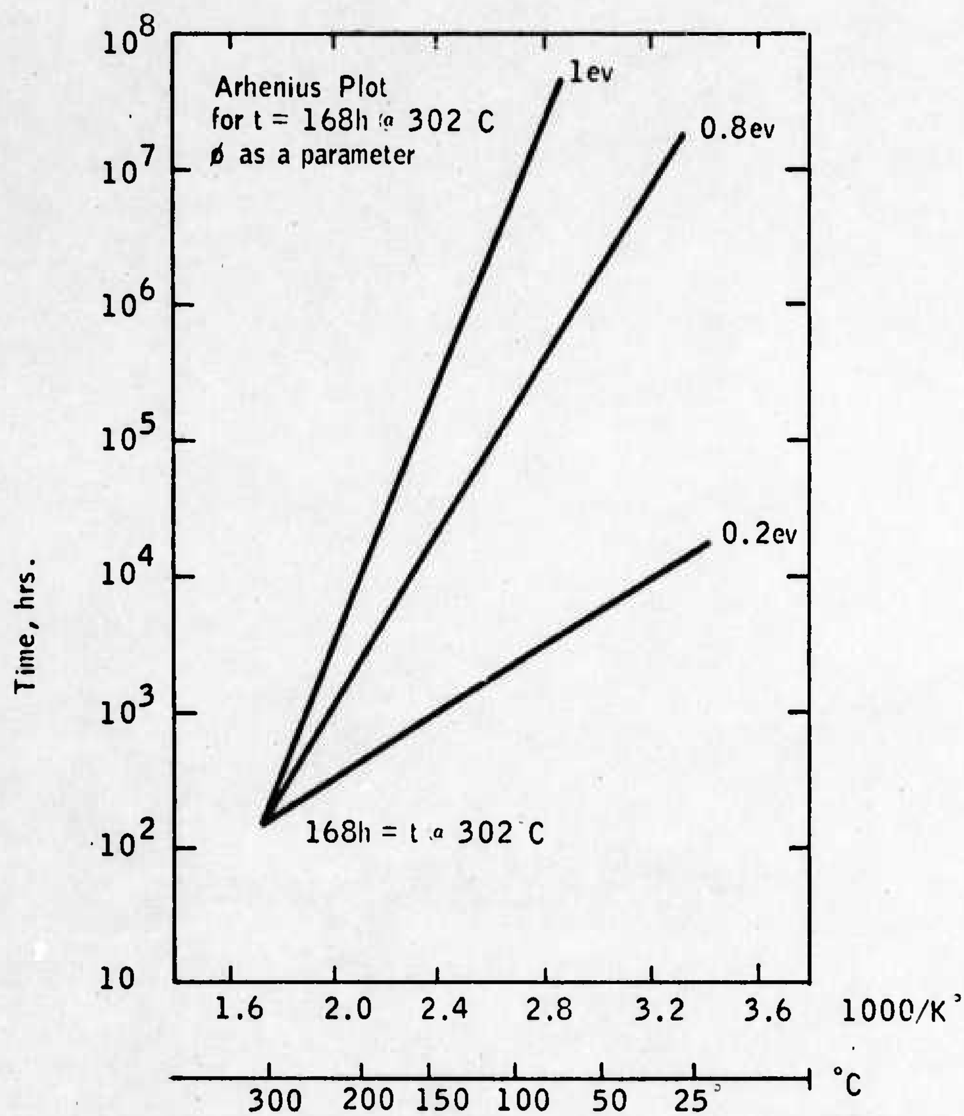
Published data, particularly from Bell Laboratories, indicates that the activation energy for the migration of gallium through gallium arsenide lies in the .8 to 1 electron volt range. Using this fact we can construct an Arhenius plot on the assumption that the activation energy in near 1 electron volt. The starting point on the plot, of course, is 168 hours MTBF at 302°. Such a plot is shown in Figure 12. This plot indicates that the MTBF for an FET operated at 100°C would be $5X10^6$ hours, approximately.

Before starting the final phase of the reliability test it was necessary to redesign the carriers for the transistors in order that they would be capable of standing temperatures up to 275°C. After examining the properties of various insulators available, it was determined that the only type of carrier which could be considered reliable at elevated temperatures such as would be needed for this test, would be ceramic. In addition, it would be necessary that the wiring and sockets for the test fixtures be capable of withstanding up to 275 or 300° in the oven. The new test fixture is shown in Figure 13. The base material is aluminia with nickel, overlaid with silver, contacts. The connecting wires which hold the ferrite beads are pure gold and are welded to the metal overlay on the ceramic. To hold the transistor against the ceramic base, a machinable glass disc is used. This disc in turn is held snugly against the ceramic by means of an inconel spring. The entire assembly is capable of withstanding temperatures up to 400°C.

The wiring for the oven is made of nickel-clad copper in a teflon fiberglas insulator. The sockets themselves use contacts formulated from a special berrilium-copper alloy. Some of the special components such as the sockets are available only on special order. This has slowed down the building of the final test chamber to operate to 300°C. The fixturing has been partially completed and checked out. The remaining test sites in the oven await the arrival of additional special card sockets.

6. Buffer Layer and Capacitance Problems

At the time this program was begun it was known that buffer layers, while solving some problems, could introduce other problems of their own. For example, it was known that if the conductivity of the buffer layer were not low enough, a high output conductance would result which would decrease device gain. However, this problem turned out to be relatively minor compared to some other ones which were discovered as the buffer layer implementation progressed. The first problem is associated with the capacitance between the gate pad and the



Arhenius Plot for t - 168h
@ 302°C ø as a parameter

Figure 12

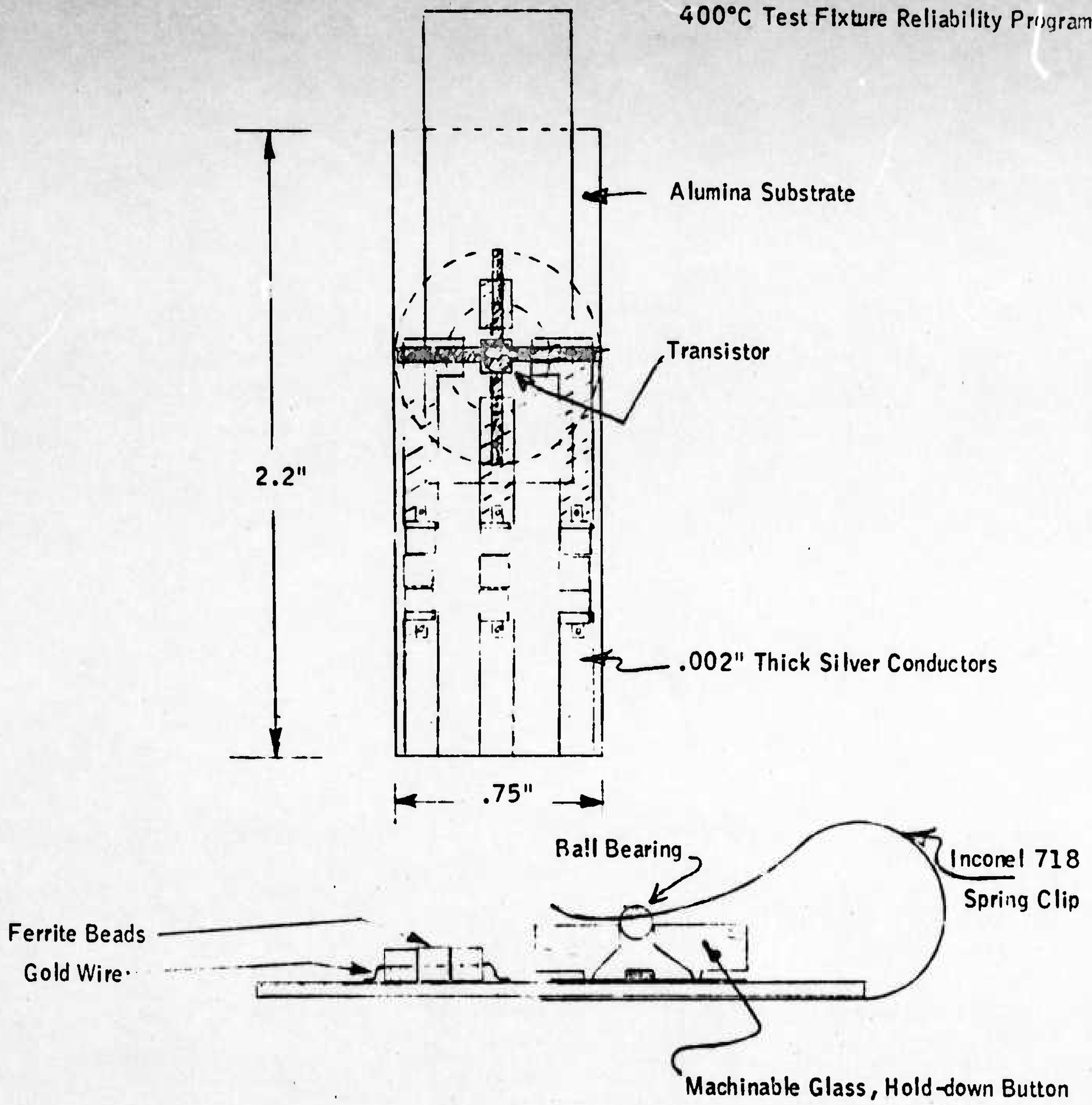


Figure 13

source of the transistor. For an FET to be easily bondable the area of the gate pad must be many times the area of the active gate. The ratio of the area of the gate pad to the active gate can be as low as 10 and as high as 70 for the various devices we have examined. The gate pad-to-source capacitance is a pure parasitic, which reduces the gain of the transistor, particularly at the higher frequencies. The magnitude of the capacitance between the gate pad and source depends upon the width of the depletion layer under the gate pad as well as the gate pad area. Thus, a large or wide depletion layer under the gate pad would tend to minimize the gate pad capacitance. In order for this to occur the doping level for the material adjacent to the gate pad must be very small relative to that under the active gate in the channel. The total gate source capacitance can be written as follows:

$$C_{gs} = \text{Area of gate} \cdot \left[\frac{q N_{act} \varepsilon \varepsilon_o}{2(V + \varphi_1)} \right]^{1/2} + \text{Area of gate pad} \cdot \left[\frac{q N_{buff} \varepsilon \varepsilon_o}{2(V + \varphi_2)} \right] = C_g + C_p$$

Where C_{gs} = Capacitance of active gate

C_p = Capacitance of gate pad

The above equation can be written in a somewhat more useful form which will show the importance of the various parameters affecting the gate pad capacitance.

$$C_{gs} = C_g \left[1 + \frac{A_p}{A_g} \left(\frac{N_{buff}}{N_{active}} \right)^{1/2} \right]$$

The ratio of $\frac{A_p}{A_g}$ is, of course, most unfavorable the larger it is. It is worst for FET's with very short gates (1/2 micron or less). The Avantek 1/2 micron FET has a ratio of 30 which, although high, compares favorably with competitive designs having ratios of 40 to 70. Using a ratio of 30 and an active layer doping concentration of 10^{17}, the maximum doping level in the region under the gate pad can be calculated for a given contribution of capacitance from the gate. For example, if the contribution of the gate pad is to be kept to only 10% of the total capacitance then:

$$\frac{A_p}{A_g}\left[\frac{N_{buff}}{N_{act}}\right]^{1/2} \leq 0.1 \quad ; \quad \frac{A_p}{A_g} = 30, \; N_{act} = 10^{17}$$

Then $N_{buffer} \leq 1.1 \times 10^{12}$

The above result indicates that the doping level under the gate should be in the 10^{12} range or less in order that the gate pad would not contribute significantly to the total gate capacitance.

While examining the gate-to-source capacitance in relation to the gate pad problem, it was discovered that the measured gate-to-source capacitance of an FET was always somewhat higher than the calculated value. An anomalous excess capacitance has also been reported by a research group at Stanford (Reference 2). As a result of the work on this contract it is now believed that the anomalous capacitance is actually the capacitance of the side wall of the depletion layer under the gate. The experimental evidence is very strong that this is indeed the case. It is felt that this result is new and worth publishing. A paper has been prepared and submitted to ECOM for approval to publish. The paper is included in Appendix I of this report.

III TEST SAMPLES

Four test sample transistors were delivered to ECOM (CLIN 0003) during the interval covered by this report. The samples were:

A. 2-1/2 micron FET's on buffer layers

B. 2-1/2 micron FET's

(a) one with polycrystalline GaAs passivation

(b) one without polycrystalline GaAs passivation

The buffered devices were included to demonstrate the advantages of such a type of structure (See Section I). The second sample, included at the request of ECOM, demonstrates the difference between passivated and unpassivated devices.

The data were presented in the form of a Test Report and included:

- DC test data
- 6 GHz noise figure and gain
- S parameters (HP, ANA)
- Curve tracer photos
- Other data

One of the major objectives of this program to increase the high frequency limit of FET's. The devices included in the sample are useful up to 18 GHz providing they are properly mounted. A standard FET package is useful only to about 10 GHz. Avantek has developed a carrier and transition which can be used to above 20 GHz. A test fixture complete with two microstrip to coax transition was therefore supplied to ECOM. Since the quality of match is a very important feature of the transition the return loss of each transition was measured. A short segment of microstrip terminated in a precision 50 ohm resistor was used for the test. The results are plotted in Figures 14 and 15. Through most of the range from 2 to 18 GHz, the return loss exceeds 24 dB (VSWR$\approx$1.2).

IV WORK FOR NEXT PERIOD

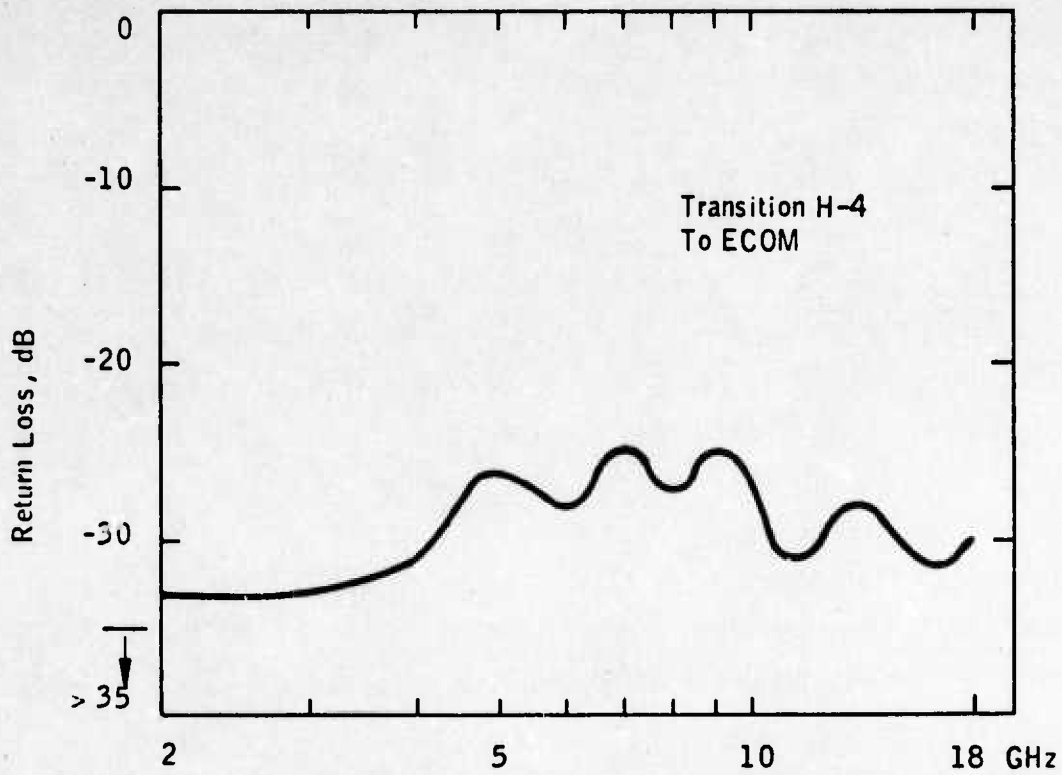
ECOM has requested that the work in the last half of the contract period would include an investigation into the exact causes of FET drift and how polycrystalline gallium arsenide affects this drift. A number of transistor runs will be made in which the slice is prepared with and without polycrystalline gallium arsenide. Transistors from these lots will then be assembled and tested for drift. If the drift is severe enough the transistors will then be considered candidates for more extensive tests. The tests will include the complete measurement of drift and RF characteristic of the transistor before the application and after the application of PGA. From this data a model can be built up which shows how PGA actually affects the device and what known physical properties could be responsible for these changes.

In addition to the drift investigation, noise mechanisms, cooled noise figure, and burn out levels, will be examined in the last half of the contract period.

V CONCLUSIONS

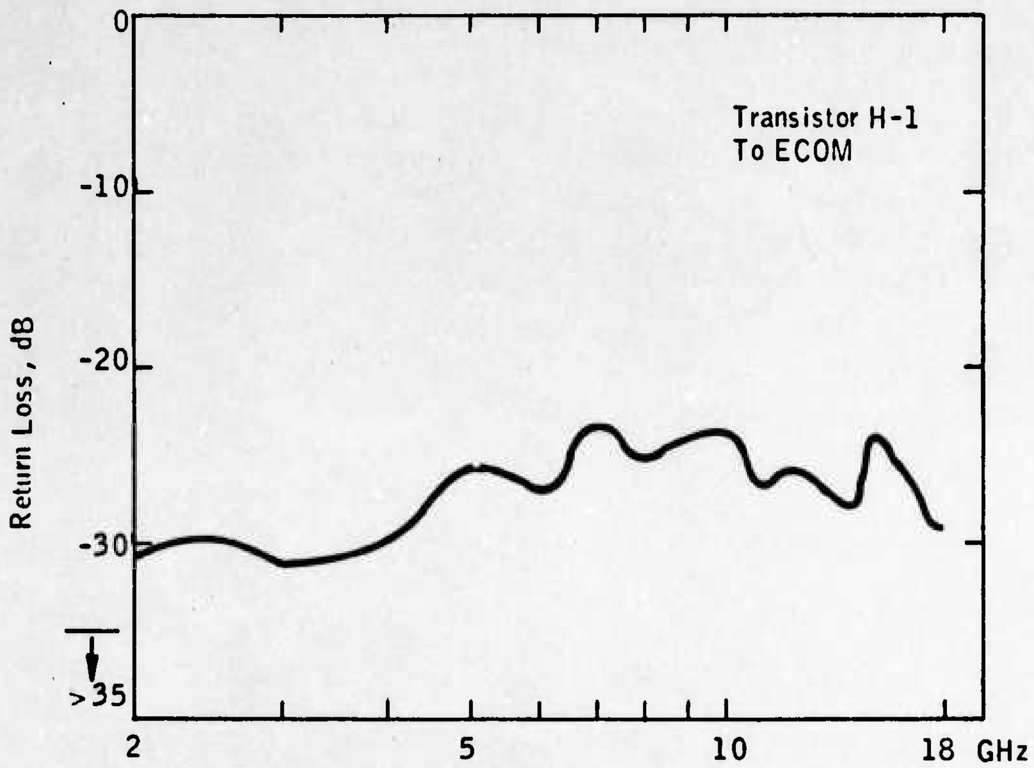
During the first half of this program a number of significant accomplishments were realized.

- Buffer layers were applied to transistors with the result that Gunn oscillations, break up, looping, and other backside problems were eliminated.
- A more accurate model for metal contacts on thin epitaxial layers was developed.
- A reliability study was initiated which results to date indicate that FET reliability will be excellent with MTBF's in the 10^6 range.
- A more complete model for the gate of an FET was developed which includes capacitances not heretofore known or defined.



Return Loss Versus Frequency
Transition No. H-4

Figure 14



Return Loss Versus Frequency

Transistion No. H-1

Figure 15

References

1. H. H. Berger - "Models for Contacts to Planar Devices," - Solid State Electronics, V. 15, pp 145-158, 1972.

2. Vasudev, P. K., et al; "Excess Capacitance and Non Ideal Schottky Barriers on Ga As," Solid State Electronics, Vol. 19, pp 557-559, 1976.

APPENDIX I

Avantek

ANOMOLOUS GATE CAPACITANCE IN GA AS FET's

By

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ANOMOLOUS GATE CAPACITANCE IN GA AS FET's

Introduction

It has been reported that Schottky barrier diodes (S. B.) on GaAs exhibited an excess capacitance which was designated as Co. [1] A similar capacitance has been found associated with S. B. gates on FET's. The value of Co measured varied from about 10% to over 50% of the actual active junction capacitance. As a result of this study it is now believed that this excess capacitance is associated with the sidewalls of the depletion layer. A synthesis of the C(V) plot using this theory and two models, produces a plot which both qualitatively and quantitatively duplicates experimental curves made from an FET.

Analysis

Figure 1 is a plot of C vs $[V + \varphi]^{-1/2}$ taken directly from an FET. Adjustments have been made to C, to take care of package, bonding pad and other extraneous capacitances. Using the medhod of [1] a value of .075 pf for Co is obtained by extrapolating the flat region of the plot through $[V + \varphi]^{-1/2} = 0$. The total gate capacitance is 0.440 pf when the device is biased for Id = 15 ma. Subtracting Co from this value gives an active gate capacitance of 0.36 pf. This number is in good agreement with the calculated value of Cgs based on the material profile. Thus Co seems to be an extraneous capacitance, not accounted for in the usual calculatation.

The exact shape of the depletion layer under the gate is not agreed upon in general, so a simplified synthesis is proposed as follows: Refer to Figure 2. To provide for a tractable analysis, Cgs is broken up into two components; C_1 the depletion layer capacitance and Csw, the sidewall capacitance. This model is not exact since it assumes a vertical edge to the depletion layer, rather than a curved one. The sidewall capacitance, Csw, is that of two orthogonal planes displaced by a distance equal to the depletion layer width, Xd. Capacitance per unit length for this topology is available in a closed form [2.] Using the original notation [2]:

$$\frac{Csw}{Wg} = 2\varepsilon\varepsilon_o K(k) \left[K(1-k^2)^{1/2}\right]^{-1} \left(\tfrac{1}{2}\right)^{*} \quad (1)$$

ε = dielectric constant of the medium

ε_o = permativity of free space, 8.85×10^{-14}

Wg = gate width

*The factor 1/2 is needed since the FET is not symmetrical about the X axis.

Fig 1

Profile of An FET
Experimental Data

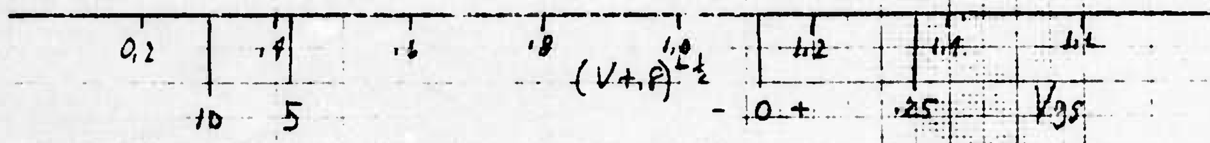
C_{gs} vs $(V_{gs}+.8)^{-\frac{1}{2}}$

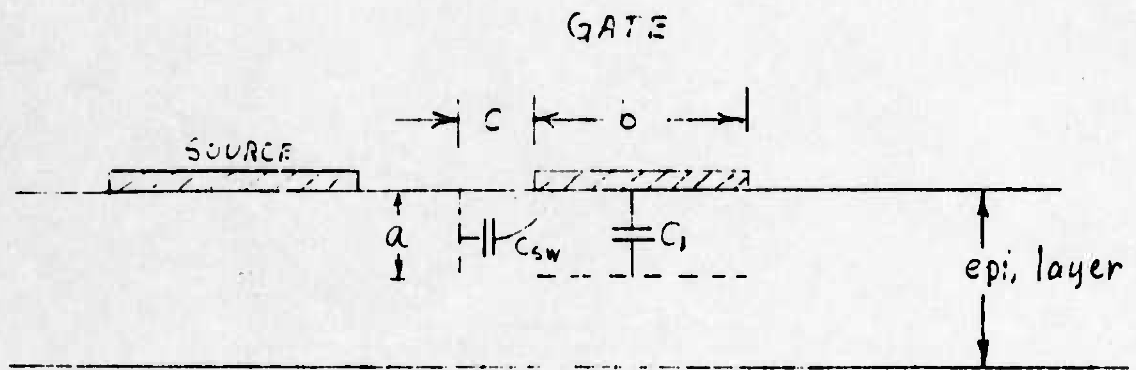
$N = 10^{17}$
$L_g = 1\mu M$
$W_g = 500\mu M$

C_{gs}

1.0
.9
.8
.7
.6
.5
.4
.3
.2
.1

15 ma point





$$k^2 = \frac{2a\left\{\left[(c+b)^2 + a^2\right]^{1/2} - \left[c^2+a^2\right]^{1/2}\right\}}{\left\{\left[(c+b)^2 + a^2\right]^{1/2} - a\right\}\left[(c^2+a^2)^{1/2} + a\right]}$$

Since $\quad x \doteq c \doteq a \,, \quad b \doteq L$

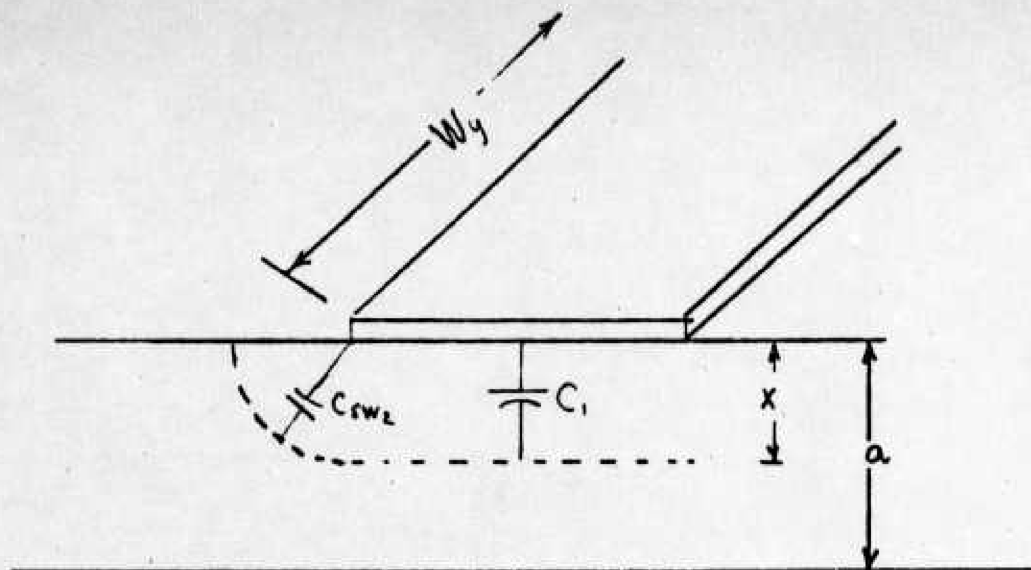
$$k^2 = \frac{\frac{2}{1+\sqrt{2}}\left\{\left[\left(1+\frac{L}{x}\right)^2+1\right]^{1/2} - \sqrt{2}\right\}}{\left\{\left[\left(1+\frac{L}{x}\right)^2+1\right]^{1/2} - 1\right\}}$$

L = gate length
x = depletion layer depth

Fig 2
First Model For Sidewall Capacitance

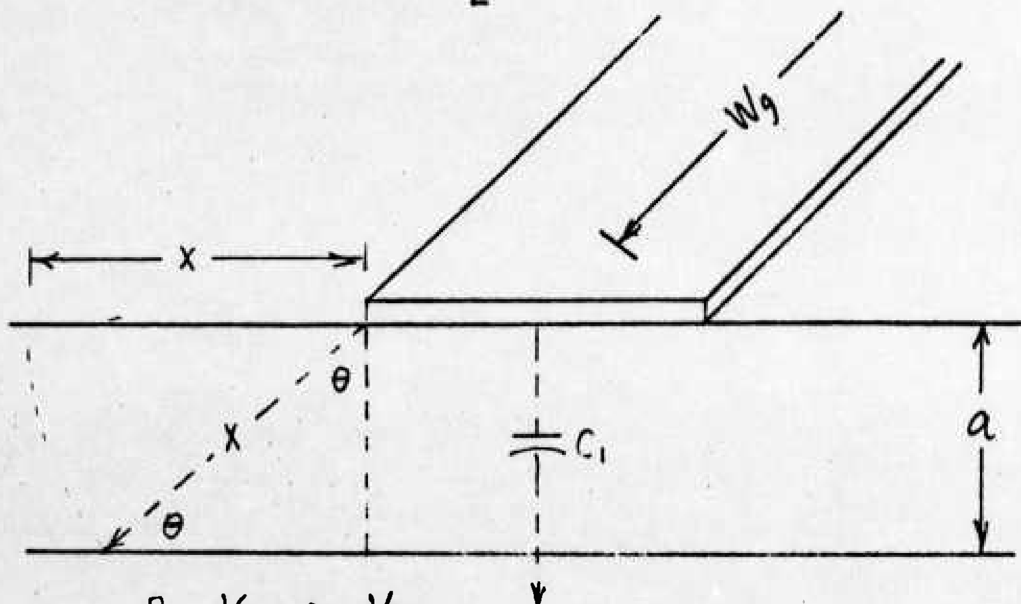
Fig. 3

Second or Quadrant Mode. For Sidewall Capacitance



A. $V_{gs} < V_p$

$$C_{sw_2} = \frac{\pi \varepsilon \varepsilon_0 W_g}{2}$$



B. $V_{gs} > V_p$

$$C_{sw_2} = \varepsilon \varepsilon_0 W_g \sin^{-1} \sqrt{\frac{V_p}{V_{gs}}}$$

TABLE I

Capacitance Parameters for an FET, $N = 10^{17}$, $a = 0.2\,\mu$, $W_g = 500\,\mu$, $L_g = 1\,\mu$

$\varepsilon\varepsilon_o W_g = 5.53 \times 10^{-14}$ $W_o = 2.89$ $V_p = 2.09$

V_{gs}	χ_d	$\frac{1}{\sqrt{V+.8}}$	k	C_{sw_1} from O.P. Model pf	C_{sw_2} from Quad. Model pf	C_1 pf	$C_1+C_{sw_1}$ pf	$C_1+C_{sw_2}$ pf	$\frac{C_{sw_2}}{C_1}$
+.62	.05	2.36	.895	.0753	.087	1.106	1.181	1.193	.078
+.54	.06	1.96	.893	.0749	↓	.922	.997	1.009	.094
+.45	.07	1.69	.891	.0745	↓	.790	.865	.877	.110
+.34	.08	1.47	.889	.0743	↓	.691	.765	.778	.126
+.21	.09	1.30	.887	.0739	↓	.614	.688	.701	.142
+.08	.1	1.18	.885	.0736	↓	.553	.627	.640	.157
-.24	.12	.98	.881	.0731	↓	.461	.534	.548	.189
-.62	.14	.84	.877	.0724	↓	.395	.467	.482	.220
-1.05	.16	.74	.873	.0716	↓	.345	.418	.432	.252
-1.54	.18	.65	.869	.0712	↓	.307	.378	.394	.283
-2.09	.20	.59	.865	.0706	↓	.276	.347	.363	.315
-5.0	.28	.415	.850	.0685	.039	0	.0685	.039	-
-10.0	.386	.30	.830	.0661	.026	0	.0661	.026	-

$K(k)$ and $K(1-k^2)^{1/2}$ are complete elliptic integrals, and

$$k^2 = \frac{2a\left\{\left[(c+b)^2 + a^2\right]^{1/2} - \left[c^2 + a^2\right]^{1/2}\right.}{\left\{\left[(c+b)^2 + a^2\right]^{1/2} - a\right\}\left[(c^2+a^2)^{1/2} + a\right]} \qquad (2)$$

This expression for k can be simplified somewhat by noting that

$$X \overset{\circ}{=} a \overset{\circ}{=} C$$

$$L = b$$

then

$$k^2 = \frac{\frac{2}{1+\sqrt{2}}\left\{\left[(1 + \frac{L}{X})^2 + 1\right]^{1/2} - \sqrt{2}\right\}}{\left\{\left[(1+\frac{L}{X})^2 + 1\right]^{1/2} - 1\right\}} \qquad (3)$$

Using this method, the values of C_1 and Csw were calculated for an FET with the following parameters:

Lg	=	1 μM	φ	=	0.8V
N	=	10^{17}	Vp	=	2.09V
tepi	=	0.2 uM			
Wg	=	500 μM			
ε	=	12.5 i.e., GaAs			

Table 1 presents the data for values of X varying ±0.05 to 0.3 uM. The pinch off point is 0.2 uM.

Since the vertical dimension of the sidewall increases as X increases, Csw remains essentially constant while C_1 varies appreciably. If C_1 + Csw is plotted vs $V + \varphi^{-1/2}$, the curve of Figure 4 results. Compare this plot with Figure 1. Up to the pinch off point, the plots are almost identical, as to slope and Co intercepts.

An alternate model for the sidewall capacitance is obtained by computing the charge contained in a cylindrical quadrant as shown in Figure 3. The total charge is

$$Q_{sw} = qN\pi \frac{X^2}{4} Wg \quad (4)$$

For an abrupt junction,

$$V = \frac{X^2 qN}{2 \varepsilon \varepsilon_o} \quad (5)$$

Then computing C,

$$Csw = dQ/dV \quad (6)$$

$$= \frac{\pi \varepsilon \varepsilon_o Wg}{2}$$

$$= 1.7 \times 10^{-12} Wg, \text{ and is independent of } X$$

For the transistor considered Wg is 500 μM, and Csw = .086 pf

This value is in somewhat better agreement with the experimental results, since the quandrant is a better approximation of the actual depletion layer shape. Beyond pinch-off a more complex model is required and

$$Csw \cong \varepsilon \varepsilon_o W_g \sin^{-1} \left[\frac{V}{V_p} \right]^{1/2} \quad (7)$$

$$\text{At } V = V_p, \quad \sin^{-1} 1 = \frac{\pi}{2} \quad (8)$$

and equations (6) and (7) agree.

Since Csw is not associated with the channel modulation, it is desirable that the ratio Csw/C_1 be minimized. This means (Table 1) that the device should be operated at low gate-bias. However, a low gate bias means high Id (and high noise figure) unless the FET has a value for Idss closer to the normal operating current. We have observed that lower Idss devices in general have better rf performance. The sidewall capacitance may be the critical factor.

Beyond pinch off, the sidewall capacitance is the dominant component of Cgs. It should be noted that the extrapolated value of Co is always slightly larger than that obtained beyond pinch off. This is because, Csw continues to deplete to a value less than that in the active region, i. e., Co.

Circular diodes are commonly used to profile epitaxial material. Since the sidewall capacitance is a possible source of error, it is useful to compute the minimum diode size to insure that the profile is that of the region of interest. For example, if the active layer is 0.2 uM and the buffer 10 microns, and an accurate measurement of the buffer is desired, there will be a minimum diode size for any degree of accuracy.

Letting $X_{active} = 0.2\,\mu M$, $N_{buffer} = 10^{13}$
$X_{buffer} = 10\,\mu M$, $N_{active} = 10^{17}$

At pinch off for the buffer

$$C_1 = \frac{\varepsilon \varepsilon_o \pi d^2}{4} \cdot \frac{1}{X_{active} + X_{buffer}}$$

$$= \frac{\varepsilon \varepsilon_o \pi d^2}{4.08 \times 10^{-3}}$$

The voltage to pinch off the buffer and active layer is:

$$V_{total} = V_p \text{ active} + V_p \text{ buffer}$$

$$= 2.09 + \frac{(X_{buff})^2 \; q \; N_{buffer}}{2 \varepsilon \varepsilon_o}$$

$$V_{total} = 2.09 + \frac{(10^{-3})^2 \; 1.6 \times 10^{-19} (10^{13})}{2(12.5)\;(8.85 \times 10^{-14})}$$

$$= 2.09 + .72$$

$$= +2.81\,V$$

Then the sidewall capacitance is (Eq. 6)

$$C_{sw} = \varepsilon \varepsilon_o \pi d \sin^{-1} \sqrt{\frac{V_p}{V_t}}$$

$$= 1.04\, \pi\, d\, \varepsilon \varepsilon_o$$

If 1% accuracy is desired; $C_1/C_{sw} = 100$

$$100 = C_1/C_{sw} = \frac{d}{(.08\times10^{-3} \times 1.04}$$

$$d \cong 0.5 \text{ cm}$$

Where an accurate profile of the active layer only is needed (the usual case), then:

$$C_1 = \frac{\varepsilon\varepsilon_0 \pi d^2}{4(.2\times10^{-4})} = \frac{\varepsilon\varepsilon_0 \pi d^2}{0.8\times10^{-4}}$$

$$C_{sw} = \varepsilon\varepsilon_0 \pi d \,\sin^{-1}(1) = \frac{\varepsilon\varepsilon_0 \pi d^2}{2}$$

Therefore:

$$\frac{C_1}{C_{sw}} = 100 = \frac{d_{min}}{\pi(1.6\times10^{-4})}$$

$$d_{min} = .0126 \text{ cm}$$

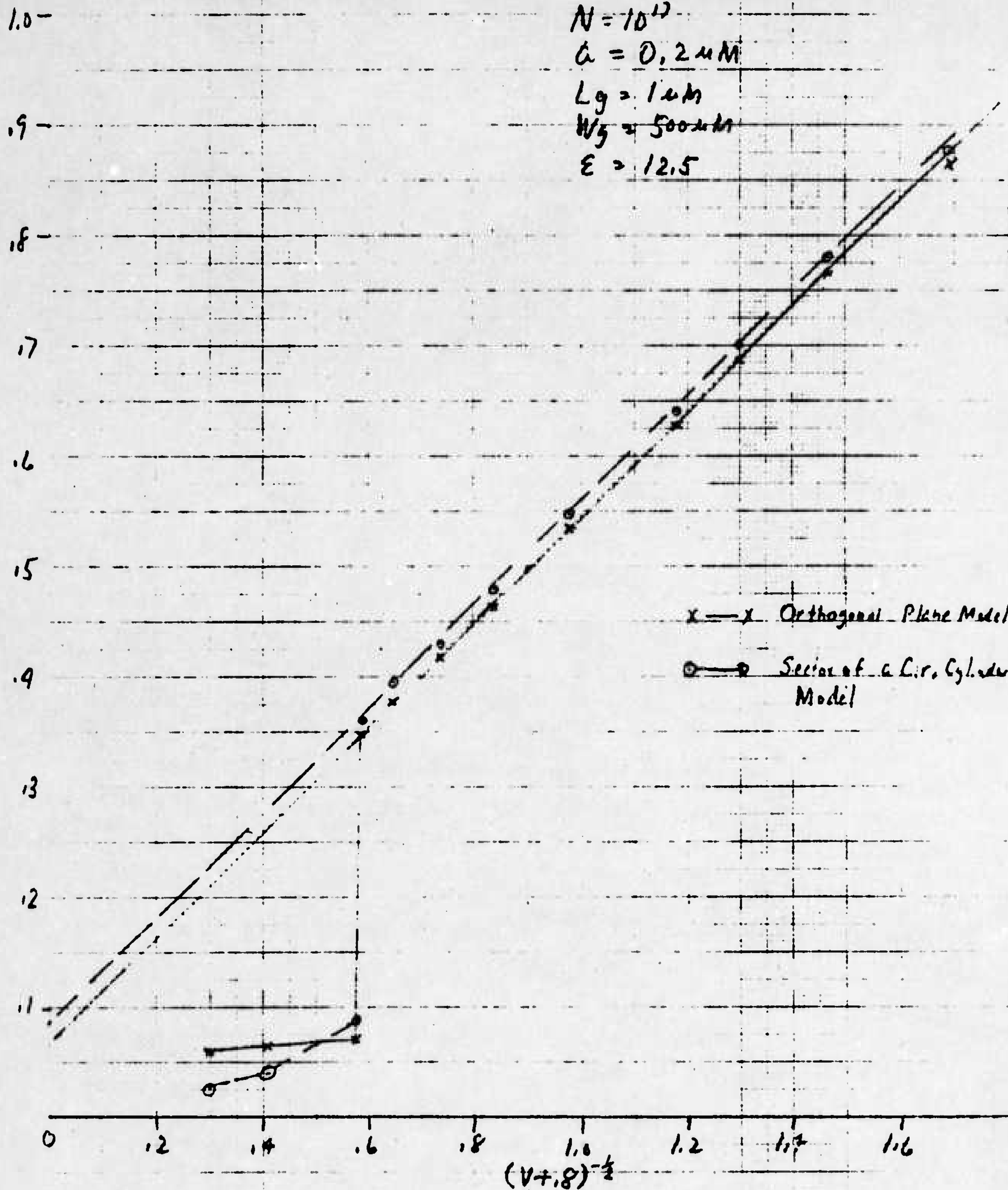
$$\cong 5 \text{ mils}$$

Conclusion: The value for sidewall capacitance has been computed using two models, with a radically different approach. Results were both very close to the experimental data. While the or thoganal plane model is not as accurate as the other model, it does have the advantage of a single expression for Csw which can be used both below and beyond pinch off for the active layer. The computation for minimum diode size indicates not only the size needed, but also that an FET gate profile cannot delineate the buffer without corrections for Csw.

References:

(1) Vasudev, P. K., et al, "Excess Capacitance and Non Ideal Schottky Barriers on GaAs," Solid State Electronics, Vol. 19, pp. 557-559, 1976.

(2) American Inst. of Physics Handbook, McGraw Hill, New York, 1972, p. 5-16, eq. 6.



Cgs
Fig 4
Computed Profile
For an FET
N = 10^17
a = 0.2 uM
Lg = 1uM
Wg = 500uM
ε = 12.5
1.0
.9
.8
.7
.6
.5
.4
.3
.2
.1
0
.2
.4
.6
.8
1.0
1.2
1.4
1.6
(V+.8)^-1/2
x — x Orthogonal Plane Model
Sector of a Cir. Cylinder Model

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