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LINCOLN EXPERIMENTAL SATELLITE (8/9) SIMULATION

SYSTEM DEVELOPMENT BRANCH
SYSTEM AVIONICS DIVISION

SEPTEMBER 1976

TECHNICAL REPORT AFAL-TR-76-198
FINAL REPORT FOR PERIOD AUGUST 1974 to MARCH 1976

AIR FORCE AVIONICS LABORATORY
AIR FORCE WRIGHT AERONAUTICAL LABORATORIES
AIR FORCE SYSTEMS COMMAND
WRIGHT-PATTERSON AIR FORCE BASE, OHIO 45433

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This technical report has been reviewed and is approved for publication.

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FOR THE COMMANDER

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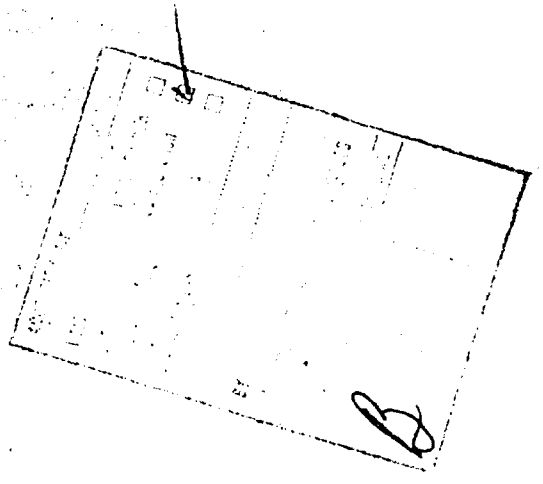

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This document provides a description of the in-house work performance in the Air Force Avionics Laboratory's Communication Systems Evaluation Laboratory (CSEL) to successfully implement a Lincoln Experimental Satellite (LES 8 or 9) simulator. The work description covers both the software and hardware aspects of the simulator's implementation.

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FOREWORD

This technical report was prepared in the System Avionics Division (AA), System Development Branch (AAD) of the Air Force Avionics Laboratory, Wright-Patterson Air Force Base, Ohio. The work was accomplished under Project No. 1227, "Advanced Microwave Communications", Task No. 122712, "Communication Test and Evaluation", Work Unit No. 12271218, "Lincoln Experimental Satellite (8/9) Simulation". The Project Engineer was Mr. John Mayhan (AFAL/AAD).

Acknowledgment is given to Mr. John Garrett (AFAL/AA/DAIS), whose programming expertise was greatly appreciated and to Messrs. William Jardine and Martin McLain of System Research Laboratory for their maintenance of the RF portion of the system.

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SECTION I

INTRODUCTION AND SUMMARY

This document provides a description of the work performed in the Air Force Avionics Laboratory's Communication Systems Evaluation Laboratory (CSEL) under the in-house work unit 12271218, titled "Lincoln Experimental Satellite (8/9) Simulation". The main objective of this program was to develop a limited Lincoln Experimental Satellite (LES 8/9) simulator, using the Programmable Data Terminal (PDT) and the Signal and Interference Generator (SIG) housed in the CSEL. In order to accomplish this overall objective, four basic in-house tasks were successfully completed under this work unit. They are: (1) the development of the appropriate software for the PDT to implement a 700 MHz intermediate frequency (IF) satellite simulator, (2) the integration of this IF satellite simulator with the SIG to achieve an overall satellite simulator operating at the proper operational frequencies of LES 8 and 9, (3) the implementation of self-test modes for validation of various portions of the system, and (4) the integration of the overall simulator with the K band and UHF modems and terminals that were designed for operation with the actual satellites. Aside from these four basic tasks, there were numerous detailed, but nonetheless important, tasks associated with implementing a system of this size. Most of these detailed tasks pertain to specialized hardware and interface problems which are too numerous to elaborate on in this report.

In the successful completion of task 4 it has been demonstrated that all of the simulated satellite modes that will be subsequently described in the remainder of this report are indeed operational. Various experimental tests using the modem/terminal/simulator have been, and are currently being, performed in conjunction with the flight test group. These tests have shown that the simulator is a valuable experimental tool and, if kept in its proper prospective with due regard to its capabilities and limitations, should continue to serve as such.

The in-house work that was performed to successfully implement the satellite simulator will be described in this report from both the software and hardware aspects. In this description, however, much information about the actual details of the LES 8 and 9 satellites, as well as the Programmable Data Terminal and Signal and Interference Generator, is utilized. It is not possible to elaborate in detail on any of these topics in this report. Detailed information on the LES 8 and 9 satellites are contained in numerous reports, most notably 1, 2, 3 and 4. Descriptions of the Programmable Data Terminal and Signal and Interference Generator are given in 5 and 6 respectively.

There are some functional capabilities of the actual satellites that are not included in the satellite simulator described herein due to the limitations of the RF drawer and the digital processing speed of the Programmable Data Terminal. Since there is only

a single satellite simulator, all functions pertaining to the cross-link are absent. Among the more notable digital processing functions absent for a single satellite are the high rate conferencing 100,000 bits/sec differential quadraphase demodulator, all cover and decover operations and all telemetry insertions. One of the more important differences in the RF processing is due to the linear automatic gain control in the Programmable Data Terminal as opposed to the crystal filter/limiter combination in the actual satellite.

The report is divided into eight sections. Section II begins with a description of the IF satellite from a system point of view. In this section particular emphasis is devoted to providing insight into the input/output capabilities and limitations of the IF simulator, as well as to a partitioning of the IF simulator into analog processing and digital processing. The digital processing required for the simulator are described from a system point of view.

Sections III and IV follow with a description of the software programs that were generated to achieve the implementation of the digital processing described in Section II. A functional flow diagram approach is used throughout the software description rather than any elaborate explanation of detailed programming instructions. Section V continues the description of the simulator by considering the required interface of the IF satellite with the Signal and Interference Generator in order to provide the actual operating front end of the simulator. This is followed by Sections VI and

VII in which the implementation and capabilities of the self-test and operational modes of the simulator are described. The baseline performance of the two digital demodulators implemented via software (DQPSK and 8ary FSK) are also presented in terms of probability of error vs. bit energy to noise density ratio curves. Section VII concludes with an elaboration of a particular operational mode, namely the mode in which relative linear motion between the satellite and modem/terminals is simulated.

SECTION II

SYSTEM DESCRIPTION OF THE IF SATELLITE SIMULATOR

Before getting into the description of the work required in order to make the PDT "look like" the LES 8 or 9 satellite, the final IF satellite simulator that resulted from this effort will be described from a system point of view. The translation of the IF satellite simulator to the actual RF simulator will be covered in Section VI.

The basic system architecture of the IF satellite simulator is shown in Figure 1. The 700 MHz input signal consists of either the K band Forward and/or Low Rate Conferencing (LRC) uplink signals, or the UHF Report Back (RB) uplink signal, associated with LES 8 or 9 when these signals are linearly translated to a 700 MHz IF frequency. In fact, for the case of the Forward and/or LRC modes, the 700 MHz uplink signal generated by the K band modem/processor may (with the exception of power levels) be directly interfaced with the input to the IF simulator. For the case of the RB mode, the output of the ARC-151 must be linearly translated by 332.5 MHz, and again adjusted in power levels, before uplink interfacing can proceed.

There are two 700 MHz outputs associated with the simulator. The first is a 700 MHz carrier differentially phase shift keyed (DPSK) modulated by either a 200 b/s, 10,000 b/s, or 100,000 b/s data bit stream. The second is an 8ary frequency shift keyed (FSK)

modulated signal which is identical to the UHF downlink signal structure of LES 8 or 9 when linearly down converted by 457.4 MHz. The DPSK modulated output signal format for the 200 b/s and 10,000 b/s mode is the same as the 200 b/s and 10,000 b/s K band downlink format of LES 8 and 9 (report back mode included), with the exception of the covering and telemetry insertions. The 100,000 b/s DPSK output signal structure is the K band downlink signal structure generated by the LES 8 or 9 satellite when the satellite is being operated in the high rate report back mode only, again with the above exceptions of covering and telemetry insertions.

The baseband outputs of the satellite simulator consist of data and clock bit streams at either 200 b/s, 10,000 b/s or 100,000 b/s rate. These baseband data bit streams are identical to the data bit streams that are DPSK modulating the 700 MHz carrier to achieve the IF downlink K band signal structure. These output bit streams were appropriately interfaced so that they may be routed directly to the K band modem/processor at the port where it receives the demodulated downlink data and clock from the K band terminal. Thus, using the 700 MHz output of the K band modem/processor and the above respective bit stream outputs of the IF satellite simulator, the simulator may be used directly with the K band modem/processor, bypassing the K band terminal.

Also shown in Figure 1 are seven auxiliary inputs and outputs labeled: start switch, real time clock display, doppler commands,

mode commands, 12 MHz frequency synthesizer, initial clock load and the 1 pps output of the Rubidium standard. The mode command refers to the sixteen-bit front panel master switch register by which various modes (including self-test modes) of the satellite may be executed. For actual operation with the UHF and K band modems and terminals, the primary function of the switch is to command the simulated satellite to the Forward and/or LRC modes, or the high or low rate report back modes.

The 12 MHz frequency synthesizer, driven by a Rubidium standard, provides the basic source of timing for the three programmable interrupts of the PSP as well as the basic reference frequency to drive the RF drawers of the PDT. By offsetting this source from its nominal value of 12 MHz, relative linear motion between the satellite simulator and the K band and UHF terminals may be simulated. However, since both transmitting and receiving functions of the simulator are controlled by the same clock, care must be taken to properly interpret the effects of this offset. The simulation of relative linear motion is explained in further detail in Section VIII.

The initial clock load and frequency offset commands shown in Figure 1 refer to front panel mounted thumb wheel switches which may be used to manually insert various frequency offsets and arbitrary real time starting epochs. The frequency commands merely offset the receive and transmit frequency synthesizer accordingly, and are in no way related to the frequency offset incurred when

offsetting the basic 12 MHz source. For operational purposes, a real time counter calibrated in hours, minutes and seconds is used to display satellite time.

Also interfaced to the programmable data terminal is a 1 pps output of either a Rubidium standard or WWV receiver. This 1 pps input to the simulator, in conjunction with an initial clock load, allows the simulated satellite to be time synchronized with either the time epoch display on the Rubidium standard or WWV receiver. In effect, this is accomplished by loading the desired start time via an initial clock load and, on activating the start switch, the program and interrupt clocks will start on the next one-second input tick. Hence, the normal mode of K band modem/processor time synchronization may be employed when using the simulated satellite.

A further breakdown of the IF satellite simulator is shown in Figure 2 and essentially depicts the partitioning of the Programmable Data Terminal into analog processing and digital processing functions. The incoming 700 MHz IF signal is routed to both of the receivers contained in the PDT. Here they are dehopped to a fixed 2 MHz frequency, passed through automatic gain control circuitry and subsequently downconverted to quadraphase baseband (I,Q) channels. At this point the baseband quadrature signals are filtered and sampled by analog-to-digital converters (twelve bits) at a rate dictated by the mode of the satellite. For the low rate conferencing receiver (receiver #1) the usable sampling rate is 5000 samples/second whereas

for the report back mode the sampling rate is either 5000 samples/second or a hard decision (1 bit sign sample) sample at 50,000 samples/second. The sampling rate for the forward link baseband channel, or receiver #2, is always 3.2 KHz. The baseband filters that were constructed for receiver #1 are, of course, not the same for the 5000 sample/sec and 50,000 sample/sec modes and must be physically switched when these modes are switched.

Once the sample values of the baseband channels are ready, an interrupt to the computer is generated and the results of the A/D conversion are loaded into the computer at a rate dictated by the interrupt rate. The resulting software that was developed subsequently performs a frequency shift keyed (FSK) demodulation of the 8ary Forward link data, a differential quadraphase shift keyed (DQPSK) demodulation of the LRC data (or hard sample decision on the RB link), formats the resulting FSK and DQPSK demodulated data with the frame, forward/parity and slip sequence bits to achieve the K band downlink data, and block-encodes the forward data for transmission on the UHF downlink. Concurrently with these operations, the computer is calculating the next transmit and receive hop-dehop commands on a five-millisecond basis. A system diagram of these digital processing functions is shown in Figure 3.

SECTION III

THE OPERATIONAL PROGRAM FOR THE LOW RATE PROCESSING MODE

The low rate processing mode refers to the 200 b/s and 10 kb/s K band downlink modes of the LES 8 or 9 satellite simulator. The 100 kb/s downlink report back mode will be explained separately in Section IV.

The overall structure of the program generated to implement the functional operations depicted in Figure 3 is shown in Figure 4 and consists of five basic parts: start-up or initialization procedure, the main or executive program, and three interrupt programs executed at a rate of 10 KHz, 3.2 KHz and 10 KHz respectively. The start-up procedure is performed in all cases where an initial start or time synchronization is required. A functional diagram of the start-up procedure is shown in Figure 5. The program begins with a disable interrupt command, followed by an execution of the fixed digital commands which pertain to the RF transmitter and receiver operating modes (i.e., transmitters on or off, narrowband or wideband IF filtering, 70 MHz or 700 MHz operation, etc.). Subsequently, it then initializes all registers and variables used in the main program, as well as those used in the interrupt programs for bookkeeping purposes. This is followed with a loading of the initial clock epoch, which is inserted via thumb wheel switches mounted on the front panel, and goes into a wait loop

until the depression of the start switch. The initial clock epoch load always corresponds to a second mark. Upon the depression of the start switch the program waits for the next one-second tick of the Rubidium standard or WWV receiver. Upon receipt of this one-second tick, the three programmable interrupt clocks are loaded with their respective rates, interrupts are enables and an exit is made to the main program.

The three interrupt clocks, which are labeled C1, C2 and C3, are programmed to interrupt the main processing program at a 10 KHz, 3.2 KHz and 10 KHz rate respectively. Clocks C1 and C2 are inherently tied to the analog-to-digital (A/D) converters in RF drawers #1 and #2, respectively, and also control the sampling rate of these converters. When an interrupt is generated, digital data generated by these A/D converters are ready for processing by the computer. Clock C3 is independent of any external A/D device and simply interrupts the computer at its programmed rate. The priority of each interrupt goes from C1, highest priority, to C3, lowest priority. The timing epochs C1 and C2 are, for all practical purposes, identical, and the epochs of C1 and C3 are shown in Figure 6. The reason for choosing these particular epochs and rates will become clear in the description of the interrupt and main processing programs.

A functional flow diagram for interrupt #1 is shown in Figures 7a and 7b. From a system viewpoint, this interrupt has the responsibility of generating the RF transmit commands as well as the generation

of the baseband digital outputs; i.e., the 700 MHz differential phase shift keyed K band downlink, the 8ary FSK hopped UHF downlink, and the 200 b/s and 10 kb/s digital data bit stream and clock. In addition, interrupt #1 has the responsibility of implementing the proper K band downlink format and of utilizing the 10 KHz A/D samples associated with receiver #1 to perform the LRC DQPSK demodulation algorithm, or the RB hard decision demodulation algorithm. As depicted in Figure 7a, the interrupt is entered at a 10 KHz rate with a pair of in-phase (I) and quadrature (Q) samples. The input baseband signal is therefore sampled at twice the rate required for the LRC or the low rate RB mode. The particular reason for choosing the 10 KHz rate is that the interrupt also generates the 10 kb/s commands to the PSK demodulator and also the 10 kb/s digital data output bit stream. To perform the DQPSK or hard decision demodulation algorithm, therefore, only alternate samples of this input are used.

The first command upon entering interrupt #1 is the determination of whether the 200 b/s downlink or 10 kb/s downlink mode is being exercised. If it is the 10 kb/s mode, there is a transfer of an A bit to the 700 MHz phase modulator of transmitter #1. Initially, this A bit is an arbitrary bit used for phase reference. This command is followed by a transfer of a B bit (again first time arbitrary) to the output device which generates the 10 kb/s digital data bit stream. The next decision pertains to the UHF downlink frequency control.

The time of this output command (the bit command to the frequency synthesizer is ready at this point and has been calculated in the main program) is determined by counting the appropriate number of samples after a five-millisecond flag bit is set. The flag bit is set in interrupt #2 concurrently with a five-millisecond uplink dehop command.

If the initial decision had been made that the 200 b/s downlink mode was being exercised, the program would bypass the transfer of the A and B bits to their respective outputs and go directly to the UHF downlink decision. This UHF output command/decision is followed by a determination as to whether the next bit on the downlink bit stream of the 10 kb/s mode is to be a frame bit. If the decision is yes, the frame bit is transferred directly to the B bit location as well as to a temporary C bit location. This is followed by an exit from the interrupt routine via the point labeled $E_{\emptyset}$ in Figure 7a. Any exit via $E_{\emptyset}$ will differentially encode the bits C and A and transfer the result to A followed by a return interrupt (RI) command. If the frame bit is not to be transmitted, a decision is made as to whether a forward bit is to be transmitted (Figure 7a). If the decision is yes, another decision is made as to whether this is the 200 b/s mode or 10 kb/s mode. For the case of the 200 b/s mode, the program differentially encodes the previous transmitted bit of the forward link and transfers the result to the PSK modulator. It also transfers the forward bit directly to the I/O device for digital

output and executes a return interrupt. For the case of the 10 kb/s mode, the forward bit is transferred to the B and C bit locations followed by an exit via $E_{\emptyset}$. If the forward bit is not to be inserted on the downlink another decision is made as to whether the slip/seq bit is to be inserted on the downlink. If the decision is yes, the proper slip/seq bit is transferred to the B and C bit locations, again followed by an exit via $E_{\emptyset}$. If the decision is negative, the program continues and determines whether the present input samples (I,Q) are the proper pair to be either DQPSK or hard decision demodulated. The results of these demodulations, which are performed on every other interrupt, are denoted by I_D and Q_D. If the decision is to demodulate, the demodulation is performed with the proper one being determined by whether the simulation is in the LRC mode or RB mode. If the decision is not to demodulate, the present value of Q_D is transferred to I_D and the program is forced to the location shown in Figure 7b. At this point, the present value of I_D is transferred to bit locations B and C followed by an exit via $E_{\emptyset}$.

There were two DQPSK demodulation algorithms programmed for utilization with interrupt #1. The first is the standard decision-making algorithm to determine the most likely phase shift (i.e., 0, 90°, 180°, or -90°) which had occurred between successive transmissions. The second is a software simulation of the particular DQPSK algorithm employed by the LES 8 and 9 satellites. The experimental baseline results of these demodulators are described in

Section VI. The hard decision demodulator is a simple decision-making algorithm which outputs a logical one for a positive sample and zero for a negative sample.

Not shown in the flow diagram of interrupt #1 is a software implementation of a one-millisecond delay of the K band downlink data output both for the PSK output as well as the data bit and clock output. This delay was implemented via straightforward load and store commands using the appropriate number of dummy variables. The reason for this delay is to simulate the one millisecond input delay of the received signal in the LRC and Forward mode. This delay is due almost entirely to the crystal filter/limiter combination inherent in the actual LES 8 and 9 satellites. Since the front end of the PDT has no such delay, it was simulated by delaying the total output data bit stream.

The functional flow diagram for interrupt program #2 is shown in Figure 8. The basic function of this interrupt is to store sixteen A/D samples of I,Q values obtained at a 3.2 KHz rate from receiver #2, as well as to output the dehop commands for receiver #1 and #2 on a five-millisecond or two-hundred-millisecond basis (Forward or RB mode). As shown in Figure 8, this interrupt is entered at a 3.2 KHz rate. Its first decision is to determine whether to store the present A/D samples in high buffer or low buffer memory. Once sixteen sample values are determined for either case, a basic five-millisecond flag and frame synch flag are set to identify that a five-millisecond

interval has passed. These flags are used by the main program and interrupt #1 program respectively as appropriate indexes. Once these flags are set, the receive dehop commands previously calculated in the main program are transferred to the receive synthesizers. These commands are executed every five milliseconds for the Forward and LRC modes and every two-hundred milliseconds for the RB mode.

Interrupt program #3, the simplest of the interrupts, is depicted in Figure 9. Its only purpose is to generate the clock bits corresponding to the 10 KHz data bits stream generated in interrupt #1. Upon entering this interrupt, a command is issued to reset the value of the clock output to its low state. The high position of the clock state is reverted to on entering interrupt #1. Since this interrupt occurs midway through a present bit level position, there occurs a high-to-low transition in the middle of the data bit. For the utilization of this output bit stream with the K band modem/processor, however, a specialized interface was constructed to transfer the PDT output bit stream and clock to a line-driver, twisted-shield pair combination containing high and low data and clock lines.

A functional flow diagram of the main program is depicted in Figures 10a, 10b and 10c. It is initially entered via the exit from the start-up procedure. The main responsibility of this program is to demodulate the sixteen FSK samples generated in interrupt #2, format the proper demodulated forward bits and downlink slip/sequence

bits at the proper intervals, block-encode the Forward bits for downlink UHF transmission, increment the real time clock from its initial epoch in increments of two and three milliseconds, and last, but most time-consuming, to determine the proper frequency commands for the K band uplink frequency dehop and UHF uplink and downlink frequency hops. All the above must be implemented on a five-millisecond basis.

As depicted in Figure 10, the initial decision made on entering the main processing program is to determine whether the five-millisecond flag is set. If it is not set, the program goes into a wait loop. Once the five-millisecond flag is set, however, the program continues with an initial reset of the five-millisecond flag and determines whether the real time program clock is on a second mark. If it is, a one-second tick is routed to the external display clock. If not, the program determines whether the next five-millisecond interval will be a multiple of two-hundred milliseconds. If so, an appropriate index is set for use in interrupt #2. This is followed by a determination as to whether or not a proper slip/sequence bit should be inserted on the next five-millisecond interval. Subsequently, a chip demodulation of the sixteen FSK-stored samples is performed. If this chip demodulation is the last of four chips, the program continues to a complete demodulation of the four chips to determine the three-bit forward data. If the present chip demodulator corresponds to the third of four chips, the previous

stored forward bits are block-encoded for the UHF downlink data and formatted with the proper parity bit for insertion into the K band downlink data bit stream. If the chip demodulation corresponds to either the first or second chip, the program continues, as shown in Figure 10, to increment the present time epoch by two milliseconds. After this time increment, a decision is made as to whether the satellite is in the RB mode. If this decision is affirmative, the UHF uplink word of day is used, with the present time epoch, to determine the LES 8 and 9 UHF uplink frequency command. If the report back mode is not in effect, the K band uplink word of day is used and the LES 8 and 9 K band uplink frequency command algorithm is executed. This is followed by a transformation of the frequency commands to the format required by the PDT's receive synthesizers. Once the uplink dehop commands are determined, the program increments the present time epoch by three milliseconds and, in conjunction with this incremented time and the UHF downlink word of day, determines the LES 8 and 9 UHF downlink frequency hop command. The program then proceeds to add the FSK block-encoded forward bit data to the UHF downlink frequency commands and performs a transformation of these commands to a set of digital commands compatible with the PDT's transmit frequency synthesizer. The program then jumps to the wait location and repeats the main program on a five-millisecond basis.

SECTION IV

THE OPERATIONAL PROGRAM FOR THE 100 kb/s REPORT BACK MODE

The high sample rate dictated by the 100 kb/s mode (ten microseconds between interrupts) required special consideration from both the hardware and software aspects. From the hardware standpoint, a hardwired modification on the A/D converters and interrupt circuitry was mandatory since, in their normal mode of operation, these converters cannot sample at such a rate. Essentially, this modification permits the A/D converter to be reset and interrupts enabled after only the sign bit has been determined from the sample (i.e., not the normal 12-bit fill-up). Since, in the report back mode, a hard decision is all that is required, this hardware modification will suffice. This is not the case for the 100 kb/s uplink DQPSK mode, however. From the software point of view, various constraints had to be imposed due to the speed at which the calculations are required. First, only a zero word of day is allowed in the hop mode. This constraint considerably speeds up the required frequency algorithm. Second, interrupts #2 and #3 are not used; hence, all real time calculations are performed in one interrupt, namely, the high priority interrupt. Third, there cannot be a 100 KHz digital data output simultaneously with a 100 kb/s DPSK output.

Except for the above constraints, the overall structure of the high rate report back mode program is generally the same as that of

the low rate program described in the previous section. The start-up procedure is identically the same. The main differences are in the main and interrupt #1 program structure. The high rate report back functional flow diagram for interrupt #1 is shown in Figures 11a and 11b. It is entered at a 100 KHz rate with a sign determination of the I and Q samples and immediately transfers an A bit to the PSK modulator. As with the low rate mode, this initial transfer is a dummy bit used for phase references. This is followed by a decision as to whether or not to overwrite the frame, forward/parity and slip/sequence bits onto the downlink bit stream. If the decision is affirmative, the overwrite proceeds, as depicted by the instructions shown in Figure 11a, and an exit via E_1 is performed. If the overwrite is not to be performed, a decision is made as to whether the present I,Q samples are the proper ones for demodulation. If it is a proper pair, the I sample sign is determined and appropriately differentially encoded with the present A bit, the result being transfer back to the A bit. This is followed by a determination of the Q input sign with the result being inserted into a temporary B bit. An exit is then made via E_1. If it is not a proper pair, the B bit is appropriately differentially encoded with the present A bit and transferred to the B bit, followed by an exit E_1.

In the exit E_1 routine, an initial decision is made as to whether a five-hundred-microsecond subframe has passed. If the decision is negative, a return interrupt (RI) is executed. If the decision is

affirmative, the overwrite counter and five-hundred-microsecond subframe counter are reinitialized. This is followed by a determination as to whether or not a five-millisecond frame has been achieved. If the decision is negative, a return interrupt is executed. If affirmative, a five-millisecond flag is set (for use in the main program), the five-millisecond frame counter is reinitialized and the frequency commands for the UHF downlink are executed. After this execution, a decision is made as to whether the five-millisecond counter is a multiple of two-hundred milliseconds. If the decision is negative, a return interrupt is performed. If affirmative, the frequency synthesizer commands to the UHF uplink receiver are executed, followed by a return interrupt.

The main program for the 100 KHz mode has such minor changes from the main program of the low rate mode that its flow diagram will not be repeated. In fact, the main program at the high rate is identical to the main program for the low rate modes shown in Figures 10a, 10b and 10c, with the exception of the FSK chip and final demodulations. For the high-rate mode, these subroutines are bypassed with dummy-demodulated bits being inserted as the final demodulation outputs. These dummy bits were inserted to allow the UHF terminal to achieve and maintain synchronization on the UHF downlink even in the high rate report back mode, and also to enable the K band modem/processor to legitimately obtain block synch as well as frame and one-sec epoch synchronization.

SECTION V

THE RF SATELLITE SIMULATOR AND TEST SETUP

In order to interface with the actual K band and UHF terminals, the simulator's transmit IF output must be linearly translated to the appropriate downlink frequencies, and the K band and UHF terminals' uplink frequencies must be linearly translated to the proper IF frequency. To implement this, the Signal and Interference Generator (SIG), housed in the CSEL, was utilized. The appropriate system setup is shown in Figure 12. Not shown in Figure 12 are the necessary attenuators and amplifiers required at selected points for the proper adjustment of power levels. As shown in Figure 12, the IF output of the PDT corresponding to transmitter #1, which is the K band downlink signal structure, is interfaced to the SIG via the 700 MHz input to access #1, which in turn linearly frequency translates the 700 MHz input to either the LES 8 or 9 K band downlink frequency. The IF output of the PDT generated by transmitter #2, which is the simulated satellite's UHF downlink, is routed to access #2 of the SIG where it is linearly downconverted to the proper UHF downlink frequency spectrum. This UHF output signal is then routed to the UHF TX/RX box shown in Figure 12. This box enables the satellite to operate full duplex in the UHF mode with the UHF downlink transmitter signal always being radiated. The UHF received signal is, in turn, linearly upconverted to the appropriate 700 MHz IF and routed to the switch

shown in Figure 12. For the UHF report back mode, the switch is always in the up position (RB). For the low rate conferencing and/or forward link mode, the switch is always in the lower position (LRC/FOR). The output of this switch is then appropriately routed to receivers #1 and #2 of the Programmable Data Terminal. The input to the LRC/FOR switch position is the K band uplink signal after an appropriate conversion from the K band uplink frequency to the 700 MHz IF frequency.

The test setup employed for utilization of the satellite simulator is shown in Figure 13. Here, the appropriate inputs and outputs of the satellite simulator are shown routed to their respective terminals or antennas depending on the location of the K band and UHF terminals being utilized in the tests. For the case where the K band and UHF terminals and modems located in the rooftop facility (directly above the CSEL) are being used, the respective inputs and outputs are routed directly to these terminals. For the case where the K band and UHF terminal and modems housed in the C135 test aircraft are utilized, the satellite input and outputs are routed to their respective antennas, shown in Figure 13.

SECTION VI

DEMODULATOR SELF-TEST AND IF BASELINE RESULTS

There were two basic test subroutines written to explicitly determine the validity and baseline performance of the FSK and DQPSK demodulators that were implemented via software and used in the satellite simulator. These test subroutines were structured in such a manner as to minimize changes in the operational program. To this end, appropriate breaks in the system structure of Figure 3 were implemented as branch points determined by the setting of a manual switch register bit on the front panel of the PSP. The baseline performance of the DQPSK demodulators were examined by breaking the flow of the system shown in Figure 3 immediately after the DQPSK demodulator, and routing this output to the self-test DQPSK subroutine. The system block diagram of this implementation is shown in Figure 14. As depicted in Figure 14, the DQPSK self-test subroutine essentially replaces the K band downlink formatting and differential encoding with a random bit stream generator, a DQPSK encoder and error detector. Except for this modification, the remainder of Figure 3 is not changed. In the DQPSK self-test mode, therefore, transmitter #1, which operationally has the K band downlink signal structure, is replaced by the K band LRC uplink signal structure. This 700 MHz output is then routed to a special test box where it is linearly combined with a wideband 700 MHz noise source possessing a known

flat spectral density over the bandwidth of the transmitted signal. The combined output is subsequently routed to receiver #1, which is the normal receiver for the reception of the K band uplink LRC signal.

In order to more easily obtain error printouts (the PSP as configured in the PDT has no printout capability), the error detector output is routed over to the PDP 11/20 via the PDT-PDP 11/20 interface. This interface, in effect, provides the PDT with all the input/output devices on line to the PDP 11/20.

A similar technique was also used to obtain the 8ary FSK baseline results. For this case, the output of the FSK demodulator, depicted in Figure 3, was routed to an 8ary FSK self-test subroutine. The block diagram of this test mode is given in Figure 15. As shown in Figure 15, this test subroutine consists of a random bit stream generator, an 8ary FSK uplink formatter, which essentially divides the bit stream into groups of three bits each and offsets the transmit frequency synthesizer accordingly, and an error detector. The forward uplink signal structure is then generated by using transmitter #1. The output of transmitter #1 is, as in the DQPSK test, routed to the special test box and combined with a 700 MHz noise source. The combined output is subsequently routed to receiver #2, which is the normal receiver for the reception of K band uplink forward messages.

The results of the baseline tests performed under a no-hop condition are depicted in Figures 16 and 17. Figure 16 shows the results

of a probability of error vs. bit energy to noise density ratio test for both of the DQPSK demodulators considered. The results verify that the DQPSK software routines are demodulating in a reasonable manner. They also indicate that the LES 8 and 9 demodulation follows the standard algorithm up until about a $5x10^{-2}$ error rate. At this point a tapering off of the LES 8 and 9 algorithm seems to be indicated.

Figure 17 shows the results of this same type of curve for the 8ary FSK demodulator. Again the results verify that the software routine is demodulating in a reasonable manner.

SECTION VII

OTHER SELF-TEST MODES AND OPERATIONAL CONSIDERATIONS

The satellite simulator program has various modes which can be exercised by setting the appropriate bit positions on the manual switch register (MSR) of the Programmable Data Terminal. Some of these bit settings (15 and 12) are only for self-test purposes and cannot be used during an operational test since satellite timing would be destroyed. Some are for purely operational modes (3, 4, 5, 6, 7 and 8) and some can be used during operational tests (0, 1, 2, 10, 11, 13 and 14) since they do not destroy satellite timing, but are not truly operational modes of the satellite. The particular function of each bit setting will now be described.

Bit 15. Bit 15 controls the 8ary FSK self-test mode described in the previous section. If bit 15 is set, the program structure is altered from that of Figure 3 to that depicted in Figure 15. The only difference is that the random bit stream generator of Figure 15 is replaced by a repetitive three-bit pattern determined by the setting of bits 2, 1 and Ø on the MSR. Initially, this test mode was used to verify the FSK demodulator. However, once the software is verified, this mode can be used to check the operational status of transmitter #1 and receiver #2. If the only bit that is set is bit 15, then the output of transmitter #1 is the actual hopped K band forward uplink signal structure. When this transmitter output is in turn routed to

receiver #2 and the 2 MHz test point (as well as the I,Q channels of receiver #2) is observed, the proper operation of transmitter #1 and receiver #2 can be verified. If bit 14, as well as bit 15, is set, then transmitter #1 and receiver #2 are constrained to a no-hop mode with the frequency determined by thumb wheel input commands. The particular function of bit 14 is elaborated upon below.

Bit 14. Bit 14 has two roles: one in conjunction with the DQPSK and FSK demodulator self-test modes, and the other in the operational mode. In the FSK demodulator self-test mode (bit 15 set), the setting of bit 14 constrains the output of transmitter #1 and the dehop frequency of receiver #2 to a fixed frequency determined by a twenty-bit input command via front panel thumb wheel switches. The relationship between the twenty-bit input command and the output frequency is the same as that of the twenty-bit command of the slow-live register of the K band modem/processor to the 700 MHz output of the K band modem/processor. The particular entry of these twenty bits are via the thumb wheel switches labeled DISPLAY and RX on the front panel of the PDT, as shown in Figure 18.

If bit 14 is set during an operational mode, receivers #1 and #2 are then tuned to fixed frequencies w :h the frequency of receiver #1 being determined as in the above self-test mode, as illustrated via Figure 18. Receiver #2 is always tuned 100 KHz below that of receiver #1. In addition, the UHF downlink is also constrained to a fixed frequency, with the value of frequency being determined by

the twenty-bit command word entered via the thumb wheel switches of the TX/MODE switch, as shown in Figure 19. The relationship between the UHF downlink frequency and the twenty-bit command is the same as that of the twenty-bit slow-live register contents of the satellite and the UHF downlink frequency. The primary utilization of bit 14 in the operational mode is for close loop tests of the LRC and Forward Monitor modes in a no-hop condition, as well as for diagnostic purposes, utilizing a fixed UHF downlink frequency.

Bit 13. Bit 13, if set, exercises a self-test mode which forces the output of the FSK and DQPSK demodulators to be a fixed repetitive pattern. Satellite time is not destroyed. For the case of the FSK demodulator, the output is constrained to be one of the eight three-bit patterns determined by the settings of the MSR bits 2, 1 and Ø. For the case of the DQPSK demodulator, the output is constrained to be a repetitive sequence of either 00, 01, 10 or 11. The particular sequence is determined by the MSR bits 11 and 10. The remaining portion of the program structure is identical to Figure 3. The primary function of this mode is for diagnostic purposes using a fixed downlink data stream for both the K band downlink and the UHF downlink.

Bit 12. Bit 12 controls the DQPSK self-test mode described in Section VI. If bit 12 is set, the program structure is altered from that of Figure 3 to that of Figure 14. However, there is a slight difference here in the fact that with bit 12 set, the random bit stream generator of Figure 14 is replaced by a fixed pattern of

either 00, 01, 10 or 11. The particular sequence is again determined by the setting of the MSR bits 11 and 10. Aside from the verification of the DQPSK demodulator, this mode can be used to verify the operational status of transmitter #1 and receiver #1 which is the normal receiver for the DQPSK uplink.

As with the FSK test, bit 14 can also be used with bit 12, the DQPSK test. With only bit 12 set, the output of transmitter #1 is the actual hop DQPSK uplink signal structure. With bit 14 also set, transmitter #1 is constrained to a no-hop mode as discussed under the FSK test.

Bits 11 and 10. Bits 11 and 10 are used only in their described manner associated with bits 12 and 13.

Bit 9. Bit 9 is not used.

Bit 8. Bit 8 refers to the option of selecting either one of the two DQPSK algorithms mentioned in Section III. In the up or reset position, the program chooses the LES 8 and 9 simulated demodulation algorithm, in the set or down position, the program uses the more conventional demodulation algorithm.

Bit 7. Bit 7 refers to the report back mode. When, in a normal operating configuration, a request is given for the satellite to go into the low rate (10 KHz) report back mode, bit 7 must be set (for all other modes it is in the reset position).

Bit 6. Bit 6 refers to the high rate (100 KHz) report back mode. For this request, both MSR bits 7 and 6 must be set.

Bit 5. Bit 5 refers to the doppler mode of operation. When bit 5 is set, manual, fixed-frequency offset commands may be inserted via the front panel thumb wheel switch to both of the receivers and transmitters. The particular insertion of these bits is clarified with the aid of Figure 20. The sixteen bits entered via the RX thumb wheel switch of Figure 20 refers to the frequency offset added or subtracted to receivers #1 and #2 (i.e., the K band uplink receiver). The 15th bit of this command is the sign bit, with bits 14 (MSB) through 0 (LSB) representing the absolute value of the frequency offset command. The sixteen bits entered into the TX thumb wheel switch are divided as follows: bits 13 (MSB) through 0 (LSB) represent the absolute value of the K band downlink frequency offset with bit 15 representing the sign bit. Bit 14 is reserved for the sign bit of the UHF transmit frequency offset with the absolute value of the UHF frequency offset being determined by the eight bits in the MODE and DISPLAY registers. Bit 3 of MODE is the MSB, and bit 0 of DISPLAY is the LSB. In all cases the LSB of the absolute value of the frequency offset represents 6 1/4 Hz. Since mode 14 and 5 use the same input thumb wheel switches, under no circumstances should bits 5 and 14 be used simultaneously.

Bit 4. Bit 4 is a fixed UHF uplink mode. The setting of this bit constrains the satellite's UHF uplink receiver to be tuned to a fixed frequency of 343 MHz.

Bit 3. The setting of bit 3 transfers the satellite to the 200 b/s downlink mode.

Bits 2, 1 and Ø. Bits 2, 1 and Ø are used only in their described functions associated with bits 15 and 13.

The following may be considered to be a list of initial operational procedures to be followed on initially setting up the satellite simulator:

1) Configure the Programmable Data Terminal and auxiliary subsystems as depicted in Figures 1 and 2.

2) Interface the Programmable Data Terminal with the Signal and Interference Generator as depicted in Figure 12.

3) Load the satellite simulator program into the PSP.

4) Enter the desired start time into the TX/MODE/DISPLAY thumb wheel switches as shown in Figure 21.

5) Set all manual switch register positions to reset.

6) Enable the RUN switch on the PSP.

7) On the desired start time minus one second (obtained by observations of the WWV receiver clock or Rubidium clock), enable the start switch.

The system is now in the configuration where any of the manual switch register modes may be executed. If only self-test modes are being considered, the time synchronization, step 7, may be excluded.

SECTION VIII

RELATIVE LINEAR MOTION SIMULATION

In order to further elaborate on the relative linear motion mode of simulation, briefly mentioned in Section II, it is instructive to consider what happens when the simulator's basic source f_o (f_o = 12 MHz) is offset by the amount ef_o, where $e = (df)/f_o$ and (df) is the incremental offset, in Hz, from the basic source frequency. When this offset is inserted, there are two basic changes which take place: first, the real time scale of the satellite simulator is offset from its nominal value by the amount et, where t denotes the nominal time scale (e = 0), and second, all transmit and receive tuning frequencies are offset by the amount ef_r and ef_R respectively, where f_T and f_R denote the general nominal values of these frequencies (e = 0).

Consider now what takes place if one tries to establish a close loop mode (i.e., say LRC mode) between the satellite simulator and K band modem and terminal. For this case, the downlink transmitted frequency of the simulator will be $f_d + ef_d$, where f_d denotes the nominal downlink transmitted frequency, and the keying epochs of the DPSK downlink demodulator will be offset by et. The K band terminal will receive this downlink signal and, with the appropriate phase lock loops, remove the frequency offset for demodulation purposes, and the bit timing loop in the demodulator will also be

adjusted to follow the linear offset trend in the downlink DPSK keying epochs. Furthermore, the terminal will route the value of this frequency offset to the K band modem/processor where e will be determined. If e is greater than zero, the effect is to simulate the radial motion of the satellite moving toward the terminal and, if e is less than zero, away from the terminal.

After the K band modem/processor determines the algebraic value of e, two more functions are implemented. First, the uplink frequency is, via actions taken by both the terminal (center frequency correction) and modem/processor (differential doppler correction), tuned to $f_u - ef_u$, where f_u denotes the nominal uplink frequency. Second, the K band modem/processor will increment its uplink timing by the amount -et. However, since the satellite is controlled by a single frequency source, the satellite receive frequency and time scales are offset by ef_u and et respectively. Thus, the satellite receive frequency and time scales are in error from the uplink transmit frequency and time scales by the amount 2 ef_u and 2 et. Hence, as far as the simulation of the downlink relative linear motion is concerned, a simple offset of the basic source will suffice. However, for the close loop system the results are meaningless. In order to circumvent this dilemma, the satellite's downlink transmit frequency synthesizer is further offset by the amount -2 ef_d via manual frequency offset controls. This manual frequency offset changes the downlink transmit frequency only, and not basic timing. With this change the downlink

frequency becomes $f_d - ef_d$. The K band terminal receives this frequency and removes the frequency offset while adjusting its bit timing, as in the previous case. For this case, however, the physical meaning is not consistent; that is, the direction of relative motion determined from the downlink frequency offset is opposite the direction of motion inferred from bit timing corrections. Since these two functions are quite independent, and receive bit timing corrections are not used to further correct uplink timing, this physical inconsistency is of no concern. When the terminal accomplishes these functions, the K band modem/processor determines -e and the uplink frequency is adjusted, as before, with an offset opposite the sign of the doppler value. For this case, therefore, the uplink frequency is $f_u + ef_u$. Similarly, the uplink time scale is adjusted with an offset of et. However, these are now precisely the time/frequency scales at which the receiver in the satellite simulator is functioning, given an offset of the basic source of ef_o. Thus, a close loop may be established, and the evaluation of the modem/processor/terminal under relative linear motion may be accomplished.

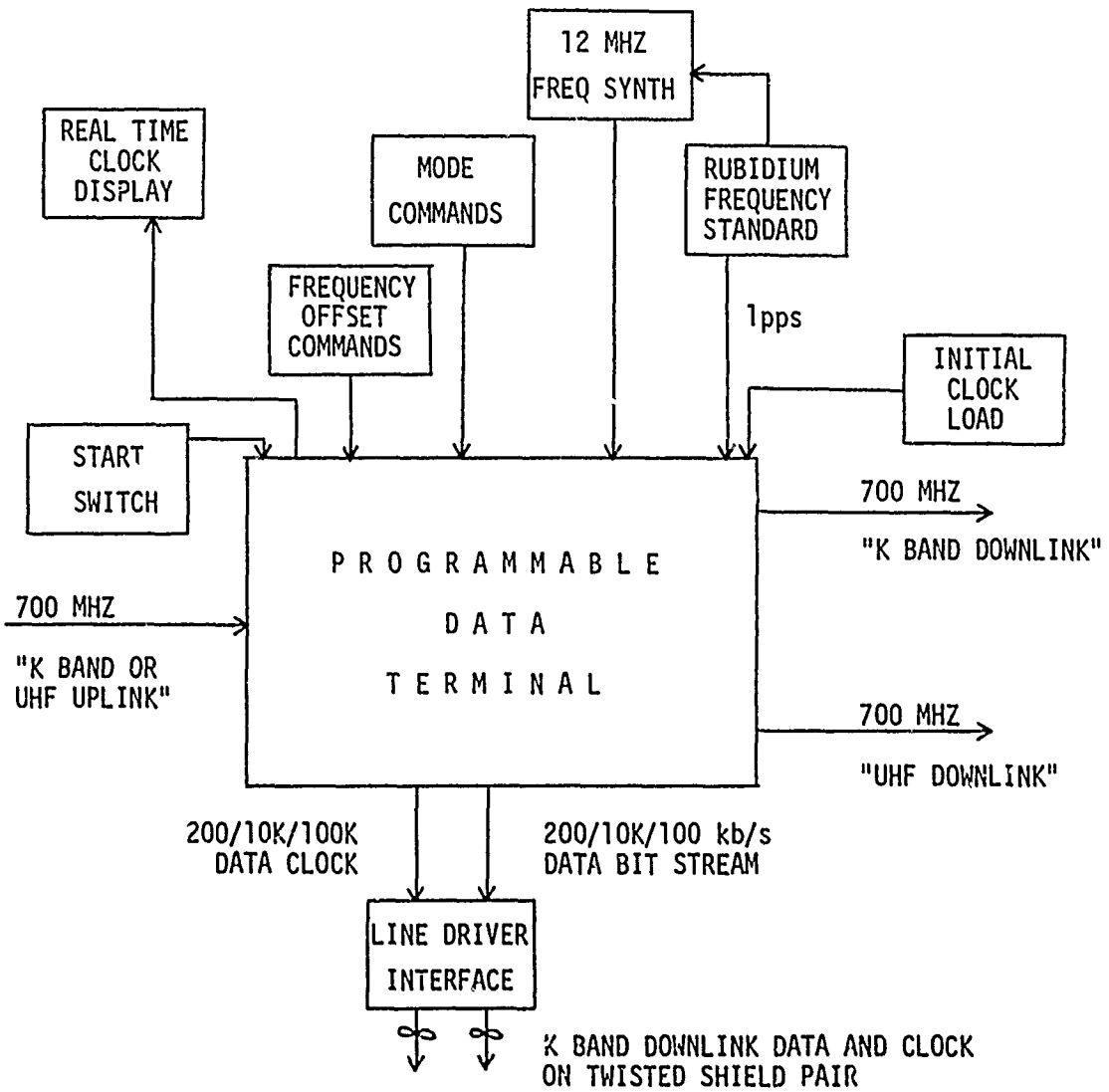

Figure 1. System Architecture of the I-F Satellite Simulator

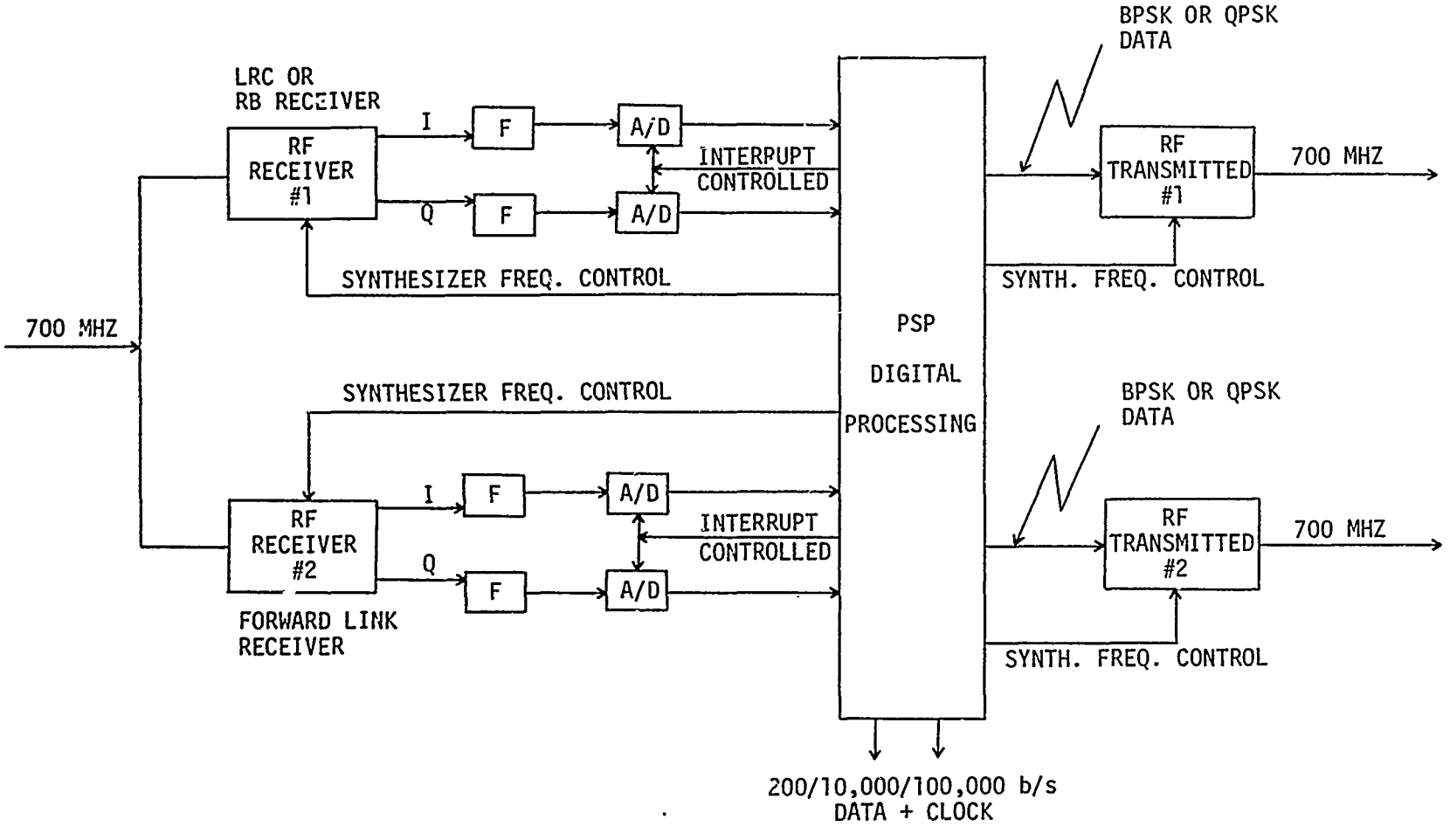

Figure 2. Partitioning of PDT into R-F and Digital Processing

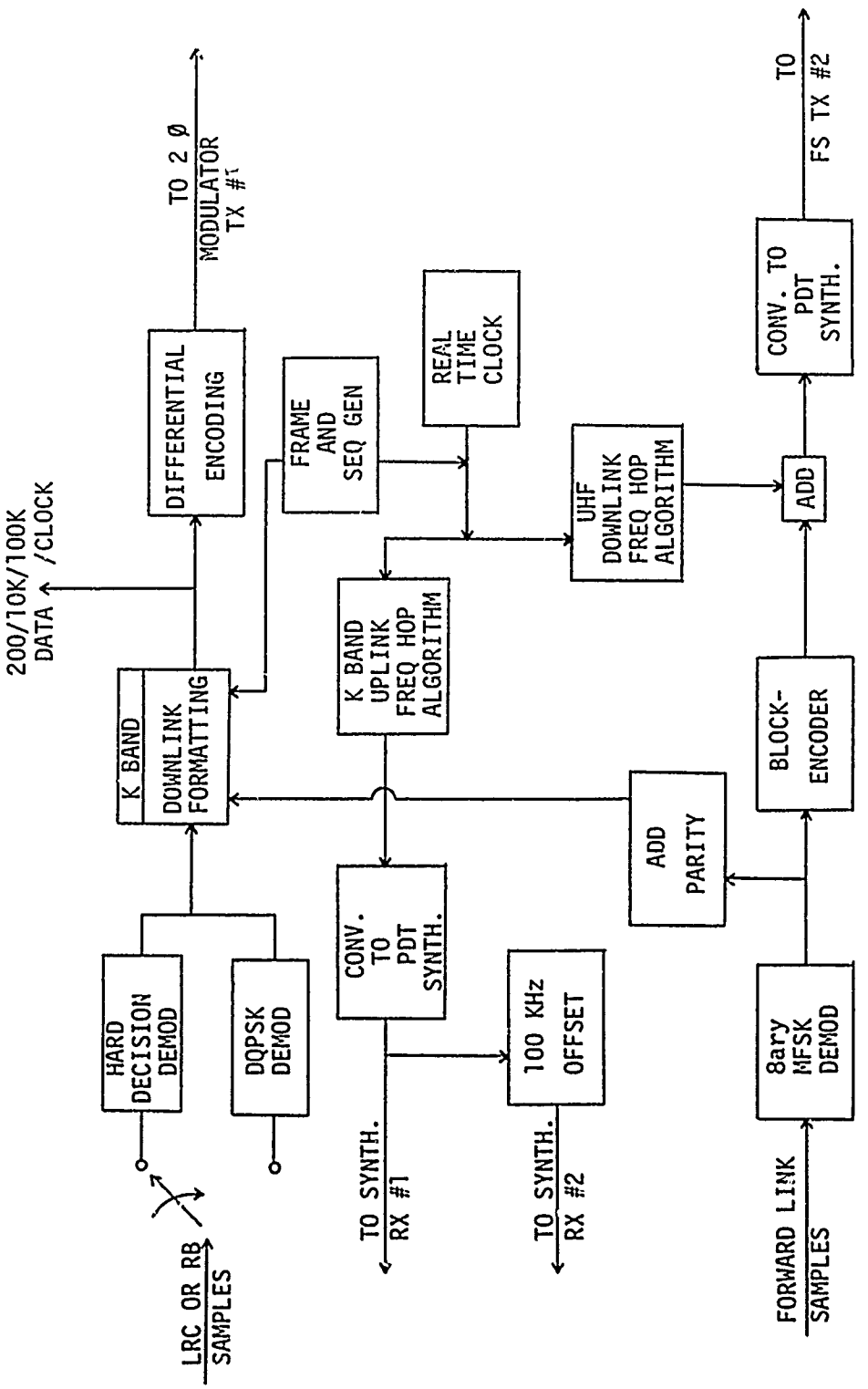

Figure 3. Functional Diagram of Digital Processing Required for the Satellite Simulator

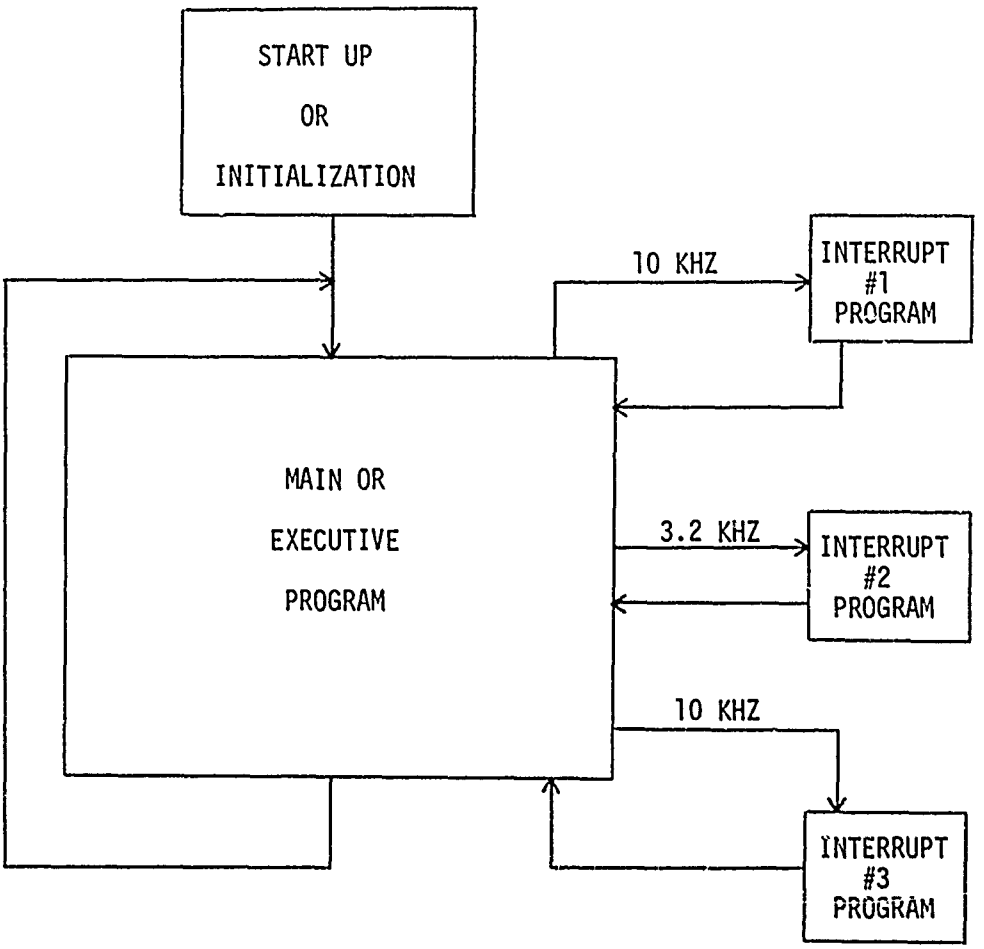

Figure 4. Overview Structure of the Satellite Simulator Program

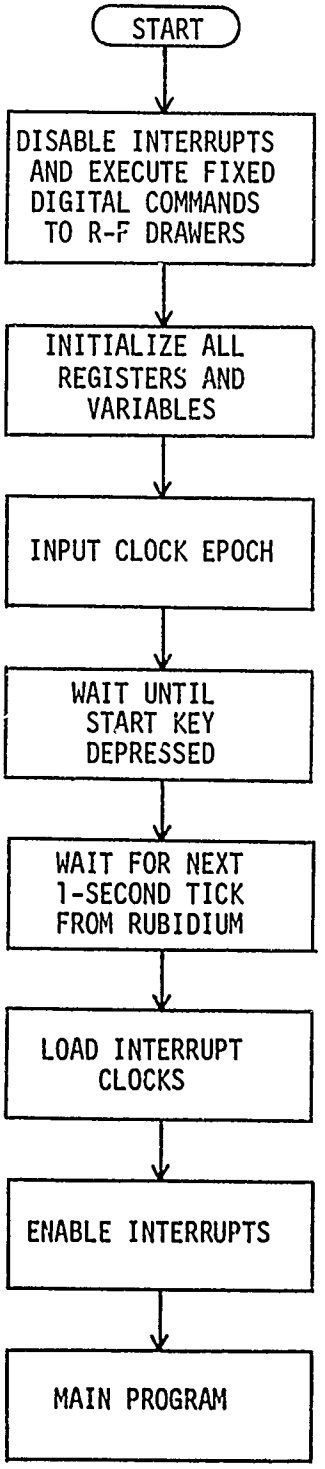

Figure 5. Functional Flow Diagram of Start-Up Procedure

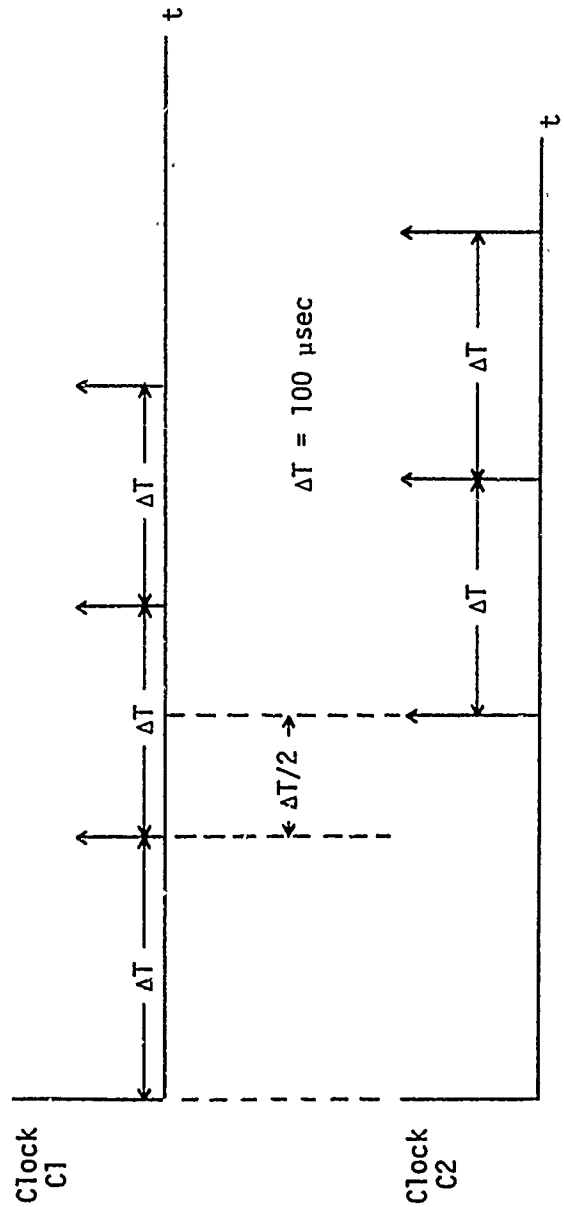

Figure 6. Clock Epochs of C1 and C2 Interrupts

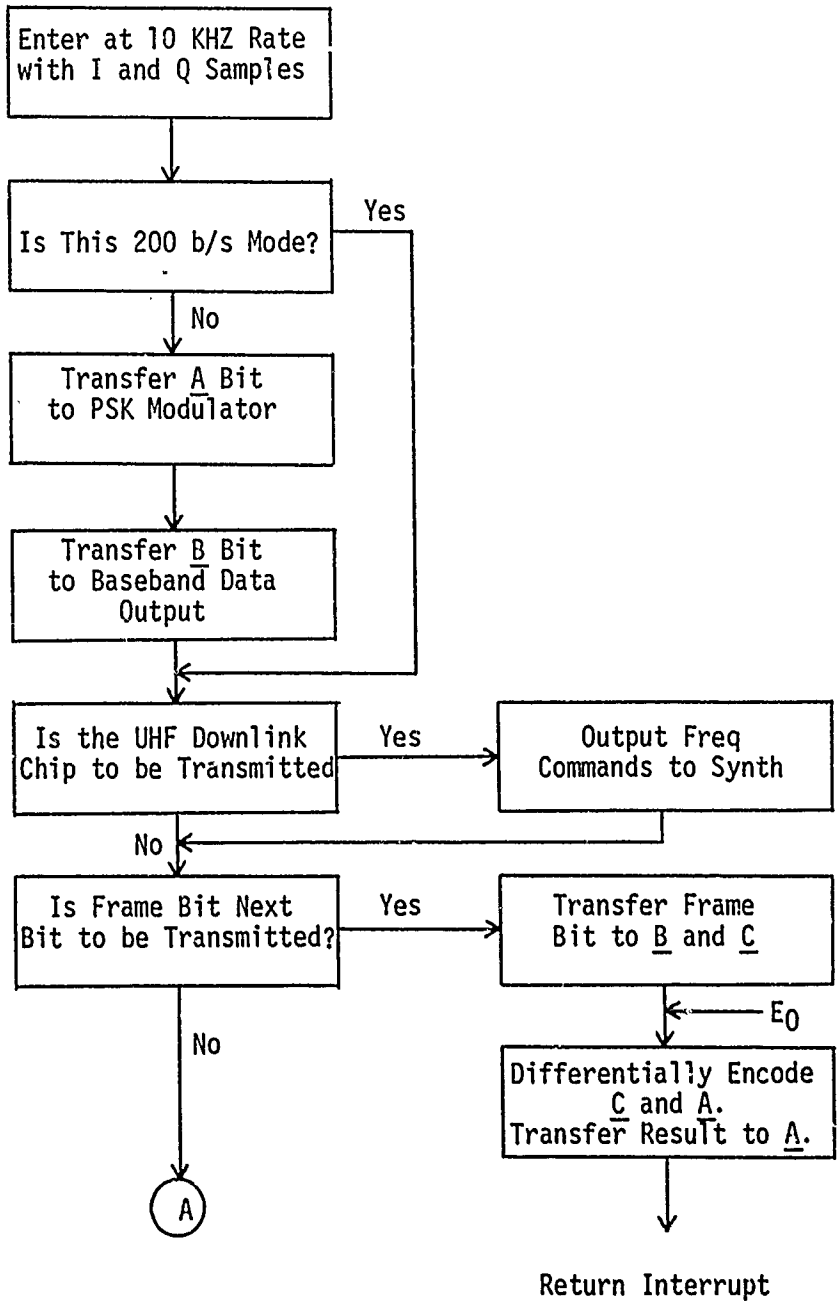

Figure 7a. Function Flow Diagram of Interrupt #1

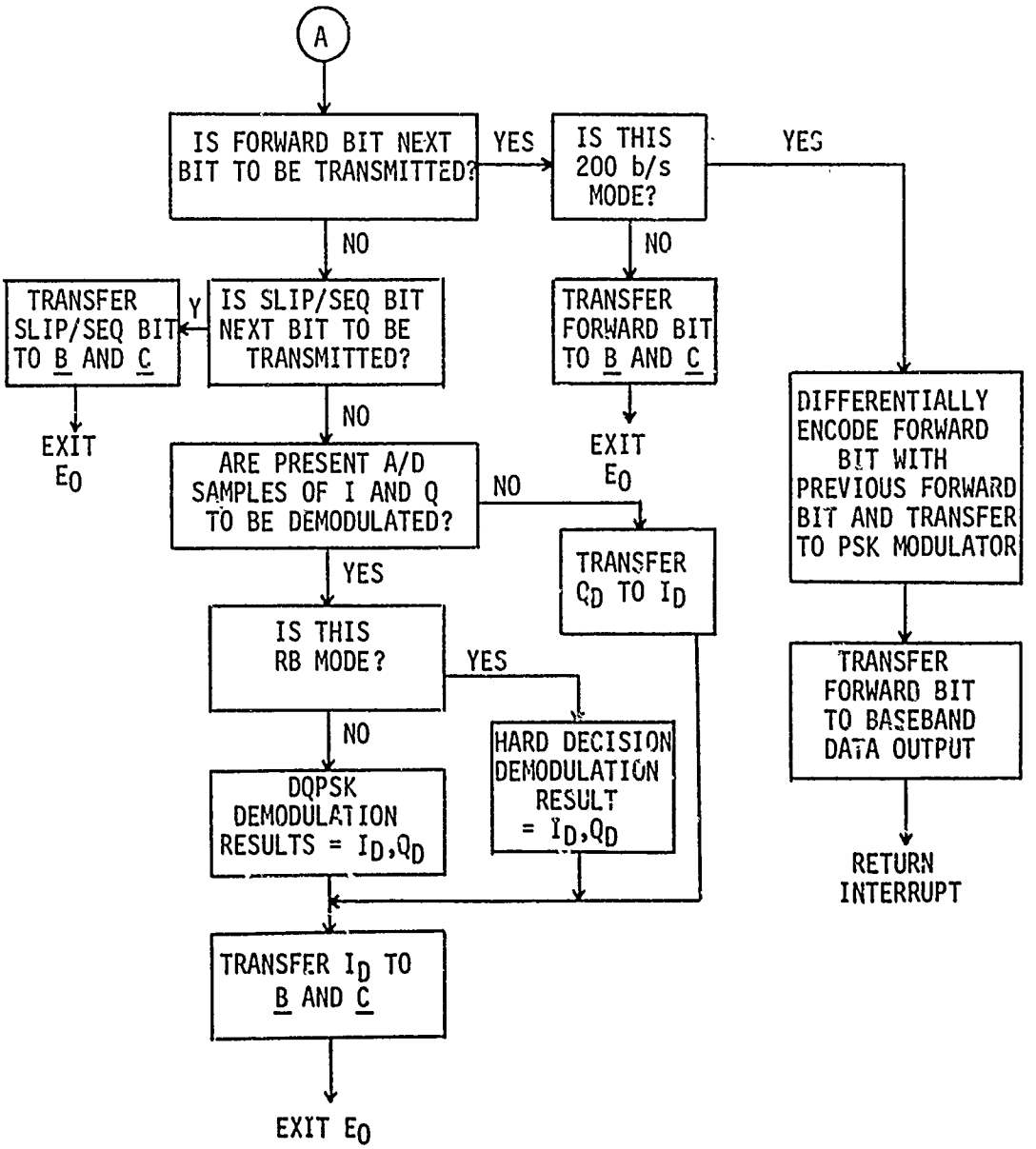

Figure 7b. Functional Flow Diagram for Interrupt #1

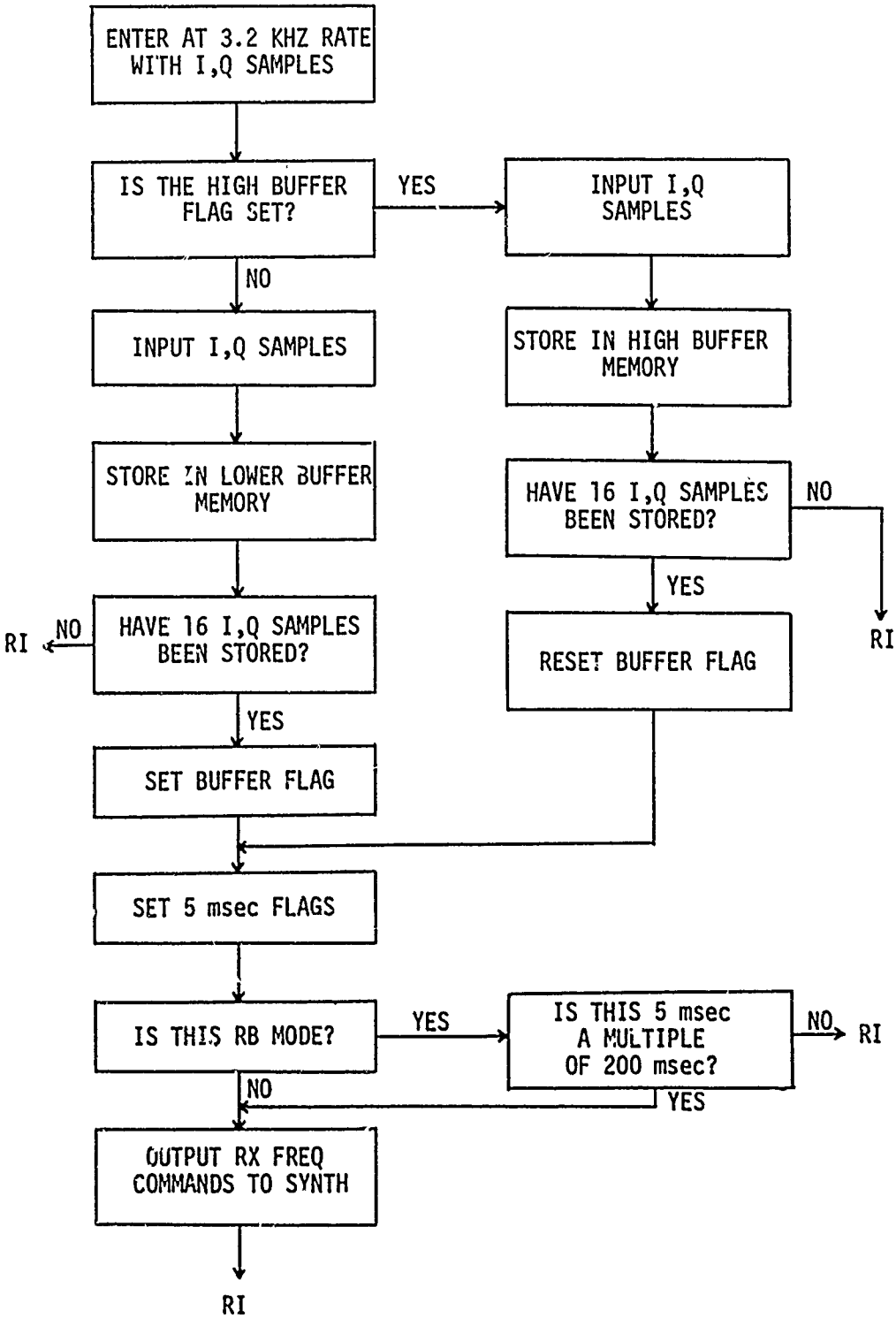

Figure 8. Functional Flow Diagram of Interrupt #2

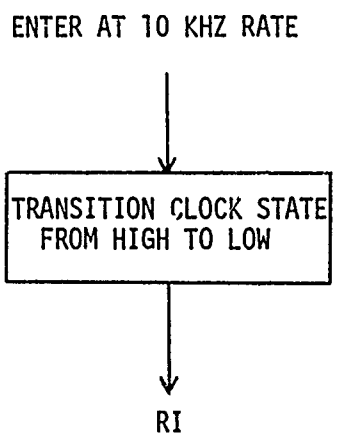

Figure 9. Functional Flow Diagram for Interrupt #3

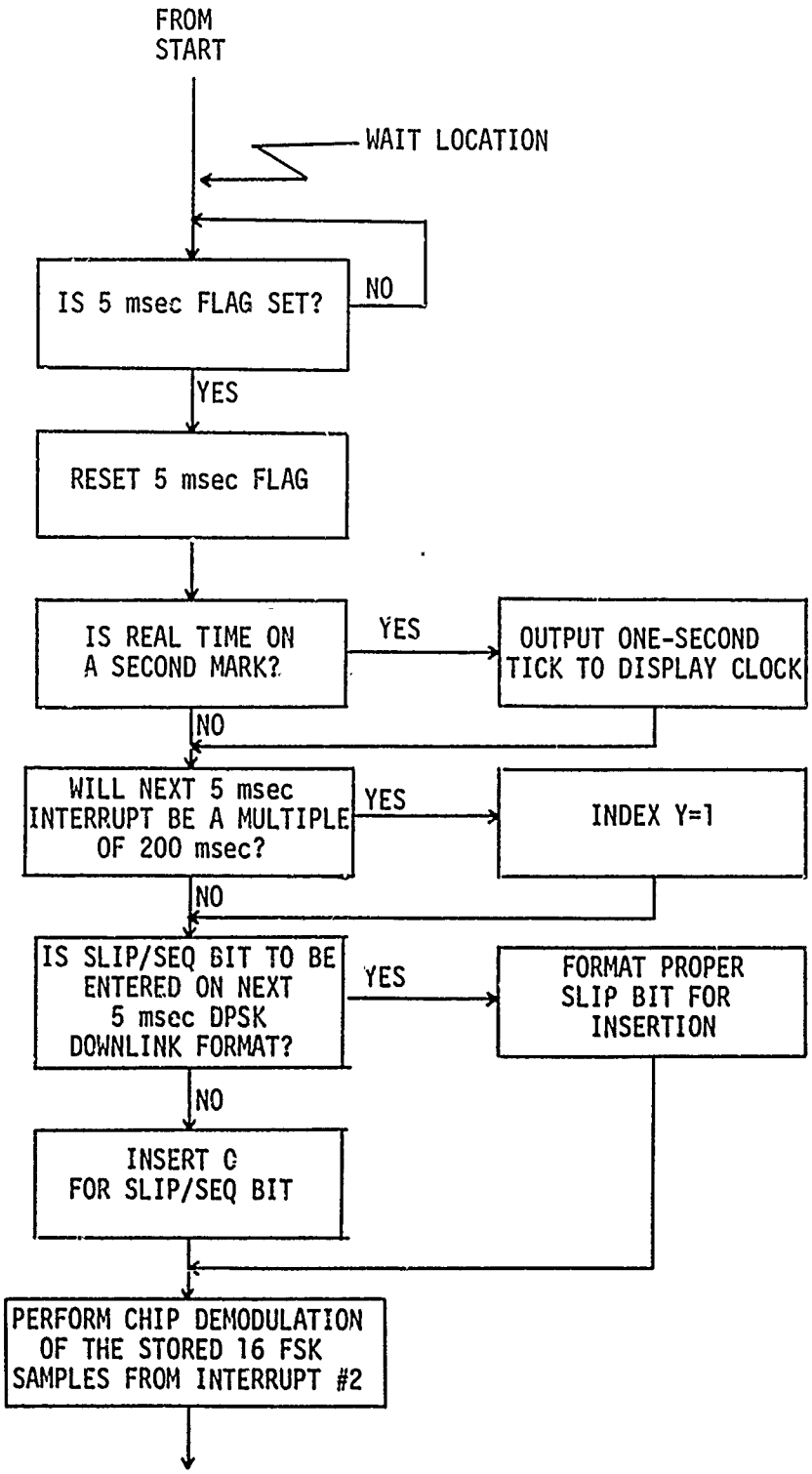

Figure 10a. Functional Flow Diagram of Main Program

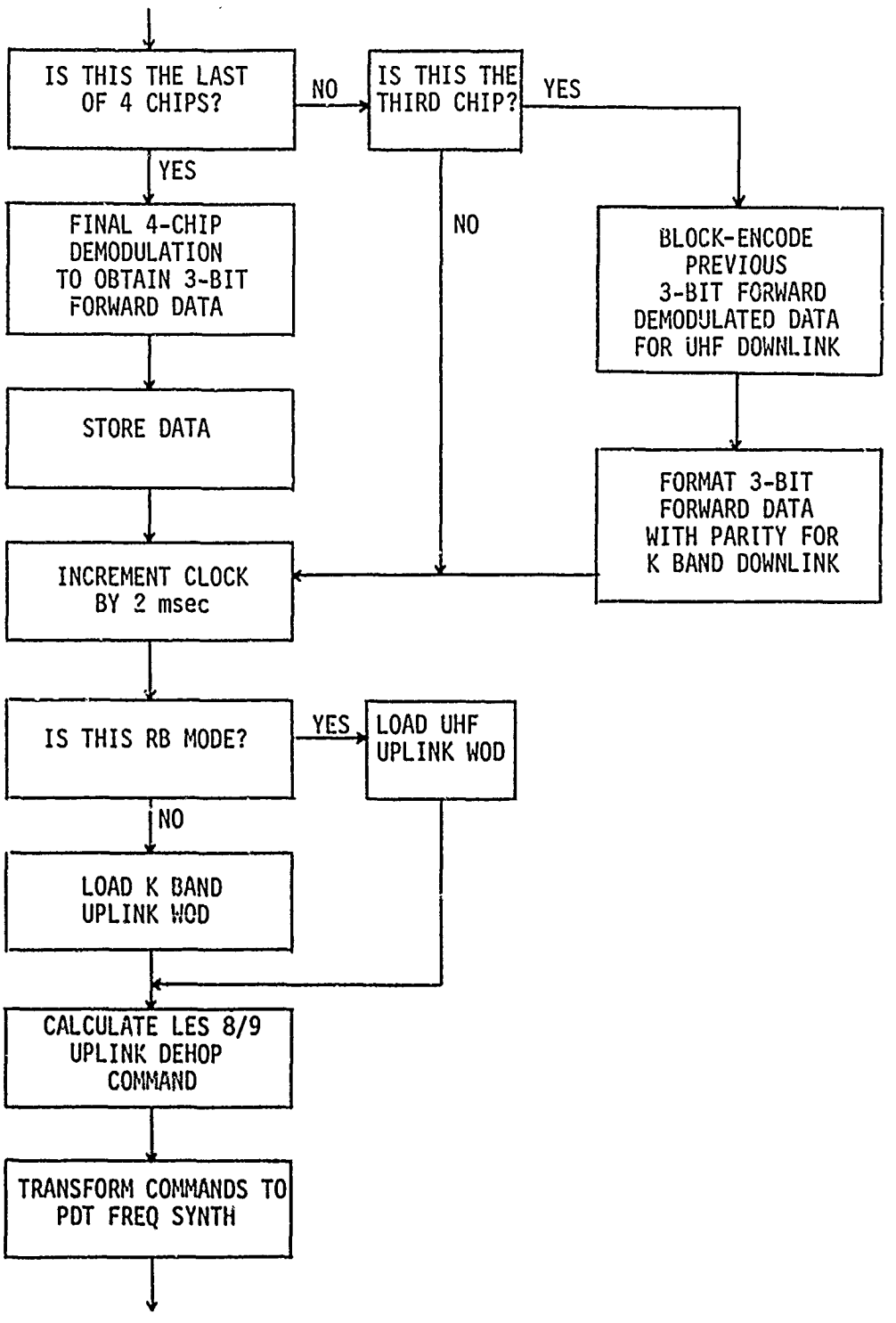

Figure 10b. Functional Flow Diagram of Main Program

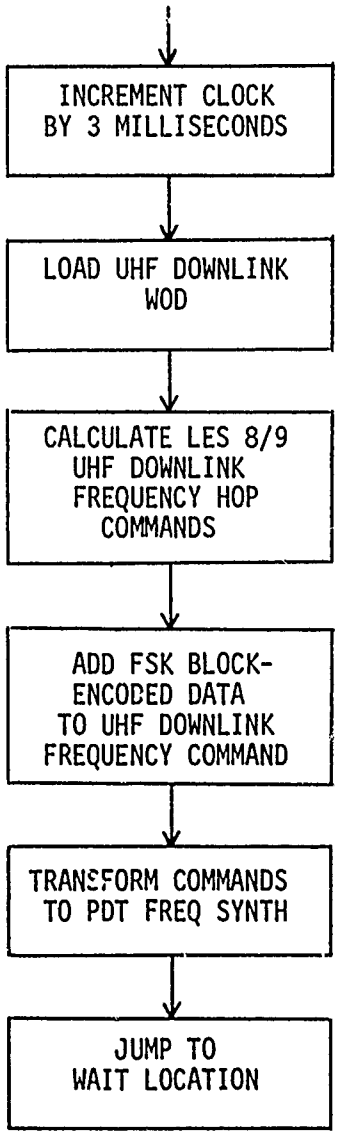

Figure 10c. Functional Flow Diagram of Main Program

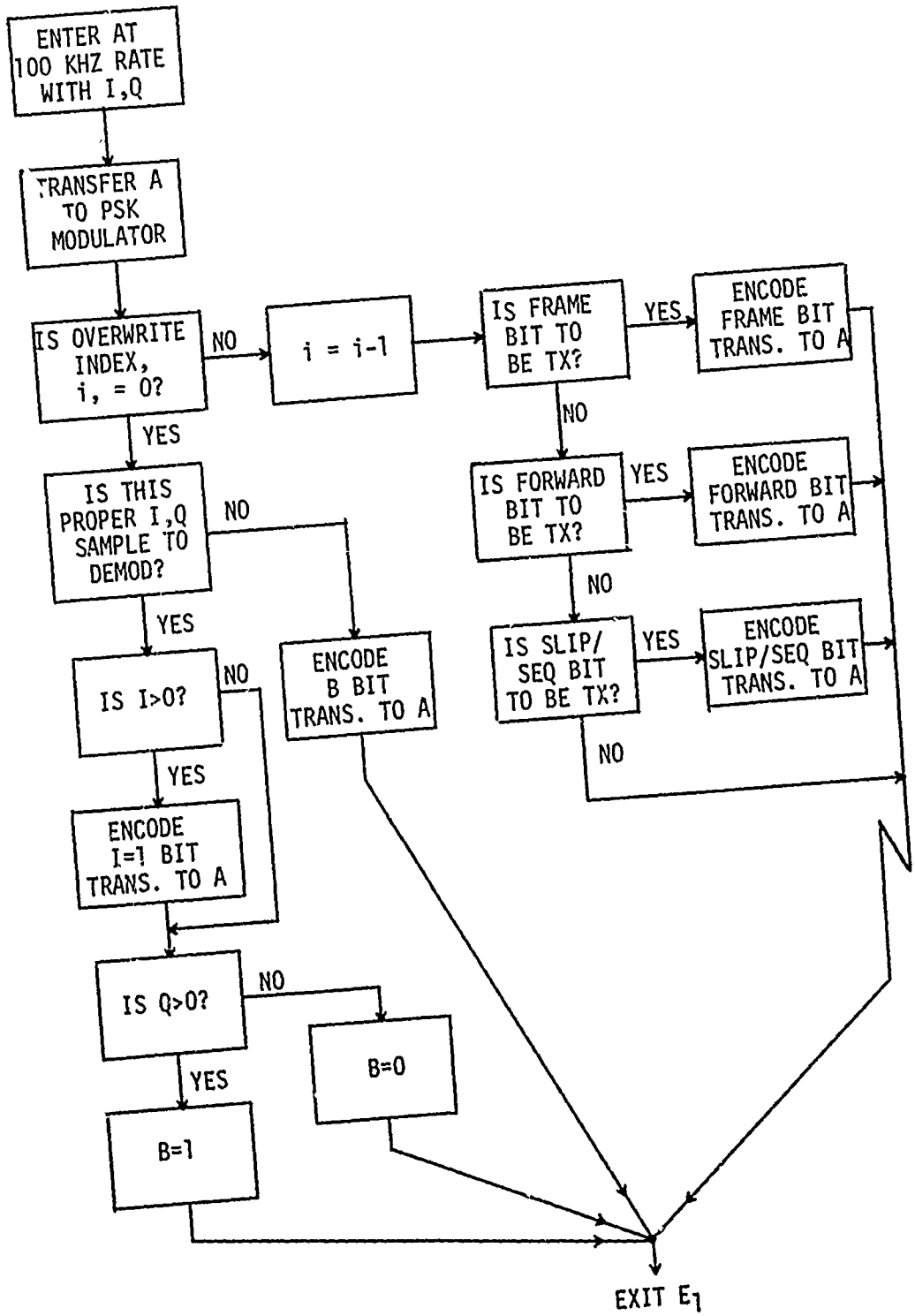

Figure 11a. Functional Flow Diagram of Interrupt #1 for High Rate RB Mode

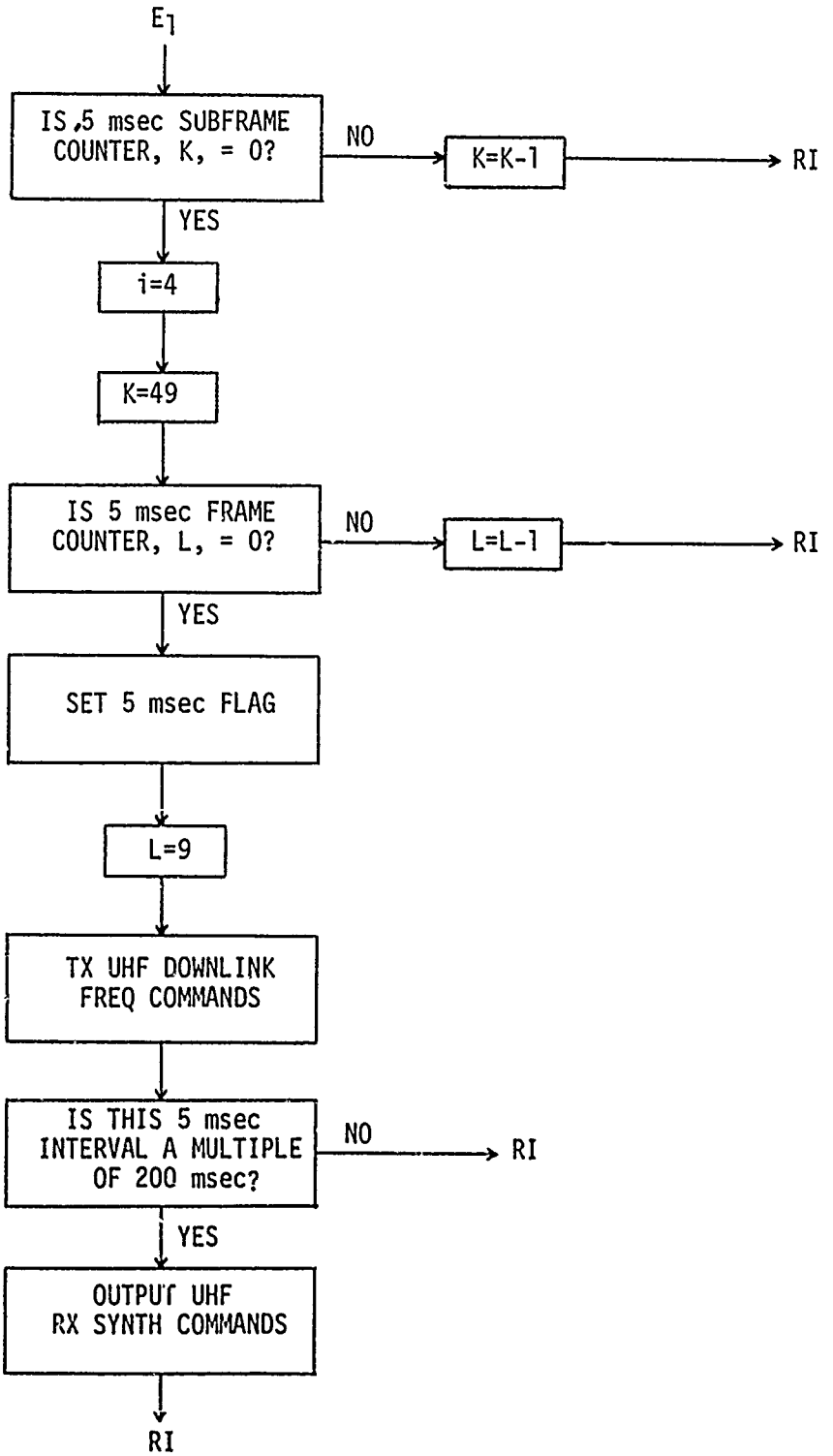

Figure 11b. Functional Flow Diagram of Interrupt #1 for High Rate RB Mode

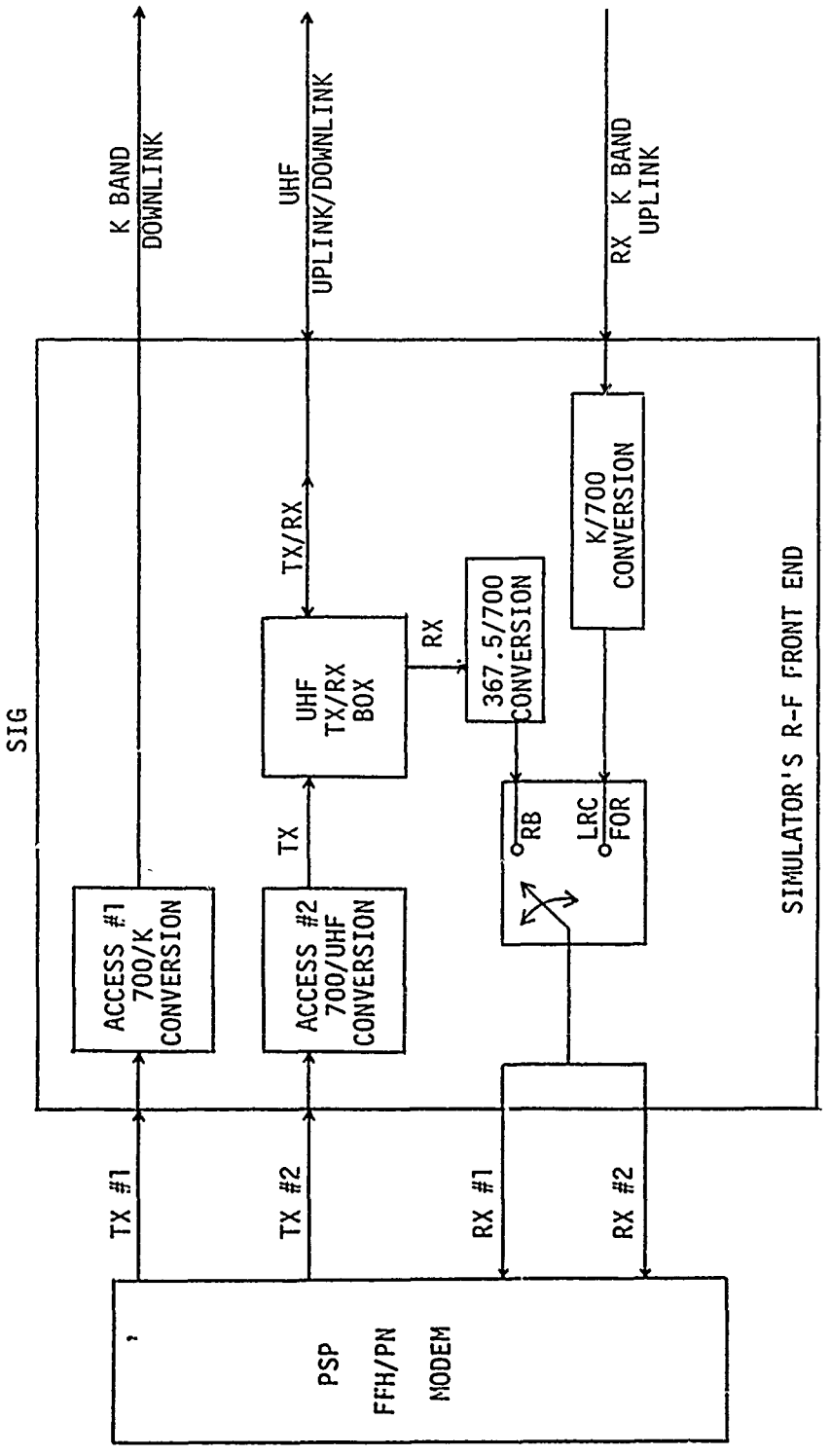

Figure 12. R-F Satellite Simulator

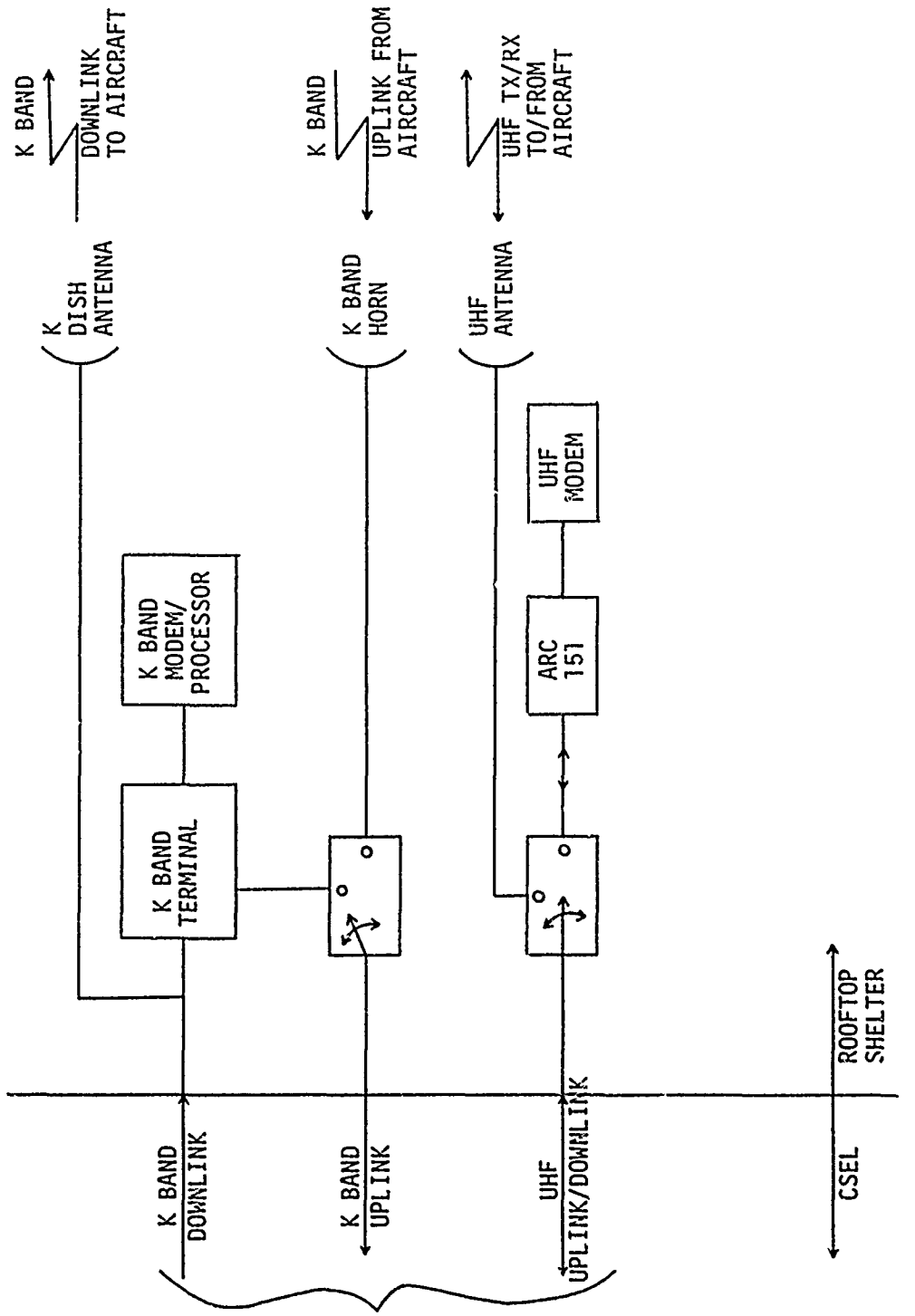

Figure 13. Satellite Test Set-Up

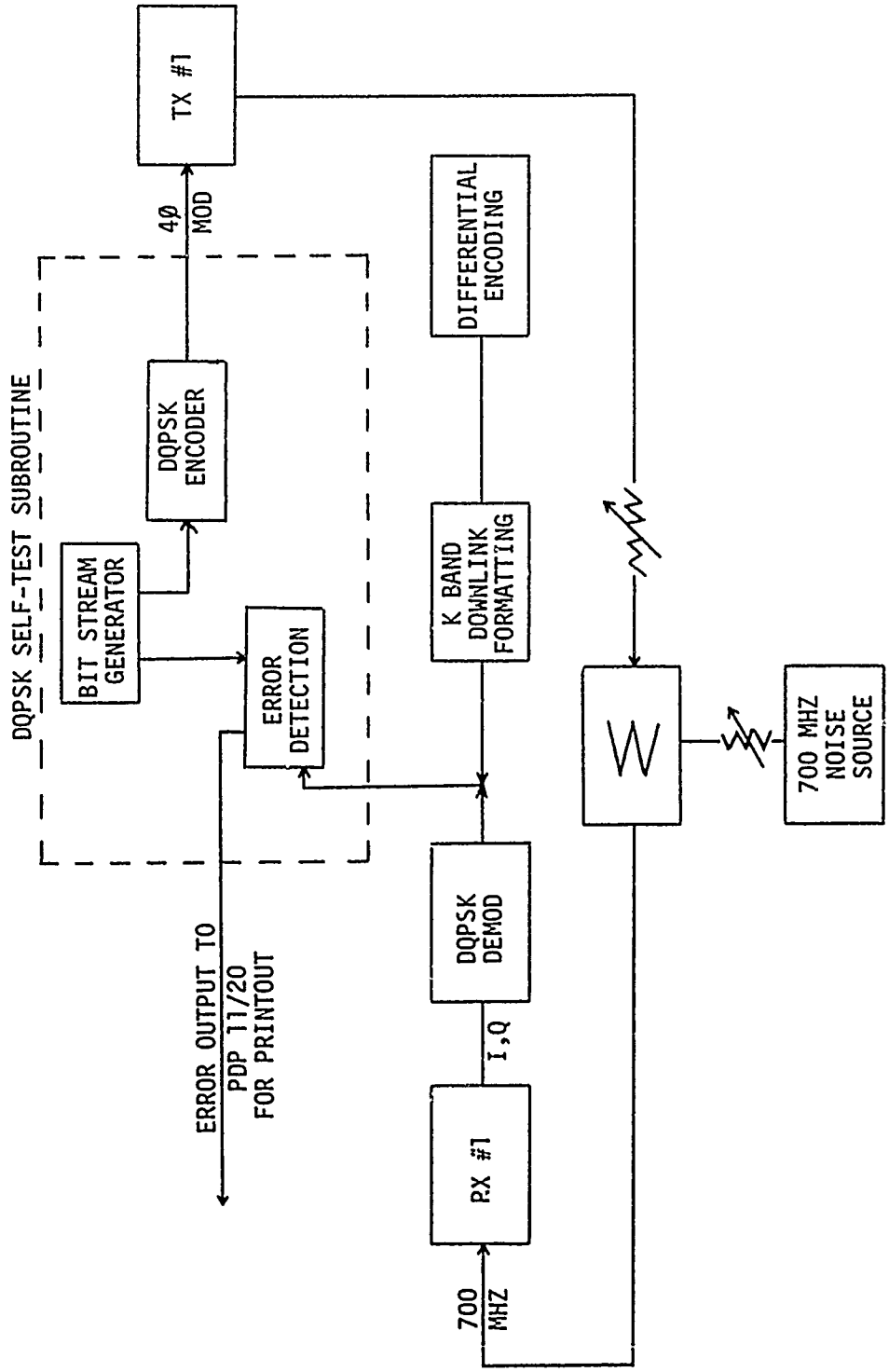

Figure 14. Self-Test System for DQPSK Demodulator

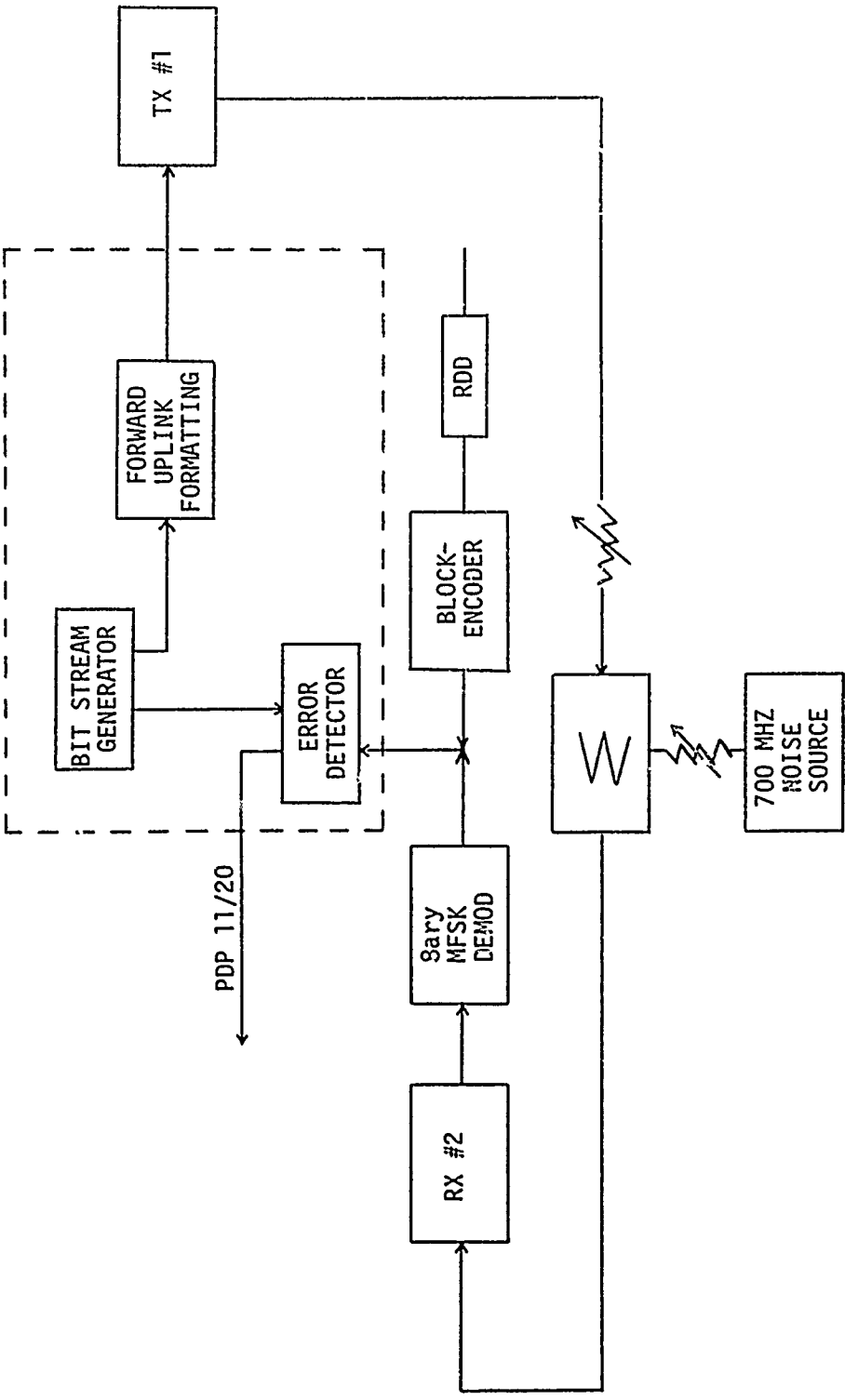

Figure 15. Self-Test System for MFSK Demodulator

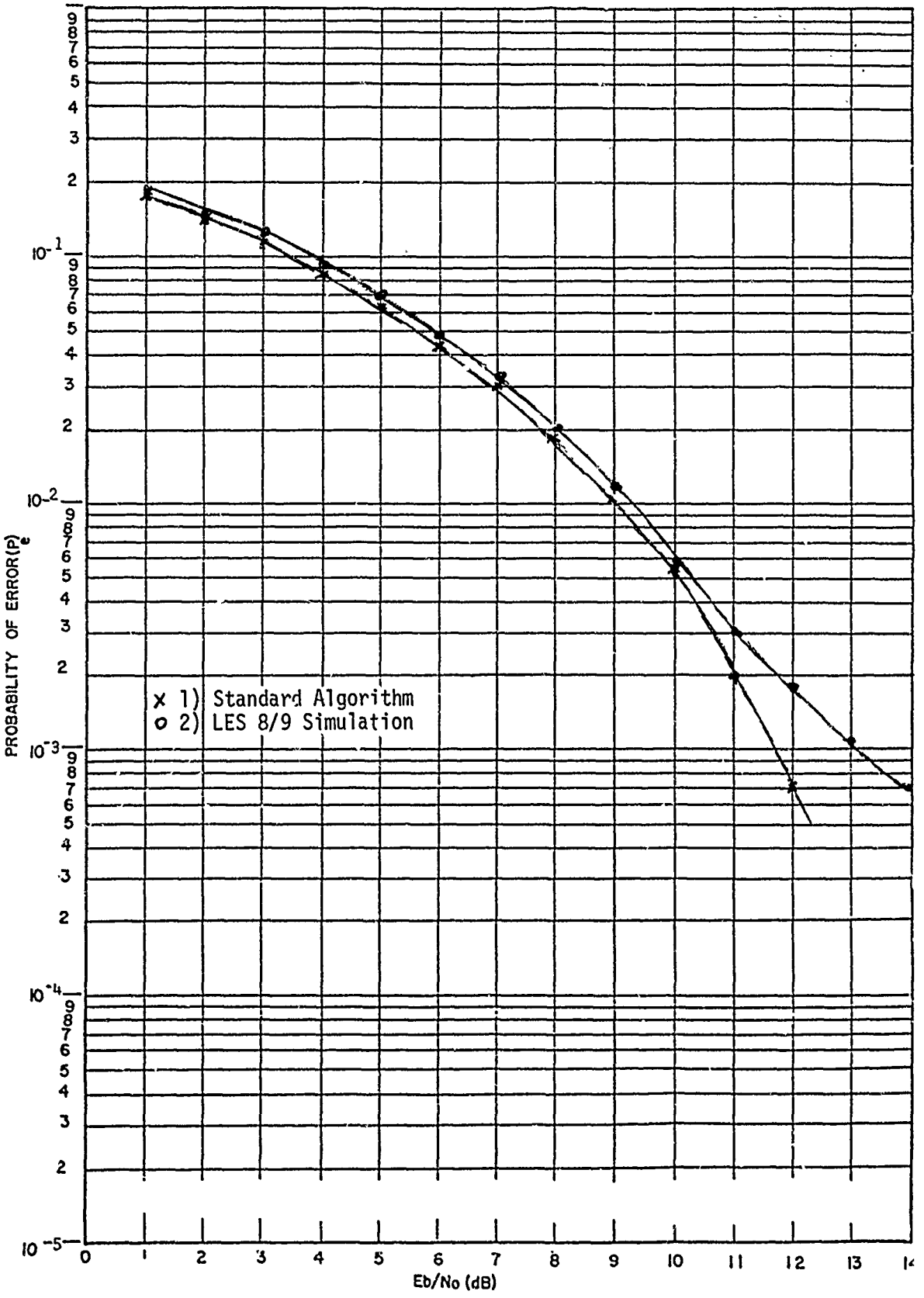

Figure 16. DQPSK LRC (10 KB) Baseline Results

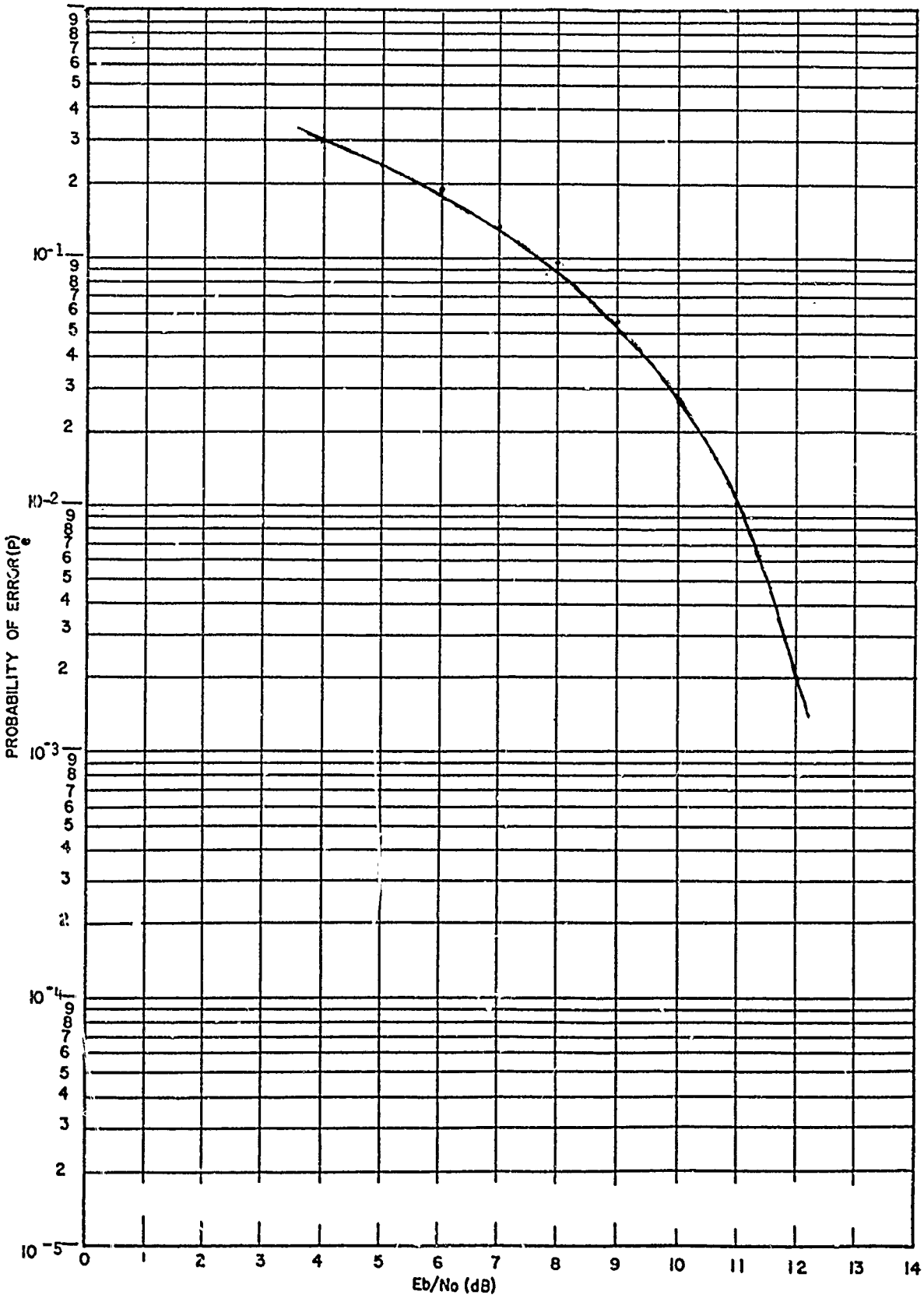

Figure 17. 8ary MFSK Baseline Results

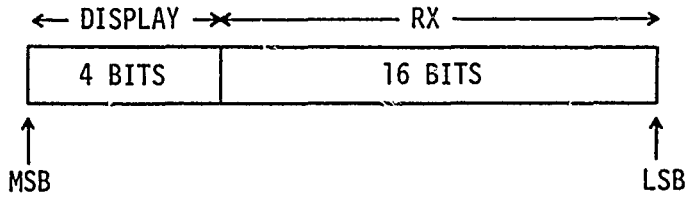

Figure 18. Twenty-Bit Input Command (RX)

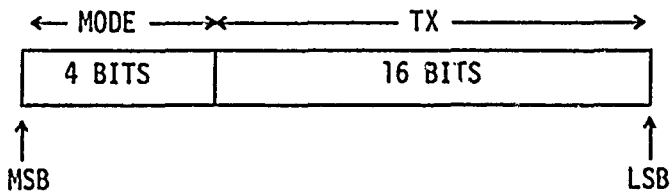

Figure 19. Twenty-Bit Input Command (TX)

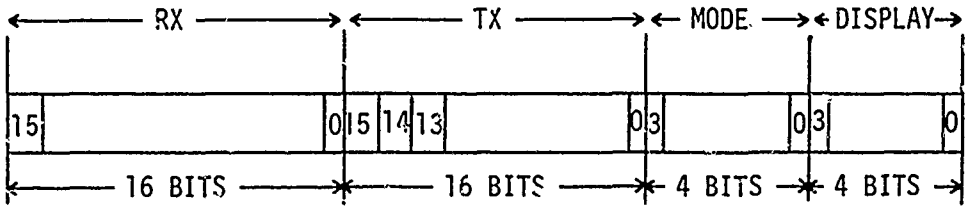

Figure 20. Designation of Doppler Input Commands

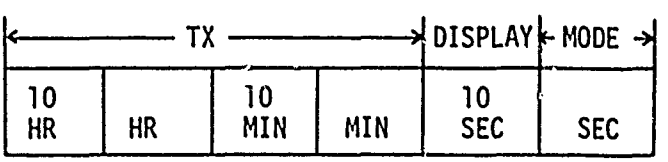

Figure 21. Initial Clock Epoch Input

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