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February 1976

RELIABILITY EVALUATION
of
ALUMINUM IMPLANTED CMOS MICROCIRCUITS

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20. ABSTRACT *(Continue on reverse side if necessary and identify by block number)*

A reliability evaluation of Complementary Metal Oxide Semiconductor (CMOS) microcircuits which were made hard to total ionizing dose by means of ion implanting aluminum in the gate insulator was conducted. The testing revealed the existence of room temperature threshold voltage instabilities. Failure analysis isolated the cause to charge migration within the insulator. A complete description of the instability in relation to temperature and gate voltage is developed. Finally, a model for the CMOS behavior under temperature

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20. Abstract (Cont'd)

bias conditions as well as radiation response is proposed.

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ILLUSTRATIONS

ILLUSTRATIONS (CONTINUED)

I INTRODUCTION:

This report discusses the results of a reliability investigation of a radiation hardened CMOS technology. Radiation studies show the N-channel transistor of a Complementary pair is sensitive to threshold voltage shifts while under bias in a total dose environment. To ameliorate this situation aluminum ions were ion implanted in the SiO_2 of the N-channel MOS gate region.

Dr. H. Hughes of the Naval Research Laboratory, Washington DC, directed the radiation hardening work on these devices and should be contacted for the exact processing procedure of this hardening technique.

DNA provided the funds to perform the reliability testing, the bulk of the routine electrical and environmental testing being performed by STL Electronics of Dallas TX.

II APPROACH:

Initially, the testing schedule planned was as shown in Figures 1A and 1B. However, because of the unexpected threshold voltage instabilities at room temperature, to be discussed later, it was decided that to proceed with the long term life test would be a waste of time and money. The plan then was reduced to that shown in Figure 1A.

The mechanical tests (thermal shock, thermal cycling, mechanical shock and constant acceleration) as well as two stability tests (i.e., temperature storage and ring oscillator) were performed by STL Electronics, Inc., Dallas, Texas, a testing house under contract to RADC.

The microcircuits tested were type 4007 (Dual Complementary Pair plus Inverter), See Figure 2A, where the major interest was the use of these circuit elements as building blocks for the more complex circuits. To ease in the definition of failure and configuring realistic tests, the units were wired as 3-input NOR gates and were subsequently tested to the 4002 NOR gate specifications as shown in Figure 2B. In addition, threshold voltage (V_{th}) measurements and gain (gm) measurements were made on each of the three p and three n channel transistors. This was done to facilitate failure analysis.

When the units arrived at RADC, they were first sent to STL for serialization, fine and gross hermeticity tests and then returned. At this point, V_{TH} and β measurements were taken on all 100 units. Thirty-five units were retained at RADC for those tests shown in Figure 1; the remainder were returned to STL for routine testing. For convenience, the STL and RADC testing results are kept separate in the remainder of the report.

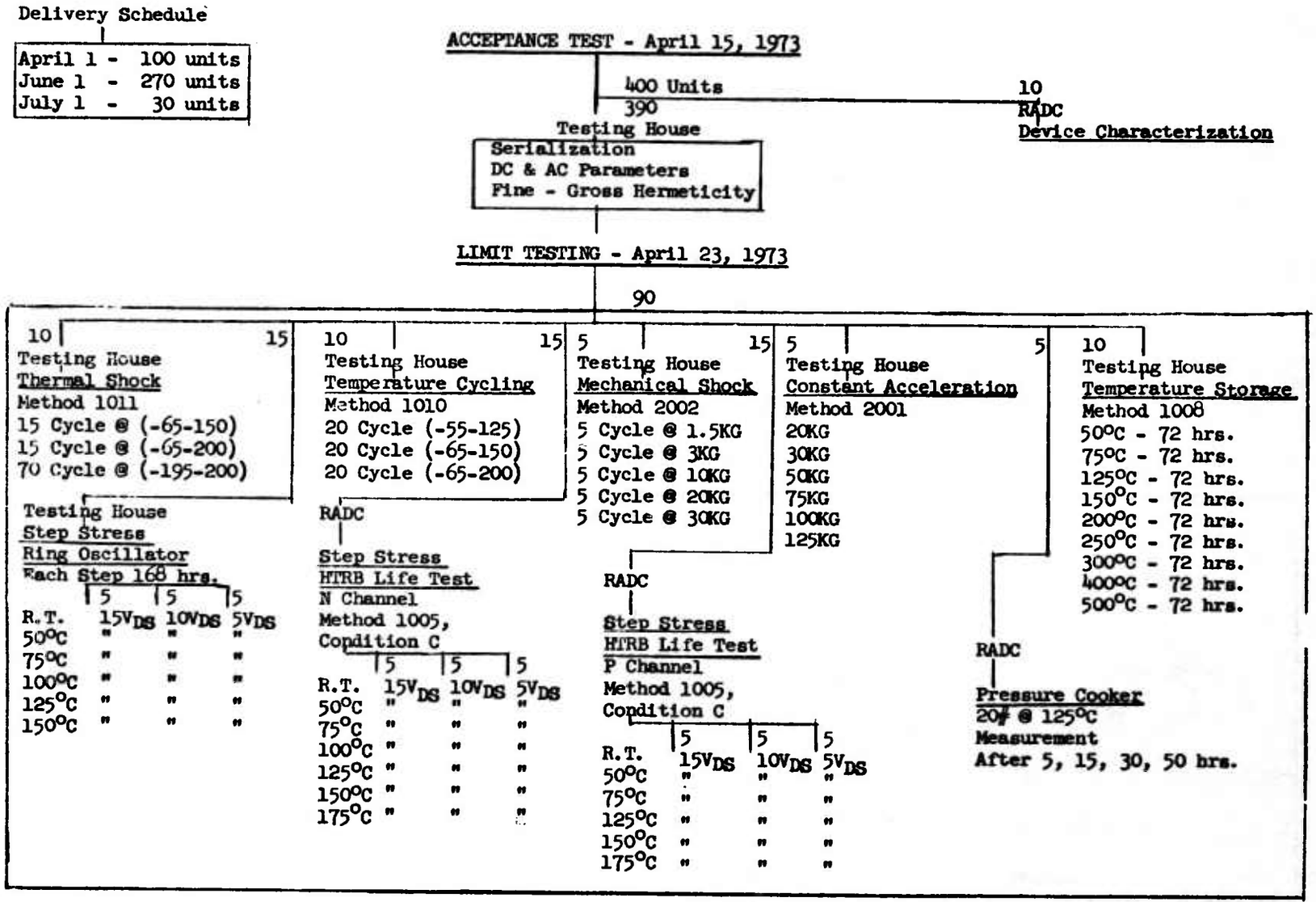


FIGURE 1A
HARDENED CMOS RELIABILITY PROGRAM

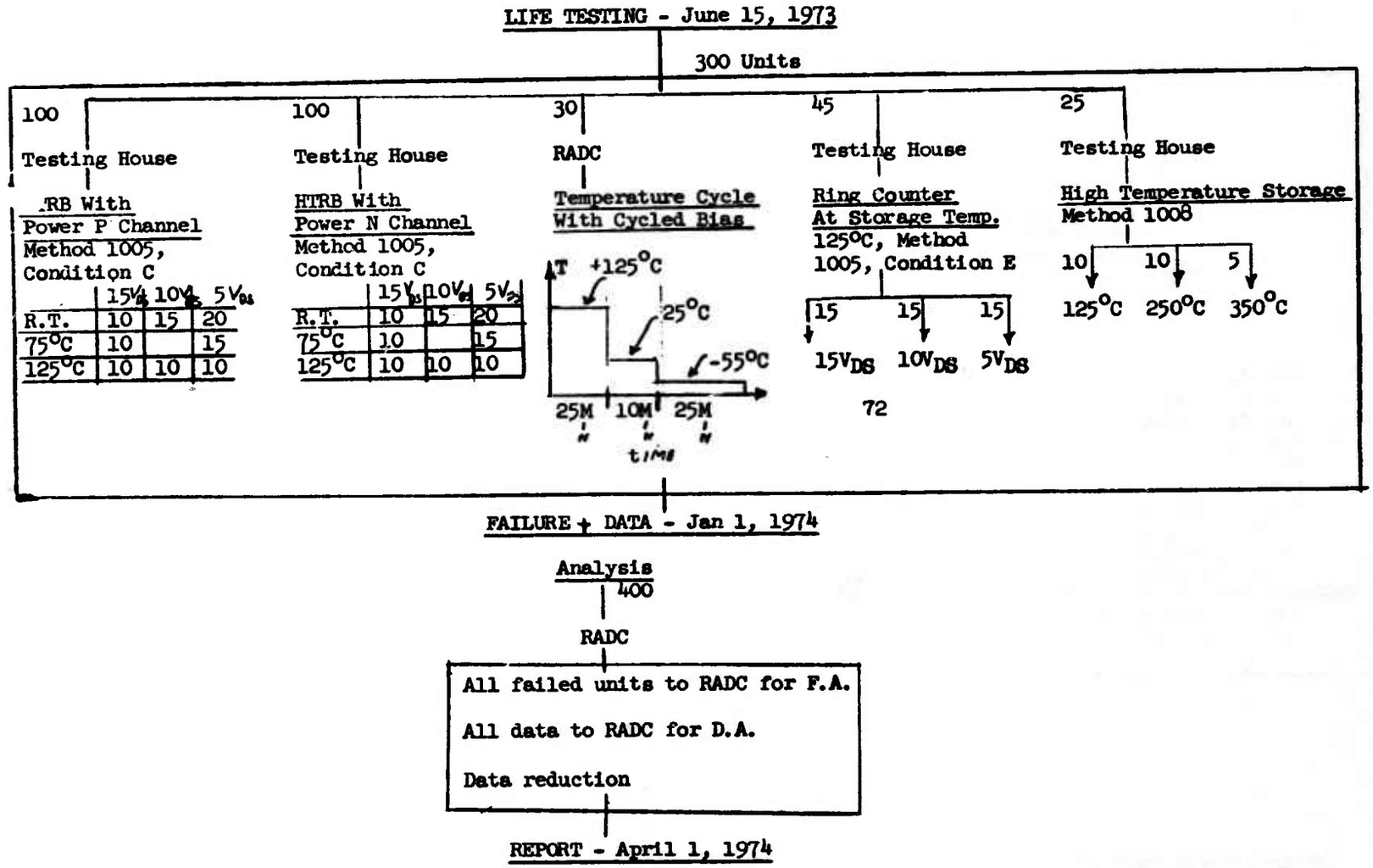


FIGURE 1B
HARDENED CMOS RELIABILITY PROGRAM

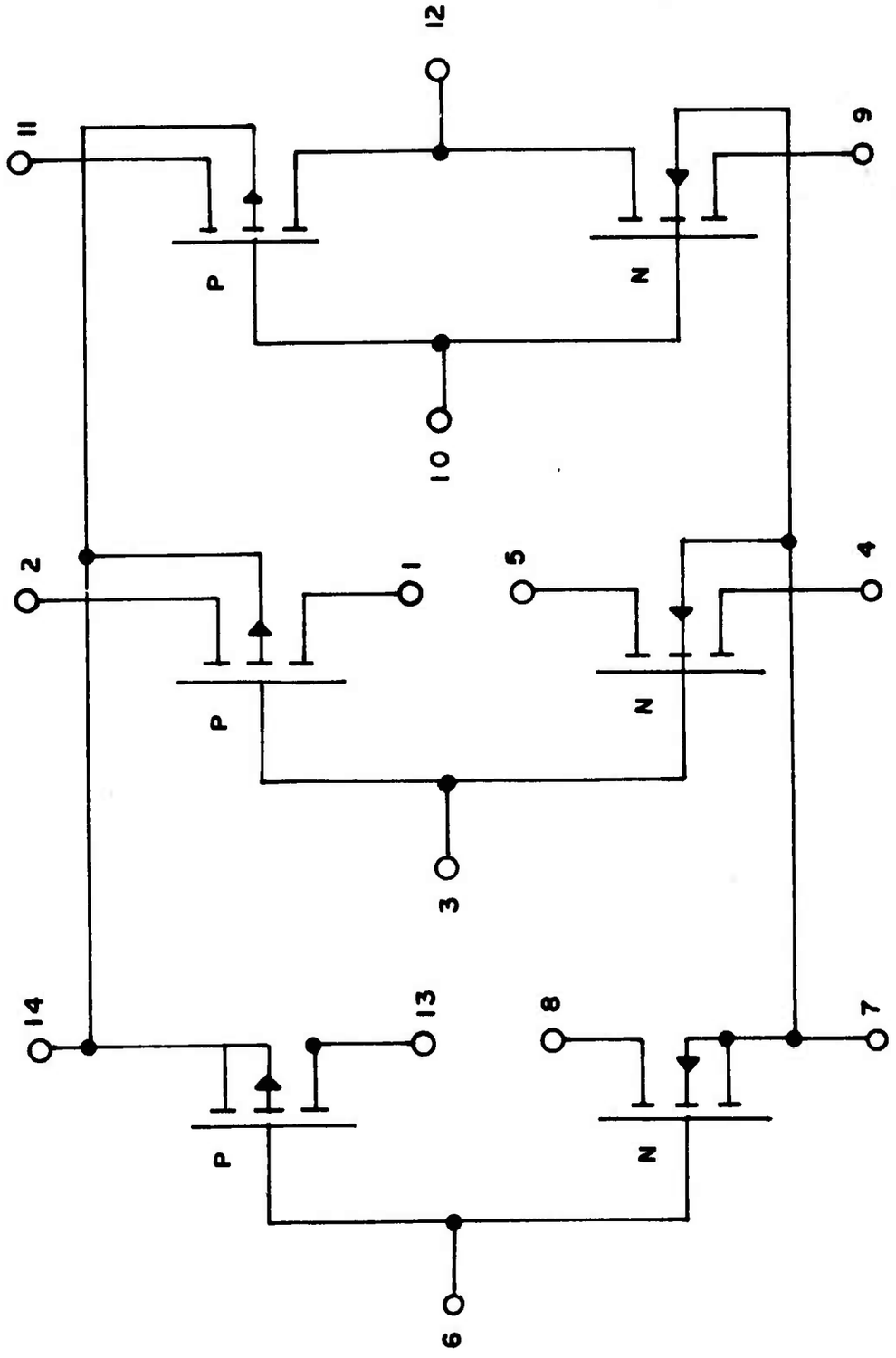


FIGURE 2A
CD4007

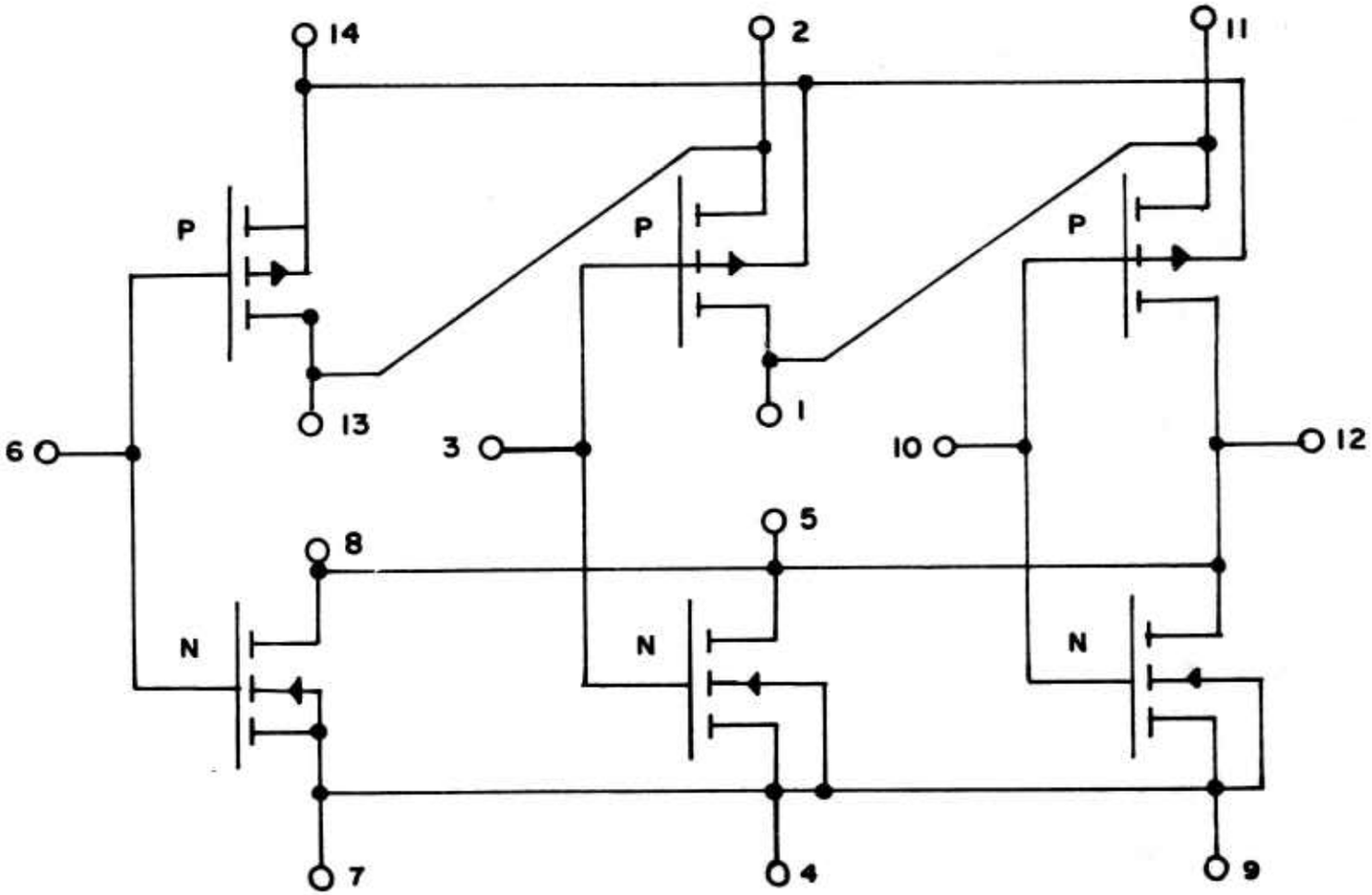


FIGURE 2B
CD4002 WIRING CIRCUIT

III RESULTS:

A. STL Test Results

The STL test results are divided into two categories of stress tests.

1. Mechanical Stress Tests - The following tests are designed to evaluate the integrity of the package, lead bonds and die to header bond.

a. Mechanical Shock (Mil-Std-883, Method 2002)

This shock test calls for a single impact shock to the body of the device ranging between 500 and 30,000 g with a pulse duration between 0.1 and 1.0 milliseconds. For this test program, five devices were subjected to an impulse shock of 1,500 g with D.C. parameter tests followed by 3,000 g with D.C. parameter tests. At the end of the two stress levels, the devices were checked for package hermeticity loss. The results are shown in Table I.

Table I - Mechanical Shock

Test	No. Devices (Serial #)	No. Failures (Serial #)	Parameters Failed
1,500 g	5 (38, 39, 40, 41, 43)	0	0
3,000 g	5 (38, 39, 40, 41, 43)	1 (38)	D.C. Parameter

There were no hermeticity failures.

b. Constant Acceleration (Mil-Std-883, Method 2001)

Constant acceleration is used to test the integrity of flying lead wire bonds and package integrity. In this case it was planned to subject 5 devices to acceleration levels of 20,000 g and 30,000 g. At the end of each stress level, the devices were checked with D.C. parameter readings and hermeticity measurements. The results are shown in Table II.

Table II - Constant Acceleration

Test	No. Devices (Serial #)	No. Failures (Serial #)	Parameters Failed
20,000 g	5 (44, 46, 47, 48, 49)	3 (47, 48, 49)	D.C. Parameter

The 30,000 g level stress was deleted after the poor showing at 20,000 g stress level. There were no hermeticity failures.

c. Thermal Shock (Mil-Std-883, Method 1011)

The purpose of this test is to determine the resistance of the device to sudden exposure to extreme changes in temperature. Effects of thermal shock include opening of terminal seals, case seams, changes in

electrical characteristics due to moisture and mechanical displacement of conductors or insulating materials. The temperature extremes were -65°C to +150°C with a transfer time of less than 10 seconds. D.C. parameter read outs were taken after 25, 50, 75 and 100 temperature cycles. Upon completion of the 100 cycles, a package hermeticity test was made. The results are shown in Table III.

Table III - Thermal Shock

Test	No. Devices (Serial #)	No. Failures (Serial #)	Parameters Failed
25 cycles	10 (28 thru 37)	2 (28, 35)	D.C. Parameter
50 cycles	10 (28 thru 37)	10 (28 thru 37)	D.C. Parameter

2. Stability Stress Tests:

For characterizing a new technology, the most important series of tests are those which attempt to examine the long life capabilities of that technology. The first step in that analysis is a step stress program where the devices are subjected to ever more severe temperatures and voltages until failure occurs. While the step stress program does not provide long life data, it can indicate (depending on the failure level) whether a technology has a reasonable chance of meeting long life requirements.

a. Ring Oscillator Test

In this test the 4007 was configured as a 3-input NOR gate with the devices configured in series where the output of the last device feeds the input of the first to complete the ring. With an odd number of devices in the ring, oscillation between the 1 to 0 states continues indefinitely. Because microcircuit gates are designed to do just this function, their performance in this test is especially meaningful. The Ring Oscillator test closely approximates the normal use of microcircuit gates.

As can be seen from Figure 1, the devices were operated at 3 different bias levels, i.e., 15 volts (maximum specification limit), 10 volts (a value close to normal operation) and 5 volts (a value likely if a T^2L CMOS hybrid system were contemplated).

Initially, in each voltage cell the devices were allowed to oscillate for 168 hours at room temperature. A D.C. parameter reading was taken with failures noted. The devices were placed on test for another 168 hours, but at a higher temperature (50°C). This process was repeated up to 150°C. The results are shown in the following Tables according to voltage cells.

Table IV

Ring Oscillator - 5 Volts V_{DD}, 5 Devices (12 thru 16), (168 hr. steps)

Temperature Step	Previous Failures	New Failures	Recovered Devices	% of the Total
Initial	0	0	0	0%
25°C	0	0	0	0%
50°C	0	0	0	0%
75°C	0	1	0	20%
100°C	1	4	0	100%
125°C	5	0	3	40%
150°C	2	1	2	20%

Table V

Ring Oscillator - 10 Volts, 168 hr. steps, 5 Devices (7 thru 11)

Temperature Step	Previous Failures	New Failures	Recovered Devices	% of the Total
Initial	0	0	0	0%
25°C	0	0	0	0%
50°C	0	5	0	100%
75°C	5	0	0	100%
100°C	5	0	3	40%
125°C	2	0	2	0%
150°C	0	1	0	20%

Table VI

Ring Oscillator - 15 Volts V_{DD}, 168 hr. step, 5 Devices (1-6)

Temperature Step	Previous Failures	New Failures	Recovered Devices	% of the Total
Initial	0	3	0	60%
25°C	3	2	0	100%
50°C	5	0	0	100%
75°C	5	0	0	100%
100°C	5	0	4	20%
125°C	1	0	0	20%
150°C	1	0	0	20%

b. Temperature Cycle With Bias

This test is conducted for the purpose of determining the resistance of a part to exposures at extremes of high and low temperatures, and to the effect of alternate exposures to these extremes, such as would be experienced when equipment or parts are transferred to and from heated shelters in arctic areas. The bias is applied to simulate operational environment. It is particularly important for accelerating moisture dependent electrochemical corrosion.

The devices were again configured as a triple input NOR gate. The units were then subjected to 10 minutes at -55°C, a transition to room temperature of no more than 5 minutes, followed by 10 minutes at 125°C with a return to room temperature again of no more than 5 minutes to complete one temperature cycle. During this entire time, power was applied with a V_{DD} equal to 10 volts.

Table VII

Temperature Cycle With Bias

Test	No. Devices (Serial #)	No. Failures	Parameters Failed
Initial	25 (39, 40, 41, 43, 44, 46, 50 thru 70 minus 67)	0	0
100 cycles		25	D.C. Parameters

Test Discontinued

c. Temperature Storage

The purpose of this test is to determine the effect on microelectronic devices of storage at elevated temperatures without electrical stress applied. The devices were stressed at each step for 72 hours. (The results are shown in Table VIII).

Table VIII

Temperature Storage

Test	No. Devices (Serial #)	No. Failures	Parameters Failed
Initial	10 (17 thru 27)	0	D.C. Parameters
150°C		1	D.C. Parameters
250°C		6	D.C. Parameters
350°C		10	D.C. Parameters

B. RADC In-House Testing

The testing performed at RADC was devoted to High Temperature Reverse Bias (HTRB) stress testing. Originally this test was designed for bipolar microcircuits and called for placing as many junctions in reverse bias as possible and elevating the temperature. The intent of the test was to check the integrity of passivation layer. Mobile surface ions or contaminants in the oxide could be caused to migrate due to the temperature and fringing fields present. This, in turn, could result in unwanted inversion layers to form on the chip.

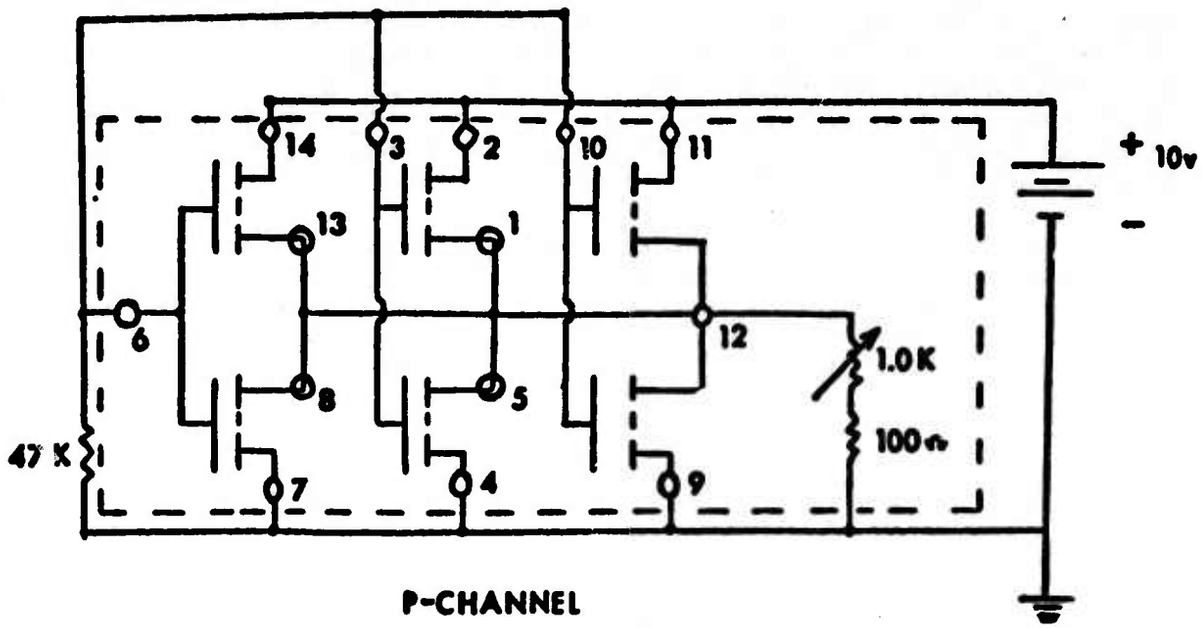
The test as it applied to CMOS is primarily intended to examine mobile ions in the insulator or, for that matter, any charge instability in the MOS insulator. As can be seen from Figure 1, CMOS requires two bias cells instead of one. Each type of transistor, n and p channel, must be stress tested separately, since at any instant a strong field across one implies a weak field across the other transistor insulator.

The units were configured as 3-input NOR gates and placed in the stress circuit shown in Figure 3. Note that in addition to the steady state voltage from insulator to substrate, some current was allowed to flow through the turned on p or n channel transistor. The load resistor was adjusted so that for V_{DD} = 5 and V_{DD} = 10 V the voltage at the output was set at 2 volts, for a V_{DD} = 15 V the output voltage was 3 volts. This meant a steady current of approximately 10 mA was being driven through 3 n channel devices in parallel or 3 p channel transistor in series. As will be shown later, this load current had no effect on the results observed.

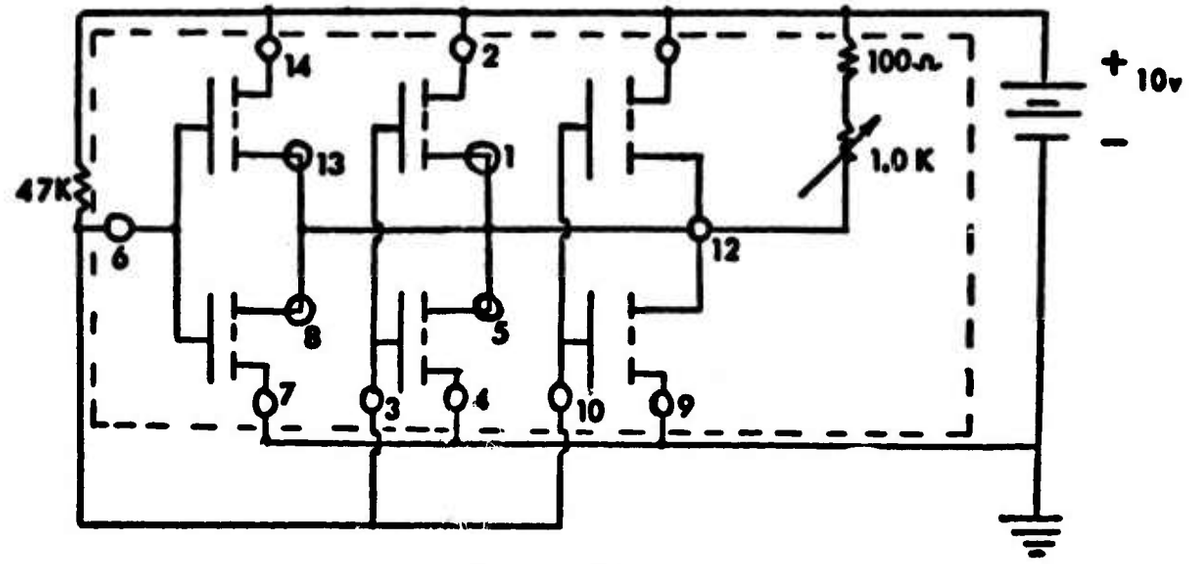
In anticipation of some voltage dependence on stability, the step stress program was designed as shown in Figure 1. Note that in total there are six step stress cells at any given temperature, three n-channel cells being biased at 5, 10 and 15 volts respectively, and three p-channel cells under the same bias conditions. In each cell there were five devices.

While D.C. parameter measurements as well as gain and threshold voltage measurements were taken, the essential results are best illustrated by a comparison of the threshold voltage stability of the devices as they went through the step stress program. The results are shown in Tables IX thru XIV.

As can be seen from the Tables, the p channel devices are very stable while the n channel units are not. This is particularly true for the transistor N1 which shows room temperature instabilities, and N2 and N3 which are unstable but at higher temperatures. In fact, even on the initial reading, N1 is sufficiently different to warrant further investigation. An investigation into the essential differences and the cause of that difference was the major effort in failure analysis reported in that section.



P-CHANNEL



N-CHANNEL

FIGURE 3
4007 HTRB STRESS CIRCUIT

TABLE IX

P CHANNEL 5 VOLTS BIAS
(DEVICES 42,45,67,72,73)

TEST CONDITION	THRESHOLD VOLTAGE	STANDARD DEVIATION	DEVICES TESTED
INITIAL	P1-1.87	0.07	42 45 67
	P2-1.93	0.11	72 73
	P3-1.93	0.10	
RMTEMP/72HRS	P1-1.88	0.07	42 45 67
	P2-1.94	0.11	72 73
	P3-1.93	0.10	
RMTEMP/167HR	P1-1.93	0.02	42 45 67
	P2-2.03	0.06	72 73
	P3-2.01	0.06	
50 C/72HRS	P1-1.88	0.07	42 45 67
	P2-1.94	0.11	72 73
	P3-1.94	0.10	
75 C/48HRS	P1-1.86	0.08	42 45 67
	P2-1.94	0.11	72 73
	P3-1.94	0.10	
100 C/48HRS	P1-1.88	0.07	42 45 67
	P2-2.35	0.84	72 73
	P3-1.93	0.10	
125 C/72HRS	P1-1.90	0.03	42 45 67
	P2-1.94	0.03	72 73
	P3-1.93	0.01	

TABLE X

P CHANNEL 10 VOLTS BIAS
(DEVICES 75,76,77,78)

TEST CONDITION	THRESHOLD VOLTAGE	STANDARD DEVIATION	DEVICES TESTED
INITIAL	P1-2.01	0.08	75 76 77
	P2-2.06	0.09	78
	P3-2.04	0.10	
RMTEMP/72HRS	P1-1.98	0.03	75 76 77
	P2-2.04	0.05	78
	P3-2.02	0.06	
RMTEMP/167HR	P1-1.98	0.04	75 76 77
	P2-2.04	0.05	78
	P3-2.02	0.07	
50 C/HRS	P1-1.98	0.04	75 76 77
	P2-2.04	0.05	78
	P3-2.03	0.06	
75 C/48HRS	P1-1.98	0.04	75 77 78
	P2-2.04	0.05	
	P3-2.00	0.06	
100 C/48HRS	P1-1.97	0.04	75 77 78
	P2-2.02	0.05	
	P3-2.00	0.05	
125 C/72HRS	P1-1.96	0.04	75 77 78
	P2-2.00	0.04	
	P3-1.98	0.05	

TABLE XI

P CHANNEL 15 VOLTS BIAS
(DEVICES 79,80,81,82,83)

TEST CONDITION	THRESHOLD VOLTAGE	STANDARD DEVIATION	DEVICES TESTED
INITIAL	P1-1.80	0.08	79 80 81
	P2-1.82	0.07	82 83
	P3-1.83	0.10	
RMTEMP/72HRS	P1-1.80	0.08	79 80 81
	P2-1.82	0.07	82 83
	P3-1.83	0.10	
RMTEMP/167HR	P1-1.81	0.08	79 80 81
	P2-1.82	0.07	82 83
	P3-1.84	0.10	
50 C/72HRS	P1-1.81	0.08	79 80 81
	P2-1.82	0.07	82 83
	P3-1.83	0.10	
75 C/48HRS	P1-1.81	0.08	79 80 81
	P2-1.83	0.07	82 83
	P3-1.83	0.10	
100 C/48HRS	P1-1.80	0.09	79 80 81
	P2-2.24	0.89	82 83
	P3-1.82	0.10	
125 C/72HRS	P1-1.80	0.08	79 80 81
	P2-2.26	0.90	82 83
	P3-1.82	0.09	

TABLE XII

N CHANNEL 5 VOLTS BIAS
(DEVICES 84,85,86,87,88)

TEST CONDITION	THRESHOLD VOLTAGE	STANDARD DEVIATION	DEVICES TESTED
INITIAL	N1 1.79	0.04	84 85 86
	N2 3.09	0.09	87 88
	N3 3.32	0.09	
RMTEMP/72HRS	N1 1.41	0.03	84 85 86
	N2 3.07	0.09	87 88
	N3 2.89	0.10	
RMTEMP/167HR	N1 1.30	0.16	84 86 87
	N2 3.04	0.09	88
	N3 3.25	0.08	
50 C/72HRS	N1 1.31	0.06	84 86 87
	N2 3.04	0.09	88
	N3 3.24	0.08	
75 C/48HRS	N1 0.88	0.03	84 86 87
	N2 2.94	0.11	88
	N3 3.12	0.11	
100 C/48HRS	N1-0.61	0.01	84 86 87
	N2 1.82	0.20	88
	N3 1.85	0.19	
125 C/72HRS	N1 2.84	0.11	84 86 87
	N2 3.29	0.07	88
	N3 3.42	0.05	

TABLE XIII

N CHANNEL 10 VOLTS BIAS
(DEVICES 90,91,92,93,94)

TEST CONDITION	THRESHOLD VOLTAGE	STANDARD DEVIATION	DEVICES TESTED
INITIAL	N1 1.74	0.06	90 91 92
	N2 2.99	0.18	93 94
	N3 3.17	0.17	
RMTEMP/72HRS	N1 0.30	0.12	90 91 92
	N2 2.61	0.23	93 94
	N3 2.72	0.24	
50 C/72HRS	N1-0.74	0.32	90 91 92
	N2 2.23	0.31	93 94
	N3 2.26	0.39	
75 C/48HRS	N1-0.03	0.28	90 92 93
	N2 2.28	0.15	94
	N3 2.36	0.20	
100 C/48HRS	N1-0.89	0.04	90 92 93
	N2-0.35	0.20	94
	N3-0.49	0.06	

TABLE XIV

N CHANNEL 15 VOLTS BIAS
(DEVICES 25,95,97,98,99)

TEST CONDITION	THRESHOLD VOLTAGE	STANDARD DEVIATION	DEVICES TESTED
INITIAL	N1 1.73	0.13	25 95 97
	N2 3.23	0.30	98 99
	N3 3.40	0.29	
RMTEMP/72HRS	N1-0.43	0.02	25 95 97
	N2 2.15	0.07	98 99
	N3 3.33	0.15	
50 C/72HRS	N1 3.10	0.21	25 95
	N2 1.27	0.05	
	N3 4.09	0.23	
75 C/48HRS	N1-0.39	0.16	25 95 97
	N2 2.69	0.35	
	N3 2.67	0.30	
100 C/48HRS	N1 5.01	0.75	25 95 97
	N2-0.55	0.06	
	N3 0.42	0.67	

IV FAILURE ANALYSIS:

It was apparent very early in the testing that something was different about the N1 transistor compared to N2 and N3. To begin with, its threshold voltage was significantly lower than the other two transistors. Table XV is a summary of the threshold voltages for the entire NRL lot of 100 devices received.

Table XV

Transistor	Average V_{th}	Std. Dev.	% Std. Dev.
P1	-1.94	±.12	± 6%
P2	-2.05	±.55	±27%
P3	-2.04	±.63	±31%
N1	1.84	±.28	±15%
N2	3.30	±.79	±24%
N3	3.51	±.34	±10%

In addition, from the Tables IX thru XIV, the N1 transistor has considerable room temperature instability.

Much of the failure analysis was focused on this transistor and its behavior. A graphical description of the charge instability is shown in Figures 4 and 5 where a comparison in behavior of the N2 transistor can be made with the N1 transistor. At the higher steady state biases, i.e., 10 and 15 volts, N1 is very unstable, failing in 72 hours at room temperature. The 5 volt bias required approximately 48 hours at 100°C to cause the N1 transistor to be turned on. At the same time, it is clear that while N2 is significantly more stable, it too is turned on in the relatively benign test of 48 hours of bias at 100°C. Each line on the graph represents the average value of threshold voltage for 5 devices. The threshold voltage here is defined as that gate voltage necessary to drive 10 μA of current through the transistor with a 10 volt drain to source voltage.

A. Device Description

Because the initial measurements indicated a very uniform electrical characteristic for the lot and because there was no apparent random behavior in the devices tested under the various stress test programs, as well as the bias-temperature stability tests, the first thought on the problem was the existance of some mask error in device production.

With this in mind, a careful study of the device and its operation was made. The chip is shown in Figure 6. Notice the p channel devices have channel widths approximately three times that of the n channel transistors. In addition, the N1 device is grounded internally making it unique with respect to N2 and N3. It has been known for some time the presence of a guard band diffusion serving as a channel stopper is an essential feature

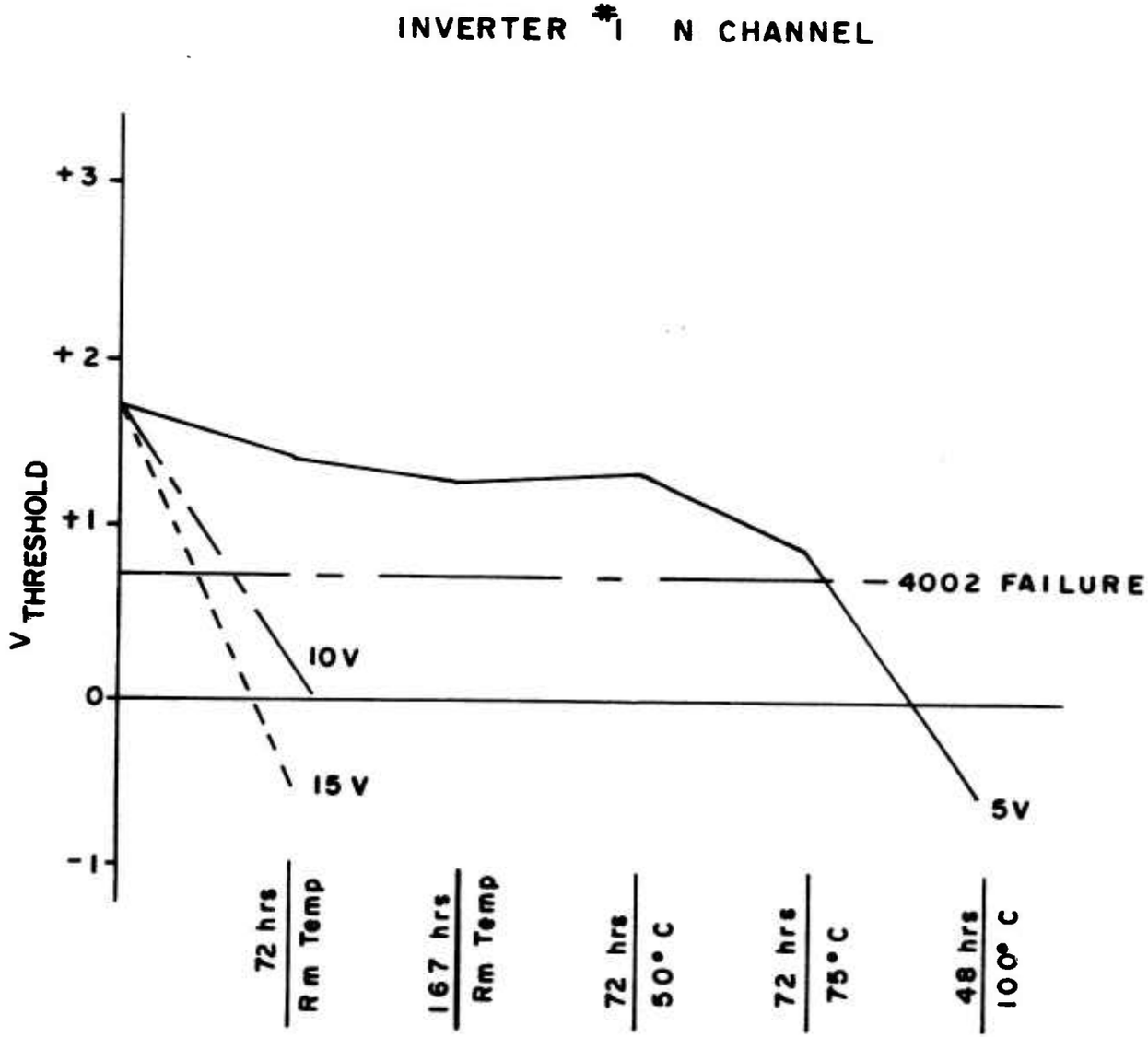


FIGURE 4
THRESHOLD VOLTAGE AS A FUNCTION OF STATIC BIAS STRESS

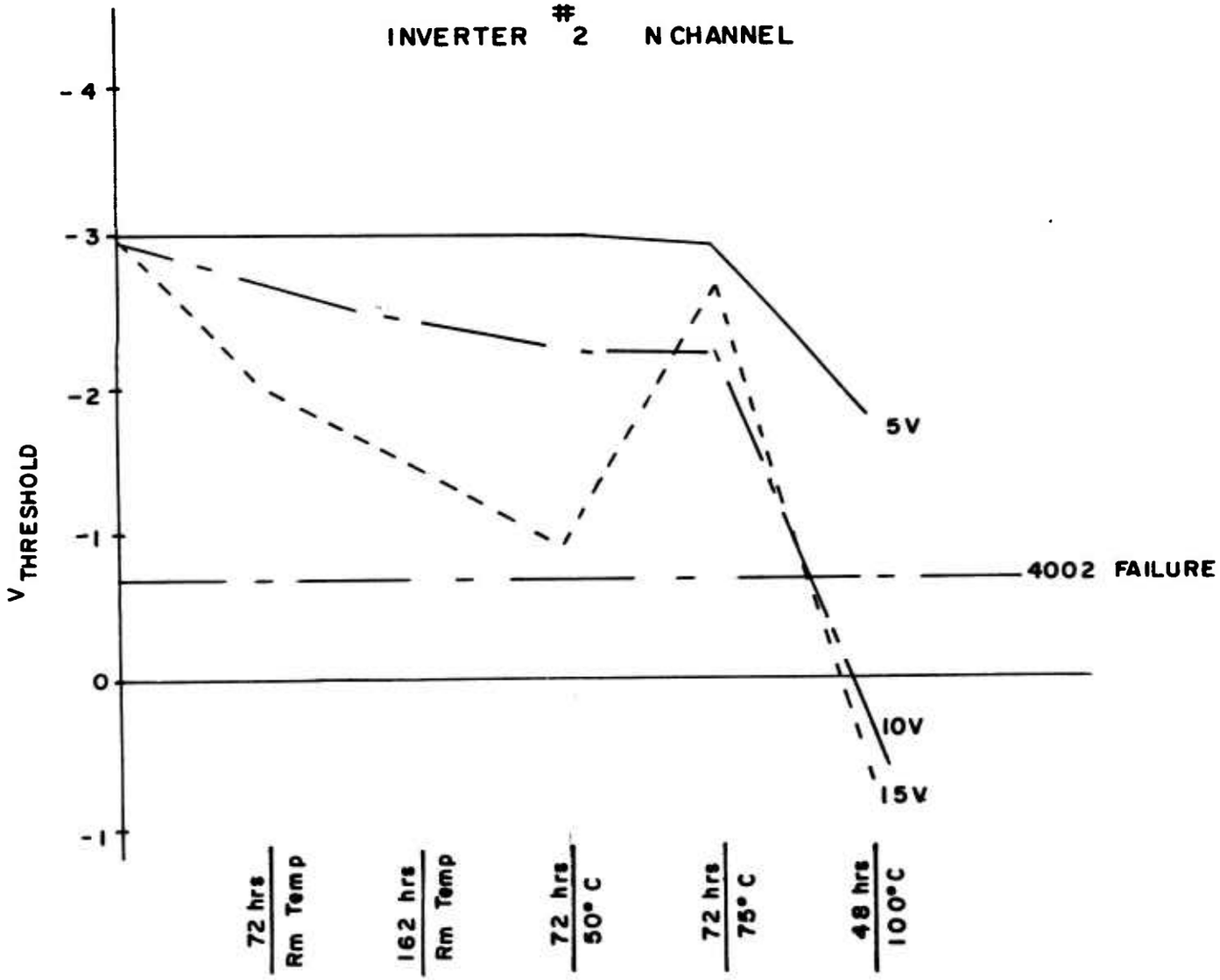
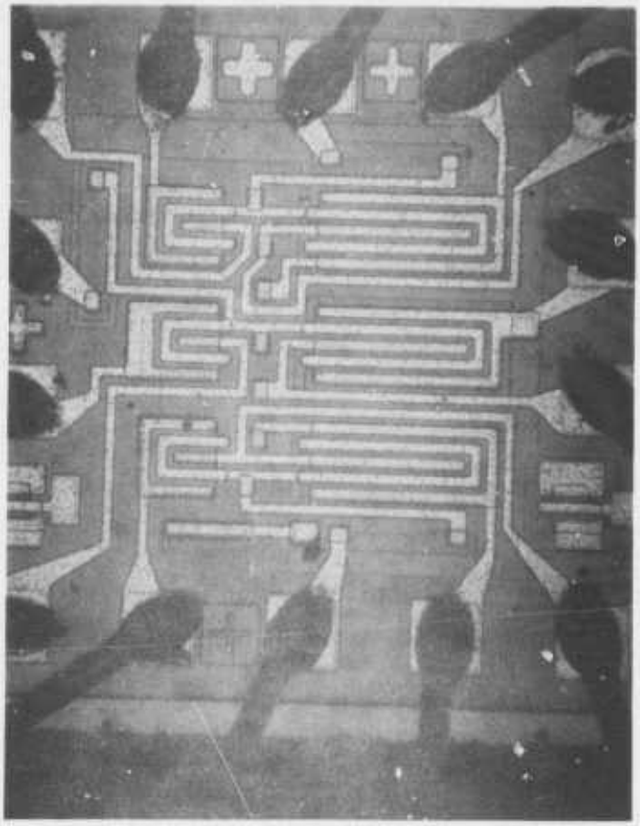


FIGURE 5
THRESHOLD VOLTAGE AS A FUNCTION OF STATIC BIAS STRESS



100 X MAGNIFICATION

FIGURE 6
4007 MICROCIRCUIT

for stable MOS transistor operation. Several models were postulated which attempted to account for the lower initial threshold voltage. One of the most promising models was based upon the gate lead riding slightly over the lightly doped p well. This could be expected to invert that region and would be electrically connected to the drain. Should the remaining p well become inverted as a result of surface charging, further conduction would take place. This effect might explain the charge instability but not the initially low threshold voltage on N1. Furthermore, as long as the channel stop is present, there can be no electrical connection between the source and drain without a gate voltage providing the inversion. Figure 7 shows the N1 channel transistor in question and a drawing of the model just presented. The arrows indicate the hypothetical current path between source and drain. Also shown on the drawing is the effect of a faulty guard band. Surface charging denoted by I_{DS} could very definitely cause both an initial shift in threshold voltage as well as charge instability.

Having eliminated the gate metallization path as a workable model, an angle lap and stain of one of the devices which was demonstrated to have an unstable threshold voltage was performed to investigate the presence of the p+ channel stop. From Figure 8 it is clear this p+ guard band completely surrounds each n channel transistor and that surface charging would have to invert the p+ region in order to connect source and drain.

B. Photoresponse

To insure further that no such leakage path existed, a failed unit was subjected to a photoresponse[1] measurement. The principal of this instrument is based upon photovoltage a p-n junction generates when exposed to light. Should the p+ guard ring be inverted, a response of this additional junction should be seen. For more details the reader is advised to see Reference 1.

An initial measurement was made as shown in Figure 9. Notice the complete absence of the source-to-substrate junction response because the junction is shorted and no photovoltage is possible. Nevertheless, the drain region, except where blocked by the drain metallization is visible. An extension of this junction would indicate possible surface charging effects. To understand the response the reader is referred to Figure 6. For N2 and N3 the source region is not grounded to the p and p+ regions as in Figure 6. A light spot scanning the transistor when in the p- region must be extremely close to the p region in order for minority carriers to reach the source diffusion giving rise to a photovoltage. When the light spot hits the lightly doped p well (the diffusion length estimated to be roughly 40 mils) the minority carriers generated should reach the source region with very little recombination, thus giving a good signal denoted by brightness in Figures 9 thru 11. Next the light spot hits the metallization and we have dark current only. The light spot falls on the n+ source and drain diffusions. In the n+ region the recombination of minority carriers is high but the diffusion of the carriers is simply the depth of that source or drain diffusion (approximately 1.5 microns). A response is seen but considerably lower in magnitude when compared to the lightly doped p region. The device (1056) was subjected to 5 hours, 15 volts gate to substrate bias on each of the three transistors. As was expected,

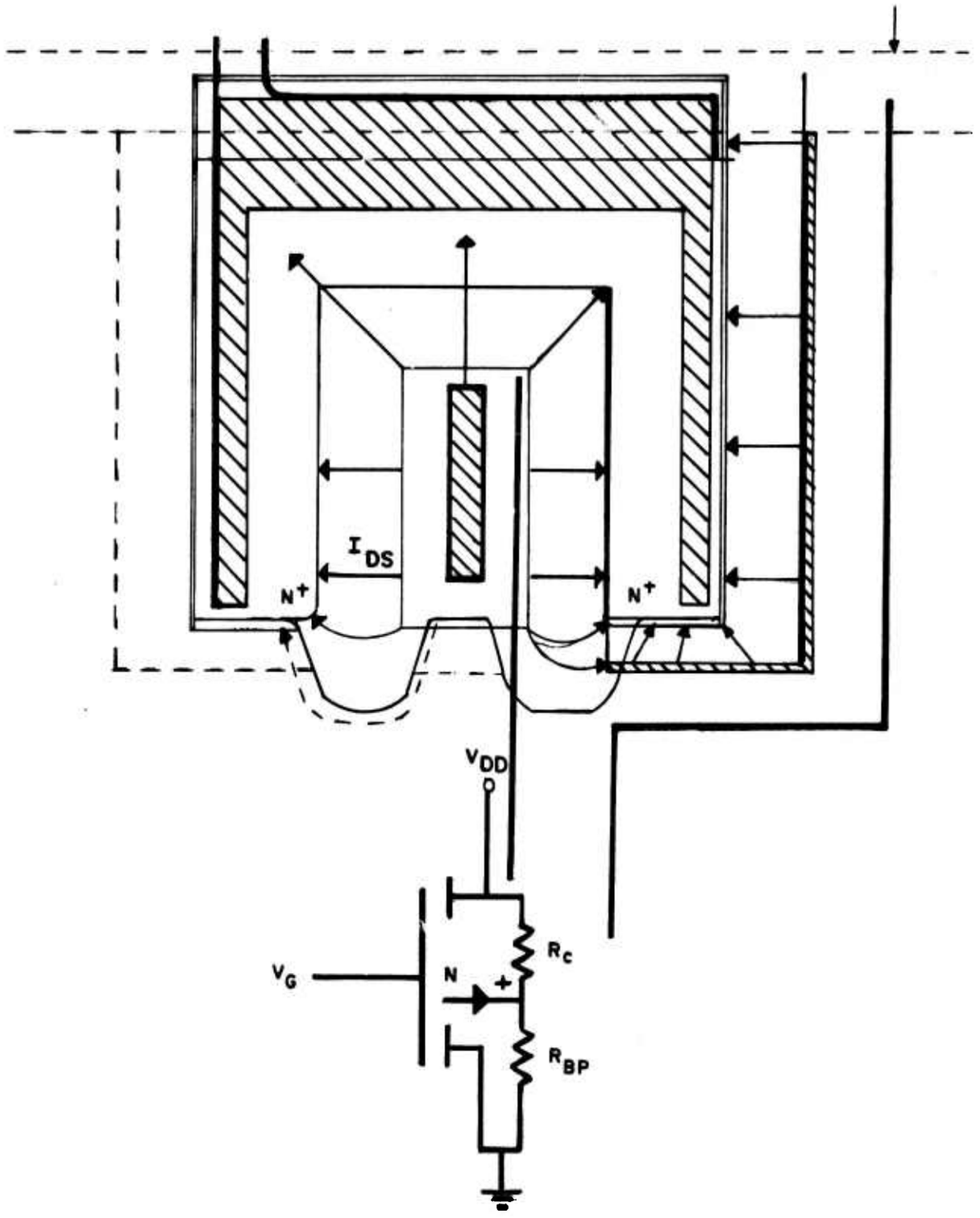
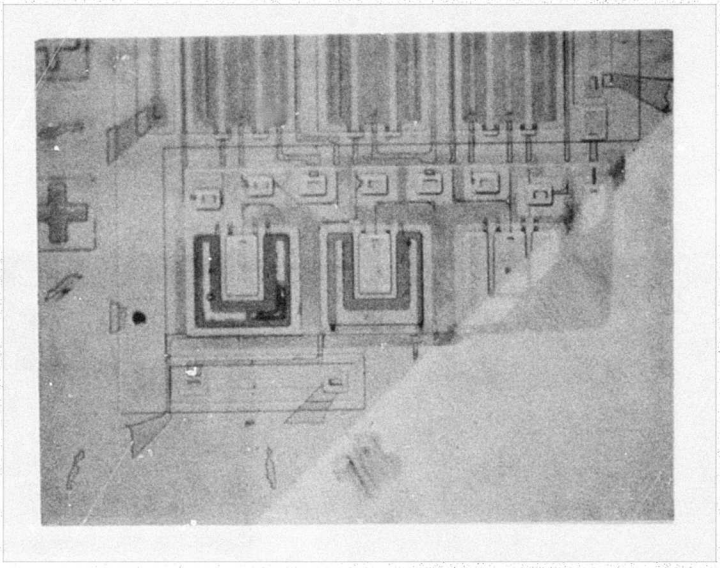
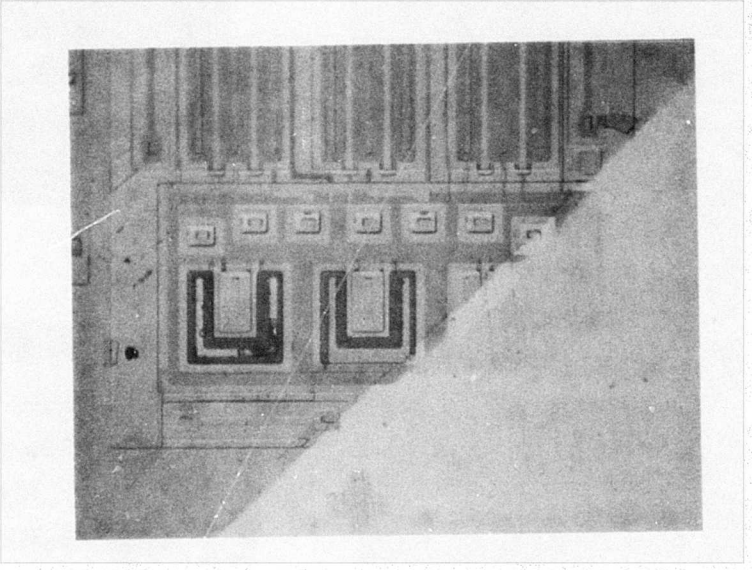


FIGURE 7
HYPOTHESIZED EXTRA CURRENT PATH



MAGNIFICATION 150X



MAGNIFICATION 150X
P-STAIN (DARK)

FIGURE 8
ANGLE LAP SECTION OF I 4007

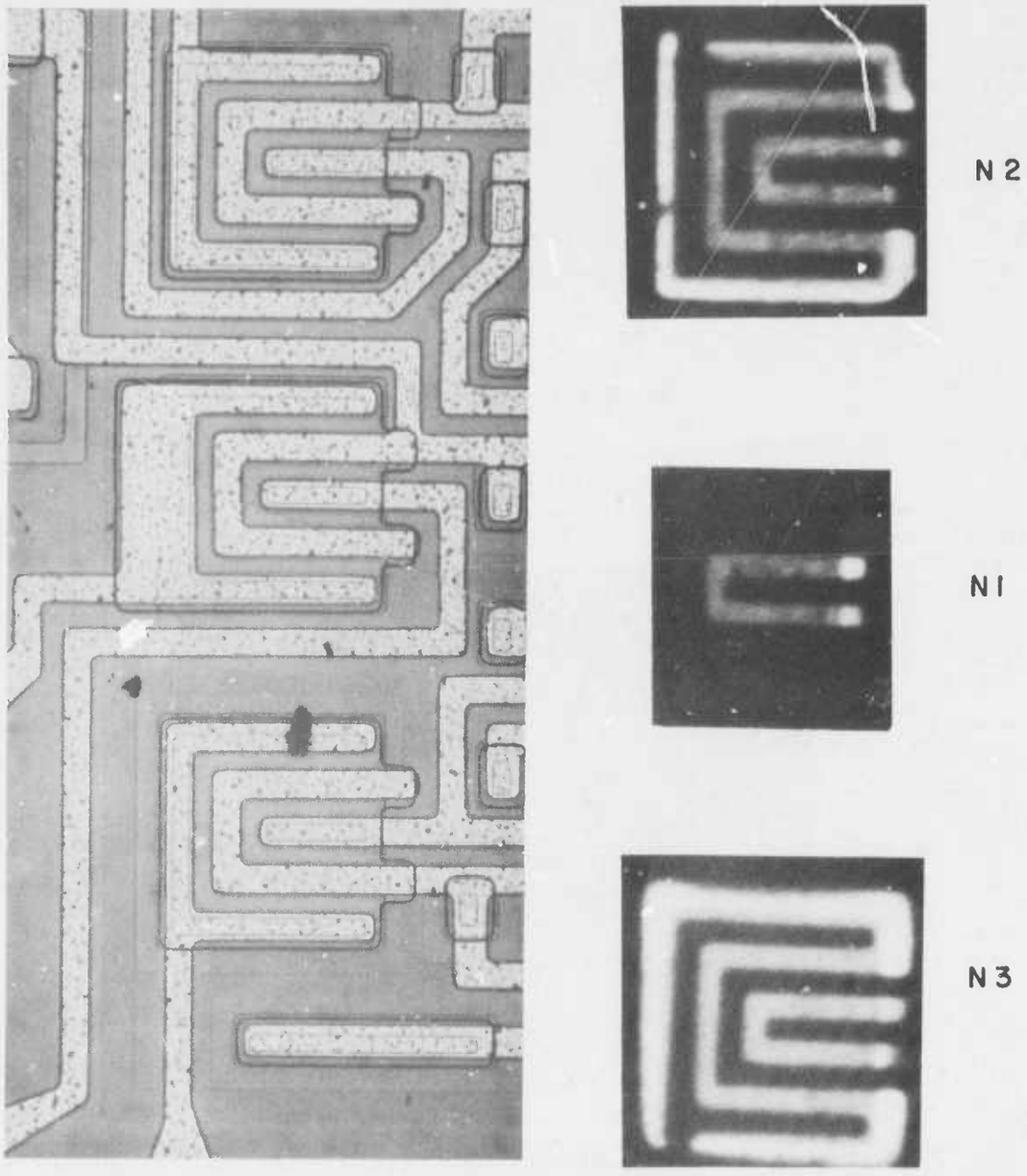


FIGURE 9
PHOTOSCAN OF I056, INITIAL SCAN

the N1 transistor turned on. The result is shown in Figure 10. Note the absence of the N1 response. This arose from the very high leakage between drain to source such that only very small photovoltages were generated. After 24 hours, the N1 units threshold voltage crossed 0 so that the unit was once again high impedance. The photocurrent generated now permitted observing the drain junction (see Figure 11). A comparison between this N1 response and the initial photoresponse shows no apparent inversion layer extending the drain region, yet the threshold voltage has shifted nearly 1.5 volts. It was tentatively concluded that no charge, whether on the surface or in the bulk outside the gate region, was responsible for either the initial threshold voltage behavior of N1 or its instability.

C. Electrical Measurements

The threshold voltage measurement circuit is shown in Figure 12. This measuring technique simply indicates the amount of gate voltage necessary to get 10 μA of current to flow out the source lead. While the measuring technique is extremely convenient, it is capable of being very misleading. For one thing, the source of the 10 μA current is undefined. Suppose for example there is a faulty drain to source protective diode as is shown in Figure 13. The leakage could in whole or in part be due to this faulty diode. If this were the case, then the voltage measured at the gate has little or no relationship to the threshold voltage of the transistor in question. Any current that does not originate from the operation of the transistor can cause significant "apparent" threshold voltage shifts with this instrumentation. While the stray leakage current effect is a concern for arriving at good threshold voltage measurements, it does serve as an indicator for stray non-transistor related leakage currents.

The ideal MOS transistor characteristic in the current saturated mode is governed by the relationship[2]

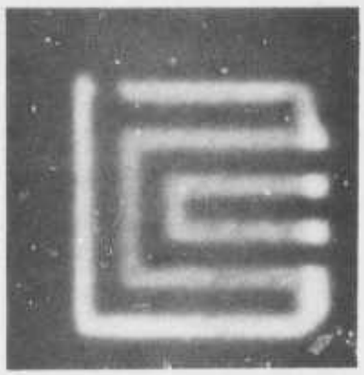
$$I_{DSAT} = \frac{Z}{2L} \mu_n c_i (V_G - V_T^1)^2$$

where Z = Channel Length
L = Channel Width
μ_n = Mobility of the Channel
c_i = Capacitance of the Insulator
V_G = Gate Voltage
V_T = Effective Threshold Voltage

It is clear then if the transistor we are measuring is ideal, a plot of the $\sqrt{I_{DSAT}}$ vs. V_G should produce a straight line whose slope is $\left(\frac{\sqrt{Z}\ \mu_n c_i}{2L}\right)^{\frac{1}{2}}$ and the $\sqrt{I_{DSAT}} = 0$ intercept gives the threshold voltage for that unit.

The effect of extra leakage current depends on the nature of that leakage current. For example, suppose the drain to source diode is conducting, this current is nearly independent of the gate to source voltage (See Figure 13). Experimentally then the extra current would serve as a constant (I_x) and the ideal equation would be transformed to

AFTER 5HRS., 15V N CHANNEL BIAS



N 2

NO PHOTORESPONSE POSSIBLE FROM NI DUE TO EXCESSIVE LEAKAGE CURRENT.

NI

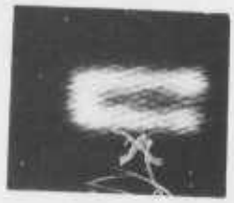
N 3

FIGURE 10
PHOTOSCAN OF I056, AFTER 5 HRS., 15 V N-CHANNEL

AFTER 24 HRS AT ROOM TEMP

RECOVERY ANALYSIS

N2



N1

N3

THIS RESPONSE TAKEN AT MOMENT OF $V_{THRESHOLD}$ CROSSING 0 VOLTS PERMITTING LOOK AT N1 DURING RECOVERY. THERE IS STILL A SUBSTANTIAL RECOVERY PERIOD TO FOLLOW.

FIGURE 11
PHOTOSCAN OF I056, AFTER 24 HRS. AT ROOM TEMPERATURE

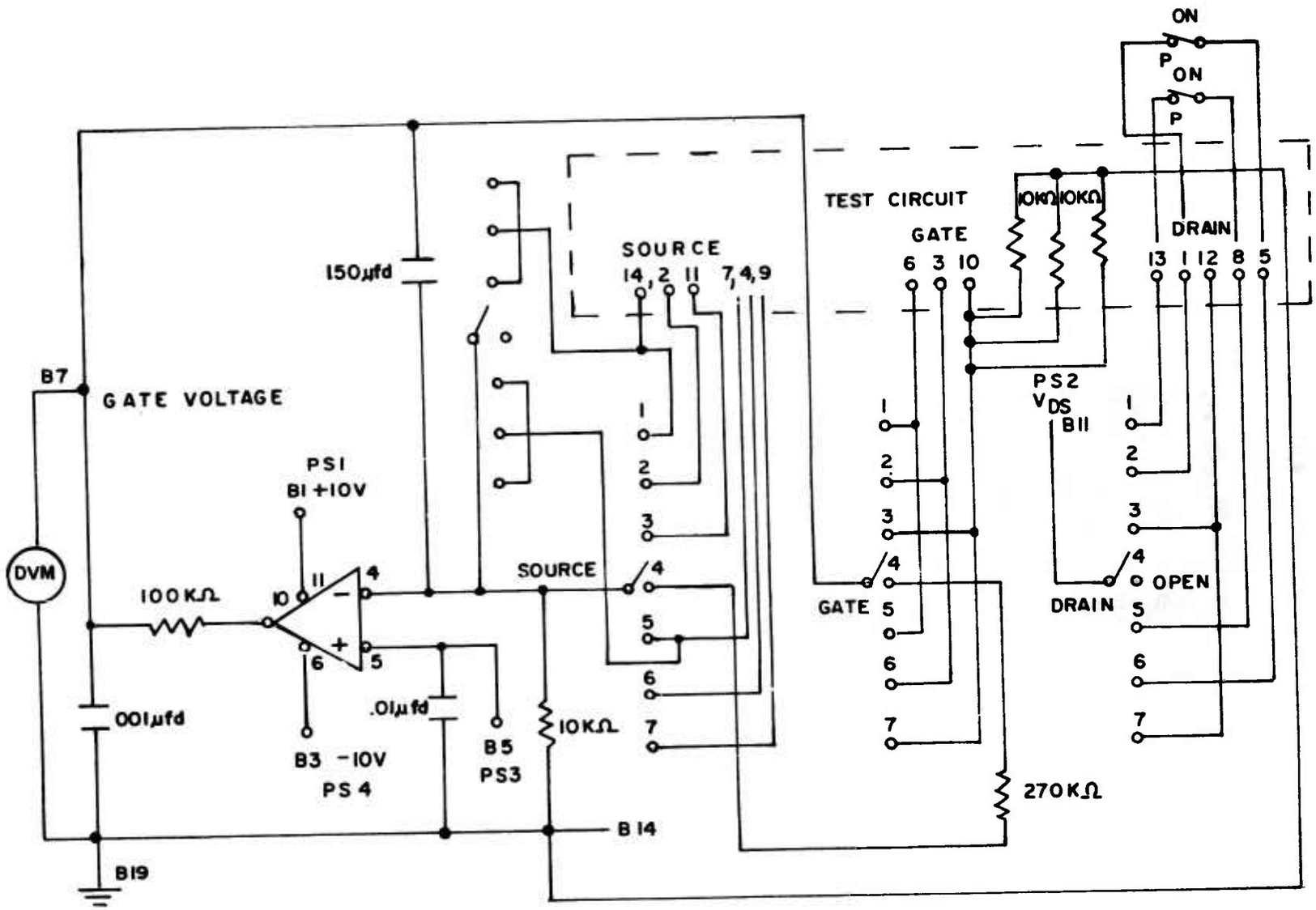


FIGURE 12
THRESHOLD TEST CIRCUIT

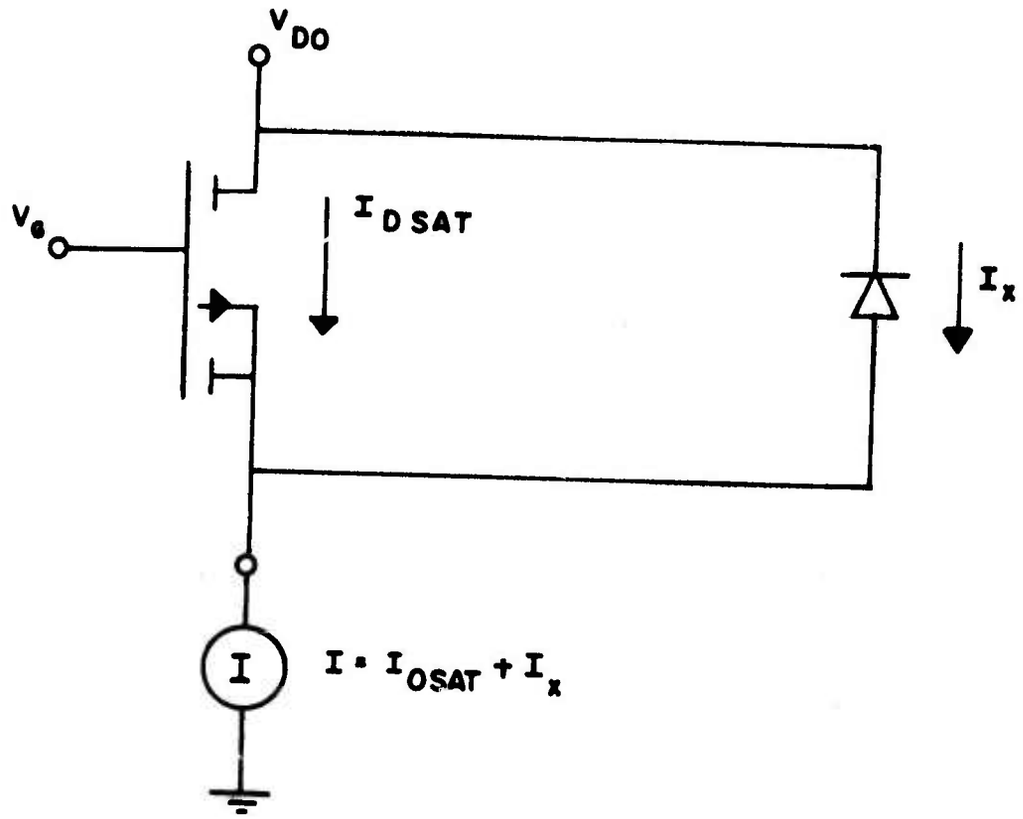


FIGURE 13
EXTRA LEAKAGE CURRENT EFFECT ON $\sqrt{I_{DS}}$ AS A FUNCTION OF GATE VOLTAGE

$$\sqrt{I_{DSAT}} = \left(\sqrt{Z}\,\frac{\mu_n C_i}{2L}\right)^{\frac{1}{2}} (V_G - V_T^1) + \sqrt{I_x}$$

For the condition $\left(\sqrt{Z}\,\frac{\mu_n C_i}{2L}\right)^{\frac{1}{2}} (V_G - V_T^1) < \sqrt{I_x}$

the equation would be $(I_{DSAT})^{\frac{1}{2}} = (I_x)^{\frac{1}{2}}$

A plot then of $\sqrt{I_{DSAT}}$ vs. V_G would not be linear at or near the threshold voltage. One would expect a curve as shown in Figure 14.

Thus if there is a true shift in the threshold voltage due to stored charge in the oxide, one would expect a simple translation of the ideal curve. If on the other hand, there were additional leakage paths such as that suggested, some curvature in the $\sqrt{I_{DSAT}}$ vs. V_G could be expected.

To test whether the shift in threshold observed was simply misinterpretation of the threshold measuring technique, a group of 5 devices were subjected to temperature biased testing at 75°C and 10 volts between gate to source on the N1 device. Figure 15 shows the results of that testing as a function of time on test (note the time is in seconds). The figure shows the average gate voltage necessary to drive the appropriate current with 10 volts drain to source. The error bars are the mean deviation about the average.

The electrical measurements suggest two points. First, the conclusion regarding threshold voltage shifts from the 10 μA measurement scheme is completely justified. Second, because there is no measurable curvature in the $\sqrt{I_{DSAT}}$ vs. V_G in the initial curve, the low threshold voltage is due to the nature of the charge within the insulator directly beneath the gate electrode. For devices which have been temperature biased there is some evidence of extra leakage current being generated but the overriding effect is again due to a true threshold voltage shift.

In summary then, based upon the negative results of photoscan, visual inspection, and lap and stain for the three n channel transistors and the positive result of little or no curvature in the $\sqrt{I_{DSAT}}$ vs. V_G curve it is a safe conclusion the failures observed from N1 were not due to contamination of the oxide in any region other than directly beneath the gate metallization. There are no inverted regions other than directly beneath the gate metallization which could provide the anomolous electrical behavior of the N1 transistor as compared to the N2 and N3 transistors. This stage of the failure analysis concluded that the initially low threshold voltage and unstable nature of the N1 MOS transistor was due to a changing threshold voltage in the insulator directly beneath the gate metallization.

D. Threshold Voltage Instability

The next stage of the failure analysis was devoted to characterizing the instability in N1. It was apparent that the behavior of the threshold voltage

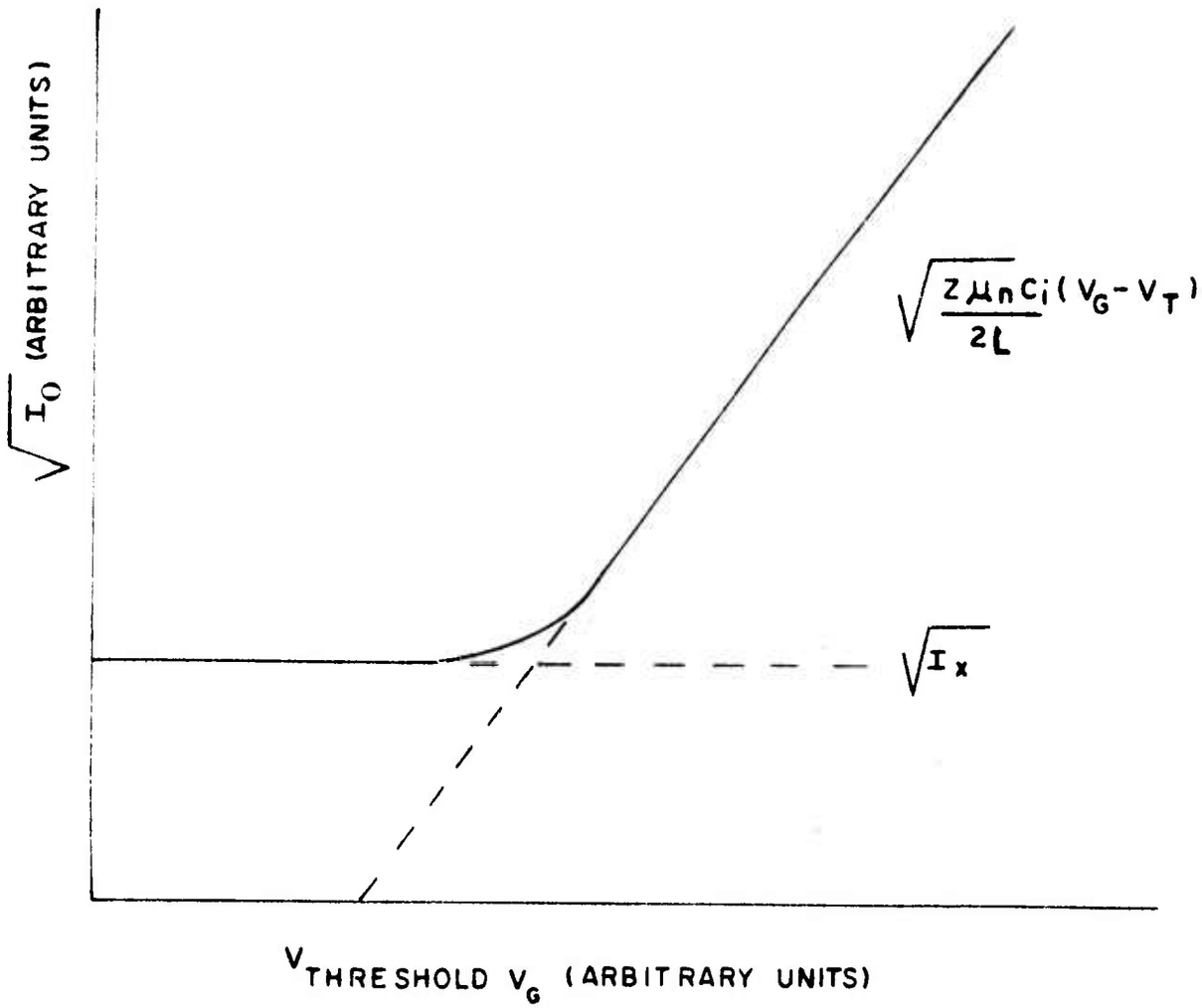


FIGURE 14
$\sqrt{I_O}$ VS. GATE VOLTAGE

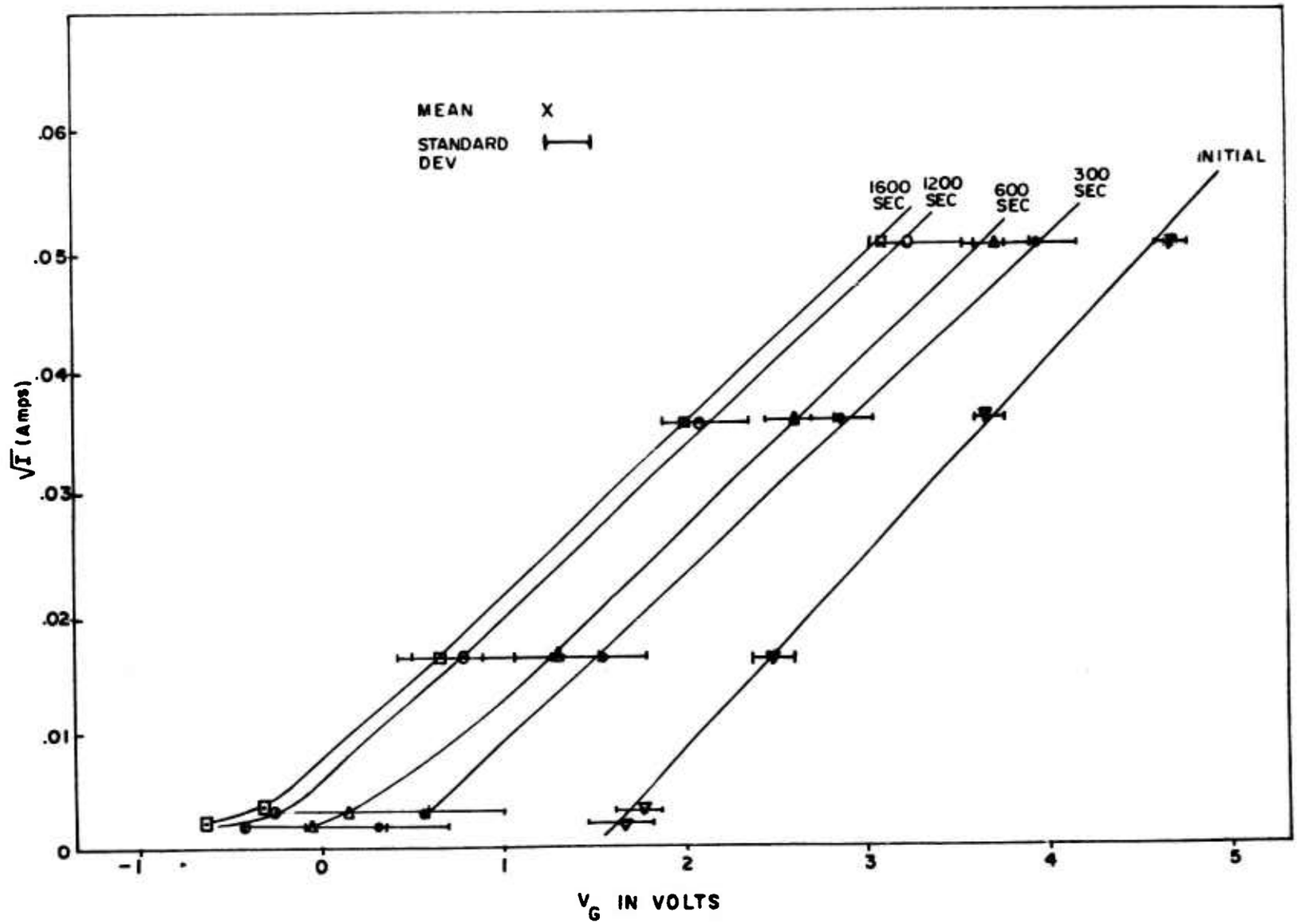


FIGURE 15
$\sqrt{I_{DS}}$ AS A FUNCTION OF V_G WITH TIME UNDER BIAS

was temperature sensitive. Generally, temperature dependence comes from the populating or depopulating of surface states at the oxide-silicon interface. The rate of change in the density of occupied trapping sites (n_t) can be expressed as the difference between the rate of filling and emptying those trap sites.

The rate of filling the traps is dependent on the $\bar{v}$ (velocity) of the mobile carriers and the capture cross section σ_n of the traps. A mobile charge sweeps out a volume $\bar{v}\sigma_n$ per second of possible recombination. If the density of filled traps is n_t, then the density of empty traps is $(N_t - n_t)$, where N_t is Density of trap sites. The rate at which conduction carriers recombine with traps is $\bar{v}\sigma_n(N_t-n_t)n_c$ where n_c is the density of conduction carriers.

The interaction of the trapping centers with the crystal lattice releases carriers from the traps at a rate proportional to their number. The rate of release is $\bar{v}\sigma_n n_t n_1$, where n_1 is the sites in the conduction band available for filling and is given by

$$n_1 = N_c \exp \frac{(-E_t)}{kT}$$

where Nc = Effective density of states in the conduction band.

Equation [1] describes the net rate of change of trapped carriers.

$$\frac{dn_t}{dt} = \bar{v}\sigma_n (N_t-n_t)n_c - \bar{v}\sigma_n n_t N_c \exp \frac{(-E_t)}{kT} \qquad [1]$$

For the case of the n channel transistor, the n_c term is very small and the rate of filling is small compared to emptying the traps. Note that as the traps fill, an inversion layer may form tending to increase n_c and the approximation may not be valid. Initially, for the N1 transistor the rate of trap depopulating can be expressed as

$$\frac{dn_t}{dt} = \bar{v}\sigma_n n_t N_c \exp \frac{(-E_t)}{kT} \qquad [2]$$

Integrating we get $\ln n_{t1} - \ln n_{t0} = \bar{v}\sigma_n N_c \exp \frac{(-E_t)}{kT} \Delta t$

where the boundary condition $n_t = n_{t0}$ at $t = 0$, $n_t = n_{t1}$ at $t = t$ is assumed.

The threshold voltage is related to n_t by the expression

$$V_{th}^{o} = \frac{+q\bar{x}_o n_o}{c_i}$$

Note that all the traps are assumed to exist a distance $\bar{x}_o$ in the insulator from the silicon.

Then $\ell n \left(\frac{+C_i}{q\bar{x}} V_{th}^{1} \right) - \ell n \left(\frac{+C_i}{q\bar{x}} V_{th}^{o} \right) = \bar{v}\sigma_n N_c \exp \left(\frac{-E_t}{kT} \right) \Delta t$

This reduces to

$$\frac{\Delta \ell n \, V_{th}}{\Delta t} = A \exp \frac{(-E_t)}{kT} \qquad [3]$$

Thus for a fixed temperature, the $\ell n \, V_{th}$ vs. time should plot a straight line.

Data was taken on device 077 to generate such a curve for three different temperatures, i.e., 75°C, 100°C and 125°C. The device has a 10 volt gate to source bias applied with the drain floating. After so many seconds, the device was removed with bias still applied and allowed to cool down. Threshold voltage as defined by the 10 μA leakage specification was taken and is shown in Table XVI.

A plot of this data is shown in Figure 16 and replotted as theory suggests in Figure 17. As can be seen, while the experimental error bars are large we do appear to be justified in the assumption that trap filling is negligible and that depopulation of trapping sites is occurring.

Now by taking the log of both sides of [3] an estimate of the activation energy for trap depopulation can be obtained.

$$E_t = -k \frac{\Delta \ell n \left(\frac{\Delta \ell n \, V_{th}}{\Delta t} \right)}{\Delta \left(\frac{1}{T} \right)}$$

A plot of the slopes in Figure 16 is shown in Figure 18 (denoted by x) as a function of reciprocal temperature in °K. The activation energy can be seen to be increasing with increasing temperature. This maybe a consequence of a distribution in energy of the trap sites. Notice at the lower temperatures the trap energy is relatively low, i.e., 0.32 ev. This is a clue as to the identity of the species and will be discussed later.

Having examined the behavior of the threshold voltage (V_{th}) at a fixed applied voltage as a function of temperature, it was necessary to characterize V_{th} as a function of applied voltage. A collection of CMOS inverters were placed under varying gate biases at room temperature and their V_{th} was monitored. The raw data is given in Table XVII and the results are shown in Figure 19 and replotted in Figure 20 on log-log paper. These results suggested a square root dependence in time and a strong function of $V_{applied}$. The $t^{\frac{1}{2}}$ dependence suggested a field enhanced diffusion mechanism which can be characterized by

$$\Delta V_{th} = 2\sqrt{\frac{R}{C}} g_s \left(\frac{t^{\frac{1}{2}}}{\sqrt{\pi}} - \frac{X\sqrt{RC}}{2} \right) \qquad [4]$$

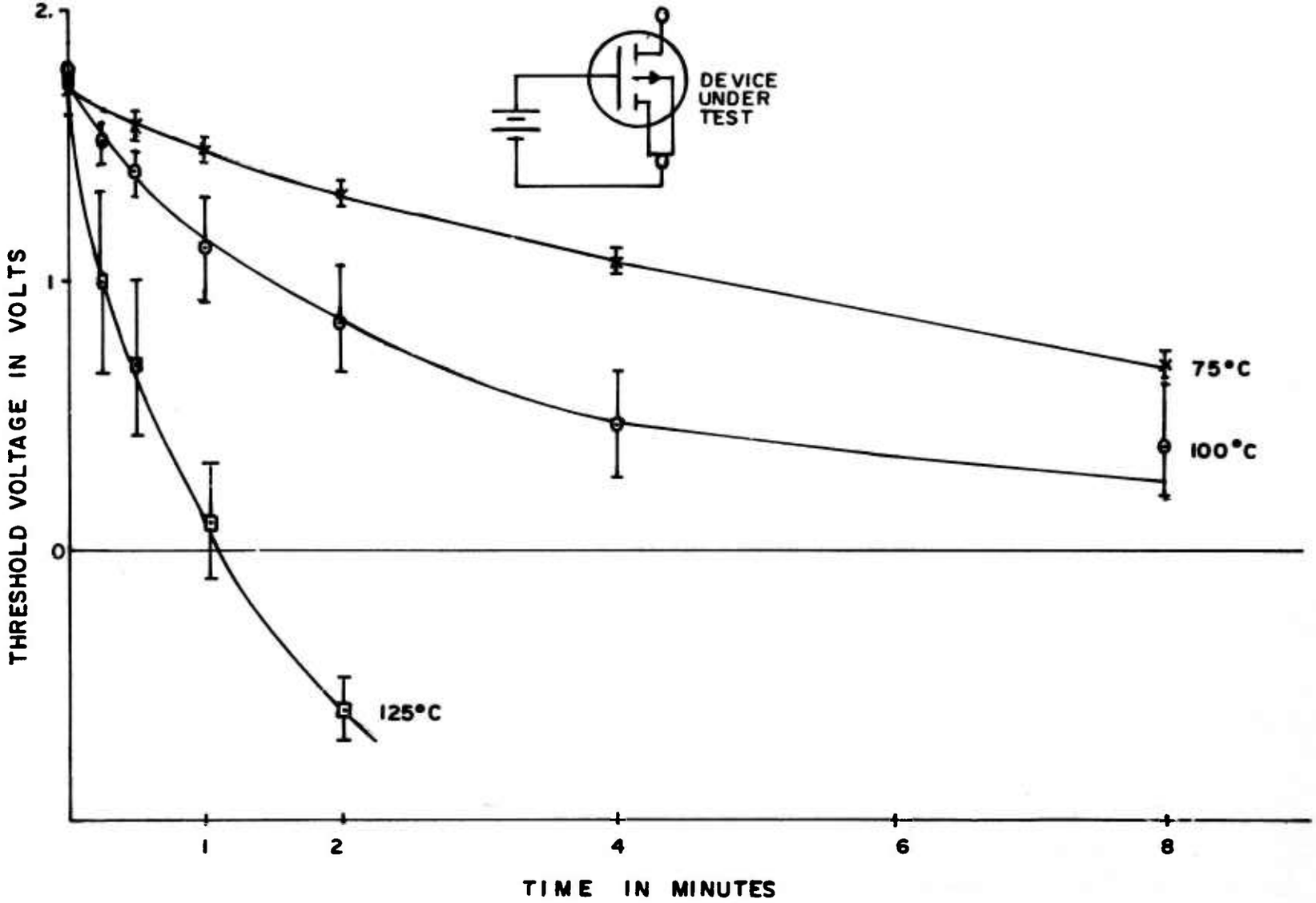


FIGURE 16
ACTIVATION ENERGY EXPERIMENT

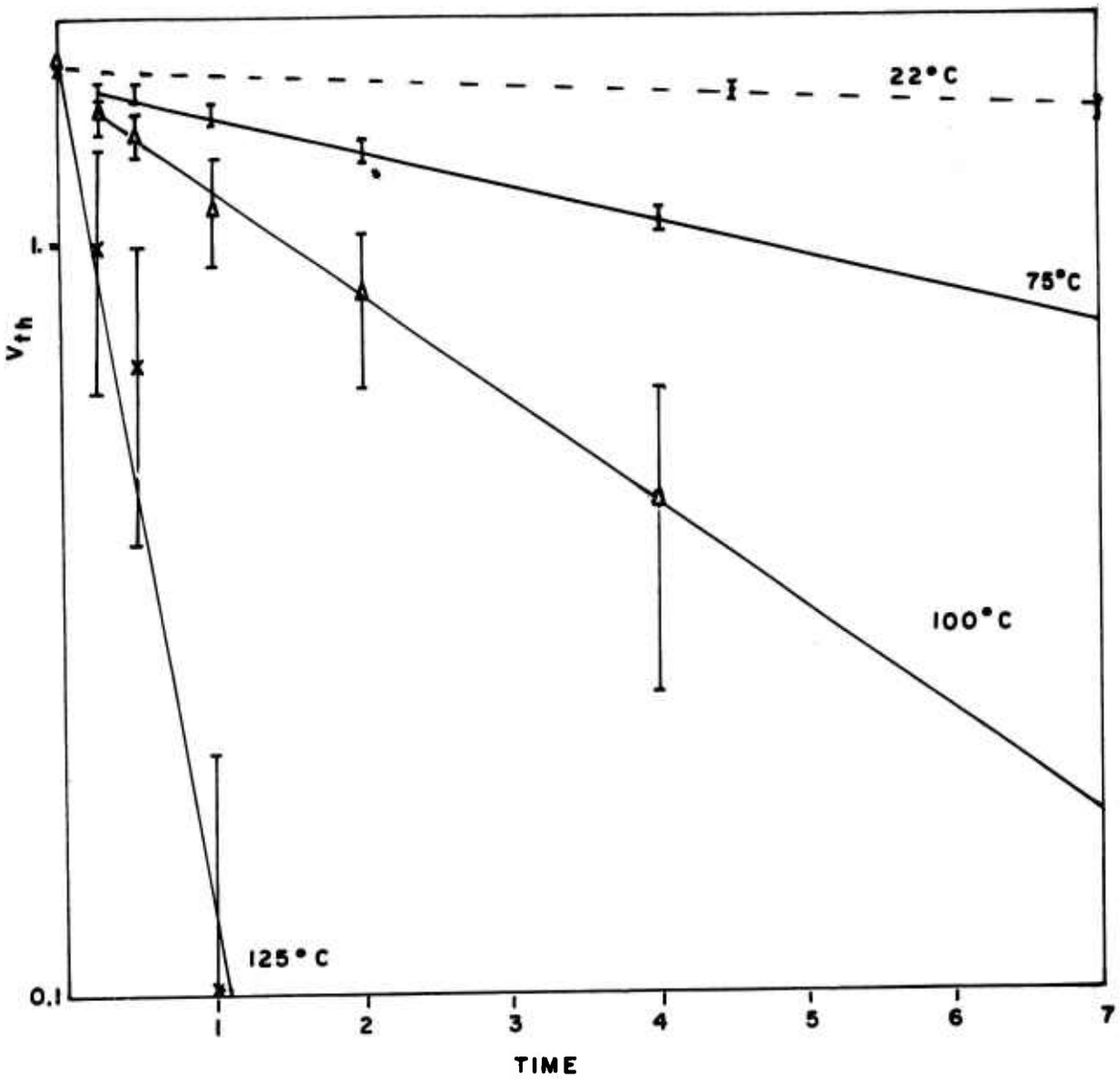


FIGURE 17
THRESHOLD VOLTAGE DEGRADATION AT 10 VOLTS
GATE SUBSTRATE AS A FUNCTION OF TIME IN MINUTES

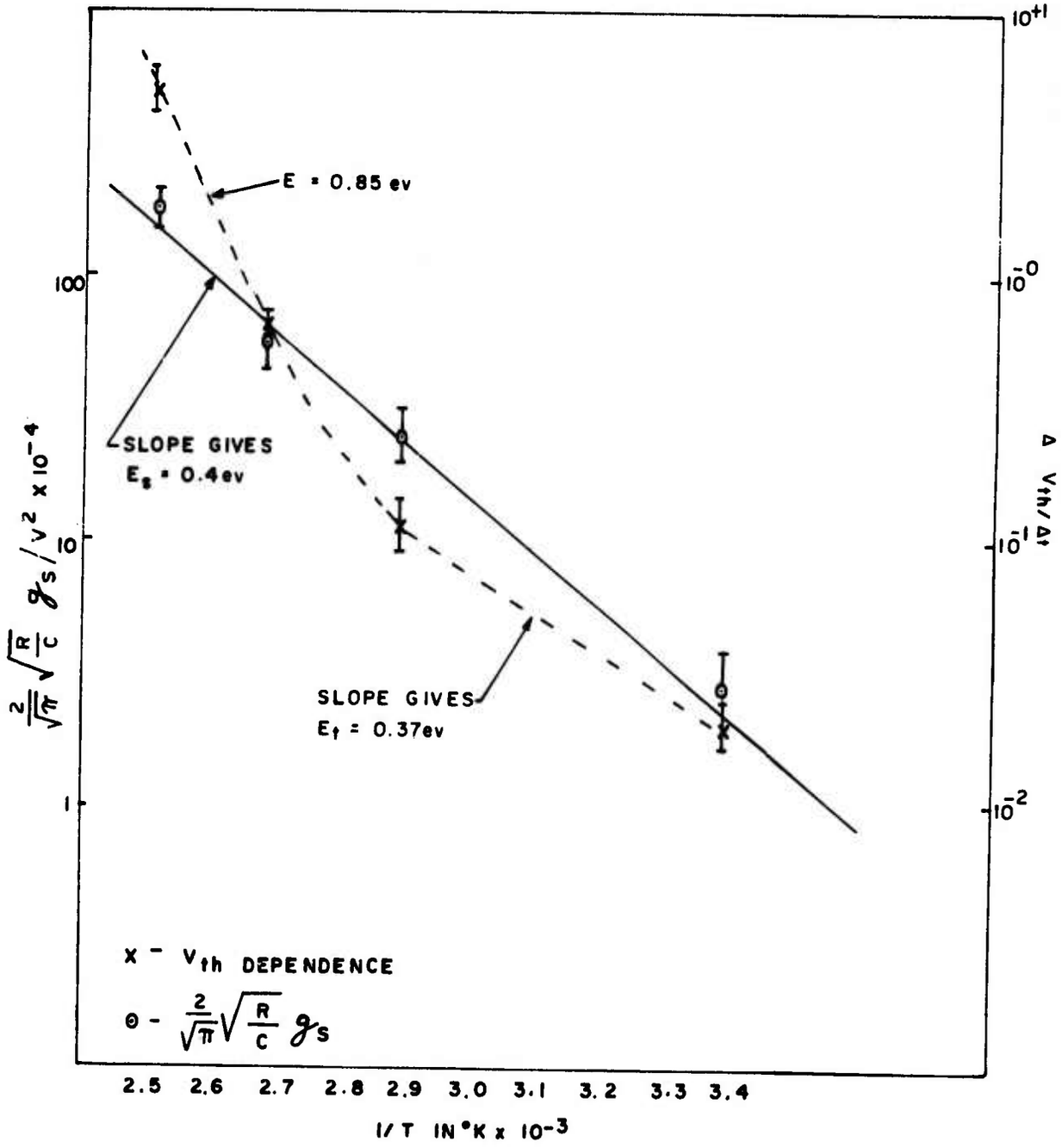


FIGURE 18

TEMPERATURE DEPENDENCE OF $\frac{2}{\sqrt{\pi}}\sqrt{\frac{R}{C}}\,g_s$ AND THRESHOLD VOLTAGE

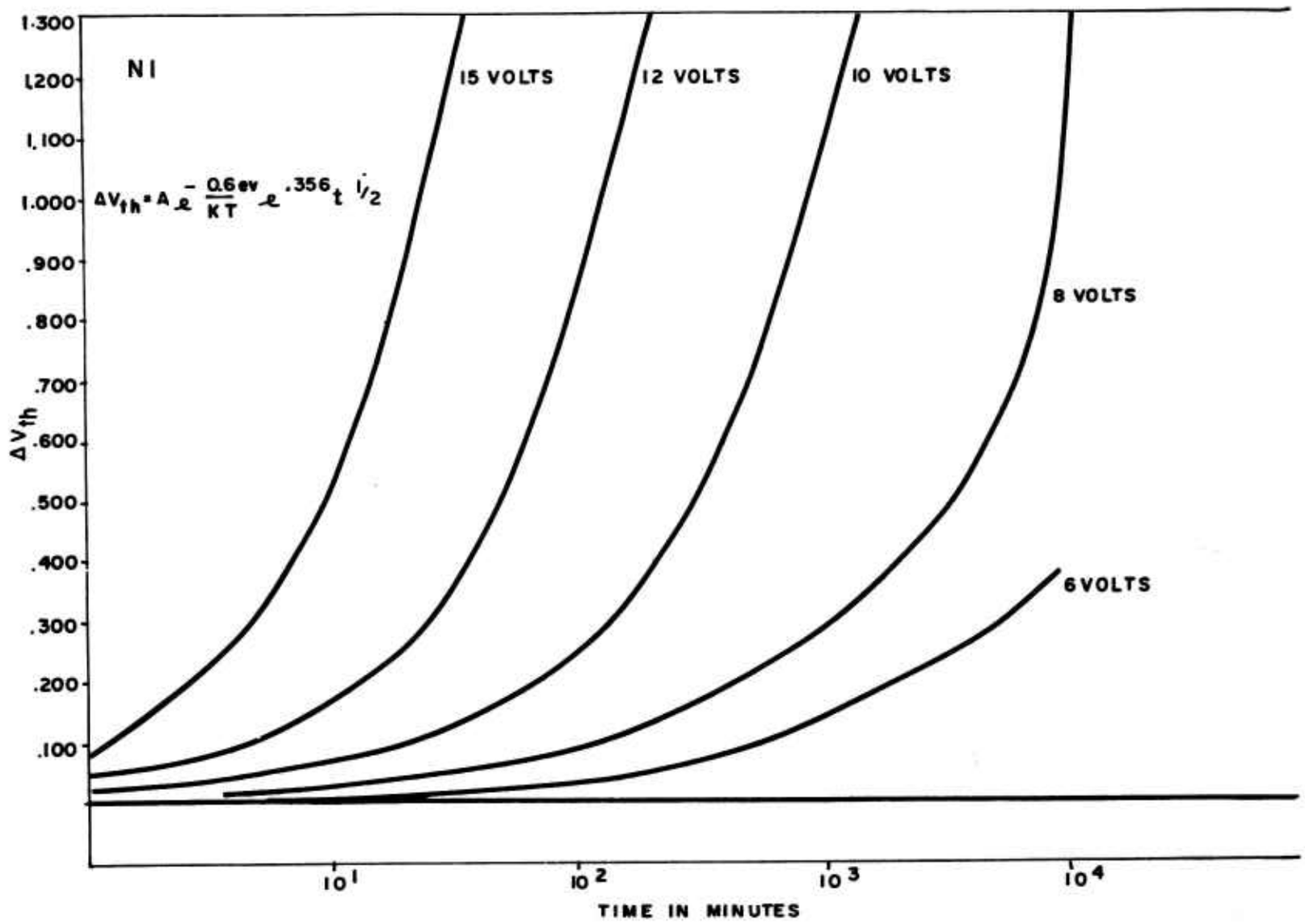


FIGURE 19
CHANGE IN THRESHOLD VOLTAGE AS A FUNCTION OF TIME AND BIAS

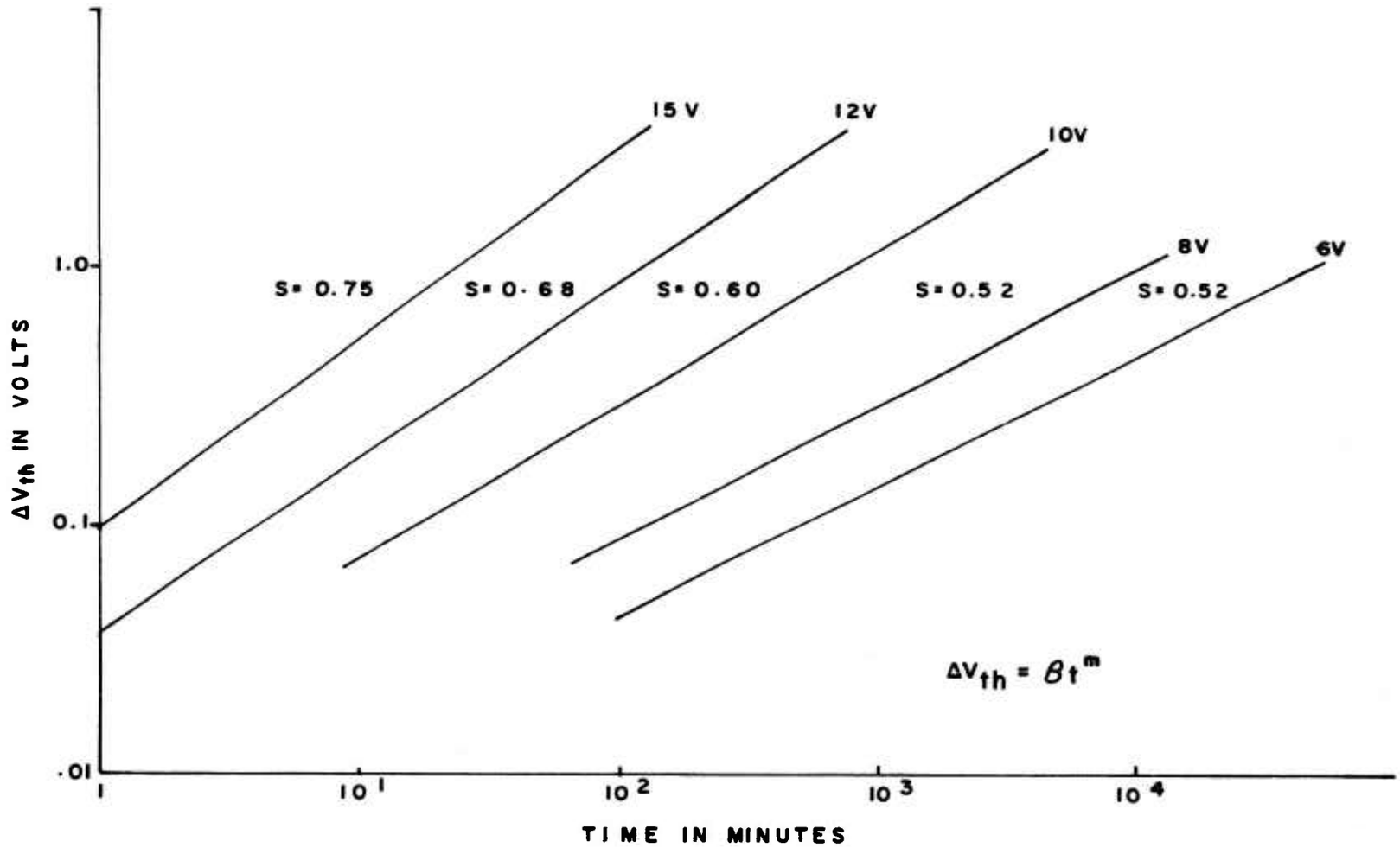


FIGURE 20
CHANGE IN THRESHOLD VOLTAGE AS A FUNCTION OF TIME AND BIAS

Table XVI

10 Volts Gate to Source

Time Under Bias	T = 75°C		T = 100°C		T = 125°C	
	V_{th} N1 (±3%)	V_{th} N2 (±1%)	V_{th} N1 (±3%)	V_{th} N2 (±1%)	V_{th} N1 (±3%)	V_{th} N2 (±1%)
0	1.71	3.34	1.78	3.34	1.7	
15	1.62	3.33	1.52	3.43	0.99	
30	1.58	3.33	1.41	3.41	0.69	
60	1.49	3.32	1.13	3.37	0.01	
120	1.325	3.30	0.86	3.32	-0.58	
240	1.08	3.27	0.46	3.09		
480	0.68	3.21	0.39	2.25		
960	0.16	3.12				
1920	-0.15	2.96				

Table XVII

6 Volts, Device #014, Room Temperature

Initial	2.350	2.350	2.350	2.294	2.294	2.294	2.294
Final		2.328	2.307	2.015	1.988	1.925	1.921
ΔV_{th}		.022	.043	.279	.306	.369	.373
Time	0	100	200	4520	5960	7700	9140
$t^{\frac{1}{2}}$		10	14.14	67.23	77.20	87.75	95.6

8 Volts, Device #015, Room Temperature

Initial	2.430	2.430	2.430	2.317	2.317	2.317	2.317
Final		2.367	2.311	1.738	1.659	1.432	1.462
ΔV_{th}		.063	.119	.579	.658	.885	.855
Time	0	100	200	4520	5960	7700	9140
$t^{\frac{1}{2}}$		10	14.14	67.23	77.20	87.75	95.6

10 Volts, Device #016, Room Temperature

Initial	2.032	2.032	2.032	2.032	2.032	1.798	1.798
Final		1.932	1.852	1.776	1.624	.426	.359
ΔV_{th}		.100	.180	.256	.408	1.372	1.439
Time	0	20	50	100	200	4520	5960
$t^{\frac{1}{2}}$		4.47	7.07	10	14.14	67.23	77.20

12 Volts, Device #069, Room Temperature

Initial	1.851	1.851	1.851	1.851	1.851	1.851	1.851
Final		1.805	1.747	1.689	1.597	1.340	1.010
ΔV_{th}		.046	.104	.162	.254	.511	.841
Time	0	2	5	10	20	50	100
$t^{\frac{1}{2}}$		1.41	2.25	3.16	4.47	7.07	10

15 Volts, Device #069, Room Temperature

Initial	1.807	1.807	1.807	1.807	1.807	1.807	1.807
Final		1.650	1.488	1.266	.932	.302	- .323
ΔV_{th}		.157	.319	.541	.875	1.505	2.130
Time	0	2	5	10	20	50	100
$t^{\frac{1}{2}}$		1.41	2.25	3.16	4.47	7.07	10

Where R = Insulator Resistance/Unit Distance
C = Capacitance/Unit Area
g_s = Rate of Charge Generation at Source

See Appendix A for derivation.

Equation 4 suggests that if a plot of the threshold voltage shift, i.e., ΔV_{th} (which is simply a reflection of V(x,t)) as a function of $t^{\frac{1}{2}}$ were made straight lines should be generated whose slope is $2g_s\sqrt{\frac{R}{\pi C}}$ and zero intercept in the $t^{\frac{1}{2}}$ region is $-Rg_sX$.

The change in threshold voltage (equivalent to V(x,t) in equation 4) was then plotted as the square root of time in minutes for the various voltages. The results are shown in Figure 21. As can be seen, the fit to $t^{\frac{1}{2}}$ is very close for low applied voltage levels. The fit is not as good at the higher voltages for longer times. Note the extrapolation to t = 0 is clearly not valid because at $t << \frac{x^2}{4\alpha}$ in Equation 9, Appendix A, V(x,t) approaches 0. However, with the approximation used to arrive at Equation 4 we have assumed the time of the measurement is large and, therefore, Equation 4 is forced to fit our data. Under these conditions, Equation 4 predicts a negative intercept as can be seen in Figure 21. Since it is expected that g_s, the charge generating source at the surface of the insulator, is voltage dependent, we see that not only is the slope voltage dependent but also the intercept as Equation 4 predicts.

Now letting x_0, the location of accumulated charge in the insulator be independent of the applied voltage, an examination of g_s as a function of voltage can be accomplished.

At room temperature, $2g_s\sqrt{\frac{R}{\pi C}}$ was calculated by simply taking the slope of each of the applied voltage lines in Figure 21. At higher temperatures $2g_s\sqrt{\frac{R}{\pi C}}$ can be calculated from Figures 22 and 23 where ΔV_{th} is plotted as a function of V applied for a constant time interval (namely, 120 seconds). The term $2g_s\sqrt{\frac{R}{\pi C}}$ in these curves is simply $\Delta V_{th}/(2\ \text{min})^{1/2}$ at each V applied.

The results for g_s as a function of V applied are given in Table XVIII.

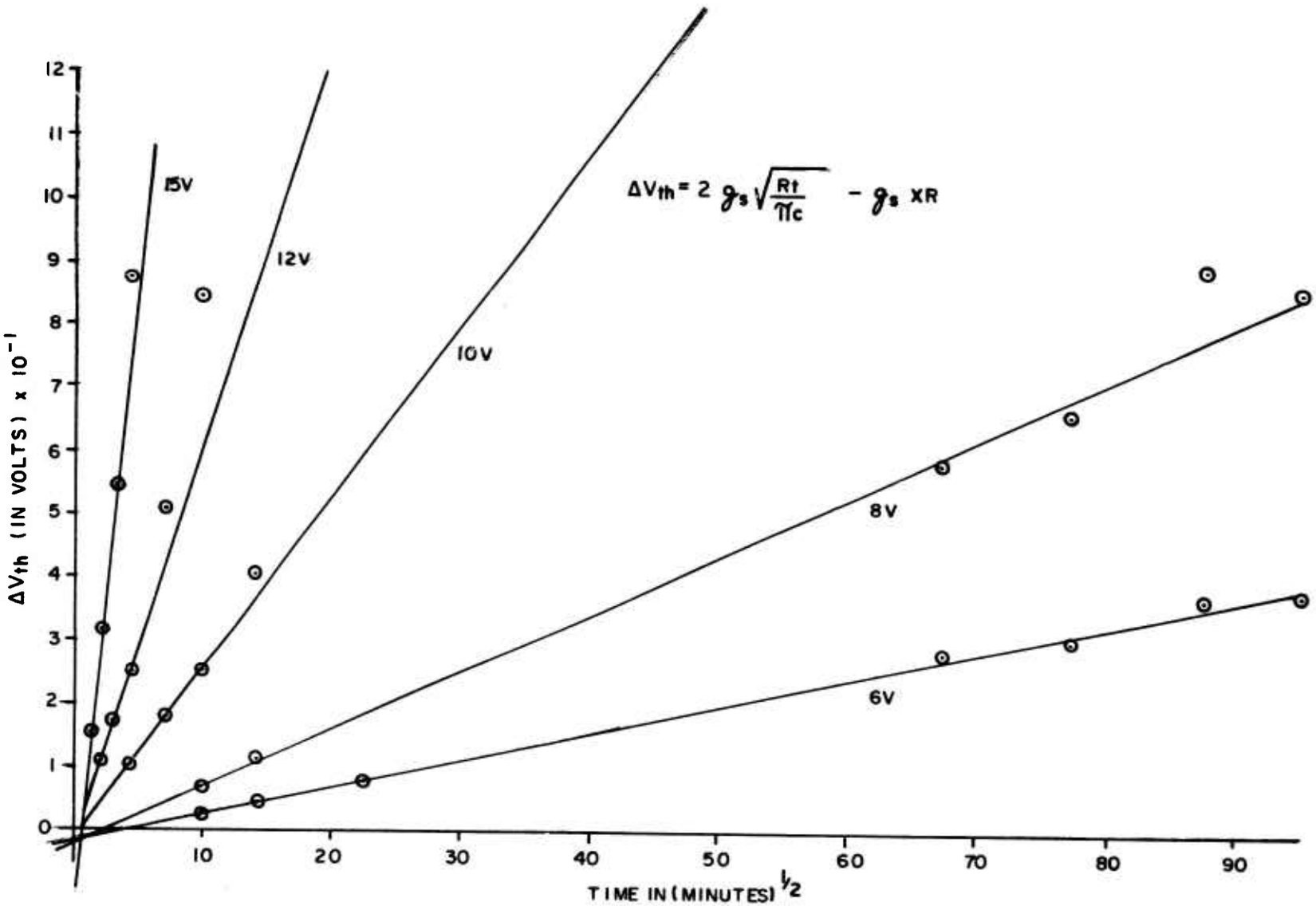


FIGURE 21
THRESHOLD VOLTAGE SHIFT AS A FUNCTION OF
TIME AND BIAS AT ROOM TEMPERATURE

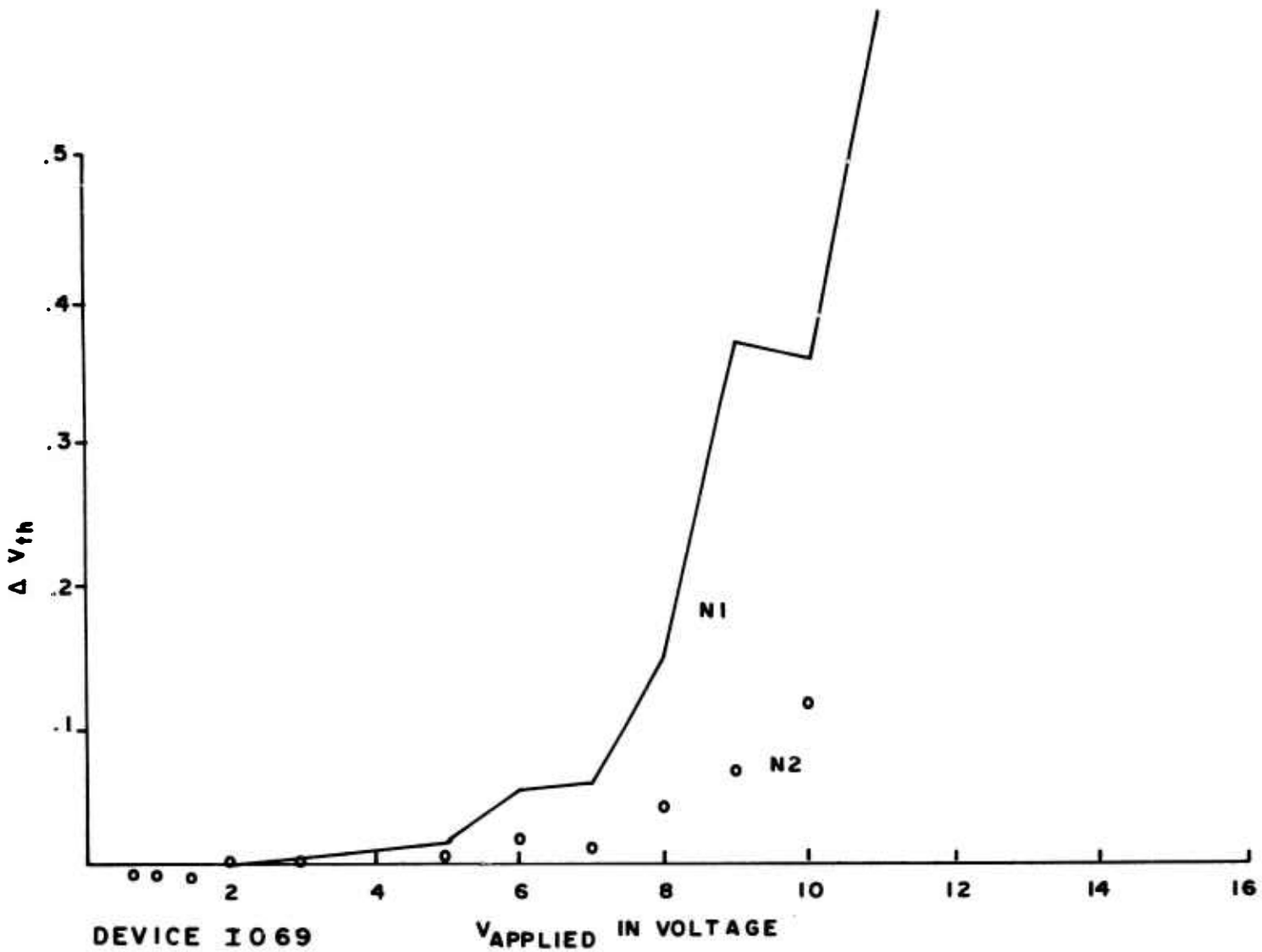


FIGURE 22
VOLTACE DEPENDENCE OF V_{th} AT
75°C WITH V_A FOR 120 SEC.

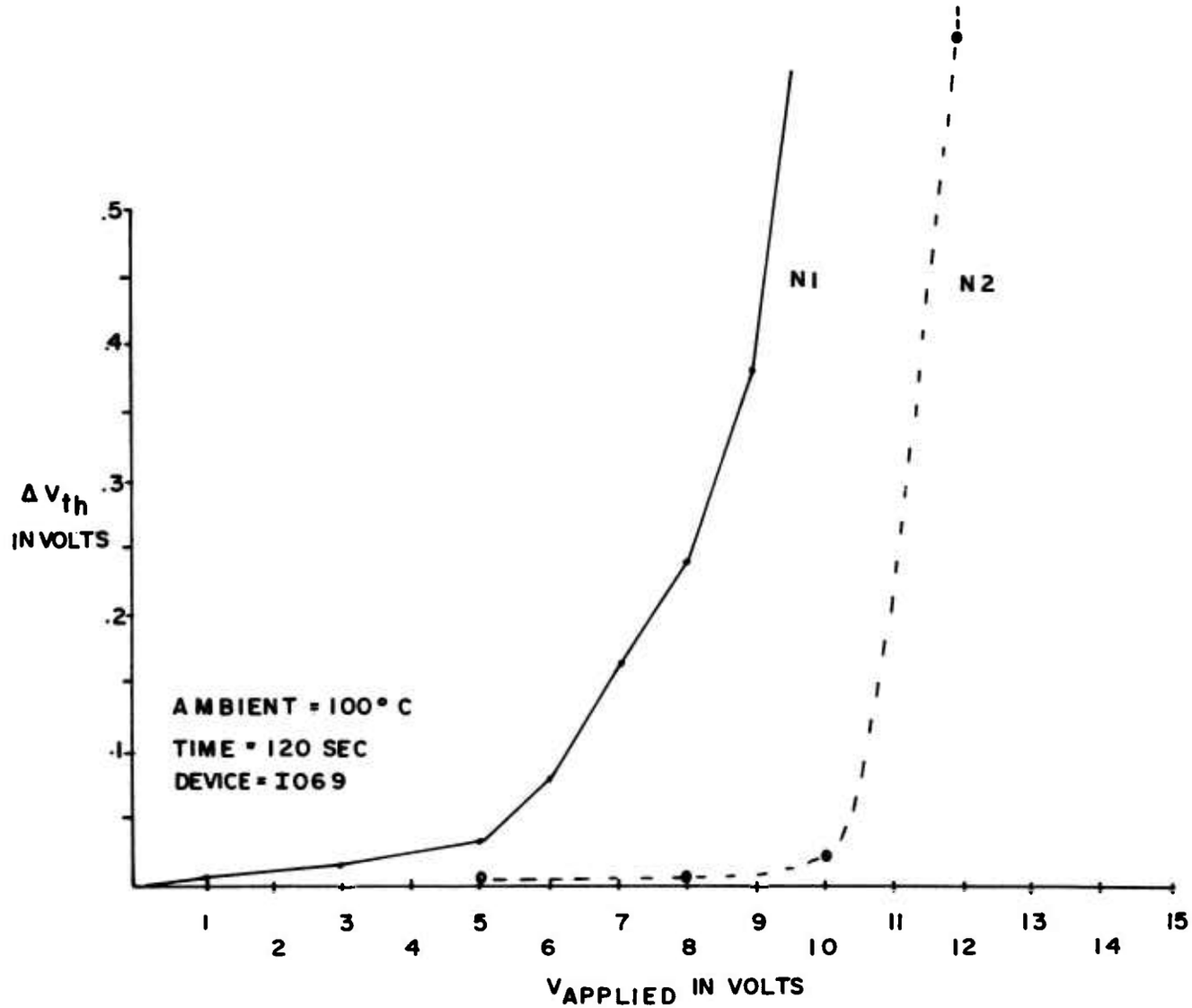


FIGURE 23
CHANGE IN THRESHOLD VOLTAGE AS A FUNCTION OF $V_{APPLIED}$

Table XVIII

Rm. Temp.		75°C		100°C	
V(volts) Applied	$2\sqrt{\frac{R}{C}}\, g_s$	V Applied	$2\sqrt{\frac{R}{C}}\, g_s$	V Applied	$2\sqrt{\frac{R}{C}}\, g_s$
	x 10^{-2}		x 10^{-2}		x 10^{-2}
				4	1.49
		5	1.41	5	2.12
6	.426	6	2.83	6	5.66
		7	4.24	7	11.32
8	.810	8	9.90	8	16.27
		9	17.68	9	26.17
10	2.81	10	25.46	10	55.87
12	6.85			12	159.12
15	19.61	15	157.71	15	177.51

A tunneling mechanism for the current (i.e., g_s) is suspected. Tunneling I - V characteristics (assuming a Fowler-Nordheim triangular barrier) are typically of the form

$$I = BV^2\, e^{-b/v} \qquad [5]$$

If this is true, then dividing

$$2\sqrt{\frac{R}{C}}\, g_s \quad \text{by} \quad V^2_{applied}$$

and plotting this versus $\frac{1}{V_a}$ should produce a straight line on semi-log paper. Table XVIII was manipulated in this fashion and the results shown in Figure 24. There is a very clear saturation at the low applied voltages implying a V^2 dependence in addition to a postulated tunneling mechanism so that $2\sqrt{\frac{R}{C}}\, g_s$ takes the form

$$2\sqrt{\frac{R}{C}}\, g_s = AV^2 + BV^2\, e^{-b/v}$$

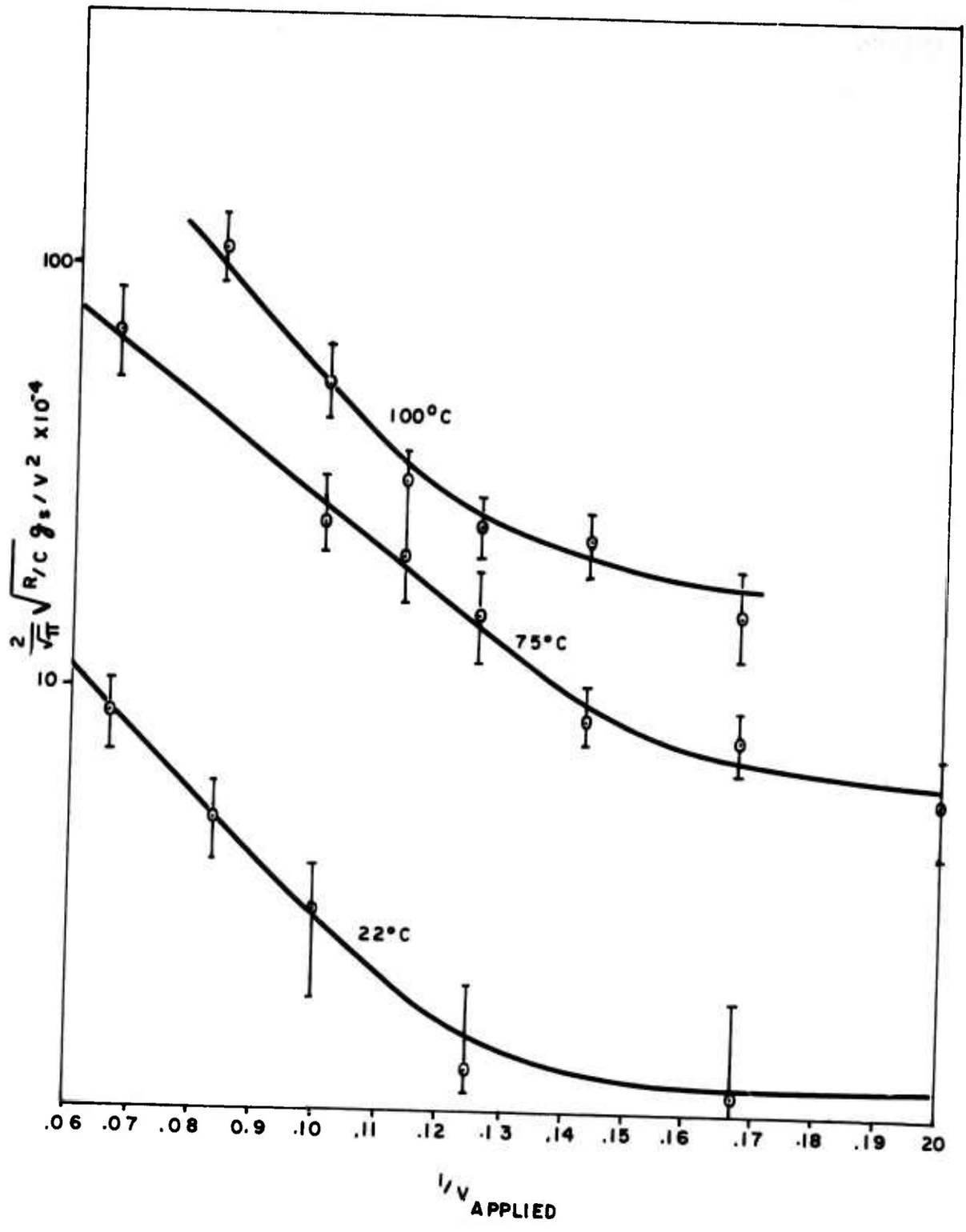


FIGURE 24

$\frac{2}{\sqrt{\pi}}\sqrt{\frac{R}{C}}\ g_s$ AS A FUNCTION OF APPLIED STATIC BIAS VOLTAGE

The change in the threshold voltage is then completely characterized by the equation

$$\Delta V_{th} = \{AV^2 + BV^2 e^{-b/v}\} e^{-E_s/KT} t^{\frac{1}{2}} + CV_{th} e^{-E_t/KT} t$$

The second term comes from our previous discussion of trap charge population as a function of temperature shown in Figure 18. If we labor under the assumption of tunneling, the AV^2 term has the form of a space charge limited current mechanism. The term $e^{-E_s/KT}$ comes from the assumption that the source of the charges is exponentially temperature dependent. The temperature dependence is also shown in Figure 18.

Comparing the two temperature dependence reveals that the activation energy seen at low temperatures for the threshold voltage is simply that of the source of the charges. Whereas, at higher temperatures we may be observing the energy level of the traps at the Si-SiO_2 interface or deeper energy level traps within the insulator.

The analysis leads to the following model. To begin with, the insulator contains some positive charges probably evenly distributed spacially. Thermal generation of electron-hole pairs are in balance with recombination. At the instant of applied positive voltage on the gate positive charges begin to migrate to the SiO_2-Si interface. The resultant space charge alters the field within the insulator inhibiting further positive charge accumulation at that interface. This gives rise to a space charge limiting dependence on voltage for the threshold voltage at low voltages. At any fixed low voltage, the rate at which the positive charge accumulates will behave under a field enhanced diffusion mechanism modulated by the creation of thermally generated holes. In the hole rich region near the Si-SiO_2 interface an electron from an electron-hole pair stands a good chance of recombining in the same region because of the increased hole density. In addition, electrons will experience only a small field from the metal electrode thus spending more time in the hole rich region. A thermally generated electron-hole pair near the metal is quite a different matter. This region has been depleted of its holes and the field available for electron migration may be fairly strong. Thus, the picture emerges of a source of thermally generated holes near the metal electrode migrating to the hole traps at the Si-SiO_2 interface. During this period, the threshold voltage has a quadratic dependence on time.

As the process continues particularly for higher applied voltages, the charge accumulation at the SiO_2-Si interface results in an ever larger field between the positive charge traps and the silicon. This field becomes so strong that electrons from the silicon begin to tunnel through the barrier. A fraction of those which tunnel through the barrier combine with a positive trap in the hole rich region which is then supplemented by another thermally generated hole in the insulator. There are, however, some electrons which, after tunneling through the SiO_2-Si barrier have sufficient energy to cause ionization resulting in an extra electron-hole pair. The two electrons are swept to the metal electrode and the hole migrates to the interface adding to the hole concentration at the Si-SiO_2 interface further increasing the field. The source of the positive charges at higher voltages is dominated

by the tunneling mechanisms. This new source of charges increases the rate of change of threshold voltage in time. Thus, at the higher voltages $t^{\frac{1}{2}}$ dependence goes to a straight conduction mechanism as seen in the data. At higher temperatures there is, in addition to some species generating hole electron pairs in the insulator, a depopulation of the traps at the $Si-SiO_2$ interface.

The activation energy for ionizing the source of positive charges is, based upon our model, approximately 0.4 ev arrived at by the temperature dependence of g_s. This is extremely low. If sodium were the species in a good thermally grown glass, an activation energy of 1.0 ev is expected[5]. Since the insulator has been ion implanted a considerable amount of unannealed damage is expected. The existance of damage suggests a large interstitial concentration of an ionic species such as sodium. Interstitial diffusion normally has a lower activation energy than substitutional diffusion. However, it does not appear probable that it could be lowered to 0.4 ev. A more likely species is hydrogen. In a good glass structure an activation energy of 0.68 ev has been measured. In the damaged glass this might be lowered by a few tenths of an ev.

Reports on the behavior of hydrogen ion migration suggest that protons once migrated to the $Si-SiO_2$ interface become bound and electrically neutralized causing an irreversible change in threshold voltage[6]. No such action has been reported regarding sodium migration. Since our energy levels are similar to those of hydrogen, a test for that irreversibility was conducted.

Five devices were restored to their initial condition by baking for 8 hours at 125°C. The threshold voltage was measured as previously described. Then the devices were subjected to a 10 volt gate bias at room temperature for 47 and 96 hours respectively (See Figure 25). Note that the -3 volt threshold voltage cannot be trusted since the input protective diodes turn on for voltages less than 0.6 volts. It is clear, however, the threshold voltage is still below 0 for the N channel transistor. Subjecting the devices to a **back** bias for 24 hours at 125°C shows some recovery but still at or below 0 threshold voltage. However, keeping the devices at 10 volts bias for 72 hours at 125°C shows unmistakable recovery. This recovery suggested an irreversible change had taken place within the insulator. Repeating the stress testing at room temperature for 24, 48 and 72 hours reveals that the previously observed instability is no longer present. Thus, through the action of bias and temperature, the charge instability has been eliminated. This irreversibility coupled with the low activation energy suggests that the migrating species may be hydrogen.

Sodium, the common cause of instability in SiO_2 MOS devices, remains a possibility because of its unknown diffusion properties in damaged glass. An attempt was made to detect sodium in the insulator using the x-ray analysis capabilities of a microprobe. The results are shown in Figure 26. The NaKα line is simply background noise in the crystal detector. The limits of detectability for this instrument are estimated to be equivalent to a sodium concentration of 10^{18} atoms/cm^3. If there is sodium present in the SiO_2, it must be less than that concentration. This is still inconclusive since concentrations of 10^{15} atoms/cm^3 can cause threshold voltage instabilities.

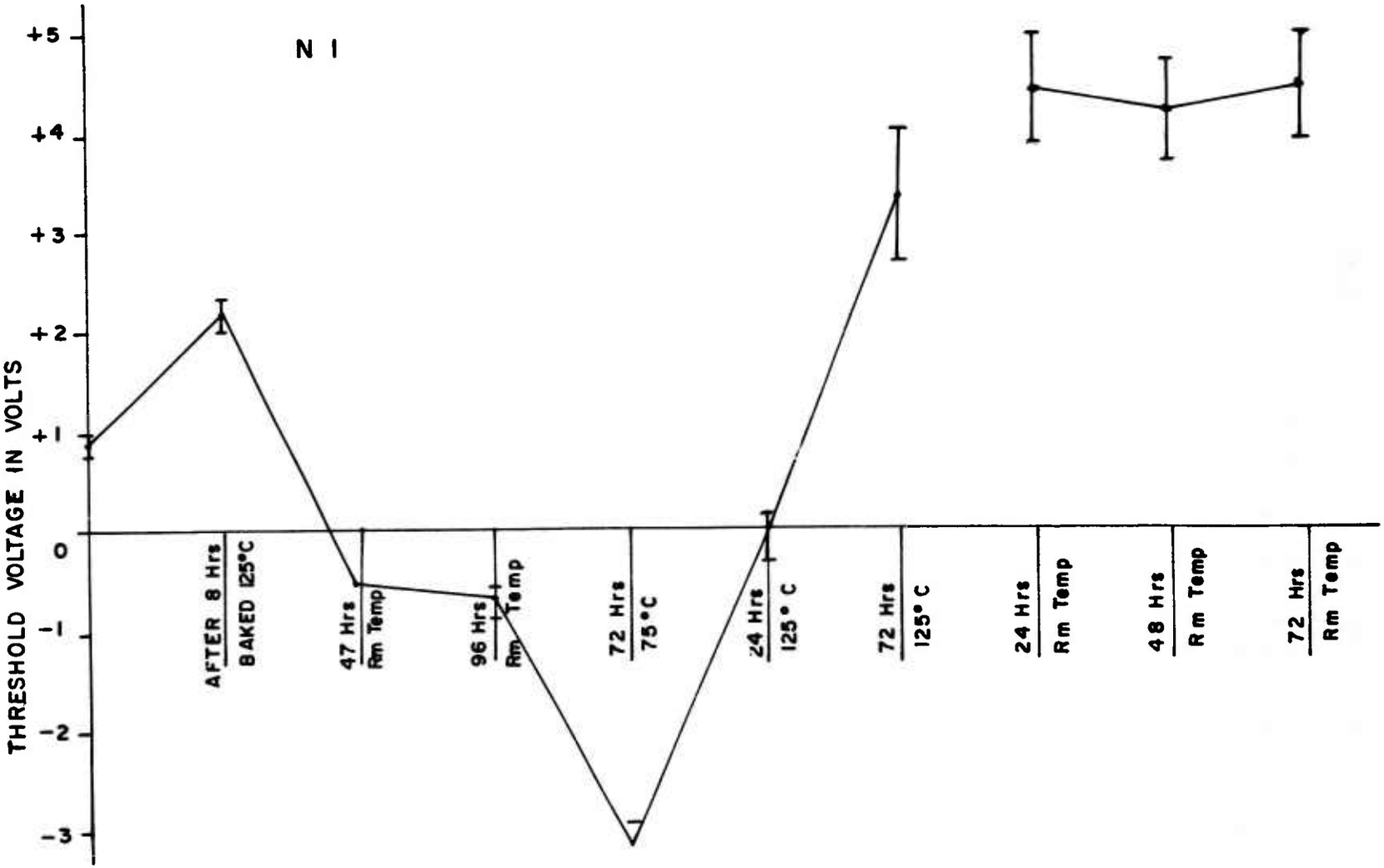
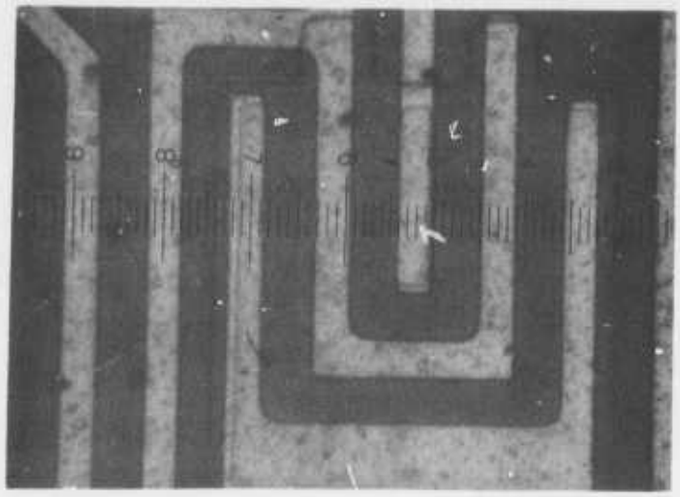
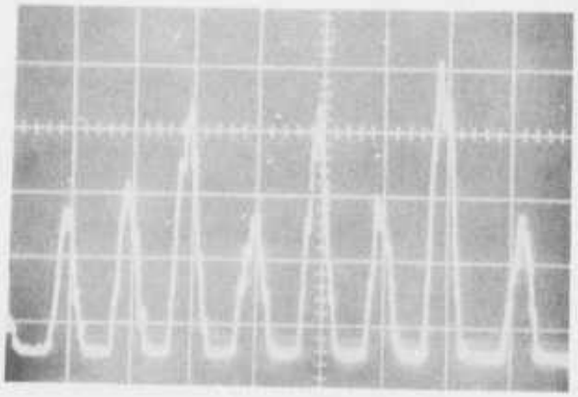


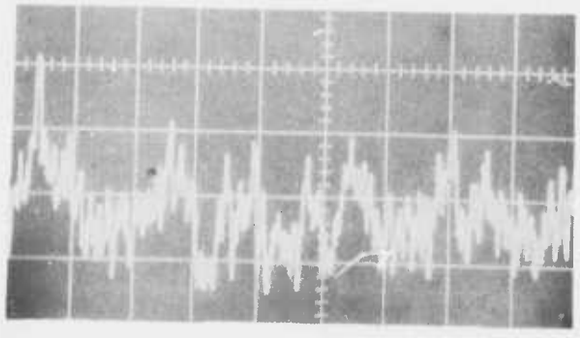
FIGURE 25
SUMMARY OF DEVICE PARAMETER FOR $V_{APPLIED}$ = 10V (39, 40, 41, 44, 46)



NI



AL Kα



N_a Kα

FIGURE 26
ELECTRON BEAM SCAN FOR SODIUM

V RADIATION TESTS:

Two groups of devices were sent to the Air Force Cambridge Research Lab for total dose radiation testing. The first group was temperature biased at 125°C for 72 hours after which time the N1 transistors were "set" by the irreversible process identified earlier. The second group had as its chief characteristic the unstable N1 transistor and were considered "unset". The results of this testing is given in Appendix B. For convenience, Table XIX summarizes those radiation test results.

Table XIX

			$V_{threshold}$ in Volts		
			N1	N2	N3
Set	044	Pre	$5.30_{}$	$4.90_{}$	$5.27_{}$
		Post 10^6r	1.75^{0}	3.15^{9}	1.90^{0}
	046	Pre	$5.38_{}$	$4.90_{}$	$5.25_{}$
		Post 10^6r	3.00^{9}	1.90^{0}	1.80^{0}
Unset	054	Pre	$0.90_{}$	$3.10_{}$	$3.15_{}$
		Post 10^6r	1.60^{0}	3.50^{9}	1.80^{0}
	056	Pre	$0.95_{}$	$3.25_{}$	$3.20_{}$
		Post 10^6r	2.60^{9}	1.75^{0}	1.90^{0}

* The superscripts denote the voltage applied during the radiation exposure.

A study of the table reveals two trends in the data. First except for N2 of device 54, the N2 and N3 of the "unset" devices behave similarly to the three transistors of the "set" units, i.e., the threshold voltages drift down with a total dose of 10^6 rad (Si). The magnitude of the decrease is larger with no bias than with 9 volts applied. On the other hand, in the "unset" devices the N1 drift is in the opposite direction with the 9 volts applied enhancing the shift.

The decrease in threshold voltage of the N channel transistor as the result of the application of +9 volts on the gate is consistent with the model involving electron migration to the metal electrode leaving a net positive charge in the insulator? What is surprising is the application of voltage seems to retard this charge separation rather than being enhanced (see pre and post of 044, 046 for N2 in the Table). In addition, for the "unset" N1 transistors, this model doesn't work at all. Here the 9 volts enhances an <u>increase</u> in the threshold voltage. It is evident that the charge separation model does <u>not work</u> for these units.

If we assume the reason for the breakdown in the standard model is due to electron injection into the insulator from the silicon, we can explain nicely the behavior of device 044, 046 for the N2 transistor. That is, while charge separation goes on, the rate at which it proceeds is modified by the injection of electrons from the silicon slowing down the decrease in

threshold voltage. In the case of the "unset" N1 transistors, one might say the charge separation mechanism has been overpowered by the electron injection process. Evidently, the initial state of the oxide plays a significant role in determining whether charge separation or electron injection are the dominant mechanisms determining the size and direction of shifts in the threshold voltage.

The applied voltage seems to modify the final state the threshold voltage reaches. For 9 volts at 10^6 rad (Si), the devices seek a threshold voltage around +3.0 volts whether the devices are "set" or "unset" and for 0 volts the threshold voltage goes to approximately 1.9 volts again, independent of the initial state of the insulator.

This can be explained by assuming greater electron injection at larger applied voltages and thus the balance between the two mechanisms will be at a higher threshold voltage than for no applied gate voltage.

Figure 4 of Appendix B is very important from an understanding viewpoint. Notice for devices with high V_{th} the rate of decrease is higher for 0 volts than for +9 volts. And in the opposite sense, the low V_{th} devices change more rapidly with +9 volts applied during the radiation. Now from the behavior at 0 volts for both the high and low initial threshold voltage devices, it is evident there is a field inside the insulator at the start. The charge in the insulator must be positive and close to the metal oxide interface in the high threshold devices otherwise the charge separation mechanism would be suppressed, rather than enhanced when comparing the 0 and 9V curves for 046 and 044. We are then forced to assume because the 056 and 054 devices have low threshold voltages that they contain a higher concentration of positive charges than 046 and 044.

This discussion then leads us to a model which describes the entire sequence of data in the radiation environment and at the same time is consistent with the behavior of the N1 and N2 class of transistors in the temperature bias studies reported previously.

VI PROPOSED MODEL OF ALUMINUM IMPLANTED MOS TRANSISTOR:

Assume that within the insulator which has been ion implanted but not burned in, a layer of positive charges exist which are close to the Si-SiO_2 interface as shown in Figure 27. In addition, assume there is a finite quantity of an easily thermally ionized species such as hydrogen distributed more or less evenly throughout the insulator. Finally, assume electron injection from the silicon is possible when a high field exists at the SiO_2-Si interface (See Figure 27).

With these assumptions, we will first describe the behavior of the devices under temperature bias stress testing and then go into the radiation behavior with bias.

Temperature Bias Conditions

Condition 1, Zero Bias, Room Temperature to 125°C

At zero bias and room temperature, the state of the insulator is in charge balance as far as positive charge production and annihilation is concerned. Hole-electron pairs thermally generated from the hydrogen species separate in the internal field, the electrons recombining with the positive charge layer at X_0 and the holes accumulating at the metal insulator interface. This process continues until the field drops to zero in the region of X_0. At this point, charge separation is impossible and the device has stable properties. At elevated temperature, thermal generation of the hydrogen species is accomplished more readily and the equilibrium condition is reached faster. The effect of this redistribution of positive charge is to raise the threshold voltage somewhat simply because the centroid of positive charges has changed. Evidence of this change can be seen in Figure 25 (V_{th} after 8 hours bake at 125°C).

Condition 2, 10 Volt Gate Bias, Room Temperature to 125°C

The positive charges having been redistributed according to Condition 1, will now see a field established by the applied voltage. The positive charges will be swept to the trap layer indicated. For a short period, the rate of accumulation at the X_0 layer will be linear with voltage and time. Once the charge layer begins to be established such that it alters appreciably the field in the X_0 region, the rate of accumulation will be from the field enhanced diffusion mechanism previously discussed, thus giving a $t^{\frac{1}{2}}$ dependence. Having established the positive charge layer from the existing holes in the insulator, to add to them requires thermal generation of the hydrogen species in the region. The subsequent rate of accumulation will be limited in voltage by the existing space charge. In addition, if the voltage is large enough, a tunneling mechanism* creates further holes for accumulation as was previously discussed. The net effect is to cause a drastic reduction in threshold voltage as can be seen in Figure 25.

Eventually, we exhaust the population of hydrogen, i.e., they have been accumulated at the X_0 layer. Now the electrons injected by tunneling begin to neutralize the positive charge layer which we assume is a deep energy trap.

* While tunneling is postulated, simple SiO_2-Si interface barrier lowering may be involved.

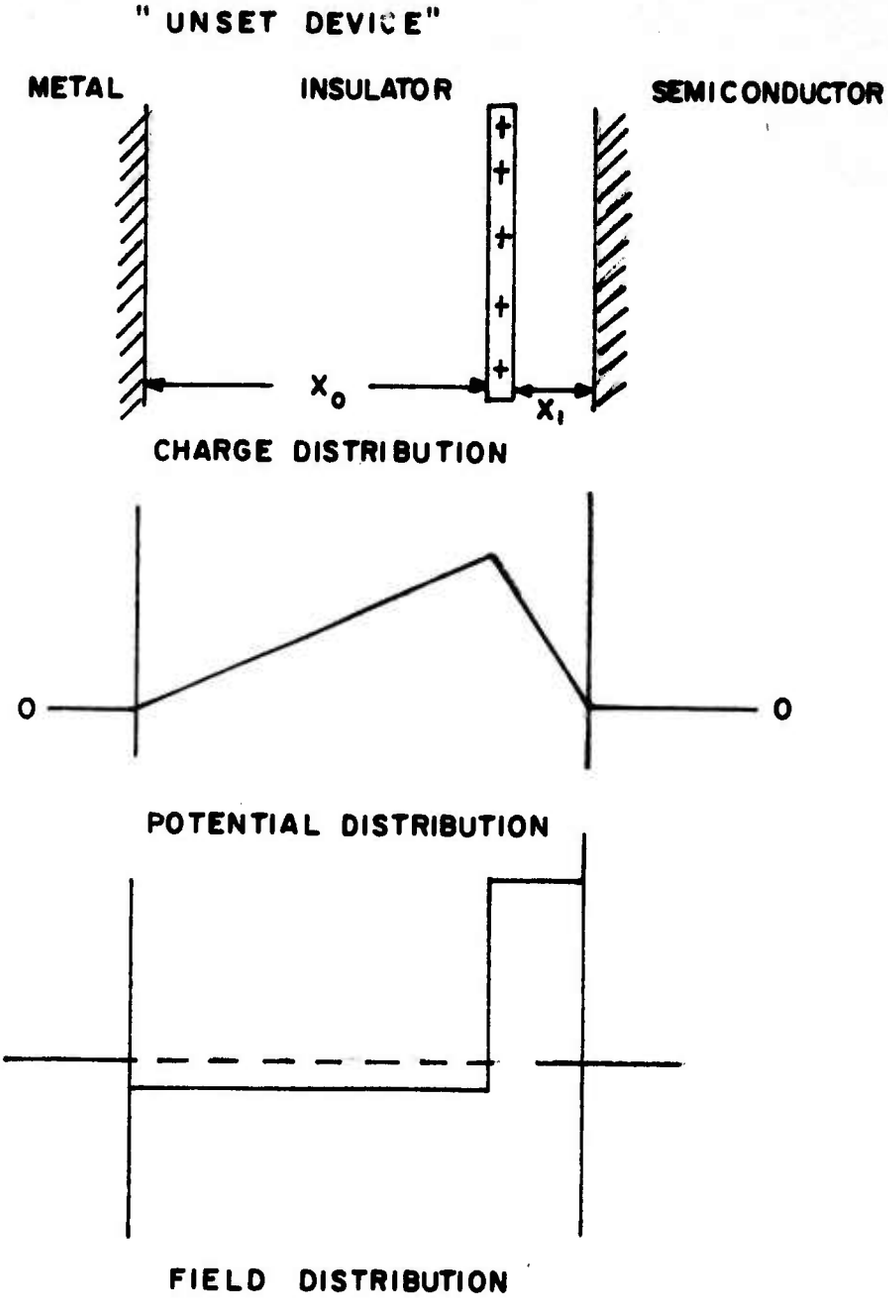


FIGURE 27
MODEL OF "UNSET" DEVICE

The hydrogen is in effect eliminated from the insulator. At this stage, the threshold voltage increases again and stabilizes at the point where the rate of charge accumulation is balanced by electron injection. The exact balance is a function of the applied voltage (See Figure 25).

Condition 3, 10 Volt Gate Bias, Room Temperature

The hydrogen having been "cleaned" from the insulator no longer plays a role in room temperature instability. We have fewer positive charges at the X_0 layer so the threshold voltage is higher than Condition 1 or the early part of Condition 2. The device is now relatively stable. There is further evidence that the layer of positive charges at X_0 has been nearly eliminated and that a new layer considerably closer to the metal exists. The reason is that the X_0 layer has been depleted of charge, reducing the field and turning off the tunneling mechanism (See Figure 27). The charge concentration at the new layer is inversely proportional to the gate voltage during the burn-in. This may account for the threshold voltage in Figure 25 at the end of the test being over a volt higher than the original burn-in of transistors N2 and N3.

Radiation Testing:

The model remains the same but because of the ionizing radiation, the electron injection from the silicon into the insulator is greatly enhanced. We begin by considering the "unset" devices.

"Unset" Devices, Zero Volts Gate Bias

The "unset" zero gate voltage devices have a significant charge layer as indicated by the low initial threshold voltage in Figure 24 and depicted in Figure 27. The field in region X_1 set up by the charge layer at X_0 enhances electron injection into the insulator. At the same time, in region X_0 the charge separation acts in such a direction as to deplete the positive charge accumulation at X_0 while adding positive charge at the metal insulator interface. The net effect of the depletion at X_0 is offset somewhat by the metal interface accumulation. The resulting field for charge separation in X_0 is minimized as well for injection at X_1. The result is a gradual increase in threshold voltage with dose.

"Unset" Devices, Nine Volts Gate Bias

The rate of charge separation increases in direct proportion to the voltage applied and is in such direction to accumulate charges at X_0. However, the field in the region X_1 will increase as well. The electron injection mechanism should be a powerful function of the X_1 field and therefore we can expect that the electron injection will increase faster than the charge separation mechanism. Thus, the accumulated charge will be rapidly annihilated until a balance between the two mechanisms is reached. In this case, that balance should be at a higher threshold voltage than for the zero bias case.

Thus for the "unset" devices, one would expect the threshold voltage to behave as shown in Figure 28.

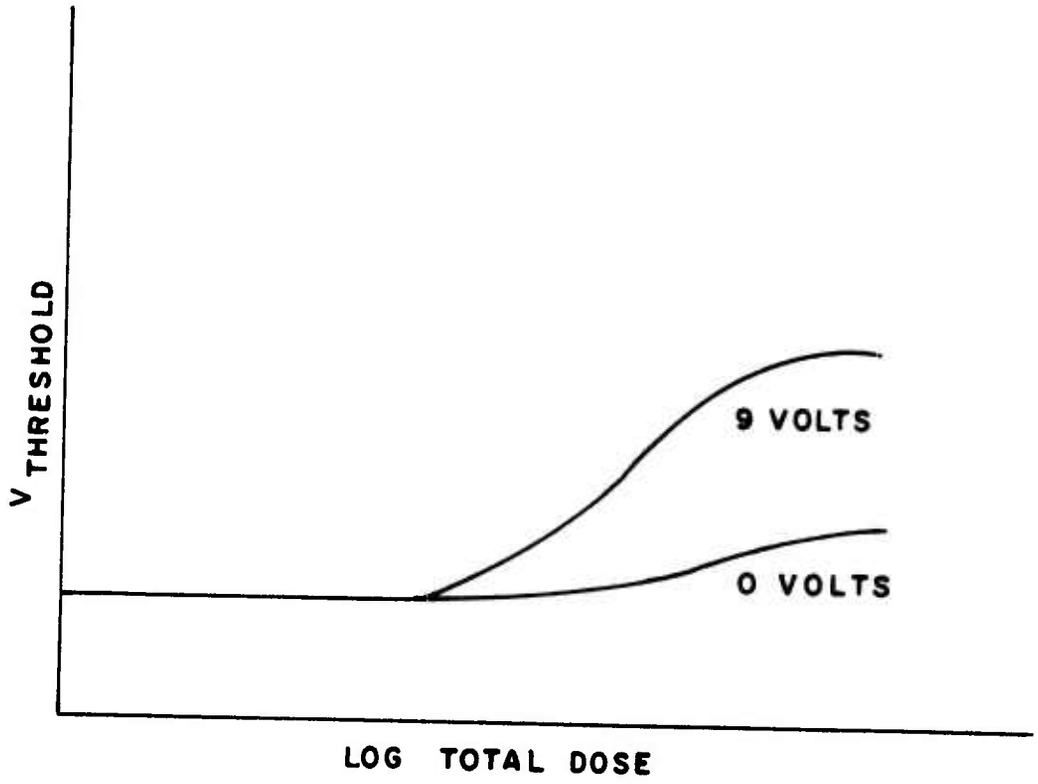


FIGURE 28
THRESHOLD VOLTAGE AS A FUNCTION OF TOTAL IONIZING DOSE

"Set" Devices, Zero Volts Gate Bias

Remember in the "set" devices, the positive charge accumulation layer has all but disappeared and has been replaced by another layer somewhat closer to the metal (See Figure 29).

Now under zero bias conditions the built-in field in the bulk of the insulator causes the charge separation mechanism to accumulate positive charges at the X_0 layer, i.e., depleting the positive charges near the metal and increasing the positive charges at X_0. At the same time, since the field in X_1 is considerably lower, the electron injection mechanism is small. Thus, for zero gate voltage we expect a rapid drop in threshold voltage and saturation at quite a low level.

"Set" Devices, Nine Volts Gate Bias

With nine volts, the charge separation mechanism is more active, driving holes to the X_0 layer. But the higher field causes a large increase in electron injection from the silicon. If the injection mechanism is a powerful function of field, this is not unreasonable. The result is still a decrease in threshold since the separation mechanism is dominant, but the rate of decrease has been slowed down. We would expect the saturation threshold voltage to be higher due to the considerably higher electron injection process. Hence, the threshold voltage as a function of total dose could be expected to appear as in Figure 30. Close agreement then is found between Figures 28 and 30 and Figure 4 of Appendix B.

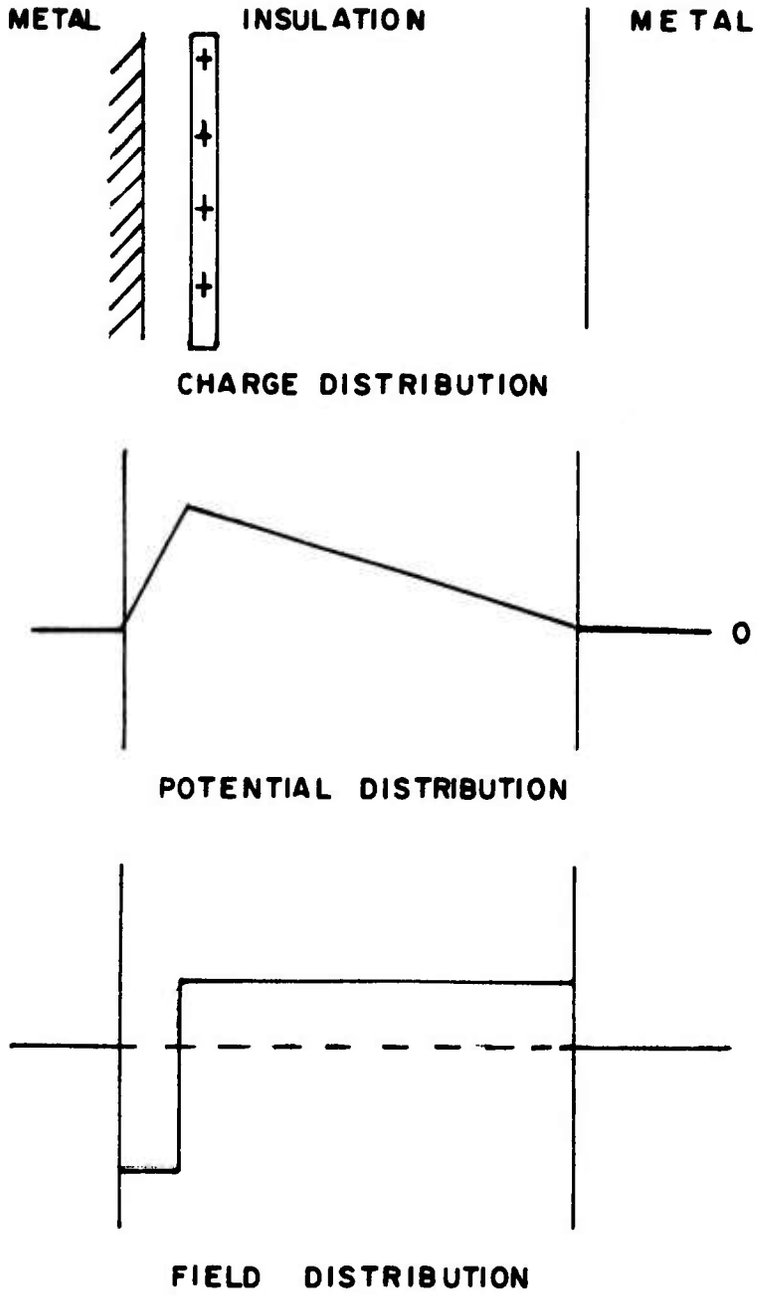


FIGURE 29
MODEL OF SET DEVICE

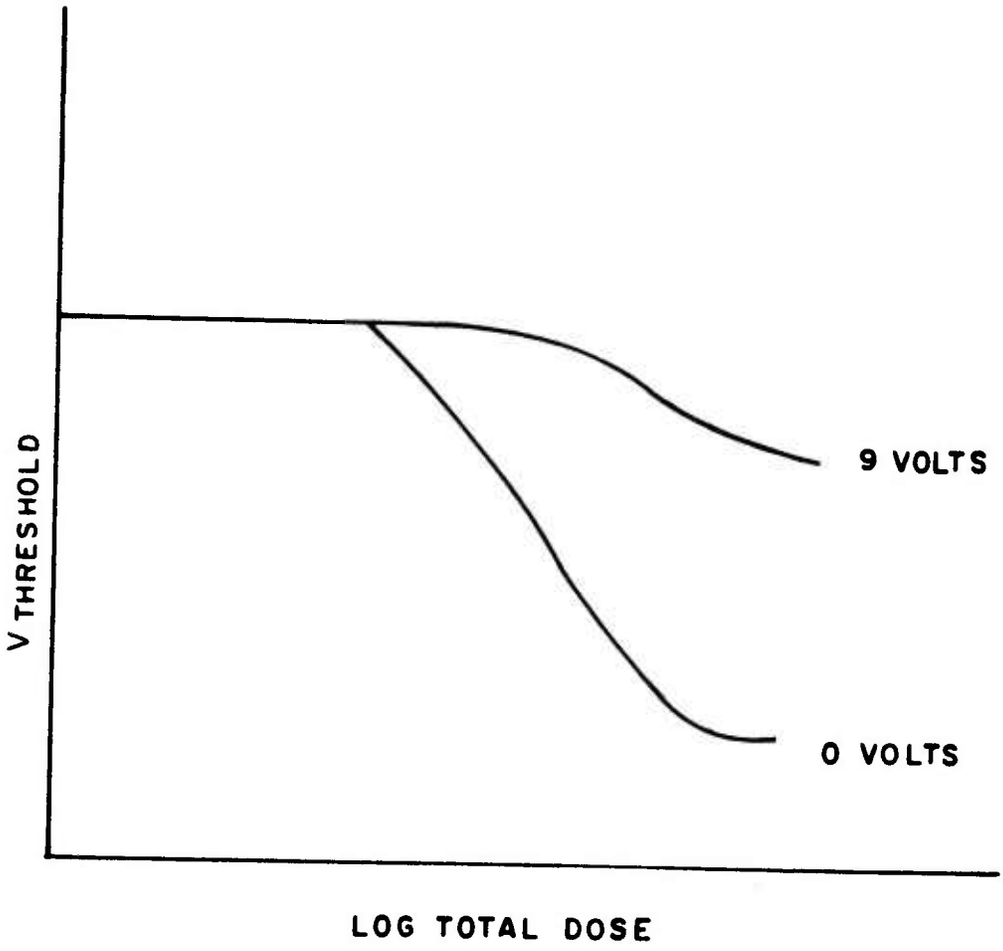


FIGURE 30
THRESHOLD VOLTAGE SHIFT AS A FUNCTION OF IONIZING RADIATION

VII CONCLUSIONS:

Aluminum ion implanted CMOS/Bulk units were shown to have uniform electrical properties. The N1 transistor had threshold voltages consistently lower than N2 and N3.

Under step stress temperature bias testing, the 4007 microcircuits were found to be extremely unstable, failing in a matter of hours at maximum rated voltage at room temperature and in minutes at nominal voltages at elevated temperatures of 100°C.

The major cause of failure was threshold voltage instability of the N1 transistor. The N2 and N3 transistors were considerably more stable and the P channel transistors were very stable.

Failure analysis of the N1 transistor showed the failure to be due to charge instability in the gate insulator resulting in a threshold voltage shift and not a result of leakage current in the input protective network diodes nor was it related to inadequacy in the guard band diffusion.

The N1 transistor instability was characterized for both temperature and voltage. The threshold voltage shift could be described by the relation

$$dV_{th} = [AV_a^2 + BV_a^2 e^{-b/V_a}] e^{-E_s/kT} t^{\frac{1}{2}} + CV_{th} e^{-E_t/kT} t$$

A model based upon an ionic species drifting under the influence of applied bias was proposed. The species appeared to be thermally generated at room temperature and migrated with a space charge limited voltage dependence. At higher voltages, an additional source of charge results from electrons tunneling across the $Si\text{-}SiO_2$ barrier* and, the resulting ionization leads to additional positive trapped charge at the insulator. The activation energy for ionizing the species (E_s) is approximately 0.4 ev and that of the trap sites (E_t) around 0.9 ev.

The N1 instability was demonstrated to be irreversible if left on bias at elevated temperature. This accounted for the difference in N1 and N2, N3 threshold voltages of the population prior to stress testing. It was learned that N1 was unbiased while N2 and N3 were biased during the burn-in screen.

The curing of the instability and low activation energy suggest hydrogen as the ionic species though no positive identification of the species was possible.

Based upon these results it is very possible that the introduction of the ionic species was caused by the ion implantation or the implantation process caused sufficient unannealed damage to enhance ion migration in the insulator.

* This may be simple barrier lowering.

Unless an annealing schedule after implantation can be found to restore the interstitial ionic species to substitutional sites in the insulator, it is likely the instability problem will not be eliminated.

The proposed model suggests that the principal reason for improved performance in the radiation environment is a field built into the insulator as the result of ion implantation. The presence of this field enhances electron injection from the silicon to cancel the effects of hole-electron pair separation caused by the applied gate voltage.

The threshold voltage instability and improved radiation tolerance, (i.e., the positive shift in threshold of an N channel device) are not necessarily related. While the data (See Figure 4, Appendix B) suggests there is a trade off between hardening and reliability, the problems may be specific to this group of devices. The model suggests the reason for the instability is charge migration in the insulator, while the hardening is associated with the built-in field. Eliminating the charge migration may not drastically affect the source of the built-in potential.

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APPENDIX A

Functional Dependance of Field Enhanced Diffusion with a Generating Source

Consider an element of oxide surface of width ℓ and depth $\Delta x = X_2 - X_1$. To obtain an expression for the charge density Q accumulated in this element per unit time an expression for the current crossing X_1 and X_2 is as follows:

$$I_1 = -\frac{\ell}{R}\frac{\partial V}{\partial X}\Bigg|_{x_1}$$

$$I_2 = -\frac{\ell}{R}\frac{\partial V}{\partial X}\Bigg|_{x_2}$$

where R = is the bulk resistance per unit distance of the oxide (assumed a constant) and V (x,t) is the electrostatic potential at each depth.

$$\frac{dQ}{dt} = \frac{I_1 - I_2}{\ell\,\Delta x} = \frac{1}{R\,\Delta x}\left(\frac{\partial V}{\partial x}\Bigg|_{x_2} - \frac{\partial V}{\partial x}\Bigg|_{x_1}\right) = \frac{1}{R}\frac{\partial^2 V}{\partial x^2} \qquad [1]$$

But the charge Q is just the oxide capacitance per unit distance, C_o, times the potential difference, V, across the oxide; therefore

$$\frac{dQ}{dt} = C\frac{\partial V}{\partial t} = \frac{1}{R}\frac{\partial^2 V}{\partial x^2} \qquad [2]$$

If, in addition, charge is generated within the oxide at a rate $g(x,t)$ then this generation rate must be added to [2].

$$\frac{dQ}{dt} = C\frac{\partial V}{\partial t} = \frac{1}{R}\frac{\partial^2 V}{\partial x^2} + g(x,t) \qquad [3]$$

Letting $K = \frac{1}{R}$ and $\alpha = \frac{1}{RC}$

the differential equation is put in the form

$$\frac{\partial^2 V}{\partial x^2} + \frac{g(x,t)}{K} = \frac{1}{\alpha}\frac{\partial V}{\partial t}$$

For a semi-infinite solid $0 \le x \le D$ with an initial voltage distribution $F(x)$ and for times $t > 0$ charges are generated within the solid at a rate

$g(x,t)$ while the boundary surface at $x = 0$ is fixed at a given voltage V. The boundary value problem for charge conduction is:

$$\frac{\partial^2 V}{\partial x^2} + \frac{g(x,t)}{K} = \frac{1}{\alpha}\frac{\partial V}{\partial t} \quad \text{in } 0 \le x \le \infty, \quad t > 0$$

$$\frac{\partial V}{\partial x} = 0 \text{ at } x = 0, \ t > 0 \qquad V = F(x) \text{ in } 0 \le x < \infty, \ t = 0$$

The solution of [3] to this boundary value problem is

$$V(x,t) = \frac{1}{\sqrt{4\pi\alpha t}} \cdot \int_{x'=0}^{\infty} F(x') \cdot \left[e^{-\frac{(x-x')^2}{4\alpha t}} + e^{-\frac{(x+x')^2}{4\alpha t}} \right] dx' +$$

$$\frac{\alpha}{K} \int_{t'=0}^{t} \frac{dt'}{\sqrt{4\pi\alpha(t-t')}} \int_{x'=0}^{\infty} g(x',t') \cdot$$

$$\left[e^{-\frac{(x-x')^2}{4\alpha(t-t')}} + e^{-\frac{(x+x')^2}{4\alpha(t-t')}} \right] dx'$$

If the initial voltage distribution is everywhere zero and letting $g(x,t)$ be a constant source of charge located at b in the semi-infinite solid then:

$$F(x) = 0$$

$$g(x,t) = g_s(t) \cdot \delta(x-b)$$

and equation [4] becomes

$$V(x,t) = \frac{\alpha}{K} \int_{t'=0}^{t} \frac{g_s(t)}{\sqrt{4\pi\alpha(t-t')}} \cdot \left[e^{-\frac{(x-b)^2}{4\alpha(t-t')}} + e^{-\frac{(x+b)^2}{4\alpha(t-t')}} \right] dt'$$

Letting the charge generating term be constant and located on the surface, i.e. $b = 0$, the solution reduces to:

$$V(x,t) = \frac{2\alpha}{K} \int_{t'}^{t} \frac{g_s}{\sqrt{4\pi\alpha(t-t')}} \, e^{-\frac{x^2}{4\alpha(t-t')}} \, dt'$$

now substituting $\eta = x/\sqrt{4\alpha(t-t')}$

then $dt' = x^2 d\eta / 2\alpha\eta^3$

with the limits

$\eta = x/\sqrt{4\alpha t}$ at $t' = 0$

$\eta = \infty$ at $t' = t$

Equation 5 becomes

$$V(x,t) = \frac{g_s x}{K\sqrt{\pi}} \int_{x/\sqrt{4\alpha t}}^{\infty} \frac{e^{-\eta^2}}{\eta^2} \, d\eta \qquad [7]$$

Integrating [7] by parts leads to

$$V(x,t) = \frac{g_s x}{K\sqrt{\pi}} \left[\frac{1}{\eta} e^{-\eta^2} - \sqrt{\pi} \operatorname{erfc}(\eta) \right] \qquad [8]$$

Substituting for $[\eta]$ from [6] into [8] yields:

$$V(x,t) = \frac{2g_s\sqrt{\alpha}}{K} \left[\frac{t^{\frac{1}{2}}}{\sqrt{\pi}} e^{\frac{-x^2}{4\alpha t}} - \frac{x}{2\sqrt{\alpha}} \operatorname{erfc}\left(\frac{x}{\sqrt{4\alpha t}} \right) \right] \qquad [9]$$

Equation [9] describes the voltage at any x and t greater than 0 which is developed as a result of charges being generated at the surface of an insulator and subsequently drifting under the influence of a voltage applied on that insulator after t = 0.

Now for long times, i.e., $t >> \frac{x^2}{4}$ then $e^{\frac{-x^2}{4\alpha t}} \longrightarrow 1$ and $\operatorname{erfc}\left(\frac{x}{\sqrt{4\alpha t}} \right) \longrightarrow 1$ equation [9] approaches

$$V(x,t) = \frac{2g_s\sqrt{\alpha}}{K} \left[\frac{\sqrt{t}}{\pi} - \frac{x}{2\sqrt{\alpha}} \right] \qquad [10]$$

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