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STUDY OF RADIATION EFFECTS IN BULK CMOS MICROCIRCUITS, I^2L/LSI LOGIC CELLS AND OPTICAL COUPLERS

Northrop Research and Technology Center
3401 West Broadway
Hawthorne, California 90250

June 1975

Final Report for Period January 1974—December 1974

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Prepared for

Director
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Results are presented on the study of radiation effects in bulk CMOS microcircuits, basic logic cells of developmental integrated-injection-logic (I^2L) LSI, and optical couplers. Radiation effects considered include the permanent damage effects resulting from neutron displacement damage and total ionizing radiation dose. Transient photoresponse has been measured as a function of ionizing radiation pulse width. CMOS latch-up was investigated as induced by electrical pulsed overstress

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20. ABSTRACT (Continued).

and/or pulsed ionizing radiation exposure. No significant synergistic effects were observed.

PREFACE

Results presented in this report are part of a continuing effort to study radiation effects on the components and technologies of modern MSI/LSI. The scope and documentation of earlier work has been presented in the following reports:

1. "Radiation Effects on MSI/LSI Electronic Devices and Circuits," J. P. Raymond, D. N. Pocock, J. R. Srour, R. E. Johnson, and G. T. Fujii; Contract DASA 01-70-C-0093, Report No. DASA 2616; July, 1971.

   Characterization of transient photoresponse and neutron damage of bipolar digital and analog SSI and MSI arrays as well as transient photoresponse on thin-film transistors, p-MOS SSI and MSI static arrays, and p-MOS MSI dynamic arrays.

2. "LSI Vulnerability Study," J. P. Raymond, D. N. Pocock, and C. W. Perkins; Contract DASA 01-70-C-0093, Report No. DNA 2865F; October, 1972.

   Characterization of transient photoresponse and permanent damage effects due to neutron-, total-ionizing-dose, and pulsed-electrical-overstress exposure on bipolar TTL and ECL and p-MOS MSI/LSI arrays. Also includes study of pulsed electrical overstress damage thresholds on discrete transistors.

3. "MSI/LSI Radiation Effects Study," J. P. Raymond, D. N. Pocock, C. W. Perkins, and J. E. Ashe; Contract DASA 01-70-C-0093, Report No. DNA 3246F; 26 March 1975.

   Characterization of Schottky-clamped TTL, hardened TTL, hardened op amp, junction-isolated CMOS, and CMOS/SOS MSI/LSI arrays. Study included modeling, transient photoresponse, and permanent damage due to neutron, total ionizing doses, electrical pulsed overstress and high level pulsed ionizing dose rate exposure.

4. "Study of Radiation Effects in MSI/LSI Technologies," J. P. Raymond, J. E. Ashe, C. W. Perkins, T. Y. Wong, and J. T. Fujii; Contract DNA 001-73-C-0154, Report No. DNA 3517F; 26 March 1975.

   Characterization of total dose and pulsed electrical overstress susceptibility on hardened CMOS arrays, completion of electrical pulsed overstress study on Schottky-clamped TTL arrays, modeling and characterization of LED and optical coupler transient photoresponse and preliminary study of neutron susceptibility and transient photoresponse of integrated injection logic (I^2L).

Key results of these earlier studies have been summarized in a paper written for the 1974 IEEE Radiation Effects Conference and is included, for convenience, as Appendix A of this report.

Results presented in this report are a continuation of the CMOS and optical coupler characterization with further study on the developing I^2L technology. Studies presently underway will emphasize the modeling and characterization of very complex arrays to develop insight into the overall test/analysis methodology, as well as continue the characterization of evolving bipolar and MOS technologies.

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1.0 INTRODUCTION

1.1 Overall Program Summary

The purpose of this study has been to evaluate the radiation vulnerability of semiconductor microcircuits as they have evolved in complexity. Original concern was motivated by the rapid escalation from single-function microcircuits to medium-scale integration (MSI) arrays of from 10 to 100 gates functions in complexity and to large-scale integration (LSI) arrays of greater than 100 equivalent gate functions in complexity. In terms of semiconductor technology, the evolution of MSI/LSI was initiated with the development of p-MOS. The development of p-MOS technology in 1965 allowed the realization of simple logic cells using minimum-geometry elements and simple processing. The principal problem of p-MOS technology was speed in the capability of driving the wiring capacitance between microcircuit packages. It was desirable, therefore, to put as much of the logic function on a single chip as possible to optimize overall performance. The advantages of small-geometry special-purpose logic cells were soon also applied to bipolar technology.

Basic technological advantages of MSI/LSI can be realized best in digital microcircuits and complex arrays, where the same basic concepts of logic cell design can be applied repetitively throughout the design. Linear microcircuits, while comparable in element density and complexity to digital MSI arrays, are generally custom designs. The degree of standardized design, however, has also been a substantial variable in MSI/LSI. On one hand, the array may be a completely custom design, utilizing the same basic logic cell technology in the design of an optimized array in terms of total geometry and performance. On the other hand, a set of

standardized logic cells can be defined to be interconnected by a computer-generated metallization pattern. Location of required cells can be either determined by a standard wafer pattern, or by the location of tested good logic cells on individual wafers. The present tendency on custom versus standard-cell LSI is to use custom designs for standard products and to use standard cells and custom metallization for each special low-quantity array requirement.

The advent of MSI/LSI introduced new types of bipolar and MOS logic cells with high element densities, and new multi-layer metallization patterns, all of which originally spurred concern in terms of introducing new failure mechanisms in radiation vulnerability. As we have found, these concerns were valid in that the nature of the MSI/LSI logic cells modifies the nature and failure levels in the arrays, but there are no indications that the basic failure mechanisms are any different than those familiar in simple microcircuits. A more subtle, but equally important distinction was, however, noted in the process of determining MSI/LSI vulnerability. The problem is that the radiation vulnerability of the MSI/LSI array must be determined in terms of the overall array operation. In SSI digital sub-systems, on the other hand, the radiation vulnerability of individual logic blocks could be measured directly, with the results used to define the worst-case subsystem test condition which was then verified by additional testing. The requirement of vulnerability of the overall MSI/LSI array performance leads to the necessity of a very thorough evaluation which, to be limited to a reasonable experimental effort, must rely on analytical techniques of logic simulation and simplified modeling.

Evaluation of MSI/LSI susceptibility under this program has consisted of investigation of a wide variety of radiation effects on selected arrays representing production MSI/LSI technologies. The characterization, in general, included measurement of the photoresponse as a function of radiation pulse width, neutron displacement damage, total ionizing dose surface effects, permanent damage due to electrical pulsed overstress, and permanent damage resulting from high-level pulsed ionizing radiation.

Selection of samples chosen for study can be presented in terms of a simplified description of the evolution of MSI/LSI technology itself. First, we can consider MOS technology, which, as previously remarked, probably initiated MSI/LSI with the constraints as we presently know it. Initial logic cells of MOS technology were essentially the same logic functions as single-function bipolar microcircuits, that is, gates and flip-flops, except realized with the simplier circuits using p-MOS technology. Initially, the gate conductor of all p-MOS arrays was aluminum with fairly high threshold voltage for the transistor elements. Five types of static logic p-MOS arrays have been characterized in this program.

The first major development in the p-MOS technology was the development of very high density logic cells in which the logic data were stored in terms of charge on the junction and gate capacitors. The development of dynamic logic allowed electrical operation at very low power levels for operation at low-medium clock rates. Four types of dynamic logic p-MOS arrays have been characterized in this program.

The next major development in MOS technology was the use of polycrystalline silicon as the gate conductor of the p-MOS transistor. This, with the evolution in oxide process control, reduced the threshold voltage of the

transistor elements and improved the performance of both static and dynamic arrays. Three types of silicon gate p-MOS arrays have been characterized in this program.

Emphasis in early MOS MSI/LSI has been in the application of p-MOS transistor elements because of the process and control difficulties in the development of n-channel enhancement MOS transistor elements. The development of n-MOS transistor elements is desirable because of the improvement of approximately a factor of three in channel conductance due to the relative increase in carrier mobility, and for the application in complementary arrays using both p- and n-MOS elements for virtually zero power dissipation during standby operation. As it turns out, development of complementary MOS has preceded the development of n-MOS LSI arrays, principally because small-scale CMOS functions could be defined that allowed evaluation of basic cell performance with a minimum number of the typical disadvantages. For this reason, in addition to the promise of advantages in both electrical performance and radiation hardening, CMOS arrays have been included in some numbers. It was anticipated that the radiation vulnerability of n-MOS arrays would be qualitatively the same as that determined by previous study of p-MOS arrays, and therefore have not yet been included in the program. Commercial CMOS was originally developed with a junction-isolated structure on a bulk crystalline silicon substrate and used aluminum-gate conductors. Development of CMOS using thin silicon film on an insulating substrate was originally developed to increase the speed of the arrays, but also is of substantial advantage in eliminating electrical- and radiation-induced latch-up and in minimizing the transient photoresponse of the CMOS array. The advantage of silicon gate technology developed initially for p-MOS

technology has also been applied to CMOS for improved performance. Ten types of CMOS arrays have been characterized in this program.

In the future development of MOS technology it seems clear that the advantages of CMOS in low-power, medium-speed application will ensure the development of CMOS/LSI. The preponderance of commercial applications will use CMOS junction-isolated on bulk silicon, but high-speed and radiation-hardened arrays will be CMOS on a bulk insulator substrate (i. e., CMOS/SOS). In addition to the development of CMOS, it seems clear that n-MOS technology will be developed for specialized applications where simple logic cells can be employed advantageously. These applications include MOS read-only, programmable read-only, and read-mostly memories. In some of these applications gate insulators of silicon dioxide and silicon nitride may be used to store information by deliberately shifting the element threshold voltage by an external data-write signal.

Evolution of bipolar MSI/LSI, unlike MOS technology, has been closely linked to SSI microcircuit technology. As an extention of microcircuit technology, bipolar development can be considered in two main branches: transistor-transistor logic (TTL), and emitter-coupled logic (ECL). TTL technology is, in turn, an evolution of diode-transistor-logic in which the input diode network was merged into a multi-emitter transistor input network with some additional modifications in the output driving network (totem-pole outputs). TTL, developed primarily as a logic family of SSI microcircuits provided medium-high speed switching performance at modest power dissipation. Emitter-coupled logic, on the other hand, was developed as a family of SSI microcircuits to provide very high switching performance regardless of the relatively high power dissipation. Improvements and variations in both TTL and ECL technology have resulted from

the improvement of the bipolar transistor elements and in the value of the resistor elements in determining the switching speed and power dissipation of the array. Thus, there are low-power, nominal, and high-speed variations in design of TTL and ECL arrays. Twenty types of TTL and ECL arrays have been characterized in this program.

The principal disadvantages of TTL arrays initially were the restrictions in transistor element design and performance resulting from saturated switching operation. Saturation of the transistor element is eliminated with the addition of a Schottky-diode in parallel with the base-collector junction. With the elimination of transistor saturation, the gold-doping used to minimize the transistor storage time could be eliminated and transistor parameters could be more favorably optimized, since the addition of the Schottky-clamped elements also allowed a substantial improvement in the overall performance of switching response and power dissipation. Five types of Schottky-clamped TTL arrays have been characterized in this program.

The newest development in bipolar MSI/LSI technology is the development of Integrated Injection Logic (I^2L) which is based on a logic cell consisting of merged pnp and npn transistors. Although I^2L has not yet been developed to production technology, it seems clear that it will be the first truly LSI bipolar technology to do so. By LSI technology we mean that the full potential of the development will be realized in complex arrays where the logic signal processing is done on the chip and performance is degraded by signal transmission between chips; much like the MOS/LSI technology. Initial results at several laboratories indicate that I^2L is competitive to the best MOS technology for low-power, low-medium-speed applications. No production-qualified samples of I^2L

samples have been characterized, but test results on developmental devices have been studied to obtain an initial estimate of the nature and failure levels of the radiation vulnerability.

The future development of bipolar technology, in the short range, will be dominated by Schottky-clamped TTL and ECL arrays; and in the long range will be dominated by I^2L for low-medium-speed applications and ECL for high-speed applications.

Quantitative results on the failure levels observed for the MSI/LSI arrays studied during the program are summarized in a technical paper which is included in this report as Appendix A. All the failure levels are those observed under laboratory test conditions with a nominal definition of required performance. Real system performance requirements will, in general, result in failure levels that are lower than the system-independent results quoted.

More important than the quantitative interpretation of the array failure levels are the overall conclusions regarding MSI/LSI vulnerability. Some of these results are in terms of what was not observed:

- All effects observed were the result of basic failure mechanisms familiar in simpler microcircuits. No failure mechanisms unique to MSI/LSI technology have been identified.
- No ionizing radiation-induced latch-up has been observed on any array at exposure levels up to 5×10^{10} rads(Si)/s. It is suggested, then, that the presence of latch-up is no more (but certainly no less) than in simpler microcircuits of the same technology.

1.2 Present Program Summary

Results presented in this report represent study of the characterization of radiation effects in bulk CMOS microcircuits, basic I^2L logic cells, and optical couplers.

In this report, Section 2 presents results of characterization of total-dose-induced permanent damage and transient photoresponse on five types of basic bulk CMOS microcircuits: CD4023A Triple 3-input NAND gate, CD4025A Triple 3-input NOR gate, CD4030A Quad 2-input exclusive-OR gate, CD4027A Dual J-K Master/Slave flip-flop, and CD4026A micro-power phase-locked loop. A total of 20 samples of each microcircuit type were obtained to a variety of reliability specifications. The total-ionizing-dose susceptibility of the microcircuits as an overall group ranged from approximately 8×10^4 rads(Si) to greater than 10 Mrads(Si). The total-dose failure levels for each microcircuit type were fairly consistent for parts of the same reliability specification. It was not possible, however, to define a dependence of radiation susceptibility on the severeness of the reliability specification.

The transient photoresponse logic upset levels for all the CMOS microcircuits were a strong function of the radiation pulse width. In the narrow-pulse (30 ns) flash x-ray environment the logic upset levels were typically on the order of 10^8 - 10^9 rads(Si)/s. In the wide-pulse (4.5 μs) linear accelerator environment, however, the logic upset levels were on the order of 10^7 - 10^8 rads(Si) with a decrease in critical dose rate of approximately 10 for each microcircuit type. There were a significant number of incidents of radiation-induced permanent damage, particularly in the wide-pulse environment, but it was not clear if the failure

mechanism was due to total-dose or radiation-induced latch-up. In one case, an anomalous photoresponse was observed, but the overall results were not conclusive.

Results on radiation effects in basic I^2L logic cells are presented in Section 3 of this report. Preliminary data are presented on the neutron-induced displacement damage, total-ionizing-radiation-dose-induced permanent damage and transient photoresponse on basic gate and flip-flop cells of developmental I^2L LSI. Results suggest that the critical neutron fluence levels for I^2L arrays are on the order of 10^{13} - 10^{14} n/cm^2 (1 MeV equivalent). Total-dose effects characterization was limited to an overall performance evaluation of R-S flip-flop samples up to an exposure of 1 Mrad(Si) with no observable degradation in flip-flop performance at design bias current levels. Transient photoresponse upset levels, measured by the radiation-induced change of state on flip-flops, were on the order of 5×10^8 to 5×10^9 rads(Si)/s for both narrow-pulse and wide-pulse ionizing radiation environments. These results present a preliminary evaluation of I^2L susceptibility and will be followed by continued study.

Results on radiation effects in optical couplers are presented in Section 4 of this report. Transient photoresponse was characterized on both a basic diode/diode optical coupler as well as a coupler in which the input light-emitting diode is coupled to an MSI analog/digital microcircuit. Electrical characteristics and transient photoresponse of the diode/diode coupler are presented in terms of a radiation-inclusive model since a transient logic upset failure level would be very system dependent. In the case of the diode/gate coupler, the transient upset level was quite low compared to that of digital MSI, as would be expected due to the

sensitivity of the basic PIN diode optical detector. Because of the high sensitivity it was difficult to accurately determine the failure level. It was approximately 10^6 - 10^7 rads(Si)/s in the narrow-pulse flash x-ray, and approximately 10^5 - 10^6 rads(Si)/s in the wide-pulse linear accelerator environment. The transient photoresponse of the diode/gate coupler was quite complex at exposure levels above the logic upset level, and in some cases, susceptible to permanent damage.

Permanent damage effects due to total ionizing radiation dose and neutron displacement damage were measured on the diode/gate couplers. No significant permanent damage due to total ionizing radiation dose was observed after exposure up to 2 Mrads(Si). Observed neutron degradation effects were a straightforward degradation in sensitivity which, at the manufacturer's specification, would be critical at exposure levels of 1 to 5 x 10^{13} n/cm^2.

Results on synergistic effects of simultaneous electrical pulsed overstress and pulsed ionizing radiation exposure are presented in Section 5 of this report in terms of bulk CMOS latch-up. Results show that synergistic effects exist in bulk CMOS latch-up, but that there is no dramatic (i.e., greater than a factor of two) synergistic decrease in either critical electrical overstress or radiation dose rate levels necessary to include latch-up.

2.0 HIGH RELIABILITY CMOS STUDY*

Five types of junction-isolated CMOS microcircuits were selected for characterization of total-dose-induced permanent damage and transient photoresponse. Four of these were selected from a group suggested by the Technical Monitor at the Air Force Weapons Laboratory and are representative of high-reliability array requirements of current systems under development. The fifth CMOS microcircuit type selected for characterization was a commercial micropower phase-locked loop. The phase-locked loop was selected as representative of performance requirements and transistor effects which may not yet have been encountered in strictly digital CMOS arrays. The CMOS array types characterized in this study were:

CD4023A Triple 3-input NAND Gate
CD4025A Triple 3-input NOR Gate
CD4030A Quad Exclusive-OR Gate
CD4027A Dual J-K Flip-Flop
CD4046A Micropower Phase-Locked Loop

Twenty samples were obtained of each array type to a variety of specifications - commercial, high reliability, and very high reliability. The very high reliability specification was RCA No. 1970891 and the high reliability specification was RCA No. 2260600, as suggested by the AFWL Technical Monitor. The more severe specification requires 100% testing and scanning electron microscope inspection, which are relaxed somewhat in degree for the less severe specification with the requirement of SEM inspection omitted. The principal concern in the characterization was for the very high reliability arrays, but because of limitations in

*See Note on page 73.

supply, samples of the high reliability arrays were included. The mixed sample set could have been helpful in determining possible effects of the screening on the radiation susceptibility, but results obtained did not establish any convincing trend.

Characterization of total ionizing dose permanent damage effects in CMOS microcircuits is complex because of the number of independent parameters that must be considered. These parameters include: 1) exposure under either static or dynamic bias conditions; 2) determination of worst-case input bias conditions for static or dynamic sequency operation during exposure; and 3) definition of circuit bias and performance parameters for evaluation of radiation-induced permanent damage. All total ionizing radiation dose exposures in this study were conducted in the NRTC cobalt-60 hot cell environment with a supply voltage (V_{DD}) of +10V. Samples of each array type were exposed under static and dynamic operation during exposure, with the logic states selected to represent all modes of array operation. Electrical performance parameters used to monitor damage to the arrays included the dc parameters for each logic output state, minimum supply voltage, and power supply current as well as electrical switching performance.

The transient photoresponse and power-supply photocurrent were measured for each of the microcircuit types in the 2 MeV narrow-pulse and IRT linac wide-pulse ionizing radiation environments. Initially, the photoresponse of a single sample was measured under all meaningful static logic input bias conditions in the flash x-ray to determine the worst-case. Four additional samples were then exposed in the worst-case bias condition(s) in the flash x-ray to get some statistical representation in the transient upset logic levels. Supply voltage (V_{DD}) for

all measurements was +10V. Samples of each array type were then exposed to the wide-pulse linac environment under both static and dynamic operating conditions. No latch-up or anomalous photoresponse was observed in any of the samples in the flash x-ray environment for exposures of up to 5×10^{10} rads(Si)/s, but anomalous photoresponse was noted in some cases as a result of the wide-pulse linac exposures. Results include the transient logic upset level as a function of radiation pulse-width and the worst-case logic state as well as the power supply photocurrent. It is interesting to note that the worst-case logic state for transient upset is not necessarily the same as that for power-supply photocurrent.

Results of the observed transient and permanent damage failure levels for all five CMOS array types are summarized in Table 2-1. In the following discussion, these results are presented in detail for each array type.

2.1 CD4023A Triple 3-Input NAND Gate Study

The CD4023A 3-input NAND gate is a junction-isolated CMOS array with three independent gates on a single monolithic chip.[1] Ten samples of the CD4023A were obtained to RCA Specification 1970891-120 in addition to the samples obtained to RCA Specification 2260600-120. The schematic diagram of a single NAND gate is shown in Figure 2-1.

Observed results on total ionizing dose and transient photoresponse susceptibility are summarized in Table 2-2. The range in data reflects the worst-case observations over all conditions of microcircuit static bias and dynamic operation.

TABLE 2-1. SUMMARY OF OBSERVED CMOS SUSCEPTIBILITY

	Total Ionizing Dose rads(Si)	Narrow-Pulse Dose Rate rads(Si)/s	Wide-Pulse Dose Rate rads(Si)/s
CD4023A Triple 3-Input NAND Gate	$0.7 - 5.8 \times 10^6$	$0.9 - 1.5 \times 10^9$	$\sim 2.0 \times 10^8$
CD4025A Triple 3-Input NOR Gate	$0.12 - 10.0 \times 10^6$	$1.5 - 2.0 \times 10^9$	$0.8 - 1.0 \times 10^8$
CD4030A Quad 2-Input Exclusive-OR Gate	$0.10 - 2.7 \times 10^6$	$1.0 - 3.0 \times 10^9$	$0.7 - 1.0 \times 10^8$
CD4027A Dual J-K Flip-Flop	$1.5 - 2.9 \times 10^6$	$0.6 - 1.5 \times 10^9$	$\sim 0.9 \times 10^8$
CD4046A Micropower Phase-Locked Loop	$6.3 - 7.5 \times 10^4$	$1.0 - 5.0 \times 10^8$	$\sim 1.0 \times 10^7$

V_{DD} = +10V in all cases.

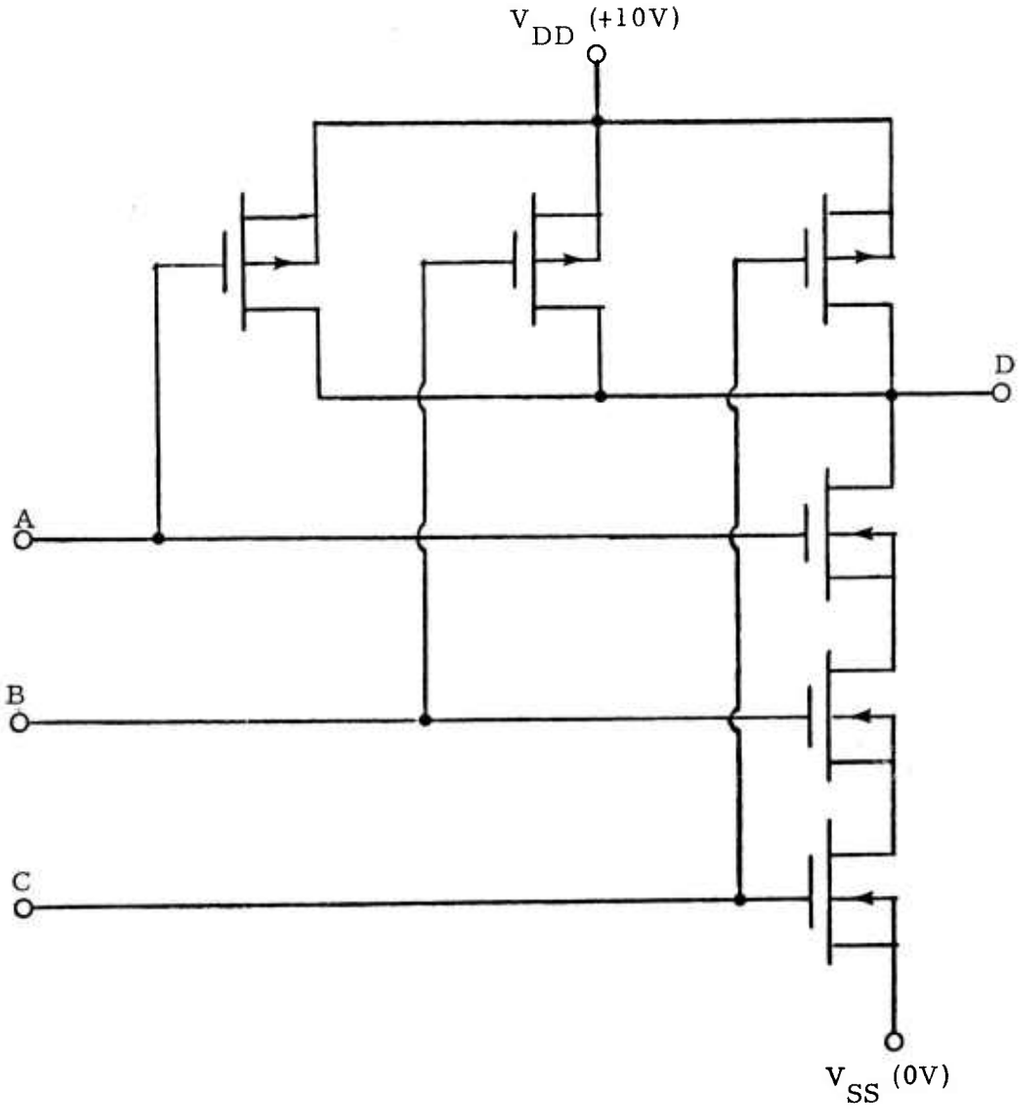


Figure 2-1. CD4023A 3-input NAND gate schematic.

TABLE 2-2. SUMMARY OF OBSERVED RADIATION SUSCEPTIBILITY - CD4023A

Transient Photoresponse

Narrow Radiation Pulse (t_p = 30 ns)

4 samples, 12 gates

$0.9 \times 10^9 \leq \dot{\gamma}_c \leq 1.5 \times 10^9$ rads(Si)/s

Wide Radiation Pulse (t_p = 4.5 μs)

4 samples, 12 gates

$\dot{\gamma}_c \cong 2 \times 10^8$ rads(Si)/s

Total Ionizing Radiation Dose

Cobalt-60 exposure at 20 krads(Si)/hour

6 samples, 18 gates

$0.7 \times 10^6 \leq \gamma_c \leq 5.8 \times 10^6$ rads(Si)

2.1.1 CD4023A Total-Ionizing-Radiation-Induced Permanent Damage. A total of six samples of the CD4023A were exposed to the ionizing radiation environment of the NRTC cobalt-60 hot cell. The six samples represented 18 samples of the individual 3-input NAND gates. Bias condition during exposure represented the three most critical static operating conditions as well as dynamic operation, as shown below:

Input Signal Conditions			Gate Types Exposed	
			891-VHR	600 HR
0	0	0	2	2
1	1	0	2	2
1	1	1	2	2
dynamic			3	3

All 18 gates were exposed simultaneously with the logic inputs of 12 gates under static bias and the inputs of the remaining six gates exercised with a 100 kHz square-wave signal. Under the test matrix, as shown above, the output logic level for one of the three static input bias conditions is a logical "0" and the two remaining static input bias conditions give a logic "1" level output. One output each from the two clocked input arrays was monitored during exposure. The total exposure time was divided into a number of shorter exposure intervals, after which, static and dynamic performance measurements were made to determine the degradation of critical parameters. Performance characterization tests consisted of measurement of the dc voltage transfer characteristic, output current-voltage characteristics, and dynamic logical operation. The critical dose for failure was defined as the total ionizing dose exposure resulting in the reduction of critical parameter values by 67% of the initial value. The critical parameters for the failure definition were the input voltage required to get to the 50% point in output voltage on the voltage transfer characteristic (i.e., threshold input voltage), and the output current in the static "0" and "1" states measured at the input threshold voltage. The worst-case total dose failure levels observed are summarized in Table 2-3 with the appropriate bias conditions.

2.1.2 CD4023A Narrow-Pulse Transient Photoresponse. Four arrays, or 12 NAND gates, of the CD4023A triple 3-input NAND gate were exposed to the ionizing radiation environment of the NRTC 2 MeV flash x-ray. Two arrays each of the very-high-reliability and high-reliability microcircuits were exposed under the static logic bias conditions as shown below,

TABLE 2-3. TEST CONDITIONS AND CRITICAL DOSE FOR CMOS Co-60 TOTAL DOSE SUSCEPTIBILITY CHARACTERIZATION

	Input Signal Conditions	Sample Types	Critical Dose (γ_c) Rads(Si)
CD4023A	0 0 0	. . .600	$2.2 - 2.7 \times 10^6$
	1 1 0	. . .600	$2.2 - 2.7 \times 10^6$
	1 1 1	. . .600	$0.7 - 1.7 \times 10^6$
	0 0 0	. . .600	$5.8 - 7.9 \times 10^6$
	1 1 0	. . .600	$5.8 - 7.9 \times 10^6$
	1 1 1	. . .600	$0.7 - 1.7 \times 10^6$
	0 0 0	. . .891	$2.2 - 2.7 \times 10^6$
	1 1 0	. . .891	$2.2 - 2.7 \times 10^6$
	1 1 1	. . .891	$2.2 - 2.7 \times 10^6$
	0 0 0	. . .891	$>10^7$
	1 1 0	. . .891	$5.8 - 7.9 \times 10^6$
	1 1 1	. . .891	$>10^7$
	Dynamic		
	1/0	. . .600	$2.2 - 2.7 \times 10^6$
	1/0	. . .600	$2.2 - 2.7 \times 10^6$
	1/0	. . .600	$2.2 - 2.7 \times 10^6$
	1/0	. . .891	$>10^7$
	1/0	. . .891	$>10^7$
	1/0	. . .891	$>10^7$

Input Signal Conditions			Gate Types Exposed	
			...891-VHR	...600 HR
0	0	0	2	2
1	1	0	2	2
1	1	1	2	2

The power supply voltage (V_{DD}) was +10V in all cases. One of the three selected input bias conditions provided a "0" logic output, while the two other input logic combinations provided a "1" logic output. In this study, a transient logic error is defined as a transient output signal sufficient in magnitude to cause a logic error in a driven gate as based on the 50% output-voltage point in the dc transfer characteristic of the gate. The test circuit used in the measurement of the transient photoresponse is presented in Appendix B.

In general, the "0"-state transient failure threshold was considerably less than that observed for the "1" output state. The overall failure range in the worst-case is then determined as between 0.9 to 1.5 x 10^9 rads(Si)/s. Specific results in the worst-case input logic condition were as follows:

Input Signal Condition			Gate Type	Critical Dose Rate rads(Si)/s
1	1	1	...600 HR	0.9 - 1.0 x 10^9
1	1	1	...600 HR	1.0 - 1.5 x 10^9
1	1	1	...891 VHR	1.0 - 1.5 x 10^9
1	1	1	...891 VHR	1.0 - 1.5 x 10^9

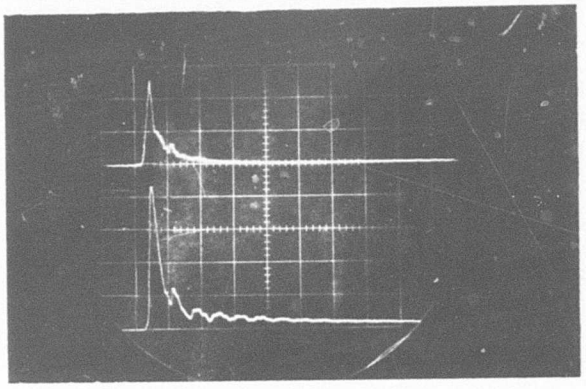
Typical output waveforms are presented in Figure 2-2. No latch-up or anomalous photoresponse was observed for exposures up to 5 x 10^{10} rads(Si)/s.

(a)

$\hat{\dot{\gamma}} \cong 9 \times 10^{8}$ rads(Si)/s

e_o = 1 V/div.

t = 0.1 μs/div.



(b)

$\dot{\gamma} \cong 1 \times 10^{10}$ rads(Si)/s

e_o = 5 V/div.

t = 0.5 μs/div.

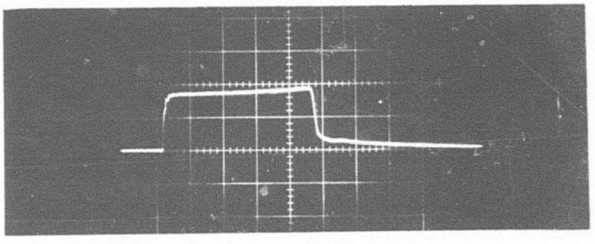


Figure 2-2. CD4023A narrow-pulse photoresponse waveforms, input bias 1-1-1, 0-output state.

In addition to the measurement of the output transient photoresponse, the power supply photocurrent was measured on two samples in the 2 MeV flash x-ray narrow-pulse environment. The measurements were taken at two radiation dose rates (5×10^8 and 2×10^9 rads(Si)/s) near the observed transient logic upset level, for the three critical static input bias conditions. The power supply voltage (V_{DD}) was set at +10V. Measured results are summarized in Table 2-4. It is interesting to note that the worst-case input bias condition for the power supply photocurrent (i.e., all zero inputs) is different than that determined for the transient logic upset (i.e., all one's input). This can be a significant consideration in determining the transient upset level in a practical CMOS subsystem since logic upset could be the result of either the direct effect on the microcircuits, or the result of a power supply voltage transient resulting from the cumulative power supply photocurrent surge.

TABLE 2-4. POWER SUPPLY PHOTOCURRENT WITH INPUT COMBINATIONS FOR TWO DOSE-RATE LEVELS

Input Combinations			Gamma Dose Rate (rads(Si)/s) 5×10^8	2×10^9
Sample #1				
0	0	0	50 mA	260 mA
1	1	1	44 mA	96 mA
1	1	0	48 mA	115 mA
1	0	0	48 mA	140 mA
Sample #2				
0	0	0	46 mA	155 mA
1	1	1	40 mA	82 mA
1	1	0	45 mA	96 mA
1	0	0	23 mA	105 mA

2.1.3 CD4023A Wide-Pulse Transient Photoresponse. Twelve gates from four CD4023A samples were exposed to the wide-pulse ionizing radiation environment of the IRT linear accelerator. The transient output photoresponse was measured for the same three static input bias conditions studied in the narrow-pulse flash x-ray measurements. The purpose of these experiments was to determine the steady-state output photoresponse of the gates using the 4.5 μs linac ionizing radiation pulse. It was determined that the worst-case for transient logic upset was the 1-1-1 input condition which set the output in the 0-state in the flash x-ray experimental results. The output photoresponse, however, was very complex, particularly at ionizing radiation levels above the worst-case failure threshold. The results in terms of peak output photoresponse may be somewhat misleading since equilibrium or steady-state outputs were not generally obtained even with the 4.5 μs wide ionizing radiation pulse. The worst-case transient upset level over the range of exposures for the four gates was approximately 2×10^8 rads(Si)/s. Detailed results on the radiation exposures are summarized in Table 2-5. Typical waveforms for the worst-case logic condition are shown in Figure 2-3 for the worst-case 1-1-1 input state and in Figure 2-4 for the 0-0-0 input state.

2.2 CD4025A Triple 3-Input NOR Gate Study

The CD4025A 3-input NOR gate is a junction-isolated CMOS array with three independent gates on a single monolithic chip.[2] Ten samples of the CD4025A were obtained to RCA Specification 1970891-121 in addition to the ten samples obtained to RCA Specification 2260600-121. The schematic diagram of a single NOR gate is shown in Figure 2-5.

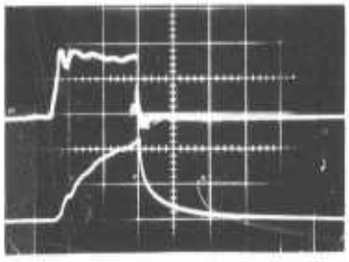
TABLE 2-5. SUMMARY OF CD4023A WIDE-PULSE PHOTORESPONSE MEASUREMENTS

Gate Sample	Input Bias	Output State	Peak Photoresponse		Comments
			Δe_o, V	$\dot{\gamma}$, rads(Si)/s	
8A-1	1 1 1	0	9.0	2×10^9	See Figure 2-3 (c)
8A-1	1 1 1	0	8.0	4.3×10^8	
8A-1	1 1 1	0	4.4	3.4×10^8	
8A-1	1 1 1	0	1.8	1.6×10^8	
8B-1	1 1 1	0	9.0	1.4×10^9	See Figure 2-3 (d)
8B-1	1 1 1	0	3.4	2.3×10^8	
9A-1	1 1 1	0	8.0	2.9×10^9	
9A-1	1 1 1	0	2.8	2.1×10^8	
9A-1	1 1 1	0	8.0	1.8×10^8	See Figure 2-3 (b)
9B-1	1 1 1	0	9.0	5×10^8	
9B-1	1 1 1	0	8.5	2.5×10^8	
9B-1	1 1 1	0	4.4	2.5×10^8	See Figure 2-3 (a)
9B-1	1 1 1	0	1.6	1.4×10^8	
8A-2	1 1 0	1	-4.4	1.3×10^9	See Figure 2-4 (c)
8A-2	1 1 0	1	-2.8	4.3×10^8	
8A-2	1 1 0	1	-0.5	3.4×10^8	
8B-2	1 1 0	1	-5.2	1.4×10^9	
8B-2	1 1 0	1	-0.9	9.0×10^8	
9A-2	1 1 0	1	-4.8	1.8×10^9	
9A-2	1 1 0	1	-0.4	2.1×10^8	See Figure 2-4 (a)
9A-2	1 1 0	1	-1.8	1.8×10^8	
9B-2	1 1 0	1	-5.6	2.5×10^9	
9B-2	1 1 0	1	-4.4	5.0×10^8	

Table 2-5. Continued

Gate Sample	Input Bias	Output State	Peak Photoresponse Δe_o, V	Peak Photoresponse $\dot{\gamma}$, rads(Si)/s	Comments
9B-2	1 1 0	1	-1.0	2.5×10^8	
9B-2	1 1 0	1	-0.4	1.4×10^8	
8A-3	0 0 0	1	-4.4	1.3×10^9	See Figure 2-4 (d)
8A-3	0 0 0	1	-3.0	4.3×10^8	
8A-3	0 0 0	1	-0.6	3.4×10^8	
8A-3	0 0 0	1	-0.2	3.4×10^8	
8B-3	0 0 0	1	-5.8	1.4×10^9	
8B-3	0 0 0	1	-0.9	2.3×10^8	
9A-3	0 0 0	1	-4.8	1.8×10^9	
9A-3	0 0 0	1	-0.6	2.1×10^8	See Figure 2-4 (b)
9A-3	0 0 0	1	-2.0	1.8×10^8	
9B-3	0 0 0	1	-5.6	2.5×10^9	
9B-3	0 0 0	1	-4.8	5.0×10^8	
9B-3	0 0 0	1	-1.0	2.5×10^8	
9B-3	0 0 0	1	-0.4	1.4×10^8	

(a)



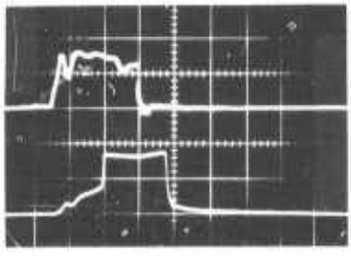
Sample #9B-1

$\hat{\dot{\gamma}} \cong 2.5 \times 10^{8}$ rads(Si)/s

$\hat{e}_o \cong 4.4V$

t = 1 μs/div.

(b)



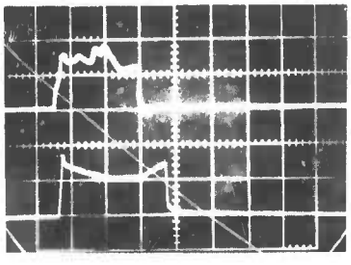
Sample #9A-1

$\hat{\dot{\gamma}} \cong 1.8 \times 10^{8}$ rads(Si)/s

$\hat{e}_o \cong 8V$

t = 1 μs/div

(c)



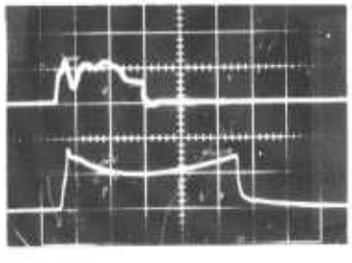
Sample #8A-1

$\hat{\dot{\gamma}} \cong 2 \times 10^{9}$ rads(Si)/s

$\hat{e}_o \cong 9V$

t = 2 μs/div.

(d)



Sample #8B-1

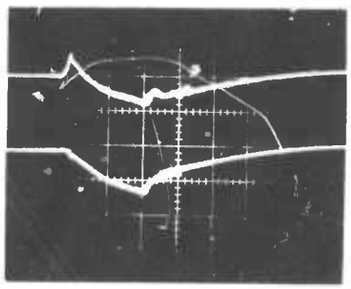
$\hat{\dot{\gamma}} \cong 1.4 \times 10^{9}$ rads(Si)/s

$\hat{e}_o \cong 9V$

t = 2 μs/div.

Figure 2-3. CD4023 0-state wide-pulse photoresponse waveforms.

Input		Bias
1	1	0
0	0	0

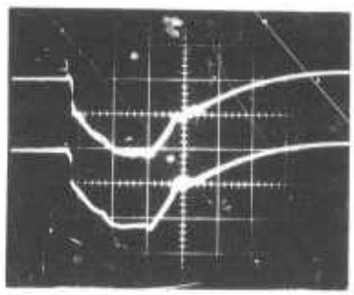


(a) Sample #9A-2

(b) Sample #9A-3

e_o = 0.5 V/div; t = 2 μs/div.

Input		Bias
1	1	0
0	0	0



(c) Sample #8A-2

(d) Sample #8A-3

e_o = 2 V/div; t = 2 μs/div.

Figure 2-4. CD4023 1-state wide-pulse photoresponse waveforms.

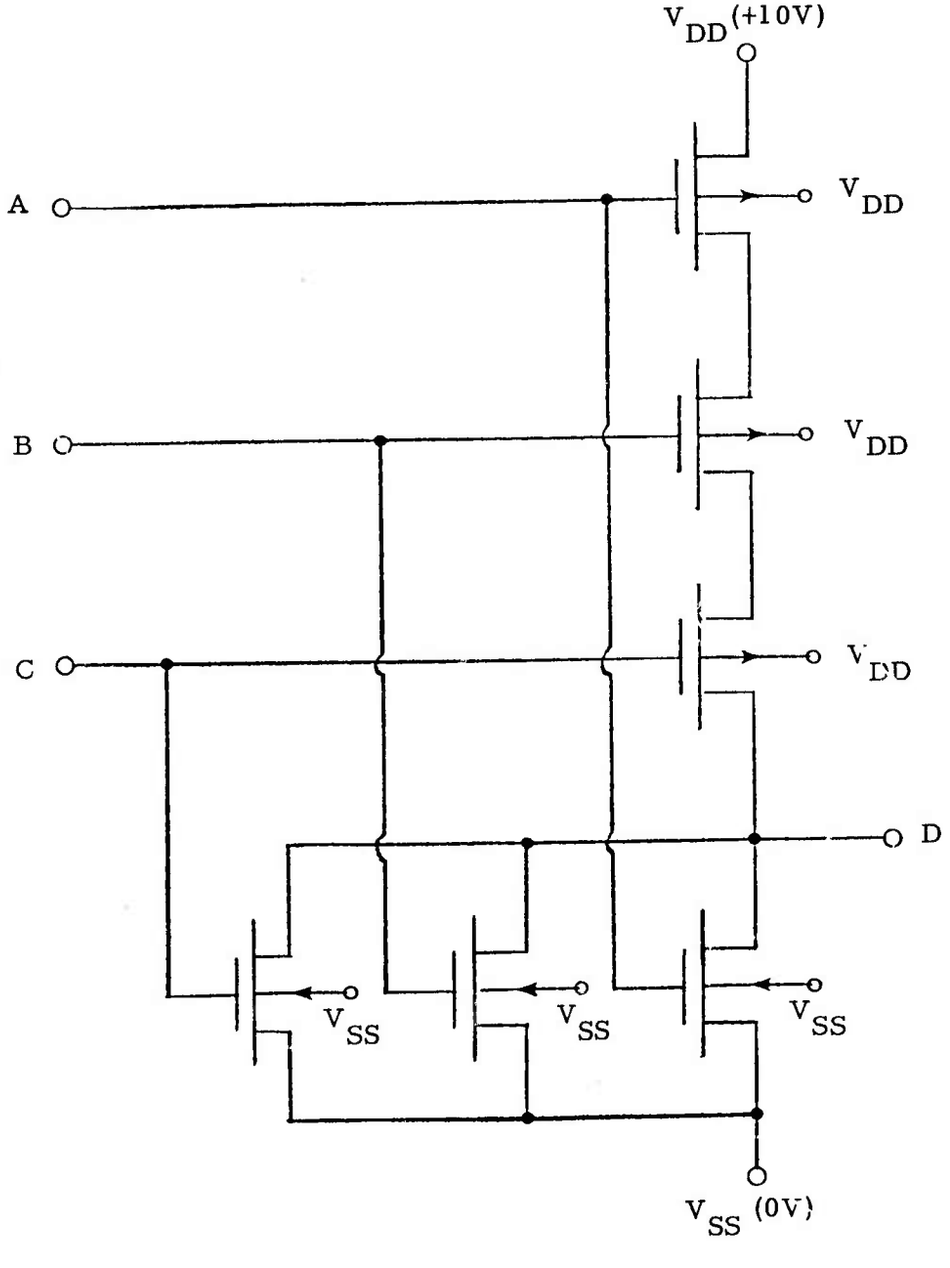


Figure 2-5. CD4025A 3-input NOR gate schematic.

Observed results on total ionizing dose and transient photoresponse susceptibility are summarized in Table 2-6. The range in data reflects the worst-case observations over all conditions of microcircuit static bias and dynamic operation.

TABLE 2-6. SUMMARY OF OBSERVED CD4025A RADIATION SUSCEPTIBILITY

Pulsed Ionizing Radiation

Narrow-Pulse Transient Failure Level ($t_p \cong 30$ ns)

4 microcircuits/12 gates

$1.5 \leq \dot{\gamma}_c \leq 2 \times 10^9$ rads(Si)/s

Wide-Pulse Transient Failure Level ($t_p \cong 4.5$ μs)

4 microcircuits/12 gates

$0.8 \leq \dot{\gamma}_c \leq 1.0 \times 10^8$ rads(Si)/s

Total Ionizing Radiation Dose

Co-60 Exposure at 20 krads(Si)/hr

6 microcircuits/18 gates

$1.2 \times 10^5 \leq \gamma_c \leq 10^7$ rads(Si)

2.2.1 CD4025A Total-Ionizing-Radiation-Induced Permanent Damage. A total of six samples of the CD4025A were exposed to the ionizing radiation environment of the NRTC Co-60 hot cell. The six samples represented 18 samples of the individual 3-input NOR gates. Bias condition during exposure represented the three most critical static operating

conditions as well as dynamic operation as shown below,

Input Signal Conditions			Gate Types Exposed ... 891-VHR	... 600 HR
0	0	0	2	2
1	0	0	2	2
1	1	1	2	2
dynamic			3	3

All 18 gates were exposed simultaneously with the logic inputs of 12 samples under static bias and the inputs of the remaining 6 samples exercised with a 100 kHz square-wave signal. Under the test matrix, as shown above, the output logic level for one of the three static input bias conditions is a logical "1" and the two remaining static input bias give a logical "0" output level. One output each from two clocked input gates were monitored during ionizing radiation exposure. The total exposure time was divided into a number of shorter exposure intervals, after which static and dynamic measurements were made to determine the degradation of critical parameters. Performance characterization tests consisted of the measurement of the dc voltage transfer characteristic, dc output current-voltage characteristics, and dynamic logic operation on each gate. The critical ionizing radiation dose at failure in this study was defined as the total ionizing dose exposure resulting in the reduction of critical parameter values by 67% of the initial value. The critical parameters for the failure definition were the input voltage required to get to the 50% point in the output voltage on the voltage transfer characteristic, and the output current in the static "0" and "1" states at that value of input voltage. The worst-case total dose failure levels observed are summarized in Table 2-7 with the appropriate bias conditions.

TABLE 2-7. TEST CONDITIONS AND CRITICAL DOSE FOR CMOS Co-60 TOTAL DOSE SUSCEPTIBILITY CHARACTERIZATION

	Input Signal Conditions	Sample Types	Critical Dose (γ_c) Rads(Si)
CD4025A	0 0 0	. . .600	120 - 140K
	1 0 0	. . .600	120 - 140K
	1 1 1	. . .600	120 - 140K
	0 0 0	. . .600	120 - 140K
	1 0 0	. . .600	120 - 140K
	1 1 1	. . .600	120 - 140K
	0 0 0	. . .891	$>10^7$
	1 0 0	. . .891	$>10^7$
	1 1 1	. . .891	$>10^7$
	0 0 0	. . .891	$>10^7$
	1 0 0	. . .891	$>10^7$
	1 1 1	. . .891	$>10^7$
	Dynamic		
	1/0	. . .600	120 - 140K
	1/0	. . .600	120 - 140K
	1/0	. . .600	120 - 140K
	1/0	. . .891	$>10^7$
	1/0	. . .891	$>10^7$
	1/0	. . .891	$>10^7$

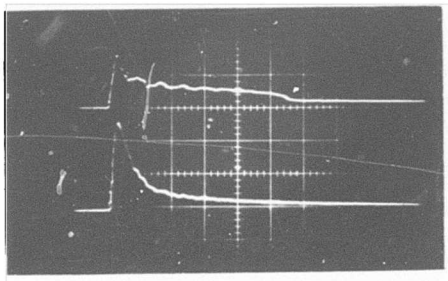
2.2.2 CD4025A Narrow-Pulse Transient Photoresponse. Four microcircuits, or 12 NOR gates of the CD4025A triple 3-input NOR were exposed to the ionizing radiation environment of the NRTC 2 MeV flash x-ray. Two arrays each of the very-high-reliability and high-reliability microcircuits were exposed under the static logic bias conditions shown below,

Input Signal Conditions			Gate Types Exposed	
			...891-VHR	...600 HR
0	0	0	2	2
1	0	0	2	2
1	1	1	2	2

The power supply voltage (V_{DD}) was +10V in all cases. One of the three selected input bias conditions provided a "high" of "1"-state level output while the two remaining input logic combinations provided a low of "0"-state logic level at the output. In this study, a transient logic error is defined as a transient output signal sufficient in magnitude to cause a logic error in a driven gate based on the 50% output-voltage-point in the dc transfer characteristics of the gate. The test circuit used in the measurement of the transient photoresponse is presented in Appendix B.

In general, the "0"-state transient failure threshold was considerably less than that observed in the "1" state. The failure range, as determined from the "0"-state output photoresponses was in the range of 1.5 to 2.0×10^{9} rads(Si)/s. Typical output waveforms are presented in Figure 2-6. No latch-up or anomalous photoresponse was observed for exposures up to 5×10^{10} rads(Si)/s.

In addition to the measurement of the output transient photoresponse, the power supply photocurrent was measured on two samples. The



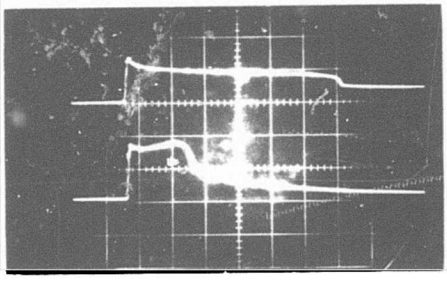
Input State 0-1-1

Input State 1-0-0

(a) $\hat{\dot{\gamma}} \cong 1 \times 10^{9}$ rads(Si)/s

e_o = 2 V/div.

t = 0.1 μs/div.



Input State 1-0-0

Input State 0-1-1

(b) $\dot{\gamma} \cong 1 \times 10^{10}$ rads(Si)/s

e_o = 5 V/div.

t = 0.5 μs/div.

Figure 2-6. CD4025A narrow-pulse photoresponse waveforms.

measurements were taken at a dose rate approximating the transient failure level (i.e., 2×10^9 rads(Si)/s) as well as at a dose rate a factor of four lower than the critical static input bias conditions at a power supply voltage of +10V. Measured results are summarized in Table 2-8. As was the case with the CD4023, the worst-case for logic upset is not the worst-case for power supply photocurrent.

TABLE 2-8. POWER SUPPLY PHOTOCURRENT WITH INPUT COMBINATIONS FOR TWO DOSE-RATE LEVELS

Input Combinations			Gamma Dose Rate (rads(Si)/s) 5×10^8	2×10^9
Sample #1				
0	0	0	60 mA	310 mA
1	1	1	33 mA	57 mA
1	1	0	52 mA	120 mA
1	0	0	60 mA	170 mA
Sample #2				
0	0	0	72 mA	300 mA
1	1	1	33 mA	48 mA
1	1	0	44 mA	140 mA
1	0	0	52 mA	180 mA

2.2.3 CD4025A Wide-Pulse Transient Photoresponse. Twelve gates from four CD4025A samples were exposed to the wide-pulse ionizing radiation environment of the IRT linear accelerator. The transient output photoresponse was measured for the same three static input bias conditions studied in the narrow-pulse flash x-ray measurements. The purpose of these experiments was to determine the steady-state output photoresponse of the gates using the 4.5 μs ionizing radiation pulse.

The transient output response was comparable in both the 0-output state and the 1-output state, unlike the CD4023A where the 0-state photoresponse was definitely the worst-case. The transient upset level was determined as approximately 0.8 to 1.0 x 10^8 rads(Si)/s with the 1-1-1 input/0-output state the most sensitive by a slight margin. Detailed results of the radiation exposures are summarized in Table 2-9, and typical output waveforms are illustrated in Figures 2-7 and 2-8.

As with the CD4023 results, the linac 4.5 μs pulse was not long enough to establish the true steady-state photoresponse of the CD4025A gates. As shown in Figure 2-7, the output photoresponse has not reached steady state at the end of the 4.5 μs pulse. Thus, the true steady-state logic upset threshold of the gates could be 10-20% less than those values observed in the linear experiments. No definitive latch-up was observed in the course of the wide-pulse exposures, but one electrical failure was observed and the output waveforms above the logic upset level are complex and suggest the possibility of anomalous photoresponse or incipient latch-up. This is illustrated by the waveforms in Figure 8(a) where the output transient voltage is still increasing after the end of the radiation pulse.

2.3 CD4030A Quad Exclusive-OR Gate Study

The CD4030A 2-input exclusive-OR gate is a junction isolated CMOS array with four independent gates on a single monolithic chip.[3] Ten samples of the CD4030 were obtained to RCA Specification 1970891-125, in addition to the ten samples obtained to RCA Specification 2260600-125. The schematic diagram of a single exclusive-OR gate is shown in Figure 2-9.

TABLE 2-9. SUMMARY OF CD4025A WIDE-PULSE PHOTORESPONSE MEASUREMENTS

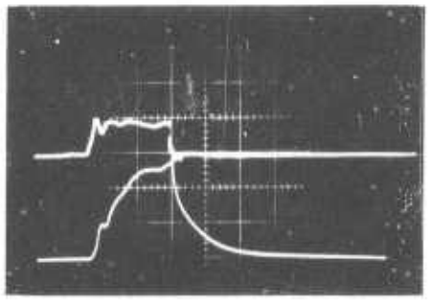
Gate Sample	Input Bias	Output State	Peak Photoresponse		Comments
			Δe_o, V	$\dot{\gamma}$, rads(Si)/s	
8A-1	1 1 1	0	+8.5	1.1×10^9	
8A-1	1 1 1	0	+8.0	3.8×10^8	
8A-1	1 1 1	0	+8.0	1.4×10^8	
8B-1	1 1 1	0	+8.0	1.6×10^9	
8B-1	1 1 1	0	+9.0	6.0×10^8	See Figure 2-8 (a)
8B-1	1 1 1	0	+5.6	1.1×10^8	See Figure 2-7 (a)
8B-1	1 1 1	0	+0.7	4.0×10^7	
9A-1	1 1 1	0	+9.0	1.2×10^9	
9A-1	1 1 1	0	+8.0	3.3×10^8	
9A-1	1 1 1	0	+8.0	1.4×10^8	
9A-1	1 1 1	0	+3.6	6.2×10^7	
9B-1	1 1 1	0	+9.0	1.1×10^9	
9B-1	1 1 1	0	+9.0	5.0×10^8	
9B-1	1 1 1	0	+7.0	1.4×10^8	
9B-1	1 1 1	0	+4.0	7.8×10^7	
8A-2	1 0 0	0	+6.4	1.1×10^9	
8A-2	1 0 0	0	+6.2	3.8×10^8	
8A-2	1 0 0	0	+4.4	1.4×10^8	
8B-2	1 0 0	0	+6.5	1.6×10^9	
8B-2	1 0 0	0	+6.5	6.0×10^8	See Figure 2-8 (b)
8B-2	1 0 0	0	+3.4	1.1×10^8	See Figure 2-7 (b)
8B-2	1 0 0	0	+0.7	4.0×10^7	
9A-2	1 0 0	0	+6.2	1.2×10^9	

Table 2-9 Continued

Gate Sample	Input Bias	Output State	Peak Photoresponse Δe_o, V	Peak Photoresponse $\dot{\gamma}$, rads(Si)/s	Comments
9A-2	1 0 0	0	+6.2	3.3×10^8	
9A-2	1 0 0	0	+4.6	1.4×10^8	
9A-2	1 0 0	0	+1.9	6.2×10^7	
9B-2	1 0 0	0	+6.4	1.1×10^9	
9B-2	1 0 0	0	+6.4	5.0×10^8	
9B-2	1 0 0	0	+2.0	7.8×10^7	
8A-3	0 0 0	1	-4.4	3.8×10^8	
8A-3	0 0 0	1	-4.0	1.4×10^8	** electrical failure after next shot
8B-3	0 0 0	1	-8.0	1.1×10^9	
8B-3	0 0 0	1	-8.0	6.0×10^8	See Figure 2-8 (c)
8B-3	0 0 0	1	-3.6	1.1×10^8	See Figure 2-7 (c)
8B-3	0 0 0	1	-0.2	4.0×10^7	
9A-3	0 0 0	1	-8.6	1.2×10^9	
9A-3	0 0 0	1	-8.2	3.3×10^8	
9A-3	0 0 0	1	-4.0	1.4×10^8	
9A-3	0 0 0	1	-2.6	6.2×10^7	
9B-3	0 0 0	1	-8.0	1.1×10^9	
9B-3	0 0 0	1	-8.4	5.0×10^8	
9B-3	0 0 0	1	-2.9	7.8×10^7	

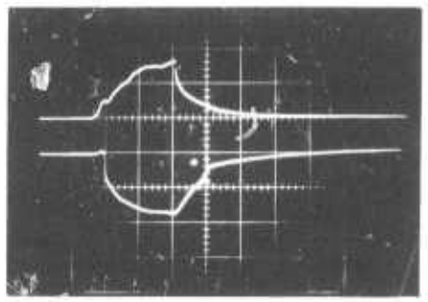
$\dot{\tilde{\gamma}} \cong 1.1 \times 10^8$ rads(Si)/s

7



(a) Input State 1-1-1

(a) Sample #8B-1



(b) Input State 1-0-0

(b) Sample #8B-2

(c) Input State 0-0-0

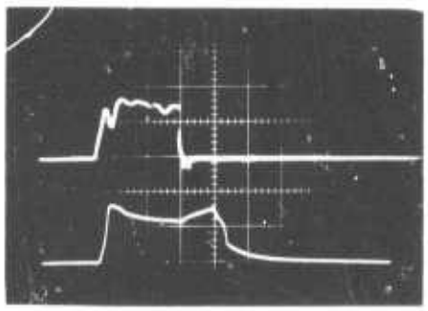
(c) Sample #8B-3

e_o = 2 V/div., t = 2 μs/div.

Figure 2-7. CD4025A wide-pulse photoresponse at transient upset dose rate.

$\hat{\dot{\gamma}} \cong 6 \times 10^{8}$ rads(Si)/s

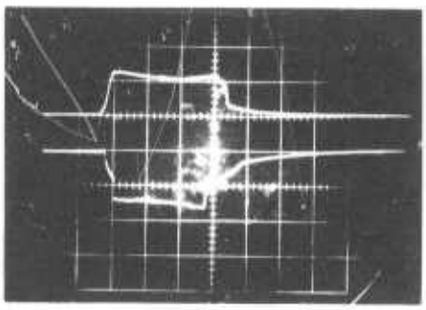
(a) Input State 1-1-1



(a) Sample #8B-1

(b) Input State 1-0-0

(c) Input State 0-0-0



(b) Sample #8B-2

(c) Sample #8B-3

e_o = 2 V/div., t = 2 μs/div.

Figure 2-8. CD4025A wide-pulse photoresponse above the upset dose rate.

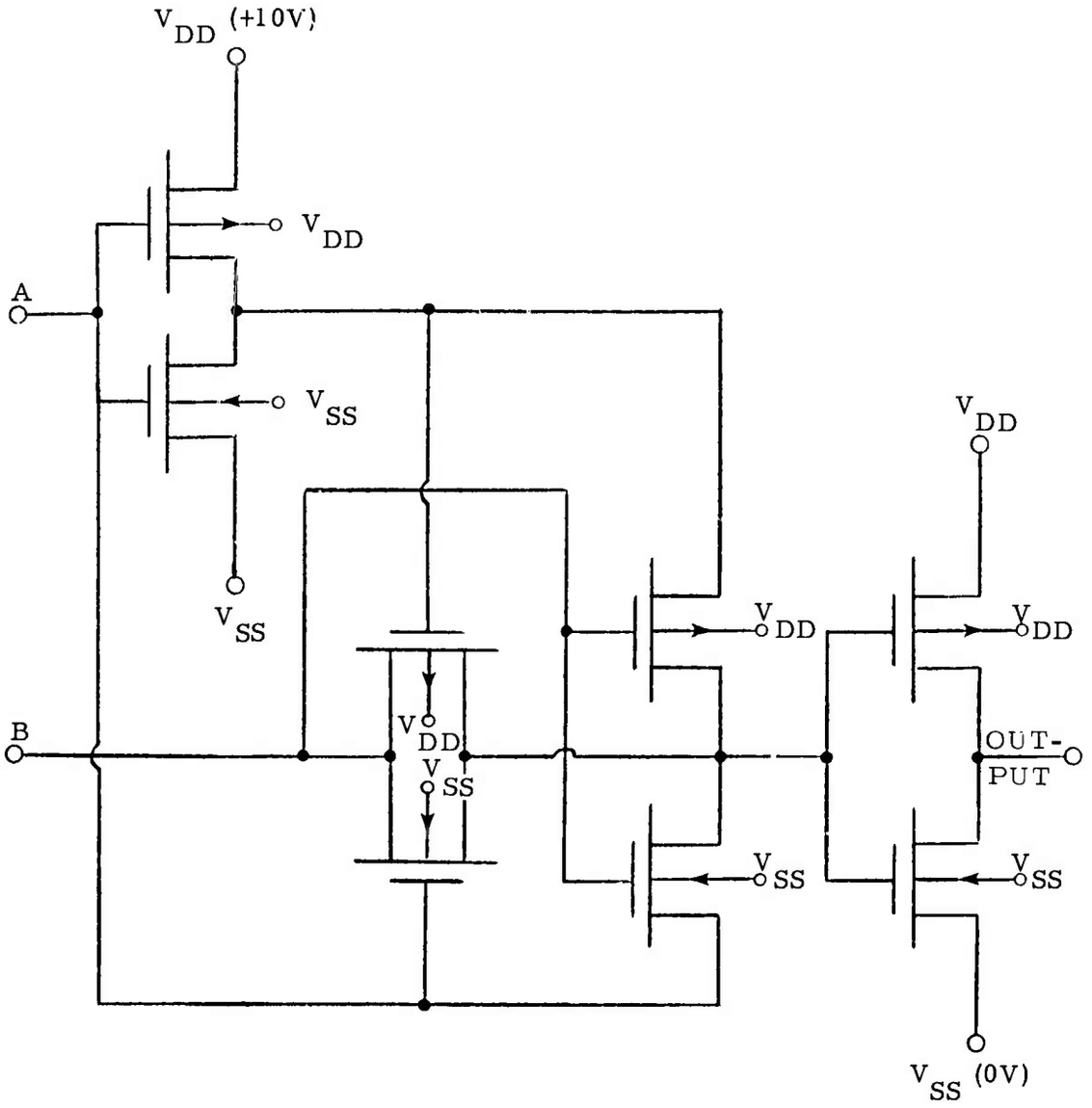


Figure 2-9. CD4030A exclusive-OR gate schematic.

Observed results on total ionizing dose and transient photoresponse susceptibility are summarized in Table 2-10. The range in data reflects the worst-case observations over all conditions of microcircuit static bias and dynamic operation.

TABLE 2-10. SUMMARY OF OBSERVED CD4030A RADIATION SUSCEPTIBILITY

Pulsed Ionizing Radiation

Narrow-pulse Transient Failure Level ($t_p \cong 30$ ns)

4 microcircuits/12 gates

$1.0 \leq \dot{\gamma}_c \leq 3.0 \times 10^9$ rads(Si)/s

Wide-pulse Transient Failure Level ($t_p \cong 4.5\ \mu$s)

4 microcircuits/12 gates

$0.7 \leq \dot{\gamma}_c \leq 1.0 \times 10^8$ rads(Si)/s

Total Ionizing Radiation Dose

Co-60 Exposure at 20 krads(Si)/hr

6 microcircuits/18 gates

$0.1 \leq \gamma_c \leq 2.7 \times 10^6$ rads(Si)

2.3.1 CD4030A Total-Ionizing-Radiation-Induced Permanent Damage. A total of six samples of the CD4030A were exposed to the ionizing radiation environment of the NRTC Co-60 hot cell. The six samples represented 24 samples of the individual 2-input exclusive-OR gates. Bias conditions during exposure represented all four possible static input bias conditions as well as dynamic operation. Two samples each of the very-high-reliability and high-reliability gates were exposed under each static

input condition, and three samples each were exposed under dynamic bias, exercised with a 100 kHz square-wave signal. One output each from the dynamically driven gates was monitored during the entire ionizing radiation exposure. The total exposure time was divided into a number of shorter exposure intervals, after which static and dynamic measurements were made to determine the degradation of critical parameters. Performance characteristization tests consisted of the measurement of the dc voltage transfer characteristic, the dc output current-voltage characteristics, and the dynamic logic operation of each gate. The critical ionizing radiation dose at failure in this study was defined as the total ionizing dose exposure resulting in the critical parameter degradation of 67% of the initial value. The critial parameters, as before, were the input voltage at the mid-point of the transfer characteristic, and the output current in the static "0" and "1" state at the value of input voltage. The worst-case total dose failure levels observed are summarized in Table 2-11 with the appropriate bias conditions.

2.3.2 CD4030A Narrow-Pulse Transient Photoresponse. Four microcircuits, or 16 samples of the CD4030A 2-input exclusive-OR gates were exposed to the ionizing radiation environment of the NRTC 2 MeV flash x-ray. Two arrays each of the high-reliability and very-high-reliability types were irradiated under all four possible static input bias conditions. The power supply voltage (V_{DD}) was +10V in all cases. For the exclusive-OR, the output is in the 1-logic state for two of the four input bias conditions, and is in the 0-logic state for the other two input logic states. No latch-up, anomalous photoresponse or radiation-induced permanent damage was observed for exposure exposure dose rates up to

TABLE 2-11. TEST CONDITIONS AND CRITICAL DOSE FOR CMOS Co-60 TOTAL DOSE SUSCEPTIBILITY CHARACTERIZATION

	Input Signal Conditions	Sample Types	Critical Dose (γ_c) Rads(Si)
CD4030A	0 0	. . .600	$2.2 - 2.7 \times 10^6$
	0 1	. . .600	$2.2 - 2.7 \times 10^6$
	1 0	. . .600	$2.2 - 2.7 \times 10^6$
	1 1	. . .600	$2.2 - 2.7 \times 10^6$
	0 0	. . .600	$2.2 - 2.7 \times 10^6$
	0 1	. . .600	$2.2 - 2.7 \times 10^6$
	1 0	. . .600	$2.2 - 2.7 \times 10^6$
	1 1	. . .600	$2.2 - 2.7 \times 10^6$
	0 0	. . .891	$1.1 - 1.4 \times 10^5$
	0 1	. . .891	$1.1 - 1.4 \times 10^5$
	1 0	. . .891	$1.1 - 1.4 \times 10^5$
	1 1	. . .891	$1.1 - 1.4 \times 10^5$
	0 0	. . .891	$1.1 - 1.4 \times 10^5$
	0 1	. . .891	$1.1 - 1.4 \times 10^5$
	1 0	. . .891	$1.1 - 1.4 \times 10^5$
	1 1	. . .891	$1.1 - 1.4 \times 10^5$
	Dynamic		
	1/0	. . .600	$2.2 - 2.7 \times 10^6$
	1/0	. . .600	$2.2 - 2.7 \times 10^6$
	1/0	. . .600	$2.2 - 2.7 \times 10^6$
	1/0	. . .600	$2.2 - 2.7 \times 10^6$
	1/0	. . .891	$1.1 - 1.4 \times 10^5$
	1/0	. . .891	$1.1 - 1.4 \times 10^5$
	1/0	. . .891	$1.1 - 1.4 \times 10^5$
	1/0	. . .891	$1.1 - 1.4 \times 10^5$

5×10^{10} rads(Si)/s. The observed transient logic upset level for each of the gates characterized is summarized below.

Sample Type	Input Logic State		Output Logic State	Critical Dose Rate rads(Si)/s
...600 HR	1	0	1	$1.0 - 2.0 \times 10^9$
...600 HR	1	0	1	$2.0 - 2.5 \times 10^9$
...600 HR	0	1	1	$1.0 - 2.0 \times 10^9$
...600 HR	0	1	1	$2.0 - 2.5 \times 10^9$
...891 VHR	1	0	1	$2.0 - 2.5 \times 10^9$
...891 VHR	1	0	1	$2.5 - 3.0 \times 10^9$
...891 VHR	0	1	1	$2.0 - 2.5 \times 10^9$
...891 VHR	0	1	1	$2.5 - 3.0 \times 10^9$

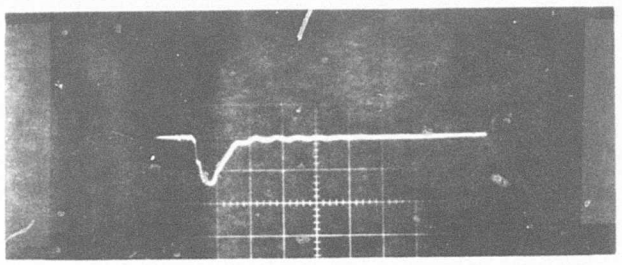
The critical dose rate for transient logic upset threshold has been defined, in this case, as that required to produce a transient voltage at the output equal in magnitude to the 50% switching input voltage of the dc transfer characteristic. In all cases, the 1-state transient failure threshold was considerably less than that observed in either input conditions for the 1-output state. The worst-case narrow-pulse logic upset level was observed, then, as approximately 1.0 to 3.0×10^9 rads(Si)/s. The upset threshold for the very-high-reliability gates was slightly higher than that observed for the high-reliability gates, but the data is insufficient to suggest that the very-high-reliability parts were significantly harder. Typical waveforms of the transient output photoresponse are shown in Figure 2-10.

(a)

$\dot{\gamma} \cong 1.5 \times 10^9$ rads(Si)/s

e_o = 2 V/div.

t = 0.1 μs/div.



(b)

$\dot{\gamma} \cong 2 \times 10^9$ rads(Si)/s

e_o = 2 V/div.

t = 0.1 μs/div.

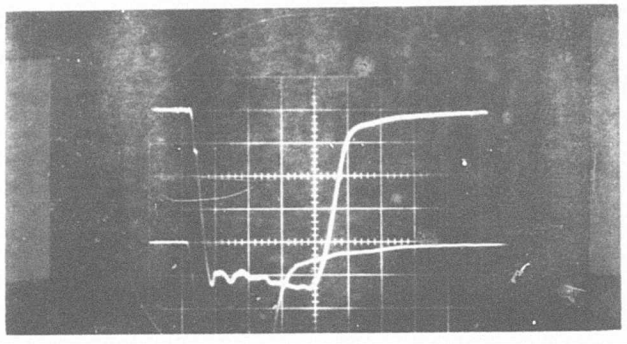


Figure 2-10. CD4030A narrow-pulse photoresponse waveforms, input bias 1-0, 1-output state.

In addition to the measurement of the output transient photoresponse the power supply photocurrent was measured on two samples. The measurements were at ionizing radiation dose rates of 5×10^8 and 2×10^0 rads(Si)/s representing the critical dose rate for logic upset, as well as an exposure at a dose rate substantially lower than that of the logic upset level. Measurements were conducted for four critical static input bias conditions at a power supply of +10V. Measured results are summarized in Table 2-12. Again, the worst-case for the transient power supply photocurrent (i.e., inputs 0 - 0) is not the same as that for the logic output upset (i.e., either 1 - 0 or 0 - 1).

TABLE 2-12. POWER SUPPLY PHOTOCURRENT WITH INPUT COMBINATIONS FOR TWO DOSE-RATE LEVELS

Input Combinations		Gamma Dose Rate (rads(Si)/s) 5×10^8	2×10^9
Sample #1			
1	1	29 mA	54 mA
1	0	34 mA	64 mA
0	1	35 mA	60 mA
0	0	50 mA	160 mA
Sample #2			
1	1	26 mA	48 mA
1	0	30 mA	70 mA
0	1	30 mA	65 mA
0	0	36 mA	215 mA

2.3.3 CD4030A Wide-Pulse Transient Photoresponse. Twelve gates from four CD4030A samples were exposed to the wide-pulse ionizing radiation environment of the IRT linear accelerator. The transient output

photoresponse was measured for the most critical three of the four possible input states (i.e., input 0-0, output 0; input 0-1, output 1; and input 1-0, output 1). Unlike either the CD4023A or CD4025A gates, the worst-case output state was the 1-state, with comparable susceptibility for the 0-1 and 1-0 input bias conditions. The transient upset level was determined as approximately $0.7 - 1.0 \times 10^8$ rads(Si)/s. Detailed results of the radiation exposures are summarized in Table 2-13, and typical output waveforms are illustrated in Figures 2-11, -12, and -13.

The transient output waveforms of the CD4030A gates were less complex than those observed on either the CD4023A or CD4025A gates, but the number of samples lost to permanent damage was much greater. Nine of the 12 gates failed during the course of the experimental study. It is not clear whether the failure was the result of radiation-induced latch-up or accumulated total-dose permanent damage affects. No anomalous waveforms were observed that would definitively point to latch-up, but the total dose on any gate did not exceed 100 krads(Si) which is much less than the total-dose failure levels observed from the Co-60 exposures. The transient output waveforms catching the moment of failure for one gate are illustrated in Figure 2-13. Gate failure is definitive, but there is no way that failure due to either latch-up or total-dose permanent damage can be identified.

2.4 CD4027A Dual J-K Master-Slave Flip-Flop Study

The CD4027A J-K flip-flop is a junction-isolated CMOS array with two independent flip-flops on a single monolithic chip.[4] Twenty samples of the CD4027A were obtained to RCA Specification 2260600-122. No

TABLE 2-13. SUMMARY OF CD4030A WIDE-PULSE PHOTORESPONSE MEASUREMENTS

Gate Sample	Input Bias	Output State	Peak Photoresponse Δe_o, V	Peak Photoresponse $\dot{\gamma}$, rads(Si)/s	Comments
8A-1	0 0	0	+0.16	1.0×10^8	
8A-1	0 0	0	+0.2	1.4×10^8	
8A-1	0 0	0	+0.32	1.7×10^8	
8A-1	0 0	0	+3.8	5.6×10^8	
8A-1	0 0	0	+9.0	2.5×10^9	
8B-1	0 0	0	+0.02	5.2×10^7	
8B-1	0 0	0	+0.04	7.2×10^7	See Figure 2-11 (a)
8B-1	0 0	0	+0.4	1.4×10^8	See Figure 2-12 (a)
8B-1	0 0	0	+10	2.1×10^9	See Figure 2-13 (a)
9A-1	0 0	0	+0.2	1.1×10^8	
9A-1	0 0	0	+0.34	1.4×10^8	
9A-1	0 0	0	+9.0	5.6×10^8	
9B-1	0 0	0	+0.09	7.6×10^7	
9B-1	0 0	0	+0.65	1.1×10^8	
9B-1	0 0	0	+1.0	1.4×10^8	
9B-1	0 0	0	+4.0	4.9×10^8	
9B-1	0 0	0	**	1.1×10^9	**Device failure
8A-2	0 1	1	-0.7	1.0×10^8	
8A-2	0 1	1	-9.0	1.4×10^8	
8A-2	0 1	1	-9.5	1.7×10^8	
8A-2	0 1	1	-9.0	7.0×10^8	
8A-2	0 1	1	**	2.5×10^9	**Device failure
8B-2	0 1	1	-1.6	5.2×10^7	

Table 2-13 Continued.

Gate Sample	Input Bias	Output State	Peak Photoresponse Δe_o, V	Peak Photoresponse $\dot{\gamma}$, rads(Si)/s	Comments
8B-2	0 1	1	-8.5	7.5×10^7	Worst-case upset level; see Figure 2-11 (b)
8B-2	0 1	1	-10	1.4×10^8	See Figure 2-12 (b)
8B-2	0 1	1	**	2.1×10^8	**Device failure; See Figure 2-13 (b)
9A-2	0 1	1	-0.9	1.1×10^8	
9A-2	0 1	1	-9.0	1.4×10^8	
9A-2	0 1	1	**	5.6×10^8	**Device failure
9B-2	0 1	1	-1.8	7.6×10^7	
9B-2	0 1	1	-8.0	1.1×10^8	
9B-2	0 1	1	-9.8	1.4×10^8	
9B-2	0 1	1	-9.5	6.0×10^8	
9B-2	0 1	1	**	1.1×10^9	**Device failure
8A-3	1 0	1	-0.5	1.0×10^8	
8A-3	1 0	1	-3.0	1.4×10^8	
8A-3	1 0	1	-9.5	1.7×10^8	
8A-3	1 0	1	-9.0	7.0×10^8	
8A-3	1 0	1	**	2.5×10^9	**Device failure
8B-3	1 0	1	-1.8	5.2×10^7	
8B-3	1 0	1	-9.0	7.5×10^7	See Figure 2-11 (c)
8B-3	1 0	1	-10	1.4×10^8	See Figure 2-12 (c)
8B-3	1 0	1	**	2.1×10^9	**Device failure; See Figure 2-13 (c)

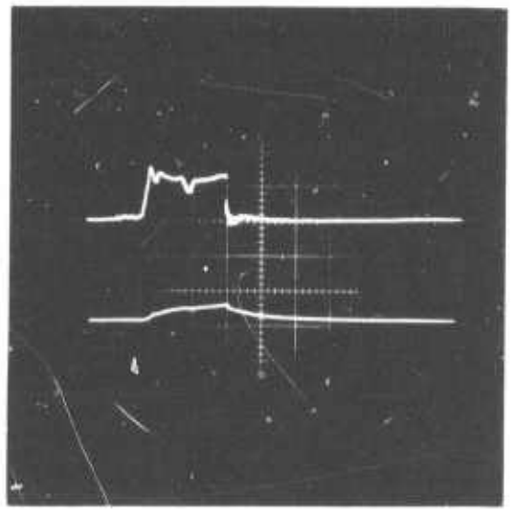
Table 2-13 Concluded.

Gate Sample	Input Bias	Output State	Peak Photoresponse		Comments
			Δe_o, V	$\dot{\gamma}$, rads(Si)/s	
9A-3	1 0	1	-1.0	1.1×10^8	
9A-3	1 0	1	-9.0	1.4×10^8	
9A-3	1 0	1	**	5.6×10^8	**Device failure
9B-3	1 0	1	-2.0	7.6×10^7	
9B-3	1 0	1	-8.0	1.1×10^8	
9B-3	1 0	1	-9.75	1.4×10^8	
9B-3	1 0	1	-9.75	6.0×10^8	
9B-3	1 0	1	**	1.1×10^9	**Device failure

$\dot{\gamma} = 7.5 \times 10^{7}$ rads(Si)/s

(a) Sample #8B-1

Inputs 0-0



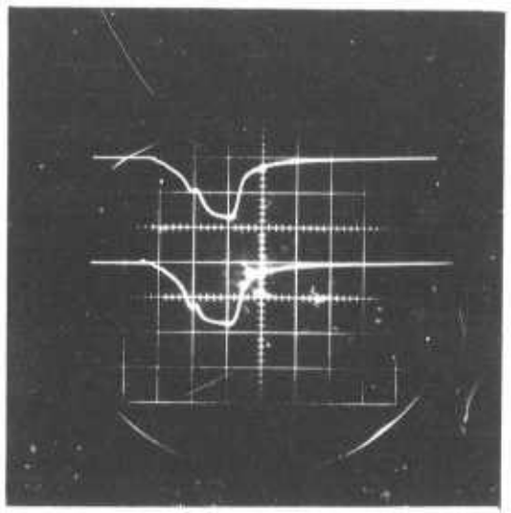
e_o = 0.1 V/div., t = 2 μs/div.

(b) Sample #8B-2

Inputs 0-1

(c) Sample #8B-3

Inputs 0-1

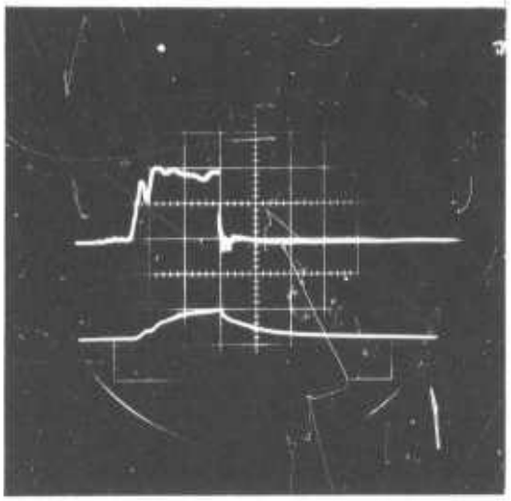


e_o = 5 V/div., t = 2 μs/div.

Figure 2-11. CD4030A wide-pulse photoresponse at the transient upset level.

$\dot{\hat{D}} = 1.4 \times 10^{8}$ rads(Si)/s

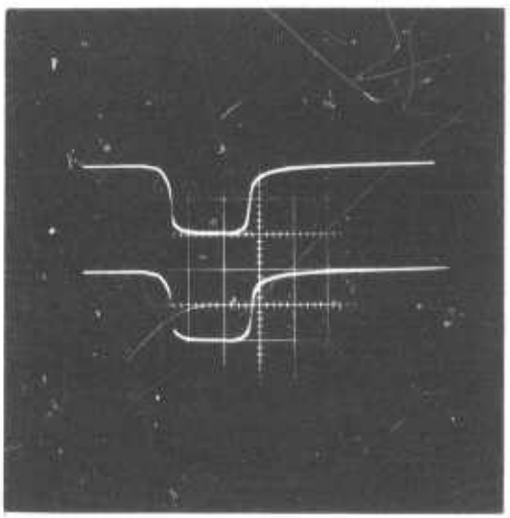
(a) Sample #8B-1



e_o = 0.1 V/div., t = 2 μs/div.

(b) Sample #8B-2

(c) Sample #8B-3

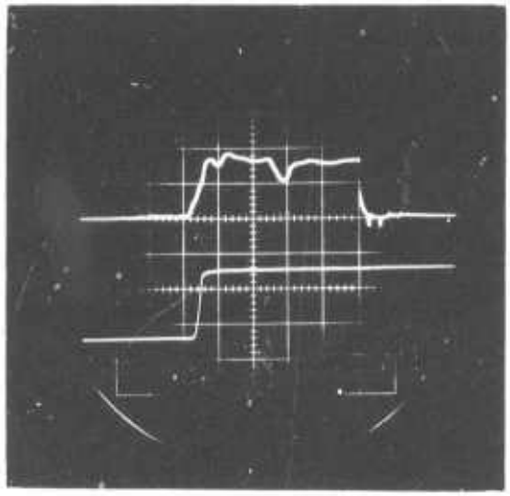


e_o = 5 V/div., t = 2 μs/div.

Figure 2-12. CD4030A wide-pulse photoresponse above the transient upset level.

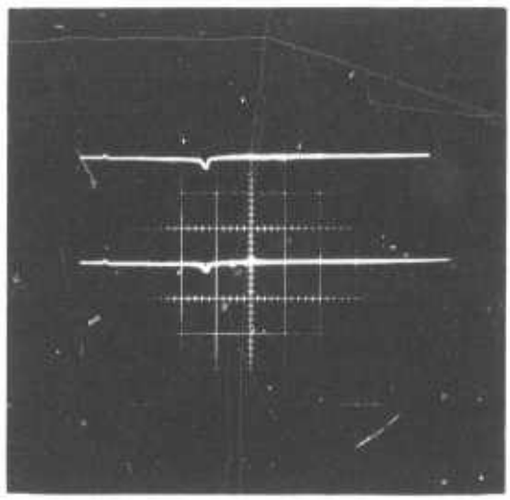
$\hat{\dot{\gamma}} = 2.1 \times 10^9$ rads(Si)/s

(a) Sample #8B-1



(b) Sample #8B-2

(c) Sample #8B-3



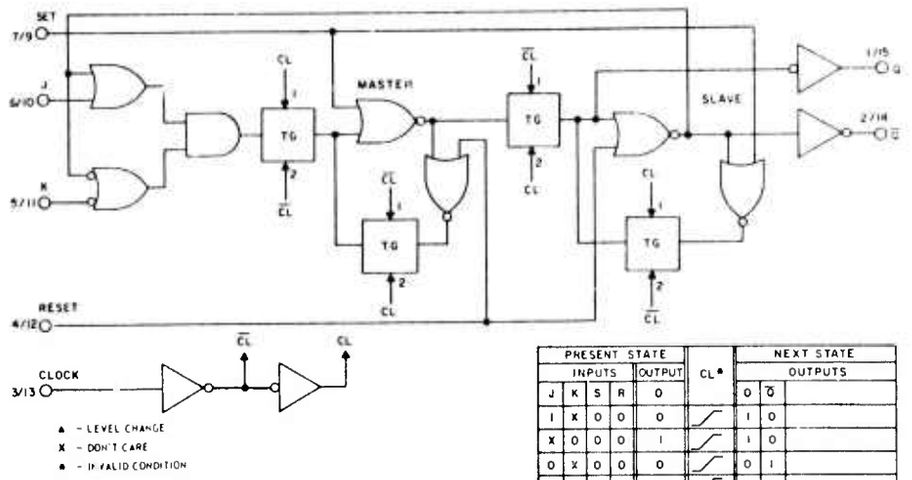
e_o = 5 V/div., t = 2 μs/div.

Figure 2-13. CD4030A radiation-induced failure.

samples of the very-high-reliability arrays were available at the time of procurement. The schematic diagram of a single flip-flop is shown in Figure 2-14.

Observed results on total ionizing dose and transient photoresponse susceptibility are summaried in Table 2-14. The range in data reflects the worst-case observations over all conditions of microcircuit static bias and dynamic operation.

2.4.1 CD4027A Total-Ionizing-Radiation-Induced Permanent Damage. A total of six samples of the CD4027A were exposed to the ionizing radiation environment of the NRTC Co-60 hot cell. The six samples represented 12 samples of the individual J-K master-slave flip-flop. All 12 flip-flops were exposed simultaneously with the logic input of eight flip-flops under static bias and the inputs of the remaining four flip-flops exercised with a dynamic logic sequence. Four flip-flops each under static bias were set in the Q = 1 and Q = 0 logic states with logic inputs in the worst-case condition. The logic sequence for dynamic operation was evaluated with logic simulation with the goal that each of the gate elements of the flip-flop was switched with a 50% duty cycle at a 100 kHz clock rate. For the dynamic logic inputs employed it was determined that 23 of the 24 gates was dynamically exercised and the remaining gate stayed in the "1" state. It is felt that this is reasonably representative of full dynamic operation. During the entire exposure, one output each from the two dynamically operated microcircuits was continuously monitored. Electrical performance characteristics of all the flip-flop samples were measured at a series of increments during the total exposure. Performance parameters measured were the output current-voltage

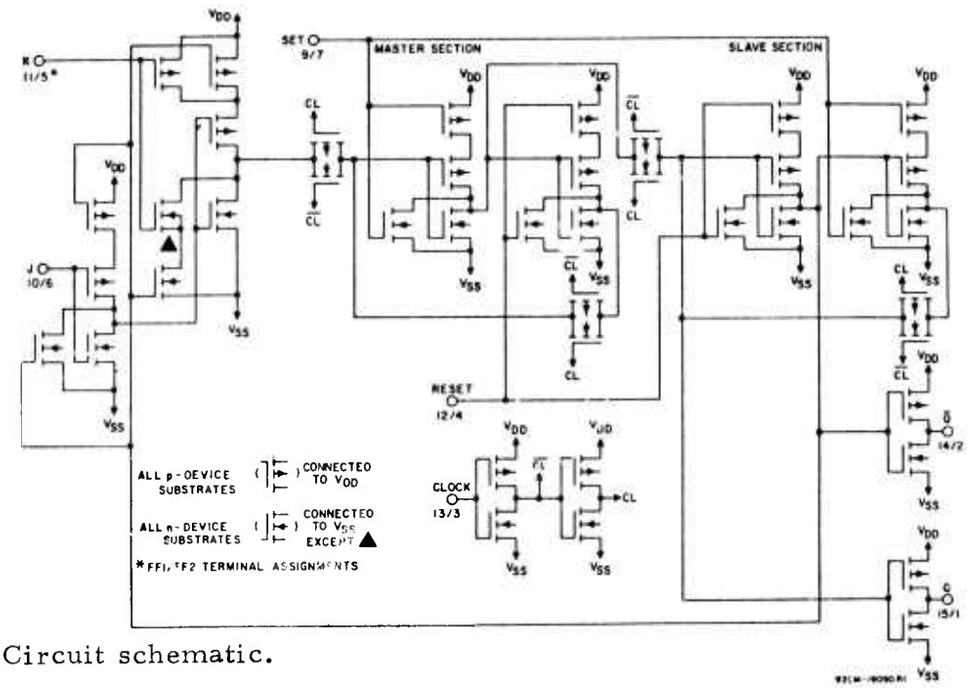


PRESENT STATE					CL●	NEXT STATE	
INPUTS				OUTPUT		OUTPUTS	
J	K	S	R	Q		Q	$\overline{Q}$	
1	X	0	0	0	⌐	1	0	
X	0	0	0	1	⌐	1	0	
0	X	0	0	0	⌐	0	1	
X	1	0	0	1	⌐	0	1	
X	X	0	0	X	⌐			← NO CHANGE
X	X	1	0	X	X	1	0	
X	X	0	1	X	X	0	1	
X	X	1	1	X	X	*	*	

WHERE 1 = HIGH LEVEL
0 = LOW LEVEL

92CM-17188R2

(a) Logic diagram and truth table.



(b) Circuit schematic.

Figure 2-14. CD4027A J-K flip-flop logic and circuit diagrams.

TABLE 2-14. SUMMARY OF OBSERVED CD4027A RADIATION SUSCEPTIBILITY

Pulsed Ionizing Radiation

Narrow-Pulse Transient Failure Level ($t_p \cong 30$ ns)

4 microcircuits/8 flip-flops

$0.6 \leq \dot{\gamma}_c \leq 1.5 \times 10^9$ rads(Si)/s

Wide-Pulse Transient Failure Level ($t_p \cong 4.5\ \mu$s)

2 microcircuits/4 flip-flops

$\sim 0.9 \times 10^8$ rads(Si)/s

Total Ionizing Radiation Dose

Co-60 Exposure at 20 krads(Si)/hr

6 microcircuits/12 samples

$1.5 \leq \gamma_c \leq 2.9$ Mrads(Si)

characteristics, the voltage transfer function and dynamic logic function. The critical ionizing radiation dose for failure definition was defined as that required to reduce the output current by 67% of its initial value for the logic "1" and logic "0" output states or overall failure of logic function. The worst-case total dose failure levels observed are summarized in Table 2-15 with the appropriate bias conditions.

2.4.2 CD4027A Narrow-Pulse Transient Photoresponse. Four microcircuits, or eight samples of the CMOS CD4027A dual J-K flip-flops were exposed to the gamma-mode environment of the NRTC 2-MeV flash x-ray. All samples represented the high-reliability specification. The

TABLE 2-15. TEST CONDITIONS AND CRITICAL DOSE FOR CMOS Co-60 TOTAL DOSE SUSCEPTIBILITY CHARACTERIZATION

Input Condition	Input Terminal Logic State				
	CLK	J	K	R	S
I	1	1	0	1	0
II	1	1	0	1	0
III	0	0	1	0	1
IV	0	0	1	0	1
V	Dynamic (See test circuit schematic in the Appendix A)				

	Input Condition	Sample Types	Critical Dose (γ_c) Rads(Si)
CD4027A	I	. . .600	$1.84 - 2.4 \times 10^6$
	I	. . .600	$1.84 - 2.4 \times 10^6$
	II	. . .600	$1.51 - 1.84 \times 10^6$
	II	. . .600	$1.51 - 1.84 \times 10^6$
	III	. . .600	$1.84 - 2.4 \times 10^6$
	III	. . .600	$1.84 - 2.4 \times 10^6$
	IV	. . .600	$1.51 - 1.84 \times 10^6$
	IV	. . .600	$1.51 - 1.84 \times 10^6$
	V	. . .600	$2.4 - 2.93 \times 10^6$
	V	. . .600	$2.4 - 2.93 \times 10^6$
	V	. . .600	$2.4 - 2.93 \times 10^6$
	V	. . .600	$2.4 - 2.93 \times 10^6$

flip-flops were exposed in both the Q = 1 and Q = 0 information logic state for all meaningful static input bias conditions of the control inputs. The test circuit schematics are presented in Appendix B. Results showed that the worst-case for the samples was the Q = 1 logic state, and that the nature of the transient failure was transient logic upset rather than radiation-induced change-of-state. The worst-case logic upset threshold observed was approximately $0.6 - 0.8 \times 10^{9}$ rads(Si)/s. No latch-up, anomalous photoresponse, or radiation-induced permanent damage was observed for exposures up to 5×10^{10} rads(Si)/s. Typical waveforms of the output photoresponse are shown in Figure 2-15.

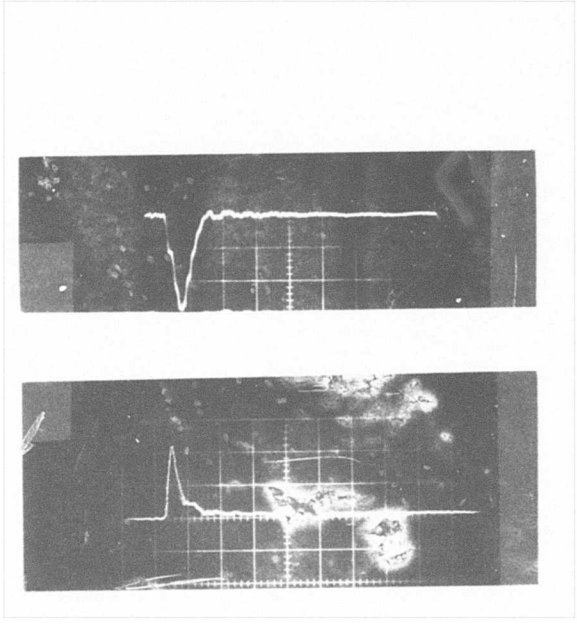


Figure 2-15. CD4027A narrow-pulse photoresponse waveforms.

2.4.3 CD4027A Wide-Pulse Transient Photoresponse. Four flip-flops from two CD4027A samples were exposed to the wide-pulse ionizing radiation environment of the IRT linear accelerator. The transient output photoresponse was measured for the flip-flops as set both in the 1- and 0-states. The test circuit used in the experiment characterization is shown in Appendix B. The transient photoresponse affects were dominated by the transient output rather than radiation-induced change-of-state. No radiation-induced change-of-state was observed in the course of the study, but anomalous photoresponse or incipient latch-up was observed on one sample. The transient logic upset level, based on the output photoresponse was determined as approximately 9×10^7 rads(Si)/s. Detailed results of the radiation exposures are summarized in Table 2-16, and typical output waveforms are illustrated in Figures 2-16 and 2-17.

The observed incipient latch-up on one of the flip-flops is illustrated in Figure 2-17. In this case, both outputs of the flip-flop settle to the 0-state for several minutes after radiation exposure and then the flip-flop returned to the normal Q = 1 output levels. These results are repeatable. No permanent damage was observed as a result of the effect.

2.5 CD4046A Micropower Phase-Locked Loop Study

The CD4046A micropower phase-locked loop is a junction-isolated CMOS array consisting of a low-power, linear voltage-controlled oscillator (VCO) and two different phase comparators having a common single-input amplifier and a common comparator input.[5] Twenty samples of the CD4046A were obtained to standard full-temperature military/commercial specifications. The schematic diagram of the array is shown in Figure 2-18.

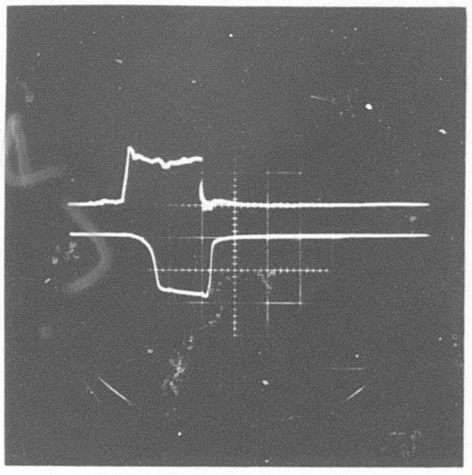
TABLE 2-16. SUMMARY OF CD4027A WIDE-PULSE PHOTORESPONSE MEASUREMENTS

Flip-Flop Sample	Logic State Q	Peak Photoresponse Δe_o, V	Peak Photoresponse $\dot{\gamma}$, rads(Si)/s	Comments
11-1	Q = 1	-9.0	9.2×10^7	See Figure 2-16 (a)
11-1	Q = 1	-9.8	2.5×10^9	
11-1	Q = 1	-9.8	2.9×10^9	
11-2	Q = 1	-9.0	9.2×10^7	See Figure 2-16 (b)
11-2	$\overline{Q}$ = 0	+9.0	9.2×10^7	See Figure 2-16 (c)
11-2	Q = 1	-2.1	3.7×10^8	
11-2	$\overline{Q}$ = 0	+0.8	3.7×10^8	
11-2	Q = 1	-9.8	2.9×10^9	
11-2	$\overline{Q}$ = 0	+10	2.9×10^9	
12-1	Q = 1	-0.3	4.8×10^7	
12-1	Q = 1	-9.2	9.0×10^7	
12-1	Q = 1	-9.5	1.4×10^9	See Figure 2-17 (a)
12-2	Q = 1	-0.3	4.8×10^7	
12-2	$\overline{Q}$ = 0	+0.4	4.8×10^7	
12-2	Q = 1	-9.2	9.0×10^7	
12-2	$\overline{Q}$ = 0	+10	9.0×10^7	
12-2	Q = 1	-6.0	1.4×10^9	See Figure 2-17 (b)*
12-2	$\overline{Q}$ = 0	+10	1.4×10^9	See Figure 2-17 (c)*

*Incipient latch-up

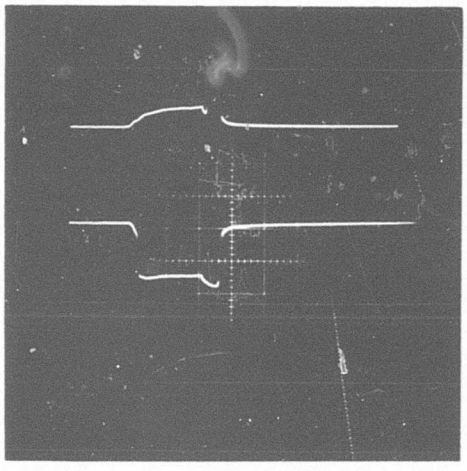
$\hat{\dot{\gamma}} \cong 9.2 \times 10^7$ rads(Si)/s

(a) Sample 11-1 $Q = 1$



(b) Sample 11-2 $\overline{Q} = 0$

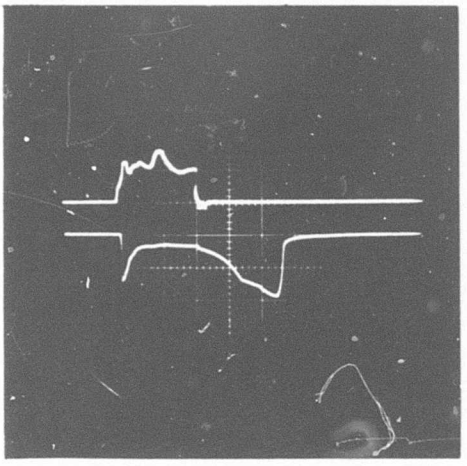
(c) Sample 11-3 $Q = 1$



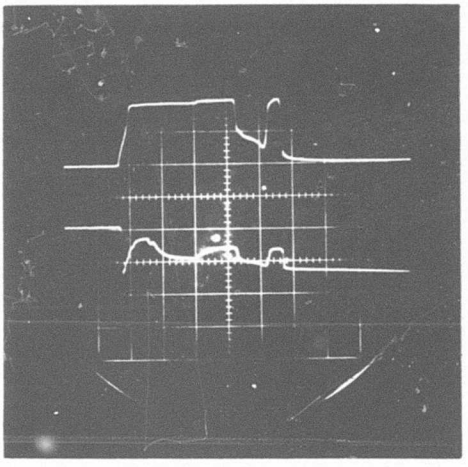
e_o = 5 V/div., t = 2 μs/div.

Figure 2-16. CD4027A wide-pulse photoresponse waveforms at transient upset dose rate.

$\dot{\gamma} \cong 1.4 \times 10^{9}$ rads(Si)/s



(a) Sample 12-1 $Q = 1$



(b) Sample 12-2 $\overline{Q} = 0$

(c) Sample 12-2 $Q = 1$

*Note, both Q and $\overline{Q}$ outputs = 0 well after the end of the radiation pulse

Figure 2-17. CD4027A wide-pulse exposure illustrating anomalous photoresponse.

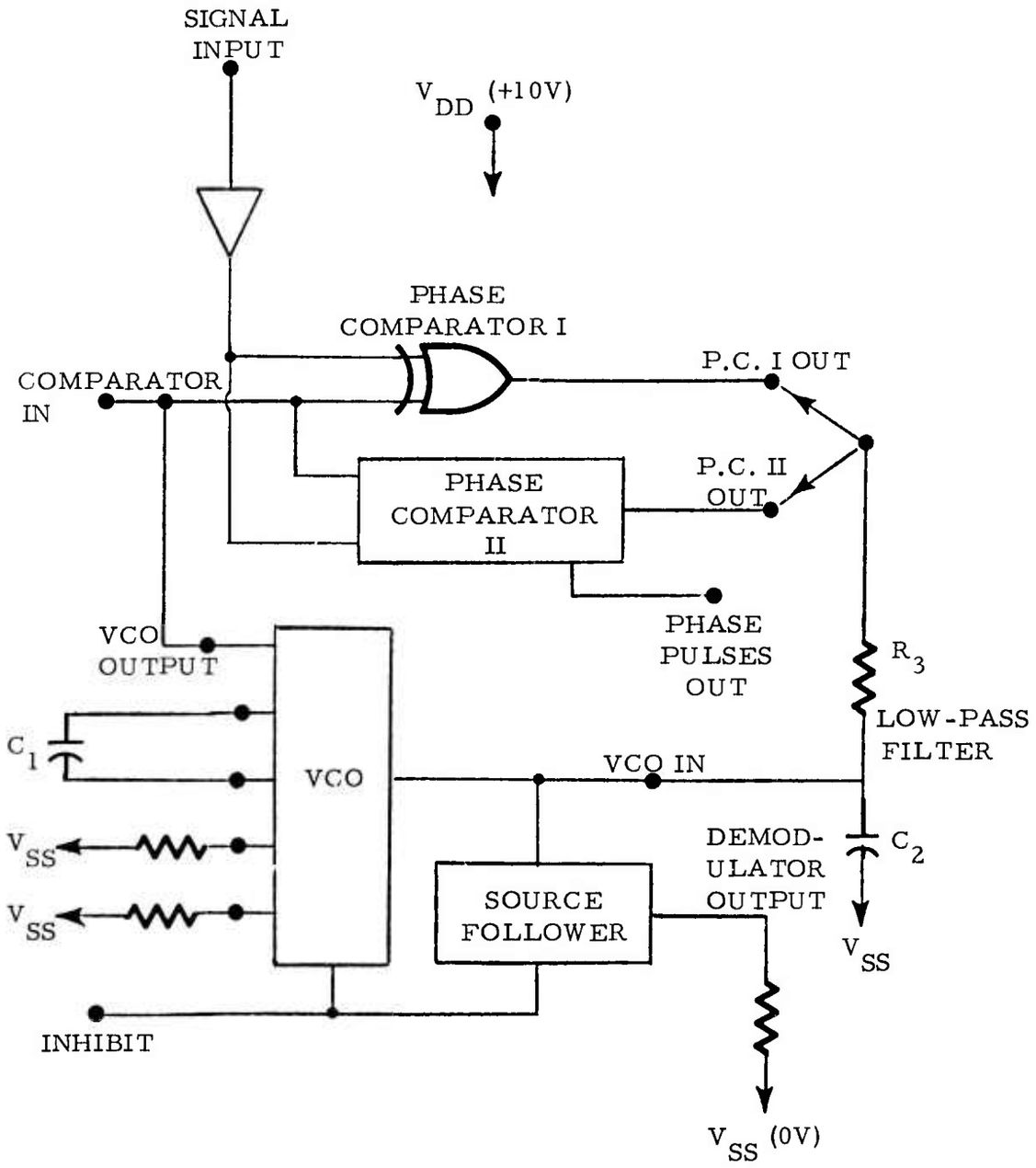


Figure 2-18. CD4046A phase-locked loop schematic.

The voltage-controlled oscillator uses an external capacitor in conjunction with external resistors to establish frequency range and frequency offset if desired. The VCO signal input is the output signal if one of the two phase comparators is selected via a low pass filter. Phase Comparator I circuit is an implementation of the exclusive-OR logic function; that is, there is an output only when the input signals are in opposite logical states. With no signal or noise input to the exclusive-OR comparator, the average output voltage is $V_{DD}/2$ or one-half the VCO signal input dynamic range. An input voltage of $V_{DD}/2$ causes the VCO to oscillate at the center frequency. This comparator is immune to disturbances with amplitudes less than CMOS critical threshold values. Another characteristic of this comparator is that it requires a 90^{o} phase difference between the input signals in the stable or locked condition. The phase difference between input signals varies between 0^{o} and 180^{o} over the entire locked frequency range. Phase Comparator II is an edge-controlled digital memory network. It consists of four flip-flop stages, controlled gating, and a tri-state output circuit comprising n- and p-type transistors connected to a common output node. When the p-type or n-type transistors are ON, they pull the output node to V_{DD} or V_{SS} respectively. This type of comparator operates only on the positive going edge of the input signal. If the signal-input frequency is higher than the comparator-input frequency, the p-type transistor is maintained ON. If the comparator-input frequency is higher than the signal-input frequency, the n-type transistor is maintained ON. If the frequencies of the two input signals are equal and the signal-input lags the the comparator-input, the n-type transistor remains ON. If the comparator-input lags the signal-input, the p-type transistor remains ON until the phases of the comparator-input and signal-input signals are equal. There is, therefore, no phase shift

between the comparator's two input signals in the locked range of the VCO. Under the locked or stable range of the P_{LL}, the output of Phase Comparator II is in the high impedance (Hi-Z) state and holds voltage on the capacitor of the low pass filter constant. The lock and capture ranges of Phase Comparator II are equal and independent of the low pass filter. Since the comparator is in the Hi-Z state in the locked condition, the comparator operates at very low power. The VCO's low frequency point is adjusted during no signal-input.

Observed results on total ionizing dose and transient photoresponse susceptibility are summarized in Table 2-17. The range in data reflects the worst-case observations over all conditions of microcircuit operation.

TABLE 2-17. SUMMARY OF OBSERVED CD4046A RADIATION SUSCEPTIBILITY

Pulsed Ionizing Radiation

Narrow-pulse Transient Failure Level ($t_p \cong 30$ ns)

4 samples

$1.0 \leq \dot{\gamma}_c \leq 5 \times 10^8$ rads(Si)/s

Wide-pulse Transient Failure Level

2 samples

$\dot{\gamma}_c \cong 1 \times 10^7$ rads(Si)/s

Total Ionizing Radiation Dose

Co-60 Exposure at 20 krads(Si)/hr

4 samples

$6.3 \leq \gamma_c \leq 7.5 \times 10^4$ rads(Si)

2.5.1 CD4046A Total-Ionizing-Radiation-Induced Permanent Damage. Four samples of the CMOS CD4046A phase-locked loop were exposed to the ionizing radiation environment of the NRTC Co-60 hot cell. All four samples were exposed simultaneously with two of the samples configured with the Phase Comparator I and the remaining two samples configured with Phase Comparator II. The power supply voltage (V_{DD}) was +10V. The four samples were operated at 100 kHz by synchronizing the phase-locked loop to an external 100 kHz square-wave signal source. The samples were exposed at a dose-rate of 20 krads(Si)/s. The nature of failure in all cases was a loss of synchronization followed by a rapid change of frequency until only a dc output resulted. Failure occurred so rapidly that it could not be determined if the loss of synchronization was accompanied by a reduction in signal amplitude. Observed levels of critical total ionizing radiation dose are summarized as

Test Condition	Samples	Critical Total Dose (rads(Si))
Phase Comparator I	1	75 k
Phase Comparator I	1	70 k
Phase Comparator II	1	63 k
Phase Comparator II	1	73 k

2.5.2 CD4046A Narrow-Pulse Transient Photoresponse. Four samples of the CMOS CD4046A micropower phase-locked loop were exposed to the NRTC 2-MeV flash x-ray environment. The output photoresponse of the arrays was monitored with the circuit operating dynamically at a frequency of 100 kHz. Critical transient effects were measured for the circuits using both type-I and type-II phase detectors. The critical dose

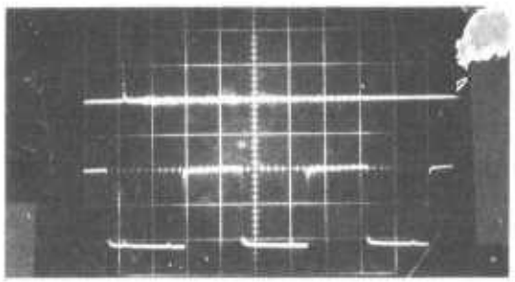
rate, in this case, was defined as either that required to cause a logic transition, or a transient change in the phase-locked loop output frequency. Results of the study are summarized in Table 2-18 in terms of critical dose rate for the worst-case of logic upset of frequency shift. The critical output photoresponse was lower with the output in the 0-state by approximately a factor of two for that observed with the output in the 1-state. The worst-case critical dose rate for the four samples was approximately $1.5 - 4.0 \times 10^8$. Typical waveforms are shown in Figure 2-19. The transient failure level was approximately the same for either the type-I or type-II phase detector circuit configuration, but the circuit configuration did have an effect on the observed waveforms at radiation levels well above the transient upset level.

TABLE 2-18. CD4046 NARROW-PULSE TRANSIENT FAILURE LEVELS

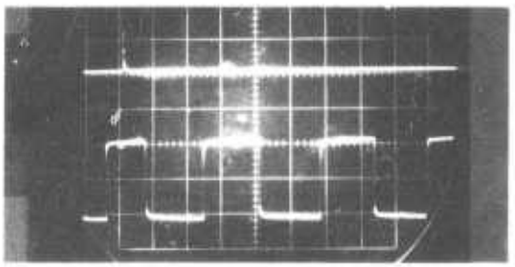
Sample Number	Phase Comparator I		Phase Comparator II	
	Output "0" (rads(Si)/s)	Logic State "1" (rads(Si)/s)	Output "0" (rads(Si)/s)	Logic State "1" (rads(Si)/s)
1	$1.5 - 2 \times 10^8$	$4.0 - 5 \times 10^8$	$2.0 - 3 \times 10^8$	$4.0 - 5 \times 10^8$
2	$3.0 - 4 \times 10^8$	$4.0 - 5 \times 10^8$	$2.0 - 3 \times 10^8$	$4.0 - 5 \times 10^8$
3	$1.5 - 2 \times 10^8$	$2.0 - 3 \times 10^8$	$1.5 - 2 \times 10^8$	$2.0 - 3 \times 10^8$
4	$1.5 - 2 \times 10^8$	$4.0 - 5 \times 10^8$	$1.5 - 2 \times 10^8$	$4.0 - 5 \times 10^8$

2.5.3 CD4046A Wide-Pulse Transient Photoresponse. Two samples of the CD4046A phase-locked loop were exposed to the wide-pulse ionizing radiation environment of the IRT linear accelerator. One of the

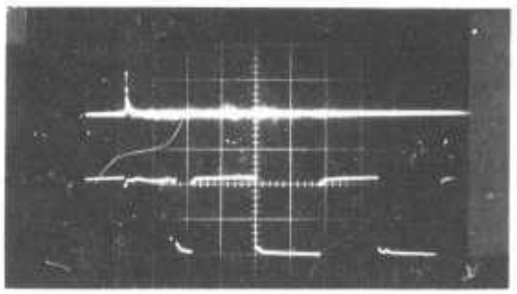
(a) $\dot{\gamma} = 2 \times 10^8$ rads(Si)/s



(b) $\dot{\gamma} = 5 \times 10^8$ rads(Si)/s



(c) $\dot{\gamma} = 5 \times 10^{10}$ rads(Si)/s



e_o = 5V/div., t = 2 μs/div.

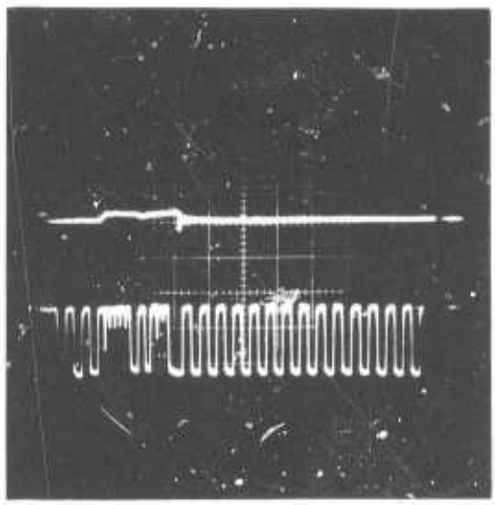
Figure 2-19. CD4046A narrow-pulse photoresponse waveforms.

phase-locked loops was set up using the I-type phase comparator, and the other sample was set up using the II-type phase comparator. Both samples were exposed while under dynamic operating conditions. The nature of the observed transient photoresponse was substantially different under the two circuit conditions, but the transient failure level was approximately 1×10^7 rads(Si)/s in both cases. Detailed results of the radiation exposures are summarized in Table 2-19, and typical output waveforms are illustrated in Figures 2-20 and 2-21.

TABLE 2-19. CD4046A WIDE-PULSE PHOTORESPONSE MEASUREMENTS

Sample Number	Test Conditions	$\dot{\gamma}$ rads(Si)/s	Result
21	Phase Comp. I	$\sim 10^7$	Slight disturbance in a single output cycle
21	Phase Comp. I	$\sim 10^7$	Breakup during radiation pulse (see Figure 2-20 (a))
21	Phase Comp. I	$\sim 10^7$	Hard breakup during radiation pulse
21	Phase Comp. I	1.3×10^8	Output clamped to +V during radiation pulse
21	Phase Comp. I	1.4×10^9	Output clamped during and following $\dot{\gamma}$ (see Figure 2-20 (b))
22	Phase Comp. II	$\sim 1.2 \times 10^7$	Slight decrease in frequency during radiation pulse (see Figure 2-21 (a))
22	Phase Comp. II	4.7×10^8	Increase in frequency during radiation pulse
22	Phase Comp. II	7.6×10^8	Breakup during radiation pulse (see Figure 2-21 (b))
22	Phase Comp. II	1.7×10^9	Output clamped to +V during radiation pusle

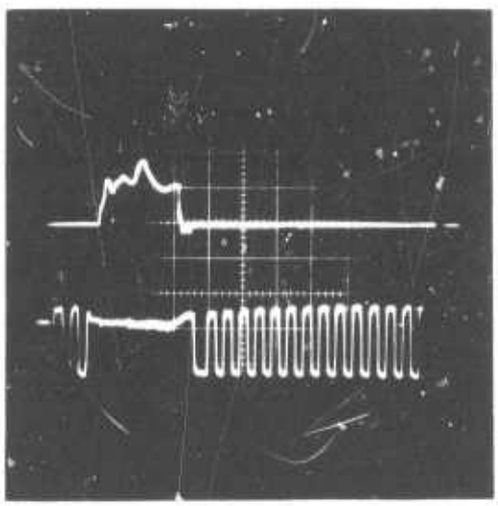
(a) $\dot{\gamma} \cong 10^7$ rads(Si)/s



PLL Output

e_o = 5 V/div., t = [illegible] μs/div.

(b) $\dot{\gamma} = 1.4 \times 10^9$ rads(Si)/s

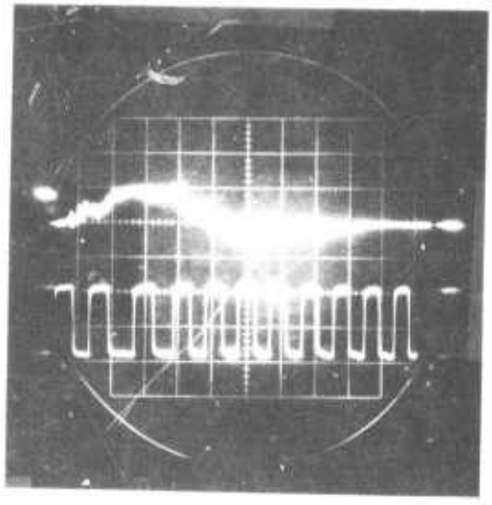


PLL Output

e_o = 5 V/div., t = 2 μs/div.

Figure 2-20. CD4046A wide-pulse photoresponse under Phase Comparator I circuit configuration.

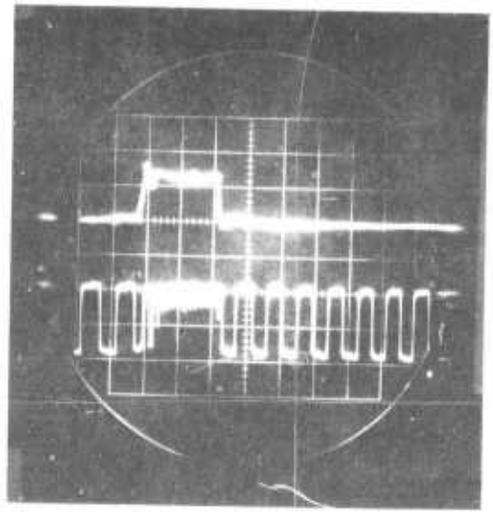
(a) $\dot{\gamma} = 1.2 \times 10^{7}$ rads(Si)/s



PLL Output

e_o = 5 V/div., t = 2 μs/div.

(b) $\dot{\gamma} = 7.6 \times 10^{8}$ rads(Si)/s



PLL Output

e_o = 5 V/div., t = 2 μs/div.

Figure 2-21. CD4046A wide-pulse photoresponse under Phase Comparator II circuit configuration.

The effects of the ionizing radiation pulse on the phase-locked loop are quite complex, and it is not clear as to the variation in observed photoresponse with change in circuit configuration. The transient upset level, however, is lower than for any of the other CMOS arrays considered in this study and should be investigated in greater detail. No permanent damage or obvious latch-up effects were observed in the course of the characterization.

2.6 Concluding Comments

2.6.1 Total Ionizing Dose-Induced Permanent Damage. The total-dose-induced permanent damage failure level varied widely through the five types of CMOS arrays. The most susceptible was the CD4046A which had been procured to standard commercial specifications. There was also a substantial variation in the susceptibility over the other four circuit types, as well as a substantial variation in the devices of the same type, but obtained to different reliability specifications.

It is not clear that the higher radiation susceptibility of phase-locked loop was due to the relaxed specification, or due to the specific performance criteria and bias conditions unique to the analog-digital operation of the phase-locked loop. Similarily, while there was a significant variation in susceptibility between parts of different reliability specifications, the pattern was not consistent between circuit types and no conclusions can be substantiated on variations with reliability screening.

2.6.2 Transient Photoresponse. The nature of the transient photoresponse and critical dose rates varied widely among the five CMOS circuit types.

All circuit types were in common, however, with the increase in susceptibility with increasing radiation pulse width. The critical dose rate, for all sample types, decreased by approximately a factor-of-ten as the radiation pulse width increased from 30 ns to 4.5 μs. This is consistent with an effect which is determined by substrate photocurrents with a minority carrier lifetime in the substrate which is on the order of 5-10 μs.

The worst-case logic states for the transient output photoresponse were generally the 0-output state. The exception was the CD4030A exclusive-OR gate where the worst-case susceptibility was definitely the 1-output state. The CD4030A, however, is the only array that employs a transmission gate which could dominate the transient photoresponse and reverse the effect compared to those arrays whose photoresponse is dominated by the standard CMOS inverter.

It is interesting to note that, in the three array types in which the power-supply photocurrent was measured, the worst-case logic input bias condition for the power-supply photocurrent was never the same as that for the output logic upset level. This is potentially an important consideration in determining the worst-case test configuration for system hardening.

Finally, in the course of photoresponse characterization, several samples were permanently damaged. It is not clear if the damage was the result of total accumulated ionizing radiation dose (which seems unlikely) or the result of radiation-induced latch-up (which was not directly observed). Results of this study only indicate clearly that the possibility of permanent damage is much greater in a wide-pulse ionizing radiation environment

than it is in a narrow-pulse environment. Further study is required on the nature of CMOS latch-up in bulk CMOS arrays as a function of ionizing radiation pulse width.

*Process parameters control for radiation hardening was not employed for the CMOS microcircuits characterized. Variations in the detailed process parameters during fabrication in late 1973 make it difficult to correlate effects between samples and the results reported should not be used as a quantative evaluation of the radiation susceptibility of CMOS fabricated with current, controlled processes.

3.0 I^2L TECHNOLOGY STUDY

Integrated Injection Logic (I^2L) is an emerging bipolar LSI technology that offers the potential of high density, high reliability and very low-power digital arrays.[6-8] In some applications it is suggested that the overall performance capability of I^2L is beyond that of any existing bipolar or MOS/LSI technology. The purpose of this study has been to determine the radiation susceptibility of available unhardened I^2L devices and logic cells with regard to the specified threat radiation environments of military systems. As I^2L technology advances, spurred by intensive development for commercial applications, performance parameters and radiation effects of I^2L will be compared to hardened TTL and hardened CMOS for manned, satellite and missile system applications. Specific comparisons cannot be made at this time because data on basic unhardened inverters and logic cells is not sufficient to define the system functions in terms of operating speed, power dissipation, and noise margin. It is hoped, however, that early discussion of radiation effects in I^2L will guide system application in relevant systems and avoid premature application in other systems. Radiation effects considered are neutron displacement damage, total ionizing-dose surface effects, and transient photoresponse.

3.1 I^2L Structure and Electrical Performance

The basic building block of an I^2L array is the single-input, multi-output inverter shown schematically in Figure 3-1. The inverter consists of a pnp transistor current source that supplies the bias current to the switched multi-collector npn transistor. When the npn transistor at the input of the inverter is turned on, all the pnp collector current is absorbed.

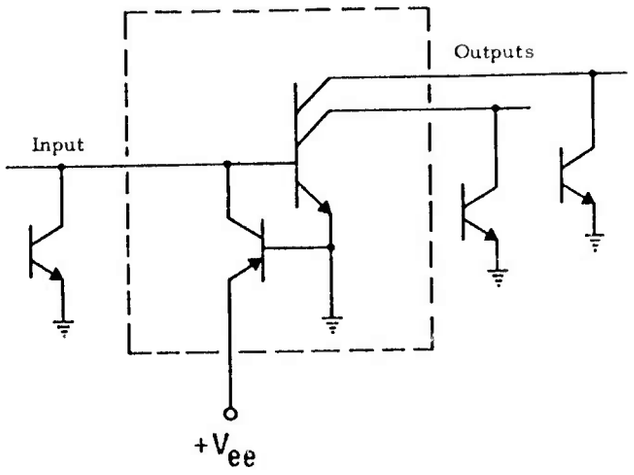


Figure 3-1. Basic I^2L inverter schematic.

The input voltage is held near zero volts and the npn transistor of the inverter is turned off. On the other hand, when the npn transistor of the previous stage is turned off, the pnp bias current of the inverter is diverted to the npn transistor and the inverter output appears as a low voltage, capable of sinking the bias current of all connected loading inverters. Application of the I^2L inverter in an array requires the connection of multiple logic signals to the single input of the inverter, forming a "wired AND" at each inverter input. Thus, to transmit the same logic signal to a variety of cells in the array it is necessary to isolate each of the connections. This is accomplished in the I^2L inverter by the use of the multiple-collector npn transistor.

The principal advantages of I^2L are the realization of the inverter as a compact semiconductor device, as shown in Figure 3-2, and the complete elimination of large-geometry diffused or thin-film resistor elements. As shown in Figure 3-2, the pnp transistor is realized as a lateral

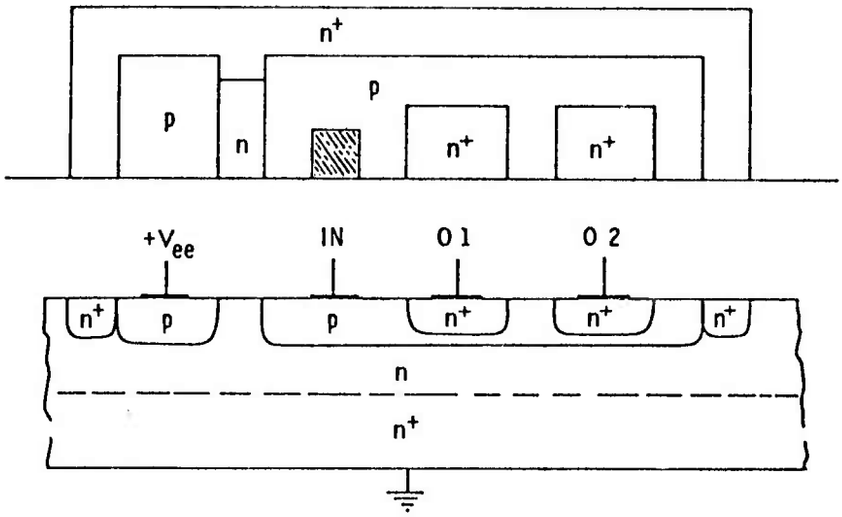


Figure 3-2. I^2L inverter structure.

structure merged with the npn transistor. The npn structure itself is "inverted" from the structure familiar in other bipolar arrays with the collector outputs as the top n^+ regions and the emitter as the "substrate" n-n^+ region. An additional advantage of the structure is the use of the back contact on the chip as the ground metallization, simplifying the surface metallization pattern and allowing increased cell density in an LSI array. Compact geometry of the I^2L inverter is illustrated by an area of 2.3×10^{-5} cm^2 for a two-output inverter using state-of-the-art design rules of conventional microcircuit processing.

The basic I^2L structure as shown in Figure 3-2 is referred to as non-isolated I^2L since all inverters are realized on a common n^+ substrate. It is also possible to realize the digital I^2L array as an n^+ pocket of a p-substrate such that linear and high-power digital elements can be realized in other parts of the junction-isolated microcircuit. This more

complex form is referred to as isolated-I^2L and has not been characterized in this study.

The disadvantages of the high-density inverter structure are the low gain of the lateral pnp transistor and the low gain of the "inverted" npn transistor. Gain of both elements is improved somewhat by the use of the n^+ collar surrounding the inverter and the $n\text{-}n^+$ doping "substrate" profile. The n^+ collar reduces unwanted carrier injection from the outside sidewalls and the $n\text{-}n^+$ "substrate" doping profile reduces the unwanted carrier flow from the pnp emitter (sometimes referred to as the injector) and increases the emitter efficiency of the npn transistor. Even with the low-gain structures of the transistor elements, it is possible to realize high performance of the I^2L inverter. The common-base current gain of the lateral pnp transistor can be interpreted as the inefficiency of transforming the power supply current to the inverter bias current. Typically, the common-base gain of the lateral pnp transistor is on the order of 0.5 to 0.8. The input bias current to the inverter, in turn, basically determines the maximum switching speed of the inverter in low-power operation. The power dissipation of the inverter is essentially independent of the frequency of operation until the maximum operating frequency is approached and is approximately

$$P_d \cong V_{EE} I_{EE} \tag{1}$$

where V_{EE} is the base-emitter voltage of the pnp transistor and I_{EE} is the dc bias current. For typical operation, the bias current would be 100 μA or less, with an input voltage of less than 1V for a power dissipation of 0.1 mW. Under these conditions, the inverter switching time

is typically less than 10 ns for an overall speed-power product of less than 1 pJ.

It should be noted at this point that like other bipolar LSI technologies, the power dissipation of an I^2L array is essentially independent of operating speed and quite unlike MOS/LSI technologies where frequently the power dissipation is proportional to the frequency of operation. Unlike other bipolar technologies, however, the power dissipation of I^2L can be adjusted by system variation of the power supply current for the maximum speed of operation required by that system.

Current gain of the npn transistor element in the I^2L inverter is particularly critical in determining the maximum fan-out. The maximum fan-out capability of the inverter is approximately equal to the common-emitter transistor gain of the npn transistor element. The maximum fan-out required in a typical I^2L array is on the order of 4, which compares favorably to the measured gains that typically range from 8 to 20.

The final concern of the I^2L structure is that of the possibility of current-hogging between two inverters whose inputs are connected to the same logic output. This effect is virtually eliminated in the I^2L structure because of the low output offset voltage of the "on" inverter (typically less than 10 mV). The low output offset voltage is due to the high inverse gain of the I^2L output transistor (typically 40-100) which is, of course, the forward gain of a more familiarly connected npn microcircuit transistor.

In summary, I^2L is a practical, realizable LSI technology whose electrical performance compares favorably with any other LSI technology for low-power, medium-speed digital applications. Commercial LSI arrays are not yet available, but several major semiconductor manufacturers have let it be known that they have intensive development programs under way and commercial arrays are expected in 1975.

3.2 Radiation Effects Study, Neutron Displacement Damage

Samples of basic I^2L logic cells have been obtained for evaluation of radiation susceptibility. These samples were fabricated in the course of the Northrop development of an I^2L/LSI frequency synthesizer under an ECOM contract.— Radiation hardening has not been a consideration in this development. Even under these circumstances, samples have been very limited, and since the logic cell design is still evolving, those samples characterized do not represent a mature production technology.

In the characterization to this point, principal emphasis was initially placed on the evaluation and analysis of neutron-induced displacement damage and transient photoresponse. Damage resulting from total ionizing radiation dose-induced surface effects has been considered in more recent studies.

The principal effect of neutron displacement damage in I^2L arrays is the familiar degradation of the minority carrier lifetime. At first glance, the susceptibility of I^2L to neutron damage would be expected to be high because of the well-known susceptibility of lateral pnp transistors in bipolar operational amplifiers, and the familiar low gain and

low gain-bandwidth product (f_T) of planar bipolar transistors operated in the inverted mode. Results indicate that the neutron-damage susceptibility in I^2L is modest because of the nature of the gain-limiting effects in the structure as well as because of the low gain requirements on the elements in a practical array.

Gain of the pnp transistor element is limited primarily by the injection of carriers vertically into the substrate rather than laterally to the collector junction. Neutron degradation of the substrate lifetime will increase this diode current as the minority carrier diffusion length decreases. Since the diffusion length varies as the square-root of the lifetime, the degradation is less severe with increasing neutron fluence than the gain degradation of a transistor that is limited by base-width-associated recombination. Similarly, the gain of the npn transistor element in the I^2L structure is limited primarily by the emitter efficiency and the current flow through the base overlap diode. The overlap diode current consists of hole current flow in the emitter region, and electron flow to the base ohmic contact and surface of the base region. The electron current is not very sensitive to minority carrier recombination, but is sensitive to surface recombination velocity as will be discussed later. Hole current in the base overlap diode is degraded as the minority carrier diffusion length decreases, as well as the hole current flow in the transistor which degrades the transistor emitter efficiency. Neutron-induced gain degradation in the transistor elements of an I^2L inverter are presented in Fig. 3-3 and 3-4. The calculated result was obtained by using typical values of geometry and bulk semiconductor parameters for the inverter structure, as described in a previous report. Experimental results, as shown, represent the measured degradation on elements of

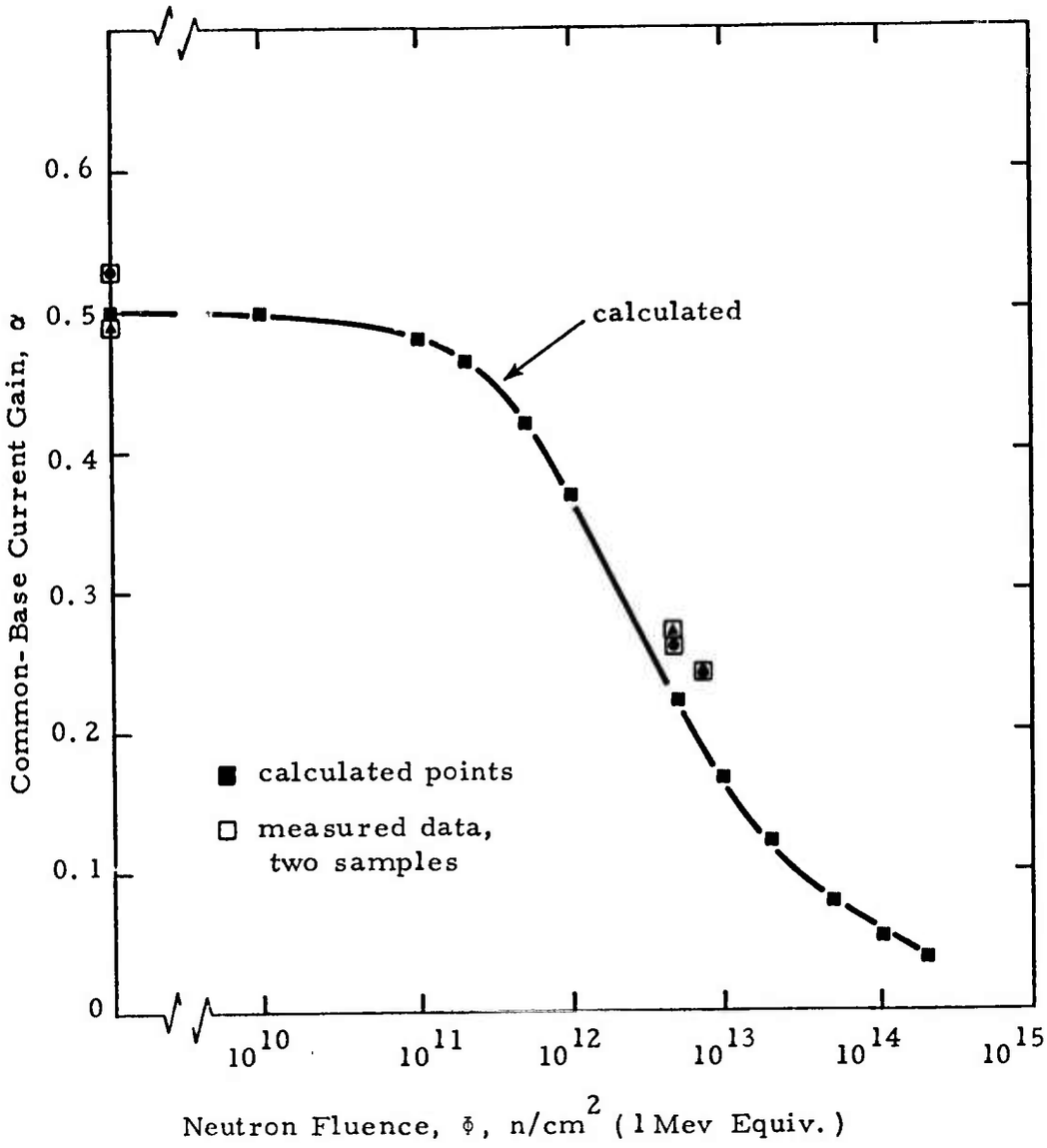


Figure 3-3. I^2L pnp transistor element gain degradation.

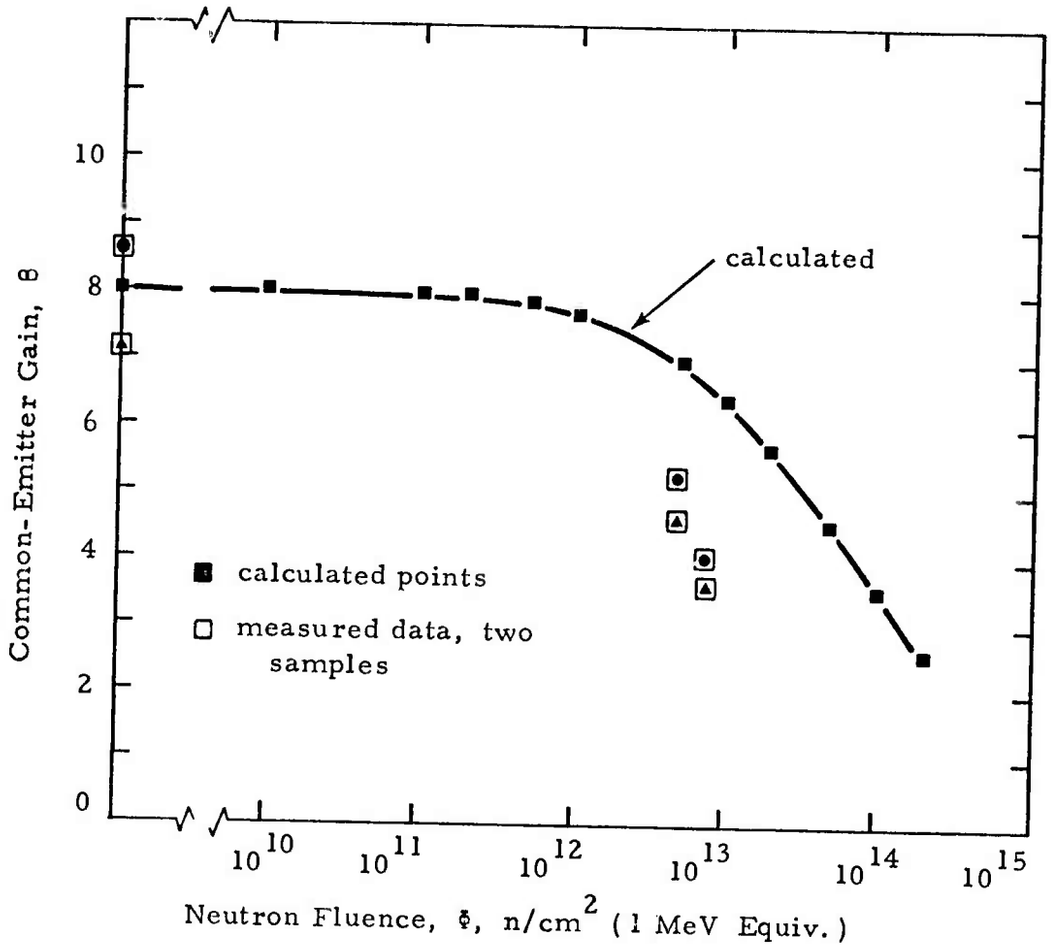


Figure 3-4. I^2L npn transistor gain degradation.

two samples of an early test chip. Degradation of the pnp transistor gain would result in a degradation of the speed-power product by a factor of two at a neutron fluence of 5×10^{12} n/cm^2 (1 MeV equivalent), and an order-of-magnitude degradation at about 5×10^{13} n/cm^2. Degradation of the npn transistor gain, on the other hand, has little effect on the overall inverter performance until the value of the gain approaches the required fan-out ratio. In this case, the gain degradation to a fan-out requirement of four would occur in the decade between 10^{13} and 10^{14} n/cm^2.

Neutron-induced degradation was measured on four samples of the R-S flip-flop. The purpose of the characterization was to obtain a preliminary estimate of the critical neutron fluence on the operation performance of a functional logic cell. The four flip-flops were exposed to the TRIGA neutron/gamma environment while operated dynamically at a clock rate of approximately 1 kHz. The bias current of the flip-flops was set at approximately 200 μA, or 40 μA per inverter. Operation of the flip-flops was monitored during exposure. The most susceptible sample failed after 10 minutes of exposure, the next after 14 minutes of exposure, and the last two after approximately 20 minutes of exposures. Critical neutron fluences were 2.4 to 4.7 x 10^{13} n/cm^2 (1 MeV equivalent).

3.3 Total Ionizing Radiation Dose Effects Study

Surface effects resulting from total ionizing dose in I^2L structures can degrade the gain of both the pnp and npn transistor elements. The lateral pnp transistor is sensitive to surface recombination in carrier transport from emitter to collector, and the current gain of the npn transistor is sensitive to the surface recombination current of the emitter overlap

diode. In an unhardened I^2L structure, surface effects could be aggravated by routing positively-biased metallization lines over critical base regions. Studies at NAD (Crane) on preliminary samples provided by a major semiconductor manufacturer indicate degradation of the pnp and npn transistor gains at total ionizing doses as low as 10^4 rads/(Si) with significant degradation at total dose of 10^5 rads/(Si).– The observed effect was most severe at very low bias currents as would be expected from surface effects. The effect of surface recombination on the npn transistor element can be illustrated analytically with the results as shown in Figure 3-5. The gain of an npn transistor element of typical geometry, doping profile, and bulk semiconductor parameters is calculated as a function of the excess base length. In this case, the zero excess base length represents the geometry of a minimum size single-output inverter, and the maximum excess base length corresponds to that necessary if it were required to pass four metallization lines over the base to get metallization cross-overs. The highest gain is obtained with a surface recombination velocity of 10 cm/s or less which is representative of that observed in unirradiated structures. A surface recombination value of 10^5 cm/s is a very large value, even accounting for radiation enhanced effects.

Preliminary evaluation of I^2L total-ionizing-radiation-dose susceptibility was investigated experimentally with the exposure of four R-S flip-flop samples to the radiation environment of the Northrop Co-60 hot cell. The flip-flops were each biased to 200 μA power supply current and the output voltage of both the Q and $\overline{Q}$ outputs was monitored continuously up to a total-dose exposure of 1 Mrad(Si). Results of the test are summarized in Table 3-1 showing the total power supply current

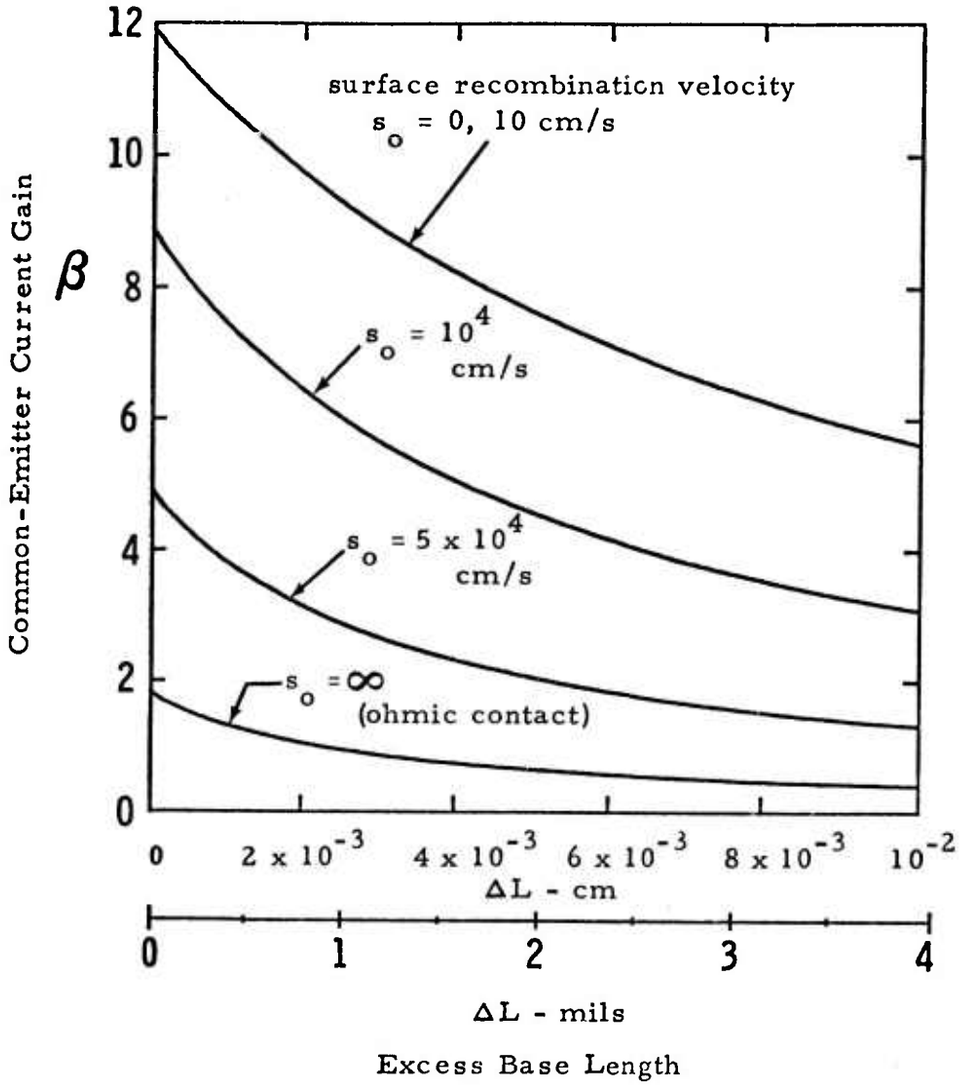


Figure 3-5. Npn transistor-base surface effects.

TABLE 3-1. I^2L FLIP-FLOP TOTAL-DOSE-EFFECTS MEASUREMENTS

Flip-Flop Sample	Q-Output, V		$\overline{Q}$-Output, V	
	$\gamma = 0$	$\gamma = 1$ Mrad(Si)	$\gamma = 0$	$\gamma = 1$ Mrad(Si)
A13	0.817	0.801	0.020	0.026
	0.026	0.038	0.817	0.801
B21	0.810	0.792	0.019	0.026
	0.026	0.048	0.808	0.790
A29	0.811	0.802	0.017	0.026
	0.021	0.032	0.810	0.802
A41	0.813	0.797	0.017	0.022
	0.023	0.033	0.805	0.797

for the four flip-flops as well as the "one" and "zero" state output voltages for pre-irradiation and after exposure to 1 Mrad(Si). These results demonstrate virtually no change in dc output levels of the flip-flop at radiation levels of up to 1 Mrad(Si). It must be pointed out, however, that the loading on the flip-flop cells is very modest since the fan-out requirement is only unity, and operation was well above the minimum operating bias current levels. The operating bias current was, however, representative of that used in an LSI array design to obtain the required switching response. More extensive characterization of total-dose-induce performance degradation is planned in follow-on studies of this program.

3.4 Transient Photoresponse Study

Transient photoresponse of I^2L arrays has been considered in terms of logic error as a function of radiation pulse width, and operational survivability at exposure levels above the transient upset level. In the initial

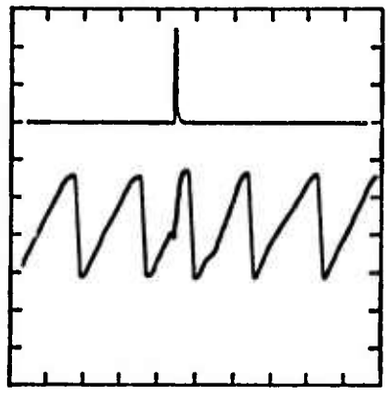
characterization, the transient photoresponse of samples of a five-stage ring counter was measured in the 30 ns 2-MeV flash x-ray environment. Observed waveforms for peak radiation levels of 5×10^8 and 5×10^{10} rads(Si)/s are presented in Figure 3-6. At the exposure level of 5×10^8 there definitely is an effect, but because of the feedback nature of the ring counter the effect cannot be interpreted as a logic upset. Analysis of the I^2L structure indicates that the first-order effect is the photocurrent of the npn transistor emitter diode. This photocurrent, if it were to exist as a dc current, acts just as the collector current of the pnp transistor, that is, to provide bias current for the switched npn transistors. Thus, as we irradiate the ring counter, the operating bias current is increased, decreasing the stage propagation delay and causing a transient increase in the oscillation frequency. This is dramatically illustrated by the waveform resulting from the exposure to 5×10^{10} rads(Si)/s as shown in Figure 3-6. The high level exposure also illustrates recovery in a few microseconds without latch-up or anomalous photoresponse.

Transient photoresponse of I^2L was investigated by the measurement of the pulsed-ionizing-radiation-induced change-of-state upset threshold on a sample set of R-S flip-flops. Five flip-flop samples were exposed to the narrow-pulse (30 ns) ionizing radiation environment of the NRTC 2-MeV flash x-ray. Three of these five samples were then subsequently exposed to the wide-pulse (4 μs) ionizing radiation environment of the IRT Linac. The logic state of the flip-flop was monitored with minimum electrical loading to determine the pre-shot/post-shot condition and detect a radiation-induced change of state. For two of the samples in the FXR experiments, the flip-flop bias current was varied by a factor

A) Pin Diode Output
1.0V, 1.0 μs/div.

B) Ring Counter Output
0.2V, 1.0 μs/div.

$\dot{\hat{\gamma}} = 5 \times 10^{8}$ rads(Si)/s

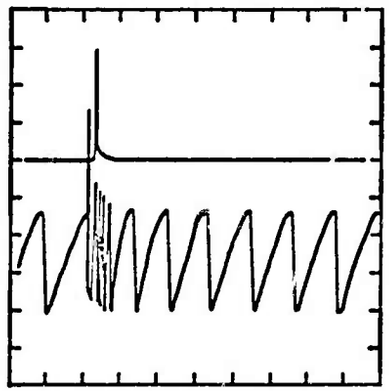


Ring Counter Output Photoresponse, 2 MeV Flash X-Ray, $\dot{\hat{\gamma}} = 5 \times 10^{8}$ rads(Si)/s

A) Pin Diode Output
20V, 2.0 μs/div.

B) Ring Counter Output
0.2V, 2.0 μs/div.

$\dot{\hat{\gamma}} = 5 \times 10^{10}$ rads(Si)/s



Ring Counter Photoresponse, 2 MeV Flash X-Ray, $\dot{\hat{\gamma}} = 5 \times 10^{10}$ rads(Si)/s

Figure 3-6. I^2L five-stage ring counter photoresponse.

of two above and below the design bias current to determine possible variations of the radiation-induced upset level.

The schematic diagram and composite mask layout of the I^2L R-S flip-flop are shown in Figures 3-7 and 3-8. The flip-flop is essentially two inverters connected regeneratively with a gated inverter for clocking of the Set and Reset inputs. The test circuit used for the measurement of the radiation-induced logic upset is shown in Figure 3-9. The input state of the flip-flop is determined by the resistors at the Set and Reset inputs that simulate "on" or "off" I^2L logic outputs. During ionizing radiation exposure the clock input ($\overline{C}_k$) is in the high impedance state setting the drive inverter "on" and the parallel gates of the flip-flop "off" such that the state of the flip-flop is unrestrained. The outputs of the flip-flop were monitored through 10 k Ω series resistance to minimize the loading effects of the instrumentation cable drivers. This also meant that the waveform transmitted by the cable drivers was essentially just the integrated output response of the flip-flop and no data could be obtained concerning the time-dependent output voltage response. It was felt that it was of critical importance to minimize the loading on the basic flip-flop cell since it was not designed to drive off-chip loads, at the sacrifice of measuring the output waveform.

No electrical or radiation-induced latch-up has been observed on any I^2L samples. Latch-up is eliminated from the non-isolated I^2L array because the input supply voltage (one base-emitter diode voltage drop) is less than the sustaining voltage of any known latch-up mechanism.

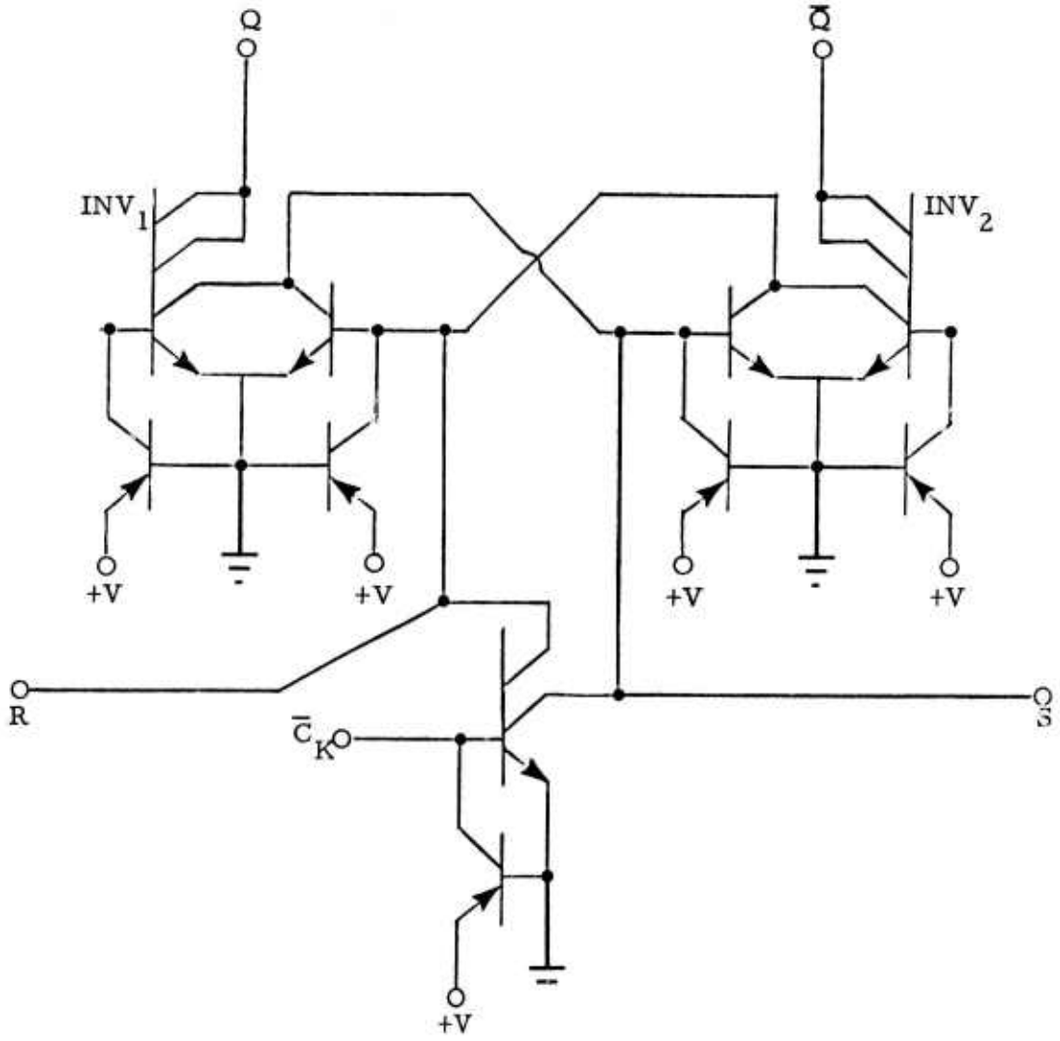


Figure 3-7. I^2L R-S flip-flop schematic.

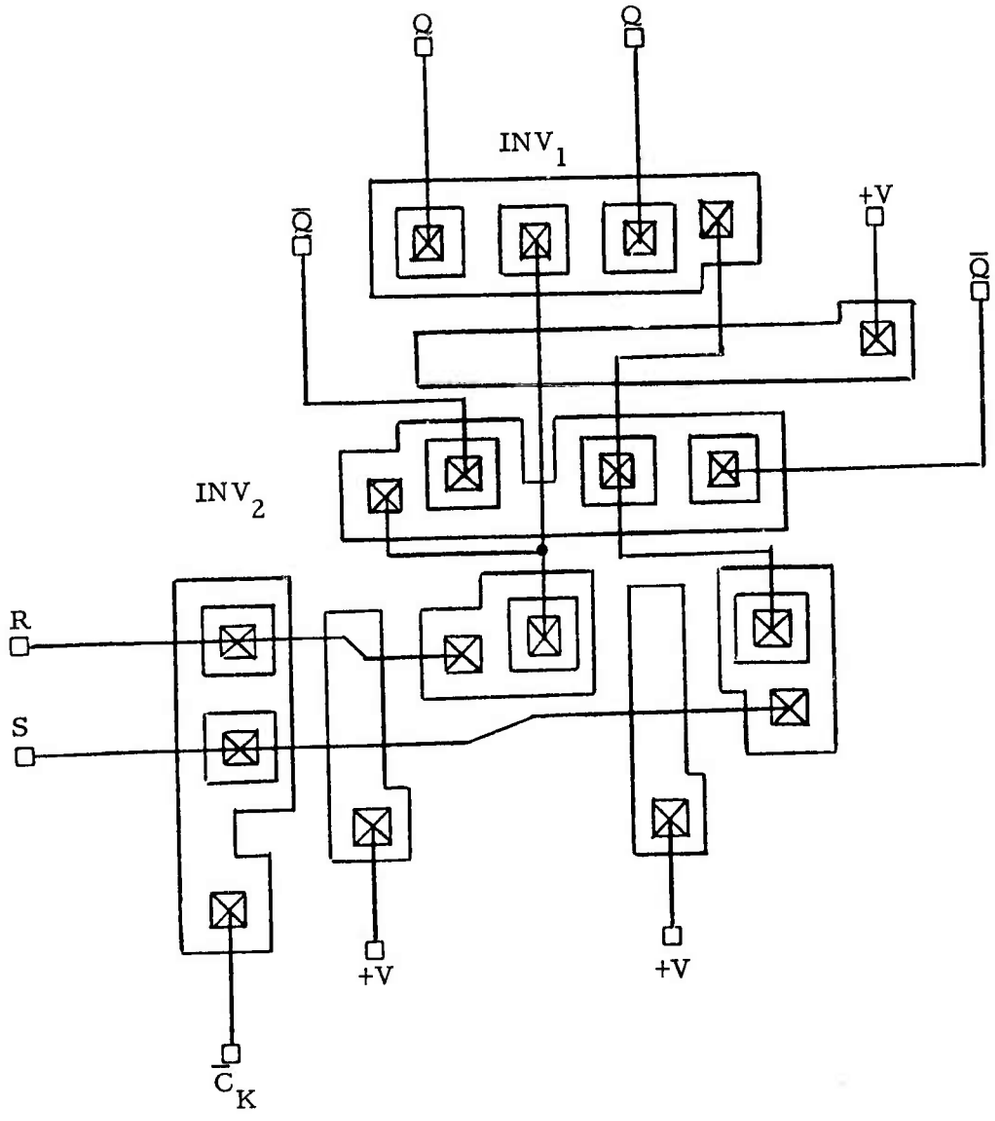


Figure 3-8. Simplified layout of the I^2L R-S flip-flop.

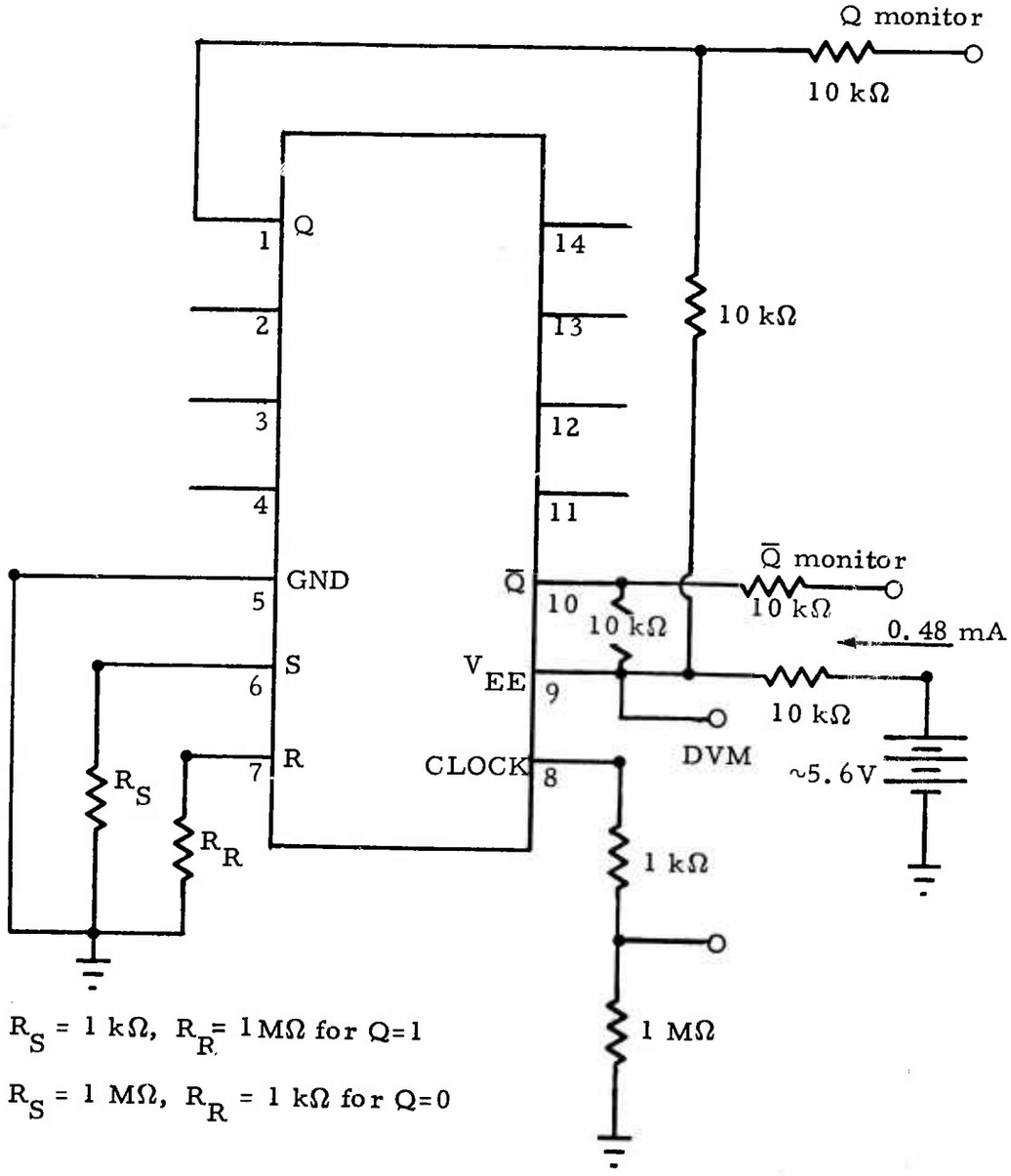


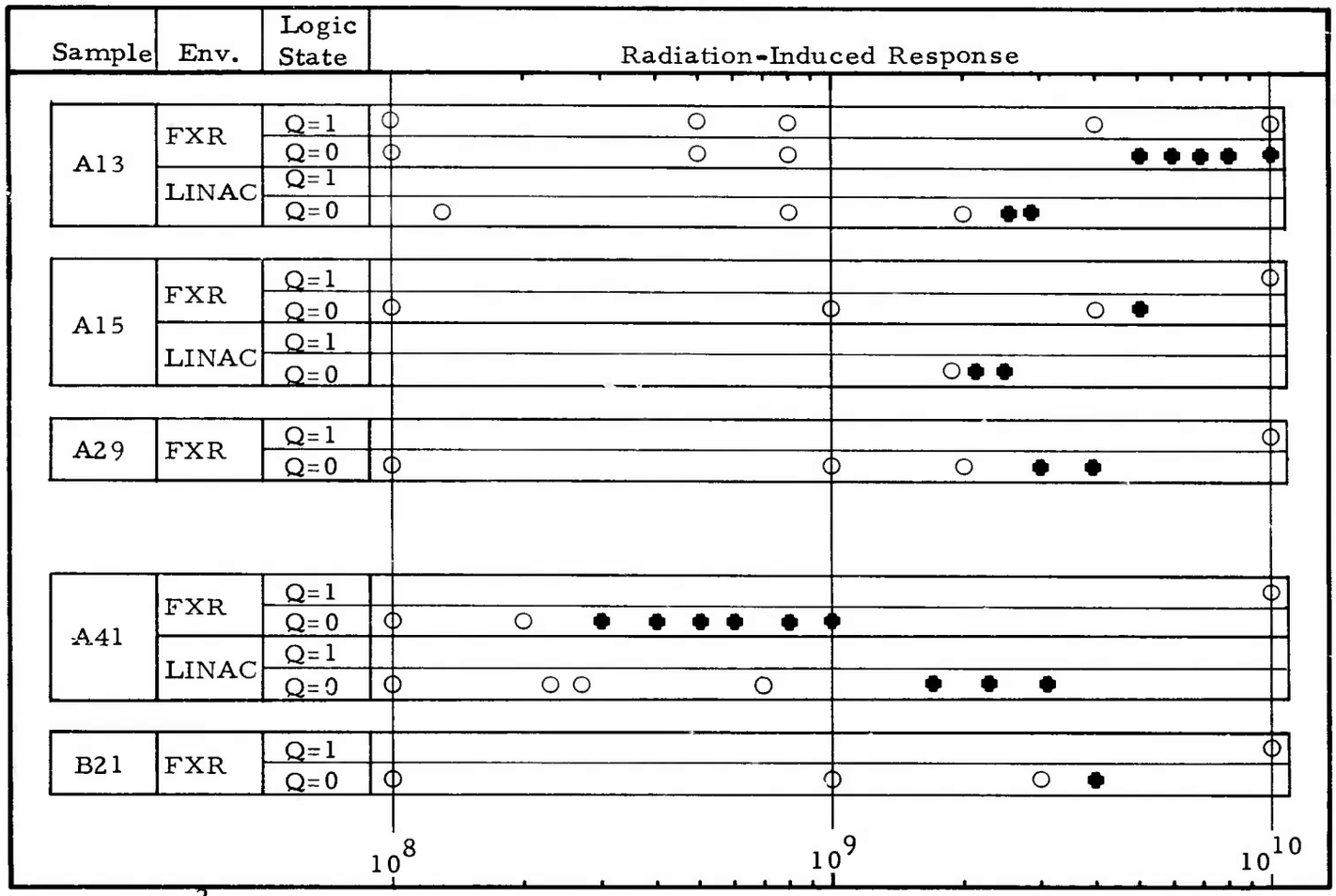
Figure 3-9. Test circuit for monitoring I^2L flip-flop radiation-induced change of state.

Results of the transient photoresponse experiments are summarized in Tables 3-2 and 3-3. In Table 3-2, the result of all radiation exposures is summarized for samples biased at a power supply current of 80 μA (which is the design operation value). As shown, the radiation-induced upset level varied from 0.3 to 5 x 10^9 rads(Si)/s for the five samples exposed in the flash x-ray, and varied from 1.8 to 2.5 x 10^9 rads(Si)/s for those three of the five subsequently exposed to the wide LINAC pulse. The photoresponse of sample A41 is significantly different from the other samples in that the upset level in the narrow-pulse flash x-ray was much lower than that of the other four samples, and in that the upset level increased when exposed to the wide-pulse ionizing radiation environment rather than decreasing as did the other samples. In all other digital microcircuit photoresponse studies on devices of virtually all technologies, the logic upset level decreases with increasing ionizing radiation pulse width. Without considering sample A41, the narrow-pulse upset level would be 3 to 5 x 10^9 rads(Si)/s compared to the wide-pulse upset level of 2 to 3 x 10^9 rads(Si)/s.

Variation in radiation-induced upset level with flip-flop bias current is summarized in Table 3-3. While results on only two samples in the narrow-pulse flash x-ray environment are too limited to make general conclusions, the effect of power supply bias current seems to be very small.

Analytical simulation of the flip-flop photoresponse requires the development of a non-linear radiation-inclusive I^2L model not yet available. Intuitively, however, it can be assumed that the first-order effect is the photocurrent of the emitter-base diode of the npn transistor. Also, it

TABLE 3-2. SUMMARY OF OBSERVED I^2L FLIP-FLOP PHOTORESPONSE



I^2L R-S Flip-Flop, I_{EE} = 80 μA, FXR $t_p \cong$ 30 ns, LINAC $t_p \cong$ 4 μs

TABLE 3-3. VARIATION OF I^2L R-S FLIP-FLOP CHANGE-OF-STATE THRESHOLD WITH BIAS CURRENT

SAMPLE A13	I_{EE} = 40 μA	$\dot{\gamma}_c = 5 \times 10^9$ rads(Si)/s
	I_{EE} = 80 μA	$\dot{\gamma}_c = 5 \times 10^9$ rads(Si)/s
	I_{EE} = 160 μA	$\dot{\gamma}_c = 5 \times 10^9$ rads(Si)/s
SAMPLE B21	I_{EE} = 40 μA	$\dot{\gamma}_c = 4 \times 10^9$ rads(Si)/s
	I_{EE} = 80 μA	$\dot{\gamma}_c = 4 \times 10^9$ rads(Si)/s
	I_{EE} = 160 μA	$\dot{\gamma}_c = 5 \times 10^9$ rads(Si)/s

would be expected that this photocurrent is proportional to the emitter-base junction area. From the composite mask diagram it can be seen that the junction area of the inverter on the reset side of the flip-flop is 5% greater than that on the set side of the flip-flop. This was done for the convenience of laying out the metallization pattern. This slight asymmetry has little effect on the electrical performance of the flip-flop and radiation-hardness was not a consideration in the cell development. The photocurrent generators of the I^2L inverter, as added to the flip-flop schematic in Figure 3-7, are in the direction to increase the normal bias current and should actually improve flip-flop performance. As a practical matter, however, there will be some radiation level at which the voltage drops in the substrate due to the excess current will obscure the logic voltage levels and result in logic upset. For the I^2L flip-flop under study, however, the first-order effect seems to be the unbalance in photocurrents. All observed radiation-induced upsets were transitions from the Q = 0 state to the Q = 1 state with no transistions

observed in the opposite direction. This is consistent with increased bias currents on the Q side of the flip-flop as is the case in the mask layout. The observed transient upset levels, therefore, are a worst-case estimate for those that could be anticipated from a radiation-hardened flip-flop cell.

Results on the observed transient upset level, even in light of the inverter symmetry are quite impressive, however. It must be remembered that the I^2L flip-flop is a low-power LSI logic cell. These results indicate transient upset levels of 4×10^9 rads(Si)/s even with the cell biased at a power level of 32 μW. This upset level is significantly greater than that observed in any other bipolar or MOS microcircuit technology with the exception of CMOS/SOS or radiation-hardened TTL operated at approximately 1000 times the power level.

4.0 OPTICAL COUPLER STUDY

Application of data communication systems linked by fiber optics is under consideration for several avionics, shipboard, and ground tactical systems.[9] The purpose of this study was to investigate the radiation susceptibility of the source and receiver electronics independent of the transmission media. The semiconductor devices selected for study were three types of optical couplers: 1) a light-emitting diode with a PIN diode sensor output; 2) a light-emitting diode with a bipolar amplifier output; and 3) a light-emitting diode with an amplifier and digital gate output. Most of the effort in this study was devoted to the characterization of electrical response, transient photoresponse, and neutron-induced permanent damage in the Hewlett-Packard HP 5082-4360 diode/digital-gate coupler.

Characterization of the optical couplers is somewhat of a change of scope from the general study of digital MSI/LSI arrays which has been the principal effort of this program. The effort, in this case, is intended to supplement studies in other laboratories on the radiation effects in fiber-optics material to gain insight into the overall fiber-optics digital communication system susceptibility.[10-11] In addition, the combination of the PIN sensor diode to a bipolar microcircuit requires a combination of circuit and processing parameters not encountered in other MSI arrays.

Results of the study showed that the radiation susceptibility of the diode/diode optical couplers was straightforward and reasonable to model and simulate analytically. Results of the diode/amplifier and diode/digital-gate couplers were, on the other hand, quite complex and exhibited

non-linearity, high sensitivity, and some anomalous permanent damage which may have been the result of either electrical operation or ionizing-radiation-dose-rate-induced effects.

4.1 MCD2 Diode/Diode Optical Coupler Characterization

The Monsanto MCD2 is a diffused planar silicon PIN photodiode optically coupled to a diffused planar gallium arsenide light-emitting diode. Samples were obtained mounted in a six-lead plastic DIP package. The coupler is intended for applications where high input/output isolation is required with fast switching response, at the penalty of relatively low current transfer gain. Four samples of the couplers were characterized in terms of dc performance, electrical switching response, and radiation-induced transient photoresponse. Results of the experimental characterization are presented in terms of parameter values derived for a radiation-inclusive mathematical model. Analytical simulation of observed effects were verified with computations using the NET-2 computer program. Extra effort is required to take the results of an experimental characterization and transform them into a quantitative mathematical model. The advantage, however, is that the experimental results can be used in analytical simulation for test conditions other than those of this specific characterization.

The mathematical model used for the diode/diode coupler is shown in Figure 4-1. Diode D_1 is the gallium arsenide light-emitting input diode, and diode D_2 is the planar silicon PIN output diode. Coupling between the diode is accomplished, in the mathematical model, by a voltage-controlled current source where the dependence current generator is proportional to the voltage across the small resistor R_1. The proportionality

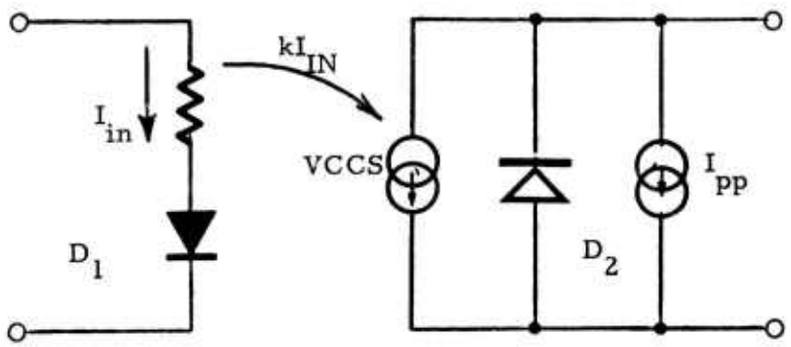


Figure 4-1. NET-2 diode/diode coupler model.

constant between the input current and output current generator is fixed at a single value in the model.

The dc characteristics of the diodes are defined by the diode equation,

$$I = I_s \left[\exp(\theta V) - 1 \right], \tag{1}$$

the shunt conductance, G_c, and the bulk resistance R_b. Electrical switching response is represented by adding the voltage-dependent depletion capacitance given by,

$$C_t = C \left[1 - (V/V_z) \right]^{-N}, \tag{2}$$

and the diode diffusion capacitance given by,

$$C_d = \left[\theta I_s \exp(\theta V) \right] / \omega. \tag{3}$$

Radiation-induced transient photoresponse in the diode/diode coupler is represented by the output diode photocurrent generator. The output photocurrent is defined in terms of prompt and delayed components. The current

I_{p1} represents the photocurrent directly proportional to the time-dependent ionizing radiation intensity in units of mA/rads(Si)/ns. The current component I_{p2} represents the steady-state value of the delayed or diffusion component of the diode photocurrent which varies with a single-time-constant exponential with the time constant T in ns.

Dc electrical characteristics of the MCD2 samples were measured in the test circuit shown in Figure 4-2. The most critical aspect of the dc characterization is the current transfer characteristic. Experimental results for one sample on the current transfer characteristic, input diode current-voltage characteristic, and output current-voltage characteristic are shown in Figures 4-3, -4, and -5, with the results as simulated using the model and NET-2.

Characterization of the electrical switching response of the diode/diode coupler must include the switching response of the input diode as well as the overall switching response to the output. One of the principal advantages

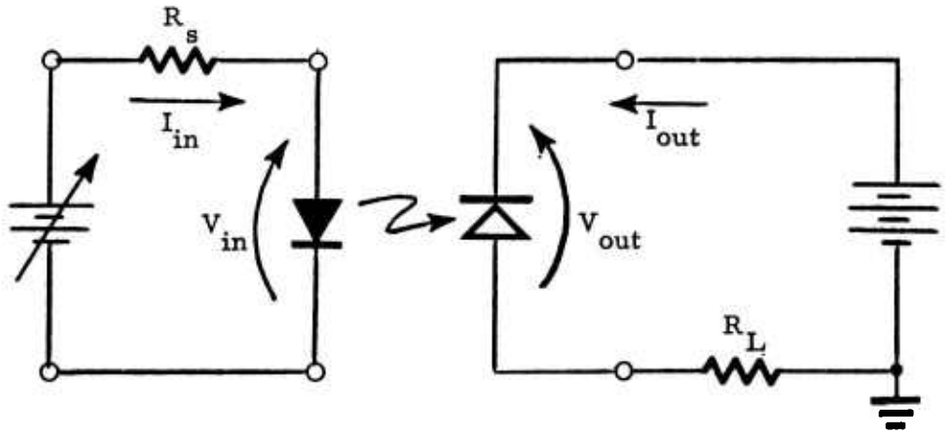


Figure 4-2. MCD2 dc test set-up.

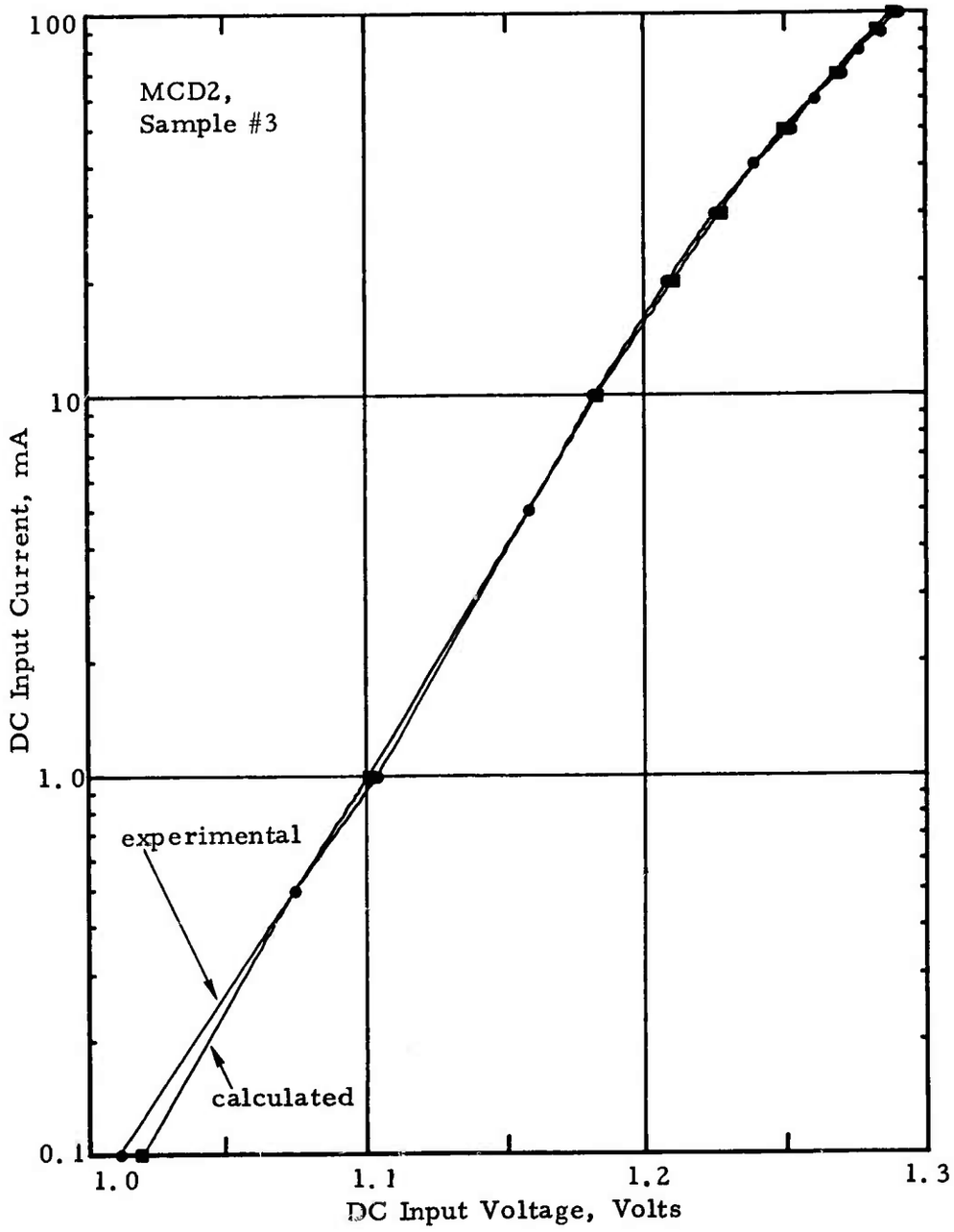


Figure 4-3. Measured and calculated MCD2 diode/diode coupler input I-V characteristics.

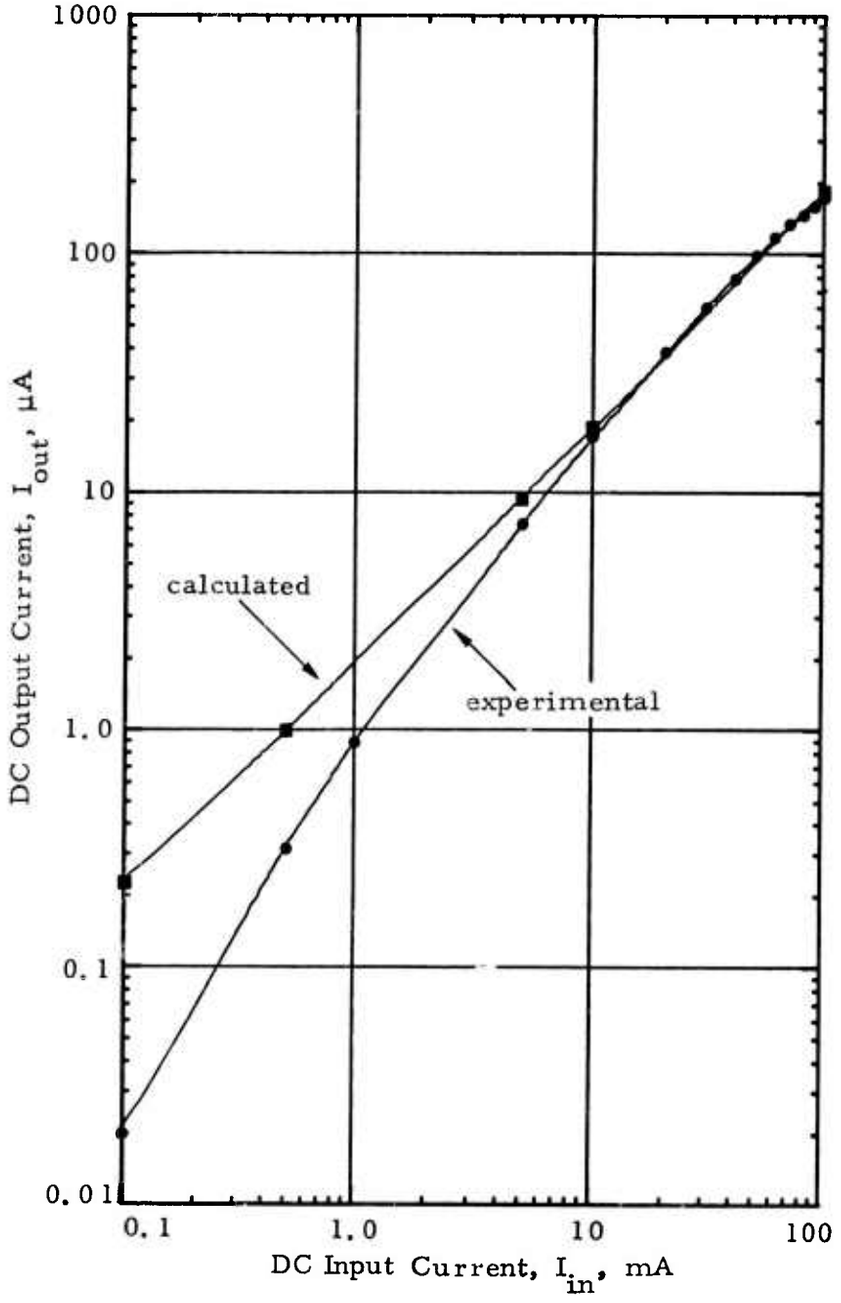


Figure 4-4. Measured and calculated MCD2 current-current transfer characterics.

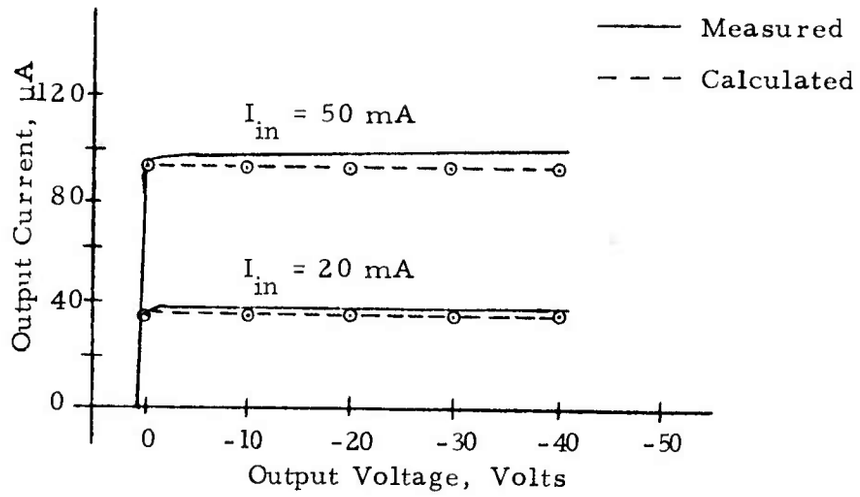
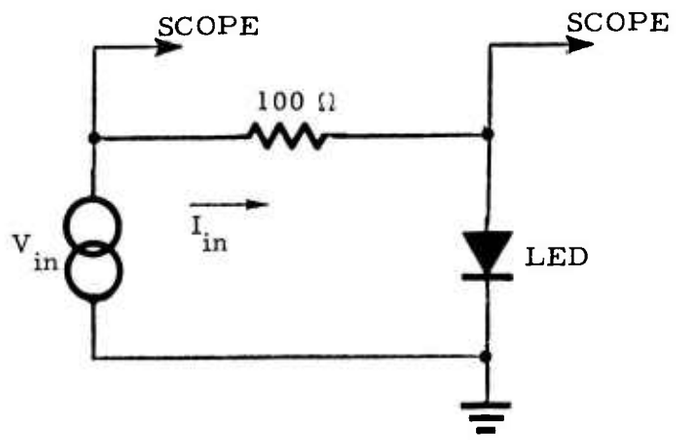


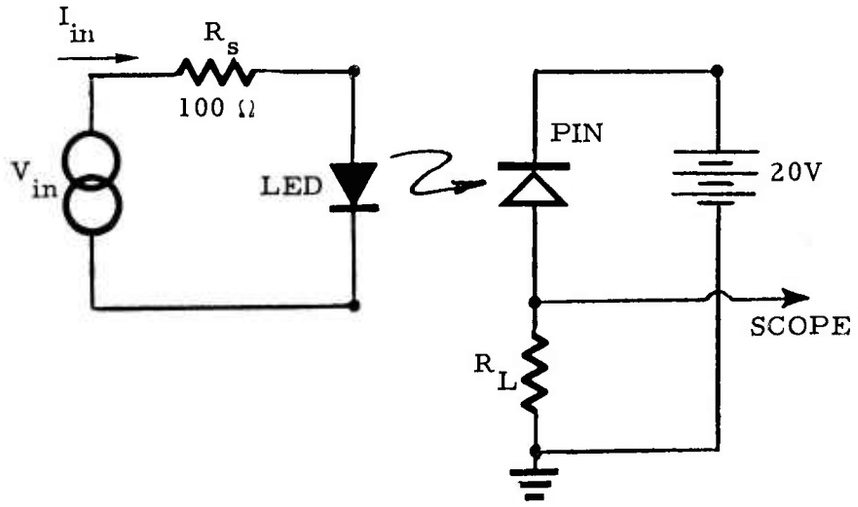
Figure 4-5. MCD2 output current-voltage characteristic.

of the diode/diode coupler is its fast switching response. The test circuits used to measure the input diode and overall switching response are shown in Figure 4-6. The input electrical pulse was adjusted for a rise time of 15 ns and a fall time of 10 ns. Capacitance of the scope probe was 7 pF. Electrical switching response of the input diode and NET-2 simulation is shown for one example in Figure 4-7. The overall electrical switching response was measured for all samples as a function of source resistance, R_s, output load resistance, R_L, and input drive current levels. Experimental results and analytical simulation are shown in Figures 4-8 and 4-9 for values of load resistance 1, 5 and 10 kΩ and drive currents of 20 mA and 50 mA.

Model parameters for the dc and electrical switching response of the four diode/diode coupler samples are summarized in Table 4-1.



(a) Input switching response circuit.



(b) Output switching response circuit.

Figure 4-6. Test circuits for MCD2 switching response measurements.

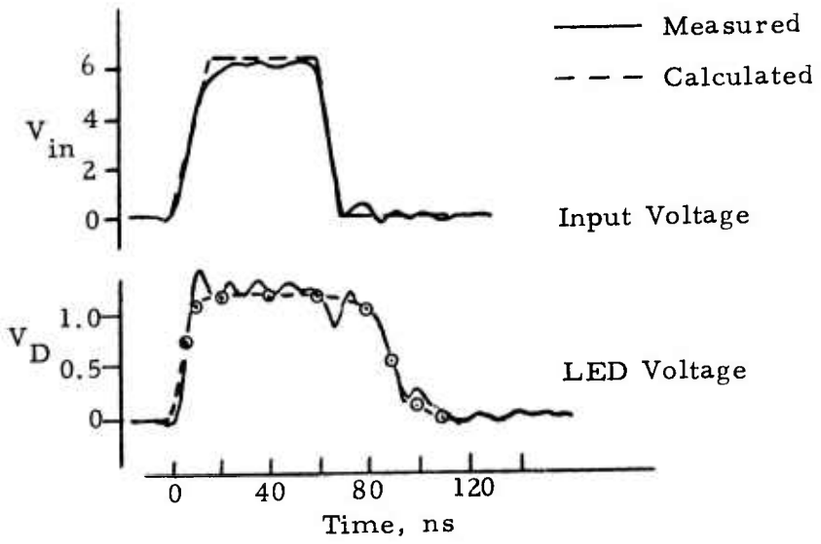


Figure 4-7. MCD2 input switching response.

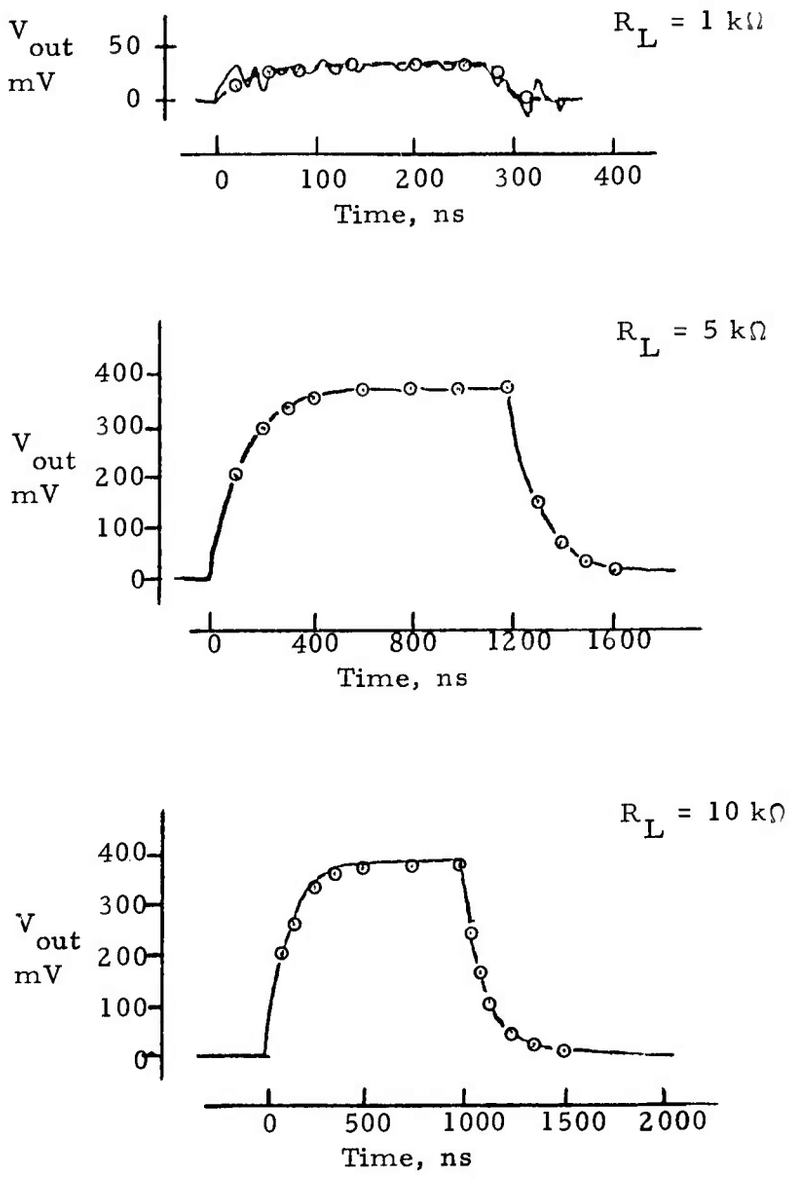


Figure 4-8. MCD2 output switching response, pulsed input current, I_{in} = 20 mA.

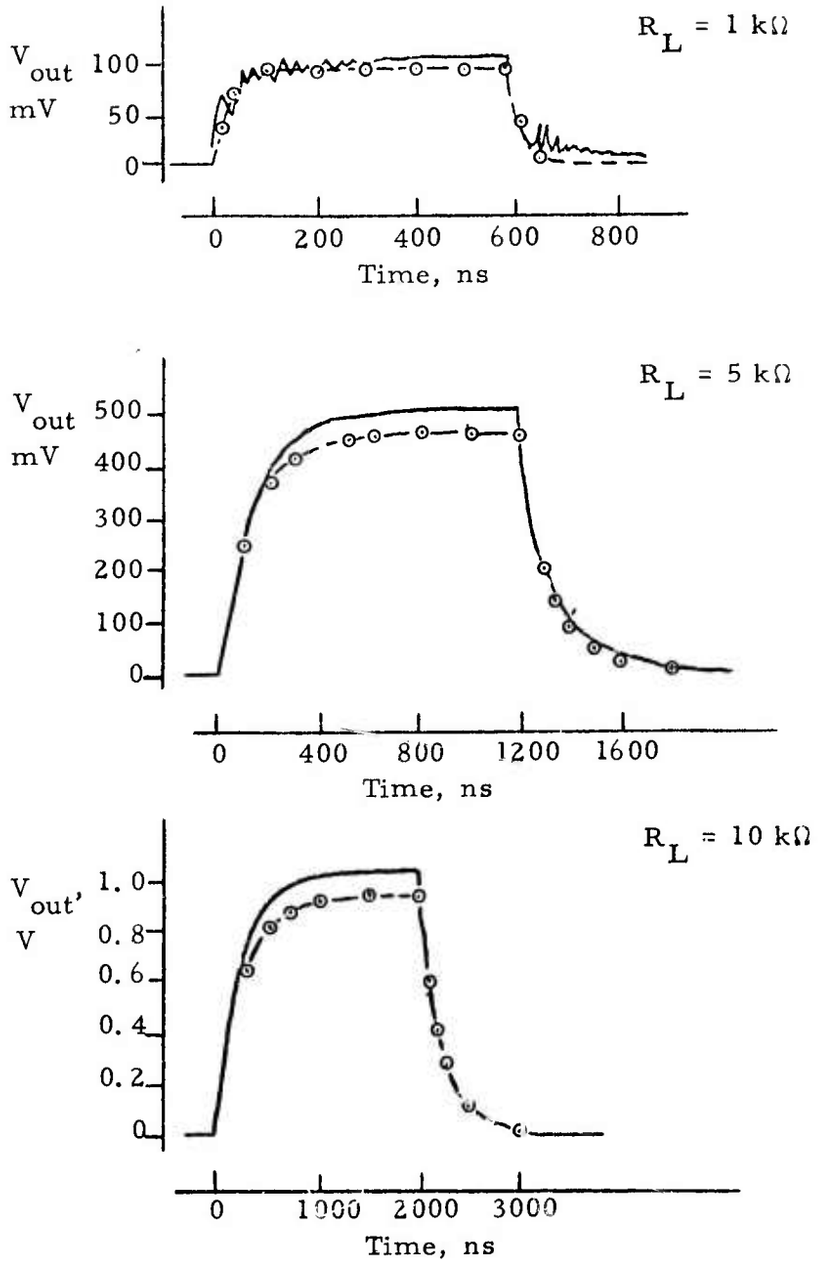


Figure 4-9. MCD2 output switching response, pulsed input current, I_{in} = 50 mA.

TABLE 4-1. SUMMARY OF MCD2 NET-2 MODEL PARAMETERS

	SAMPLE #1		SAMPLE #2		
	D1 (LED)	D2 (PIN)	D1 (LED)	D2 (PIN)	Units
C	50	30	50	37	pF
GC	1×10^{-6}	2×10^{-6}	1×10^{-6}	2×10^{-6}	$(k\Omega)^{-1}$
IS	8.6×10^{-14}	8.02×10^{-8}	7.02×10^{-14}	4.17×10^{-8}	mA
N	0.5	0.5	0.5	0.5	–
RB	1.8×10^{-4}	5×10^{-3}	8×10^{-4}	8×10^{-3}	kΩ
(θ)TH	27.5	25.9	27.4	27.7	$(v)^{-1}$
VZ	1.0	0.55	1.0	0.55	–
(ω)W	0.1	0.1	0.1	0.1	$(ns)^{-1}$
K	2.1×10^{-3}		1.92×10^{-3}		mA/v

	SAMPLE #3		SAMPLE #4		
	D1 (LED)	D2 (PIN)	D1 (LED)	D2 (PIN)	Units
C	53	45	50	40	pF
GC	1×10^{-6}	2×10^{-6}	1×10^{-6}	2×10^{-6}	$(k\Omega)^{-1}$
IS	1.73×10^{-14}	1.85×10^{-8}	1.64×10^{-12}	1.10×10^{-8}	mA
N	0.5	0.33	0.5	0.33	–
RB	2.8×10^{-4}	1×10^{-2}	8×10^{-4}	1×10^{-2}	kΩ
(θ)TH	28.8	29.1	24.7	29.6	$(v)^{-1}$
VZ	1.0	0.55	1.0	0.55	–
(ω)W	0.1	0.05	0.1	0.05	$(ns)^{-1}$
K	1.86×10^{-3}		1.12×10^{-3}		mA/v

The transient photoresponse of the MCD2 diode/diode coupler was determined through a series of measurements on two samples in the ionizing radiation environment of the NRTC 2-MeV flash x-ray. The general test set-up for the photoresponse measurements is shown in Figure 4-10. The output detector diodes were reverse-biased at 10V through a load resistor that was varied from 100 Ω to 1 kΩ. Initially, the output photoresponse was measured on one sample as a function of bias conditions on the input LED diode as well as with variations in load resistance. It was found that the output photoresponse was essentially independent of the bias conditions on the input diode including forward-bias, zero-bias (i.e., short-circuit), and reverse-bias. The measured unsaturated output photoresponse was that of the output diode photocurrent through the output load resistance and shunt capacitance. Time dependence of the diode photocurrent was approximately that of the ionizing radiation pulse as would be expected from a fully-depleted PIN diode. At high ionizing radiation dose rates, the output diode was saturated and the output waveform increased in pulse width. In the exposure of the second coupler sample, only the variation with output load and radiation dose rate was included with independence of the input diode bias assumed from the first test results. Measured photoresponse on the MCD2 diode/diode couplers is summarized in Table 4-2.

Results of the photoresponse measurement suggest that the total photoresponse can be simulated by a prompt diode photocurrent added to the output PIN diode. The magnitude of the prompt photocurrent is approximately 1×10^{-10} A/rads(Si)/s, or a constant of 100 mA/rad(Si)/ns for IP1 of the NET-2 model. In saturation, the radiation-induced storage time can be represented approximately as,

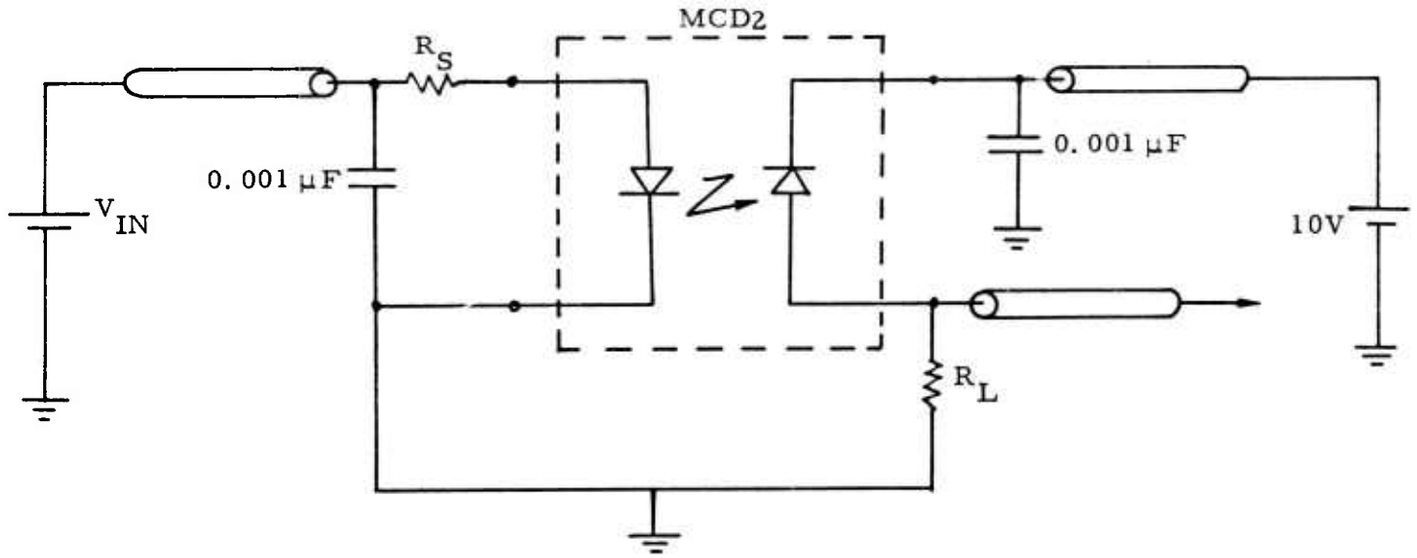


Figure 4-10. MCD2 photoresponse test circuit.

TABLE 4-2. SUMMARY OF MCD2 OPTICAL COUPLER PHOTORESPONSE, V_{out} = 10V

Test Conditions	$\hat{\dot{\gamma}}$ (rads(Si)/s)	$\Delta\hat{e}_o$ (volts)	Output transient pulse width (ns)	Sample
I_{in} = 0, R_L = 1 kΩ	2 x 10^7	1.2	50	#1
	5 x 10^8	11.0	200	
	1 x 10^{10}	11.0	2300	
I_{in} = 50 mA, R_L = 1 kΩ	2 x 10^7	1.1	50	#1
	5 x 10^8	10.5	200	
	1 x 10^{10}	11.0	2300	
V_{in} = -2V, R_L = 1 kΩ	2 x 10^7	1.1	50	#1
	5 x 10^8	11.0	220	
	1 x 10^{10}	11.0	2300	
I_{in} = 0, R_L = 100 Ω	2 z 10^7	0.25	30	#1
	5 x 10^8	5.5	30	
	1 x 10^{10}	11.0	440	
I_{in} = 0, R_L = 1 kΩ	2 x 10^7	1.0	50	#2
	5 x 10^8	11.0	200	
	1 x 10^{10}	11.0	2000	
I_{in} = 0, R_L = 100 Ω	2 x 10^7	0.2	30	#2
	5 x 10^8	4.7	30	
	1 x 10^{10}	11.0	400	

$$t_{s\dot{\gamma}} \cong \tau_s \, \mathrm{erf} \left(\frac{i_{pp}}{i_{pp} + \frac{V}{R_L}} \right)^{1/2} \qquad (4)$$

with a value of 500 ns for τ_s. In the NET-2 model, the storage time constant must be included in the constant, W, for the diode diffusion capacitance.

4.2 Hewlett-Packard 5082-4360 Optically-Isolated Gate

The Hewlett-Packard 5082-4360 optically-isolated gate is the combination of a gallium-arsenide-phosphide (GaAsP) light-emitting input diode with an optically-coupled output network which consists of a PIN photodiode, a high-gain linear amplifier and a Schottky-clamped open collector output transistor. The output circuit also has a DTL-type enable input to provide strobing of the detector. The coupler design enables high dc and ac isolation between input and output with DTL/TTL circuit compatibility. The schematic diagram of the 4360 is shown in Figure 4-11. Complexity of the output circuitry is on the same order as that found in small digital MSI arrays.

Five samples of the diode/gate coupler were characterized initially in terms of dc transfer characteristics, dc output characteristics and electrical switching response. Results of the dc transfer and output characteristics on a typical sample are shown in Figures 4-12 and 4-13. Electrical switching response was determined by measurement of the propagation delay between the output and input and enable signals. It was noted in the switching response characterization that the bypass capacitor on the supply voltage was critical. Its purpose is to stablize

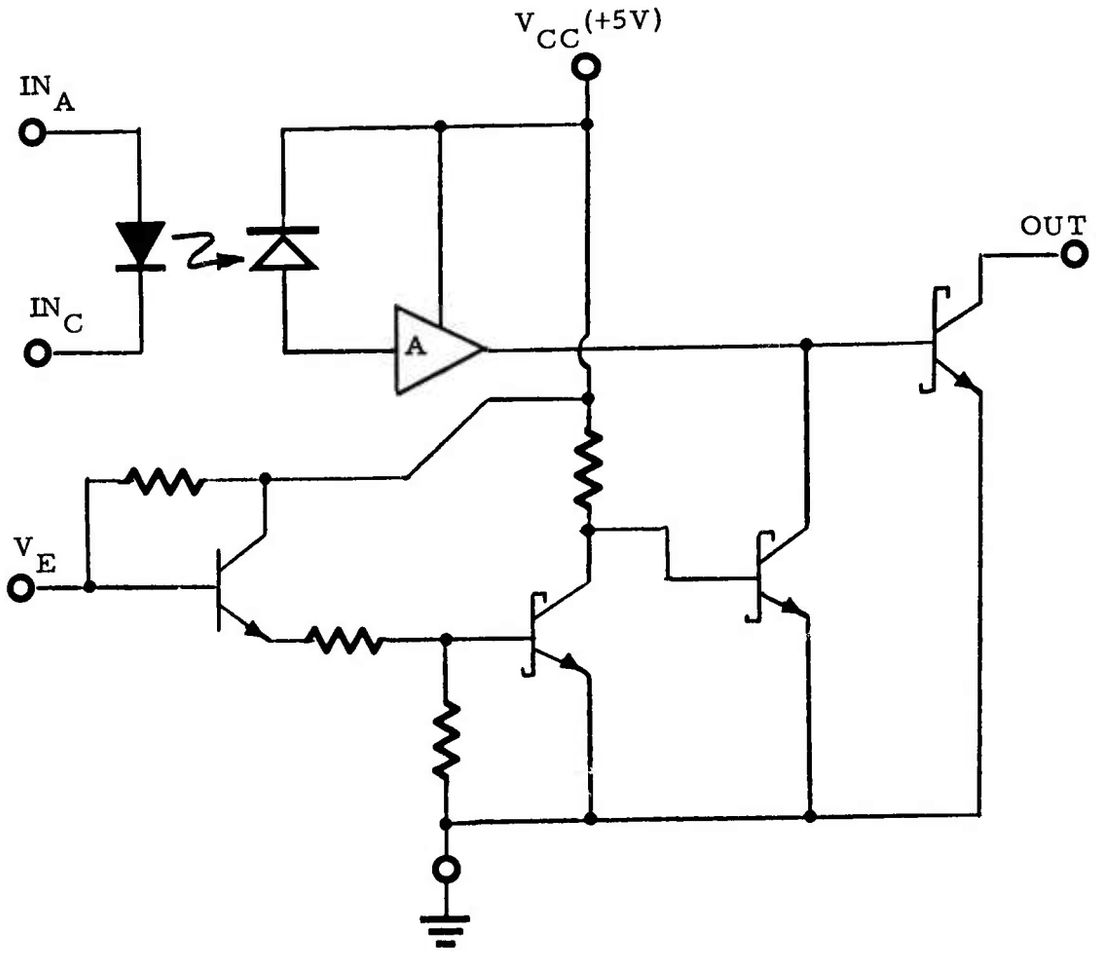


Figure 4-11. HP 5082-4360 optically-coupled gate.

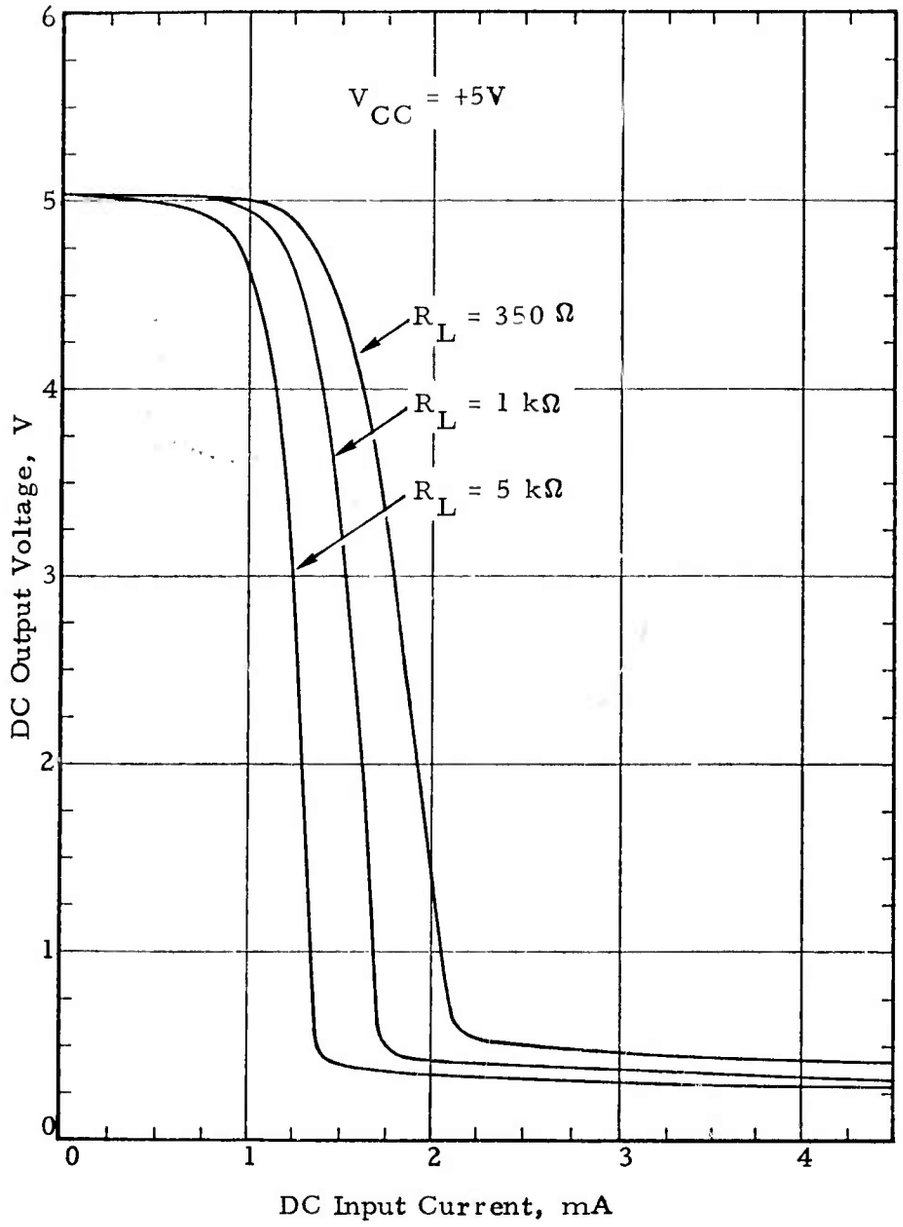


Figure 4-12. HP 4360 diode/gate coupler dc transfer characteristic.

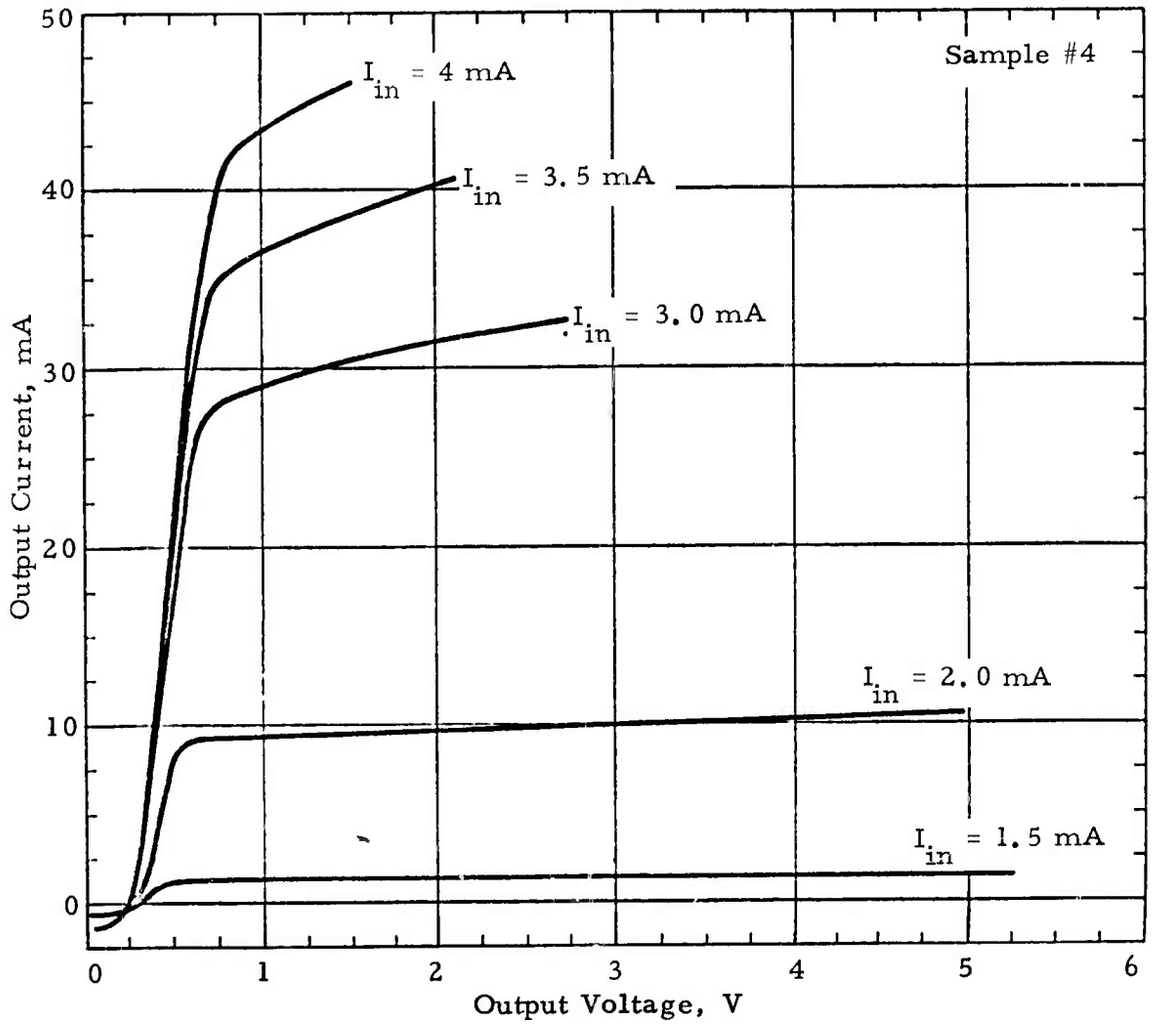


Figure 4-13. HP 4360 output current-voltage characteristics.

the operation of the high-gain linear amplifier. Failure to provide sufficient bypassing may impair the transfer and switching response. Measured propagation delays on the diode/gate couplers are summarized in Table 4-3.

Characterization of radiation effects on the diode/digital-gate couplers included measurement of the transient photoresponse in the narrow-pulsed ionizing radiation environment of the NRTC 2-MeV flash x-ray, measurement of total-dose-induced permanent damage by exposure to the NRTC Co-60 ionizing radiation environment, measurement of neutron-induced permanent damage by exposure to the NRTC TRIGA neutron/gamma radiation environment, and measurement of the wide-pulse transient photoresponse by exposure to the ionizing radiation environment of the IRT linear accelerator. Overall results of the radiation effects study are summarized in Table 4-4.

4.2.1 HP4360 Narrow-Pulse Transient Photoresponse. The initial series of experiments was the measurement of the photoresponse in the 2-MeV flash x-ray environment. Six samples were included in the tests. Two of the six samples were substantially damaged after a few low-level exposures and two more were somewhat degraded. Permanent damage effects were noted in measurement of the dc transfer characteristics after each series of exposures. Two additional samples were exposed to the complete series of exposures, which ranged from dose rates of 10^7 to 5×10^{10} rads(Si)/s, without damage. The cause of the damage could have been either a destructive oscillation resulting from insufficient power-supply bypassing, a radiation-induced dose rate effect, or permanent damage resulting from total ionizing dose.

TABLE 4-3. SUMMARY OF MEASURED HP4360 SWITCHING RESPONSE

	Input/output		Enable/output	
Sample No.	t_{p1} (ns)	t_{p2} (ns)	t_{p1} (ns)	t_{p2} (ns)
1	60	50	20	80
2	50	80	25	340
3	60	60	30	200
4	50	60	20	90
5	50	60	25	100

17

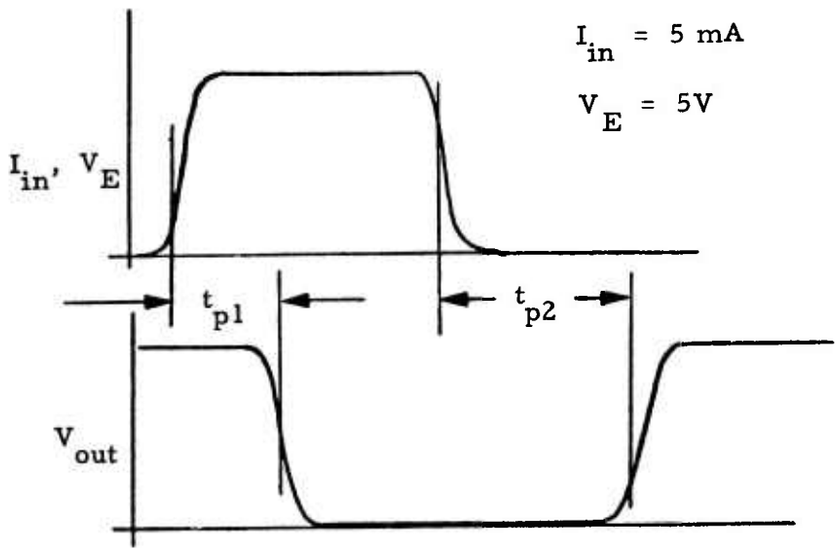


TABLE 4-4. SUMMARY OF OBSERVED HP5082-4360 RADIATION SUSCEPTIBILITY

Transient Photoresponse

Narrow Pulse (t_p = 30 ns)

4 samples

$6 \times 10^5 \leq \dot{\gamma}_c \leq 6 \times 10^6$ rads(Si)/s

Wide Pulse ($t_p \cong 4.5\ \mu s$)

2 samples

$\dot{\gamma}_c \cong 10^5$ rads(Si)/s

Permanent Damage

Total Ionizing Dose

5 samples

$\gamma_c > 1.9$ Mrad(Si)

Neutron Displacement Damage

5 samples

$1.1 \times 10^{13} \leq \Phi \leq 4.9 \times 10^{13}$ n/cm^2 (1 MeV equiv)

Transient photoresponse as measured on those four samples that were not damaged is summarized in Figures 4-14 to -17. Four test conditions are represented in the results shown. Defining zero input current and zero enable voltage as logic "0" and 5 mA input current and +5V enable voltage as logic "1", the test conditions were:

Test Condition	Input Current	Enable Voltage	Test Condition	Input Current	Enable Voltage
I	1	1	III	1	0
II	0	1	IV	0	0

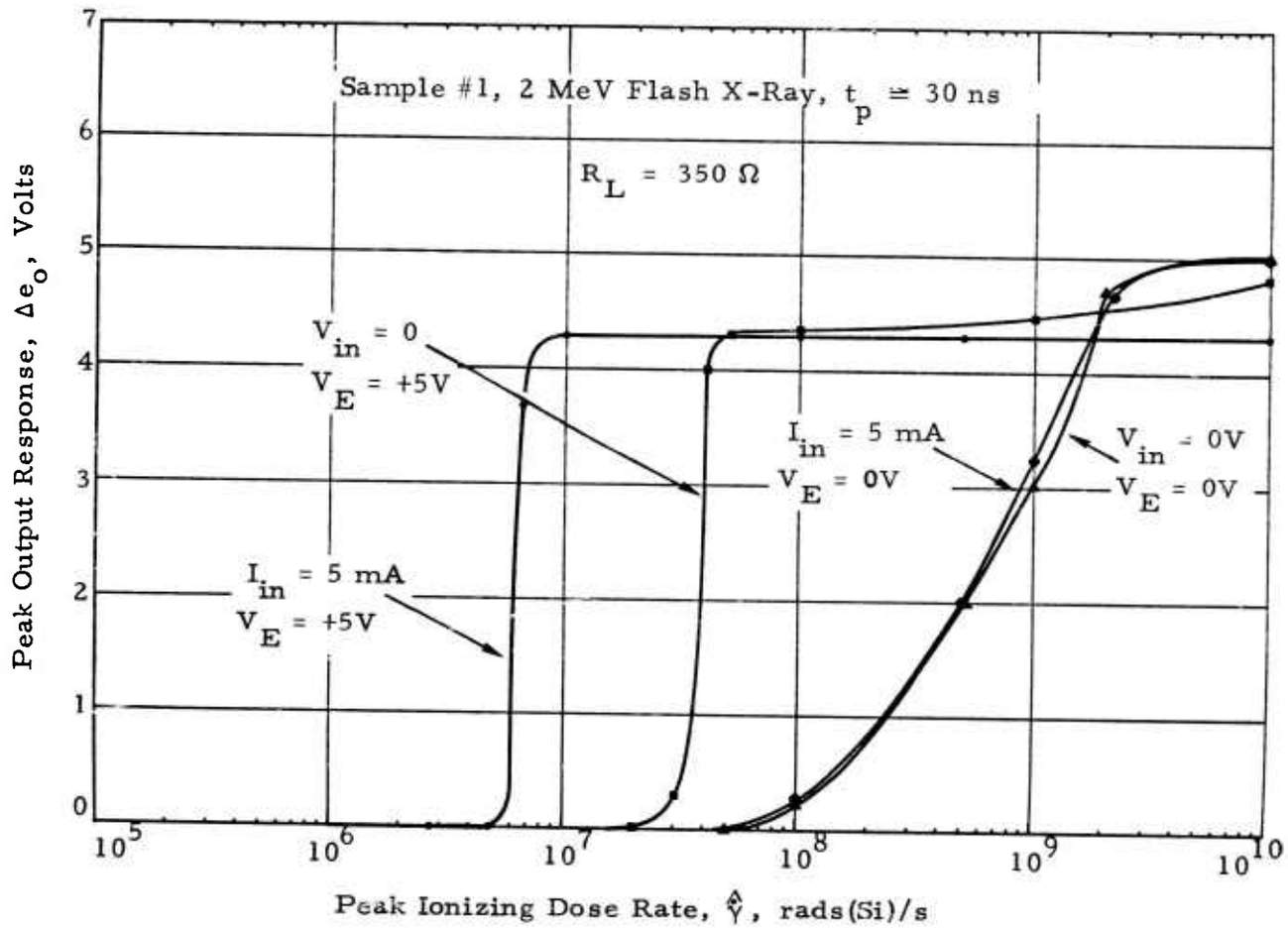


Figure 4-14. HP4360 Narrow-pulse transient photoresponse, Sample #1, $R_L = 350\ \Omega$.

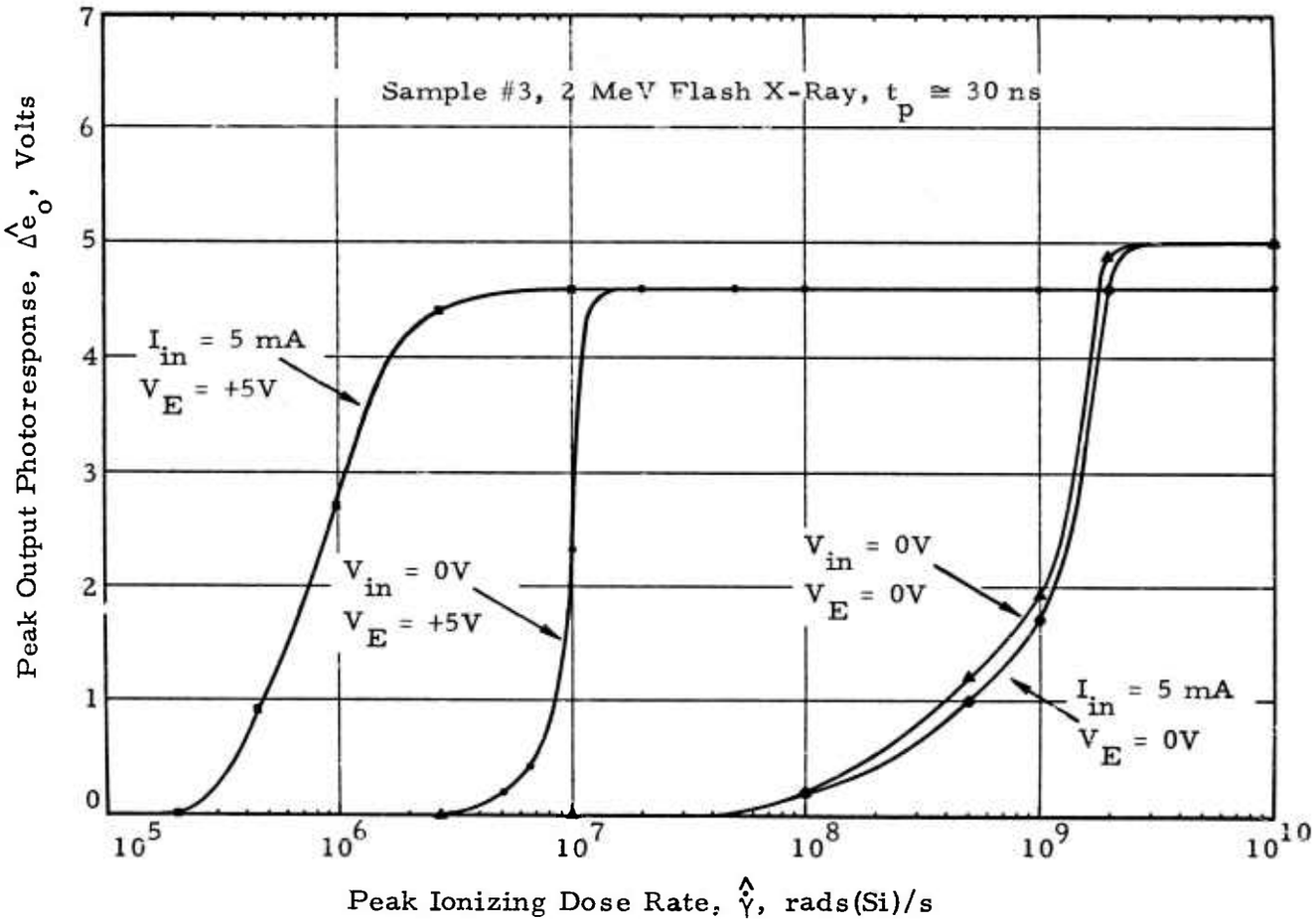


Figure 4-15. HP4360 narrow-pulse transient photoresponse, Sample #3, $R_L = 350\,\Omega$.

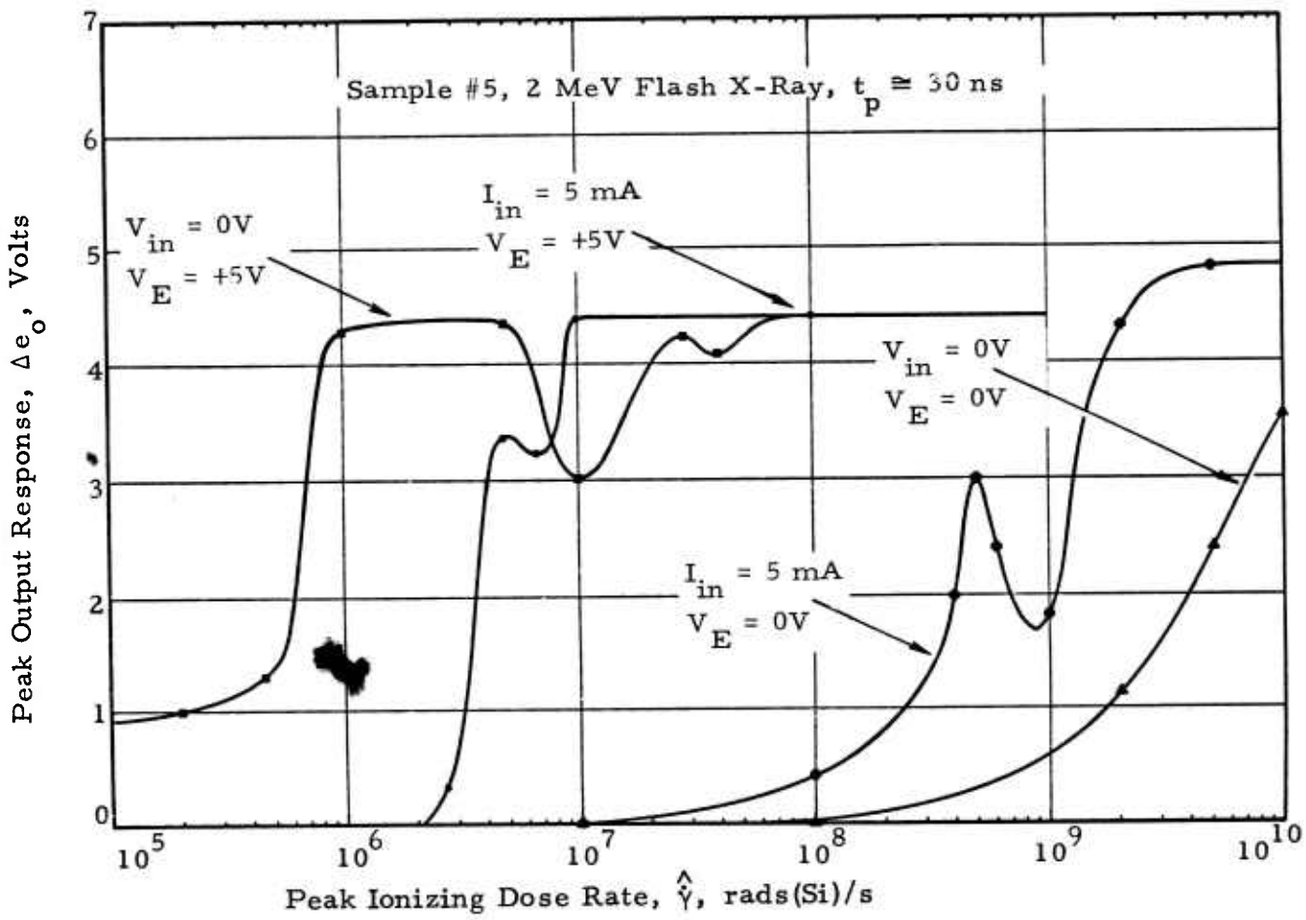


Figure 4-16. HP4360 narrow-pulse transient photoresponse, Sample #5, R_L = 350 Ω.

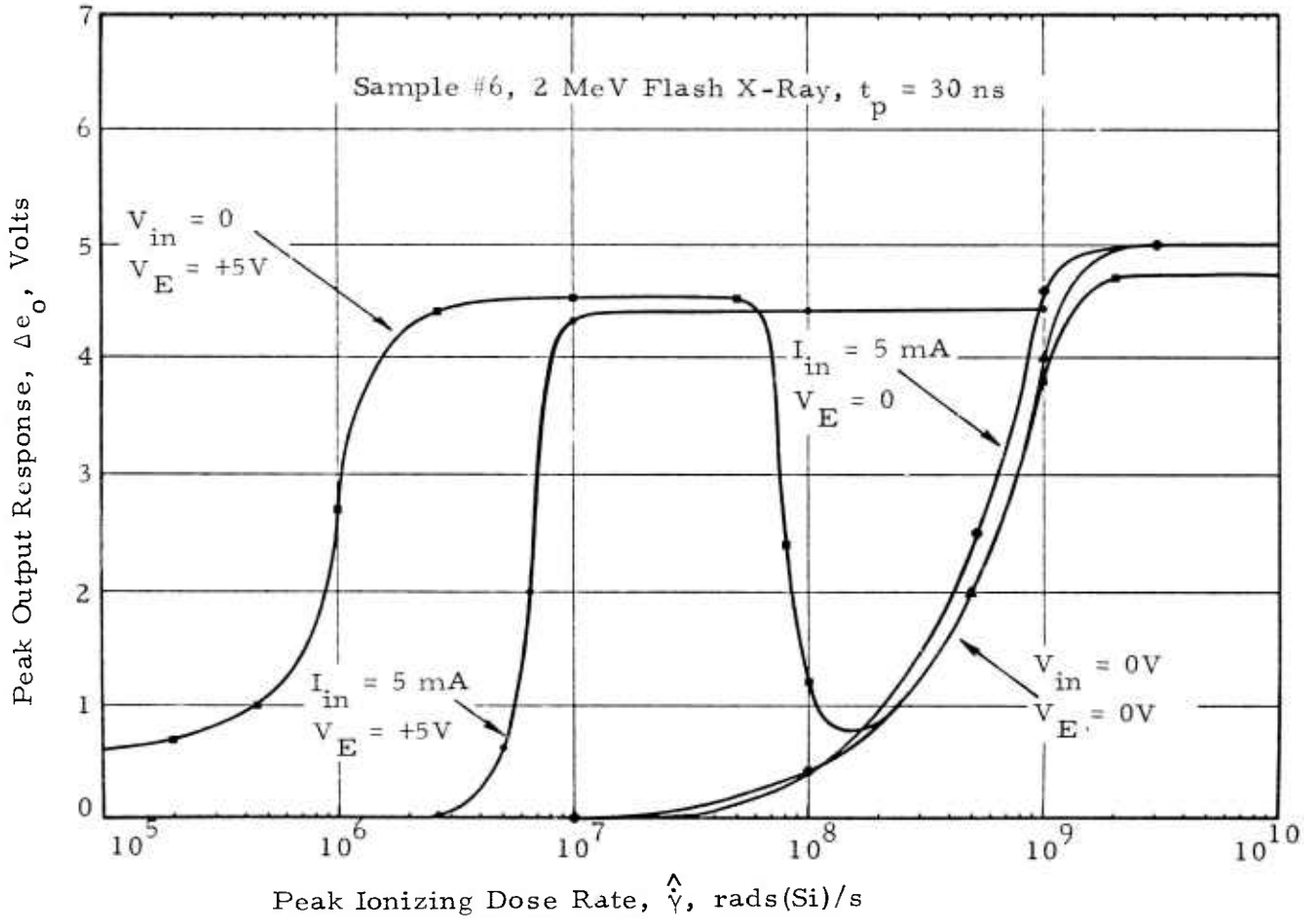


Figure 4-17. HP4360 narrow-pulse transient photoresponse, Sample #6, R_L = 350 Ω.

For each of these test conditions, the output voltage of the gate is in the "on" or logic "0" state which was determined, with additional measurements, as the worst-case. For three of the four samples the worst-case logic upset level was on the order of 6-8 x 10^5 rads(Si)/s for the test conditions of zero input current and +5V on the enable input. In one case, however, the logic upset level was substantially greater at 6 x 10^6 rads(Si)/s and the worst-case test condition was with both high input current and enable voltage.

Sample No.	Worst-case critical dose-rate	Test Condition
1	6 x 10^6 rads(Si)/s	I
3	6 x 10^5 rads(Si)/s	II
5	6 x 10^5 rads(Si)/s	II
6	8 x 10^5 rads(Si)/s	II

Typical waveforms observed in the narrow-pulse flash x-ray exposure are illustrated in Figure 4-18. The response at low radiation dose rates appears straightforward in a single output pulse that produces the radiation-induced logic upset. At high ionizing radiation dose rates, (i.e., above 10^9 rads(Si)/s), the output photoresponse becomes quite complex. The complexity of the output photoresponse suggests complex interactions in the recovery of the digital gate and high-gain linear amplifier sections of the output microcircuit. No sample showed an anomalous photoresponse that would suggest latch-up for exposures up to 5 x 10^{10} rads(Si)/s. Even those devices that exhibited damage, apparently as a result of the ionizing radiations exposure, the waveforms showed no anomalous response in the measurement of the transient photoresponse.

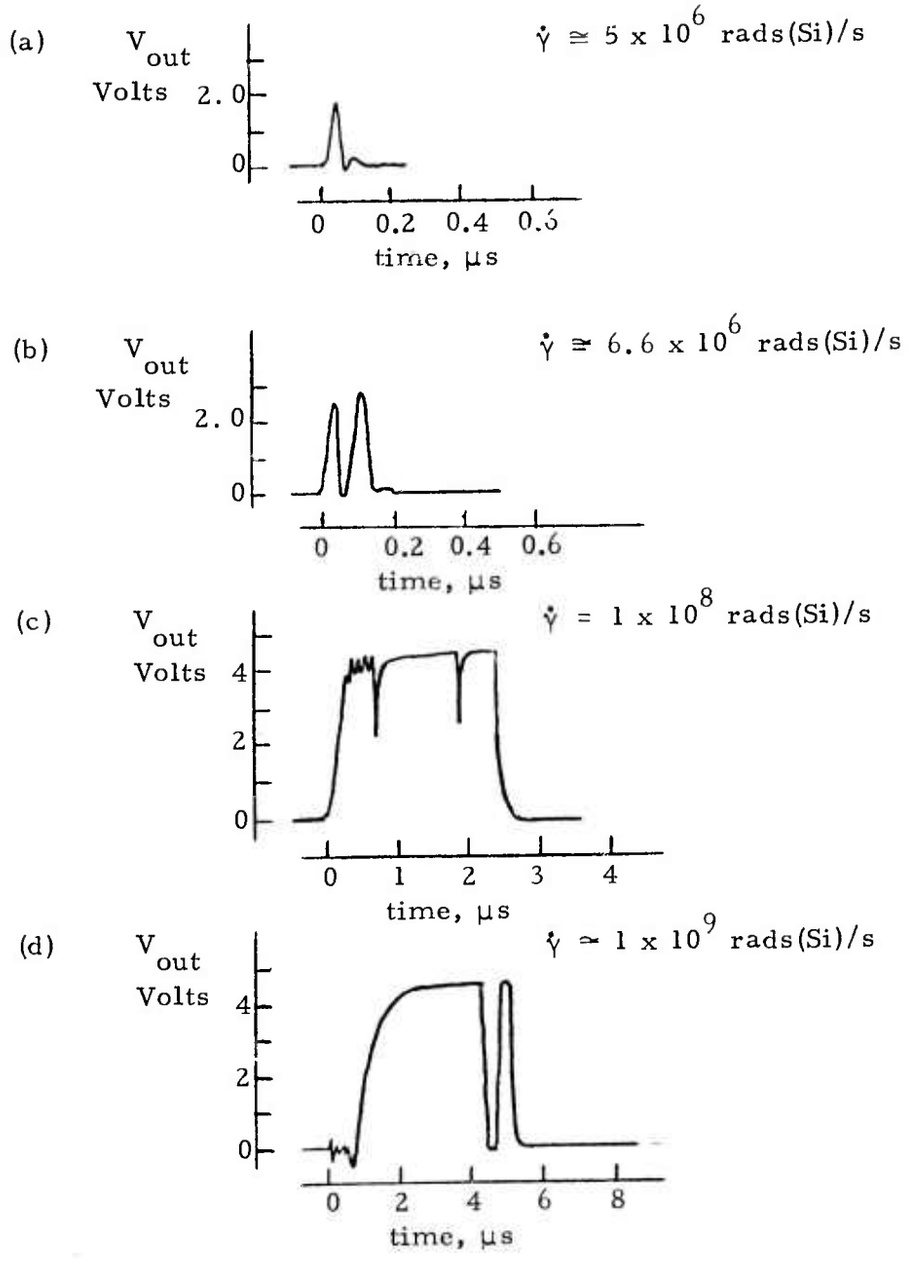


Figure 4-18. HP4360 narrow-pulse photoresponse waveforms, I_{in} = 5 mA, V_E = +5V, R_L = 1 kΩ

In order to further explore the transient photoresponse of the HP5082-4360, a limited effort was spent on the photoresponse measurement of a similar diode/gate coupler. The HP5082-4364 diode/gate coupler consists of a pair of inverting optically isolated gates each with a GaAsP light-emitting diode and a detector consisting of a detector diode, high-gain amplifier, and open-collector Schottky-clamped output transistor as shown schematically in Figure 4-19. The principal difference between the 4364 and the 4360 which was characterized extensively is the lack of the digital enable gate. The purpose of including the 4364 in the study was to verify that the complex photoresponse of the 4360 was due to the photoresponse of the digital gate. A single sample was exposed in the NRTC 2-MeV flash x-ray environment to radiation doses from 2.8×10^{6} to 1×10^{10} rads(Si)/s. The measured peak output response is shown in Figure 4-20 and the output waveforms, Figure 4-21, are in fact similar to those of the 4360 diode/gate coupler as shown in Figure 4-18, and strongly suggest that the photoresponse is due principally to that of the high gain amplifier.

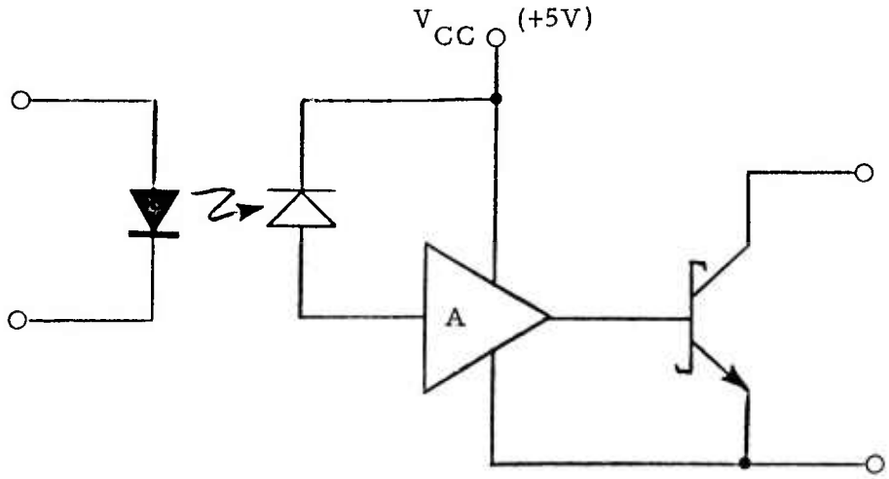


Figure 4-19. HP5082-4364 diode/gate coupler schematic.

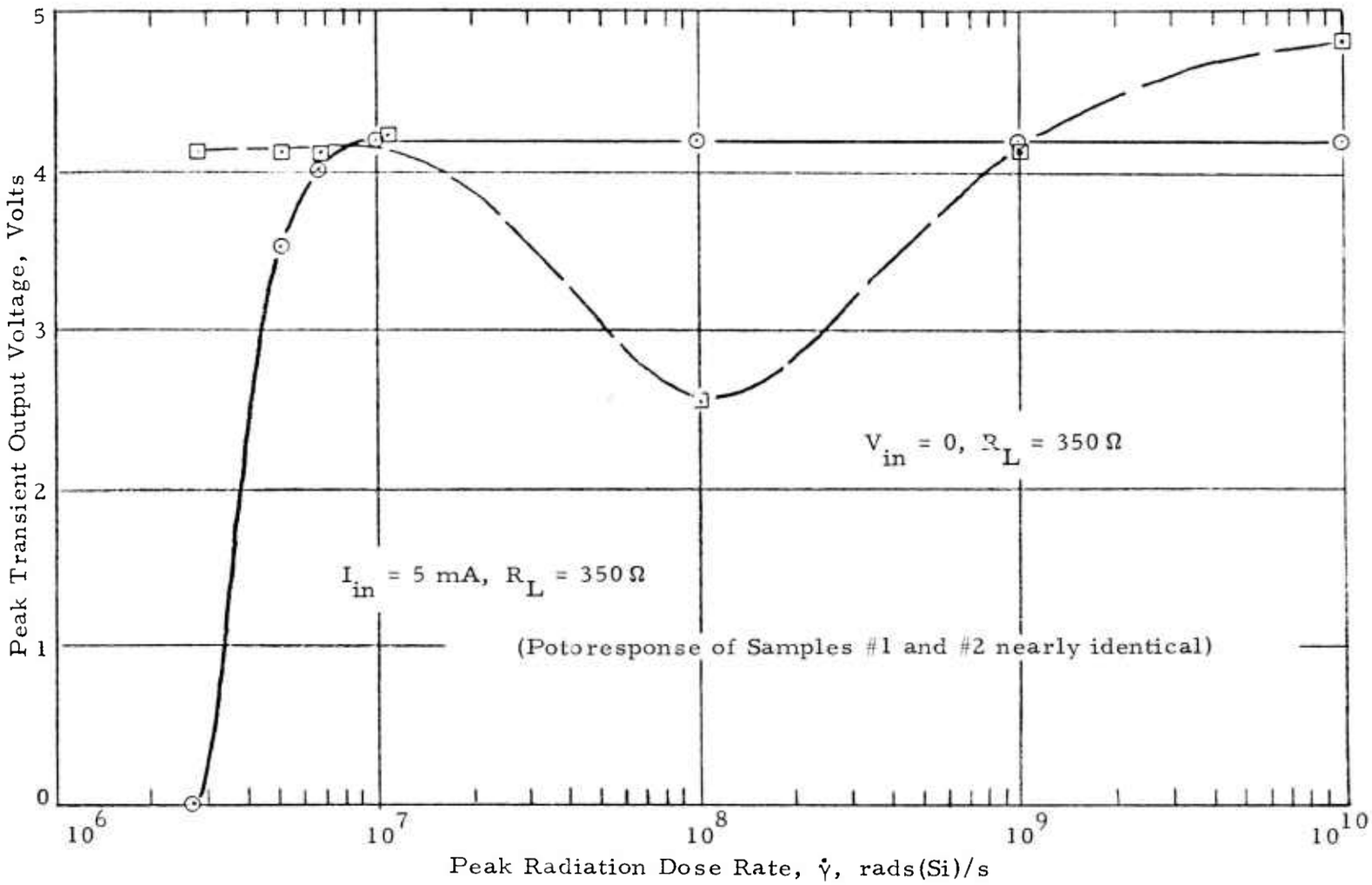


Figure 4-20. HP4364 narrow-pulse photoresponse.

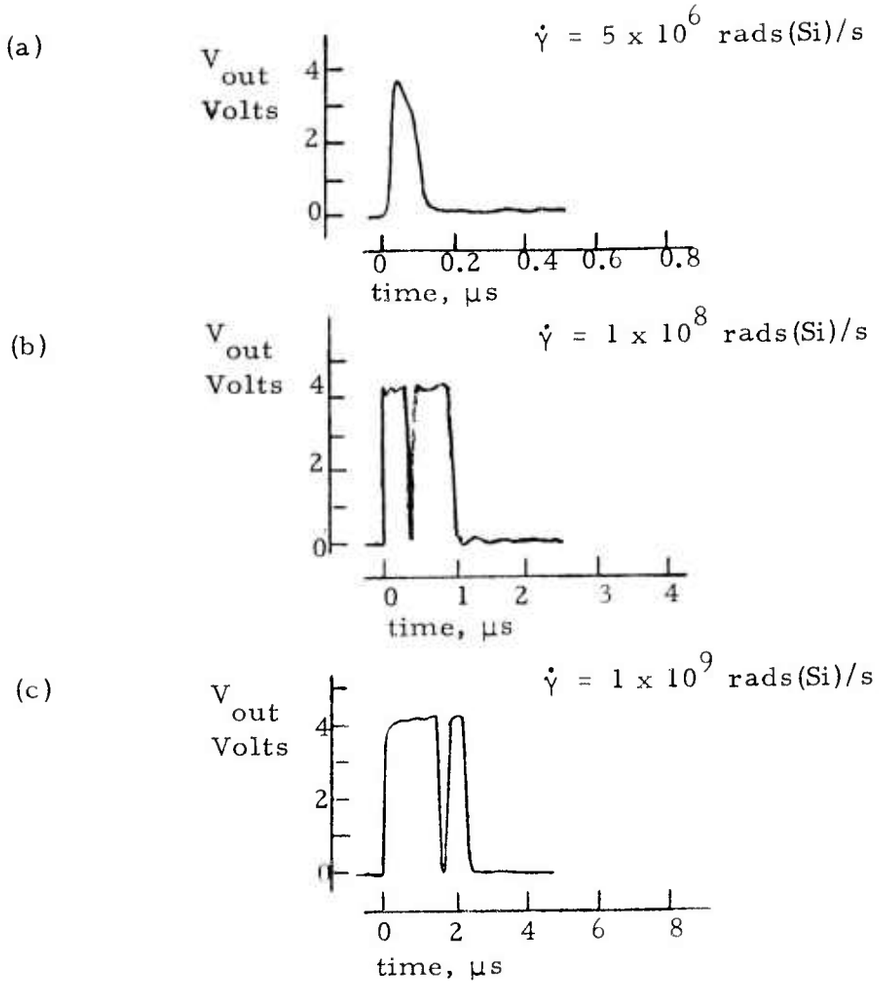
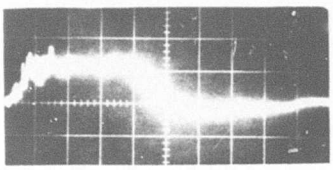


Figure 4-21. HP4364 narrow-pulse photoresponse waveforms, I_{in} = 5 mA, R_L = 350 Ω.

4.2.2 HP4360 Total-Ionizing-Radiation Dose Study. In order to investigate possible total-ionizing-dose permanent damage susceptibility of the diode/gate couplers, five unirradiated samples were exposed in the environment of the NRTC Co-60 source. All samples were under nominal supply voltage bias of +5V. Three of the five samples were operated dynamically during exposure with a sine wave input voltage of 50 Hz frequency applied at the input. The amplitude of the input signal was adjusted to a peak input current of 10 mA. The fourth sample was exposed with a static bias of 5 mA input current and +5V enable signal. The fifth sample was exposed with a static bias of 5 mA input current and with the enable input open-circuited. All samples were exposed to a total ionizing radiation dose of 1.9 Mrads(Si), with electrical performance checked at periodic intervals during the exposure through measurement of the input current/output voltage dc transfer characteristic. The result of the characterization was that there was very little radiation-induced permanent damage at exposures up to 1.9 Mrads(Si) and negligible effect at flash x-ray total dose levels of 20 krads.

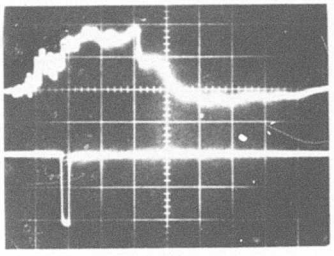
4.2.3 HP4360 Wide-Pulse Photoresponse. Two samples of the HP4360 optically coupled gate were tested in the 4.5 μs wide ionizing-radiation pulse of the IRT LINAC facility. As previously mentioned, the microcircuit contains an LED, a PIN diode detector, a linear amplifier, and a TTL-compatible output gate, all connected in series from input to output. Although the output photoresponse is obviously a net result of the photoresponses of the individual components, a plausible (by no means conclusive) separation of the susceptibilities of the individual components can be obtained from the composite output response to the wide-pulse LINAC enviroment shown in Figure 4-22. Part (a) of the

(a) RF noise on dosimetry channel
50 mV/div, 2 μs/div



(b) LINAC pulse (plus noise)
50 mV/div, 2 μs/div
(about 5×10^6 rads(Si)/sec per div.)

(c) Output photoresponse
2 V/div, 2 μs/div



(d) LINAC pulse
0.5 V/div, 2 μs/div
(about 5×10^7 rads(Si)/sec per div.)

(e) Output photoresponse
2 V/div, 2 μs/div

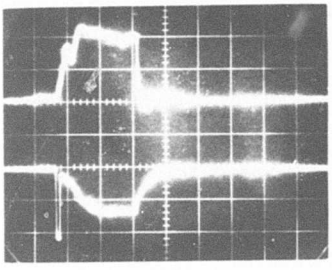


Figure 4-22. Wide-pulse LINAC photoresponse of HP4360 optically coupled gate.

figure shows the RF noise level on the active dosimetry channel that must be subtracted from the radiation pulse level shown in part (b) which was the lowest level tested to. The photoreponses shown in parts (c) and (e) of Figure 4-22 can be rationalized as follows. The experiment shown was performed with no bias current flowing through the LED, and therefore no light impinging on the PIN diode detector. It has been shown that the photoresponse of the LED is negligible, and if, for the moment, we assume that the amplifier and output gate are "hard" to ionizing radiation, we would expect the radiation to be "detected" by the PIN diode, thereby driving the output to the "low" state as it would if it (the PIN) were irradiated with light from the LED. It is believed that this response determines the leading edges of the photoresponse shown in parts (c) and (e), and it is estimated that this transient failure occurs at radiation intensities on the order of 10^5 rads(Si)/s.

However, as can be seen from the photoresponse shown in part (c), the output returns to the "high" state when the radiation intensity increases to levels above about 1.5×10^6 rads(Si)/s. It is suggested that this behavior is caused by the linear amplifier being driven into saturation by the "higher" radiation intensities, the photoresponse of the amplifier masking-out the PIN response at the input of the amplifier. From the photoresponse shown in part (e) of the figure, it can be seen that at radiation intensities on the order of 10^8 rads(Si)/s that the output again tends toward the "low" state. This behavior is probably caused by the inherent photoresponse of the output gate, which in turn masks the photoresponse of the amplifier.

In conclusion, we find that the vulnerability of the HP4360 optically-coupled gate is extremely low, about 10^5 rads(Si)/s, with the "weakest-link" component being the PIN diode detector. The worst-case shift in the transfer characteristic is illustrated in Figure 4-23. The test sample in this case was operated statically with 5 mA input current and +5V on the enable input.

4.2.4 HP4360 Neutron Displacement Damage Study. In order to determine the neutron-damage susceptibility of the diode/gate couplers, six samples were exposed to the neutron/gamma environment of the NRTC TRIGA. Since the total dose exposure to 1.9 Mrads had produced negligible effects, the same five samples and bias conditions were used for the TRIGA exposures. An additional sample was added and exposed under the bias conditions determined to be worst-case from the total dose exposure (i.e., static bias, I_{in} = 5 mA, V_E = 5V). Electrical performance characteristics were measured on five of the six samples at seven intervals through exposure to a maximum fluence of 1.3×10^{14} n/cm^2 (1 MeV equivalent). The first-order effect observed in the performance degradation was the degradation of the input-current/output-voltage transfer characteristic. While there was significant variation between samples in performance degradation, there was no apparent correlation to the bias conditions under exposure. Degradation of the transfer characteristics is illustrated for two samples in Figure 4-24. Assuming the electrical specification of minimum input current of 5 mA required to ensure a logic "0" output as recommended by the manufacturer, the critical neutron fluence for five samples was determined as,

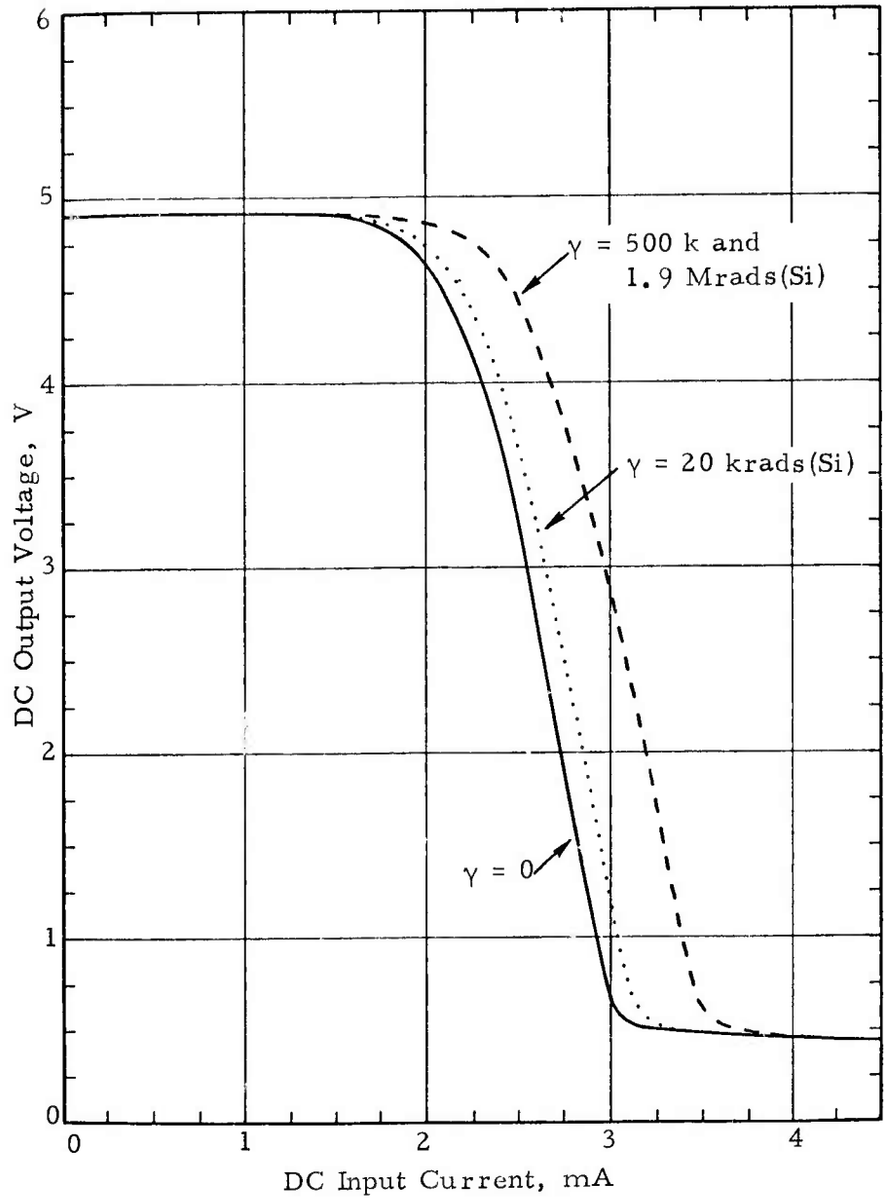
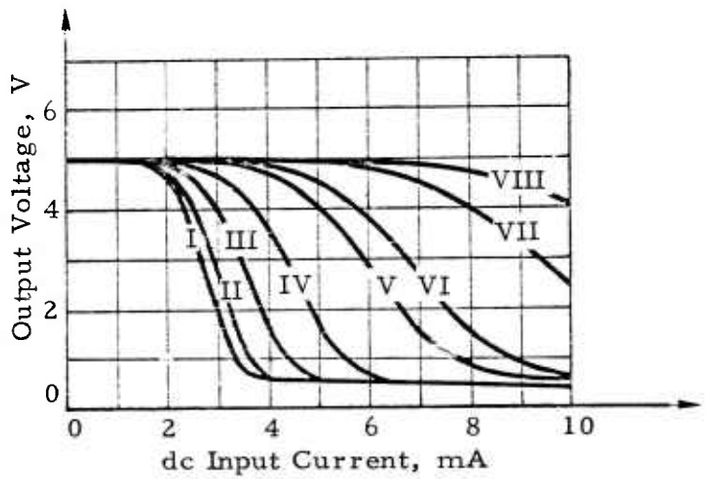
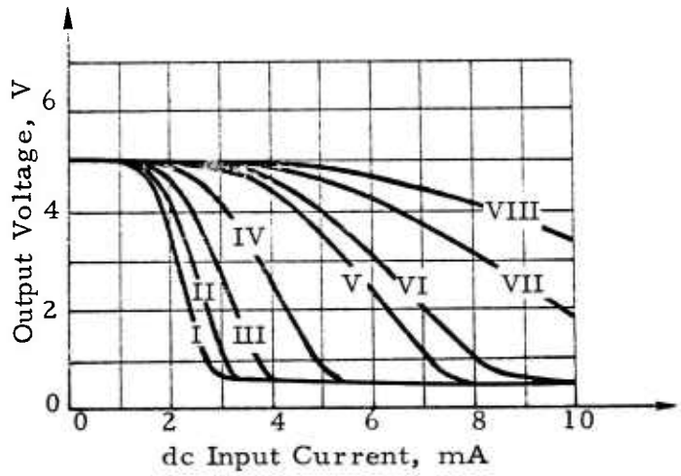


Figure 4-23. Worst-case total dose permanent damage effects in HP4360 diode/gate coupler.

Sample #7



Sample #8



I: $\Phi = 0$

II: $\Phi = 1.5 \times 10^{12}$ n/cm^2

III: $\Phi = 4.8 \times 10^{12}$ n/cm^2

IV: $\Phi = 1.1 \times 10^{13}$ n/cm^2

V: $\Phi = 1.8 \times 10^{13}$ n/cm^2

VI: $\Phi = 2.3 \times 10^{13}$ n/cm^2

VII: $\Phi = 3.8 \times 10^{13}$ n/cm^2

VIII: $\Phi = 5.4 \times 10^{13}$ n/cm^2

(1 MeV equiv.)

Figure 4-24. Neutron-induced degradation of the HP4360 dc transfer characteristics.

Sample No.	Critical Neutron Fluence (n/cm^2)
7	$1.1 - 1.8 \times 10^{13}$
8	1.1×10^{13}
10	$1.8 - 3.8 \times 10^{13}$
9	7.3×10^{12}
18	$3.4 - 4.9 \times 10^{13}$

Characterization of the sixth sample at the end of the total exposure indicated failure with the output voltage only down to 4 volts with an input current of 10 mA, with exposure to 1.3×10^{14}.

Results of the neutron damage characterization can be presented more quantitavely by defining the degradation in the threshold current required to produce an output voltage of 0.8V with the power supply voltage, V_{CC}, and enable voltage, V_E, at +5V. The threshold current is plotted against neutron fluence in Figure 4-25. Interestingly, the observed results are very close to a linear dependence of threshold current on neutron fluence, where the constant of proportionality is also proportional to the initial threshold current. That is,

$$\frac{I_T(\Phi)}{I_T(0)} = 1 + K_c \cdot \Phi$$

where, based on the observed results, the value of K_c is 6.9×10^{-14} $(n/cm^2)^{-1}$. This linear expression is plotted with the experimental data in Figure 4-25 and seems to be an accurate approximation over the range of exposures and bias conditions encountered. No

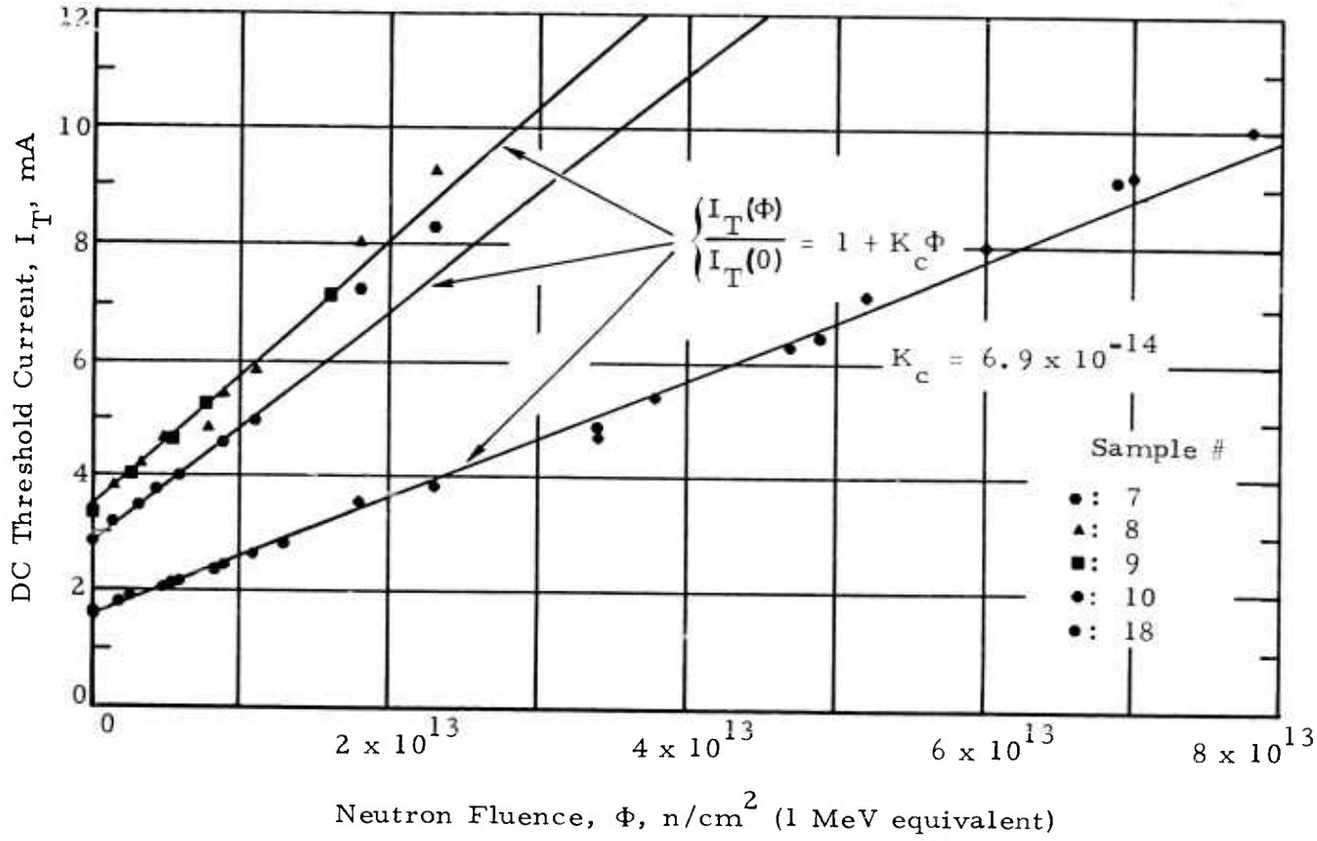


Figure 4-25. Neutron-induced degradation of HP4360 input threshold current.

detailed analysis has been attempted to justify the mathematical form of the results, but it is likely that the degradation is principally due to the gain degradation of the linear amplifier driving the digital gate output.

5.0 COMBINED EFFECTS STUDY

Effects of combining electrical pulse overstress and pulsed ionizing exposure have been investigated on discrete semiconductor devices (i.e., diodes and transistors). Synergistic effects have been observed but not to the degree that clearly defines the effect compared to the uncertainty in either the pulsed overstress or photoresponse characterization. In this study, combined effects have been considered for CMOS circuits that have demonstrated latch-up from either electrical overstress or ionizing radiation exposure. In this case, permanent damage is the result of excess current flowing from the power supply after the array has latched into a low-voltage, high-current mode. The critical energy is not that required for burn-out, since burn-out results from the infinite-power voltage supply with whatever time interval required, but rather that required to induce latch-up. This study, then considered possible synergistic effects in CMOS latch-up under simultaneous electrical overstress and pulsed ionizing radiation exposure. The observed results suggest that a synergistic effects exist, but are not a first-order effect.

Latch-up in CMOS integrated circuits have been reported by B. L. Gregory and B. D. Shafer.[12] They observed latch-up in bulk CMOS types CK4007A, CD4009A, CD4010A, CD4011A, and CD4041A, but none in CD4020A. It was triggerable either electrically or by flash x-ray pulsed radiation. A detailed study of the phenomenon in types CD4007A and CD4041A was made.

In the work reported here, the results of Gregory and Shafer on the type CD4007A were duplicated, and then the effects of a combined electrical

pulse overstress and pulsed x-radiation were examined. Electrical latch-up was easily demonstrated on a Tektronix 575 Curve Tracer. In the normal inverter configuration a holding current of approximately 45 mA is observed with input high and 65 mA with input low. For the combined electrical pulse overstress and radiation effects, an 0.8 μsec pulse was applied to the V_{DD} terminal as shown in Figure 5-1. The supply voltage was applied to V_{SS} rather than to V_{DD}, in order to separate it from the overstress voltage so as to avoid loss of some of the overstress energy in the power supply. These latch-up tests did not include stressing the input or output terminals, because latch-up occurred only when the V_{DD} terminal was stressed. Application of the pulse to the input terminal was found only to produce damage at levels of overstress comparable to those observed in previous bulk CMOS studies. The electrical pulse overstress generator was triggered by the flash x-ray trigger, and the delay adjusted so that the radiation pulse occurred near the middle of the 0.8 μsec overstress pulse. Both the amplitude of the overstress pulse and the intensity of the x-radiation were variable during these tests. Latch-up was indicated by a current-reading meter in the power supply.

The results of these tests are plotted in Figure 5-2 for two CD4007AD CMOS inverters with inputs high. The points plotted are the critical electrical pulse overstress voltage versus x-radiation dose-rate for latch-up. The curves show some interaction between the two environmental factors, especially in Device #1. Latch-up is triggered by radiation alone at a dose-rate of 6×10^8 rads(Si)/s and above.

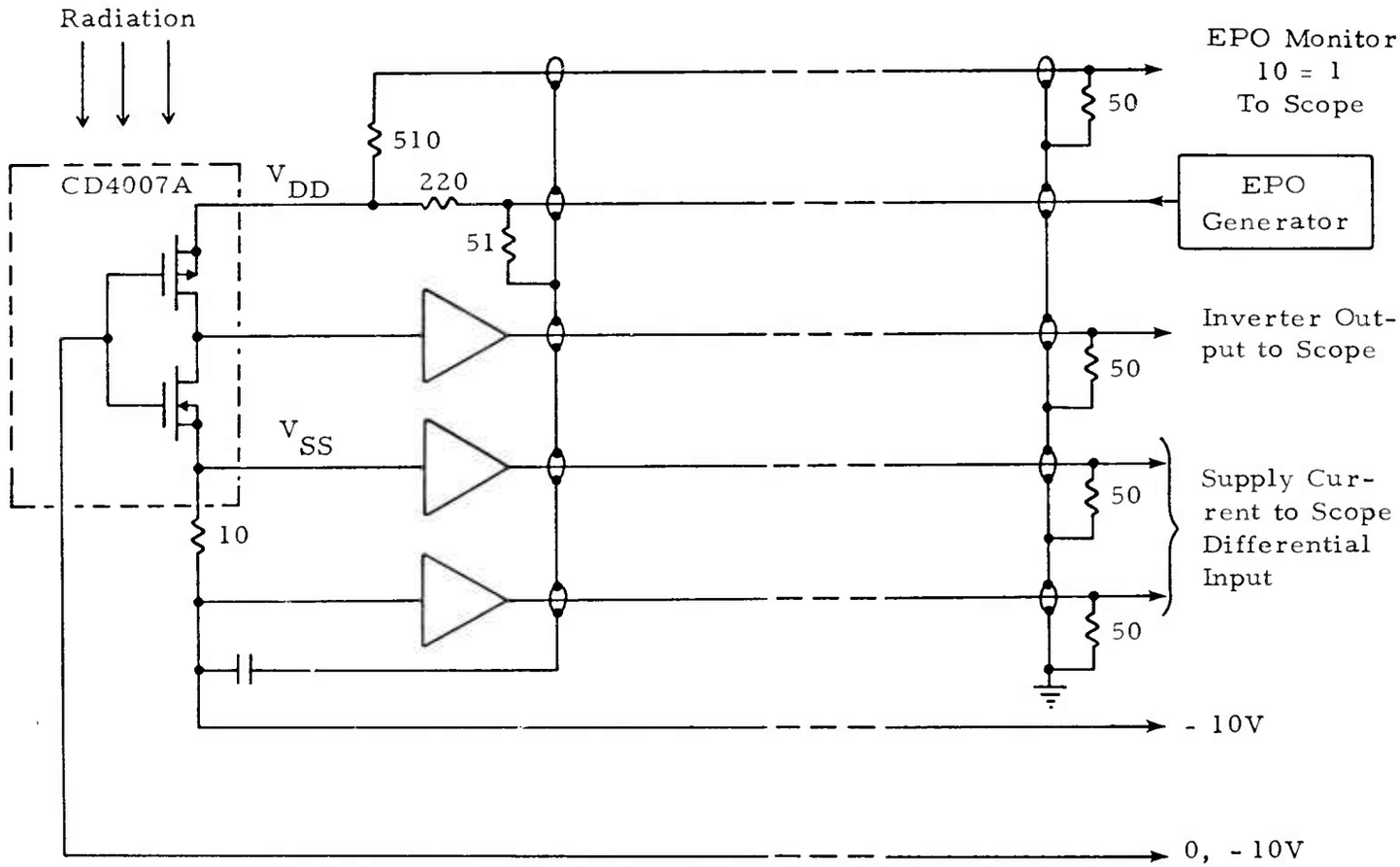


Figure 5-1. Electrical setup for combined EPO - flash x-ray tests.

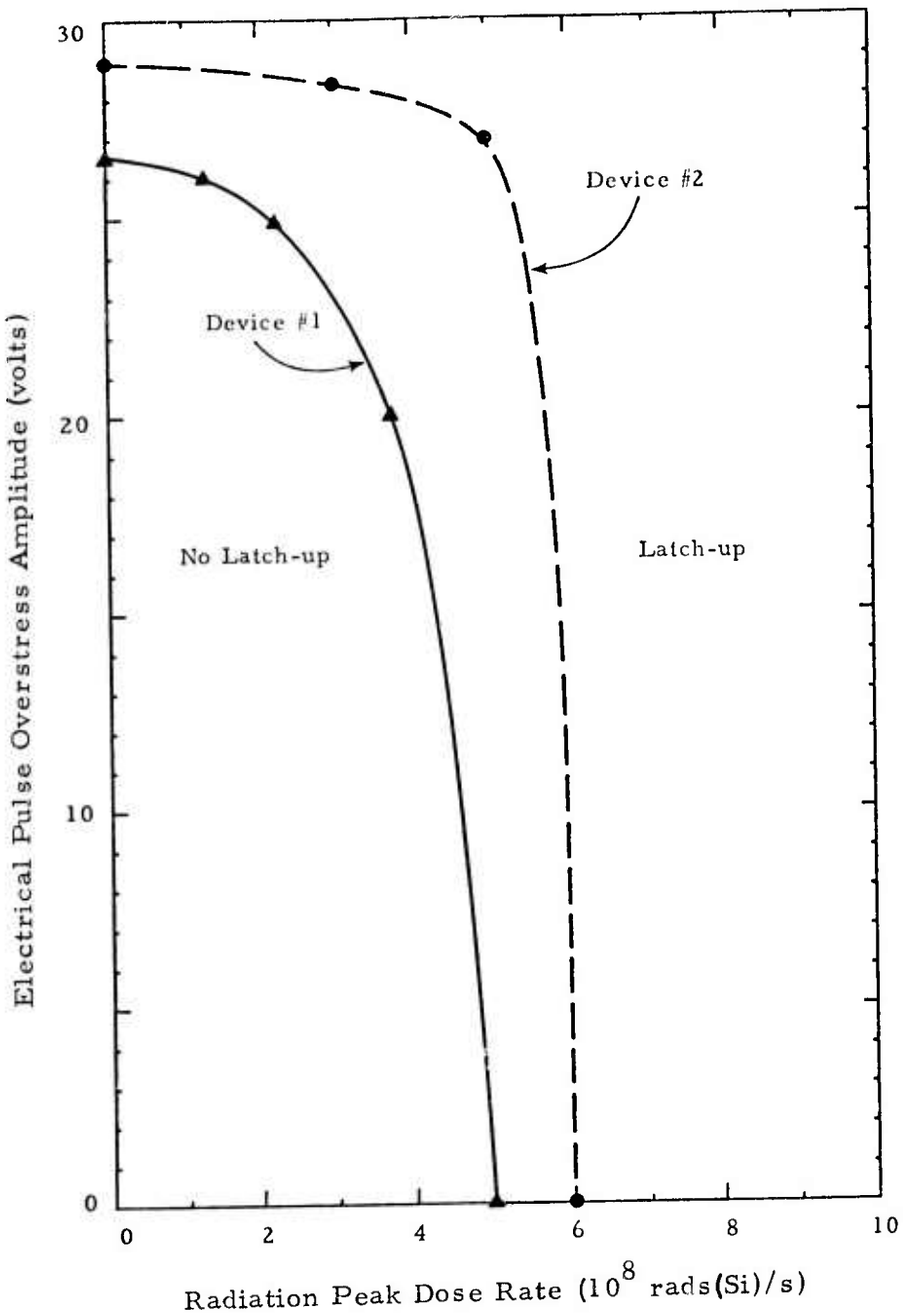


Figure 5-2. Threshold for latch-up in combined EPO-radiation environment.

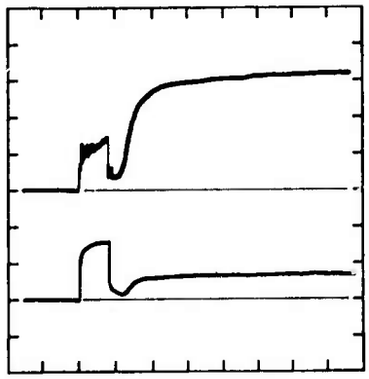
Figures 5-3, -4, and -5 show the time-dependent waveforms of latch-up when triggered by EPO alone, EPO plus radiation, and by radiation alone. When EPO is present, the supply current pulse shows an initial direct response to the overstress pulse, followed by a delayed response of higher amplitude. The direct response varies in amplitude with the EPO amplitude and may be a charging current through the substrate for the p-well to substrate junction capacitance. The delayed response is about 600 mA at peak independent of the EPO amplitude or radiation dose-rate. This is latch-up, and the delay is probably due to the motion of minority carriers released by the pulse stress. The large amplitude is not understood at this point. The power supply was set to limit at 100 mA, but this limit takes about a millisecond to take effect as was observed on slow-sweep.

It is of interest to determine if latch-up is a problem in other CMOS microcircuits. In particular, some of the other CMOS devices studied in this LSI Vulnerability Study were examined. The CD4024 7-stage binary counter and the Motorola MC14021 8-bit shift register were examined for electrically induced latch-up. All terminals were examined on a curve-tracer, but no evidence of latch-up was observed. Electrical pulse overstress also failed to produce any latch-up. The absence of latch-up in any circuit can be attributed to geometrical factors which prevent the formation of high gain npn structures in the substrate, and in these more complex microcircuits the small geometries and the closeness of the individual inverters is apparently offset by careful overall layout of the microcircuit.

Latch-up tests were performed on two microcircuits of medium complexity - a type CD4023A (triple 3-input NAND gates) and a type CD4024A

Supply Current
200 mA/div.

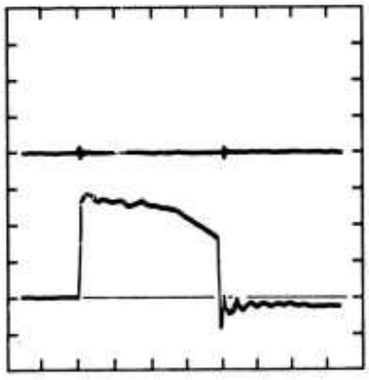
Inverter Output
10V/div.



1 μsec/div.

PIN Diode
No Radiation

EPO Monitor
10V/div.



0.2 μsec/div.

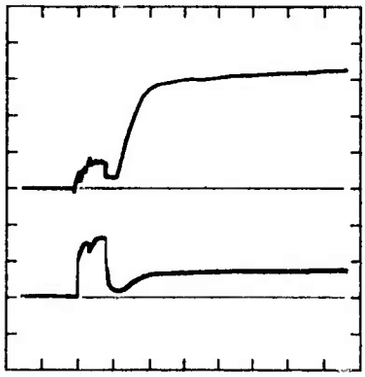
Figure 5-3. Latch-up in CD4007AD due to EPO alone.

Supply Current

200 mA/div.

Inverter Output

10V/div.



1 μsec/div.

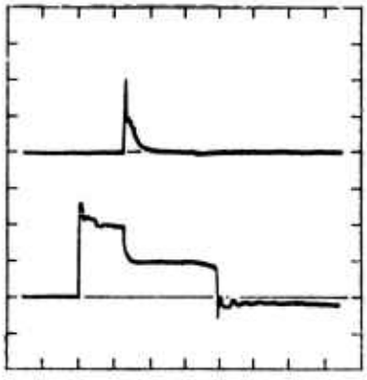
PIN Diode

1V/div.

4×10^{8} rads(Si)/s (peak)

EPO Monitor

10V/div.



0.2 μsec/div.

Figure 5-4. Latch-up in CD4007AD in combined EPO and radiation.

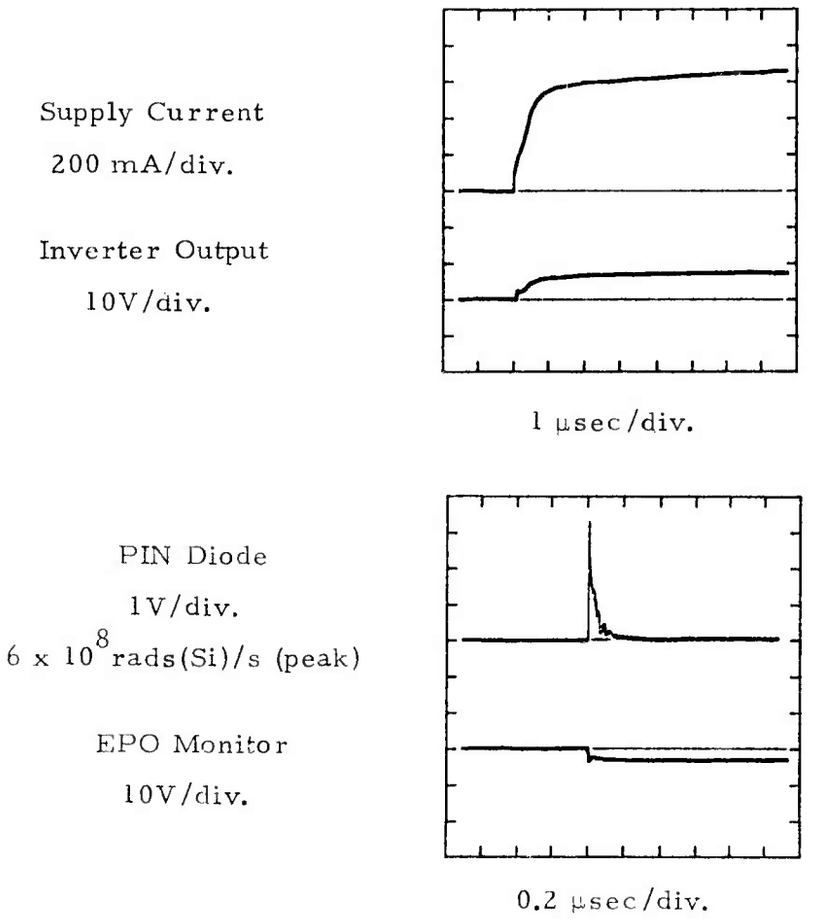


Figure 5-5. Latch-up in CD4007AD due to radiation alone.

(triple 3-input NOR gates). Examination of the bias terminal, V_{DD}, on a curve-tracer showed no evidence of latch-up. Combined EPO and flash x-ray tests were also performed on these devices with no evidence of latch-up.

6.0 CONCLUSIONS AND RECOMMENDATIONS

Electrical performance potential of bulk CMOS is of substantial advantage in many system applications, particularly those with severe power limitations. In many of these system applications, the total-dose susceptibility, transient photoresponse, and potential latch-up of the bulk CMOS arrays are of significant concern. Results of this study present effects on a small sample of microcircuits and point out critical total-dose, photoresponse, and latch-up effects. Additional study is required, however, in hardness assurance of CMOS microcircuits of SSI-MSI levels of complexity.

In contrast to the mature CMOS technology, I^2L is in the earliest stage of LSI development. Results presented on radiation susceptibility of the basic I^2L logic cells represent a very preliminary evaluation. Results on neutron-damage, total-dose, and transient photoresponse effects seem to be consistent with the well-known basic semiconductor radiation effects. Further effort is required to evaluate permanent damage and transient photoresponse effects with support of radiation-inclusive mathematical models. As I^2L technology matures, spurred primarily by extensive international development for commercial applications, more complex arrays will become available. Evaluation of the complex arrays is a key step in evaluation of I^2L susceptibility since the design of both the internal cells and interface circuits may vary significantly from the basic cells considered in this study.

Radiation susceptibility of the detectors of the optical communication system may be an important consideration in overall system hardening. As shown in the results of this study, those techniques necessary to transform the optical signal to an output logic level, even without the

losses of effects of the fiber optics, are intrinsically sensitive to pulsed ionizing radiation. On the other hand, the recovery times of the electronics are not extraordinarily long and could be accommodated in the system design. Permanent damage levels resulting from neutron displacement damage are not inconsistent with those of high-gain operational amplifiers. It is hoped that results of this study will be useful in performance evaluation of overall optical communication systems. In terms of future development, the technology of LSI will impact optical system with the development of integrated optics. At the moment, however, complex integrated-optics arrays are still in early research development and no continuing effort is suggested at this time.

In terms of the overall program, it is suggested that that the emphasis be placed on the radiation susceptibility of basic LSI technologies and complex LSI arrays. As pointed out in earlier studies, the most unique problem associated with MSI/LSI radiation effects is that of accurately determining the worst-case susceptibility in light of the array complexity. In terms of newly developing LSI technologies, I^2L and CCD arrays offer substantial promise and are receiving extensive development. In terms of microcircuit complexity, developments in MSI/LSI technology seem to be concentrating on the microprocessor as a very complex LSI array with widespread application in modern systems.

7.0 REFERENCES

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APPENDIX A

MSI/LSI RADIATION EFFECTS, CHARACTERIZATION AND TESTING*†

James P. Raymond

Northrop Research and Technology Center
Hawthorne, California 90250

ABSTRACT

Results are presented on the permanent damage and transient photoresponse of complex monolithic MSI/LSI arrays representing a variety of both bipolar and MOS technologies. Unique aspects of MSI/LSI vulnerability are principally in the nature of the basic logic cells and the complexities of overall array performance evaluation. Considerations illustrated in permanent damage evaluation are complete performance evaluation, electrical bias conditions during radiation exposure, selection of sample sizes, and electrical pulse overstress effects. Considerations illustrated in the transient photoresponse are the dependence on ionizing radiation pulse-width, determination of worst-case logic operating conditions, and power-supply photocurrent. Analytical techniques are suggested as an essential aid in MSI/LSI characterization and testing.

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INTRODUCTION

Characterization of radiation effects on microcircuits has become a routine aspect of component qualification for hardened systems. As microcircuit technology has evolved, complex MSI/LSI digital arrays have been developed to supplement the single-function microcircuits as system components. These complex arrays are the blend of semiconductor device technology with the performance capability of digital subsystems. As a direct evolution of microcircuit technology there are many similarities in radiation vulnerability between the simpler SSI (Small-Scale-Integration) and MSI/LSI (Medium-Large-Scale-Integration) devices. There are, however, unique aspects that critically distinguish MSI/LSI. These are principally the technology, circuit performance, and radiation response of the basic logic cells, and the requirement for evaluation of overall array performance and radiation vulnerability assessment without access to direct measurements on the internal logic cells.

The basic MSI/LSI logic cell, free from the constraints of external loading and noise margin, has evolved into circuit realizations that have little or no correspondence to a single-function microcircuit. This is illustrated most strongly by the development of memory cells of both bipolar and MOS memories, and in the logic cells of dynamic-logic MOS arrays. With the evolution in the circuit realization of the basic logic cell the nature and critical failure levels must also change. Results are presented on radiation effects of DTL, TTL, ECL and Schottky-clamped TTL arrays of bipolar technology as well as the static p-MOS, dynamic p-MOS, C/MOS and C/MOS/SOS arrays of MOS technology. These represent the major technologies of MSI/LSI up to the development of high-speed n-MOS, charge-coupled-devices, and bipolar integrated injection logic. The results are presented for unhardened arrays, focusing more on the nature of radiation effects rather than on the levels of radiation hardness attainable.

Given the measured radiation vulnerability of the logic cells of a digital subsystem, the subsystem vulnerability can be determined with little difficulty, subject to a few confirming experiments at the overall subsystem level. Application of MSI/LSI arrays as system components, however, makes a vital difference in the component characterization due to the lack of access to the performance characteristics and radiation vulnerability of the basic logic circuits (cells). This distinction might seem fairly subtle, but it has a first-order impact on the experimental characterization; particularly in the required analytical techniques and mathematical models necessary to support the experimental study. Techniques of simplified modeling and logic simulation, which are useful but not necessary for microcircuit study become critical in support of MSI/LSI experimental characterization.

Study of radiation effects on MSI/LSI arrays has included the measurement of transient photoresponse as a function of ionizing radiation pulse width, as well as the permanent damage effects resulting from neutron/gamma exposure and externally applied electrical pulsed overstress. Results indicate that the basic radiation-induced failure mechanisms in complex devices are essentially the same as those well known for single-function digital microcircuits[1,2], that is, 1) p-n junction photocurrents in the transient photoresponse, 2) neutron-induced gain degradation in bipolar transistor elements, 3) total-ionizing-dose-induced threshold voltage shift in MOS transistor elements, and 4) increase in the p-n junction thermal leakage currents. Critical failure levels observed are consistent with those expected from studies on basic semiconductor elements and microcircuits, but as reflected through the specific logic cell technology and overall array performance characteristics. Pulsed ionizing radiation-induced latch-up has not been observed in any of the MSI/LSI arrays tested for exposures up to 5×10^{10} rads(Si)/s, and despite the increase in element density, multi-layer metallization and functional complexity, latch-up does not seem to be any more (but not necessarily any less) likely than latch-up in a single-function microcircuit.

Radiation-Induced Permanent Damage

The principal considerations in evaluating radiation-induced permanent damage effects on MSI/LSI arrays are: 1) comprehensive evaluation of pre-/post-electrical performance characterization, 2) selection of electrical bias conditions during neutron/gamma irradiation, and 3) determination of the number of samples that must be characterized to insure adequate statistical representation for component system qualification. In addition to the characterization of radiation-induced permanent damage it also may be necessary to characterize the component electrical pulsed overstress susceptibility. In this case, the problem is to determine a test sequence that defines the worst-case vulnerability with a minimum number of samples.

Electrical performance characterization of MSI/LSI arrays is a well documented problem even without considering radiation-induced damage effects. The most straightforward method of verifying the overall logic function of the array is simply to compare the outputs of a damaged device to those of a good reference device under the same input signal sequence for all possible input conditions. The array interface, typically outputs, must also be characterized in terms of the terminal current-voltage characteristic to assure performance for specified external loads. In some cases it is more convenient to simulate the reference "good" device logically with a minicomputer programmed to direct the input sequence and compare the output results. If the array is very complex and a large number of samples must be tested the total number of input combinations can be reduced to the set just sufficient to detect the failure of any logic cells. Generation of test sequences

can also be used to isolate the radiation-induced failure to a single cell for subsequent detailed failure analysis and possible hardening. Application of the test sequences to a given array can be implemented analytically with logic simulation computer programs that consider the array as a network of idealized logic functions.[3]

Pre-/post-evaluation of array performance must also include the system-defined temperature range. Bipolar transistor gain degradation becomes most critical when the gain is low at low temperatures. Junction leakage currents, increased by displacement damage or surface effects, on the other hand, become most critical at high temperatures. Variation in the damage failure level due to both transistor gain degradation and junction leakage currents over a wide range of case temperature was observed in the neutron/gamma-induced degradation of the SMS 8228 4,096-bit Schottky-clamped TTL Read-Only-Memory. In this case, the room temperature evaluation was the best-case compared to either low- or high-temperature operation.

Damage assessment of MSI/LSI arrays is sufficient to assure adequate performance of internal logic cells, but not the safety margin to the threshold of failure. The safety margin of the internal cells must be determined experimentally. Damage effects at the interface cells, however, can be measured quantitatively and a safety margin estimated for given load requirements by extrapolating slightly to higher exposure levels. Observed neutron / gamma failure levels for a variety of MSI/LSI arrays are summarized in Table I. Neutron fluence is considered as critical for the bipolar arrays and total ionizing dose is considered as critical for the MOS arrays. Total dose exposure of the hardened TTL 6-bit adder, indicating negligible degradation to greater than 10 Mrads(Si) is a supporting verification of this assumption.

The failure levels as shown in Table I represent the results of a system-independent laboratory characterization and do not include any worst-case system requirements (e.g., power supply tolerance, termperature range, switching speed, and noise margin). Relative failure levels in the bipolar arrays of the internal logic function or the external drive capability is a function of the relative design margin and, as shown in Table I, either might be the critical failure mode for a given array type.

Total ionizing dose failure levels for a few MOS arrays have also been included in Table I. In this case, because of the variations in basic transistor effects with variations in processing technology and electrical bias curing exposure, the minimum critical total dose is probably more significant than the apparent spread in failure levels between samples. The test conditions in the MOS arrays are also critical in defining a failure level since the arrays can be operated over a wide range of power supply voltages with a substantial variation in electrical performance parameters.

TABLE I

SUMMARY OF MSI/LSI PERMANENT DAMAGE LEVELS
Critical Neutron Fluence, Φ_f, n/cm^2 (1 MeV equivalent),
TRIGA $\sim n/\gamma = 3 \times 10^8\ n/cm^2/rad(Si)$;
Critical Total Ionizing Radiation Dose, γ, rads(Si),
Co-60 $\sim 10^5$ rads(Si)/hr.

Technology	Array Type	Φ_f = range, (mean)	Samples Tested	Test Conditions
TTL	DRA2001	$5\text{-}6 \times 10^{14}(5.7)$	3	$V_{BB} = 2.5V$
TTL	F9344	$1.5\text{-}2.9 \times 10^{15}(2.2)$	3	
S/C TTL	I3101	$0.7\text{-}1.4 \times 10^{15}(1.1)$	3	$V_{CC} = 5V$, all TTL
S/C TTL	I3101A	$1.4\text{-}2 \times 10^{15}(1.7)$	3	
S/C TTL	SMS8228	$2\text{-}6.6 \times 10^{14}(4.9)$	10	room temp.
S/C TTL	SN54S181	$2.1\text{-}4.5 \times 10^{14}(3.1)$	6	max. fan out
S/C TTL	SN74LS139	$0.78\text{-}1.2 \times 10^{15}$	2	max. fan out
S/C TTL	SN74LS155	$1.0\text{-}1.2 \times 10^{15}$	2	max. fan out
S/C TTL	SN74LS194	$5.7\text{-}7.8 \times 10^{14}$	2	max. fan out
ECL	MC1678	$1.9\text{-}2.6 \times 10^{15}(2.2)$	3	$V_{EE} = -5.2V$

Technology	Array Type	γ: range, (mean)	Samples Tested	Test Conditions
Si gate p-MOS	I1402	$1.4\text{-}15 \times 10^4(4.0)$	5	$V_{DD} = -10V$, $V_{CC} = +5V$
Si gate p-MOS	I1101	$2\text{-}4 \times 10^4(3.0)$	4	$V_{DD} = -10V$, $V_{CC} = +5V$
C/MOS	CD4024A	3×10^5(min)	5	$V_{DD} = 5V$, f = 1 kHz
DI TTL	HB6A	$> 10^7$	2	$V_{CC} = 5V$

Selection of electrical bias conditions during neutron/gamma irradiation is a very important consideration for MOS arrays and important, but less critical, consideration for bipolar arrays. It is well known that the threshold voltage shift on MOS transistor elements is a function of dc bias during ionizing radiation exposure.[4] This effect is illustrated in Figure 1 by the performance degradation of the CD4024 junction-isolated C/MOS counter exposed either under static dc bias, or under dynamic operation with a 50% duty cycle. The performance parameter shown is the minimum supply voltage required for operation at 1 kHz. Other system-component performance parameters, maximum frequency of operation, power-supply current, and output current-voltage characteristics showed similar results.

The number of samples to be included in an experimental characterization of component qualification must be determined in terms of system application. There are, however, some system-independent observations that might be useful. First, the number of arrays implemented in the system is typically, at least for a while, much smaller than the number of microcircuits or discrete transistors used in older systems, principally because of the limited variety, high cost, and substantial qualification effort required. Thus, a much smaller sample size can be a respectable percentage of the system requirement. Second, it has been shown that much of the variation among a sample of discrete elements is related to the statistical distribution of displacement damage in the bulk semiconductor material.[5] Thus, the probability of at least one fatal set of damage clusters in a large bipolar LSI chip is more representative of the number of transistor elements on the chip rather than the number of arrays exposed. The statistical spread in neutron displacement damage between samples of MSI/LSI arrays would then be determined by the variation in the electrical parameters that determine the margin for transistor gain degradation before failure. The results summarized in Table I give some insight into the possible spread, but generally only for small sample sizes.

Considering the problem in a different perspective, the distribution of damage in the cells of a complex array is shown in Table II for the SMS 8228 4,096-bit ROM. In this case, the performance of the internal cells was measured in groups of 4-bit words. The statistical spread in critical neutron fluence seems to be on the order of two-three, and the requirement of complete performance evaluation to determined overall array failure is re-emphasized. This variation in damage is consistent with the expected variations considering both the distribution of damage (20-40%) and electrical parameters (100%).[5]

In addition to the considerations of radiation-induced permanent damage in MSI/LSI arrays, damage due to electrical pulse overstress (possibly resulting from system-generated EMP) has been investigated. Here, the

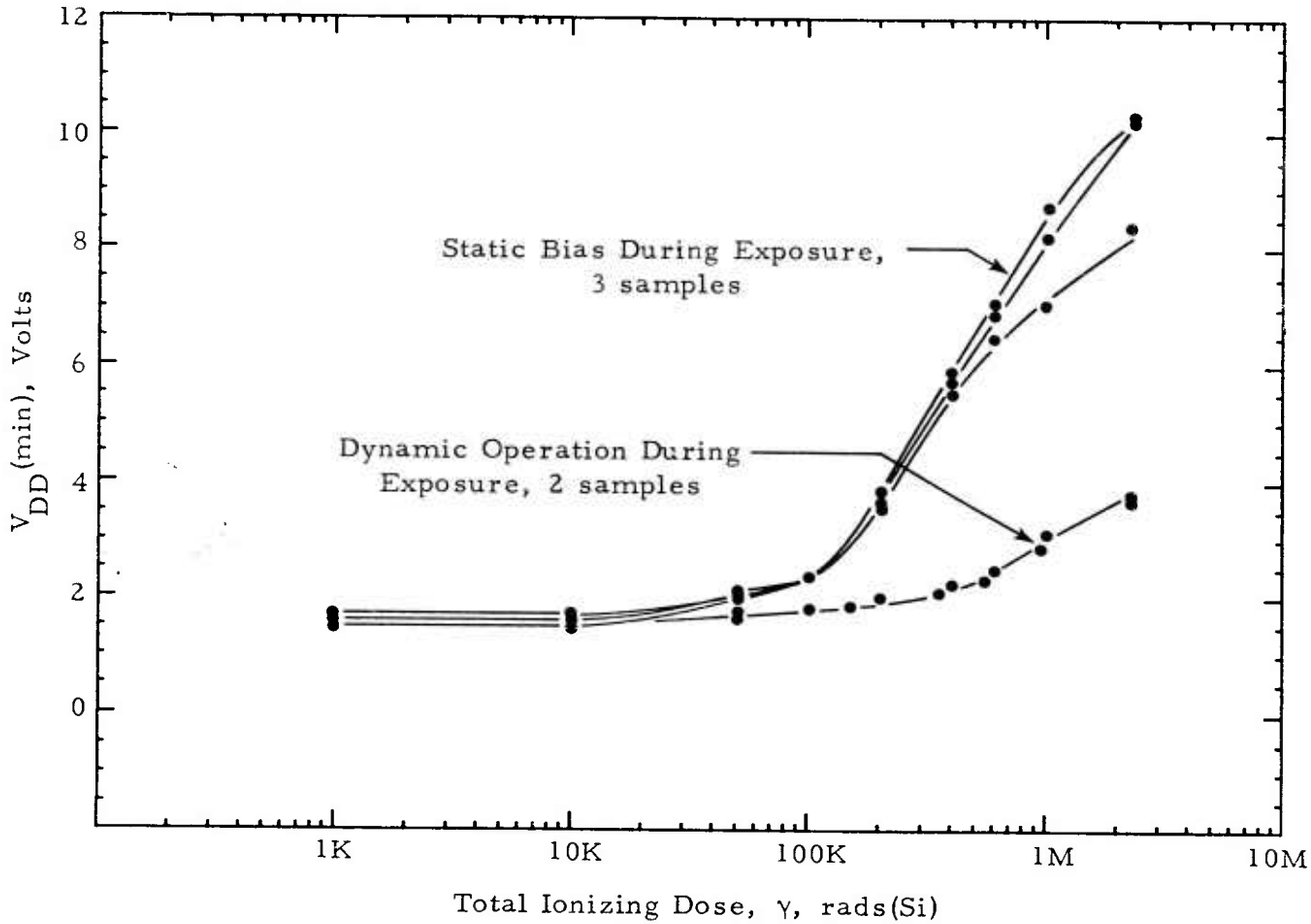

Figure 1. Variation of C/MOS CD4024 Total Dose Vulnerability with Bias During Exposure.

TABLE II

NEUTRON-INDUCED FAILURE, SMS8228, S/C TTL
4,096-BIT READ-ONLY-MEMORY, $T_c = 80^oF$

	Fraction of Bad 4-bit Words		
	Neutron fluence, n/cm^2 (1 MeV equiv.)		
Sample #	2.1×10^{14}	4.5×10^{14}	6.6×10^{14}
1	0	0.08	0.46
2	0.01	0.08	0.69
3	0	0	0.03
4	0	0.01	0.76
5	0	0.01	0.21
6	0	0	0.11
7	0	0	0.12
8	0	0	0.08

problem is in defining a test sequence to determine the worst-case susceptibility with a minimum number of samples. Also, since this study was independent of system applications, the pulsed overstress was in terms of rectangular pulses of varying pulse width, peak level, and polarity. Observed failure levels on a variety of MSI/LSI arrays are summarized in Table III in terms of the pulsed overstress energy for the polarity and terminal application observed as worst-case. The number of samples involved in the study was small (usually 6 or less) and no statistical or absolute worst-case vulnerability is suggested. Pulse-width at failure has been normalized to 1 μs, assuming in some cases, a square-root dependence of failure on overstress pulse-width. In all cases, the array was biased under normal operating conditions in terms of supply voltage and ground return. Fortunately, it is possible in many cases to measure the overstress vulnerability of some terminals of the array without destroying overall array performance, allowing additional terminal-stress characterization. In most cases, the array failure was a dramatic breech in overall array performance, but in some cases, the failure was a degradation of the current-voltage characteristics at the stressed terminal. Array operation in the case of terminal I-V damage could be sustained, but only with prohibitively high loading of the external circuit. Results of the EPO vulnerability measurement on the bipolar arrays are consistent with the results on planar transistor damage for elements of comparable geometry and considering energy sharing when several elements are connected to the input or output terminal. Failure levels for the MOS arrays are determined principally by the input protection networks which, as shown in Table III, can be very adequate for junction-isolated arrays, but are more sensitive for arrays fabricated on an insulating substrate.

Damage energy for all the arrays listed in Table III was delivered by the external electrical pulse overstress. Electrically-induced latch-up, not observed in any of these devices but reported on some junction-isolated SSI devices,[6,7] could cause damage through the energy drawn from the dc power supply. The critical overstress energy, in this case then, is that required to induce latch-up and may be quite different from that required to induce damage directly.

Transient Photoresponse

The transient photoresponse of MSI/LSI arrays is the result of radiation-induced p-n junction photocurrents. In junction-isolated arrays the principal effect is the substrate junction photocurrents (i.e., collector-substrate in bipolar structures and drain/source-substrate in p-MOS structures). The magnitude of the junction photocurrent is determined by the junction area, the substrate lifetime and the radiation pulse-width. The effect in the array, however, also involves the time-dependent current-noise tolerance in each logic cell as well as the overall electrical switching requirements. Transient failure (or radiation-induced upset) can be either the distortion of an external

TABLE III

SUMMARY OF MEASURED MSI/LSI EPO SUSCEPTIBILITY

Array	Technology	Function	W_{TO}* $\mu J/\sqrt{\mu s}$	Stressed Terminal
Fairchild 4501	DTL	Quad LSI Gate Cell	6	Input: + pulse
T.I. SN5420	TTL	Dual NAND Gate	13	Input: + pulse
Fairchild 9344	TTL	2 x 4-bit Multiplier	100	Input: + pulse
T.I. DRA2001	TTL	506-bit Shift Reg.	90	Input: + pulse
Mot. MC315	ECL	5-input NOR Gate	8	Input: - pulse
Mot. MC1678	ECL	4-bit Counter	200	Input: - pulse
Intel I3101	S/C TTL	64-bit RAM	100	Input: + pulse
T.I. SN54S181	S/C TTL	Arith. Logic Unit	5	Input: +/-
SMS 8228	S/C TTL	4,096-bit ROM	8	Input: +/-
RCA 045B	p-MOS	2-bit Adder	60	Input: + pulse
Intel 1101	p-MOS	256-bit RAM	12	R/W Input: + pulse
Intel 1402	p-MOS	1024-bit Shift Reg.	41	Input: - pulse
RCA CD4024	C/MOS	7-stage Counter	1600	Input: +/-
			190	Output: - pulse
Inselek INS4007	C/MOS	Triple Inverter(SOS)	17	Output: +/-
			0.1	Input: +/-

*Susceptibility was measured for rectangular pulse input at pulse widths ranging from 0.1 to 10 μs. The energy constant at 1 μs does not necessarily represent experimental results.

logic signal to an undefined or erroneous voltage level, or an internal effect that prevents normal electrical response of the overall array. If the logic cells that are influenced are non-memory cells (e.g., gates) the radiation-induced effect is transient. If memory logic cells are influenced, however, the logic upset will remain until cleared by correct input data.

Variation of the magnitude of the substrate photocurrents with radiation pulse width can be observed directly when the electrical response of the array is fast compared to the time constants of the photocurrent. In this case, the transient failure occurs when the substrate photocurrents just exceed the current-noise margin in the logic cells. The time dependence of the substrate photocurrent to a step turn-on radiation pulse is

$$\hat{i}_{pps} = qA_{js}g_o\dot{\gamma}\left[L_s \operatorname{erf}\left(\frac{t_p}{\tau_s}\right)^{1/2} + x_{mj}\right]$$

where A_{js} is the substrate junction area

g_o is the carrier generation constant (4×10^{13} carriers/rad(Si))

$\dot{\gamma}$ is the dose rate (rads(Si)/s)

L_s is the substrate minority carrier diffusion length

τ_s is the substrate minority carrier lifetime

and, x_{mj} is the substrate junction depletion layer width. For a given current-noise margin in a fast MSI/LSI array, the critical failure level dose rate will decrease as the radiation pulse width increases until the radiation pulse width is substantially greater than the substrate minority carrier lifetime. An example of this effect is shown in Figure 2 as the transient failure level of a Schottky-clamped TTL Random-Access-Memory. The substrate minority carrier lifetime, in this case, was on the order of 2 μs. The relatively long substrate lifetime in S/C TTL over earlier TTL is a direct result of eliminating transistor saturation. Saturated storage time limitations in TTL switching response required lifetime-limiting gold-doping. As a result of the long substrate minority carrier lifetime, the critical radiation dose rate as determined in a 30 ns 2 MeV flash x-ray pulse may be a factor-of-ten greater than that determined in a 4 μs LINAC x-ray pulse.

Transient failure levels measured for a wide variety of arrays are summarized in Table IV for narrow- and wide-pulse ionizing radiation environments. The critical dose rates for the TTL arrays are approximately equal, reflecting the lower substrate lifetime due to gold-doping. The critical dose rates for all the S/C TTL arrays are much lower in the wide-pulse

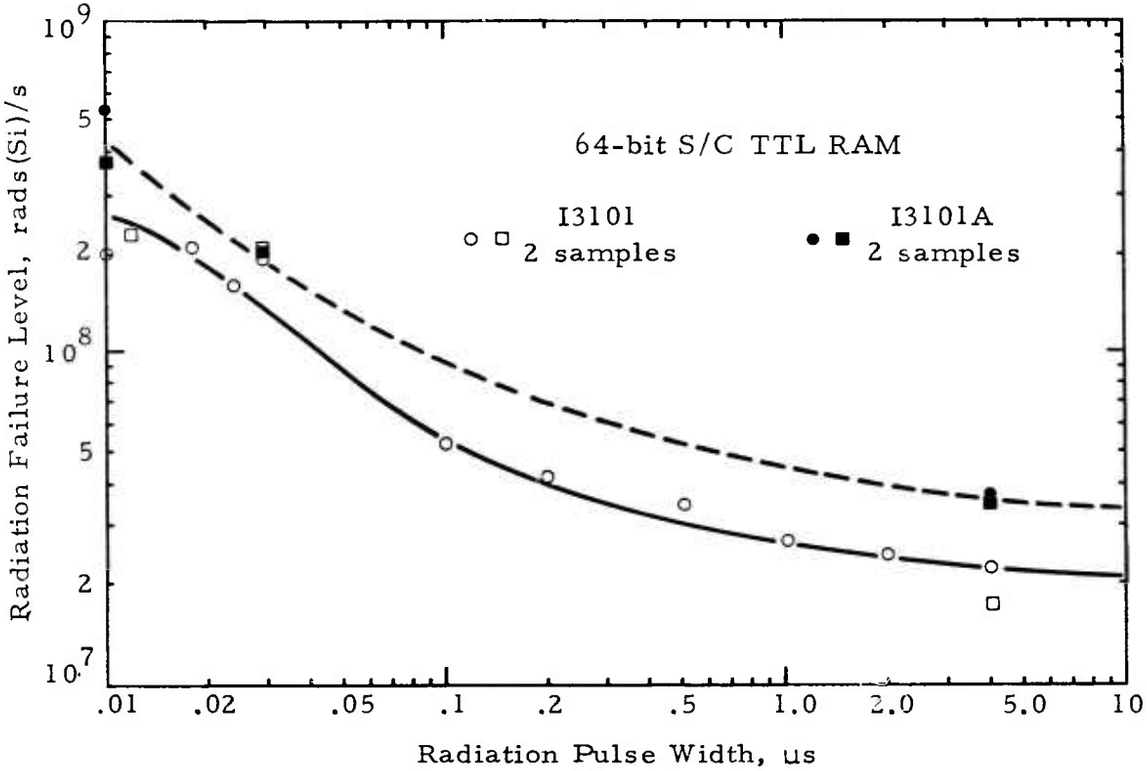

Figure 2. Pulse-Width Dependence of Transient Vulnerability.

TABLE IV

MSI/LSI TRANSIENT SUSCEPTIBILITY

$\dot{\gamma}_c$, rads(Si)/s

Array Type	Narrow-pulse $t_p \simeq 30$ ns	Wide-pulse $t_p \simeq 4\mu s$	Technology
DRA2001	$2 - 4 \times 10^8$	$2 - 2.5 \times 10^8$	TTL
F9344	$2 - 5 \times 10^8$	4×10^8	TTL
MC1678L	$3 - 5 \times 10^8$	$1 - 1.5 \times 10^8$	ECL
I3101	$1.9 - 2.2 \times 10^8$	$1.7 - 2.2 \times 10^7$	S/C TTL
I3101A	$1.9 - 2.2 \times 10^8$	$3.4 - 3.7 \times 10^7$	S/C TTL
SMS8228	$2 - 3 \times 10^7$	$\sim 2 \times 10^6$	S/C TTL
SN54S181	$1.5 - 4 \times 10^8$	$\sim 2 \times 10^7$	S/C TTL
SN74LS139	$5 - 10 \times 10^8$	$\sim 3 \times 10^7$	S/C TTL
SN74LS155	$1.5 - 3 \times 10^8$	$\sim 3.5 \times 10^7$	S/C TTL
SN74LS194	$1.5 - 2 \times 10^8$	$\sim 1.5 \times 10^7$	S/C TTL
RCA045B	$2 - 5 \times 10^9$	$1.1 - 2.2 \times 10^8$	p-MOS(static)
I1101	$2 - 3 \times 10^8$	1.7×10^8	p-MOS(static)
CD4024	$1.4 - 1.7 \times 10^8$	$\sim 5 \times 10^6$	C/MOS
MC14021	$3 - 10 \times 10^8$	$2 - 4 \times 10^7$	C/MOS

environment, reflecting relatively long substrate lifetimes, illustrating the effect most dramatically. The ECL and p-MOS arrays also have long-lifetime substrates and illustrate a decreasing critical dose rate with increasing radiation pulse width. The substrate photocurrent effect is somewhat obscured in the ECL vulnerability due to the influence of the fast collector-base photocurrent, and in the p-MOS arrays by the relatively slow electrical switching response.

Another aspect of the pulse-width dependence of the photoresponse is illustrated by the dynamic-logic MOS array. Information is stored in the dynamic array by charge on p-n junction and gate capacitances of the individual elements. This is in contrast to the static-logic bipolar and MOS arrays where the digital information is stored in dc currents of the gate and flip-flop cells. In the dynamic array, the effects of the junction photocurrents is simply to discharge the stored information. Information in the dynamic logic array must, in any event be refreshed periodically because of the charge loss due to the thermal junction leakage currents. The presence of steady-state ionizing radiation at low levels, in this case, requires that the data stored be refreshed more frequently, or in other words, the minimum frequency of operation must be increased. In radiation exposure of the Intel 1406 dynamic shift register to the ionizing radiation environment of a cobalt-60 cell, the measured minimum frequency of operation was increased from $\sim$ 0.2 Hz with no radiation, to 4 Hz with an exposure of 11 rads(Si)/s. This is a transient effect and has no influence on the ionizing radiation induced transistor threshold voltage shift that will cause array failure if the exposure is continued too long. When the dynamic array is exposed to a pulsed ionizing radiation environment the critical dose rate for transient upset is a strong function of the radiation pulse width and the data refresh rate (e.g., clock rate). If the radiation pulse width and subsequent photocurrent time constant (on the order of the substrate lifetime) are both short compared to the array clock rate (typically 100 kHz maximum) then the critical capacitor discharge is determined only by the total photocharge and the observed failure level depends only on the total dose of the radiation pulse and not the dose rate. This is illustrated in Figure 3 for the effects as observed in three types of dynamic MOS/MSI arrays.[8] This pulse-width dependence of transient upset is characteristic of the nature of the logic cell of dynamic arrays in general and should be considered in the transient photoresponse of emerging charge-coupled-device (CCD) logic arrays and image sensors.

Another critical aspect of the transient photoresponse in MSI/LSI arrays is the selection of biasing and input signal conditions to be employed in the experimental determinant of array vulnerability. In terms of the overall array performance, the transient photoresponse can be critical either in an observable output photoresponse, or by the photoresponse of an internal

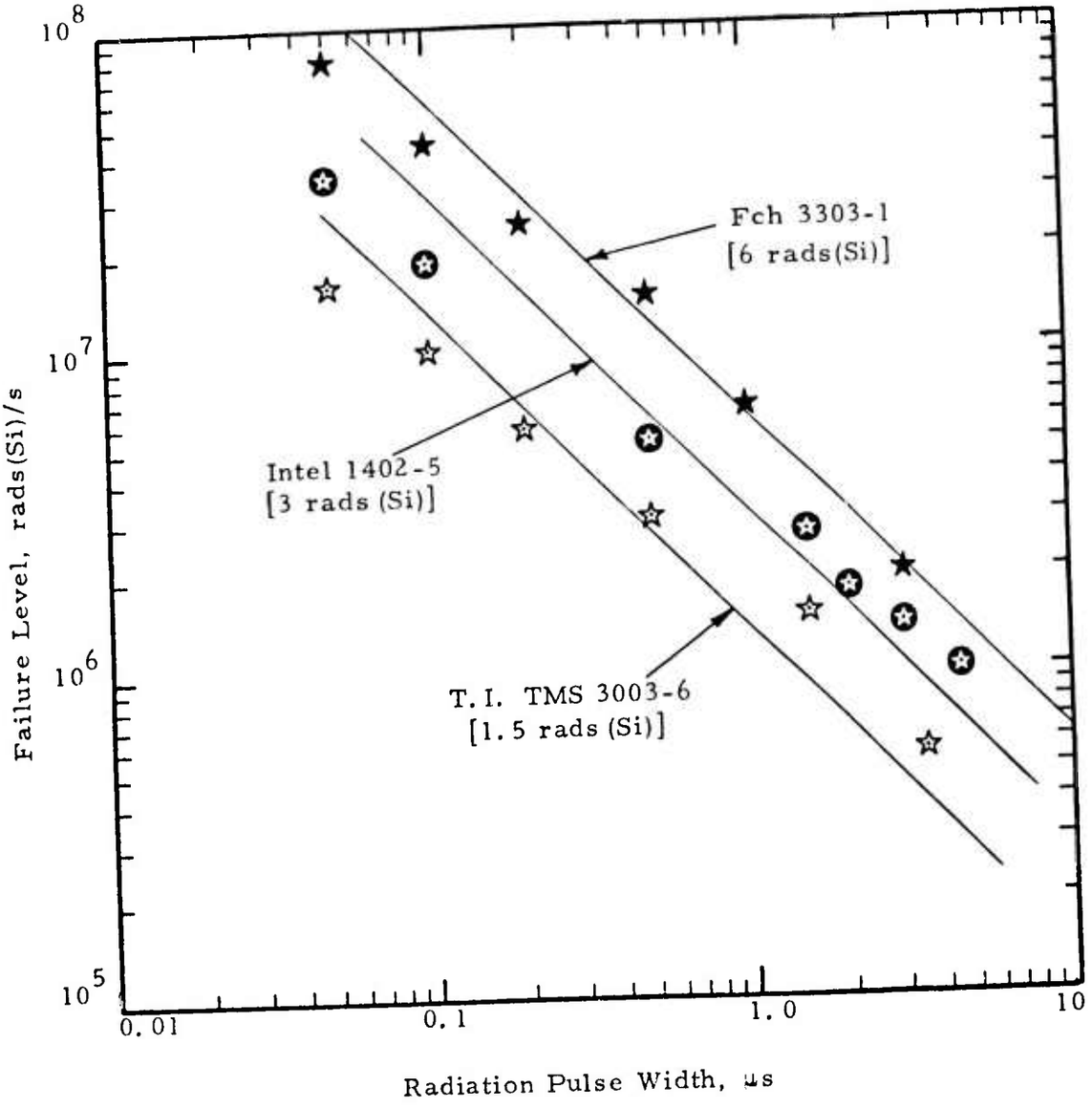

Figure 3. Critical Dose for Dynamic Shift Register Transient Failure.

cell(s) that compromise normal array logic function. Transient failure of an internal logic function will compromise the dynamic performance of the array, but is not necessarily observable in a measurement of output photoresponse under all operating conditions. Bias conditions on the array during exposure can either be static, in which the array is exposed for a specific set of dc input logic states, or dynamic in which the array is sequenced through a series of switched input combinations. The observed effect is a complex function of the operation during radiation exposure, radiation pulse width, and electrical switching response of the array.

As an example, consider a 2 x 4-bit multiplier (Fairchild 9344) photoresponse. The array is an interconnection of gate cells with no memory elements (combinatorial). Under static bias conditions any of the six outputs can be set to either logic state by many input combinations. If the output photoresponse were due only to the output gate the 1- and 0-state transients would be independent of the input logic combinations used to define the output state. Experimentally, the output photoresponse of the 9344, as shown in Figure 4, shows a substantial statistical distribution of output photoresponse as a function of the input combination selected to produce either a 1- or 0-state output. This statistical output photoresponse can be interpreted as either the transient photoresponse of internal gate cells propagating to the output, or that the influence of the input bias conditions on the output photoresponse. In order to thoroughly evaluate the output photoresponse of an n-input combinatorial logic array (assumed irredundant) it would be necessary to measure the photoresponse under 2^n input conditions parametrically with radiation intensity, searching for the worst-case condition of logic upset. For ther 14-input 9344, the data shown in Figure 4 represents less than 10% of the total possible static input conditions. Also, under static input bias conditions in a narrow-pulse ionizing radiation exposure, the critical upset of an internal logic cell may not propagate to the output and therefore not be observed. This logic upset would, however, compromise the normal logic operation of the overall array.

Experimental evaluation of the transient photoresponse of complex arrays must, therefore, be supplemented by exposure under dynamic operating conditions as well. For arrays containing memory elements, such as shift registers, this can be done in a narrow-pulse environment by the sequential flow of input data and output result. The effects in combinatorial arrays can be further investigated by dynamic input sequencing and output observation during exposure in a wide-pulse ionizing radiation environment. Results of the critical transient upset levels for a bipolar TTL LSI shift register as a function of input sequence pattern are shown in Table V. The variation in critical dose rate with input pattern is not dramatic, but does show a significant effect. The transient photoresponse of an MSI array under dynamic operation in a wide-pulse ionizing radiation environment is shown in

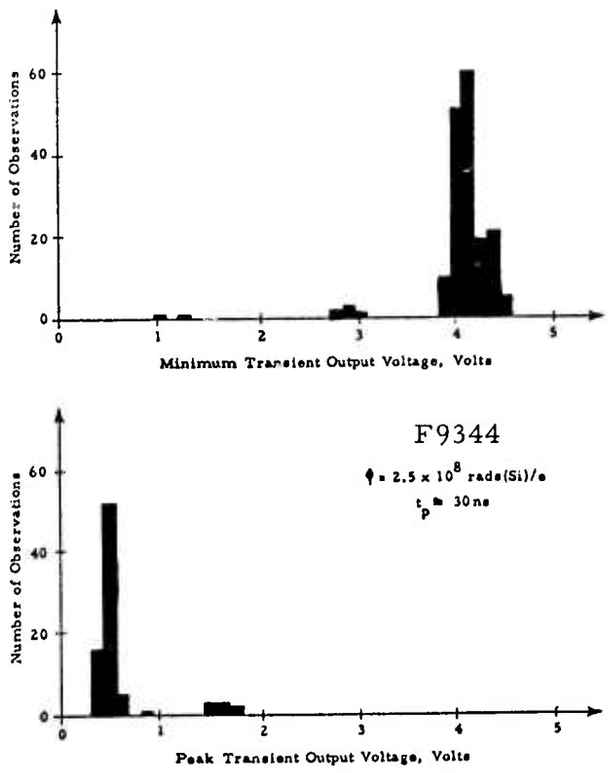

Figure 4. Logic Circuit Statistical Output Photoresponse.

TABLE V

DRA 2001 DUAL 256-BIT TTL SHIFT REGISTER, NARROW-PULSE TRANSIENT FAILURE LEVEL,

2 MeV Flash X-Ray

Sample Number	Observed Transient Failure Level, Peak Dose Rate Stored Data Pattern		
	All "Ones"	All "Zeros"	Alternating 1's and 0's
1	.4-.5 rads(Si)/ns	.4-.5 rads(Si)/ns	.4-.5 rads(Si)/ns
2	.8-1.0 rads(Si)/ns	.5-.6 rads(Si)/ns	.3-.4 rads(Si)/ns
3	.7-.8 rads(Si)/ns	.4-.5 rads(Si)/ns	.2-.3 rads(Si)/ns
4	.5-.6 rads(Si)/ns	.7-.8 rads(Si)/ns	.4-.5 rads(Si)/ns
5	.6-.7 rads(Si)/ns	.5-.6 rads(Si)/ns	.4-.5 rads(Si)/ns

Figure 5. It is very difficult to sep rate out the possible effects of an internal logic cell failure from the simpler pulse-width dependence of the photoresponse. It is clear, however, that a generalized worst-case experimental determinal of the transient photoresponse in complex MSI/LSI arrays must include characterization under both static and dynamic logic operating conditions in both narrow- and wide-pulse ionizing radiation environments.

Because of the complexity of transient photoresponse characterization without recourse to direct measurement of logic cell photoresponse, the futility of the completely-experimental characterization is becoming obvious. It is clear, then, that analytical techniques must be used to restrict the experimental investigation to those test conditions that will include the case of worst-case array vulnerability. Techniques of logic simulation of digital arrays, and simplified modeling of mic rocircuit functions must be applied to the time-dependent transient upset problem as they have already been applied to test-sequence-definition and fault-isolation for permanent damage effects in complex digital systems and MSI/LSI arrays.

A radiation-induced transient error can be introduced in a digital system by a voltage transient on the dc power supply as well as from the direct photoresponse of the logic signal outputs. The power supply voltage transient is the result of the surge current resulting from the combined component power supply photocurrents. The power supply photocurrent of a junction-isolated MSI/LSI array is the sum of the substrate junction photocurrents and the primary/secondary photocurrents of the active or parasitic transistor elements. In other words, the response is the sum of the substrate response and the circuit response. The potential effects of the circuit photoresponse and power supply photocurrent, must, as a practical matter, be evaluated independently. The circuit transient vulnerability is measured first in terms of the input/output logic signals with a well-regulated power supply. The power supply photocurrent is then measured for a range of radiation exposures below the transient logic failure level. The variation of the power supply photocurrent with ionizing radiation dose rate is generally non-linear in the range of the logic failure level. The dose-rate dependence of the substrate photoresponse is relatively linear, but that of the circuit response is typically non-linear.

The normalized power supply photocurrent measured on several types of bipolar and MOS arrays in a narrow-pulse ($\sim$ 30 ns) ionizing radiation environment are plotted in Figure 6 as a function of the total chip area. The measurement reflects the circuit condition of the worst-case photoresponse at the critical dose rate. Empirically, the measured power supply photocurrent is roughly proportional to chip areas with different scale factors for bipolar and p-MOS arrays. The scale factor for the bipolar arrays is

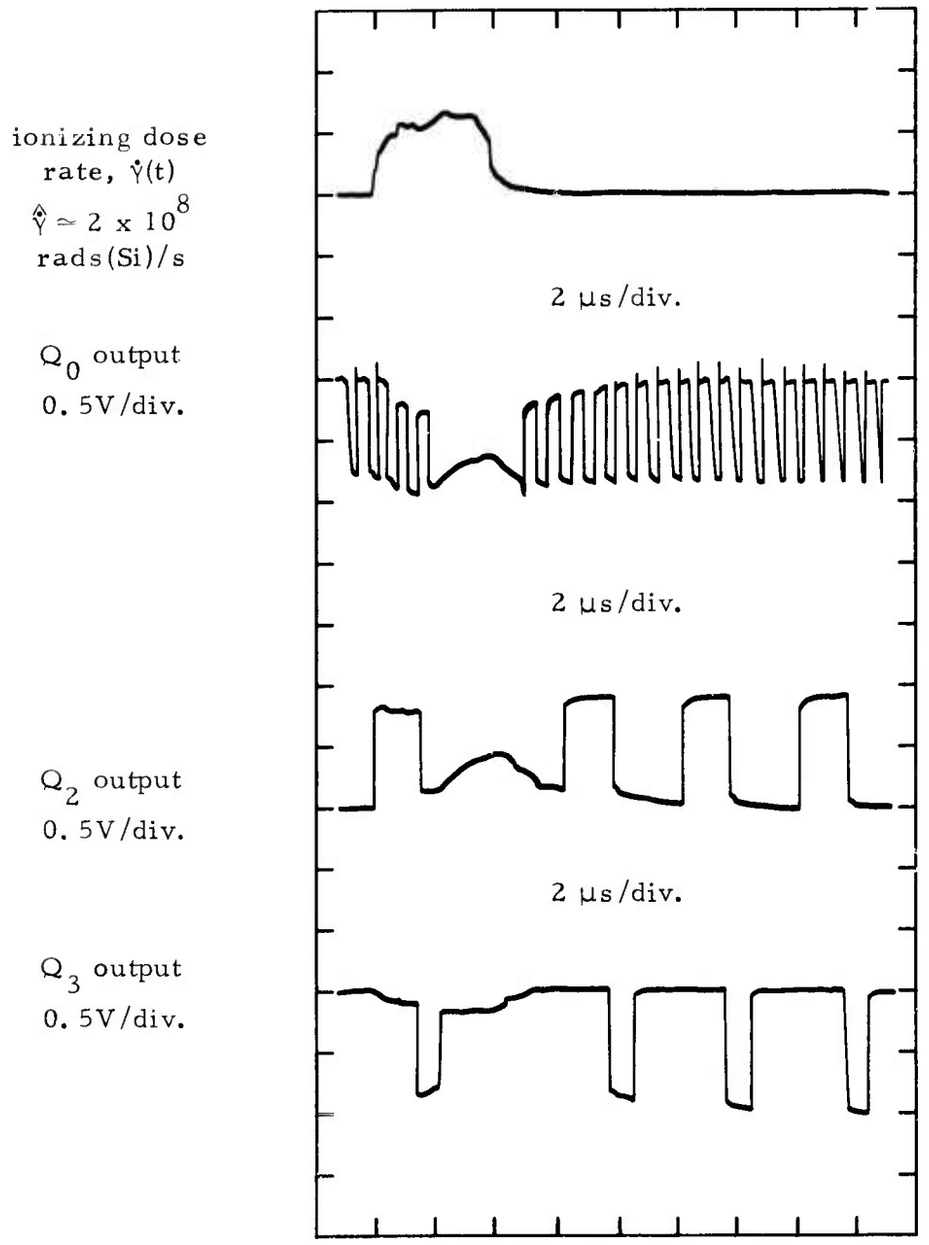

Figure 5. MC1678L ECL Four-bit Counter Wide-Pulse Photoresponse.

on the order of 7×10^{-9} A/rad(Si)/s/cm^2 and is on the order of 1×10^{-9} A/rad(Si)/s/cm^2. Extensive variations in chip area were not included for the C/MOS arrays, but the limited data fall between the bipolar and p-MOS scale factors. For reference, the photocurrent expected for a single diode whose area is equal to the entire chip area also has been plotted on Figure 6.

Conclusions

The unique aspects of MSI/LSI vulnerability characterization have been emphasized with the principal intent of demonstrating the solution of an important problem that is more complex than complicated. Adjustment to the complexity of the arrays is principally a natural requirement of the increased complexity of the system electrical performance. Basic radiation-induced failure mechanisms are all familiar as well as the bias-dependence of effects resulting from neutron/gamma exposure. Even these familiar effects, however, must be interpreted in terms of new logic cell technologies in ways that are not necessarily obvious from studies on basic elements and microcircuits. The most formidable problem of MSI/LSI characterization is that of transient effects such as the photoresponse or short-term annealing. It is clear that there is a level of system-component complexity beyond which a completely experimental characterization is clearly impractical. Analytical techniques, conventionally used to quantitatively predict and correlate experimental results must now be used to qualitatively identify the array response to supplement the experimental determination of the worst-case transient failure.

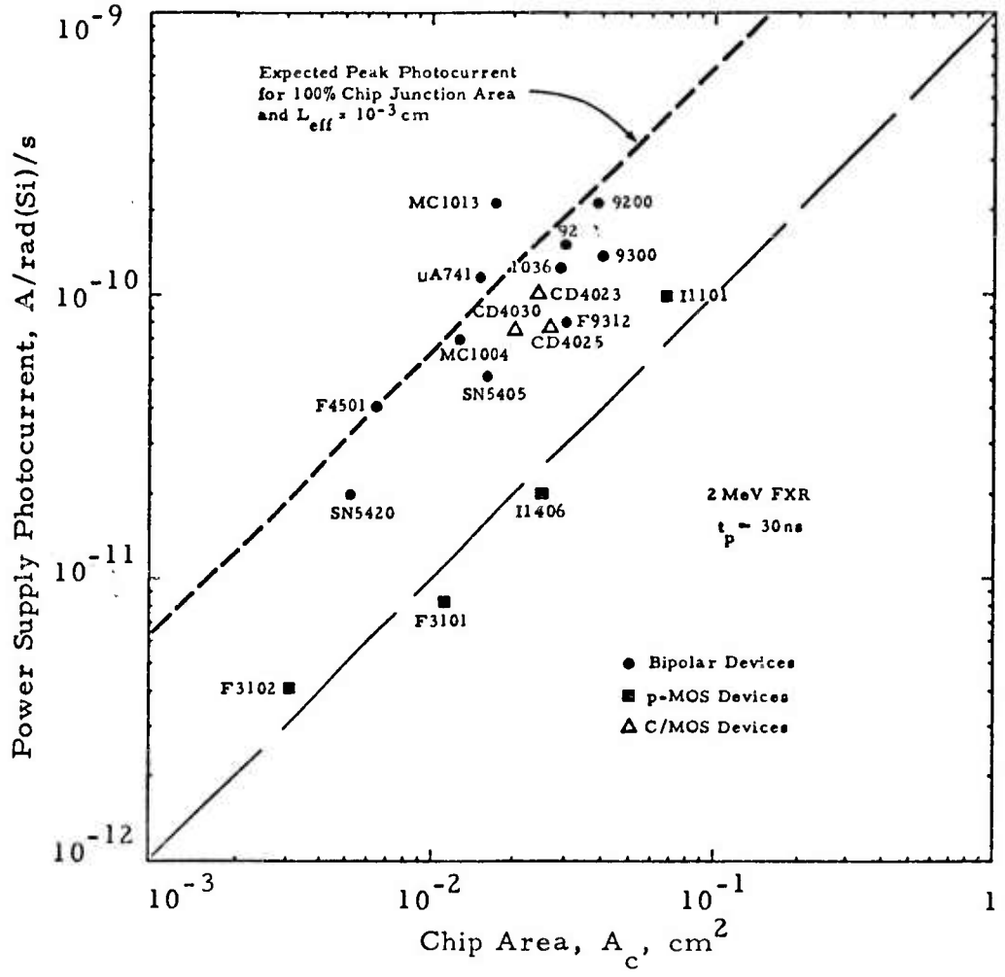

Figure 6. MSI/LSI Array Power Supply Photocurrents.

APPENDIX A

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APPENDIX B

TEST CIRCUIT SCHEMATICS

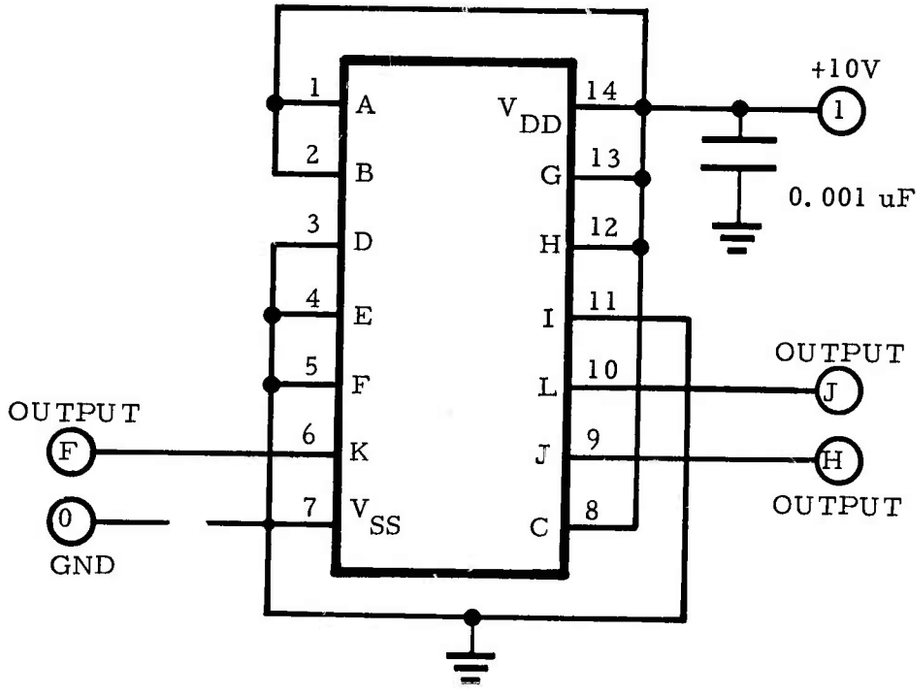

Figure B-1. CD4023A, triple 3-input NAND gate, static input test element.

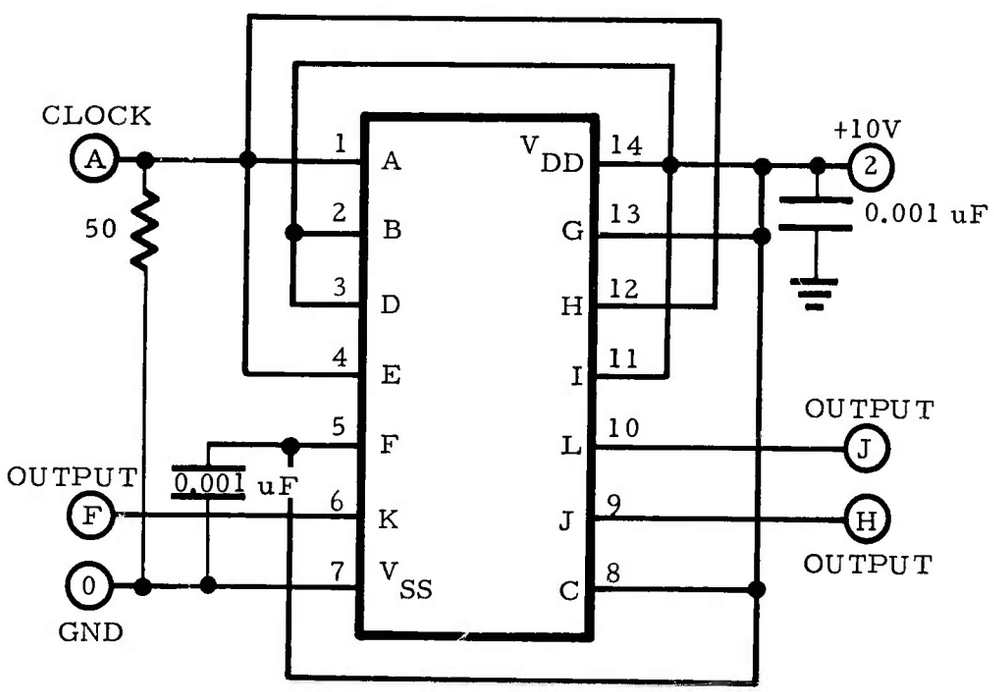

Figure B-2. CD4023A, triple 3-input NAND gate, dynamic input test circuit.

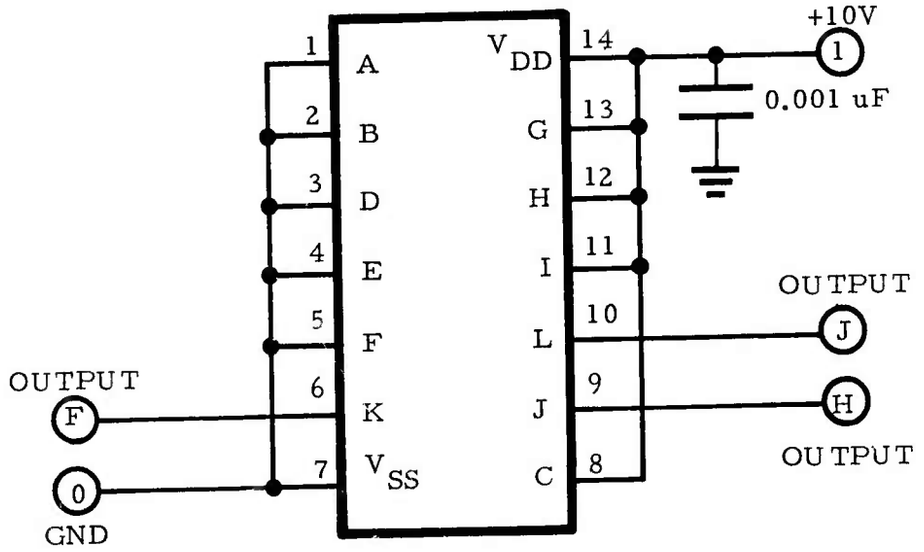

Figure B-3. CD4025A, triple 3-input NOR gate, static input test circuit.

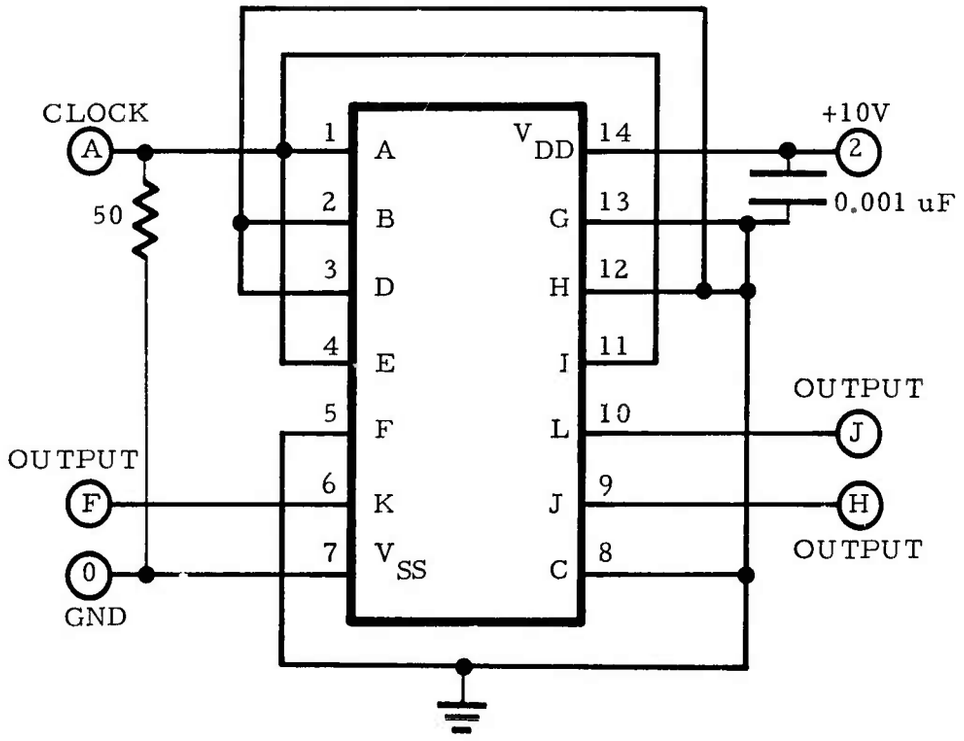

Figure B-4. CD4025A, triple 3-input NOR gate, dynamic input test circuit.

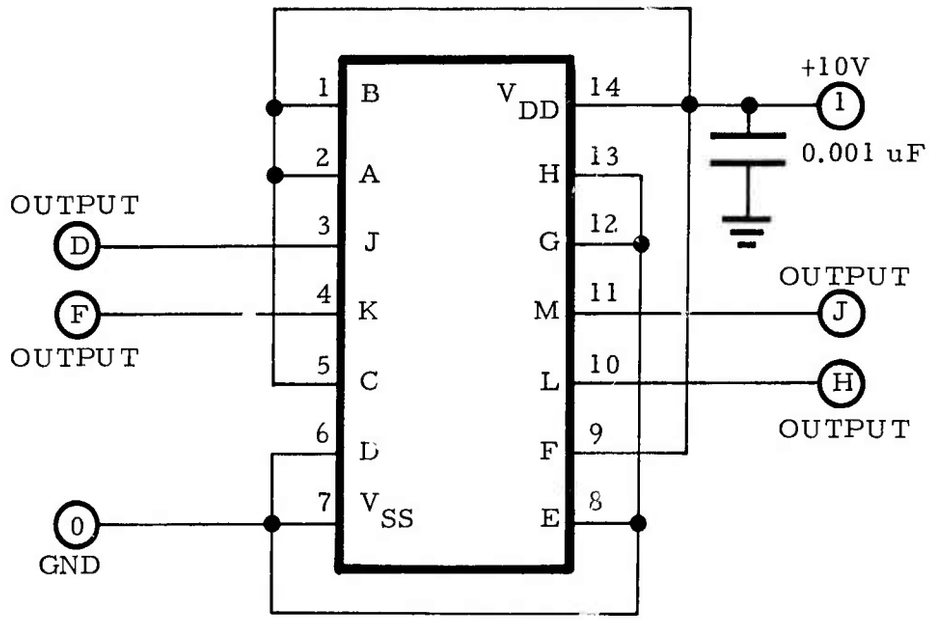

Figure B-5. CD4030A, quad exclusive-OR gate, static input test circuit.

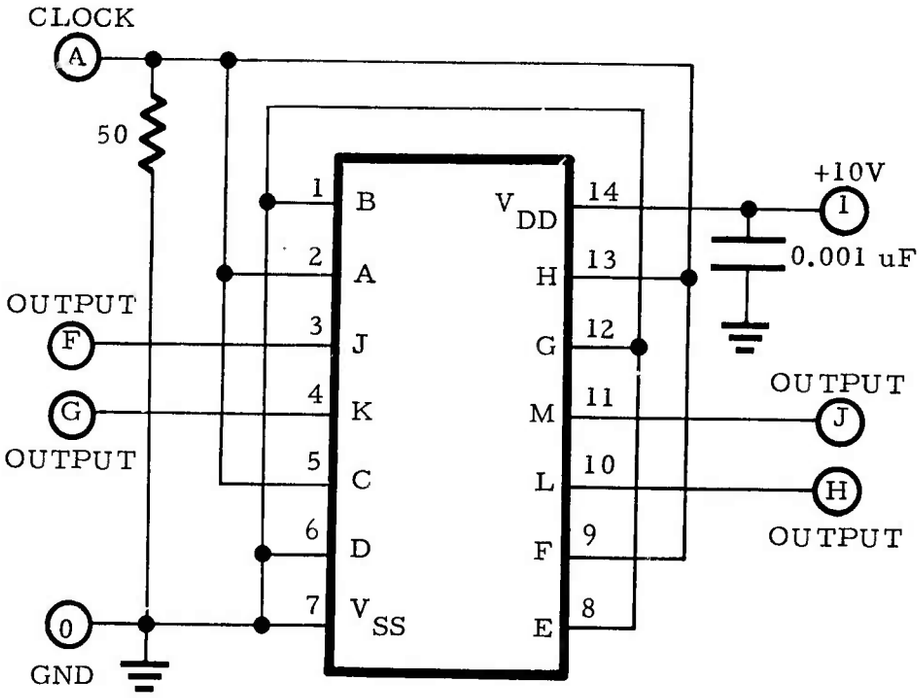

Figure B-6. CD4030A, quad exclusive-OR gate, dynamic input test circuit.

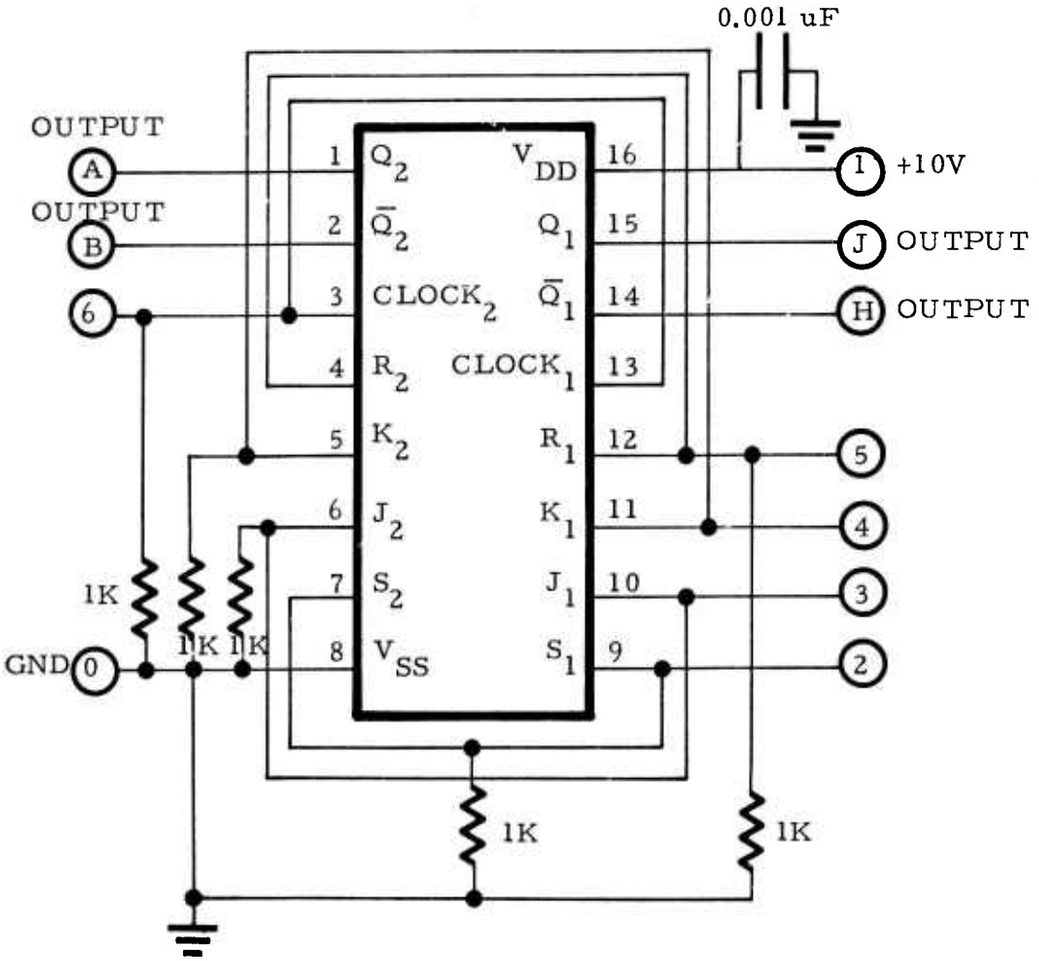

Figure B-7. CD4027A, dual J-K flip-flop, static input test circuit.

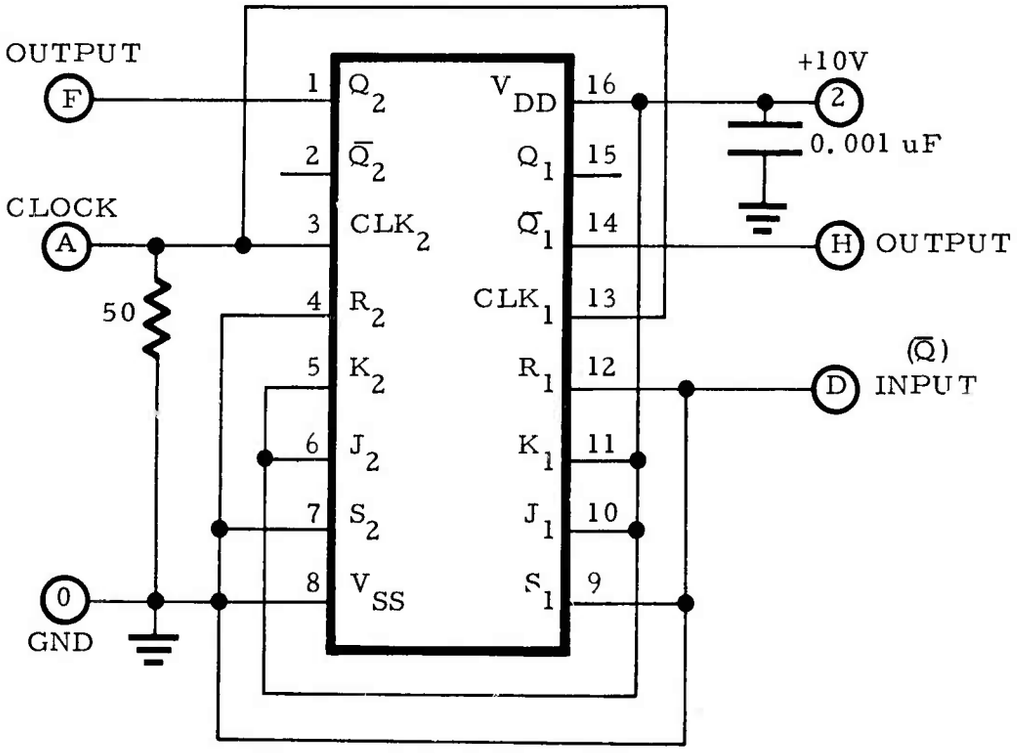

Figure B-8. CD4027A, dual J-K master slave flip-flop dynamic input test circuit.

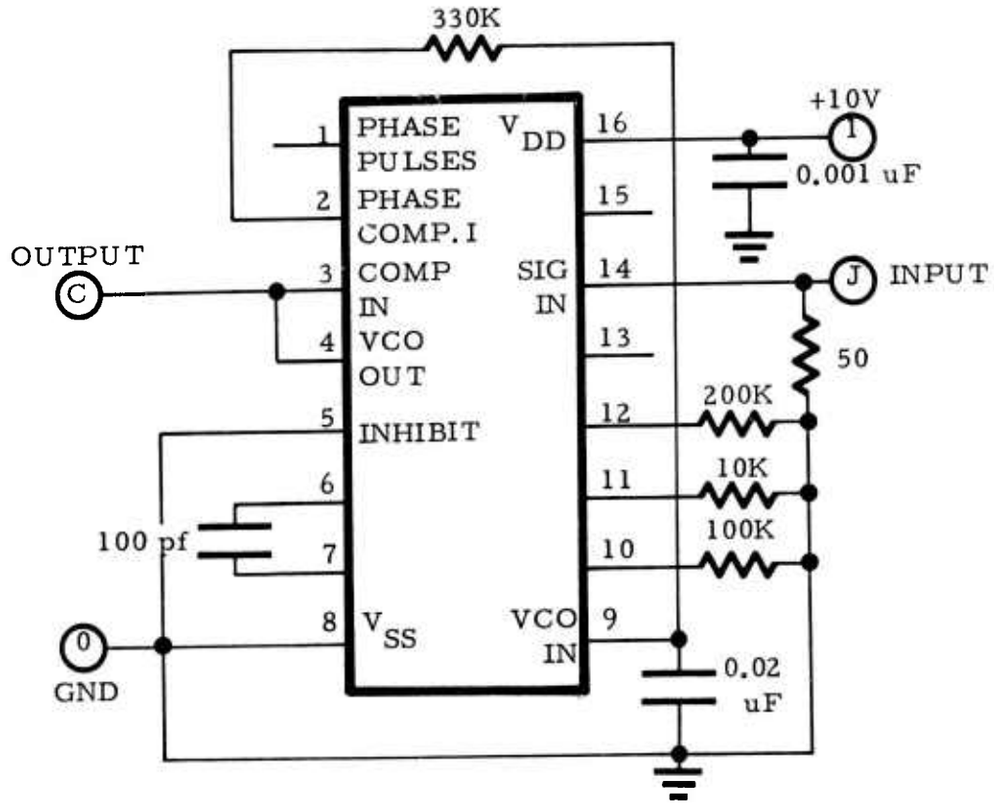

Figure B-9. CD4046A, phase-locked loop, Phase Comparator I, test circuit.

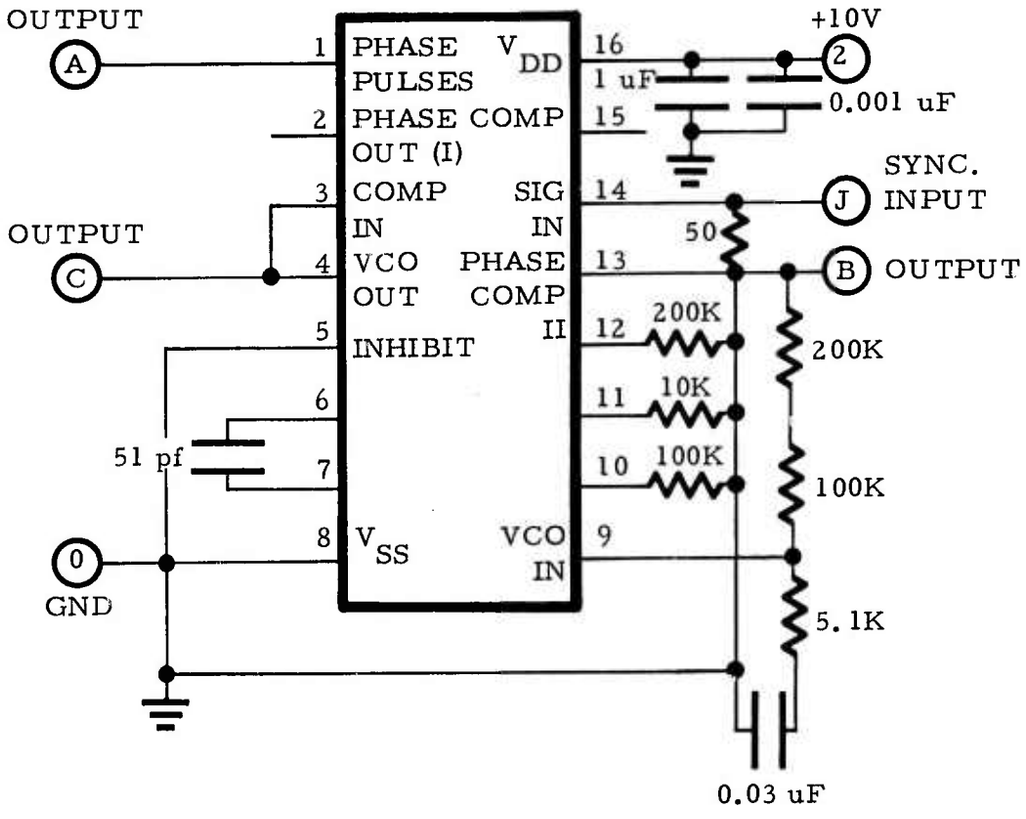

Figure B-10. CD4046A, phase-locked loop, Phase Comparator II, test circuit.

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