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RF-4C DIGITAL SIGNAL TRANSFER UNIT
MULTISENSOR DISPLAY SYSTEM (DSTUMDS)

Texas Instruments Incorporated
Post Office Box 6015
Dallas, Texas 75222

February 1976

TECHNICAL REPORT AFAL-TR-75-170
Final Technical Report for Period 1 November 1973 - 15 September 1974

AIR FORCE AVIONICS LABORATORY
AIR FORCE WRIGHT AERONAUTICAL LABORATORIES
AIR FORCE SYSTEMS COMMAND
WRIGHT-PATTERSON AFB, OHIO 45433

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This document is a final report which describes the design, development, and preliminary evaluation of a Digital Signal Transfer Unit Multisensor Display System (DSTUMDS) for the RF-4C aircraft and associated avionics equipment. The program was performed under Contract F33615-74-C-1111 for the Air Force Avionics Laboratory (AFAL), Wright-Patterson Air Force Base, Ohio. The body of this report outlines program objectives, equipment description and a general theory of equipment operation.

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PREFACE

The engineering development effort described in this
report was closely associated with two other concurrent
development efforts; the AN/APQ-99 radar MTI modifica-
tion program performed under ASD contract F33657-74-C-0363
and the Black Crow development program conducted by ASD.
These three development efforts and ensuing flight tests
comprised phase one (1) of the RF-4C Quick Strike Program.

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INTRODUCTION

This document is a final report which describes the design, development and preliminary evaluation of a Digital Signal Transfer Unit Multi-sensor Display System (DSTUMDS) for the RF-4C aircraft and associated avionics. The DSTUMDS program was performed under Contract F33615-74-C-1111 for the Air Force Avionics Laboratory (AFAL), Wright-Patterson Air Force Base, Ohio.

The DSTUMDS program can be considered as consisting of two basic phases; development and bench integration. The development phase consisted of: (1) the design and fabrication of one DSTUMDS system consisting of two line replaceable units and (2) the safety-of-flight certification of that equipment. The equipment was bench integrated with an AN/APQ-99 Radar System developed by ASD/ENAMD. Flight test evaluation of the DSTUMDS is scheduled to begin in early 1975.

The body of this report outlines the program objectives, equipment description and general theory of operation. Problems encountered and solutions implemented are also discussed.

SECTION II
PROGRAM OBJECTIVE

The RF-4C DSTUMDS Program is a part of the Quick Strike Reconniassance, Phase One Program. The objective of the Quick Strike Program is to provide near real time identification, location, and disposition of enemy targets. The Phase One effort is intended to evaluate an RF-4C sensor complement designed for target detection and identification through the simultaneous use of various independent sensors. The program required the addition of several sensors; a modification to the AN/APQ-99 Forward Looking Radar (performed under contract F33657-74-C-0363) to provide Moving Target Indication (MTI) capability, and the development of an improved display system with the following capabilities:

(1) Provide improved mapping resolution for the existing AN/APQ-99 Forward Looking Radar.

(2) Display Black Crow sensor information in a synergistic fashion simultaneously with radar PPI map and MTI information.

(3) Provide the potential of displaying TV (525-line) and FLIR (875-line) information.

(4) Provide in-flight video recording capability of all information displayed.

The general objective of the DSTUMDS program was the development of a Flyable Brassboard Digital Scan Converter Display System which would provide these capabilities. Specific tasks included designing, fabricating and qualifying for flight test, two prototype line replaceable units (LRU's); a Radar Pilots Indicator (RPI) Unit to replace the AN/APQ-99 Radar Pilots Indicator Unit and an Interface and Control Unit (ICU).

These units were designed, using as a spring-board, the existing design of a DSTUMDS developed for and flight tested in the F-4E aircraft. Interface requirements dictated that the following new blocks of circuitry be developed:

(1) Black Crow interface and processing circuitry.

(2) Cursor generation circuitry.

(3) Hyperbolic ground range correction circuitry for true ground range radar PPI modes.

(4) E^2 video correction circuitry for the radar terrain following display format.

(5) Video and range logic circuitry for interface with the AN/APQ-99 Radar and the MTI processor.

(6) Synchro-to-digital conversion of AN/APQ-99 Radar antenna position information.

Upon completion of design and fabrication of the two DSTUMDS LRU's proper DSTUMDS interface was verified with the AN/APQ-99 Radar, modified for MTI capability, as well as with the Black Crow system. Following interface verification, air-worthiness testing was performed on the DSTUMDS.

SECTION III

EQUIPMENT DESCRIPTION

A. EQUIPMENT CONFIGURATION AND INTERFACE. The Digital Signal Transfer Unit Multisensor Display System (DSTUMDS) consists of two line replaceable units (LRU's). Figure 1 represents these two LRU's which are; from left to right, the Indicator Control Unit (ICU) and the Radar Pilots Indicator (RPI). The RPI unit is designed to be mechanically interchangeable with the AN/APQ-99 RPI display unit. The ICU is an added unit designed to be installed in the avionics bay of the RF-4C aircraft. The mechanical design of this unit is identical to that of the F4-E DSTUMDS ICU. Electrical modifications to the RF-4C aircraft are required for installation of the two DSTUMDS units. The DSTUMDS has the capability for interface with the following sensors:

1. AN/APQ-99 Forward Looking Radar System.

2. Forward Looking Infared (FLIR).

3. AGM - 65A Guided Missle.

4. MK-1 MOD 0 Guided Weapon.

5. Paveway Weapons (with standard 525 line television format).

6. Black Crow System.
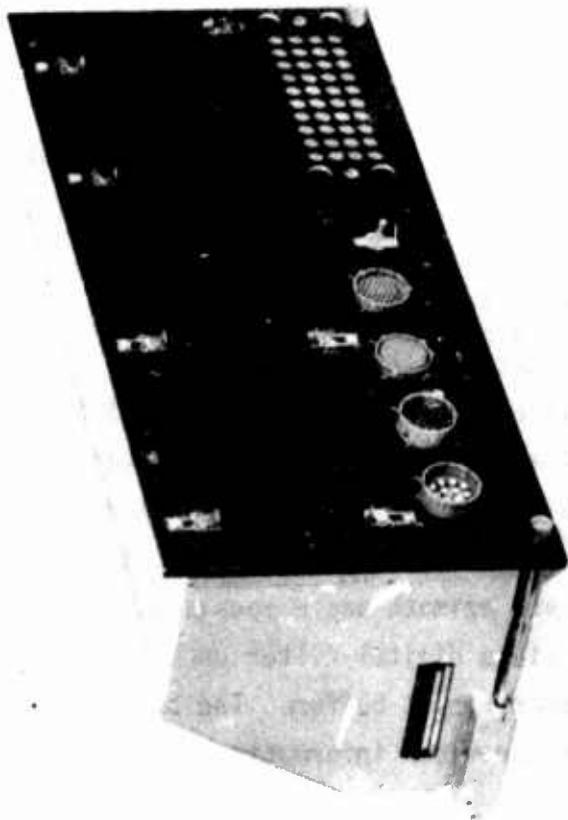
Figure 1. DSTUMDS LRU's

B DSTUMDS PRINCIPLES OF OPERATION.

1. INTRODUCTION. This section presents the basic principles of operation of the RF-4C DSTUMDS. The presentation is made at the block diagram level, progressing from a general system overview to more detailed discussions of functional blocks of circuitry. Since the RF-4C DSTUMDS is an outgrowth of the F-4E DSTUMDS, a large portion of circuitry is common between the two, including the Indicator sync separation, sweep generation, video amplification and deflection circuitry, and the ICU DSTU and low voltage power supply circuitry.

The primary advantage of the DSTUMDS over conventional display systems is its capacity to perform rate conversion of radar data. The DSTUMDS accepts radar video at a low refresh rate (the antenna scan rate), converts it to a digital format, processes it to improve the signal-to-noise ratio, stores it in a digital memory as a function of target range, azimuth (or elevation) angle and amplitude and then provides the data to the CRT display in a high-refresh raster scan format. This process allows radar information to be displayed in a non-fading flicker-free manner.

2. DSTUMDS FUNCTIONAL DESCRIPTION. The DSTUMDS performs four basic system functions:

Radar video rate conversion
Black Crow system interface
Radar interface
Data presentation

Figure 2 provides a simplified block diagram of the DSTUMDS. Radar video and antenna scan data, as well as aircraft altitude information, are provided in an analog format to the DSTUMDS where conversion is made to a digital format. The digital information generated defines the radar video in terms of video amplitude, range location and azimuth angle location. The radar amplitude information is integrated via a digital filter on a radar pulse-to-pulse basis and stored in the memory input buffer. The buffer memory capacity provides for storing all radar video information for a single azimuth angle

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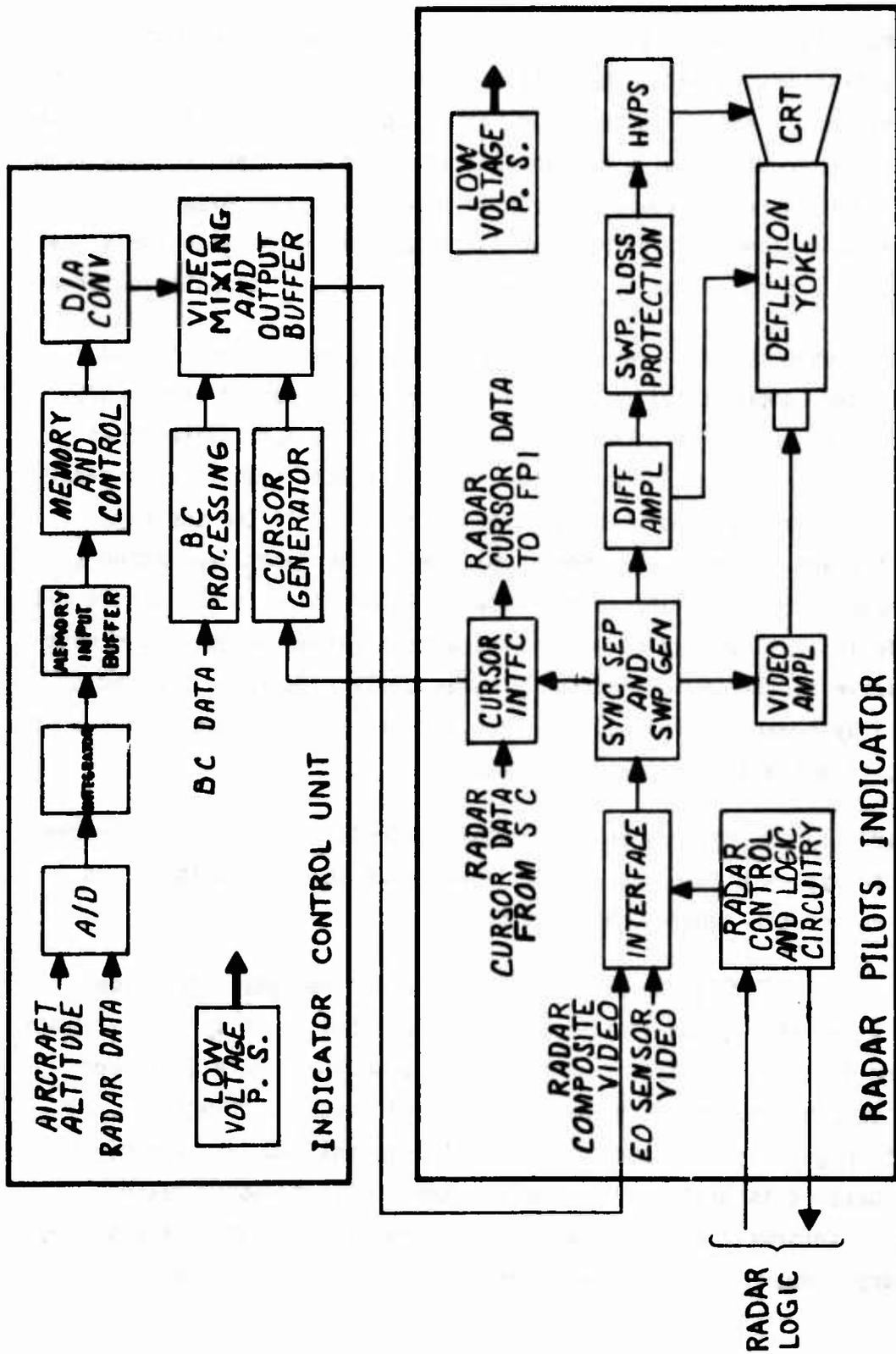
Figure 2. System Block Diagram

location. The 3-bit video is transferred from the buffer memory into the main random access memory (RAM) where it is stored in a range versus azimuth angle (θ,ρ) format. Memory update occurs as a function of antenna scan with a complete update occuring twice per antenna scan cycle. Video is read from the memory at a high rate, converted from digital-to-analog format, multiplexed with symbol video (Black Crow and Cursors) and synchronization signals, and supplied via a single wire to the display unit in a TV compatible format.

The RPI unit performs two functions: data presentation and radar interface. Radar composite video from the ICU and E.O. sensor video (875-line FLIR or 525-line TV) is accepted by the RPI. Mode logic determines which of the video inputs is to be processed. Selected video is sync-separated providing horizontal and vertical sync information to the sweep generation circuitry and video to the video amplifier. The sweep generation circuitry generates horizontal and vertical sweep information in the format dictated by mode logic. Deflection amplifiers accept raster sweeps and provide deflection drive to the CRT deflection yoke assembly. Deflection outputs are monitored by sweep loss protection circuitry to prevent tube damage which would result if deflection signals were lost.

In addition to display related panel controls, the RPI houses radar and Black Crow system control as well as radar mode logic circuitry, and radar sweep and cursor generation circuitry.

3. ICU FUNCTIONAL DESCRIPTION. The ICU accepts radar video, premaster trigger (PMT), and antenna position from the radar system as shown in the Figure 3 DSTU block diagram. PMT is used to initiate a quantizer clock which samples the incoming analog video and codes it into a digital format. This digitally coded video information is shifted into the digital integrator where it is processed to improve the signal-to-noise ratio. Antenna analog information is used by the antenna position generator to generate a binary number which represents the antenna position angle.

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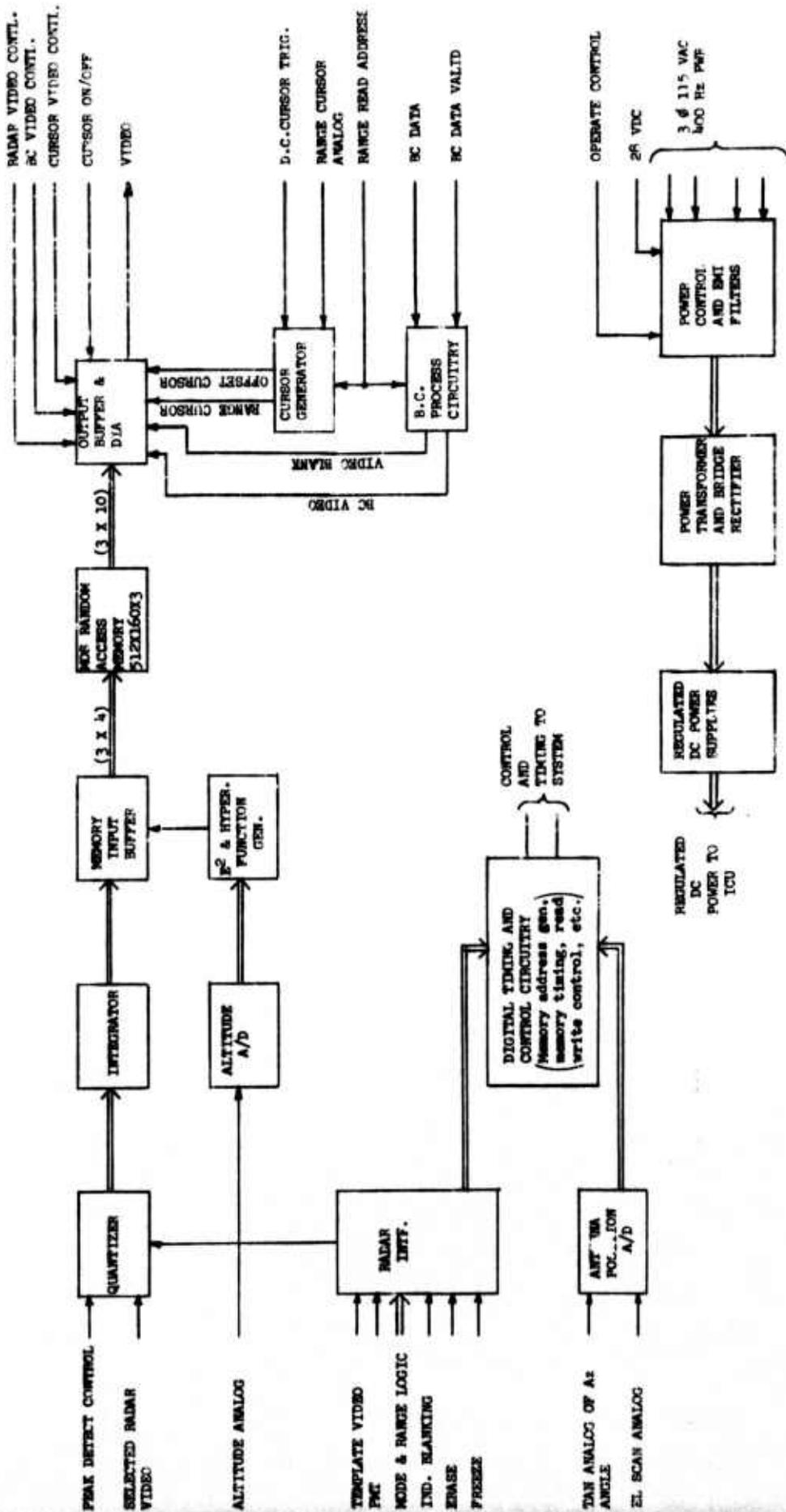
Figure 3. Functional Block Diagram, Indicator Control Unit, LRU 14

After the antenna has rotated an angle equal to one azimuth segment, the integrated video in the memory input buffer is stored in the memory as a function of range and azimuth. All timing and control signals for the video quantizer, digital integrator, and memory are generated by the timing and control circuitry.

During a read cycle, the digital video is read from the memory at constant values of range and stored in the output buffer which is part of the digital-to-analog (D/A) converter. The digital video is then shifted out of the buffer through the D/A converter to produce analog video which is used by the CRT display. The memory read address, output buffer clock, and display sync signals are generated by the timing and control circuitry. This block of circuitry also selects between the read and the write memory address and inhibits writing operations during a read cycle. The following paragraphs provide detailed discussion of each of the major circuit blocks in the ICU.

(a) VIDEO QUANTIZER. The video quantizer consists of a series of analog voltage comparators and gate logic to code the video into a binary format. These comparator threshold levels are set in a logarithmic sequence to match the radar response.

The incoming video is sampled by a high-frequency clock and then peak-detected by a slower quantizer clock. A 16.3919-MHz crystal-controlled clock is used to sample the incoming radar video. The quantizer clock is gated on with master trigger and is divided down from the basic sample clock. The quantizer clock frequency is a function of range. Since the video is displayed on 512 range lines, the quantizer clock frequency for each range is determined by the following equation:

$$f = \frac{512}{R \ (12.36 \ \mu s)}$$

where R is the selected range in nautical miles. The quantizer clock is also used to circulate data in the integrator and update data in the memory input buffer.

(b) ANALOG-TO-DIGITAL CONVERTERS. The ICU contains a total of four (4) analog-to-digital (A/D) converters in addition to the high speed video quantizer A/D previously described. These are used for A/D conversion of the following analog signals:

Altitude
Antenna Scan Position
Range Cursor
Black Crow Angle

The technique utilized in implementing each of the A/D circuits is that of dual slope integration. Figure 4 provides the block diagram of a dual slope integrator A/D converter typical of the four used in the ICU. The basic principle of operation consists of allowing an analog integrator first to integrate an unknown voltage for a known fixed period of time producing a ramp as an output, the slope and final amplitude of which is a function of the input voltage. Next, a known fixed voltage of opposite polarity is integrated until the output has reached a fixed reference voltage level. In this case the integrator output is a ramp with a constant known slope. The time required to reach the reference level is directly proportional to the unknown input voltage. A digital counter operating at a fixed clock rate is used to measure the time required to reach the output reference voltage. The counter is stopped as the voltage threshold is crossed. The counter outputs provide a parallel digital representation of the unknown analog input voltage. The contents of the counter are held and the integrator is nulled by negative feedback until the next A/D conversion cycle is initiated.

The integrator analog input switching is implemented using HA 2400 programmable linear amplifiers (PRAM's). The technique offers many advantages over more conventional methods. The integration process averages

the analog input over a period of time and hence is not as susceptible to noise on the analog input line as are other methods of A/D conversion. Since the same integrator time constant is used for both up and down integration, variations in timing component values cancel. This relaxes requirements for highly stable precision components and provides for a high degree of stability over temperature and time (component aging).

Variations in the A/D converters used occur in the areas of analog scaling, digital resolution (number of digital output bits), and cycle time as well as analog signal input format. Figure 4 depicts, in the dashed area, the additional circuitry required for converting bipolar analog signals as occur with antenna scan and Black Crow angle data. An analog comparator is used to determine signal polarity. The comparator output is used to control a PRAM so that for one input signal polarity a non-inverting amplifier is used and for the other an inverting amplifier is used allowing the PRAM output polarity to remain constant. The comparator output is also used as a sign bit for the digital word generated by the conversion process.

A/D conversion of altitude and range cursor signals is performed on the A20 and A21 assemblies. Digital altitude information is generated in a ten (10)-bit binary format. Scaling is a function of display range and is accomplished digitally. Range cursor A/D conversion produces a nine (9)-bit binary word. Scaling is a function of display range and is accomplished by scaling the analog input.

Figure 5 provides a block diagram of the antenna position generation circuitry located on the A12 assembly. Either elevation or azimuth angle information is supplied through a PRAM, depending on radar mode selection. The analog signal is A/D converted to an eight (8)-bit binary word. Azimuth information is provided as tangent θ and thus, must be converted to θ information. The A/D output is used to address a programmable read-only-memory (PROM) programmed as a tangent look-up table. The digital antenna position generated by the PROM is formatted so that the four most significant bits are binary and the four least significant bits are decade providing a range of 160.
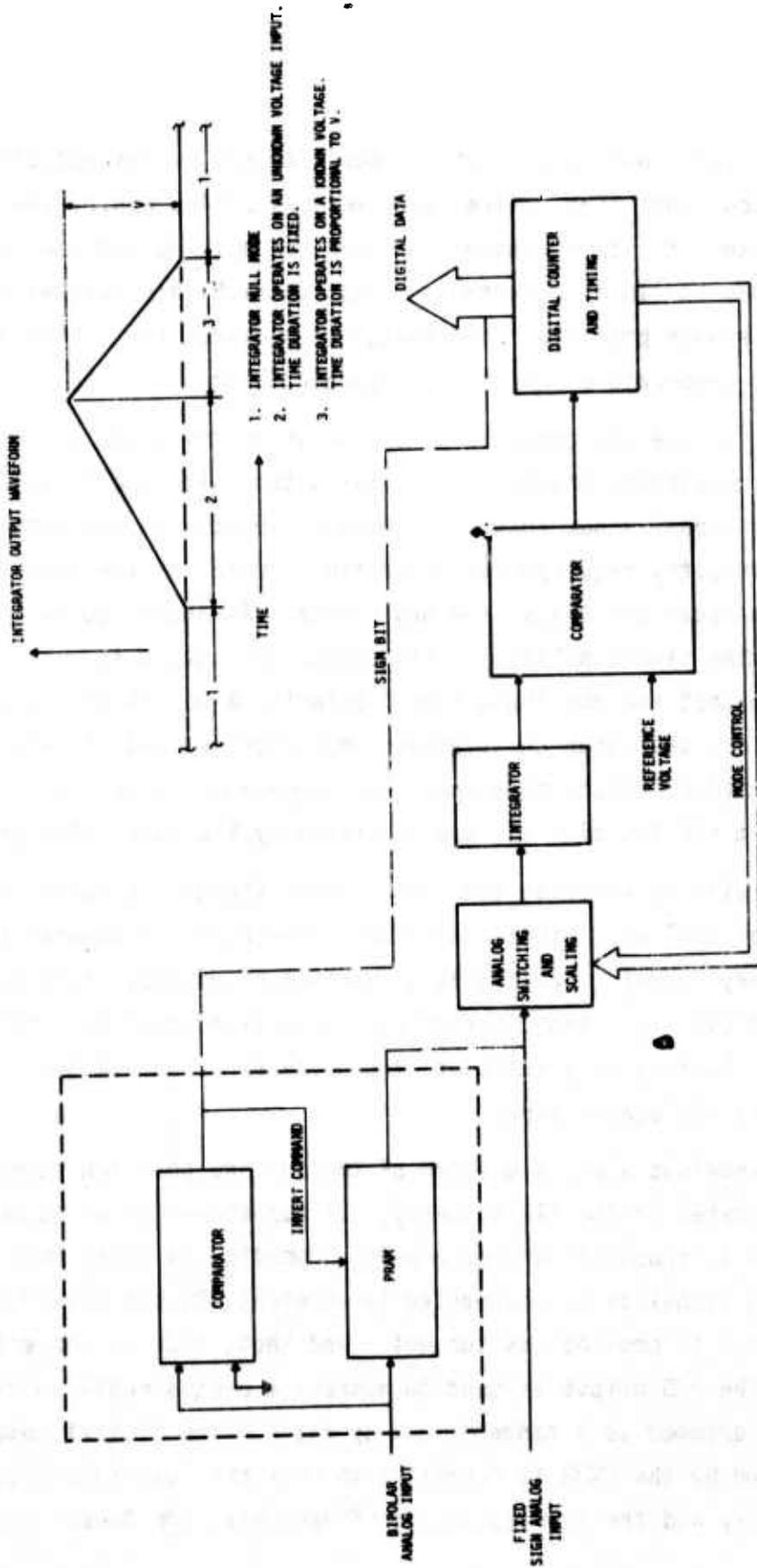
Figure 4. A/O Converter Block Diagram
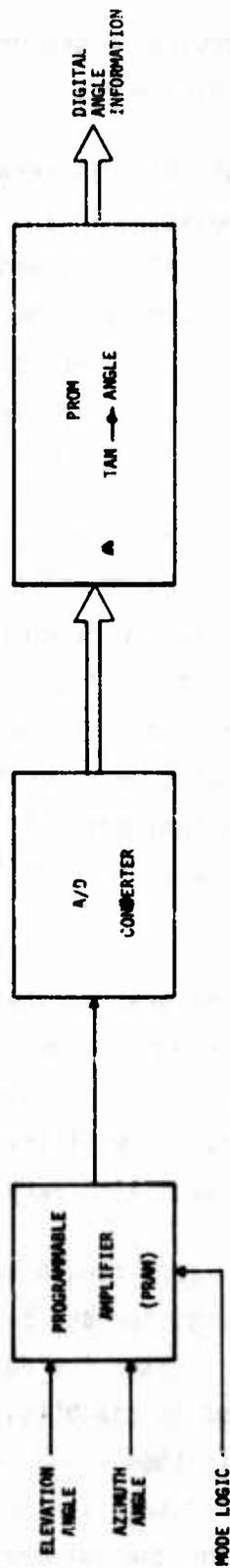
Figure 5. Block Diagram, Antenna Position Generation Circuitry

Black Crow angle A/D conversion is performed by the A27 assembly. The digital output is a six-bit binary word.

(c) DIGITAL INTEGRATOR. Integration in any radar display is required to improve signal-to-noise ratio and derive the average target return amplitude. In conventional analog systems, the inherent combination of the storage and integration processes degrade performance. In the DSTU, the integration and storage processes are separated. The incoming radar video is integrated for 1/160 of a scan by a sliding window digital integrator before the processed video is stored in the memory.

As shown in Figure 6, each radar range sweep (RRS) of digital video information from the quantizer is added to the beamwidth history which has been modified by a factor beta. This new beamwidth history is then shifted back into the integrator shift register. The feedback factor beta determines the shape of the integration curve; i.e., the number of radar range sweeps required to integrate to target amplitude saturation. By the process described, video time correlation is inherent and quantized random noise will be integrated toward zero while time coincident targets will integrate toward their respective signal amplitudes.

The value of beta affects several parameters of the integrator, including: (1) the number of radar range sweeps required to integrate a target return to its saturated level and (2) the signal-to-noise ratio. In this system, having a beta of 0.75, a return will integrate from zero to saturation in 12 radar range sweeps and exhibit a very low signal-to-noise ratio.

The digital integration is performed using three-bits of quantized video and six-bits for the shift register and beta feedback loop. Table 1 explains the integrator operation. After the data from the shift register is multiplied by beta, it is truncated to six-bits, i.e., bits with value less than 0.5 are dropped. This data is then added to the three-bits of new quantized data, and the result is stored back in the shift register. When the integrated information is taken from the integrator to be stored in the memory, it is divided by 4 and rounded up.
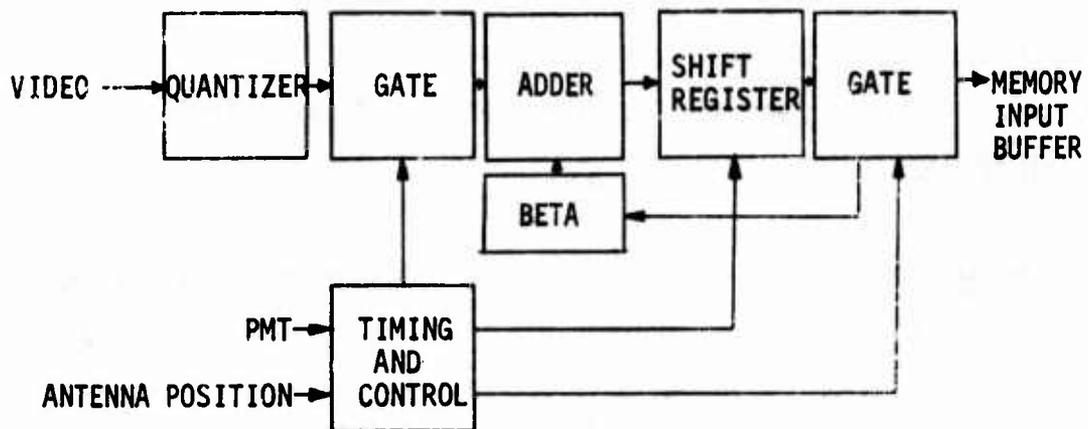
Figure 6. Digital Integrator

TABLE 1. INTEGRATOR OPERATION

Integration equation $\quad y(nt) = x(nt) + \beta y(nt - T)$

Feedback $\quad\quad\quad\quad\quad \beta = 0.75$

Target amplitude gray shade No. 8 = Binary 7 (111)

Assume truncation in the feedback loop and round up of the output.

$$Output = \frac{Integrated\ Level}{4} \quad Rounded\ up$$

Number of RRS's	Calculation	Integrated Value	Output
1	7 + 0.75 (0.0) =	7.0	2
2	7 + 0.75 (7.0) =	12.0	3
3	7 + 0.75 (12.0)=	16.0	4
4	7 + 0.75 (16.0)=	19.0	5
5	7 + 0.75 (19.0)=	21.0	5
6	7 + 0.75 (21.0)=	22.5	6
7	7 + 0.75 (22.5)=	23.5	6
8	7 + 0.75 (23.5)=	24.5	6
9	7 + 0.75 (24.5)=	25.0	6
10	7 + 0.75 (25.0)=	25.5	6
11	7 + 0.75 (25.5)=	26.0	7
12	7 + 0.75 (26.0)=	26.5	7
13	7 + 0.75 (26.5)=	26.5	7

(d) RANDOM ACCESS MEMORY. The memory capacity and organization for the DSTU is determined by many factors: range resolution, azimuth resolution, dynamic range, memory cycle time, and read/write requirements.

Memory size is primarily a function of the range resolution azimuth resolution and dynamic range. The size of the memory is 512 x 160 x 3 = 245,760 bits. The memory is constructed of 2,048 x 1-bit memory modules.

Twelve of these memory modules and associated interface circuitry have been combined on one circuit board to produce a building block which is 512 range cells high x 16 azimuth cells wide x 3 bits of intensity (eight gray shades). This building block is depicted in Figure 7. Figure 7A indicates how the 24,576 bits of the 12 modules are organized, and Figure 7B indicates how the 12 modules are physically organized. Ten of these memory building blocks are combined to provide the 512 x 160 x 3-bit memory used in the DSTU. The memory bit organization is depicted in a three-dimensional matrix as shown in Figure 8. The matrix has 512 cells in the y-direction (vertical) which represents range, 160 cells in the x-direction which represents azimuth, and 3 bits in the z-direction which represents video intensity.

Radar video is received in a rho/theta format (i.e., the antenna position is the theta angle and the time following master trigger relates to the rho). With the cited organization, it becomes an easy task to store the data in a rho/theta organization. Data will be written into the memory by filling one azimuth bin at a time (i.e., one azimuth bin is 512 range cells high, one azimuth cell wide, and 3 bits deep). The write azimuth address is generated from the antenna position.

512 BITS
RANGE

16 BITS
AZIMUTH

3 BITS
INTENSITY
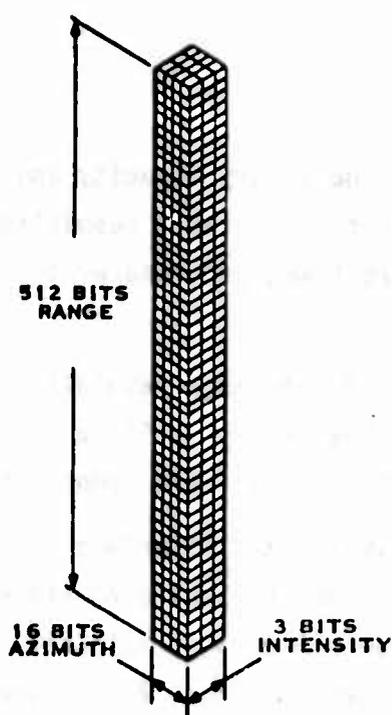
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(A) MEMORY BIT ORGANIZATION

4 MODULES

3 MODULES

1 MODULE
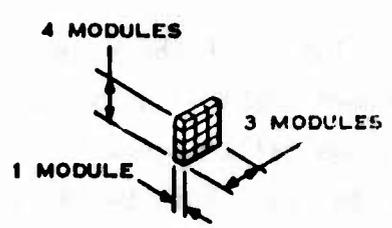
(B) MEMORY PHYSICAL CONFIGURATION

Figure 7. Memory Building Block

512
RANGE
CELLS

WRITE

160
AZIMUTH CELLS

READ

3 BITS
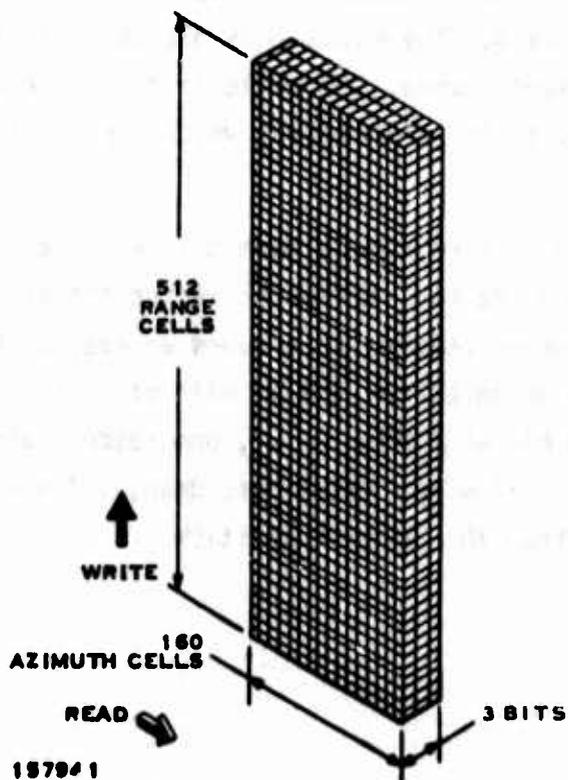
157941

Figure 8. Memory Bit Organization

20

The write range address is generated from a counter which is clocked as the data is shifted out of the digital integrator. The stored radar data is read from the memory in the range direction in a TV-like scan to form a read format consisting of two fixed interlaced fields of horizontal range lines. No coordinate conversion is made. One frame of read data (total matrix) contains radar video organized to rho/theta coordinates. In the case of PPI scan, the rho/theta format is converted to PPI by generation of spiral raster in the Indicator LRU. For depressed center PPI, the raster consists of 512 concentric 90 degree arcs where each arc corresponds to one range line of 160 azimuth bins. In E^2 formats, the spiral scan raster is inhibited and data is displayed as a 512 x 160 X-Y raster.

Since the memory is constructed of 120 memory modules, each containing 2,048 bits of storage, it is convenient to physically think of the memory as a three-dimensional matrix which is 10 wide by 4 high by 3 deep, as shown in Figure 9. Each cell of this matrix represents one 2,048-bit memory module. Input data is provided to the memory on 12 input lines (4 range cells high by 3 bits deep); each line is connected to the 10 memory modules (one row). Part of the write azimuth address is used to select one of the 10 columns. During a write cycle, data is written into the four range cells (12 bits) of the selected column. During a read cycle, one of the four rows of memory matrix is selected by part of the read range address. All 10 of the columns in that row are read to provide a 30-bit output word (10 columns by 3 bits deep). This 30-bit output word is then stored in a buffer which is a part of the output digital-to-analog (D/A) converter.

12 Bit
Input
(3 x 4)
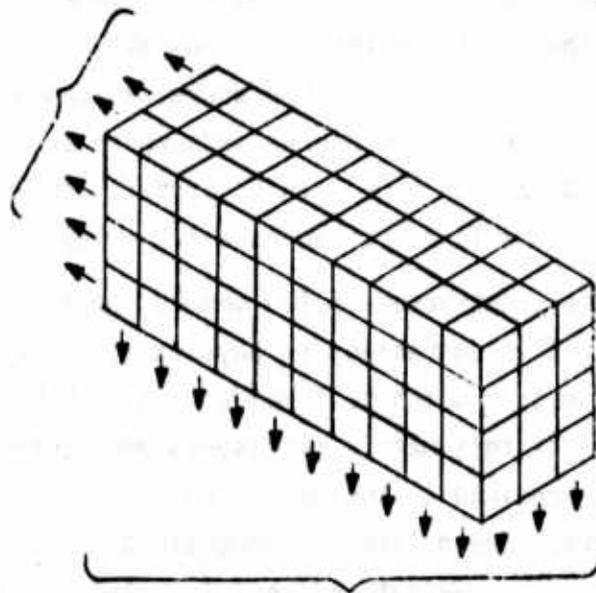
30 Bits (3 x 10)
Output

Figure 9. Physical Memory

(e) TIMING AND CONTROL. The timing and control circuitry for the DSTU is separated into two parts; reading timing and control, and write timing and control. Although both of these circuits share a common 16.3919 MHz clock, each circuit operates relatively independent of the other and thus is discussed separately.

The function of the read timing and control circuitry is to control the memory operation and generate signals needed by the output buffer to generate video, and by the Indicator LRU to display that video.

In the PPI mode, the Indicator will generate a rho/theta raster consisting of 512 concentric 90-degree arcs. Each arc corresponds to one range bin in the memory. In the E^2 mode, the Indicator will generate a 512-line raster similar to a TV raster rotated 90 degrees. In either mode, the DSTU operation is the same. To generate these rasters, the indicator requires horizontal and vertical sync signals. These signals are generated by the read timing and control generator and are incorporated into the composite video signal. The active horizontal time is 48.9 µsec, and 12.2 µsec is allowed for horizontal retrace. The total is 61.1 µsec. Since 256 range lines will be displayed in each active vertical field, the active vertical time will be 15,641.6 µsec. The vertical retrace time is different for odd fields than for even fields to maintain a positive 2:1 interlace between fields. For odd fields, the retrace is 580.5 µsec, but for even fields the vertical retrace is 611 µsec. This computes to an average field rate of 61.5 Hz.

Digital counters clocked by the master 16.3919 MHz clock are used to generate the output buffer clock and control signals, and the memory timing signals. These counters are also used to generate memory read addresses. Horizontal and vertical sync signals are generated by decoding these counters. The read timing and control circuitry accepts write addresses and a write enable signal from the write timing and control circuitry. When the memory is not being read and the write enable signal is present, the read timing and control circuitry will generate the timing and control signals

required to store the data (which is on the input lines to the memory) in the memory at a location determined by the write address.

The write timing and control circuitry, using inputs of mode and range logic generates the required quantizer/integrator clock signals. This is accomplished using a 16.3919 MHz crystal-controlled clock to drive a digital counter. The counter is controlled by a master trigger (PMT) (i.e., it starts counting when the PMT pulse is received). One of the outputs of the counter is selected by the range and mode logic. Another counter controls the quantizer/integrator clock pulses and will stop the quantizer clock after it has clocked 512 times.

Digital antenna position is used as part of the memory address. Basic timing clock signals from the read timing and control circuitry and the write cycle complete signal are used to generate clock signals used to shift data from the integrator. In conjunction with these signals, the write enable control signal is generated.

An unload control signal is generated using the output of the antenna position analog-to-digital converter. When the antenna has rotated an angle of 0.5625 degree (one azimuth cell), the least significant bit of the azimuth theta will change and an unload signal will be generated to transfer the integrated data from the memory input buffer into the memory. The memory input buffer is unloaded to the memory in a linear fashion in slant ground range PPI modes of operation because the radar video has been quantized and integrated in terms of radar slant range. TF and true ground range PPI modes of operation require range manipulation of radar video between the integrator and the memory. The digital E^2 and ground range correction circuitry functions with the memory input buffer to perform this function.

(f) DIGITAL E^2 AND HYPERBOLIC GROUND RANGE CORRECTION CIR-TRY. Radar information is quantized, integrated, and stored in the memory input buffer in equal range increments. Thus, the range information contained in the memory input buffer is linear radar slant range. In radar modes of operation where the display format requires slant range, the memory input buffer is unloaded in a linear fashion into memory so that integrator range bins directly correspond to memory range cells. In E^2 and ground range corrected modes, however, the relationship between integrator range bins and memory range cells is not a linear one. The purpose of the E^2 and hyperbolic ground correction circuitry (shown in block diagram form in Figure 10) is to generate the appropriate non-linear relationship between integrator range bins and memory range cells.

In the ground range corrected modes of operation, the slant range information stored in the memory input buffer must be converted to true ground range prior to storage in memory. As indicated in Figure 10, the problem solution is a hyperbolic equation: $R^2 = G^2 - A^2$

$$\text{where: } R = \text{slant range}$$
$$G = \text{true ground range}$$
$$A = \text{altitude}$$

The solution is implemented using a digital differential analyzer (DDA) to generate hyperbolic sine (SINH) and hyperbolic cosine (COSH) functions. Initial conditions are loaded into the SINH and COSH counters so that prior to beginning the memory input buffer unload cycle, altitude is loaded into the COSH counter and zero is loaded in the SINH counter. When the unload cycle begins, the COSH counter contents are repeatedly summed with the COSH register contents. The same scheme is used with the SINH register. Initially the SINH register and counter contents are both zero so that the register remains at zero. After several cycles (the exact number depending on altitude), the COSH adder overflows allowing the SINH counter to advance one count. The process continues until the SINH counter overflows.

SINH overflows (CHE) are used to advance information from the buffer register through a digital peak detector (peak detection

function required only in E^2) and to the serial to parallel register used to load the memory. COSH overflows (SHE) are used to generate the memory write range addresses.

Large altitude inputs may cause a double overflow at the COSH adder. When this happens the SINH counter is incremented one count and the SINH register is inhibited for one computation. In the ground range correction mode of operation, COSH overflows initially occur more frequently than do SINH overflows. This causes information in one integrator range bin to be loaded at several memory range locations, effectively stretching or expanding the slant range information. As range increases the COSH and SINH overflow rates approach, producing a linear relationship between slant and ground range.

The initial altitude delay correction is made by delaying the operation of the video quantizer each radar PMT as a function of altitude. Zero altitude indicates a linear one-to-one relationship between slant and ground range. In this case, the COSH and SINH functions are overriden and the counters allowed to count at a fixed rate.

In the TF radar mode of operation, range information must be transformed from a linear slant range format to an exponential function of the $1 - e^{-\frac{x}{a}}$. This is implemented using the SINH register and counter shown in Figure 10. In the TF mode, the SINH counter is initially loaded to capacity (all ones). The SINH adder overflows are used to decrement the SINH counter producing the $e^{-\frac{x}{a}}$ function. The contents of the memory input buffer are advanced at a constant rate (C2/7) to the memory serial to parallel input register. SINH overflows are used to generate memory write addresses. To convert $e^{-\frac{x}{a}}$ to the desired $1 - e^{-\frac{x}{a}}$ form, the following rationale is used:

$$1 - A \simeq \overline{A}$$

where: equation is Boolean

A is small number

$\overline{A}$ is compliment of A

Hence, $1 - e^{-\frac{x}{a}} \simeq e^{-\frac{x}{a}}$
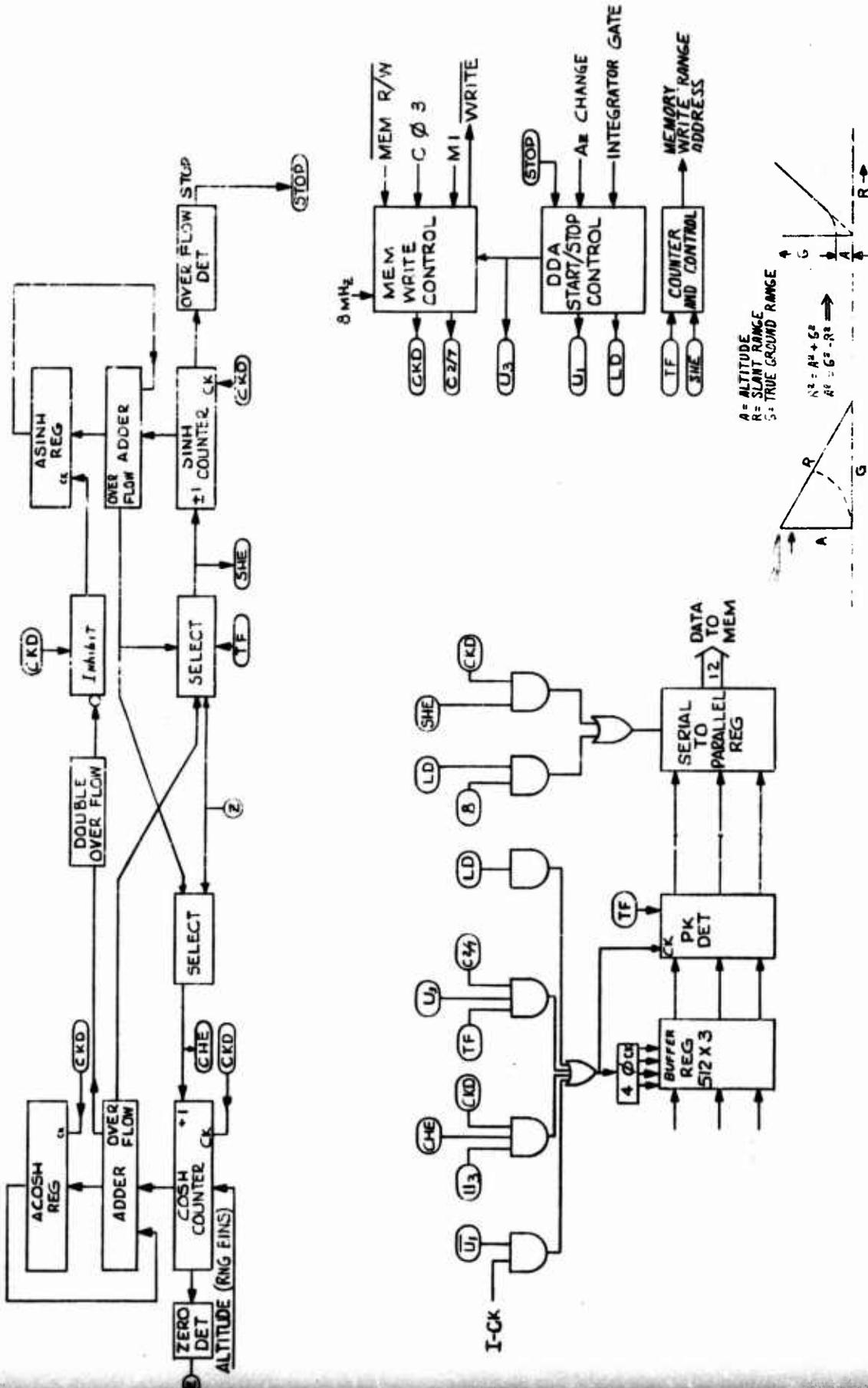
Figure 10. Hyperbolic Ground Range and E^2 Correction Circuitry Block Diagram

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This rationale is implemented by initially loading the
memory write range address counter to all ones and using SINH overflows to
decrement the counter. The compliment of the counter contents is used as the
memory write range address.

As the DDA operates in the E^2 mode, initial integrator
range bins are loaded into several memory range cells effectively stretching
the slant range information. As range increases the overflow rate (SHE)
and the fixed memeory input buffer clock rate (C2/7) approach, creating a
linear relationship. At far ranges, the (C2/7) clock rate exceeds the over-
flow rate causing compression of the slant range information. The digital
peak detector is used to select the video of highest amplitude for loading
into memory when several integrator range bins must be loaded into one memory
cell.

(g) BLACK CROW INTERFACE, PROCESSING, AND SYMBOL GENERATION. A significant part of the DSTUMDS design effort was that of developing circuitry to interface with the Black Crow System so that Black Crow information could be displayed in a systematic fashion simultaneously with radar map display presentations. Rather than develop a separate special control panel for Black Crow, Black Crow controls were incorporated in the DSTUMDS RPI design. Figure 11 defines complete signal flow for Black Crow system interface. 28 VDC is supplied by the BC system to the BC THRESHOLD/OFF control on the DSTUMDS RPI. When the control is rotated from the full counterclockwise position, 28 VDC is switched to provide a 28 VDC BC ON discrete which is supplied to the BC system, to the BC processing circuitry in the DSTUMDS ICU and to the BC annunciator on the RPI edgelit panel. This discrete allows the BC system to operate and enables the BC processing circuitry in the ICU. The BC THRESHOLD control is used to vary the BC receiver threshold for noise suppression and signal discrimination. The BC SAMPLE control is used to vary the sampling period of the processing circuitry in the ICU.

Black Crow signal processing and symbol generation circuitry is contained on the A27, A28 and A29 assemblies in the DSTUMDS ICU. Figure 12 provides a detailed functional block diagram of this circuitry and should be used as a reference for the theory of circuit operation which follows.

Two signals, BC DATA and BC DATA VALID, are supplied by the Black Crow system to the ICU for BC signal processing and symbol generation. The BC DATA signal contains target location information in terms of azimuth angle. The signal is analog in nature with the voltage polarity defining the sign of the angle and voltage amplitude indicating the angle magnitude. BC DATA VALID is a series of fixed amplitude, fixed width pulses. The pulse repetition rate is somewhat random in nature depending on BC target emmission rates, number of targets, and BC threshold setting. The presence of a BC DATA VALID pulse indicates that a target has been detected and that its location is indicated on the BC DATA signal
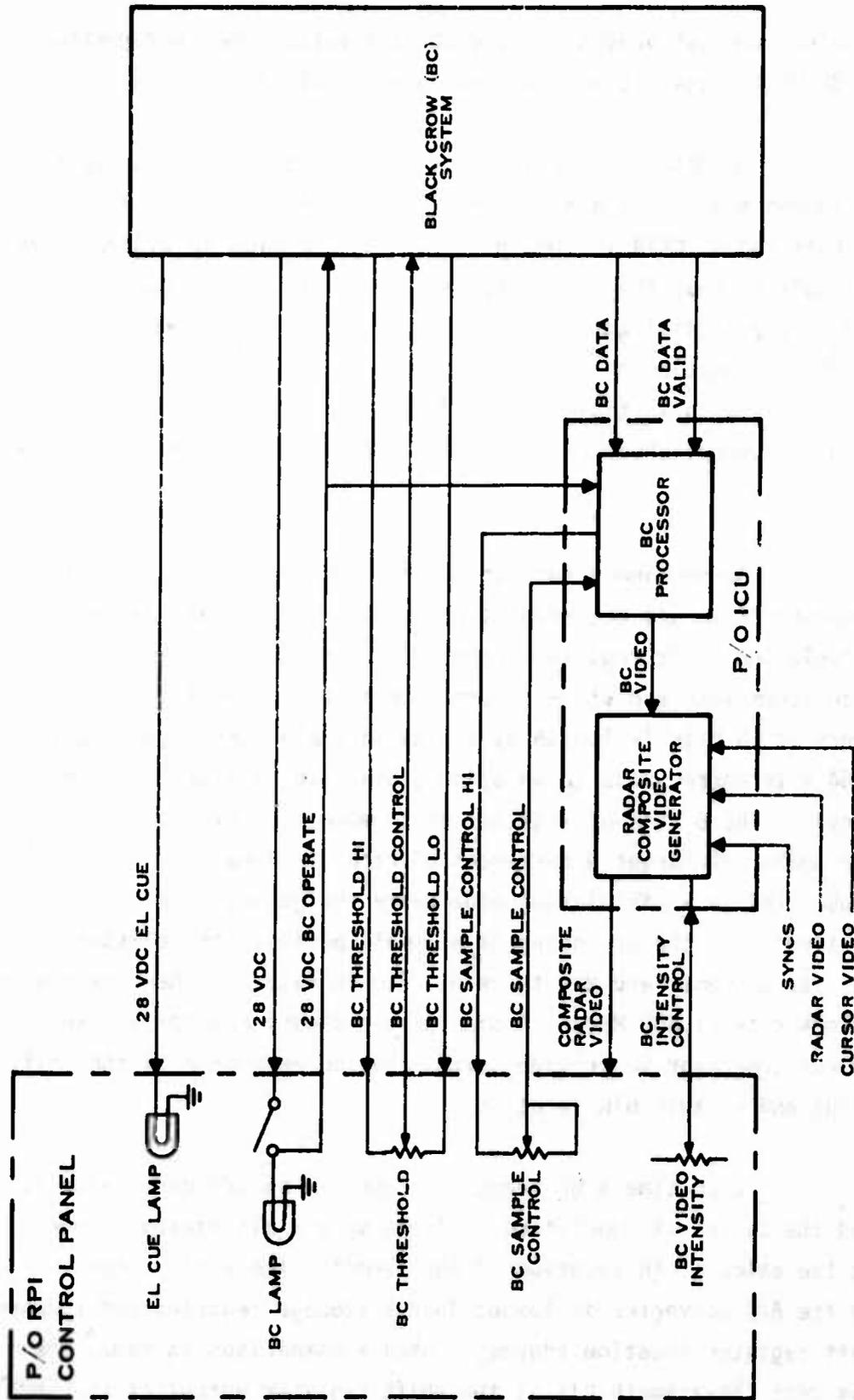
Figure 11. Black Crow System Interface

line. When pulses are not present on the BC DATA valid line, information contained in BC DATA signal is invalid and is disregarded.

BC DATA is supplied to a common mode rejection amplifier to eliminate common mode noise and to reference the signal to the ICU signal ground. The buffered BC DATA is then provided to an analog to digital (A/D) conversion circuit so that the analog target angle information can be transformed into a binary digital word six (6) bits in length. The word defines display azimuth bin location of the BC Target. The BC DATA VALID signal is level shifted and used to initiate an A/D conversion of BC DATA so that an A/D conversion is accomplished for each DATA VALID pulse and hence for each BC target.

As mentioned earlier, BC information is displayed in terms of frequency of target occurrences per unit time per unit azimuth angle. A circulating shift register memory (BC DATA ACCUMULATOR in Figure 12) is used to accumulate and store information in this format. The shift register memory is 64 bits in length by 6 bits in depth (see Figure 13). Each of the 64 bits corresponds to an azimuth bin, i.e. a discrete segment of azimuth angle. The 6 bits of register depth make up a binary number which indicates the number of target occurrences at each bin location. The shift register is operated in a circulating mode where the output data is fed into the register input. At the beginning of a sample period, the register is cleared, i.e. its contents are set to zero. The register is then circulated at a fixed clock rate (1.639 MHz). A six (6) bit binary counter is used as a memory address generator to provide correlation between data at the shift register output and azimuth bin location.

Each time a BC target is detected an A/D conversion is performed and the target is identified in terms of a 6 bit binary number representing the azimuth bin location of the target. The 6 bit number generated by the A/D converter is loaded into a storage register and compared with the shift register location address. When a comparison is made, the indication is that the azimuth bin at the shift register output corresponds

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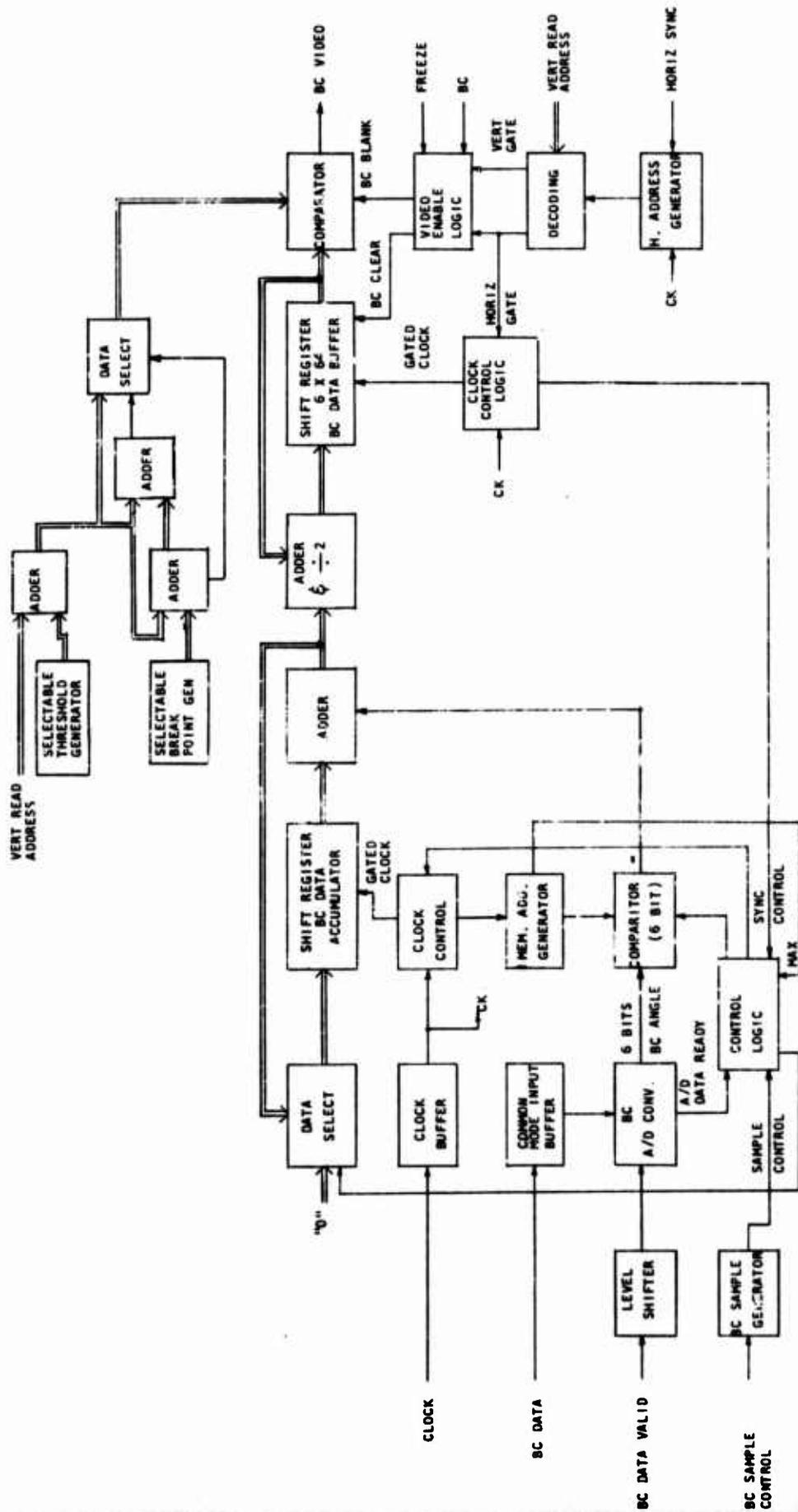
Figure 12. Functional Block Diagram BC Processing Circuitry RF-4C DSC

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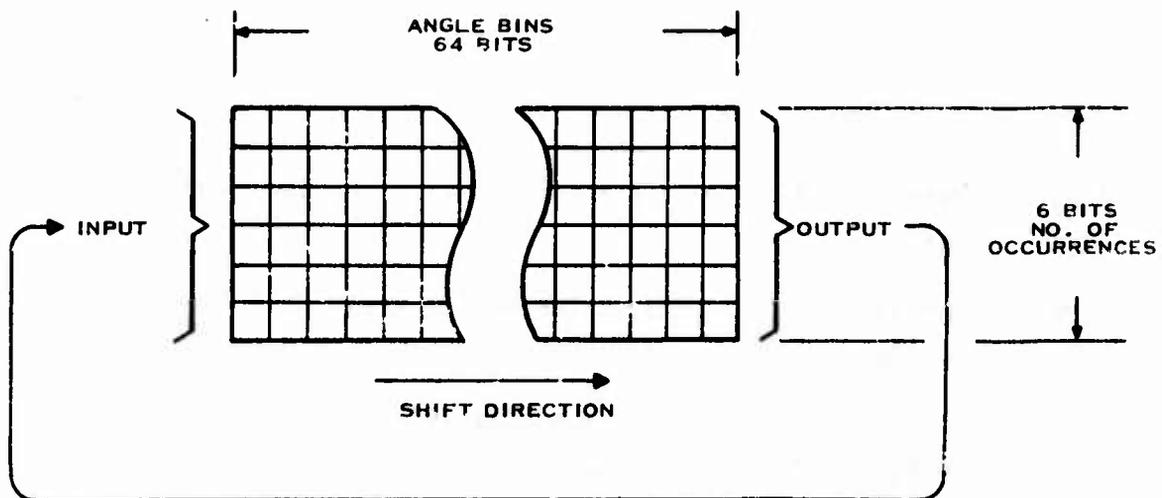
Figure 13. BC Shift Register Memory Organization

to the location of the target just detected. Thus, the number located in
the azimuth bin is increased by one via a binary adder and the resultant
number is fed back into the shift register input. The shift register cycle
time is significantly less than the A/D conversion cycle time to insure that
each detected target is stored in the fashion described above. At the end
of the sampling period, the accumulator register is stopped, synchronized
with an identical register (hereafter referred to as the BC data buffer
register), and its contents transferred to the second register through a
circuit which integrates data already stored in the buffer register with
the incomming data according to the equation:

$$y(n) = \frac{X(n) + y(n-1)}{2} .$$

where:

X(n)	represents data being transferred from the accumulator register.
y(n-1)	represents data stored in the buffer register prior to transfer.
y(n)	represents the output of the integrating circuit and hence, the data being loaded into the buffer register.

The integrator serves to smooth or average transitions in data which occur
between sample periods.

The BC data buffer register is synchronized with the main
RAM memory read timing, and thus with the composite video, so that the BC in-
formation may be converted to video and mixed with radar video and
cursor video. Proper placement of the symbology on the RPI display is
accomplished by decoding circuitry which uses horizontal and vertical RAM
read addresses to generate a symbology window. The window allows for
displaying BC symbology and inhibiting radar and cursor video in the Black
Crow Symbology Band (see Section III-E).

(h) CURSOR GENERATION. Two separate techniques are employed in generating radar cursor information. Figure 14 provides a block diagram of the circuitry used to generate offset and range cursors.

Generation of the range cursor is very straightforward. Range cursor analog DC information is supplied to the A21 assembly where it is filtered and scaled as a function of display range. The scaled analog range cursor signal is A/D converted to produce an 8-bit digital word. The A/D conversion circuitry is synchronized with memory read timing so that a comparison of vertical read address and digital range cursor information results in an indication of the required location of the range cursor in terms of vertical read address. Video is generated for an entire horizontal period. Range cursor video is generated to each raster field, resulting in a range cursor which is the equivalent of two range bins thick.

Offset cursor generation begins in the RPI on the 15A6 assembly. Two input information lines are required. The Horizontal Offset Cursor is a pulse having amplitude directly proportional to cursor horizontal offset and polarity which indicates offset direction from ground track. The Cursor Clamp Gate is used as a synchrnoization signal for the horizontal offset cursor. As indicated in Figure 14, the Horizontal Offset Cursor is provided to the A6 assembly in the RPI where it is common mode rejected and supplied to a DC clamp circuit. The Cursor Gate is provided through a level shifter to actuate the clamp circuit which is provided for clamping the Horizontal Offset Cursor baseline to a DC level near ground and eliminate errors which would occur due to baseline offset of Horizontal Offset Cursor. The Clamp Gate is also provided to initiate a one-shot circuit providing a fixed width pulse, the trailing edge of which is used to trigger still another one-shot. The initial one-shot is used to provide delay from the leading edge of the Cursor Gate (which slightly precedes the Horizontal Offset Cursor pulse). This allows the Horizontal Offset Cursor pulse to stabilize prior to the time the second one-shot initiates a sample hold operation. The output of the sample hold circuit is a DC signal (with some high frequency components resulting from sample switching) representing

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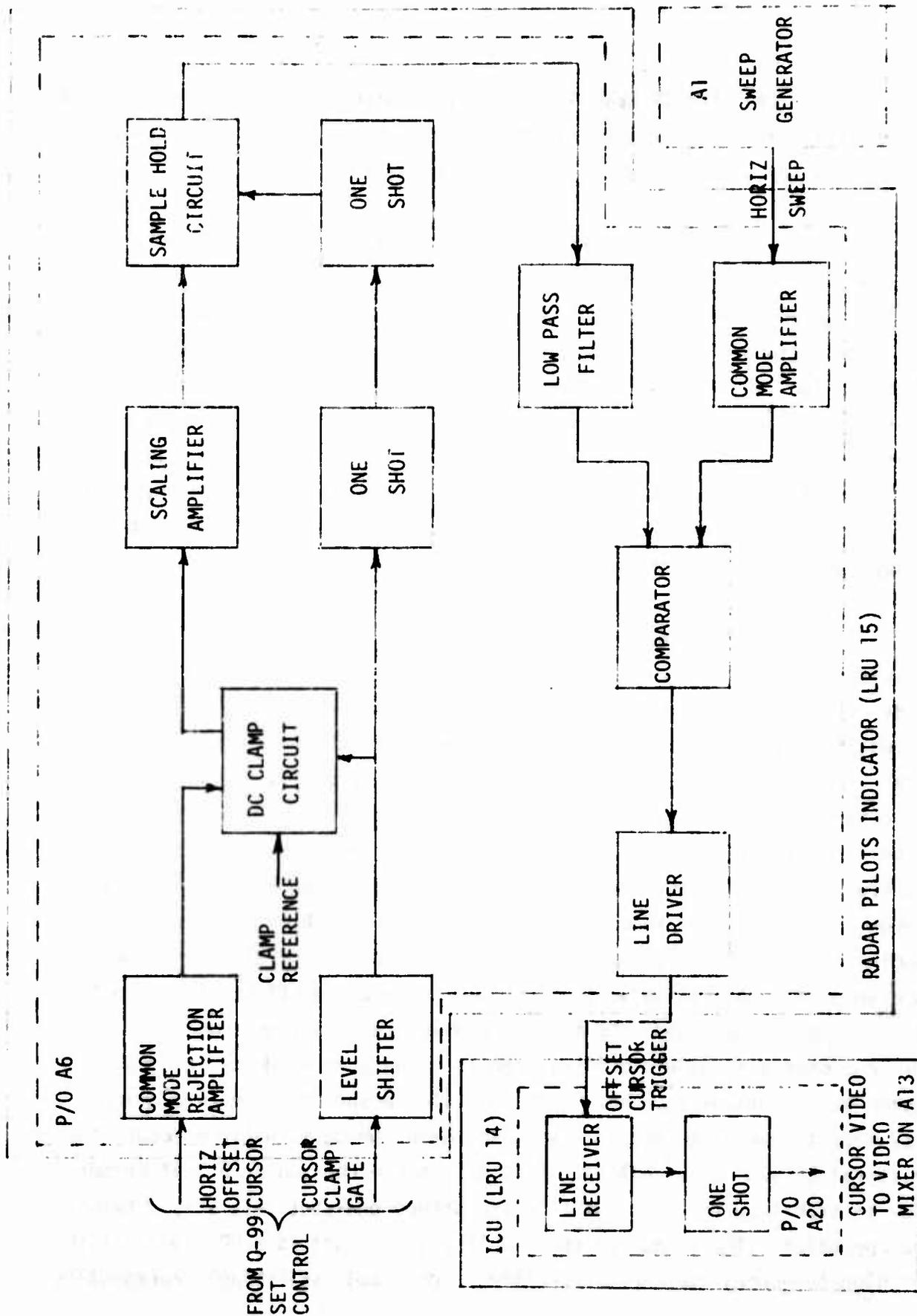
Figure 14. Block Diagram, Horizontal Offset Cursor

the amplitude of the Horizontal Offset Cursor pulse. This signal is filtered to remove AC frequency components and supplied to an analog comparator where it is compared with the raster Horizontal Sweep Signal. The comparator output is supplied through a line driver to the ICU A20 assembly where it is line received and used to trigger a one-shot circuit. The output of the one shot is supplied as offset cursor video to the video mixer where it becomes a part of composite radar video and is returned to the RPI unit and displayed. The time delay involved from analog voltage comparison on the 15A6 assembly to the presentation of the resultant video on the display is quite short, resulting only from component propagation delays. The basic concept employed in generating the offset cursor in this manner is based on the fact that the line created by the offset cursor is essentially a constant horizontal sweep voltage line. Thus, displaying a video pulse generated at a constant horizontal sweep amplitude each horizontal period results in a vertical series of raster dots comprising a vertical line. Implementing the offset cursor in this manner (in-raster) provides for video recording the cursor information.

(i) VIDEO DIGITAL-TO-ANALOG CONVERTER. The video digital-to-analog (D/A) converter accepts the 3-bit coded video read from the memory and converts it to a useable analog signal for display. To ensure that the eight levels stored are visible as distinct shades of gray, the 3-bit code is converted to an eight-level 8-bit code with each step approximately equal to 1.4 times the preceding step, as shown in Table 2.

TABLE 2. QUANTIZER LEVEL CONVERSION

Input Level		Output Level	
1	000	00	00000000
2	001	23	00010111
3	010	32	00100000
4	011	45	00101101
5	100	64	01000000
6	110	91	01011011
7	101	128	10000000
8	111	181	10110101

These outputs drive a simple 1R-2R ladder with a reference generator used for range compensation of the video in the PPI mode of operation. The D/A reference starts at a nominal voltage at the start of each field and linearly ramps up as the range arcs get progressively larger. This compensates for the increasing writing speed of the CRT trace and provides equal intensity from the bottom to the top of the display. When a symbol is being written, the output of the D/A ladder is clamped to the symbol video voltage level. Symbol intensity may be varied from black to a level approximately two gray shades brighter than maximum radar video.

During TF operation video compensation is not required and the D/A reference is maintained at a constant DC level.

A composite sync signal containing both horizontal and vertical sync information is used to clamp the video to a negative level (approximately one volt negative). The resultant is a TV compatible composite video signal containing radar video, symbol video, and sync information which is buffered by a unity gain video amplifier and routed to the RPI.

(j) REGULATED DC POWER SUPPLIES. The ICU utilizes six (6) regulated DC power supply voltages:

+5 VDC
+8 VDC
+15 VDC
-6 VDC
-12 VDC
-15 VDC

Each of the six power supplies utilize the same basic series-pass design. The regulator design is implemented using integrated circuit voltage regulators which provide a high degree of regulation and stability over temperature. Current foldback short circuit protection is provided to insure high speed overload control and to reduce the series-pass regulator transistor power dissipation under short circuit stress.

Power for the supplies is derived from a single three-phase power transformer having six (6) separate three-phase secondary windings. The 11A30 heat sink assembly contains a three-phase full wave bridge rectifier for each of the six outputs. The unregulated DC voltage from the full-wave rectifier is provided to series-pass power transistors on the heat sink assembly and to the regulation circuitry contained on the A24 and A25 assemblies. The A24 and A25 assemblies provide regulated voltage drive to the emitter follower series-pass transistors which in turn provide regulated DC voltage to the ICU circuitry.

4. INDICATOR LRU FUNCTIONAL DESCRIPTION. Figure 15 provides a functional block diagram of the Radar Pilot's Indicator. In addition to the CRT display related circuitry, the RPI contains radar mode and range logic, forward indicator sweep generation circuitry, offset cursor generation circuitry and low voltage supply circuitry.

(a) CRT DISPLAY CIRCUITRY. Radar composite video from the ICU sensor video from the aircraft are supplied to the Interface (A4) assembly. Sensor select mode logic from the aircraft selects one of the video lines and supplies it to the Sync Separator (A1) assembly. The selected video is also buffered on the A4 board by a high frequency video driver circuit and supplied to the aircraft as recorder video. In addition to sensor select mode logic, 28V radar mode logic is provided to the A4 board where it is level shifted to TTL levels used to generate raster sweep select mode logic.

The A4 board also contains a time delay circuit used to provide a 60 second high voltage turn on delay to allow CRT warm up.

Selected video is processed by the Sync Separator assembly to separate horizontal and vertical sync signals from the composite video. Sync signals are provided to the blanking circuitry on the A3 board and to sweep generation circuitry on the A2 board.

The A2 assembly generates sweeps for TV, E^2, or PPI raster as determined by the sweep select mode logic. In TV and E^2 modes the horizontal and vertical sweeps are linear ramps. In the PPI mode of operation the horizontal and vertical sweeps are sine and cosine wave forms. The sine/cosine relationship provides for generating the concentric circular arcs which make up the PPI raster. A linear differential analyzer (LDA) is used to generate the sine/cosine function. The LDA is comprised of two integrators and an inverting amplifier. The output of one integrator is a cosine function which is inverted and supplied as a negative cosine wave form to the second integrator resulting in the generation of a negative sine waveform. The negative sine function is provided as an input to the first integrator to produce a cosine function. Both integrators are preset each horizontal period to establish initial conditions. In order to get larger and larger arcs, the amplitude must be increased linearly as the vertical sweep progress upward in amplitude. This function is used to establish initial conditions each horizontal period.

The Sweep Generator Assembly provides horizontal and vertical deflection inputs to the deflection amplifier tray assemblies A10 and A11. The A10 and A11 assemblies are identical and provide drive for the deflection yoke. The yoke drive current flows through a one ohm current sense resistor. The voltage developed across the resistor is used as feedback for the amplifier.

The A3 assembly contains the video amplifier and video blanking circuitry. Video is provided to the assembly via the CONTRAST control. The video is amplified and provided to the CRT. Synchronization signals are used to generate CRT unblanking. CRT protection circuitry on the A3 board provides for blanking CRT during display mode changes and upon loss of sync signals.

The A8 and A9 assemblies provide plus and minus 20 VDC power to the other indicator subassemblies. The supplies have a modular tray form factor and are interchangeable. The assemblies are of the same basic design as the ICU low voltage power supplies.
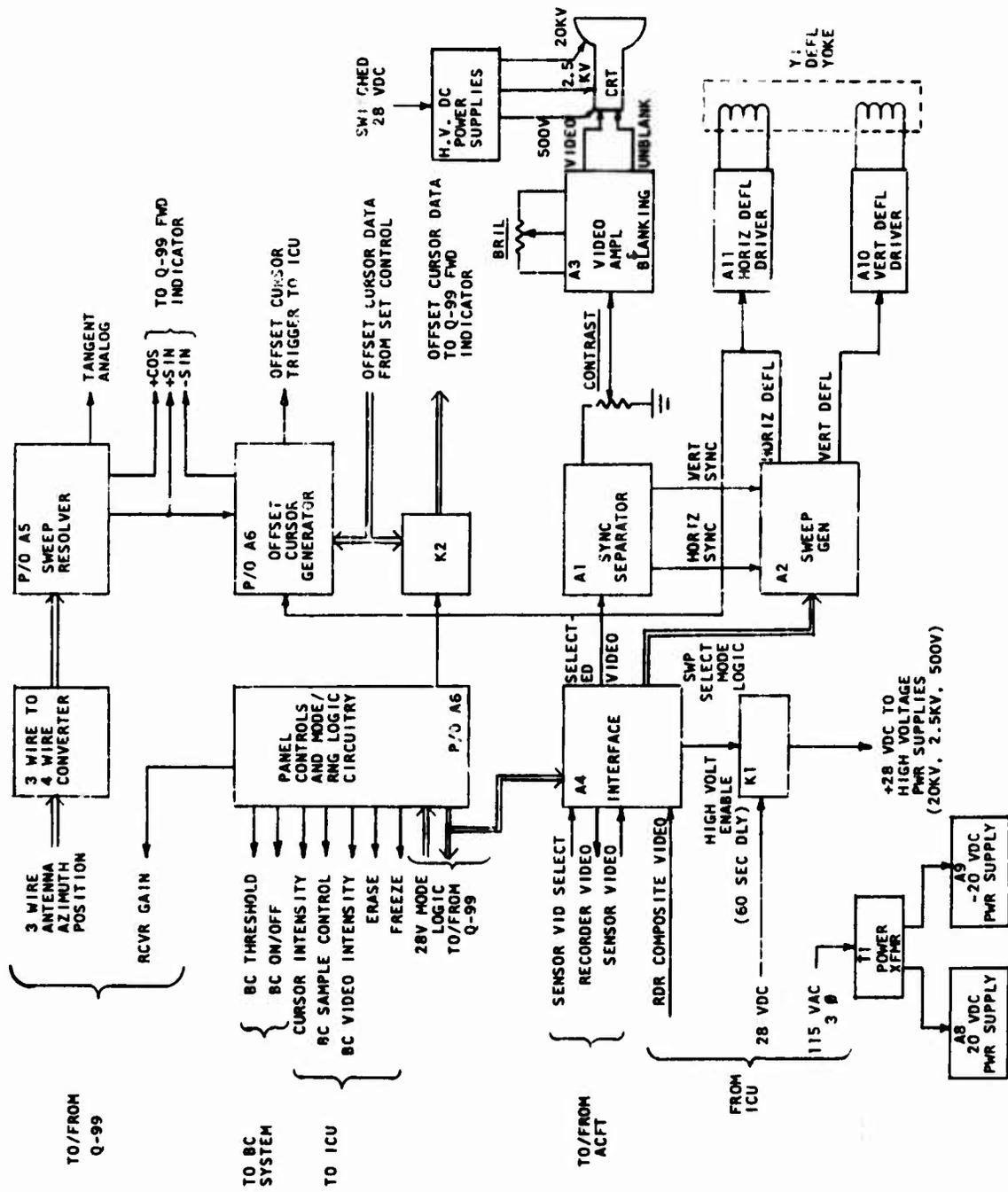
Figure 15. Functional Block Diagram Radar Pilots Indicator, LRU 15

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(b) RADAR MODE AND RANGE LOGIC. The radar mode and range logic circuitry contained in the RPI performs the same logic and control functions performed in the AN/APQ-99 RPI. Main functions include radar system mode and range control and power distribution control. Mode logic circuitry is contained on the A6 assembly.

(c) OFFSET CURSOR GENERATION CIRCUITRY. Offset cursor generation circuitry is contained on the A6 assembly. The operation of this circuitry was discussed with the ICU cursor generation circuitry. Since the RPI displays cursors in all Radar PPI display modes of operation and the Forward Indicator does not, cursor data from the set control unit is routed through a relay in the RPI to the Forward Indicator. In PPI modes of operation in which cursors are not displayed on the Forward Indicator, mode logic causes the relay to interrupt the cursor signals.

(d) FORWARD INDICATOR SWEEP GENERATION CIRCUITRY. Three wire 400 Hz antenna azimuth position information is provided from the radar antenna to the RPI. In the RPI the information is converted from three wire data to four wire sine-cosine information. The sine-cosine angle information is supplied to the sweep resolver assembly where it is demodulated and multiplied with the radar sweep from the Forward Indicator for generation of DVST deflection. Antenna position tangent information is supplied in a DC analog format from the A5 assembly to the ICU.

C. MECHANICAL DESCRIPTION

1. INDICATOR CONTROL UNIT (ICU). The DSTU ICU mechanical configuration is essentially the same as the F-4E DSTUMDS AICU unit. The unit weighs 37 pounds, is 20 inches wide, 9.1 inches high and 7.45 inches deep. An outline dimensions drawing is provided in Figure 16.

The unit is constructed of 6061 aluminum alloy. Rapid access of 29 printed circuit board positions is provided through the use of MS 21332 snap slide fasteners on the PWB bay cover.

Power supply power components are mounted on an aluminum heat sink assembly. Access to the heatsink and other chassis mounted components is provided through the use of a single hinged cover.

Cooling is accomplished with two 55 CFM fans. Cooling air is drawn into the unit through a ten (10) pore per inch flexible polyester foam air filter. Distribution of the cooling air has been tailored to the thermal load requirements of the ICU subassemblies and power components and is accomplished through the use of air metering holes.

2. RADAR PILOTS INDICATOR (RPI). The DSTU RPI is mechanically interchangeable with the AN/APQ-99 Radar Set RPI unit. The indicator unit weights 30 pounds. An outline dimension drawing is presented in Figure 17. The unit is also constructed of 6061 aluminum alloy. The unit has been designed to provide rapid access to major subassemblies.

A single 55 CFM fan provides for cooling the unit. Ambient air enters the unit via metering ports at various strategic locations on the unit. The air passes over heat emitting devices and is expelled through the fan at the rear of the box.

The ± 20 VDC power supply and deflection driver components are contained in four plastic mounting tray assemblies shown in Figure 18.

The tray assemblies have identical form factors and are fitted with separate connectors for assembly disconnent. The heat dissipating devices are mounted directly to individual mechanical metal heat sink devices. The plastic trays serve as mounting mechanisms and as plennums for distribution of cooling air through the component heat sink fans. The plastic trays are assembled as indicated in Figure 19. Mechanical design is such that the trays are attached to the back fan plate allowing the fan/tray assembly to be extended from the RPI unit on a service cable loop. The assemblies can be safely operated outside the RPI LRU providing access to all four trays for maintenance or troubleshooting.

Height: 9.10 inches
Width: 19.95 inches
Length: 7.45 inches
Weight: 37 pounds

PWB ACCESS DOOR

COOLING AIR INLET FILTER

COOLING AIR OUTLET HOLES

Figure 16. ICU LRU-14, Outline Dimensions
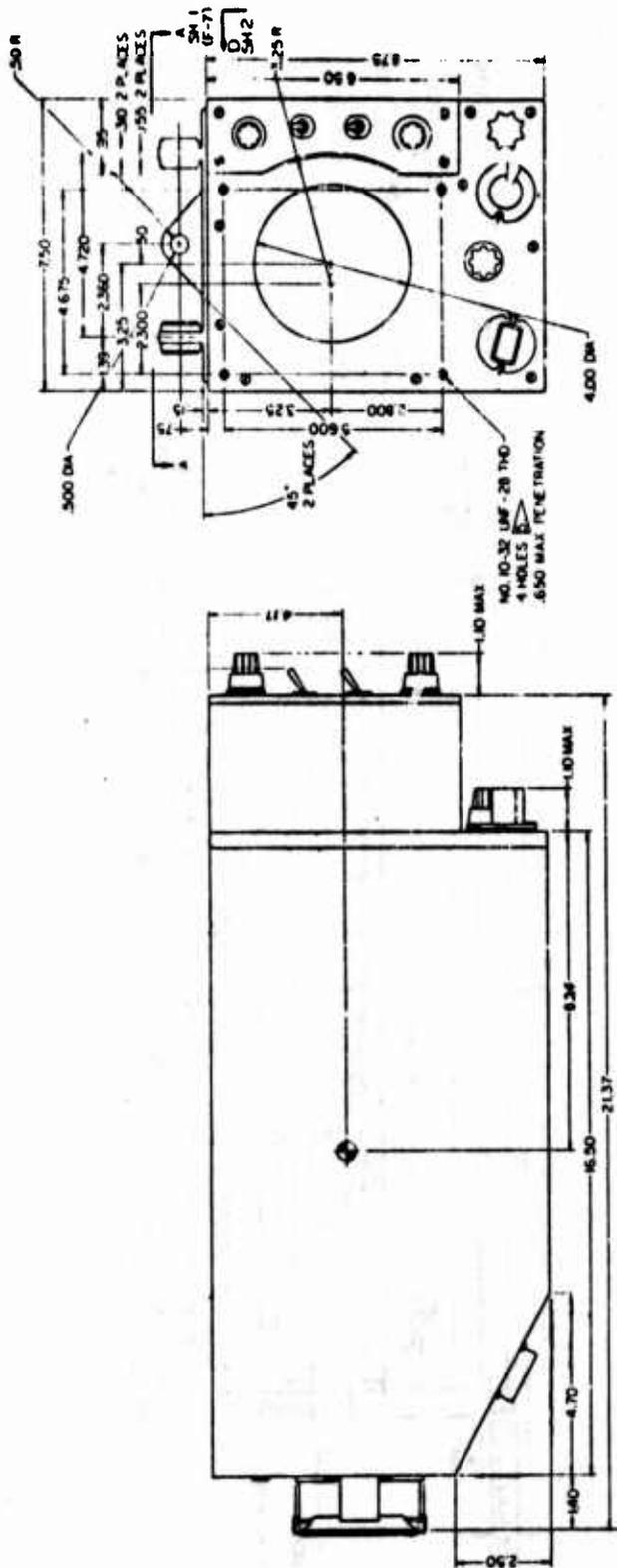
Height:	8.75 Inches
Width:	7.50 Inches
Length:	22.47 Inches
Weight:	30 Pounds

Figure 17. RPI LRU-15, Outline Dimensions
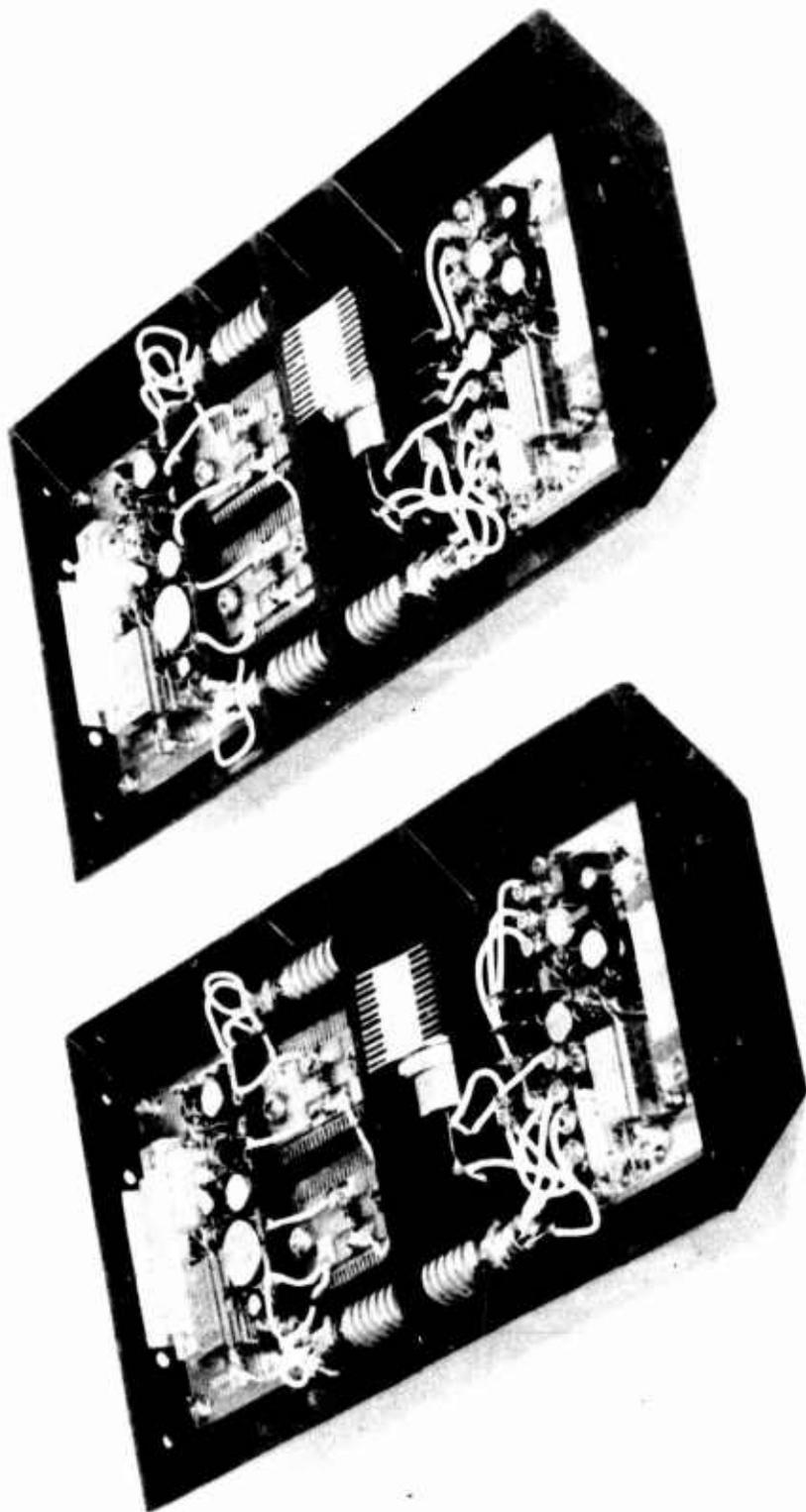
Figure 18. RPI Heat Sink Assembly Mounting Trays

TRAY CONNECTOR

WIRING HARNESS
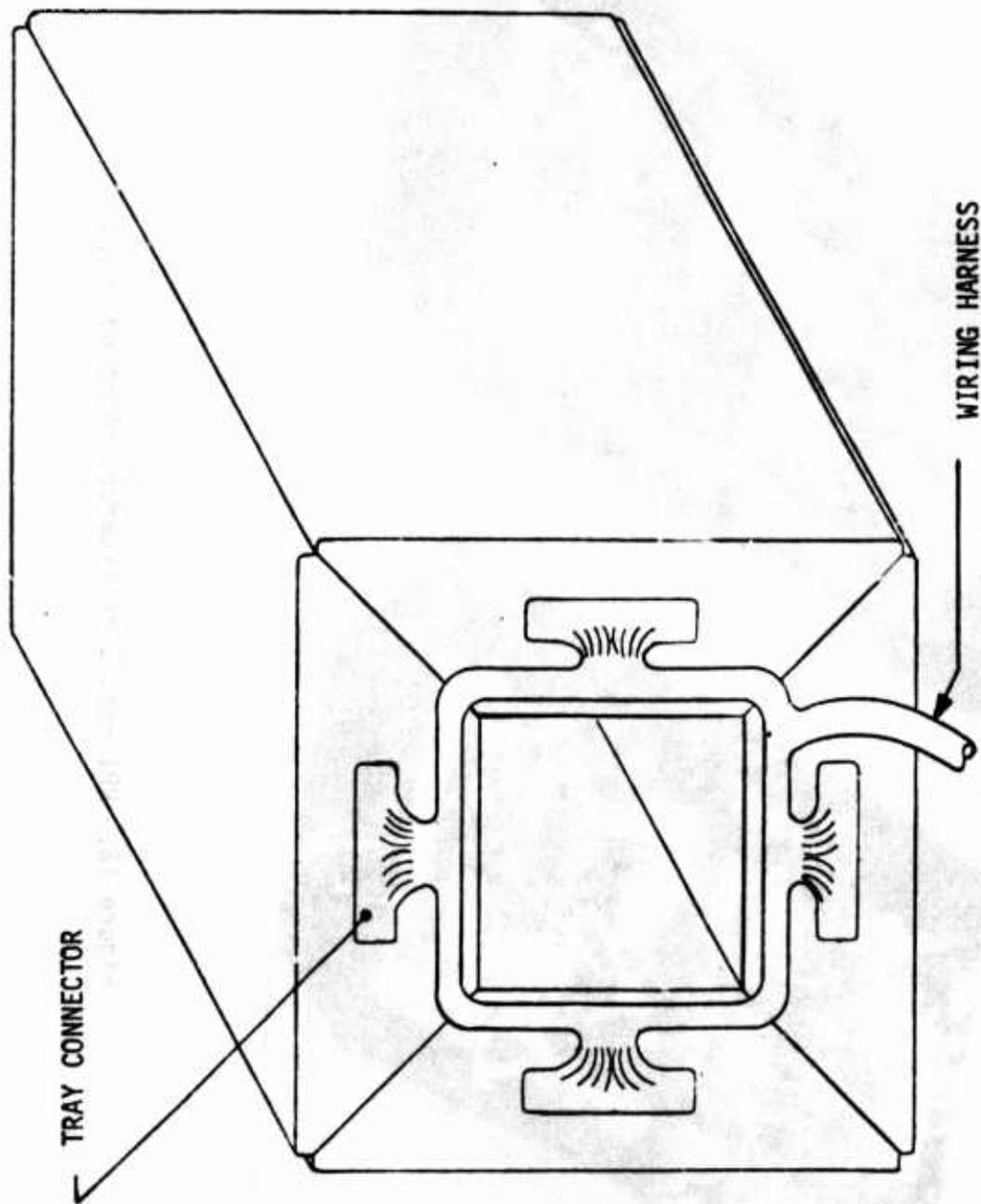
Figure 19. Four Plastic Heatsink Trays as Assembled in the RPI

D. DISPLAY FORMATS. The DSTUMDS has four basic modes of operation:

(1) PPI spiral scan radar.

(2) E² (TF) radar format.

(3) Standard 525 line electro-optical format.

(4) Standard 875 line electro-optical format.

Pictorial descriptions of each display format is shown in Figure 20.

The PPI spiral scan format is displayed as a depressed-center raster containing 512 range arcs in a 60 Hz, positive 2:1 interlaced field. The raster width is fixed at 90 degrees (±45 degrees). In wide scan radar mapping modes, video is displayed over the full raster. In the narrow scan CS radar modes, video is displayed in a 40 degree sector (±20 degrees). Symbology available in this mode includes range and offset cursors and Black Crow symbology. All symbology is generated in-raster.

The E² radar format is a 512-line, 60 Hz, 2:1 interlaced raster presentation. Radar video is presented in terms of range versus antenna elevation angle. The elevation axis is linear and covers the range from -15 degrees to +10 degrees. The 0 to 10 mile range axis is non-linear following the exponential function characteristic of the radar terrain following display format.

The standard 525 line electro-optical display presentation is provided as a conventional 525 line, 60 Hz, 1:1 aspect ratio, X-Y TV raster.

The 875 line electro-optical presentation is provided as an 875 line, 60 Hz, 1:1 aspect ratio raster.
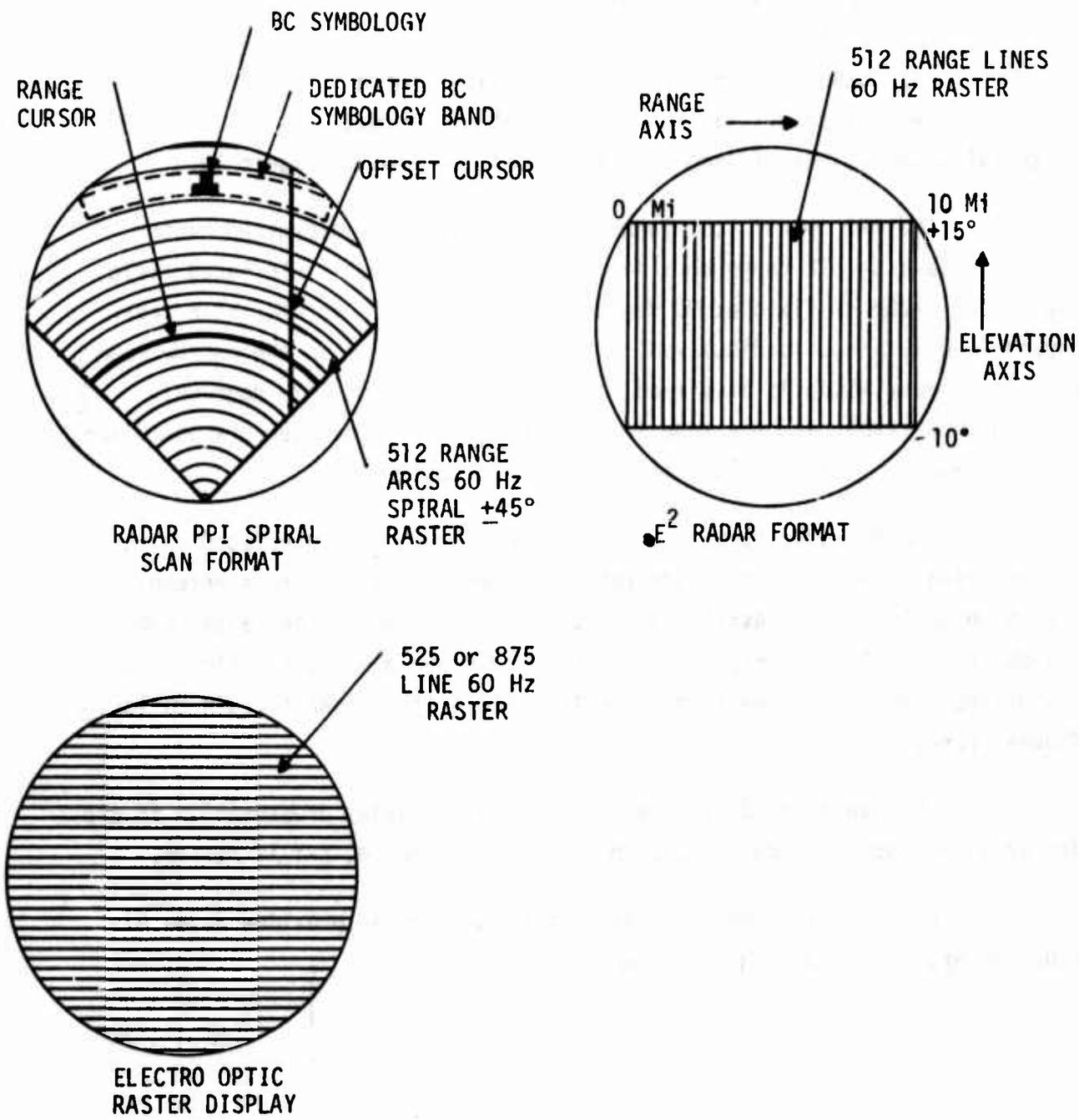
Figure 20. Multimode Display Formats

E. DSTUMDS PERFORMANCE PARAMETERS.

1. DSTU PARAMETERS - Memory type - Metal Oxide Semiconductor (MOS)

Random Access Memory (RAM)

Radar Resolution - 512 range cells per display diameter

160 azimuth bins per 90 degree azimuth scan

160 elevation bins per 25 degree elevation scan

2. DISPLAY PARAMETERS - Display Tube Type - High Brightness

Cathode Ray Tube (CRT)

Video Bandwidth - 10.5 MHz

CRT Spot Size - .006 + .001 inches

Light Output - 1000 ft. Lamberts minimum

Useable Display Diameter - 4.0 inches

F. DSTUMDS SPECIAL FEATURES. Six special features are designed in-to the DSTUMDS. These features are:

1. Selectable BC Digital Memory Range
2. Peak Detection
3. Threshold Detection
4. Display Freeze
5. BC Digital Threshold
6. Display Erase

The BC digital memory range may be varied to effectively vary the dynamic range of the BC processing circuitry in the ICU by frequency shifting the BC processing passband. This feature is provided to facilitate the determination of the optimum passband during flight test evaluation of the system.

Peak detection is mechanized in the DSTU video quantizer. The technique consists of detecting the highest amplitude signal which occurs within a quantizer clock sample gate, and selection of this peak signal for subsequent integration. Peak detection provides for increased detection

capability of the DSTU and reduced display collapsing loss. This feature is particularly desirable in the TERRAIN FOLLOWING mode of operation.

Threshold detection consists of the selection of a digital radar video signal occurring above a selected level and the display of this signal at the maximum brilliance gray shade on the CRT. The threshold level selected for threshold detection encompasses all signals above the first three gray shades.

Display freeze is mechanized by inhibiting the memory write function. Memory read continues and the last radar frame (one antenna scan) update remains unchanged in the memory. Both radar and BC information is frozen. Upon releasing the freeze function BC information is erased and then allowed to function normally.

A selectable digital threshold is provided to allow for thresholding BC information after it has been digitized and stored in a dedicated memory. This feature allows BC information below the selectable threshold to be disregarded.

The first three features listed above are selectable by four manual switches (two switches are provided for BC digital memory range selection) located on the ICU front panel beneath the fan cover. These selectable features are provided for the sake of equipment flexibility and the enhancement of equipment flight evaluation.

SECTION IV

TESTS PERFORMED

A. SUBASSEMBLY TESTS. Prior to installing subassemblies into LRU's extensive electrical testing of each subassembly was performed to evaluate and verify performance parameters. Many of the subassemblies were evaluated at the major subassembly group level (i.e. memory and memory timing subassemblies, Black Crow interface subassemblies, etc.) prior to incorporation into LRU's.

B. SYSTEM TESTS. Three types of system tests were performed on the equipment. These were LRU check-out/performance testing, system performance testing and system burn-in.

LRU performance tests were performed at room temperature to verify the desired LRU performance prior to attempting system integration. The tests were performed using individual LRU test sets which simulated LRU inputs and provided for monitoring and evaluating LRU outputs. No environmental tests were conducted at this test level.

The RPI and ICU LRU's were integrated at the bench level with the aid of a system test set which simulated aircraft, radar, MTI and Black Crow interface with the DSTUMDS. DSTUMDS performance was evaluated and the necessary system changes were incorporated. The tests were accomplished over a three week period.

A brief system burn-in under environmental conditions was conducted just prior to safety of flight testing. The burn-in test was performed informally for the purpose of evaluating system performance under environmental conditions. The test was conducted after completion of all system integration and radar and Black Crow bench integration testing. The system at this time had accrued well over 100 room ambient operating hours.

The system was subjected to a chamber environmental temperature range of -20 to +55 degrees centigrade and sea-level to 30,000 feet altitude.

The burn-in evaluation was completed in a two-day period with approximately 20 operating hours accrued on the system.

C. BENCH INTEGRATION. Bench integration was performed following system integration testing and was conducted in two phases: Radar and MTI DSTUMDS integration and Black Crow DSTUMDS integration.

Prior to bench integrating the DSTUMDS with the AN/APQ-99 Radar/MTI system, extensive modifications were incorporated in the radar bench cabling to provide compatibility with the DSTUMDS/Radar Quick Strike configuration. In addition, an interface panel was built for use in conjunction with the radar aircraft simulator test bench. The interface panel provided for Black Crow simulation and electro-optical sensor interface.

Actual bench integration was performed over a seven week period during which time the extensive interface between the two systems was verified. The tests were performed in the contractors radar tower facility. System performance was evaluated and the necessary changes were incorporated.

The Black Crow system was integrated with the DSTUMDS/Radar system at the radar bench level during the Radar/DSTUMDS integration phase. Black Crow integration was preceded by DSTUMDS integration with the Black Crow simulator test panel mentioned above. This phase of bench integration was accomplished in a two-day period.

D. SAFETY OF FLIGHT TESTS. The purpose of safety of flight tests was to certify the flight worthiness of the DSTUMDS. The test included temperature/altitude and vibration testing. All tests were performed in the contractors environmental test facility in accordance with MIL-T-5422F(AS), 30 November 1971.

1. TEMPERATURE/ALTITUDE. The temperature/altitude test was conducted according to the following test profile:

TABLE 3. TEST PROFILE

Step	Ambient Temperature	Altitude	Total Time After Stabilization	Remarks
1.	0°C	Ambient	2 hours	Operating
2.	0°C	30,000 feet	10 minutes	Operating
3.	+55°C	Ambient	4 hours	Operating
4.	+40°C	30,000 feet	4 hours	Operating

2. VIBRATION. The RPI LRU was vibrated in all three (X, Y, Z) aircraft axes in a vibration test fixture. The test fixture simulated actual aircraft installation. A nominal 2G (off resonance) accelerative force was provided as an input to the LRU. The equipment was operated during all vibration testing. The following vibration test profile was used:

(a) A resonant mode search was conducted in each of the 3 axes. Vibration inputs were as specified in Figure 21. The vibration frequency was swept from 5 Hz to 500 Hz to 5 Hz.

(b) A ten minute vibration dwell was performed at each resonant frequency point identified in the resonance search. Vibration input levels for each dwell were in accordance with Figure 21.

(c) Finally, vibration cycling was performed on the equipment. The equipment was vibrated in all three axes according to Figure 21. The vibration frequency sweep rate was logrithmic and such that a complete cycle (5 Hz to 500 Hz to 5 Hz) required 15 minutes. Two such vibration cycles were performed in each axis.

The ICU was vibration qualified by similarity to the F-4E DSTUMDS.

E. DSTUMDS ACCEPTANCE TEST. Acceptance testing of the DSTUMDS was performed at the radar bench level in the radar tower facility. The purpose of the Acceptance Test was to verify that the DSTUMDS equipment fulfilled the functional requirements set forth by the contract statement of work. The following areas were extensively tested:
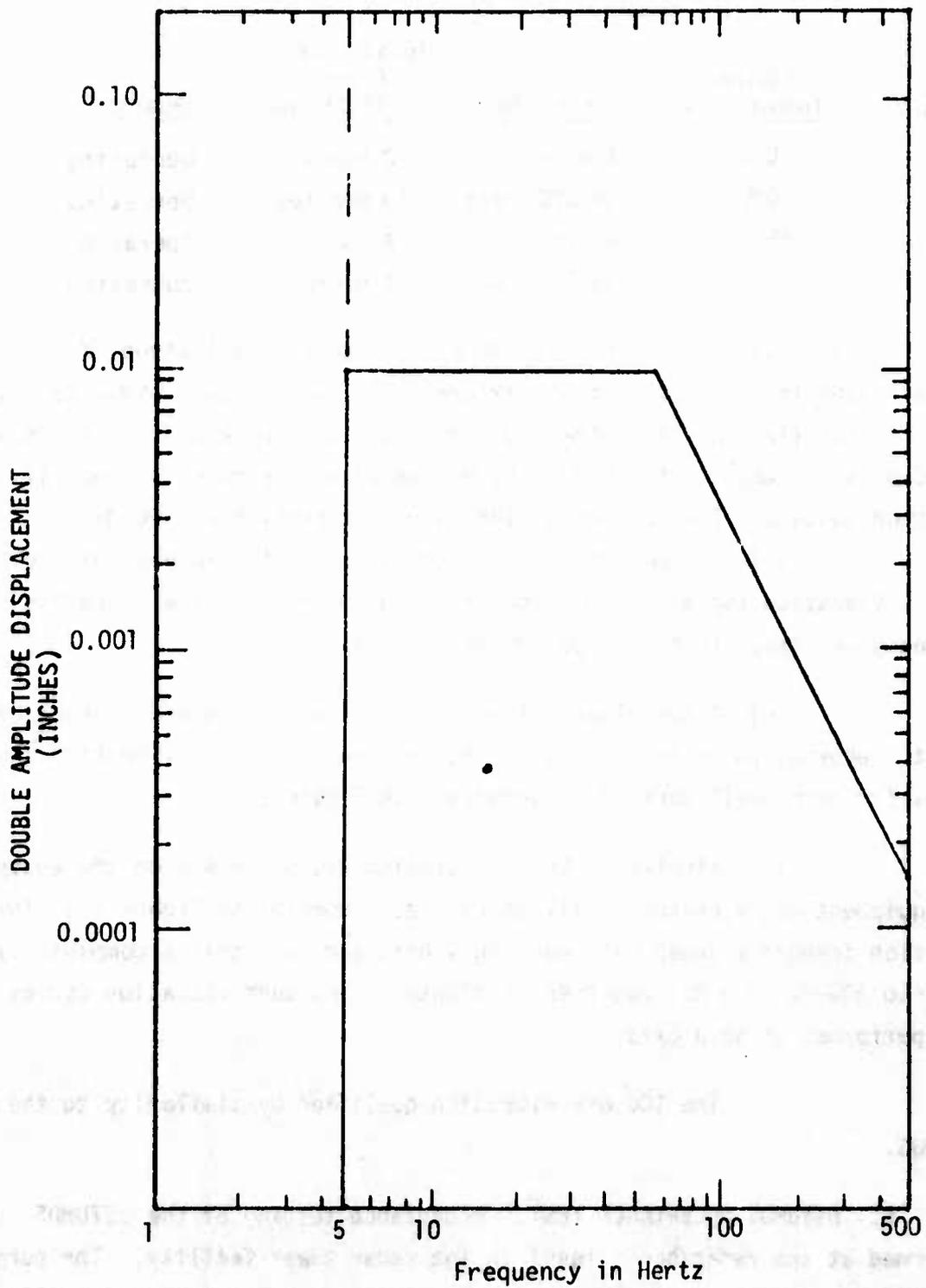
Figure 21. Vibration Level Curve

(1) Basic scan conversion functions and parameters.

(2) Interface between the DSTUMDS and the AN/APQ-99
Radar with GMTI processor.

(3) Interface between the DSTUMDS and Black Crow system.

(4) TV interface and interface with video recording
equipment.

F. AN/APQ-99 RECEIVER RESPONSE TESTS. Prior to shipment of the AN/
APQ-99, DSTUMDS and associated bench equipment; measurements were made on
the AN/APQ-99, system to determine the receiver response characteristics.
The measurements were made to verify that the receiver response assumed in
shaping the DSTUMDS video quantizer curve was correct and because it was
felt that such data would be required during flight evaluation testing.

The equipment test setup is indicated in Figure 22. The receiver
response was measured in the GMS mode of operation and was plotted as RF
signal input versus radar sum video voltage. Figure 23 provides the response
curve measured.

The response, as expected, was logrithmic and confirmed the quantizer
response implemented.
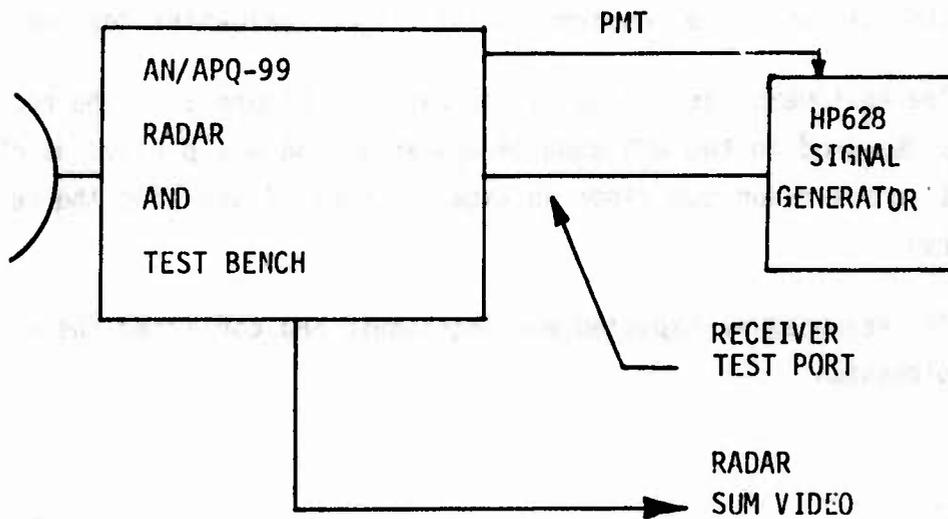
Figure 22. Receiver Response Test Setup
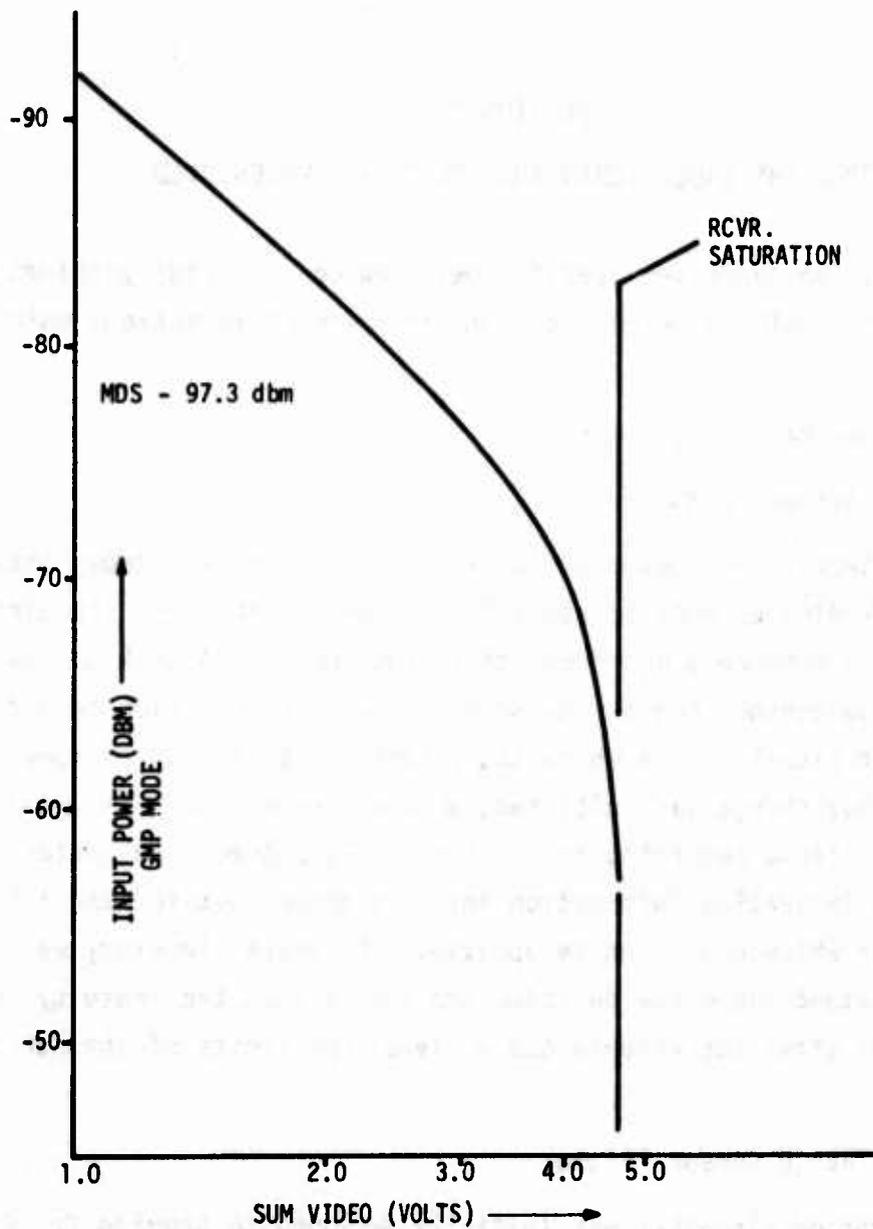
STEP	RF SIGNAL INPUT (dbm)	SUM VIDEO (VOLTS)
1	-97.3	MDS
2	-92.3	1.0
3	-86.3	1.5
4	-82.5	2.0
5	-79.4	2.5
6	-76.9	3.0
7	-73.3	3.5
8	-70.0	4.0
9	-61.5	4.5
10	-55.0	4.7 (saturation)

Figure 23.   AN/APQ-99 Quick Strike Receiver Response

SECTION V

PROBLEMS ENCOUNTERED AND SOLUTIONS IMPLEMENTED

This section addresses specific performance or design problems encountered in the DSTUMPS development and the corrective actions which were taken.

A. System Bench Test Phase

1. Automatic Mode Erase

Erase circuitry is designed to provide an automatic memory erase when the radar display mode or range is changed. Initially, the circuitry was designed to provide a short duration erase pulse. A problem was encountered in switching from a wide scan PPI mode of operation to a cross scan mode. In situations in which the antenna is at a scan extreme ($\pm45°$) when mode change was initiated, a memory erase could be completed prior to the antenna returning to the narrow ±20 degree scan sector limits. This resulted in writing information into the memory outside the ±20 degreee sector which could not be updated. The erase circuitry was modified to extend the erase duration and insure that the erase cycle was completed well after the antenna had achieved the limits of the narrow sector scan.

2. Range Cursor Flicker

Range cursor circuitry was initially designed to provide for displaying the range cursor on one display raster line and hence, only in one raster field to provide the sharpest possible cursor with best possible resolution. The problem encountered was that of range cursor flicker due to the 30 HZ field rate. The circuitry was modified to provide for writing circuitry in both fields (on two raster lines).

B. Radar Interface Phase

1. 28 Volt Line Transient Problem

Upon interfacing the DSTUMDS with the radar, a problem was noted in cross scan mode operation. Memory erases were erronously generated as a function of the antenna elevation to azimuth scan transitions. The problem was isolated to an unprotected relay in the radar which energized during the elevation portion of the antenna scan generating severe transients on 28 VDC logic lines supplied to the RP1. The transients coupled to the erase line in the RP1 causing unwanted memory erases. Diode protection was added to the relay.

2. Display Contrast Control

Rapid adjustment of the contrast control on the RP1 caused the display presentation to intensify in an erratic fashion. The source of the problem was determined to be potentiometer wiper bounce resulting in an intermittant open video amplifier control line as the control was rotated rapidly. The open line resulted in saturating the video amplifier causing video to be displayed at maximum intensity. Biasing was incorporated into the amplifier circuit to provide low amplifier gain when the control line opened.

3. TF Target Shift

It was noted while viewing live TF video that targets shifted as a function of antenna scan direction. This phenomenon resulted from the antenna azimuth offset creating a slightly different target scene in each scan direction (the antenna azimuth look angle is shifted approximately 4 degrees between the elevation down scan and up scan to form the standard TF box scan). Thus, information stored in memory during the down scan was replaced with different information during the up scan. Although the information presented was completely accurate the 3 HZ scene change rate was objectionable from a human factors standpoint. The write timing circuitry was modified so that in TF mode odd memory angle bins were updated on the down scan and even bins were updated on the up scan. This effectively integrated the two scenes and provided a more effective data presentation.

C. System Burn In

1. High Voltage Arc

The 20 KV high voltage power supply in the RP1 arced to the RP1 chassis at high altitude. The problem resulted from an improper in installation of the high voltage lead in the supply connector. Proper installation eliminated the problem.

2. High Temperature ICU Timing Problem

At +55°C ICU timing problems occured resulting in erratic video and symbology placement on the display. The problem was isolated to the Memory Timing and Control Assembly (14A11) and the source identified as noise on the signal ground plane of the 14A11 assembly adversely affecting the read address circuitry. The noise was induced by the high speed write address drivers located on the assembly. The problem was alleviated by isolating the driver grounds from the assembly signal ground.

SECTION VI

PROGRAM RESULTS

No flight evaluation of the DSTUMDS has been performed; hence the final results of the program are yet to be determined. The major results achieved thus far in the program are summarized in the following paragraphs.

A. SUCCESSFUL AN/APQ-99 BENCH INTERFACE. The DSTUMDS has been designed and interfaced with the AN/APQ-99 radar. All existing radar modes, capabilities and features have been retained and the following additional ones provided.

1. Cursors are provided in all radar PPI display presentations. Existing radar displays could not provide cursor information in 20 mile range high PRF modes of operation. In addition, the DSTUMDS provides the capability of varying the cursor intensity from a level two gray shades above the brightest video to the black level. Black cursors are very effective when used with high video density map presentations.

2. The RPI display quality has been improved. The DSTUMDS provides a flicker free high brightness presentation with a freeze capability.

3. The DSTUMDS provides the capability for in flight video recording of radar and radar symbol information.

B. SUCCESSFUL BLACK CROW INTERFACE. The DSTUMDS has been designed and interfaced with the Black Crow system. The interface provides digital correlation processing of Black Crow information and the capability of displaying the information synergistically with radar and MTI information. Video formating is such that in flight video recording of Black Crow information is made possible.

SECTION VII

RECOMMENDATIONS

This section addresses recommendations for further development, tests and investigations to be performed on the RF-4C DSTUMDS. The contractor considers these to be invaluable to the development of the final configuration RF-4C Quick Strike digital signal transfer unit and multisensor display system.

A. FURTHER DEVELOPMENT.

1. MTI SYMBOLOGY. The mechanization for processing and displaying MTI targets has been discussed in Section III. In normal MTI operation it is desirable to display MTI video and ground map video simultaneously. This capability is currently implemented so that in the MTI mode of radar operation, MTI targets are displayed at full brilliance and background map video may be varied from full brilliance to off via an operator panel control. The problem which arises is that of confusing MTI targets. The suggested development effort consists of designing and implementing circuitry which will allow MTI information to be displayed as distinct symbols, rather than as radar video targets. The required circuitry is of the nature of that described in an unsolicited technical proposal submitted to Air Force Systems Command Headquaters, Aeronautical Systems Division in November of 1973. The prosal is entitled "A Technical Proposal for the Addition of GMTI Symbol Generation Capability to the RF-4C DSC Display System" and was assigned ASD Control Number 73-D-28. While such circuitry would not improve the basic moving target detection capability of the AN/APQ-99 Radar/Moving Target Indicator system, it would significantly enhance the man-machine interface by improving the operator's display interpretation capability.

2. ELECTRONIC RETICLES. The PPI and E^2 reticles are currently implemented via an etched grid overlay. Parallax is inherent in this implementation due to thickness of the CRT faceplate. The recommended development effort consists of designing and implementing circuitry to generate in raster recticle information. Development of this circuitry is straight-

forward and its implementation would eliminate parallax, improve target registration, and provide for video recording reticle information.

3. 4 K MEMORY. As indicated in Section III, the random access memory (RAM) is constructed using 2,048 bit RAM devices (AMS 6003). Any future development effort should take advantage of the random access memory developed for F-4E DSCG production. This memory utilizes the contractors 4,096 bit RAM device. The development effort would be that of interfacing existing RF-4C DSTUMDS ICU circuitry with the F-4E DSCG production memory. Advantages include:

        1. F-4E DSCG commonality

        2. Circuit reduction (4 memory cards would replace the 10 currently used)

        3. Concomitant reliability, maintainability

4. FRONT SEAT CRT DISPLAY. The current RF-4C Quick Strike display configuration is a hybrid one using an AN/APQ-99 DVST display in the front seat and the DSTUMDS CRT display in the rear seat. This configuration was chosen as an austere means of evaluating the DSTUMDS in the RF-4C Quick Strike sensor enviornment. Any future RF-4C DSTUMDS development effort should address a dual CRT display system.

5. SELF TEST MODE. The display/radar/BC/FLIR interface in the aircraft is such that problems cannot be easily isolated between the sensors and the display system. The development of a simple DSTUMDS self test mode could significantly reduce the maintanence time required in the current configuration in analysis of problem source.

B. TESTING.

1. NON-LINEAR ANALOG-TO-DIGITAL CONVERSION. A logrithmic radar video analog-to digital conversion (quantizer) response has been implemented in DSTUMDS. This response shape was derived based on the AN/APQ-99 radar receiver video response and upon tower observations. Since the quantizer response has not been proved optimum under actual flight conditions, it is

recommended that special attention be given the quantizer response during the flight test phase of the program. The circuit response is easily changed to allow optimumiztion of the curve during flight test evaluation.

2. BLACK CROW PROCESSING CIRCUITRY. Parameters used in designing the Black Crow interface circuitry contained in the DSTUMDS ICU were theoretically derived. These parameters (particularly sample rate range and dynamic range) should be evaluated and optimized during flight tests. The circuitry has been implemented so that critical parameters may be programmed between flights.

C. INVESTIGATIONS.

1. INCREASED VIEWING AREA REAR SEAT DISPLAY. The RPI unit uses a five-inch diameter CRT to provide a four-inch diameter viewing area. Interface with high resolution sensors such as 875-line FLIR indicates a need for increased viewing area. Further investigation should be conducted to determine the optimum rear seat viewing area based on resolution requirements, and display size and design constraints.