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RADC ltr, 15 Jun 1983

RADC-TR-74-264
Final Report
October 1974

DISCRETE SIGNAL MOVING TARGET INDICATOR (MTI)

General Electric Company

Rome Air Development Center
Air Force Systems Command
Griffiss Air Force Base, New York 13441

DISCRETE SIGNAL MOVING TARGET INDICATOR (MTI)

D.N. Ludington
H. Lobenstein

General Electric Company

FOREWORD

This is the Final Report on Discrete Signal Moving Target Indicator by the General Electric Company, Aerospace Electronic Systems Department, Utica, New York, under Contract F30602-73-C-0152, Job Order 45060187, for Rome Air Development Center, Griffiss Air Force Base, New York. Mr. William Lee Simkins, Jr., and Mr. Daniel Budzynski, both of OCTS, were the RADC Project Engineers.

The principal GE contributors were H. Lobenstein and D.N. Ludinton, the authors of this report. Acknowledgment is made to J. Whitten and Dr. W. Butler, GE Corporate Research and Development Center, for many enlightening discussions. Dr. Butler also provided the charge transfer devices used in this study.

The effort described was accomplished from 7 March 1973 to 7 June 1974.

This technical report has been reviewed and is approved.

APPROVED: William Lee Simkins, Jr

WILLIAM LEE SIMKINS, JR.
Project Engineer

APPROVED: William T Pope

WILLIAM T. POPE, Assistant Chief
Surveillance and Control Division

FOR THE COMMANDER: James G McGinnis

JAMES G. McGINNIS, Lt Col, USAF
Deputy Chief, Plans Office

ABSTRACT

The objective of the Discrete Signal Moving Target Indicator (DSMTI) contract was to apply charge transfer device (CTD) technology to the design and fabrication of a three-pulse MTI, and demonstrate its capabilities in an actual radar system. The specified 50-db cancellation ratio was achieved.

The CTD is a sampled data integrated circuit where the signal is Nyquist sampled as in a digital system; however, the samples are stored and processed as discrete packets of charge. Hence, the CTD's utilize a continuous range of amplitude and therefore eliminate the cost, volume and power penalties inherent in analog-to-digital and digital-to-analog conversion, while retaining the virtues of stability and size offered by digital systems.

Design trade-offs necessitated by the capability of available devices, and subsequent limitations are discussed.

The state of the art in CTD's has progressed enormously since the inception of this contract. Indeed, progress has been so great that the multiplexing utilized to achieve the required time-bandwidth product for this contract is no longer necessary, and if the design were initiated today the hardware could be reduced by a factor of four.

It is therefore reasonable to consider this design approach where stable, low cost, replacements for existing MTI's or new MTI's within the time-bandwidth product of this contract are contemplated.

In addition signal processing methods such as pulse compression, correlation, Chirp Z transforms and allied techniques are under investigation and should be considered by the system designer.

EVALUATION

Considerable interest exists in updating present radar systems. Therefore, the development of low cost, high performance signal processing techniques is a very important area of interest to those concerned with surveillance and control. This contractual effort consisted of the design, fabrication, and testing of a three-pulse MTI utilizing a new charge transfer device (CTD) technology. The performance factors considered in this effort were the dynamic range and cancellation ratio of the breadboard MTI model and the time-bandwidth product of the basic CTD delay line.

The results of this effort demonstrate the high performance and inherent advantage of CTD techniques over digital and conventional analog systems. A brief overview of the present state-of-the-art in the rapidly developing CTD technology is presented allowing system designers to determine if present or near future devices are useable in specific applications such as pulse compression, correlation, and other allied techniques. The CTD technology could provide cost effective signal processing systems for updating old radars or for implimentation in new high performance radar systems. This work is in support of TPO-5, "EM Generation and Control."

William L Simkins Jr

William L. Simkins, Jr.
Project Engineer/OCTS

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS (Continued)

SECTION I

INTRODUCTION

The objective of the Discrete Signal Moving Target Indicator (DSMTI) contract was to apply Charge Transfer Device (CTD) technology to the fabrication of a three-pulse MTI feasibility model.

The CTD is basically a sampled data processor. That is,the time signal to be processed is Nyquist sampled as in a digital system. The samples, however, are not digitized; instead they are stored and processed as discrete packets of charge. Hence, the name Discrete Signal MTI. Thus, although operating in the sampled data domain (discrete time), as do digital devices, CTD's utilize a continuous range of amplitude. This property can therefore eliminate the cost, power requirement and volume of analog-to-digital (A/D) and digital-to-analog (D/A) conversion inherent in digital systems, while retaining all of the stability and size virtues of digital techniques.

To demonstrate the feasibility of this type of MTI, the contract required that performance be examined on a realistic basis. Hence, all appropriate circuitry for integration with the Rome Air Development Center (RADC) Test Bed Radar had to be provided.

The specified 50-db cancellation ratio (CR) performance was successfully achieved. The CTD's for this contract were developed and fabricated by the Solid State and Electronic Laboratory of General Electric Corporate Research and Development Center, Schenectady, New York.

The state of the art of CTD's since the inception of this contract has moved rapidly. The MTI portion of this contract could, for instance, now be built on at most two Cambion cards; therefore this approach should be considered seriously where stable low cost replacements of existing MTI's, or new MTI's, within the time-bandwidth range of this contract, are contemplated.

In addition devices using this generic technology should be considered for pulse compression, Chirp-Z transforms, correlation and allied techniques.

SECTION II

TECHNICAL REQUIREMENTS

The DSMTI is a direct replacement for a quartz ultrasonic delay line canceller in the RADC Test Bed Radar System.

The existing MTI provides timing pulses for the burst waveform transmission, as well as performing the MTI function.

1. BASIC MTI PERFORMANCE REQUIREMENTS

The pertinent technical requirements for MTI performance are shown in Table I.

TABLE I. TECHNICAL REQUIREMENTS

Type of MTI	Three-Pulse Vector Cancellation (In-phase and Quadrature)
Cancellation Ratio	50 db
Dynamic Range	50 db
System Waveform (PRI)	Multiple Burst. 250 microseconds intraburst PRI
Pulse Width	1 microsecond

2. SYSTEM INTERFACE REQUIREMENT

Although not specified in the contract, it was decided to build the burst generating circuitry provided by the quartz canceller, into the DSMTI, since it would be pointless to depend on a quartz delay line for the functioning of the system. Either operating mode can be connected (at the MTI front panel) by system personnel.

The interface parameters are shown in Table II.

TABLE II. INTERFACE PARAMETERS

System Local Oscillator	52.000032 MHz, Burst A 49.999598 MHz, Burst B
Input Format	In-phase (I) and Quadrature (Q) Baseband Video, 1 volt p/p, Z_o = 50 ohms.
MTI Output	a. I and Q Video, 1 volt p/p, Z_o = 50 ohms. b. 52 MHz IF, -30 dbm, Z_o = 50 ohms. c. Detected IF, 2 v peak, Z_o = 91 ohms.
S_{11}, S_{12}	4.5 v peak, 0.75 microsecond.
S_{21}, S_{22}	4.5 v peak, 0.5 microsecond, 12 pulse burst, 250 microsecond nominal spacing.

SECTION III

CHARGE TRANSFER DEVICES

1. THEORY OF CHARGE TRANSFER DEVICES

The charge transfer device (CTD) is best characterized as an analog sampled-data delay line. The CTD equivalent circuit is shown in Figure 1.

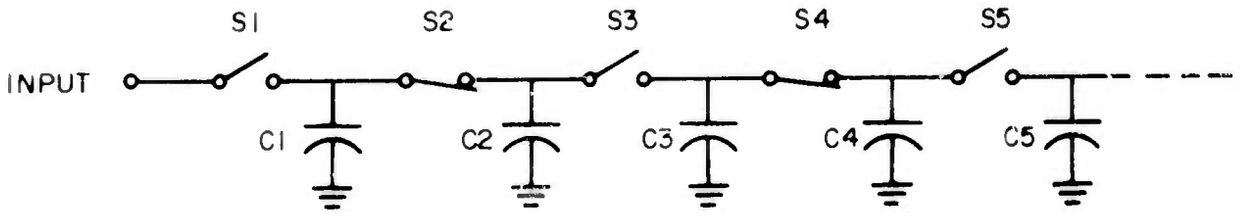

Figure 1. CTD Equivalent Circuit

The CTD consists of capacitive storage elements separated by switches. When switch S1 is closed, capacitor C1 is charged to the input signal level. Then switch S1 is opened and switch S2 is closed, which allows the input sample to be transferred to C2. In this manner, the switches alternately open and close, sending the analog samples down the device. Isolation between samples is provided since all odd-numbered switches are operated together and all even-numbered switches are operated together. Complementary square wave clocks are used to drive the switches, thus preventing the odd-numbered switches and even-numbered switches from being closed at the same time.

The rate at which the analog information is transferred through the CTD is determined by the rate at which the switches are operated. For a given number of stages (a switch and associated capacitor are considered as one stage), the total delay is determined by the digital clock period, as given by equation (1).

$$\tau = \frac{N}{2f_c} \tag{1}$$

where

τ = delay

N = number of stages in the CTD

f_c = CTD clock frequency

Thus the delay provided by the CTD can be varied either by changing the number of stages in the device or by changing the clock frequency.

2. OPERATIONAL CHARACTERISTICS

In practice switches S_i can be bipolar, MOSFET or JFET semiconductors which are implemented in the form of monolithic integrated circuits.[1] This allows many stages to be fabricated on one chip. Capacitors C_i are an integral part of the monolithic device and are on the order of a few picofarads.

Figure 2 shows a ten-stage MOSFET charge transfer device which illustrates the circuit implementation of Figure 1.

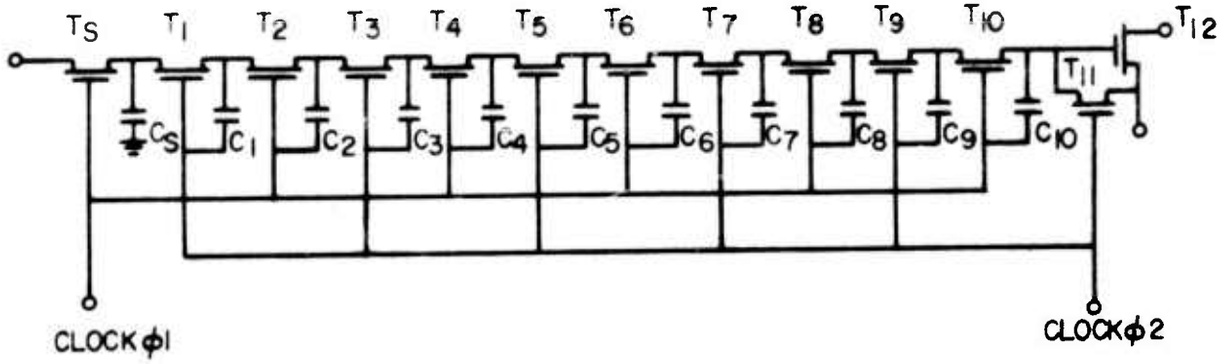

Figure 2. Ten-Stage MOSFET CTD

The MOSFET devices T_i are enhancement mode devices that are normally off and switched on only when the gate voltage exceeds the threshold voltage Vt.

A section of a basic MOS charge transfer device is shown in Figure 3 and nodal voltage waveforms are shown in Figure 4. A typical (p-channel) MOS device, Ti, is turned on by applying a negative voltage, -E, to the gate electrode. The storage capacitor C_i is precharged to -(E - Vt) volts, where V_t is the threshold voltage of the device. (The precharging takes place during the previous half-cycle.) During that period, T_{i+1} is initially on. A negative current flows to C_i until the voltage across it becomes equal to

[1]Since MOSFET devices were incorporated in the MTI, they will be used to illustrate the CTD characteristics.

$-(E - V_t)$. At this point, current ceases to flow since the source of T_{i+1} is a threshold voltage below the gate voltage. The drain of T_i is therefore at $-(2E - V_t)$ volts at the onset of charge transfer. At the source side of the device, capacitor C_{i-1} has a voltage $-e_i$ corresponding to a specific signal sample. When T_i starts to conduct, the voltage across C_{i-1} becomes more negative. Conduction continues until the source is a threshold voltage below the gate, at which time the transfer of charge is terminated. The charge $\Delta q = -C_{i-1}(E - V_t - e_i)$ is supplied by the drain current of T_i. The voltage across C_i is therefore reduced to $-(E - V_t) - (\Delta q/C_i)$ which is $-e_i$ for $C_{i-1} = C_i$. In this way, the transfer of information is accomplished by a charge-deficit transfer.

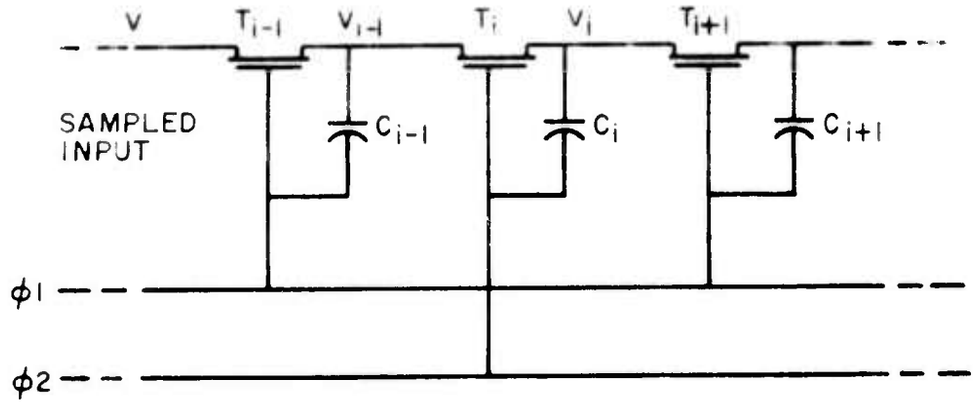

Figure 3. CTD Section

It is evident that there is never a complete transfer of charge from one storage element to the next. However, the amount of charge left behind at each transfer can be almost independent of the amplitude of the initial charge. Thus, it is not necessary to operate in a 100-percent tranfer mode (which would severely restrict the frequency at which the device could be operated). Rather, the circuit can be operated in the so-called "partial transfer mode," in which the effect of charge left behind during one transfer is compensated by the charge which is picked up from the previous transfer. In this mode of operation, the difference between the charge that is left behind and the charge that is picked up becomes progressively smaller, as the difference between successive charge packets is reduced. It follows that a bandwidth/dynamic range trade-off can be expected from these devices; i.e., for a given length of delay line, the smaller the dynamic range required, the larger the bandwidth of the circuit.

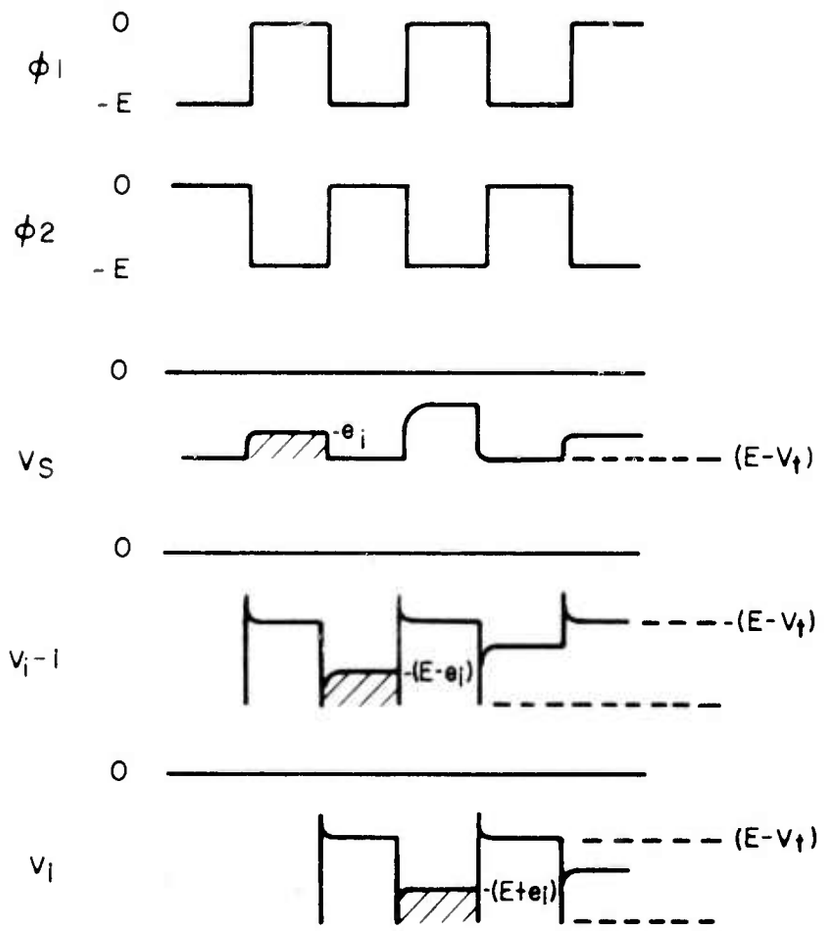

Figure 4. Nodal Voltage Waveforms for MOS CTD

The ultimate effect of incomplete charge transfer will be to bandlimit the circuit. At low clocking frequencies, the bandwidth will be determined by the Nyquist sampling requirement, i.e., the sampling frequency must be at least twice the bandwidth of the input signal. At high clocking or sampling rates, the bandlimiting will result from the transfer characteristics of the circuit itself, so that increasing the clocking rate will not necessarily result in an increased bandwidth.

An elementary analysis of the effect of cascading a large number of delay sections was performed. It was assumed for this analysis that the transfer of charge from one storage capacitance to another can be roughly modeled by a simple RC time constant as shown in Figure 5.[2]

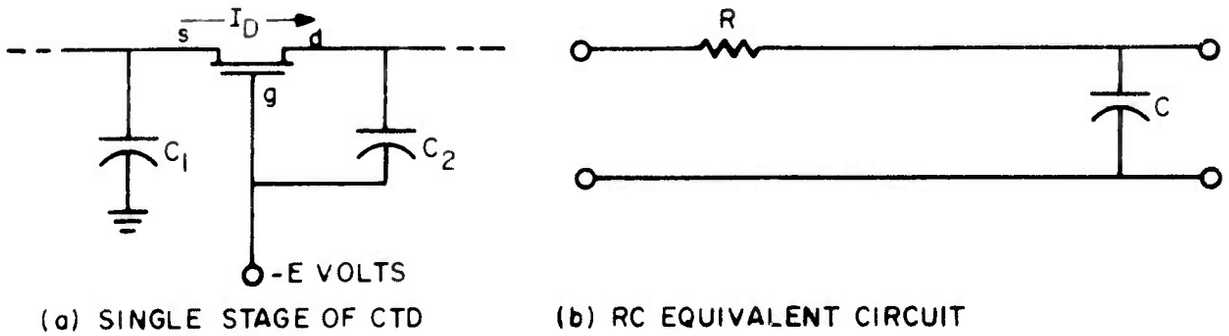

Figure 5. Single-Stage CTD and Equivalent Circuit

The transfer function of this circuit is given by:

$$T(s) = \frac{1}{1 + sCR} \tag{2}$$

where s is the complex frequency variable, and the 3-db bandwidth of the circuit is given by

$$BW_1 = \frac{1}{2\pi CR} \tag{3}$$

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2 W. J. Butler, C. M. Puckette, and M. B. Barron, "Bucket Brigade Bandwidth Characteristics," General Electric Company, Corporate Research and Development Center, Schenectady, N. Y., TIS Report 72 CRD 002 (December 1971).

It is further assumed that the time sequential transfer of charge through n sections may be modeled by cascading n isolated RC sections. Then the overall transfer function is given by

$$T(s) = \left(\frac{1}{1 + sCR}\right)^n \tag{4}$$

and the 3-db overall bandwidth, BW_C is given by

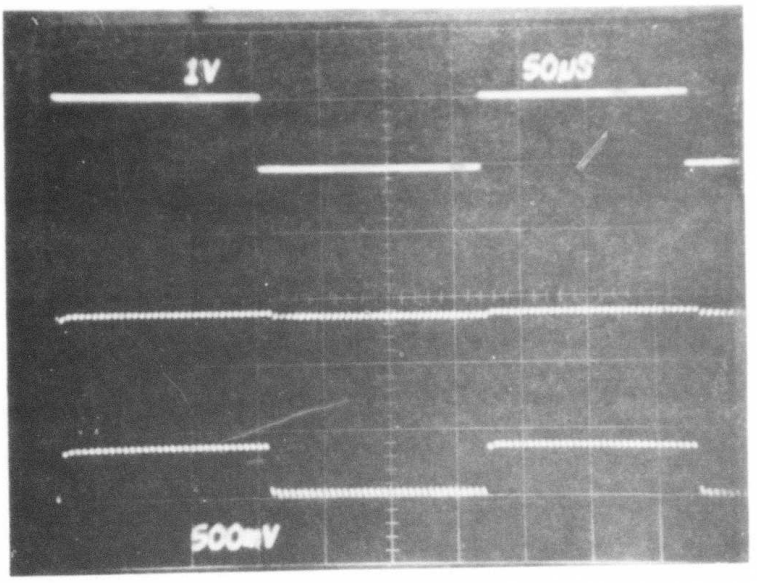
$$BW_C = \sqrt{2^{1/n} - 1}\, BW_1 \tag{5}$$

which for large n, becomes

$$BW_C = \frac{0.83}{\sqrt{n}}\, BW_1 \tag{6}$$

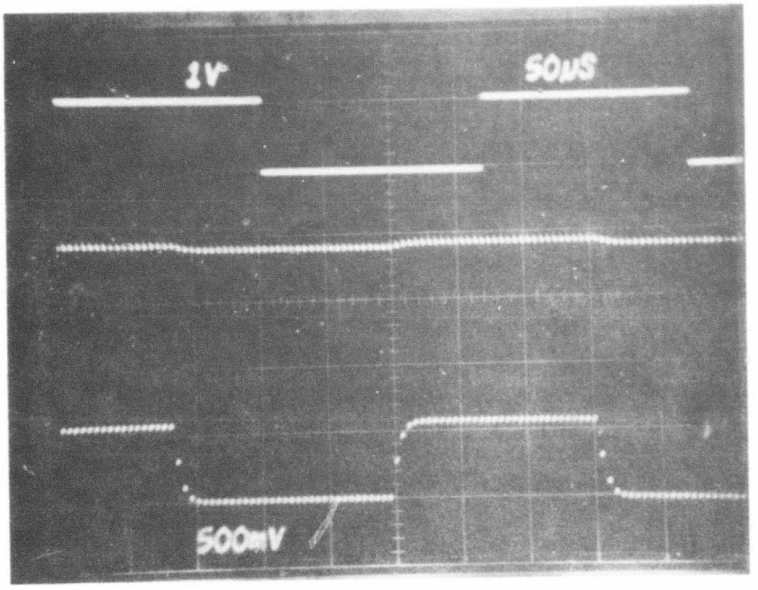
Figure 6 shows the bandlimiting effects of a MOSFET charge transfer device. In Figure 6a, the signal is picked off after the fourth stage and pulse reproduction is very good. In Figure 6b, the signal is picked off after 102 stages and the bandlimiting effect of the CTD is clearly evident.

The samples at the leading edge of the pulse are decreased in amplitude and the charge which is left behind builds up as samples at the trailing edge. These trailing voltage levels are not actual samples from the input but come from charge left behind by incomplete charge transfer. This can be verified by counting the number of samples in Figure 6; there are more samples in Figure 6b.



(a) Input

Output after
Four Stages



(b) Input

Output after
102 Stages

Figure 6. Bandlimiting Effect of a CTD

SECTION IV

SYSTEM DESIGN

1. MTI DESIGN

A moving target indicator is used to reduce the effects of stationary clutter while at the same time enhancing signals which represent moving targets. The method of implementation is to subtract a radar return which has been delayed one PRI from the incoming radar return. This is shown in Figure 7 where T is the delay.

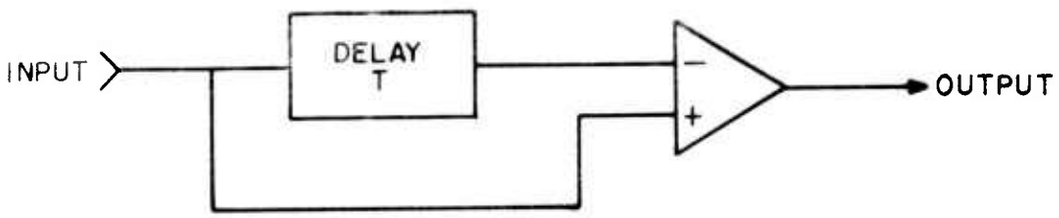


Figure 7. Basic MTI Circuit

The object of this contract was to use the charge transfer device as a delay line. The advantage of the CTD is that since the delay is controlled by a digital clock, the delay can be made very stable, while the signal path is still analog, and does not require A/D or D/A conversion as in a digital system.

From Table II, the IF bandwidth is 1 MHz. In-phase (I) and quadrature (Q) processing are used to preserve the amplitude and phase of the signal. The bandwidth of the I and Q signals is 500 KHz.

The Nyquist theorem states that the sampling frequency must be at least twice the bandwidth of the signal. Of course, this theorem assumes an ideal low-pass characteristic for the bandwidth. In the real world, the frequency response of the signal rolls off more slowly, and the bandwidth is usually taken as the 3-db bandwidth. Because of this gradual rolloff in frequency, it was decided to sample at three times the bandwidth or 1.5 MHz.

By substituting the sampling frequency and PRI into equation (1), the required number of stages for the CTD can be found.

$$N = (2 f_c)(\ ) = (2)(1.5 \times 10^{6})(250 \times 10^{-6})$$

$$N = 750 \text{ stages} \tag{7}$$

For this contract it was not possible to cascade the required number of stages and still achieve the 500 KHz bandwidth. Therefore a parallel scheme with multiplexing was required to achieve the required number of total stages while at the same time limiting the number of cascaded stages in each device. Figure 8 is a block diagram of the multiplexing scheme. The switches at the output of the CTD's are only closed when the associated CTD is being read out.

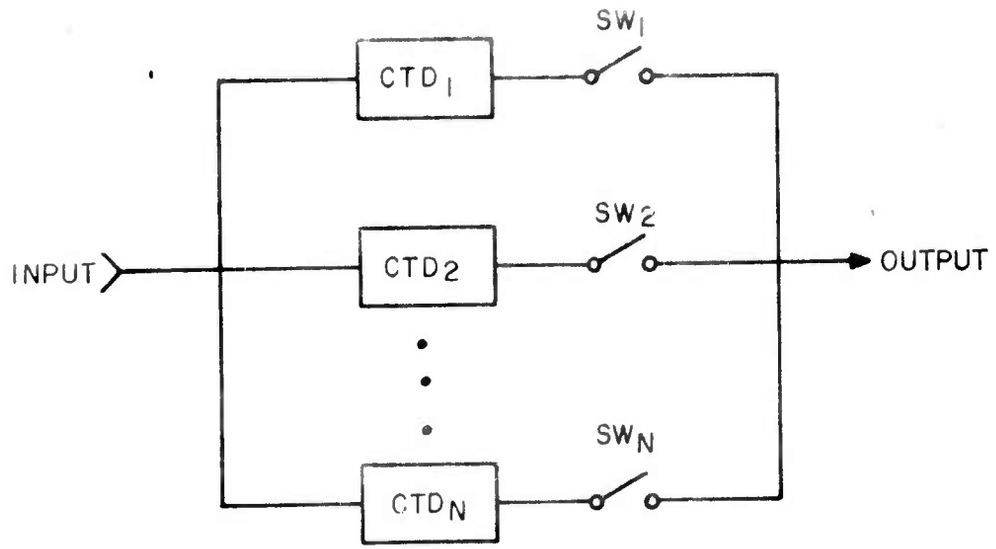


Figure 8. CTD Multiplexing Scheme

Two methods are available for clocking the charge transfer devices which will preserve the sampling rate and delay. First, the CTD's can be

clocked at a 1.5 MHz rate, but only for part of the PRI. After enough samples have been taken to fill a CTD, its clock is turned off, and the clock to the next CTD is turned on. This process is continued with each of the CTD's being clocked for a period equal to the PRI divided by N, where N is the number of parallel CTD's. At the next PRI, the sequence will be repeated. Figure 9 shows the clock waveforms for this gated clock method of operation.

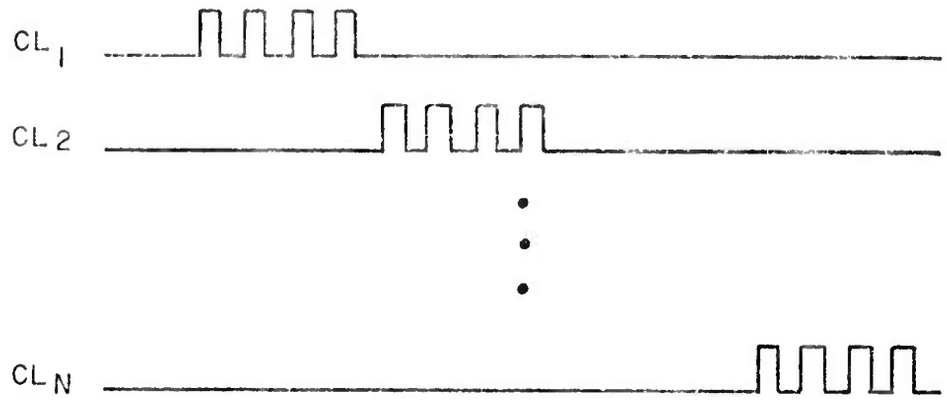


Figure 9. Gated Clock Operation

The second method of parallel operation uses overlapping clocks. In this method, the clocks to each CTD are run continuously, but between adjacent CTD's the clocks are skewed so that only one CTD is sampling the input at a time. Figure 10 shows the overlapping clock mode of operation. The output switches are closed for only a portion of the clock period.

It is evident from Figure 10 and the selected sampling rate that if N is greater than 3, the CTD clock frequency will be less than the 500-KHz analog bandwidth. This is permissible since, with the staggered clock arrangement, the time between samples is equal to the clock skew and is still equivalent to a 1.5-MHz sampling rate.

Each method has advantages and disadvantages. The advantages of the overlapping clock mode are that the clock frequencies are lower and the

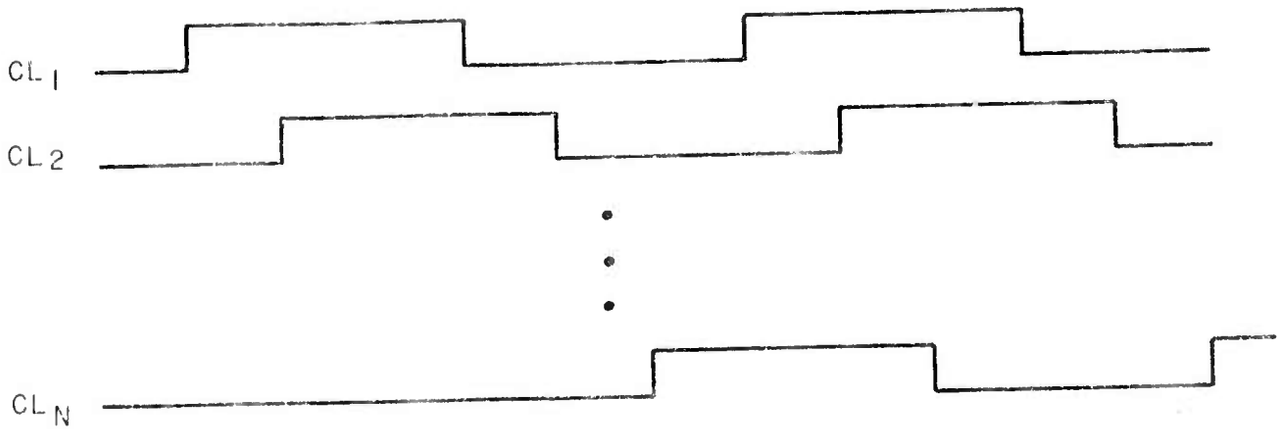


Figure 10. Overlapping Clock Operation

clocks are running continuously throughout the PRI. A lower clock frequency means that more time is available for charge transfer between stages (thus reducing the charge loss in the CTD), while the continuous clock eliminates nonuniform leakage from the storage capacitors within the CTD. If the storage capacitors all leaked at the same rate, the relative values of the samples would remain the same and only the dc level would change. Since there is nonuniform leakage, the relative difference between the sample values changes and when the clock is turned on again a "pattern noise" is superimposed on the stored signal with peak-to-peak amplitude dependent on the length of time that the CTD clock is off. The distribution of the "pattern noise" is random; some capacitors have large leakage because of processing problems and material imperfections.

The advantage of the gated clock mode is that the clock rate in each CTD is fast enough to satisfy the Nyquist rate, and the signal samples are stored in consecutive stages in the same device. This is in contrast to the overlapping clock mode where consecutive samples of the signal are stored in adjacent parallel CTD's.

Two problems are inherent in the overlapping clock configuration. Both of these are caused by incomplete charge transfer. Figure 6b shows that the first output sample is reduced in amplitude from the input. Since only one sample is taken by a CTD, the maximum signal output is reduced in amplitude. The input amplitude can be increased somewhat to compensate

for this effect as long as the first stages of the CTD do not saturate. Essentially, this reduced output decreases the dynamic range.

The effects of charge transfer inefficiency also appear as additional samples that trail the delayed pulse. When the samples are in the same CTD (at a fast sampling rate), these extra samples cause the pulse to be extended in time similar to the effect of a RC low-pass filter. However, in the overlapping clock mode, each of several parallel CTD's takes one sample of the input. These samples are propagated down the CTD's with low clock frequencies. When the outputs of the CTD's are recombined, the input will be reconstructed and then, because of the lower clock frequency, the samples from the incomplete charge transfer will be reconstructed but displaced in time from the input. In essence, extraneous pulses have been created. Figure 11 shows the input and output of the overlapping clock configuration.

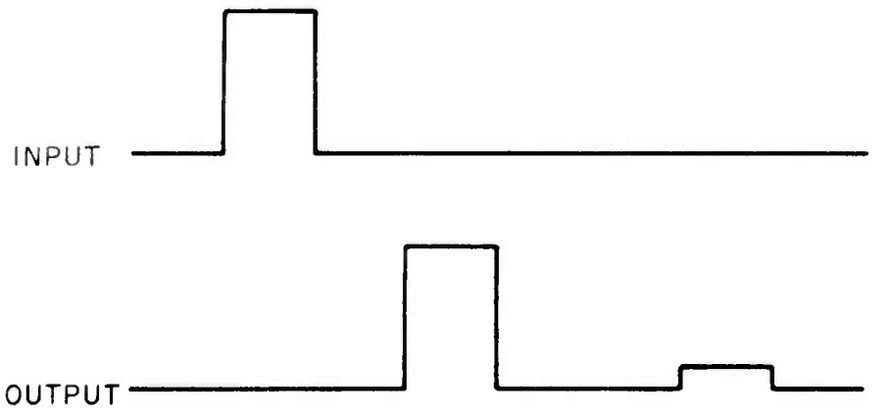


Figure 11. Input and Output of Overlapping Clock Configuration

The magnitude of the extraneous pulse depends on the charge transfer inefficiency while the relative delay time between the pulses is determined by the number of parallel CTD's (for a given clock frequency).

At the start of the contract when a decision was being made as to which multiplexing method to use, several other factors were also considered. Only a few chips were available for evaluation at that time. These chips contained 100 stages and could be clocked between 1 and 2 MHz with

a bandwidth between 500 and 1000 KHz. These chips were the best of a batch that had been processed earlier. Two of the problems at this time were the nonuniformity of devices and the low yield which could be expected from a particular batch. The problem of nonuniformity was evident in two different areas: (1) the "pattern noise" mentioned earlier; and (2) the matching of CTD characteristics from device to device. Since the uniformity between devices tends to degrade when operation is near the clock frequency limit, it was decided to use a lower frequency. Consequently the overlapping clock mode was chosen. Processing problems were encountered when building the large number of devices required for the contract, and device operation would have been marginal at the higher clock frequency required for gated clock operation. Figure 12 displays the performance obtained from a typical sample of devices.

The problem of the extraneous pulse in the overlapping clock mode evidenced itself; however, since, with the required clock frequency, the pulse range delay is approximately one-third of a mile and the amplitude is 12 to 20 db below the main pulse, this did not appear to be of significance on a PPI presentation except for very large magnitude moving targets. In the case of clutter returns, the extraneous signal bears a precise relationship to the clutter patch and cancels as an entity. The transfer efficiency of future devices is expected to improve by at least a factor of ten, practically eliminating this effect.

Two circuit implementations can be used to build a three-pulse MTI. These circuits are shown in Figure 13. In practical systems, the circuit of Figure 13b has several advantages. Each section can be adjusted independently to give the best cancellations. Also since the sections are independent, the entire canceller is not as sensitive to component changes. For these reasons, the circuit of Figure 13b was used, with a slight modification. Since the charge transfer device has a sampled data output, the subtractors would be comparing a continuous signal with a sampled data signal. This means that each sample at the output would match the input at only one point on the waveform, thus making the circuit more sensitive to any clock jitter or other circuit variations. To provide better matching, it was easier to compare two sampled data signals rather than reconstruct the output. Thus a tap was used on the CTD for the undelayed signal. This is shown in Figure 14. A fixed delay associated with the undelayed path must be compensated in any video gating circuits.

From Figure 6, it is evident that the comparison at the subtractor is between a square pulse which is present at the tap and a rounded pulse which is present at the output of the CTD. After subtraction the signal would appear as shown in Figure 15.

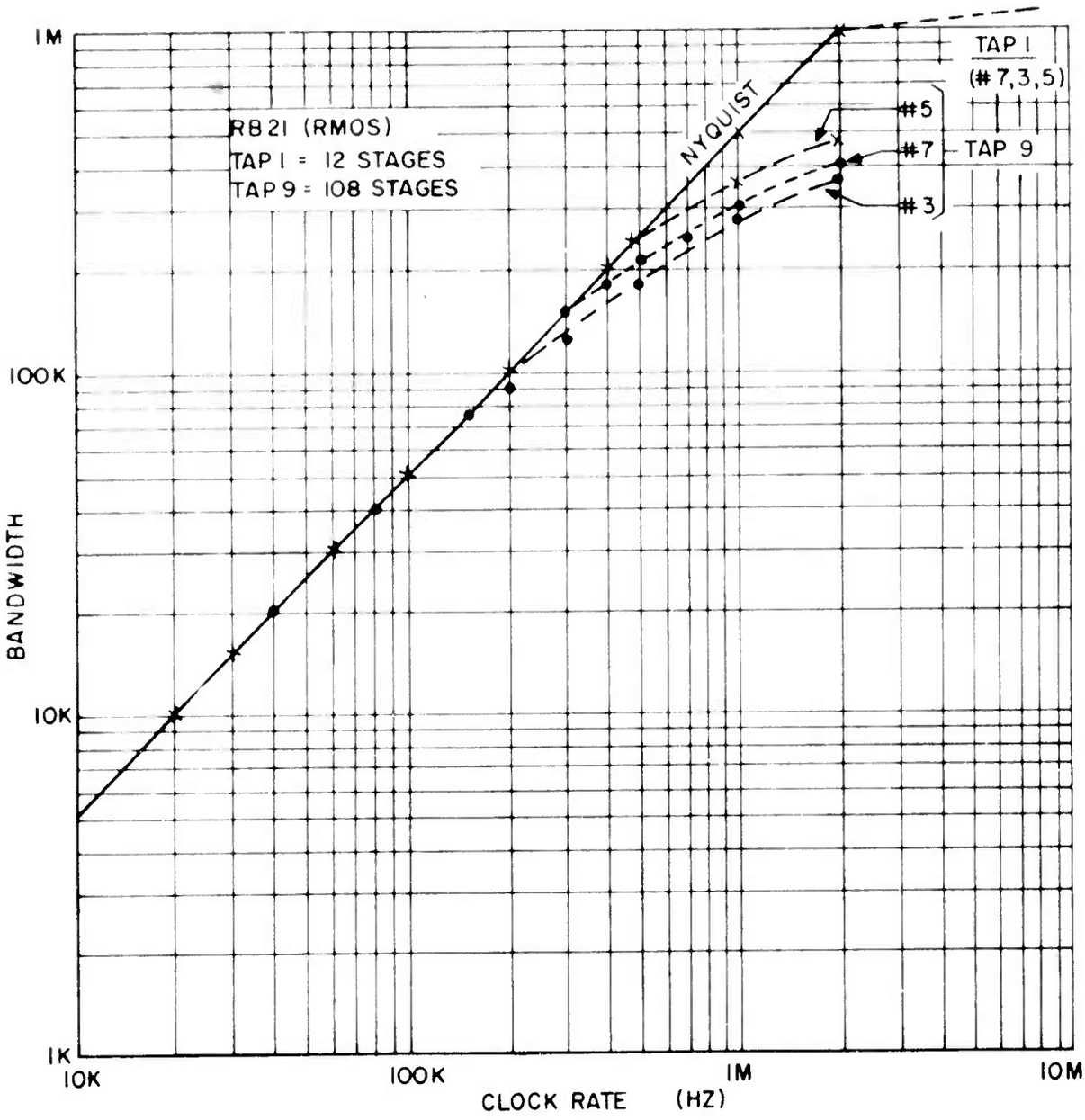


Figure 12. Clock Rate vs. Bandwidth for Typical Sample of Devices

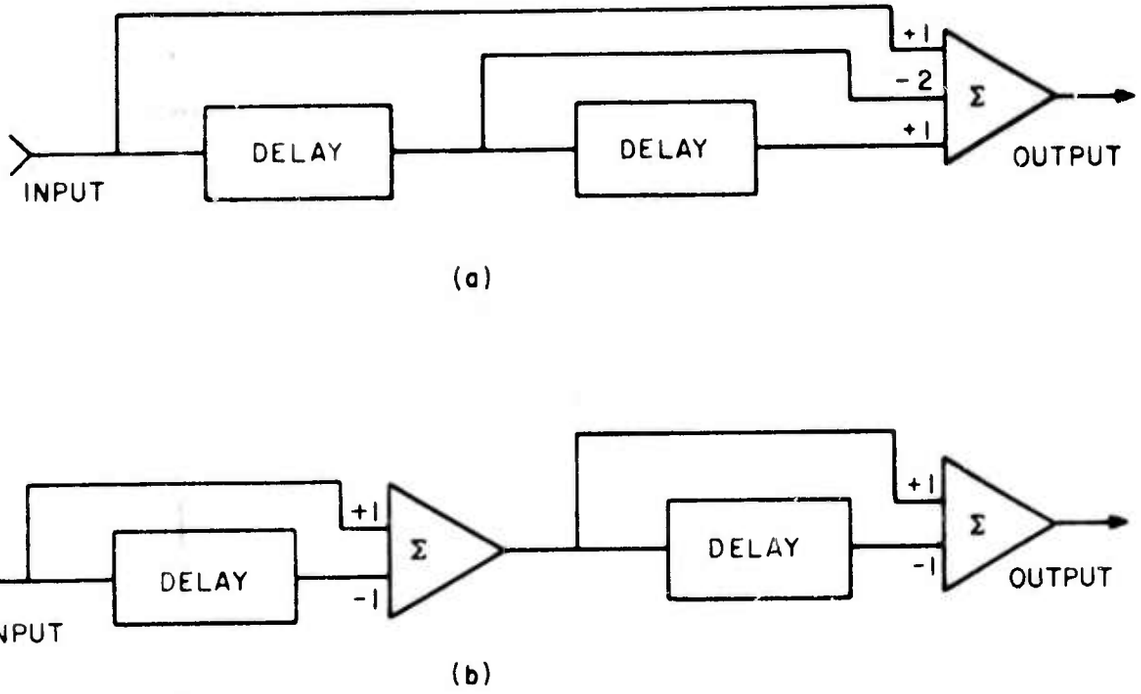


Figure 13. Three-Pulse MTI Circuits

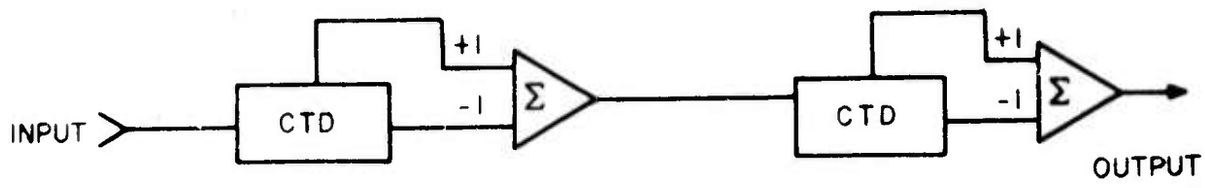


Figure 14. CTD MTI with Tap

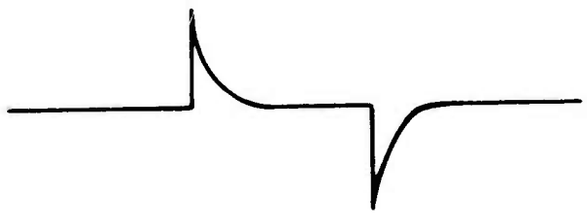


Figure 15. Subtractor Output without Compensation

The tap and output can be matched in the middle of the pulse to achieve good cancellation but the leading and trailing edges are only down about 26 db. To alleviate the problem, a compensation network is placed in the undelayed signal path to round off the undelayed pulse. The compensation network consists of the low pass filter shown in Figure 16.

Timing signals S_{11} and S_{12} determine the start of each burst. Timing signals S_{21} and S_{22} are generated by the quartz analog delay line and are used to trigger the transmitter at the start of each PRI. Since the discrete signal MTI is to replace the analog MTI, new timing signals to trigger the transmitter are required. The original radar setup is not fully coherent in that transmitter triggers S_{21} and S_{22} are not phase-locked to the transmitted signal. Since it is desirable to have the PRI locked to the master oscillator, it was decided to use the 52 MHz local oscillator as the master clock for the CTD MTI.

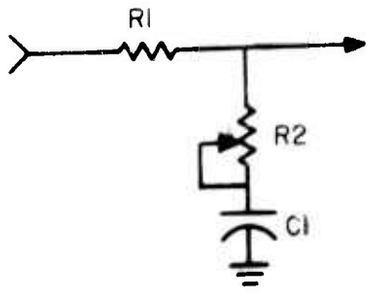


Figure 16. Compensation Filter

(The value of C1 is determined by experiment along with adjusting R2 to give the best cancellation across the pulse.)

2. INTERFACE DESIGN

The RADC Test Bed Radar is a dual-burst radar with a staggered PRI. The timing diagram is shown in Figure 17.

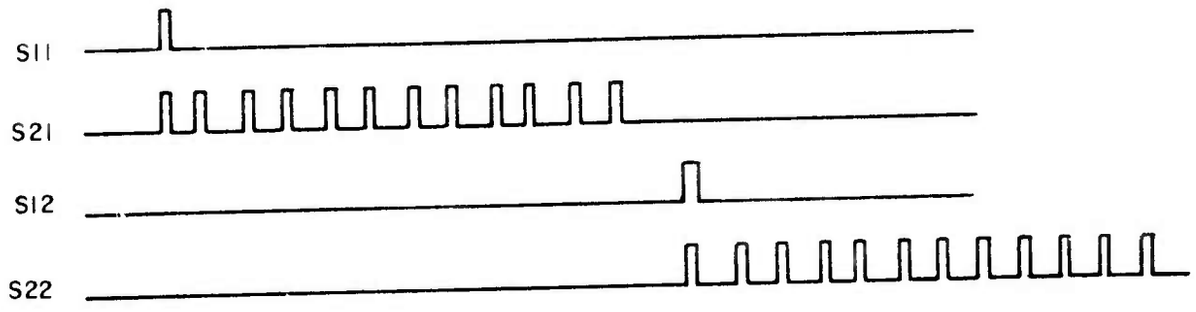


Figure 17. RADC Test Bed Radar Timing Signals

Thus the CTD clock frequencies and transmitter triggers are obtained from the 52 MHz LO by counting down by the appropriate numbers. The original burst triggers S_{11} and S_{12} are used since the timing between bursts is not critical. However, if in the future, it is desired to phase lock the burst, this could be accomplished by incorporating additional counters on the logic board of the discrete signal MTI.

The additional interfacing required is to provide the desired signal outputs as specified in Table II.

SECTION V

TESTING

1. TEST TECHNIQUES

The filter response of a moving target indicator is shown in Figure 18.

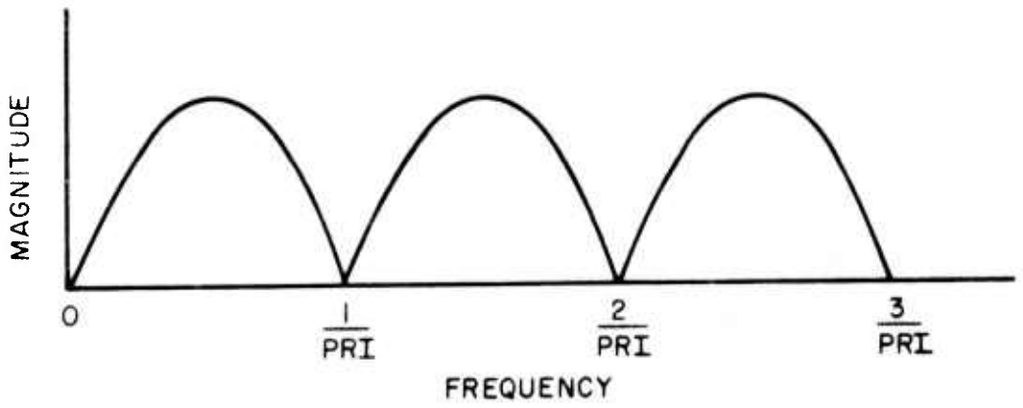


Figure 18. MTI Filter Response

The cancellation ratio (CR) may be defined as the maximum voltage magnitude divided by the minimum voltage magnitude and is usually expressed in decibels (db). Since the PRF is equal to 1/PRI, the minimum signal can be found by inserting a signal at the PRF and the maximum signal can be found by inserting a signal at one half the PRF. Figure 19a shows the test signal necessary to give the maximum response. Since the phase changes by 180 degrees at each PRI, the delayed and undelayed inputs to the subtractor reinforce at the output. In Figure 19b, the test signal has the same phase at each PRI and the signals cancel, giving a minimum. The shaded pulses in Figure 19b are not present in a radar system; however, it was convenient for testing to generate the signal in Figure 19a by dividing the signal of Figure 19b by two. Since the shaded pulses are a PRI apart, they also cancel.

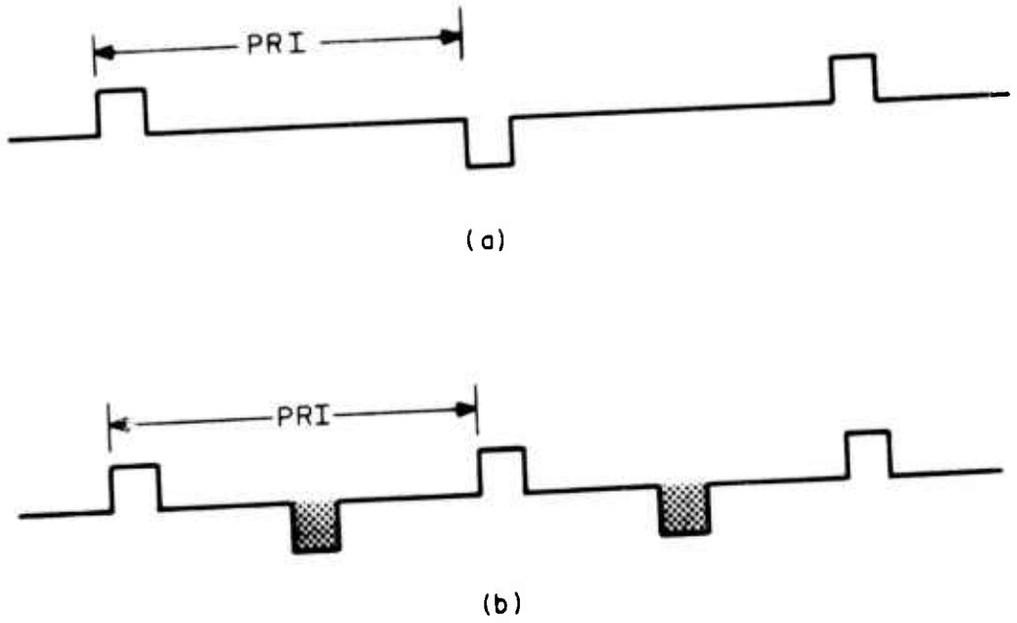
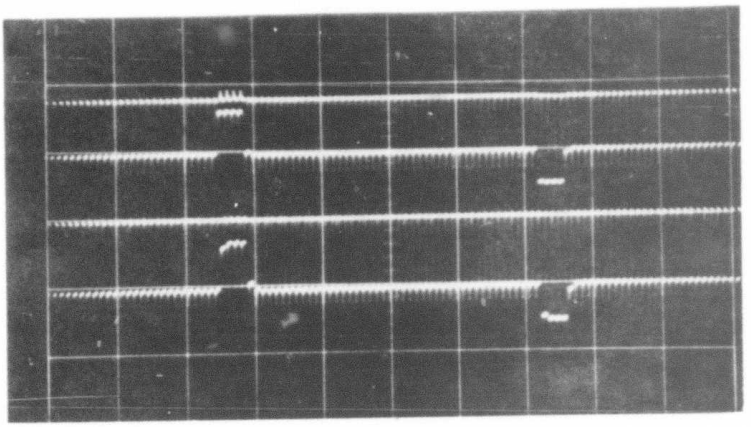


Figure 19. MTI Test Signals

2. TEST RESULTS

For the final MTI, eight parallel three-pulse channels were multiplexed using the overlapping clock mode of operation. During the design a single three-pulse channel was built and tested to evaluate the performance of the charge transfer devices. The clock frequency of the CTD's is the same as the final circuit but the input pulse is widened to demonstrate the type of operation where a single CTD device would be used for the entire delay. Figures 20 and 21 show the results of these tests.

Figure 20a shows the undelayed and delayed pulses. The bandlimiting of this device is much less than that of Figure 6b. Figure 20b shows the output of the sample-and-hold circuit which is used to reconstruct the subtracted signal, and also the output of a low-pass filter which smooths the reconstructed signal. Figure 21a shows the input signal of the required frequency to give the maximum output. In Figure 21b, the input frequency is

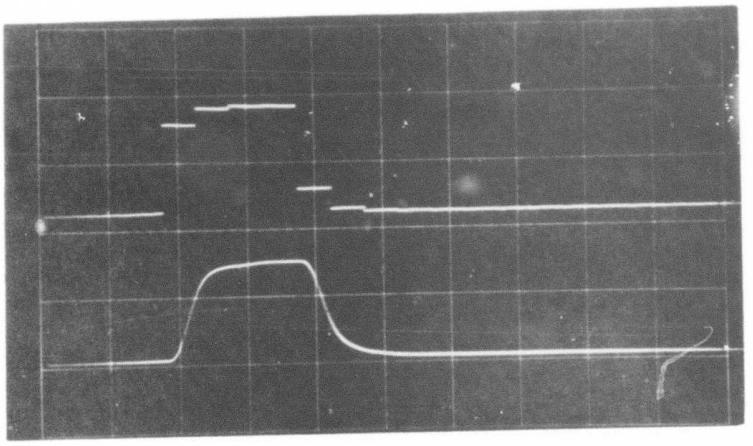


(a)

Tap at 12^{th} Stage

Tap at 108^{th} Stage

Horizontal Scale 50 μsec/cm
Vertical Scale 2 v/cm



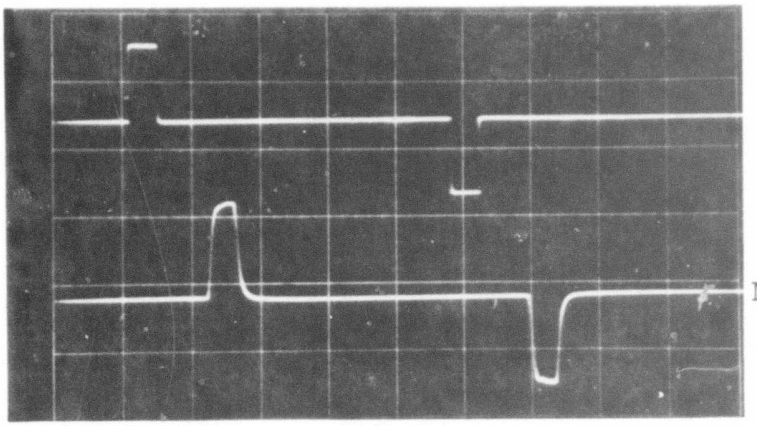
(b)

S/H Output

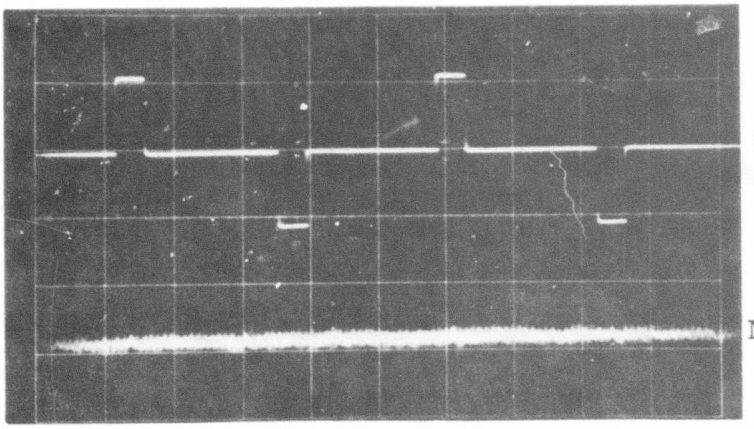
Filter Output

Horizontal Scale 10 μsec/cm
Vertical Scale 1 v/cm (Top Trace)
0.5 v/cm (Bottom Trace)

Figure 20. Single Channel Output



Horizontal Scale 50 μsec/cm
Vertical Scale 2 v/cm (Top Trace)
0.5 v/cm (Bottom Trace)



Horizontal Scale 50 μsec/cm
Vertical Scale 2 v/cm (Top Trace)
0.005 v/cm (Bottom Trace)

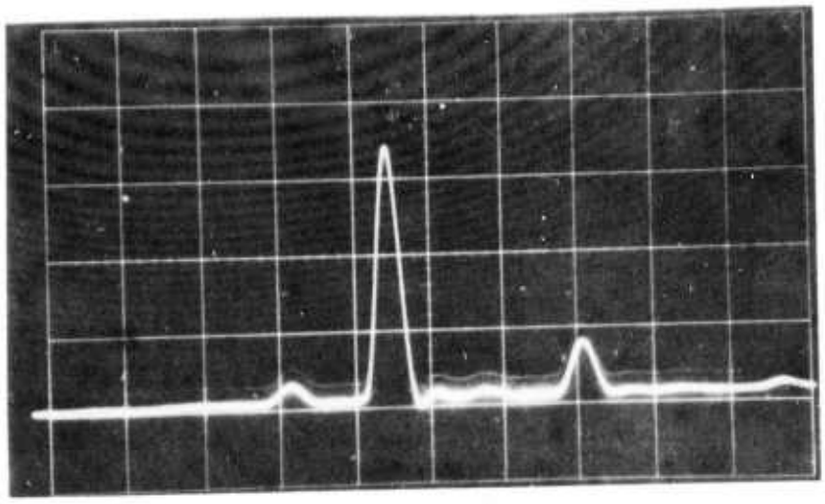
Figure 21. CR for a Single Channel

doubled and now the input pulses are one PRI apart and cancel. The cancellation ratio can be determined by dividing the maximum output by the minimum output. The maximum output is 1.3 volts peak to peak, the minimum is 0.0015 volt peak to peak. Thus the cancellation ratio is between 58 and 59 db.

When the eight parallel channels are multiplexed, a 1 μsec input pulse is used to simulate the radar. Since only one channel samples the input at a time, a variable time delay is incorporated in order to shift the input so that each channel can be tested. Figure 22 shows the output of the "in-phase" section of the MTI (the quadrature section is identical). The maximum signal is 1.3 volts peak to peak and the minimum is 0.004 volt peak to peak. Thus the cancellation ratio is between 50 and 51 db. It is evident that for the multiplexed channels the cancellation ratio has been reduced. The principal reason is shown in Figure 22b. It is difficult to adjust the parallel channels so that the dc offset is exactly balanced. Any bias supply variations or temperature variations can cause small dc shifts which are not necessarily the same in every channel. The maximum signal cannot be increased due to saturation of the charge transfer devices, so that the only way to increase the cancellation ratio would be with more sophisticated dc compensation. It should be pointed out that the problem of dc balance would also be present in the gated clock mode of operation.

In Figure 22a two extraneous pulses are present, one leading and one trailing the actual input signal. The trailing pulse is a result of the charge transfer inefficiency of the CTD's which is discussed in Section IV.1. The leading pulse is partially the product of the multiplexing scheme and partially the product of the CTD and associated clocks. The charge transfer devices are operated with two phase clocks as noted previously. One phase is turning on while the other phase is turning off and vice versa. Thus, two of the eight channels will have clocks which are 180 degrees out of phase. This is illustrated in Figure 23. Channels one and five are used for the illustration with channel one taking the desired sample. However any two channels separated by a distance of four will give the same result.

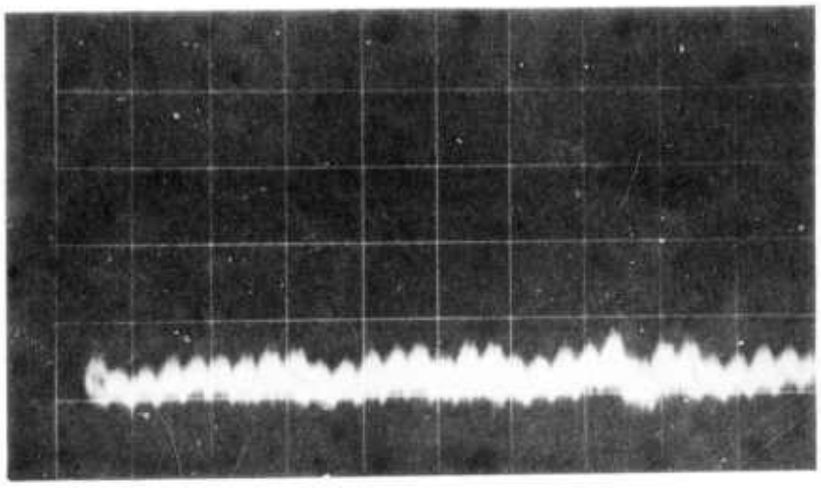
The arrows on the switches indicate the direction at the start of the discussion. Switches T11 and T_{S2} have been closed and are transferring charge. As T11 and T_{S2} start to open, T12 and T_{S1} start to close. However, the switches turn on slightly faster than they turn off. This means that adjacent switches are on together, for a short period of time, allowing a small amount of undesired charge to be placed on capacitor C_{S2}. This charge will



(a)

Uncancelled

Horizontal Scale 2 μsec/cm
Vertical Scale 0.2 v/cm



(b)

Cancelled

Horizontal Scale 2 μsec/cm
Vertical Scale 0.005 v/cm

Figure 22. In-Phase Output

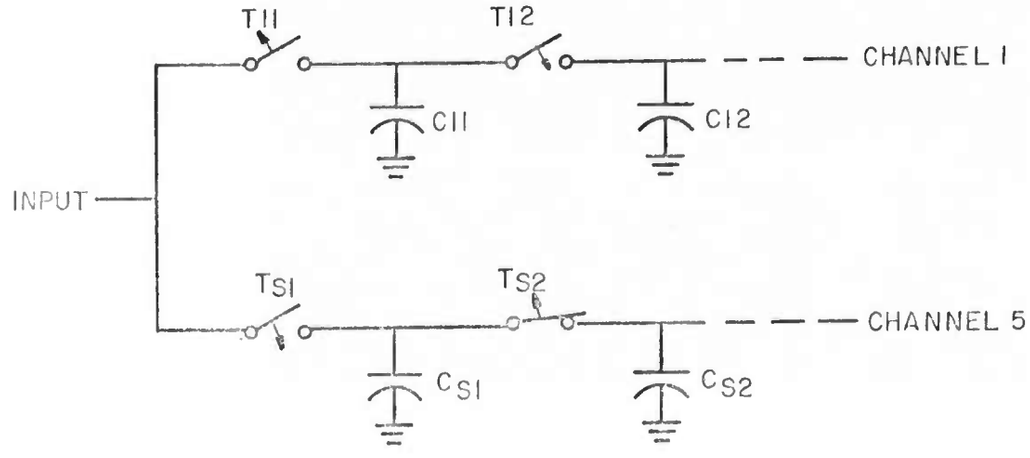
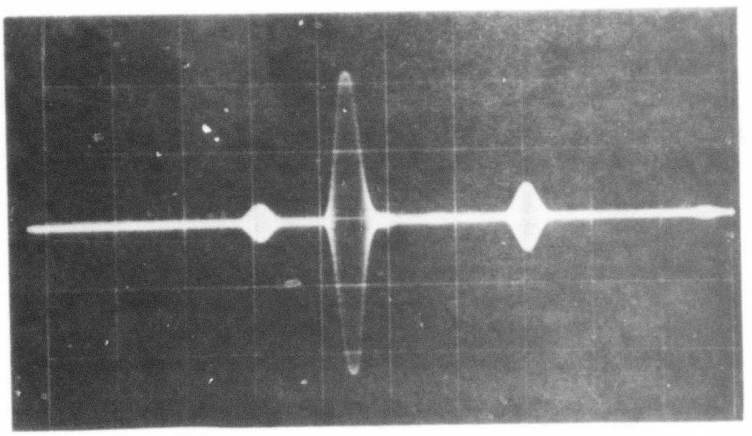


Figure 23. Two Parallel Channels

propagate down the CTD and, when demultiplexing occurs, will appear at the output ahead of channel one since the input state was bypassed on channel five and the charge placed directly on C_{S2}. Some reduction of the pulse was achieved by skewing the CTD clock voltages slightly with respect to one another to decrease amount of charge transferred to C_{S2}, but total elimination was not possible without increasing the charge transfer inefficiency.

Figure 24 shows the IF and video outputs. (Figure 24a is the uncancelled IF, while Figure 24, b and c, show the video uncancelled and cancelled outputs, respectively.) The IF signal is obtained by recombining the I and Q outputs at 52 MHz and the video output is obtained by detecting the IF signal.

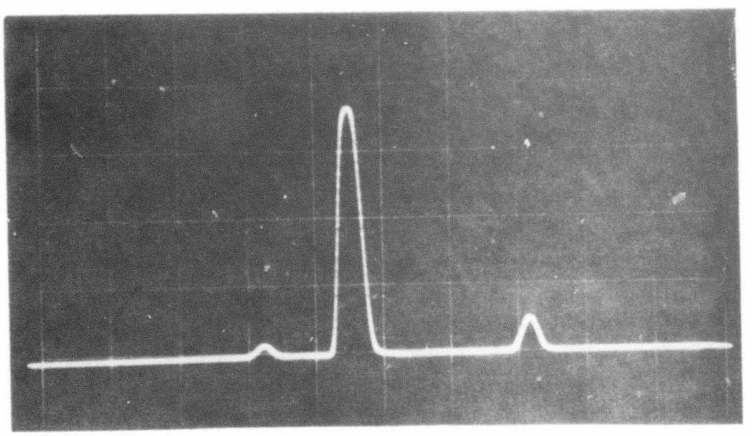
Figure 25 through 28 show the results obtained when the Discrete Signal MTI is incorporated into the RADC Test Bed Radar. These photographs were all taken on the same day (26 June 1974) from the display on the Plan Position Indicator (PPI). However, the photographs were not all taken at the same time so that, because of the short range and high aircraft speeds, direct correlation between targets in different photographs is unfortunately not possible. Figures 25 through 27 are photographs of one sweep of the PPI while Figure 28 is a photograph of four sweeps of the PPI. The range in each figure is 0 to 14 miles.



(a)

IF Uncancelled

Horizontal Scale 2 μsec/cm
Vertical Scale 0.005 v/cm

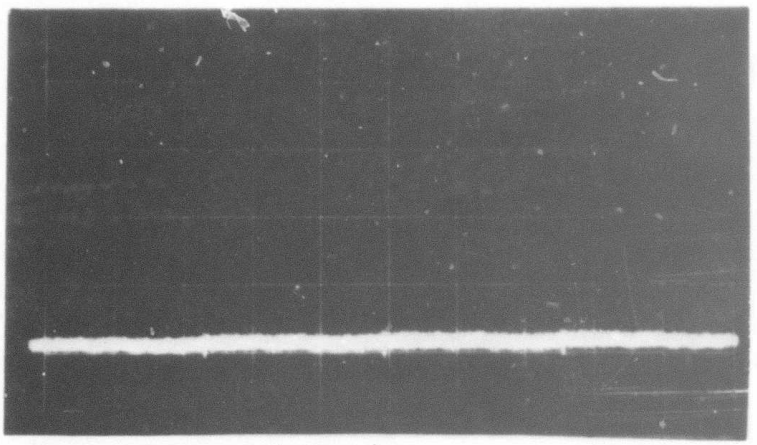


(b)

Video Uncancelled

Horizontal Scale 2 μsec/cm
Vertical Scale 0.5 v/cm

Figure 24. IF and Video Outputs (Sheet 1 of 2)



(c)

Video Cancelled

Horizontal Scale 2 μsec/cm
Vertical Scale 0.005 v/cm

Figure 24. IF and Video Outputs (Sheet 2 of 2)

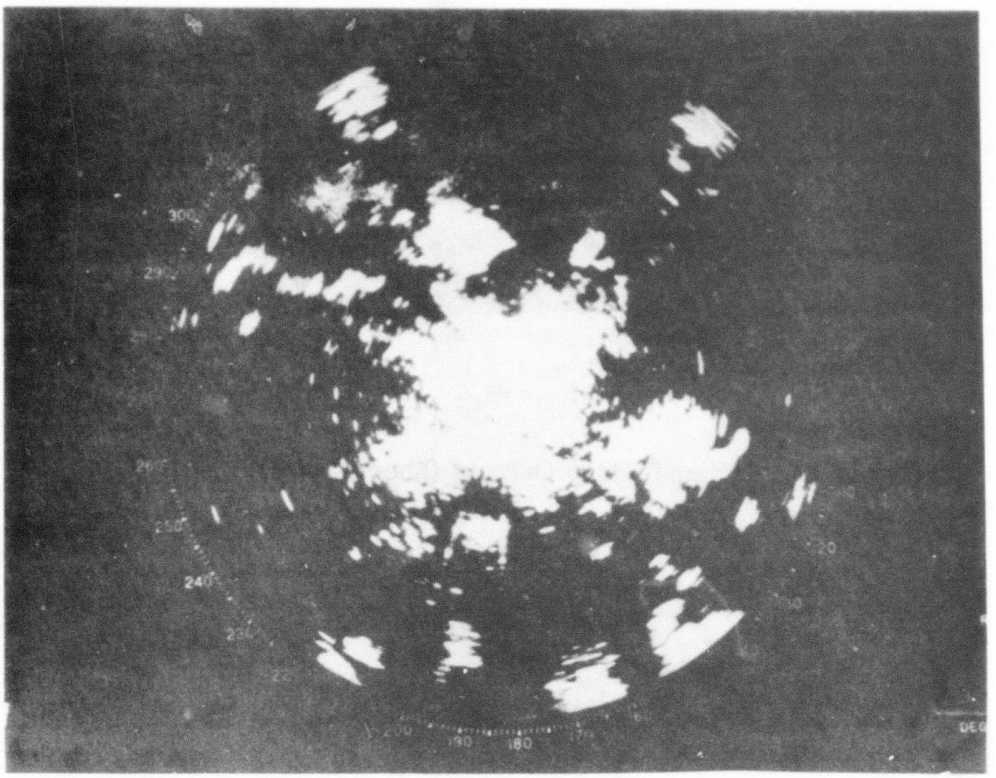


Figure 25. Clutter Map for RADC Test Bed Radar when MTI is Bypassed

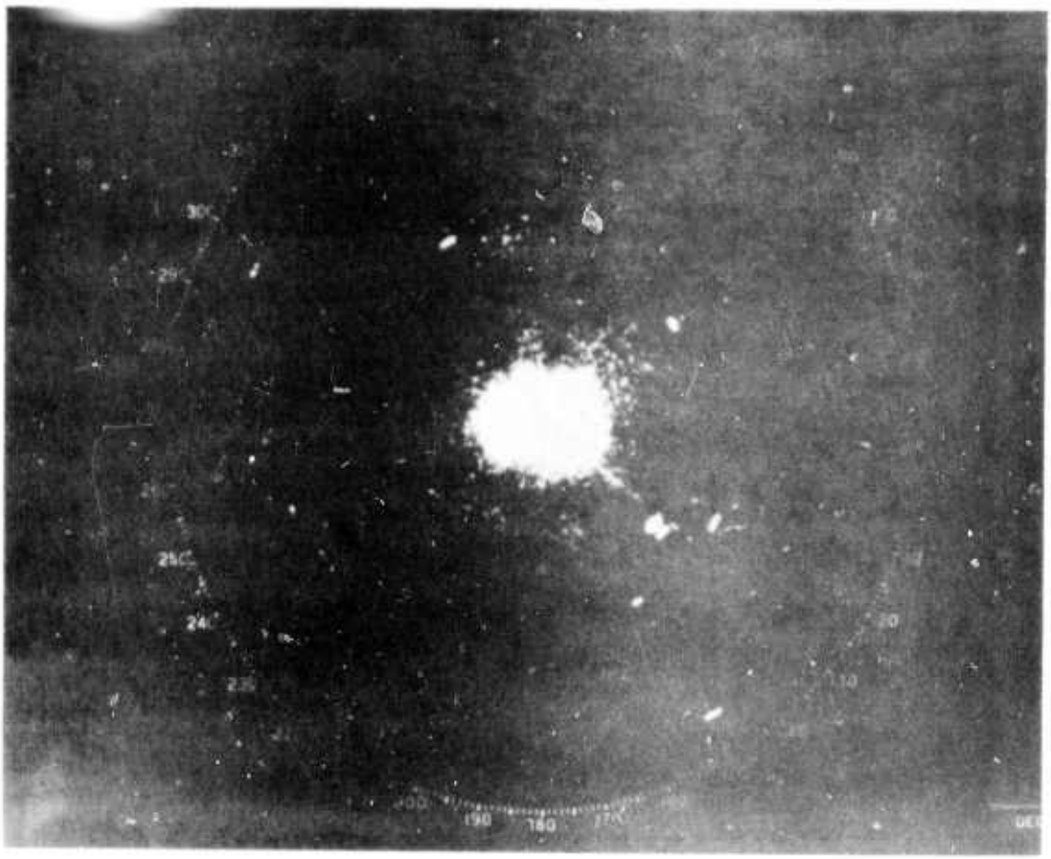


Figure 26. PPI Display for PADC Test Bed Radar Showing Effects of Variation in Strength of Target Returns

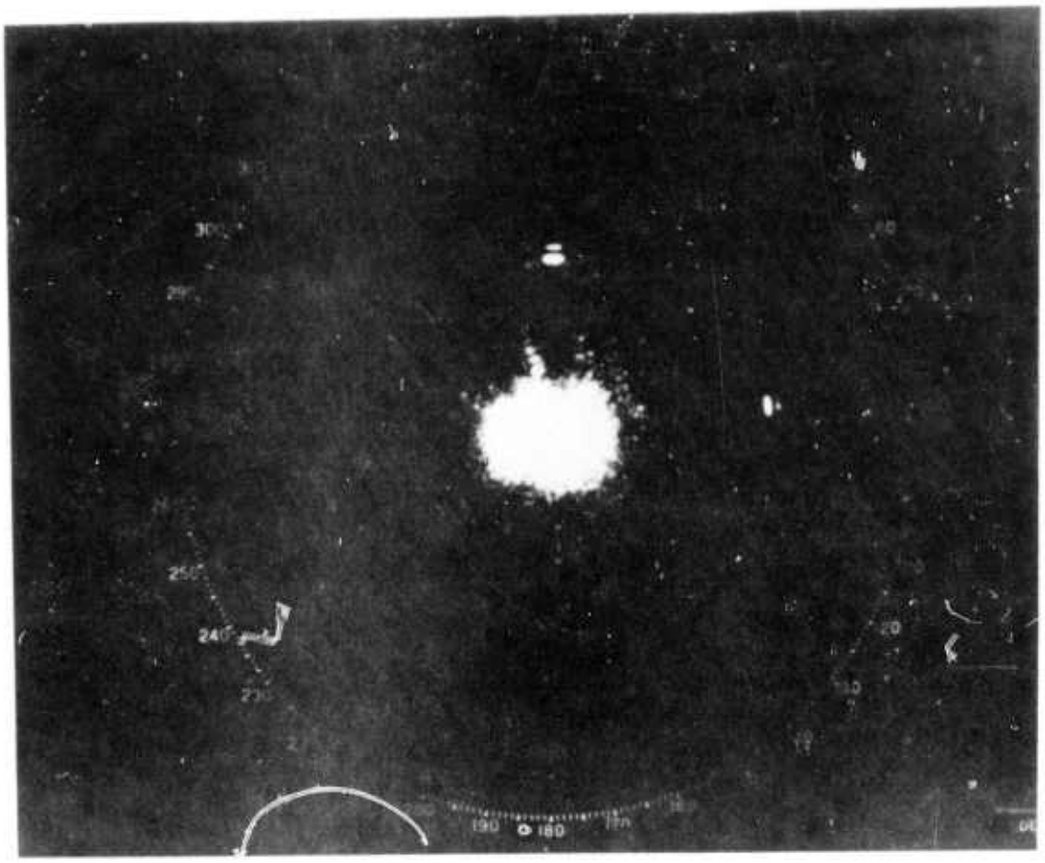


Figure 27. PPI Display for RADC Test Bed Radar Showing Enhancement Effect of MTI (Target at 347° would be undetectable without MTI)

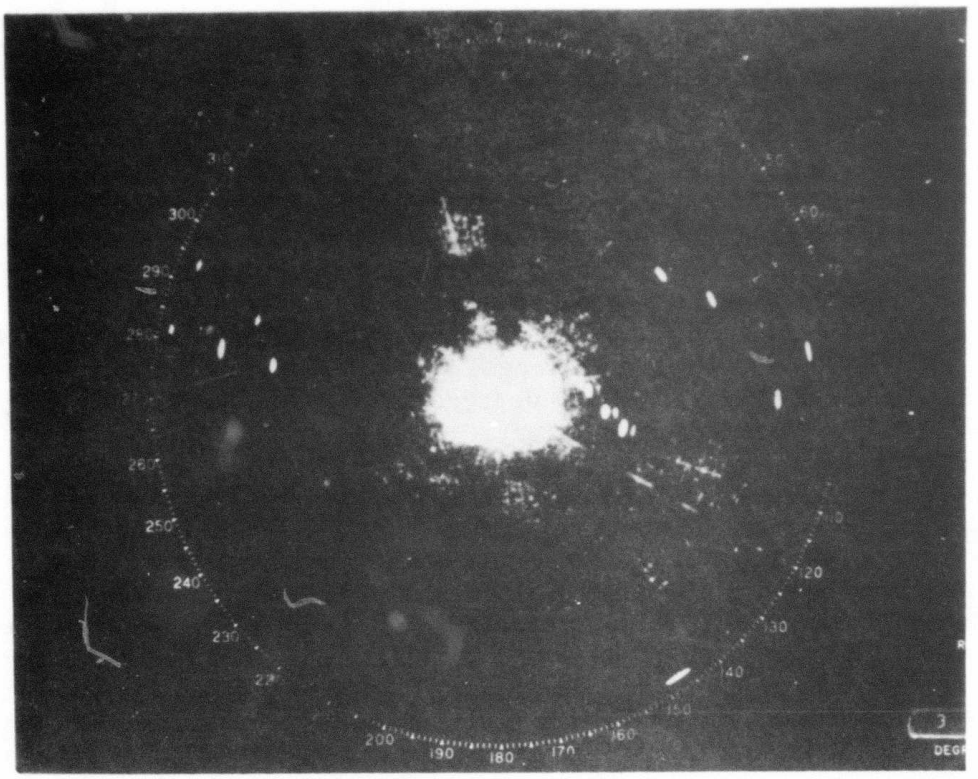


Figure 28. PPI Display for RADC Test Bed Radar Showing Four Sweeps

Figure 25 shows the clutter map which is obtained when the MTI unit is bypassed and the rest of the radar system is operating normally. A reference for the clutter strength can be obtained from a hill, located between 335 and 355 degrees at a range of 5 to 8 miles, which has a strong clutter return (60 db above noise). Also shown in Figure 25 are four targets (86 degrees at 7 miles, 95 degrees at 12 miles, 168 degrees at 6 miles, and 249 degrees at 13 miles) and a rainstorm which is located between 310 and 350 degrees at 10 to 12 miles.

Figure 26 through 28 are photographs of the PPI display when the MTI is incorporated into the radar system. From examination of the clutter reference, it can been seen that clutter cancellation is very good. The uncancelled residue in the center of the PPI display comes from very strong clutter returns (greater than 60 db above noise) close to the radar. The weaker targets may be second or third-time-around targets. Figure 26 shows the effects of variation in the strength of target returns. For very strong returns such as the target at 132 degrees and 6 miles, the trailing extraneous pulse shows up as a false target.

For weaker target returns such as the one at 148 degrees and 13 miles, the extraneous pulse does not come through. Thus the extraneous pulse may not show up at all, or if it does, it is always in conjunction with a very strong target return. Because of this fixed relationship, the extraneous pulse is easily recognized as a false target. Figure 27 shows three targets with the one at 347 degrees and 2 miles being undetectable without the MTI. Figure 28 shows four sweeps of the PPI. Although the cancellation residue is enhanced (because of the integration effect of the four sweeps) the movement of the targets from sweep to sweep can be observed. Most evident is the target between 85 and 102 degrees at 3 to 5 miles which is coming in.

SECTION VI

SYSTEM OPERATION AND ALIGNMENT

1. GENERAL

Figure 29 is a general block diagram of the Discrete Signal MTI. The system is divided into four major sections: the logic board, input/output board, canceller boards, and the up-converter/detector unit. Appendix A contains the schematics for these sections, which should be consulted for the discussion which follows. Appendix B lists the parts used in the system. Views of the completed MTI and three of the boards are presented in Appendix C. Figure 38 of Appendix C demonstrates that, even though the MTI was built for ease of investigation, it is quite compact.

2. THEORY OF OPERATION

The theory of operation presented here is a broad-brush treatment only.

The I and Q baseband signals are received from the radar synchronous demodulator, and are sent to the input/output board. There they amplified, buffered and sent via a common line (one each for I and Q) to the eight canceller boards. Each of the canceller boards has a three-pulse canceller for I and a three-pulse canceller for Q which are driven synchronously. After cancellation, the I and Q signals are returned (along separate lines) to the input/output board to be demultiplexed. Following the demultiplexing, a sample-and-hold operation is performed to reconstruct the sampled data signals. After reconstruction the signals are gated, filtered and then split so that one set of I and Q signals is sent back to the radar at baseband while the other set is sent to the up-converter/detector unit to reconstitute the 52 MHz I F. The IF signal is then split with one signal being attenuated and sent to the radar as a -30dbm IF signal while the other signal is detected and provides the unipolar video output.

The logic board generates the two-phase CTD clocks and provides the timing for all of the internal functions. In addition, the logic board provides transmitter timing signals for the radar as described previously.

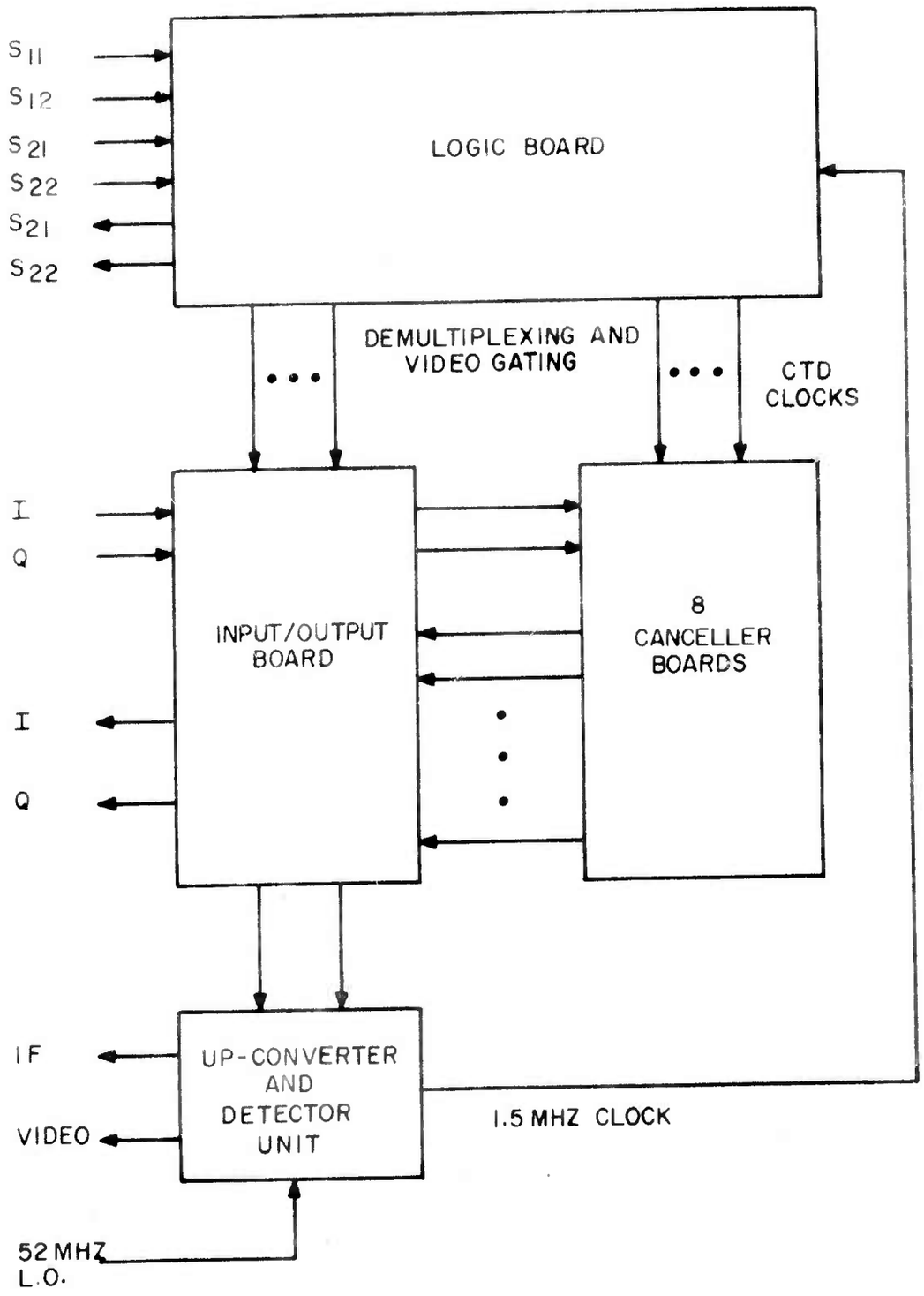


Figure 29. Discrete Signal MTI Block Diagram

3. ALIGNMENT AND TROUBLESHOOTING PROCEDURE

Figures 32 through 37 (see Appendix A) are the schematics of the Discrete Signal MTI. The following alignment procedures will reference these schematics. No calibration is normally required; however, an occasional check of the I and Q channels is recommended to insure that the dc balance between the eight parallel channels is being maintained. If adjustment is needed the procedure is as follows: Turn on the equipment and, after a warm-up period of at least 15 minutes, observe the I and Q outputs with no input. A 10-kilohm potentiometer is provided in each channel for dc balance adjustment. It is located in the bias network of the 2N2222 output transistor (Figure 35, Sheet 2). If only one channel is unbalanced, it is sufficient to find the appropriate channel and adjust the potentiometer. If several channels are unbalanced, it is recommended that a reference point be established by looking at the output of the SHM-UH sample-and-hold circuits (see Figure 34, Sheet 1). At this point, each channel can be adjusted for a zero volt dc level.

If a charge transfer device needs to be replaced the procedure is as follows: Place the particular canceller board on an extender board. Insert a 1 volt peak to peak test pulse into the appropriate I or Q channel. Then adjust the 50 kilohm bias potentiometer at the input of the CTD so that the output of the CTD is not limiting in either the positive or negative direction. After the bias is properly adjusted, the compensation circuit in the undelayed path must be adjusted for best cancellation. This can be accomplished by looking at the appropriate I or Q output and adjusting the 10K potentiometer and capacitor C* (in Figure 34) until best cancellation is achieved.

The logic section does not require any adjustments. The timing diagram of Figure 30 is provided to assist in troubleshooting if equipment malfunction occurs. Upon application of power to the equipment, a reset signal is generated by the SN7413 Schmitt trigger in Figure 32, Sheet 2 to clear all logic circuits. When the reset signal returns high, the range clock (1.5 MHz) and radar burst triggers are enabled. The range clock serves two functions. In one function, the range clock runs continuously and generates the CTD clocks and demultiplexes timing signals from the SN74164 shift registers in Figure 32, Sheet 1. In the other function the range clock is gated on during the burst to generate transmitter triggers S_{21} and S_{22}. This is accomplished by the three 9316 counters in Figure 32, Sheet 2. At the end of each burst, the initialize signal is generated which presets these counters for the next burst. As an added feature, transmitter triggers S_{21} and S_{22} are used to generate an internal test signal (selectable from the front panel) which can be used to check system cancellation performance.

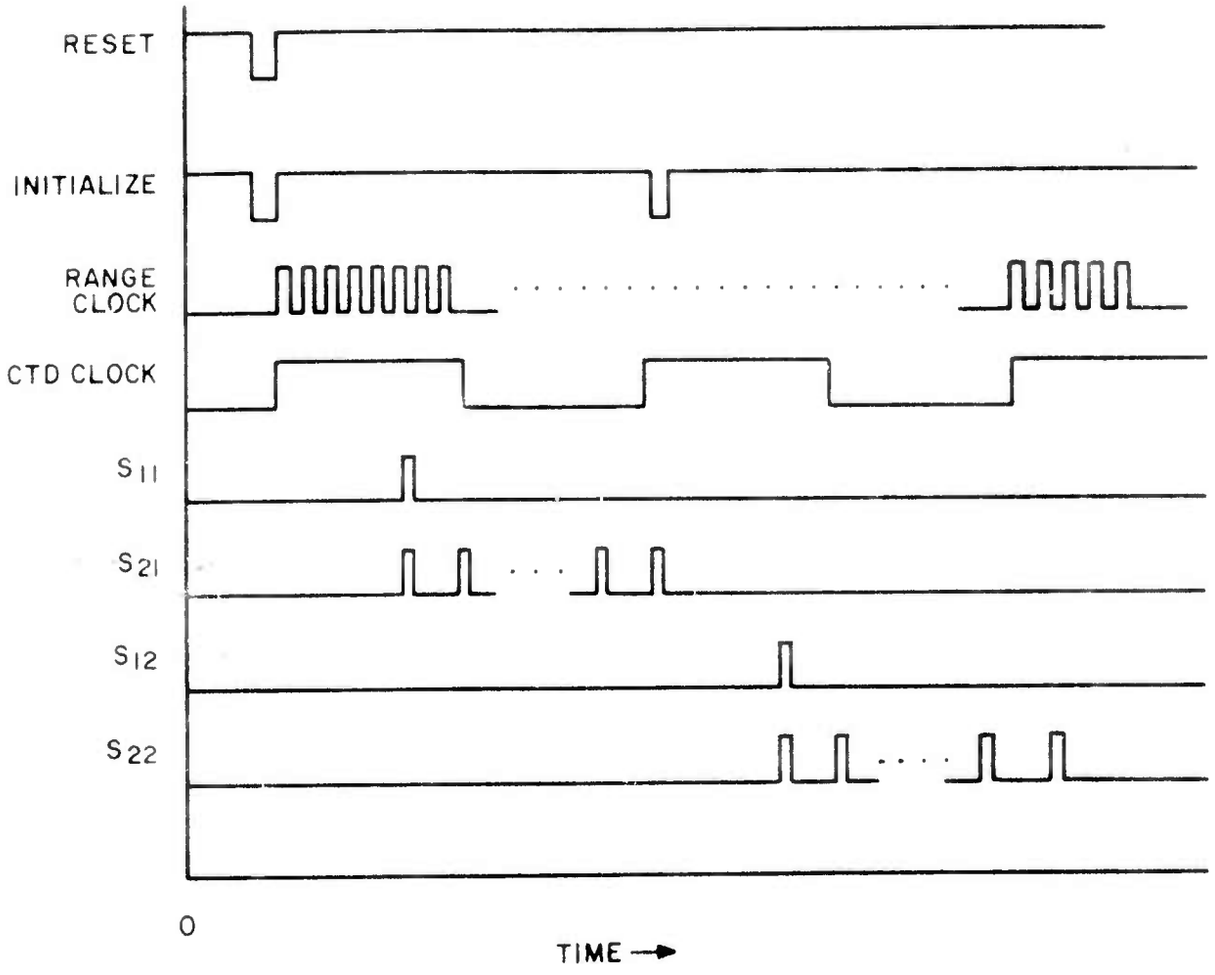


Figure 30. Logic Timing Diagram

The power supplies are overvoltage and current protected and require no maintenance. If problems develop, the manufacturer's operating manual should be consulted.

The up-converter/detector unit requires no calibration. For convenience, a limit level and gain adjustments are provided to control the video output amplitude.

SECTION VII

CONCLUSIONS AND RECOMMENDATIONS

It is evident from the test results that charge transfer devices can be used to implement an MTI with excellent clutter cancellation capability. Advances in the device state of the art should make it less necessary to utilize complex multiplexing for next generation systems with similar parameters. However, if this type of technique needs to be implemented to extend the time-bandwidth product for a particular application, the leading extraneous pulse can be eliminated by inserting an analog switch in front of each parallel channel and actuating the switch for only the period of time directly before the CTD takes a sample. The trailing extraneous pulse can be reduced, but not necessarily eliminated, by a transversal equalizer. Figure 31 shows an experiment performed with an available LC delay line whose rise time and delay were not exactly matched for best cancellation: however, the principle is illustrated. The trailing pulse can also be reduced directly in proportion to an increase in transfer efficiency, so that a factor of 10 improvement, which is reasonable, can reduce the trailing pulse an additional 20 db.

The state of the art in charge transfer, and charge coupled devices, remains very dynamic. A 160 stage JFET device operating at 6 MHz with a 3.3×10^{-3} transfer inefficiency has recently been reported by the General Electric Corporate Research and Development Center. Dr. Esser of Phillips has demonstrated a Peristaltic Charge Coupled Device (PCCD) operating at 135 MHz. Various other companies are actively pursuing large scale CCD's for use as computer main frame memories as well as part of the readout devices in solid state imagers.

The impact new devices would have on an MTI similar to the one demonstrated for this contract is shown in Table III. An estimate of size, weight and power for a production type design is included.

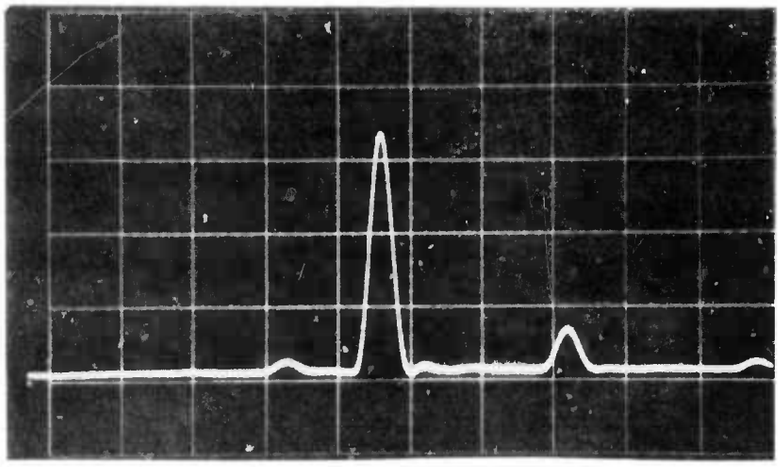
Recommendations for future work fall in two categories: (a) Improvements in device performance; i.e., transfer efficiency, dynamic range, and operating frequency, and (b) low cost implementation of signal processing functions. In the latter category, sidelobe cancellation compatible with MTI, Barker Code compressors with weighting, and correlator/transverse filter implementations using a special chip having built-in signal multiplication plus addition function are suggested. One might also consider an extension of the technology to implementing Z transforms. CR&D is in the process of demonstrating transversal filters on a surface charge transistor chip for this application.

TABLE III. DEVICE STATE OF THE ART IMPACT

	RMOS	JFET	PCCD
No. of Stages	108	160	128
Max. Sampling Frequency	1 MHz	>6 MHz	>100 MHz
Dynamic Range	60 db	60 db	>50 db
Volume (cu.ft.)	0.2	0.1	Applicable to high performance system
Weight (lbs)	6	4	
Power (Watts)	50 W	30 W	

The most direct extension of this work would be to achieve compatibility between a sidelobe canceller (SLC) and MTI. The availability of a controllable delay line (one whose precise delay can be automatically adjusted to match an existing MTI delay line) in conjunction with an additional adaptive control loop can make it possible to interconnect the SLC and MTI in such a way that the MTI removes ground clutter from the SLC feedback. Moreover, the modified SLC circuit can accurately cross correlate the auxiliary channel input with the output from the MTI. This capability alleviates the undesirable tendency of the SLC to operate on main beam clutter.

Since the exact delay of a CTD is determined by input clock signals, it is relatively easy to match the delay of an existing MTI delay line.

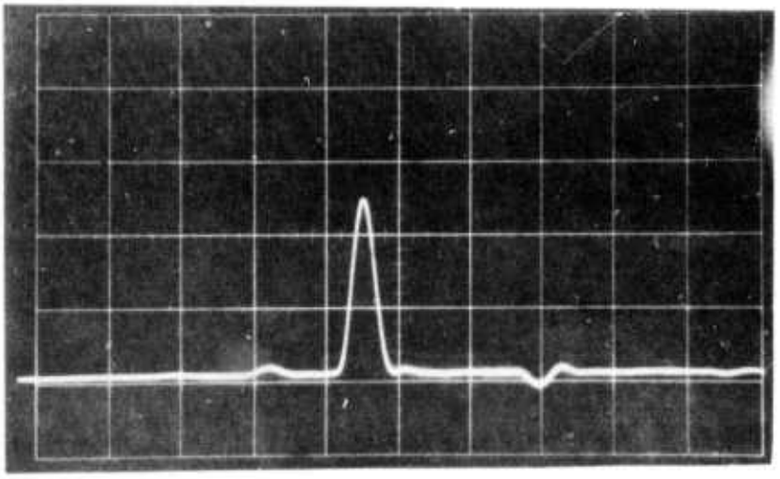


(a)

Q Channel

Uncancelled

Horizontal Scale 2 μsec/cm
Vertical Scale 0.2 v/cm



(b)

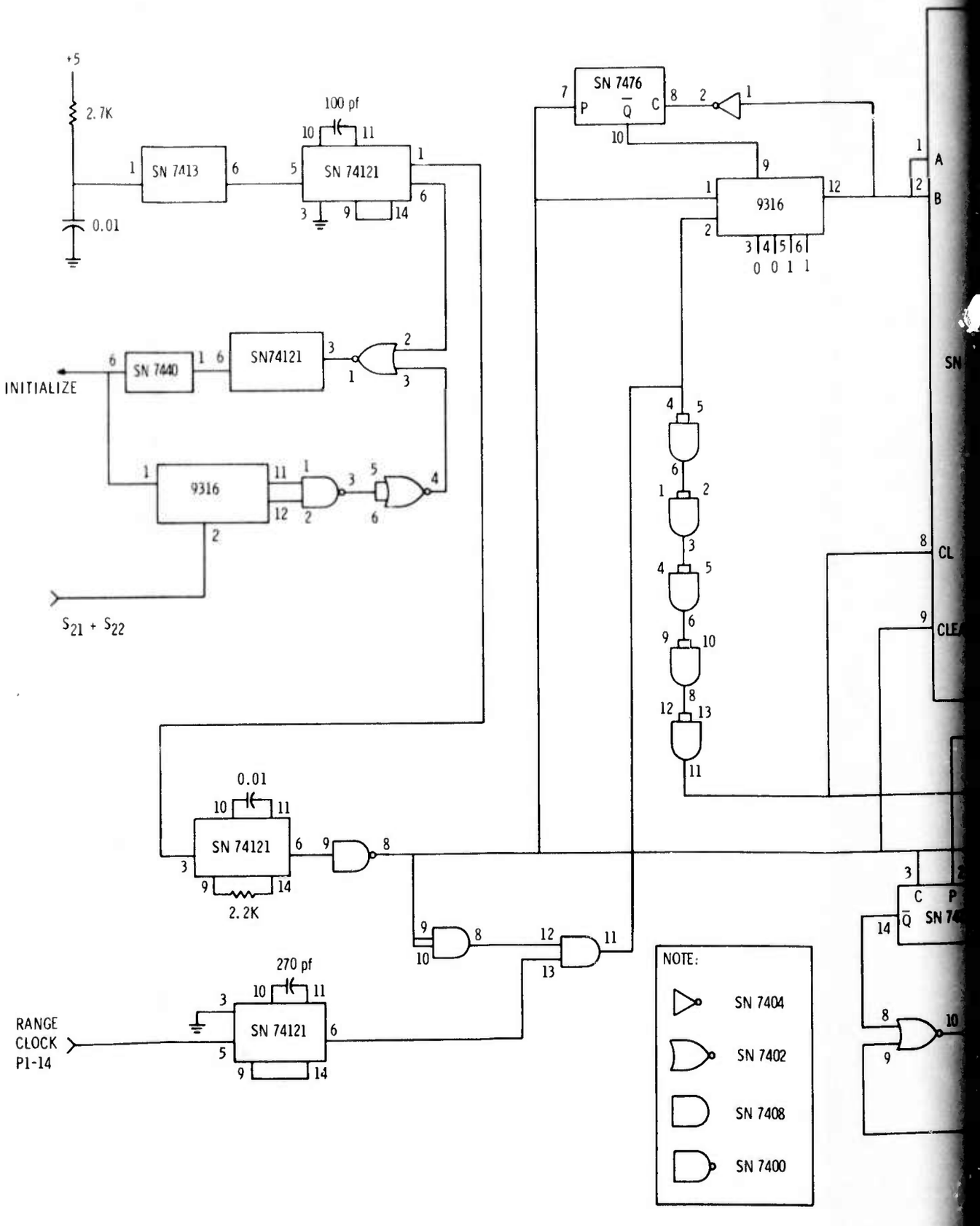
Q Channel (TE)
Uncancelled

Horizontal Scale 2 μsec/cm
Vertical Scale 0.2 v/cm

Figure 31. Results of Transversal Equalizer Experiment

APPENDIX A

SCHEMATICS


+5
2.7K
0.01
SN 7413
100 pf
SN 74121
SN 7476
P
Q
C
9316
0 0 1 1
A
B
SN
INITIALIZE
SN 7440
SN74121
9316
S_{21} + S_{22}
CL
CLEA
0.01
SN 74121
2.2K
270 pf
SN 74121
RANGE
CLOCK
P1-14
NOTE:
SN 7404
SN 7402
SN 7408
SN 7400

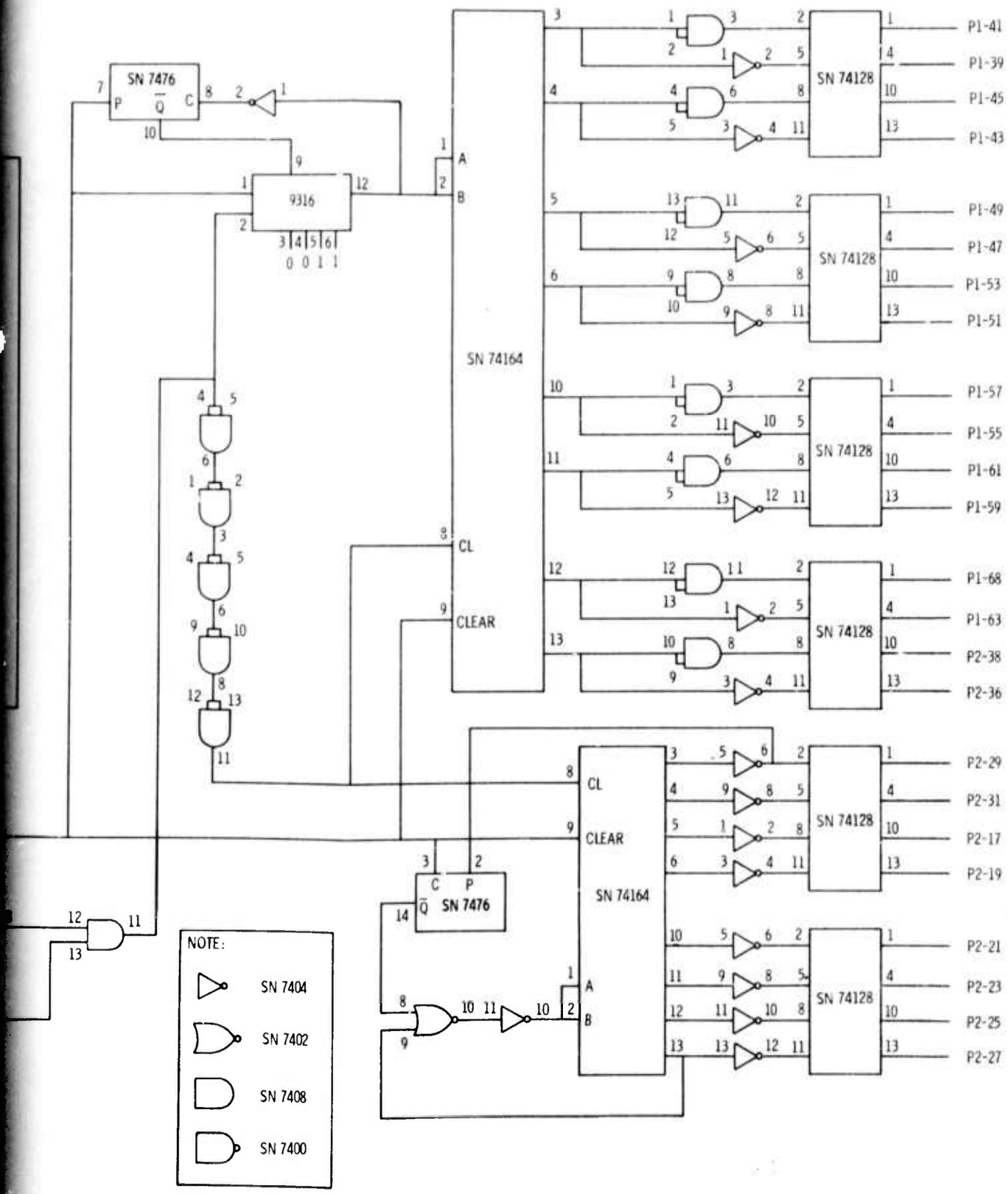


Figure 32. Logic Board (Sheet 1 of 2)

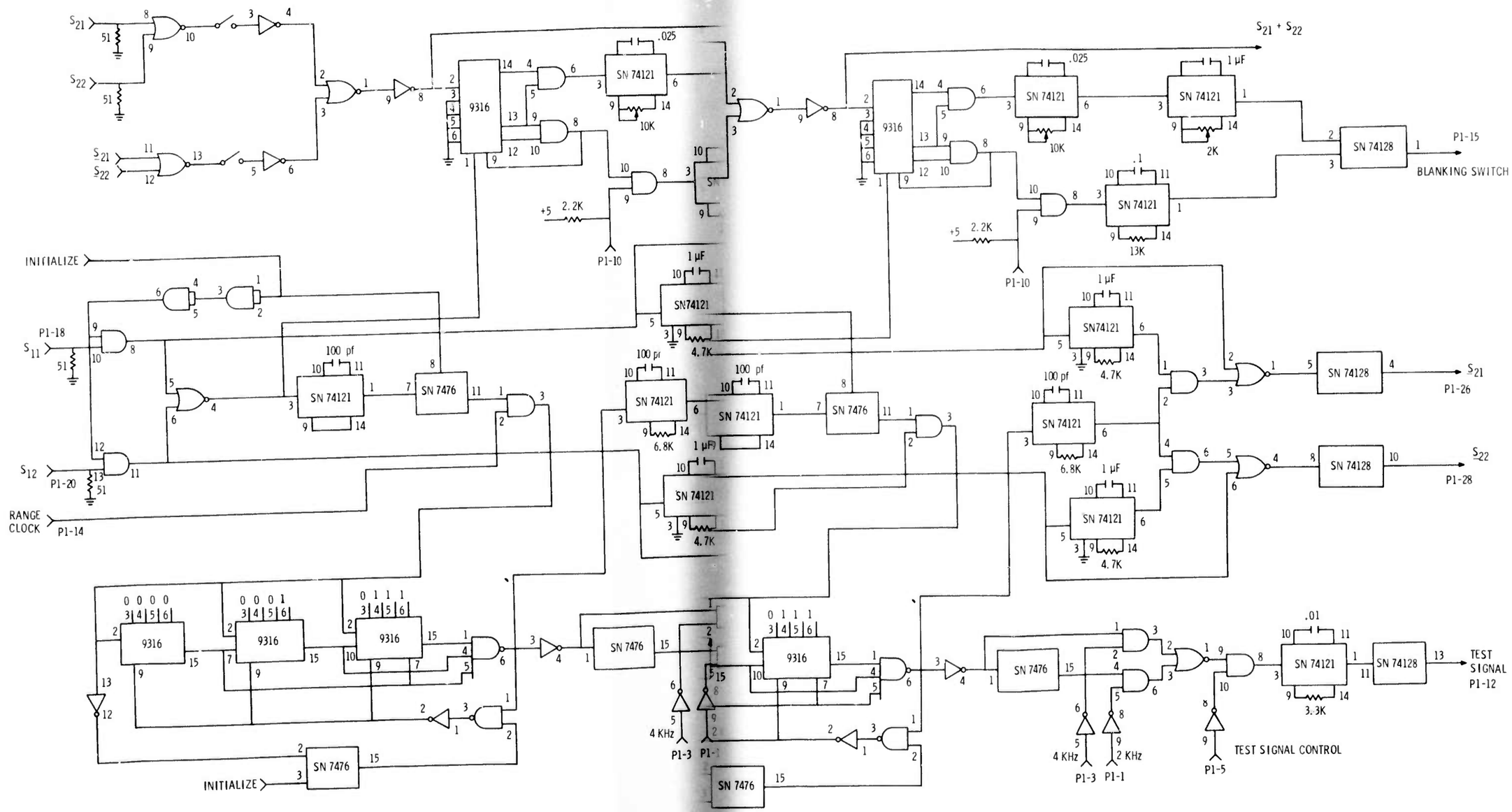


Figure 32. Logic Board (Sheet 2 of 2)

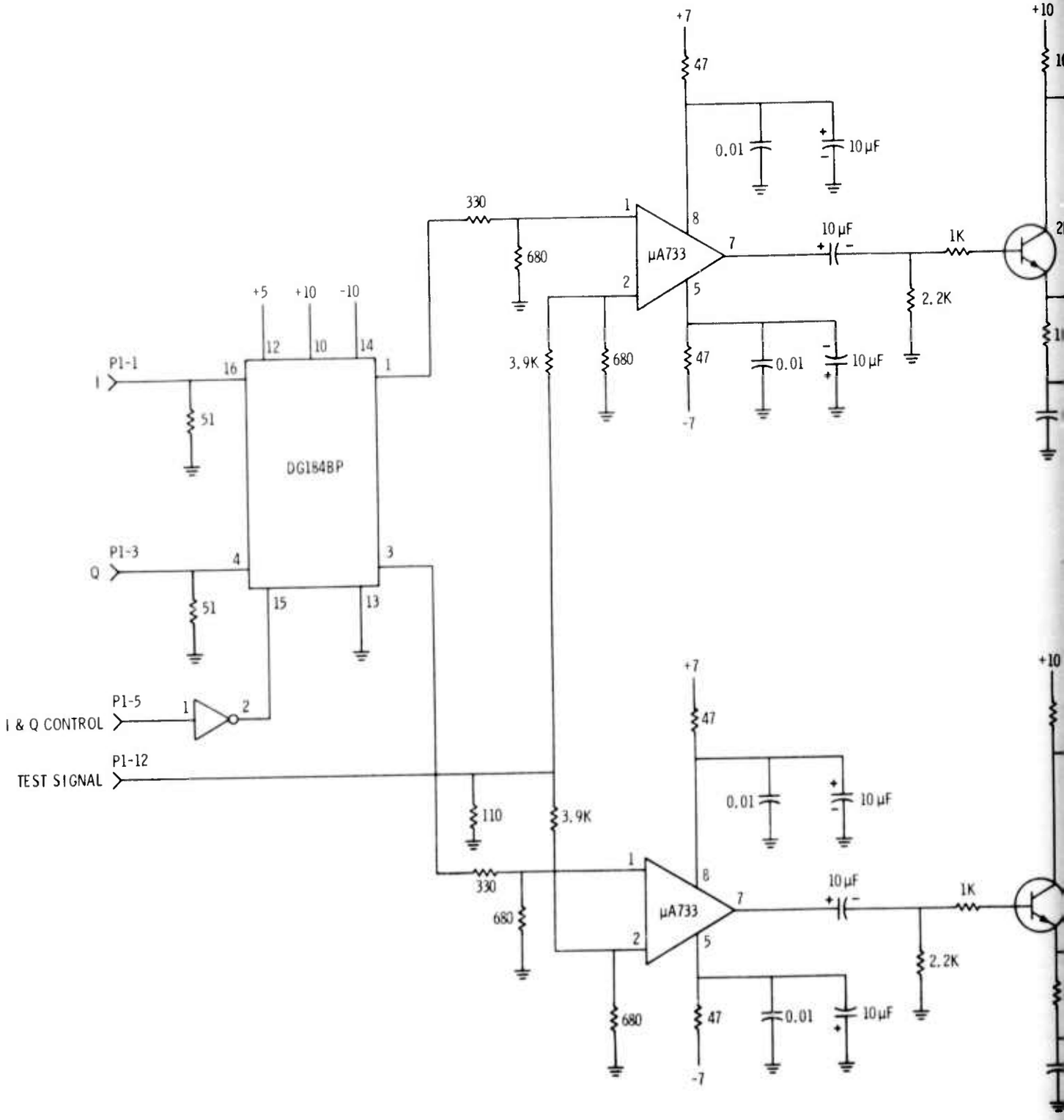


Figure 33. Input/O
Input Section

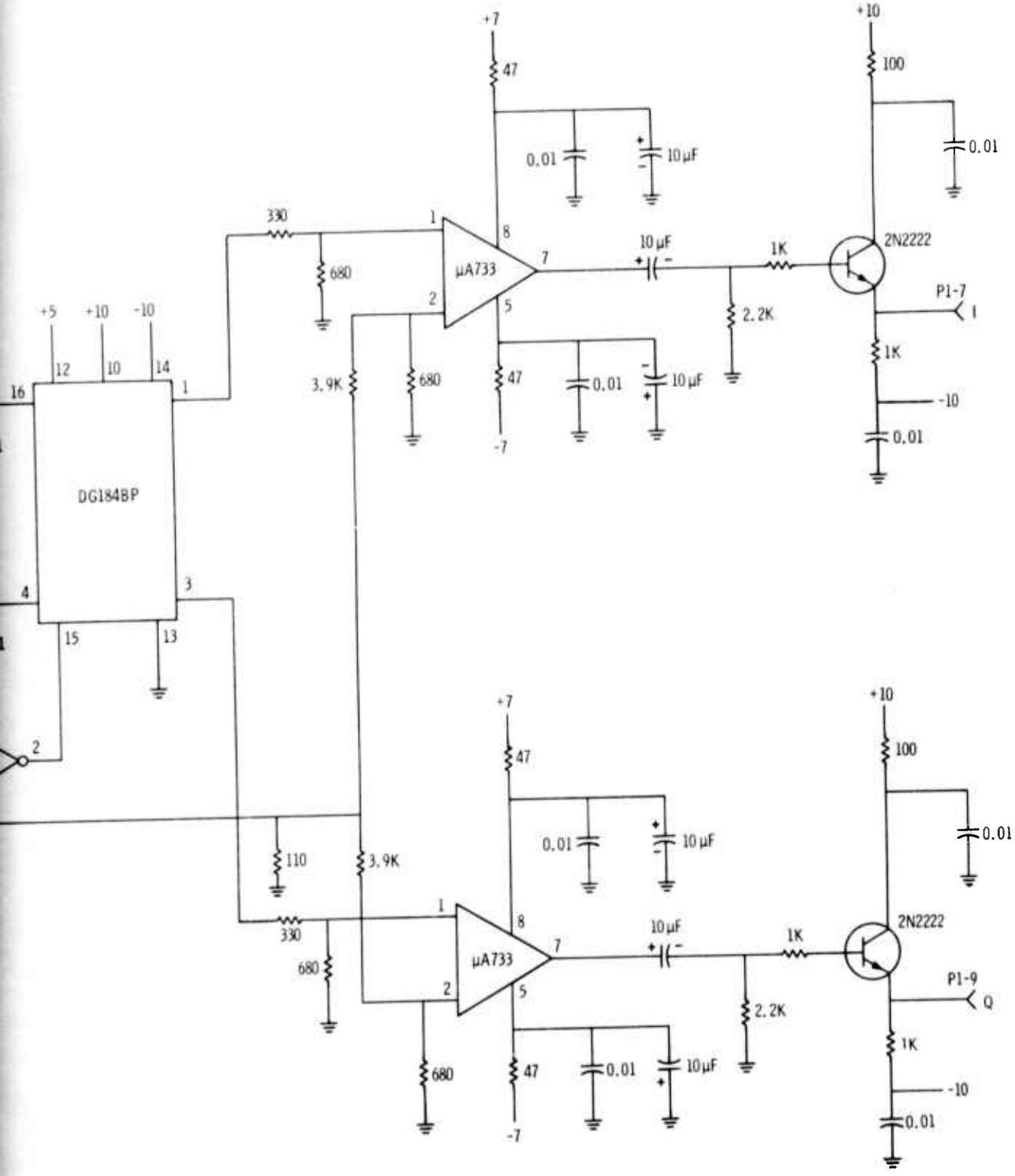
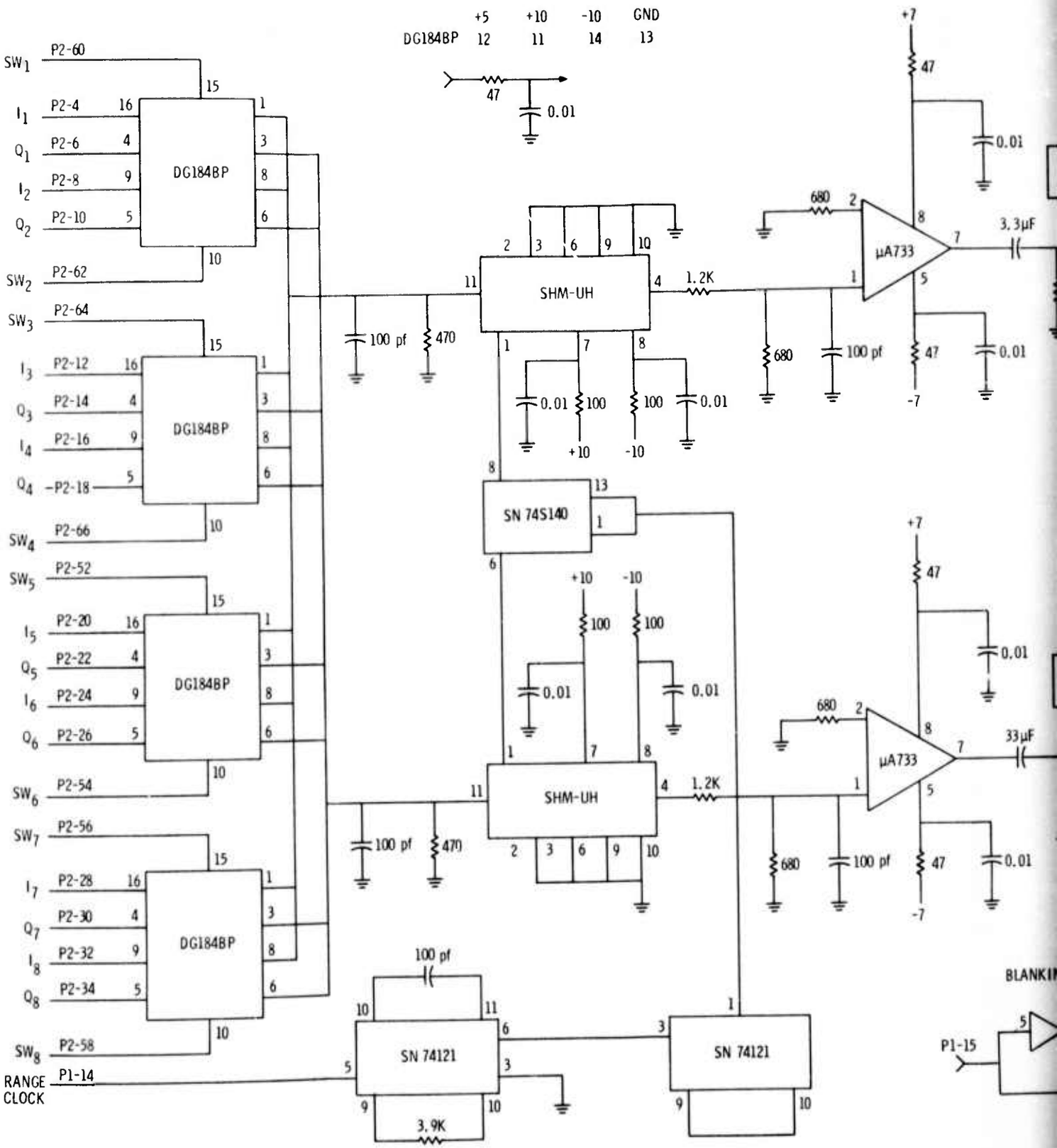


Figure 33. Input/Output Board - Input Section


+5 +10 -10 GND
DG184BP 12 11 14 13
47
0.01
SW1
P2-60
I1
P2-4
Q1
P2-6
I2
P2-8
Q2
P2-10
SW2
P2-62
SW3
P2-64
I3
P2-12
Q3
P2-14
I4
P2-16
Q4
P2-18
SW4
P2-66
SW5
P2-52
I5
P2-20
Q5
P2-22
I6
P2-24
Q6
P2-26
SW6
P2-54
SW7
P2-56
I7
P2-28
Q7
P2-30
I8
P2-32
Q8
P2-34
SW8
P2-58
RANGE CLOCK
P1-14
DG184BP
SHM-UH
SN 74S140
SN 74121
SN 74121
3.9K
100 pf
470
1.2K
680
μA733
3.3μF
33μF
100
+7
-7
+10
-10
BLANKI
P1-15

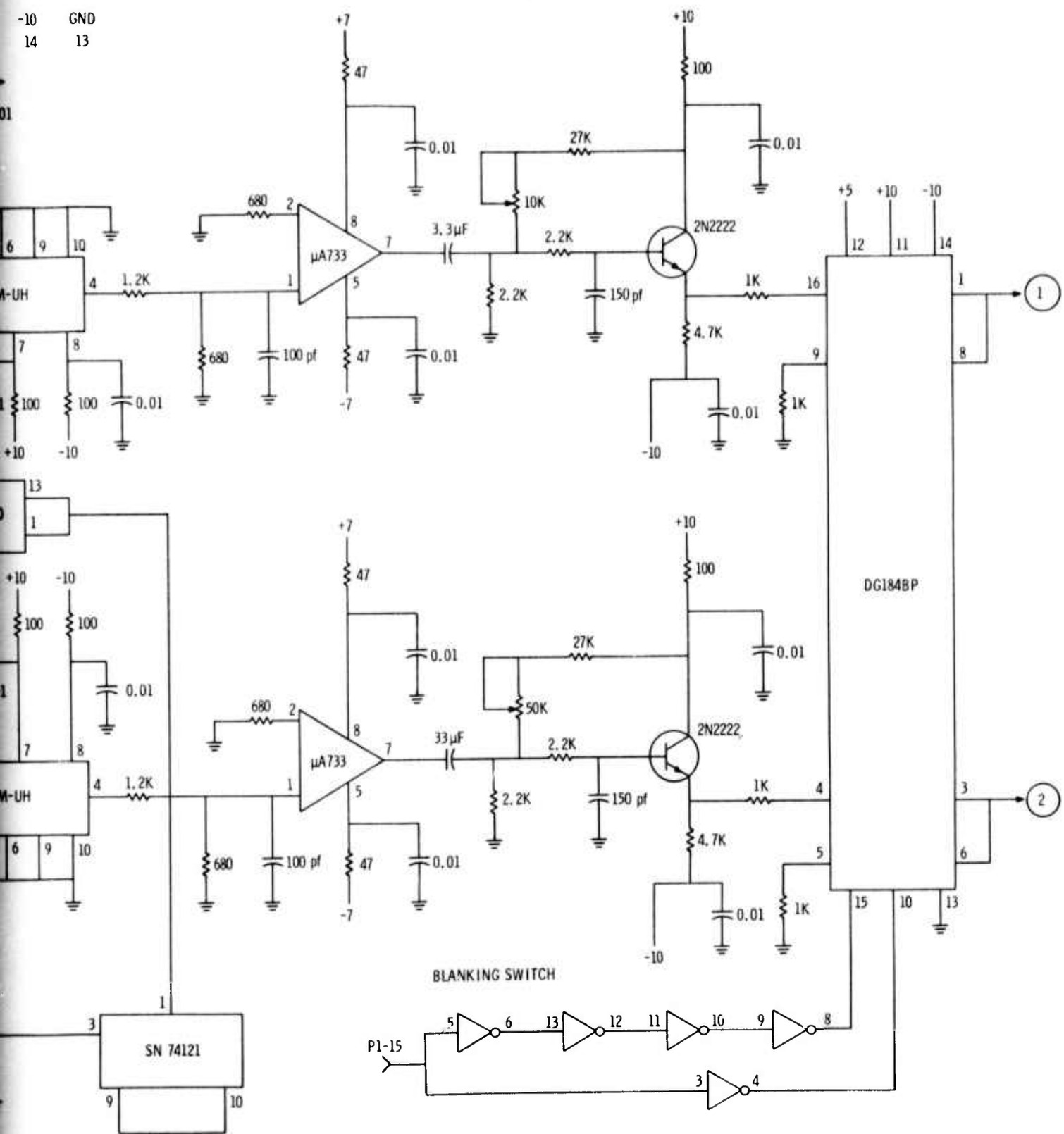


Figure 34. Input/Output Board - Output Section (Sheet 1 of 2)

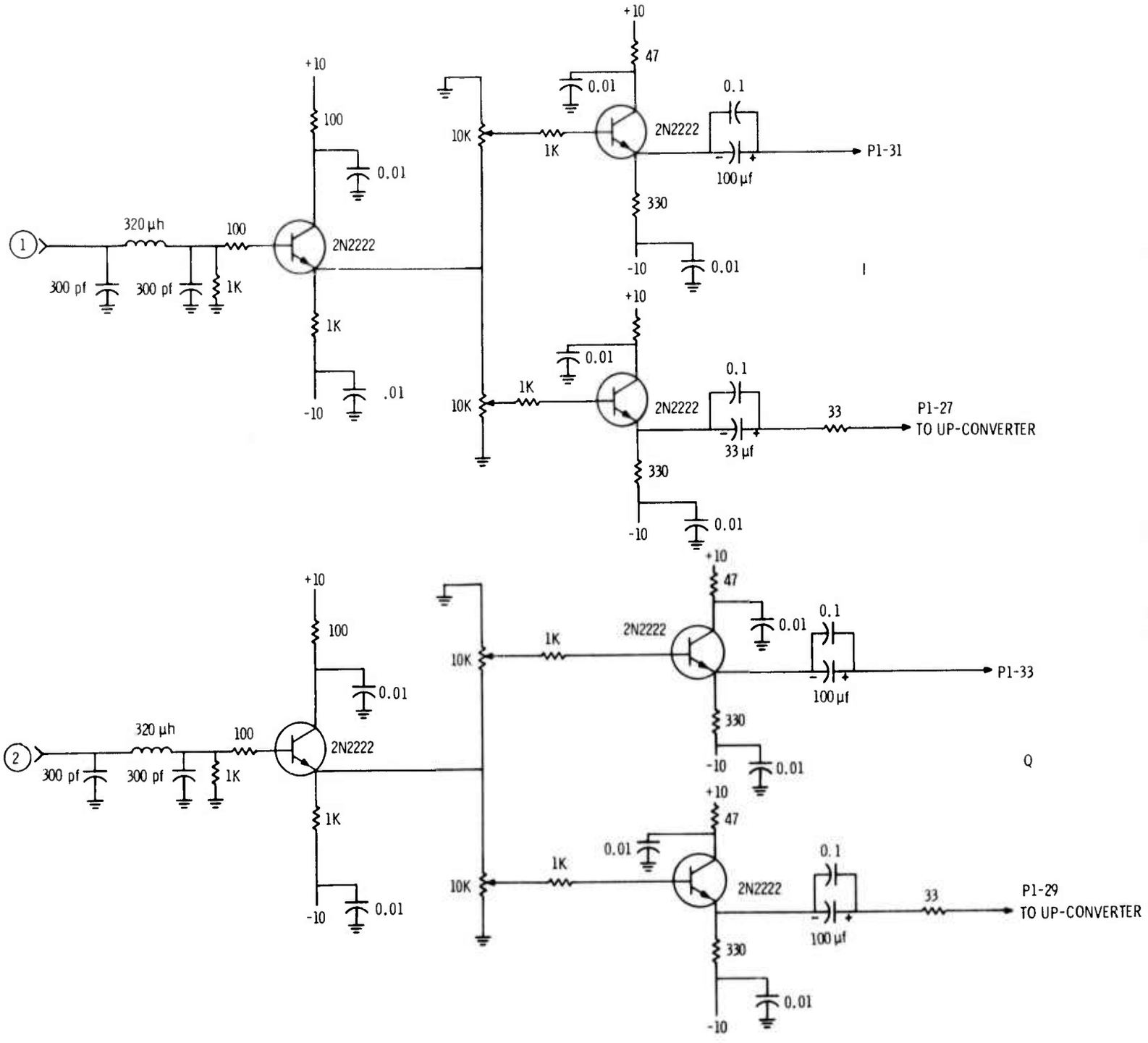
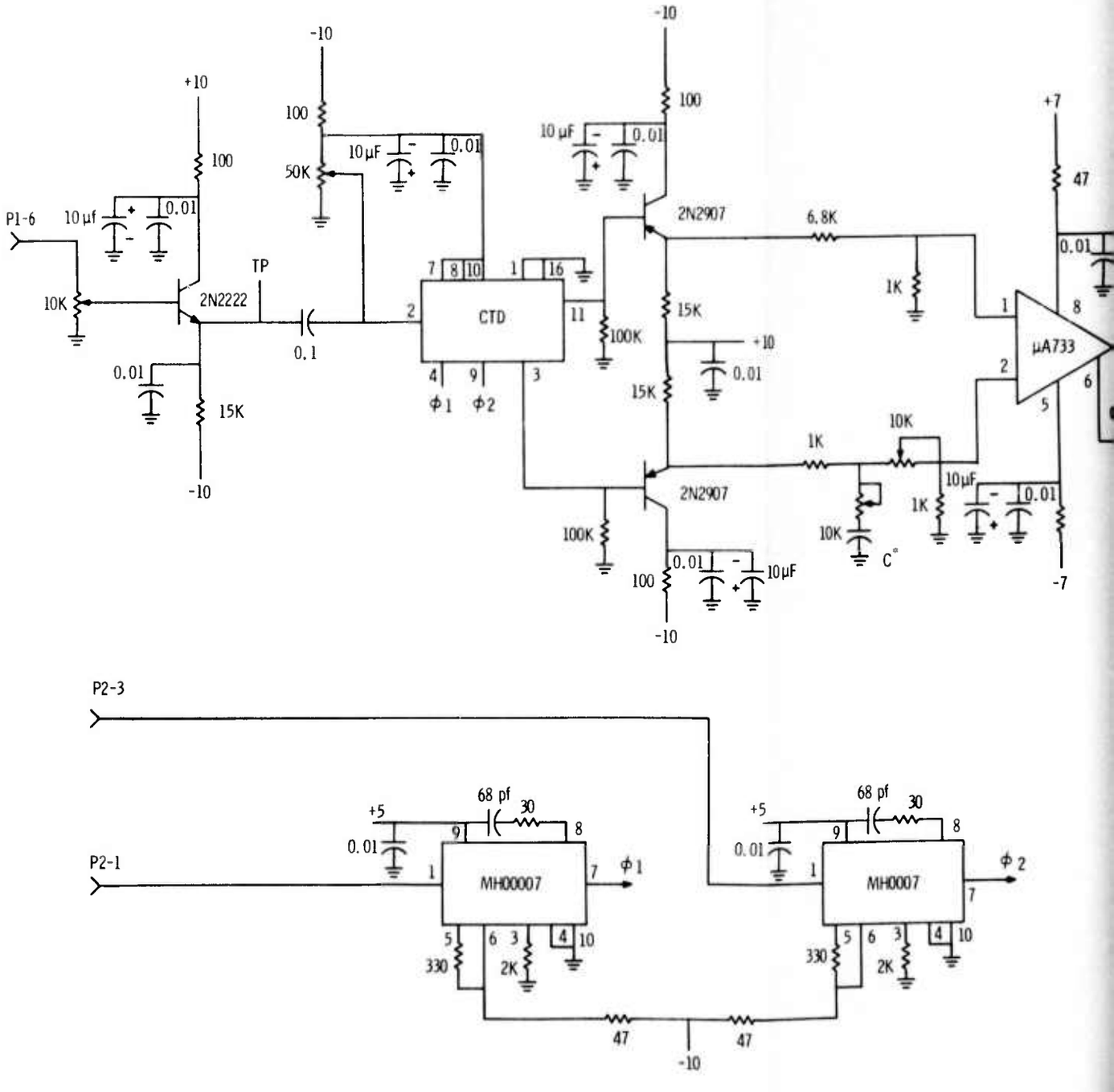


Figure 34. Input/Output Board - Output Section (Sheet 2 of 2)


-10
+10
100
50K
10 µF
0.01
P1-6
10 µf
2N2222
TP
10K
0.1
0.01
15K
-10
7 8 10 1 16
2
CTD
11
100K
4 9 3
ϕ1 ϕ2
2N2907
6.8K
1K
15K
+10
0.01
+7
47
µA733
10K
C°
-7

P2-3
P2-1
+5
68 pf
30
0.01
MH00007
ϕ1
ϕ2
330
2K
47
-10

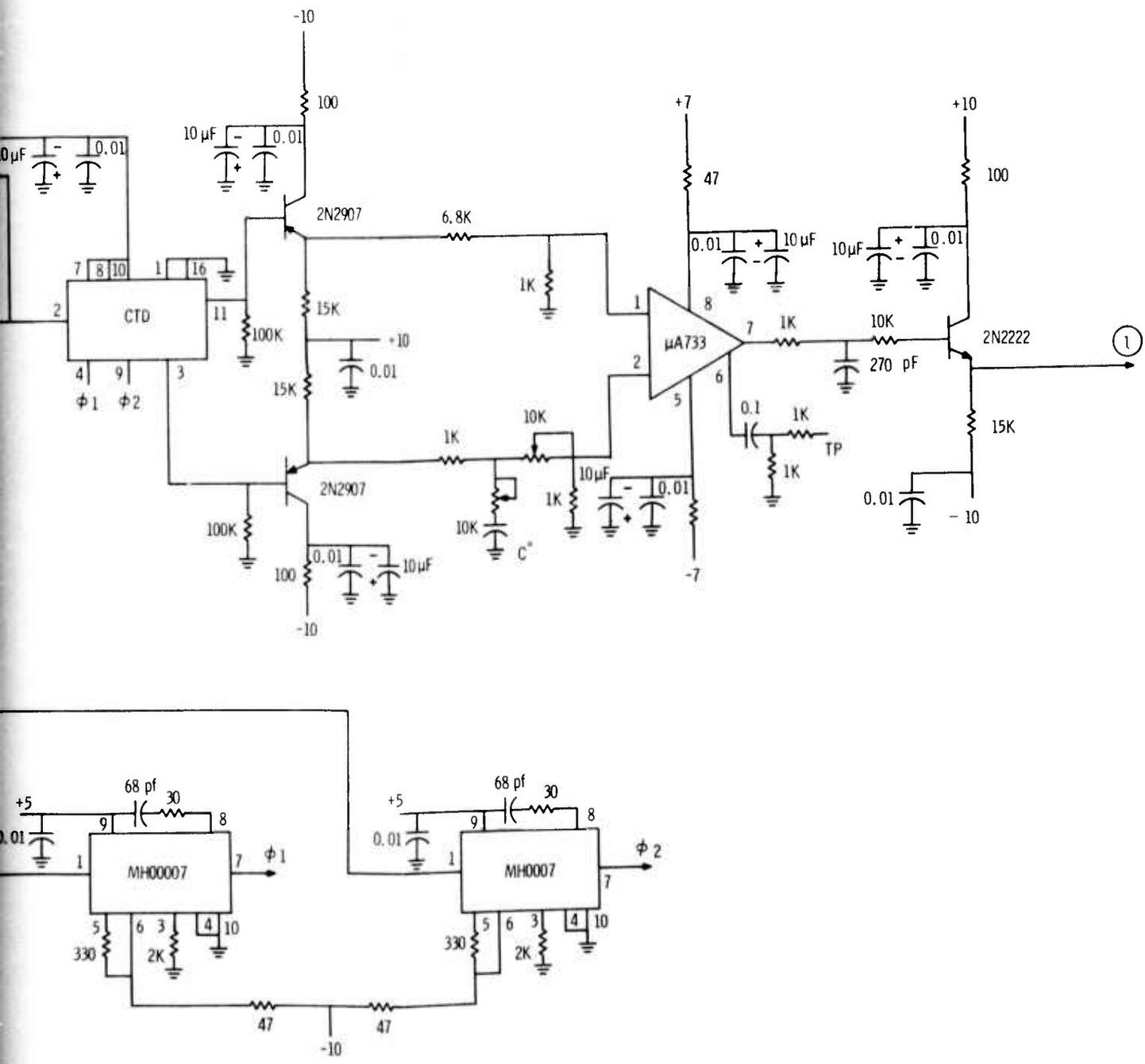
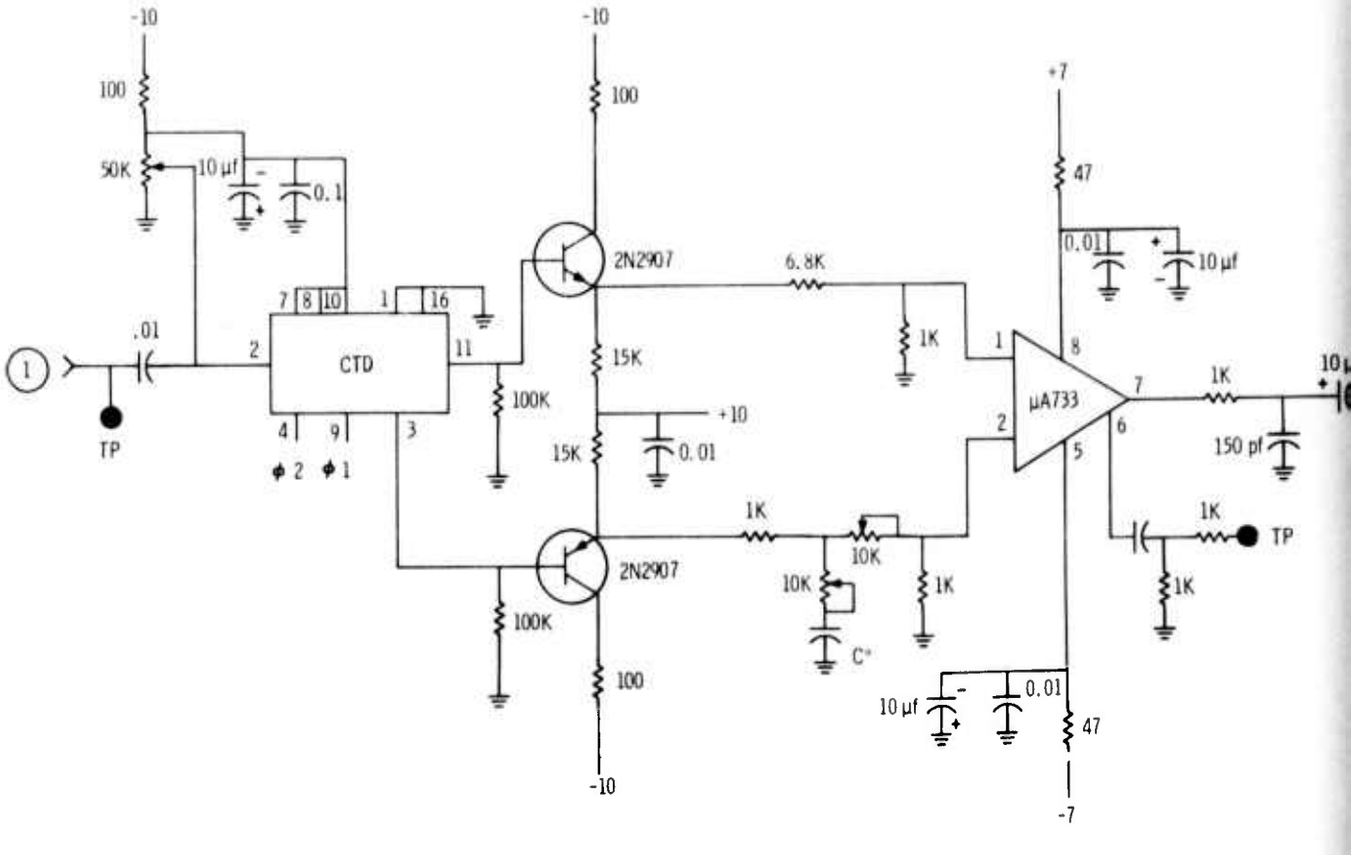
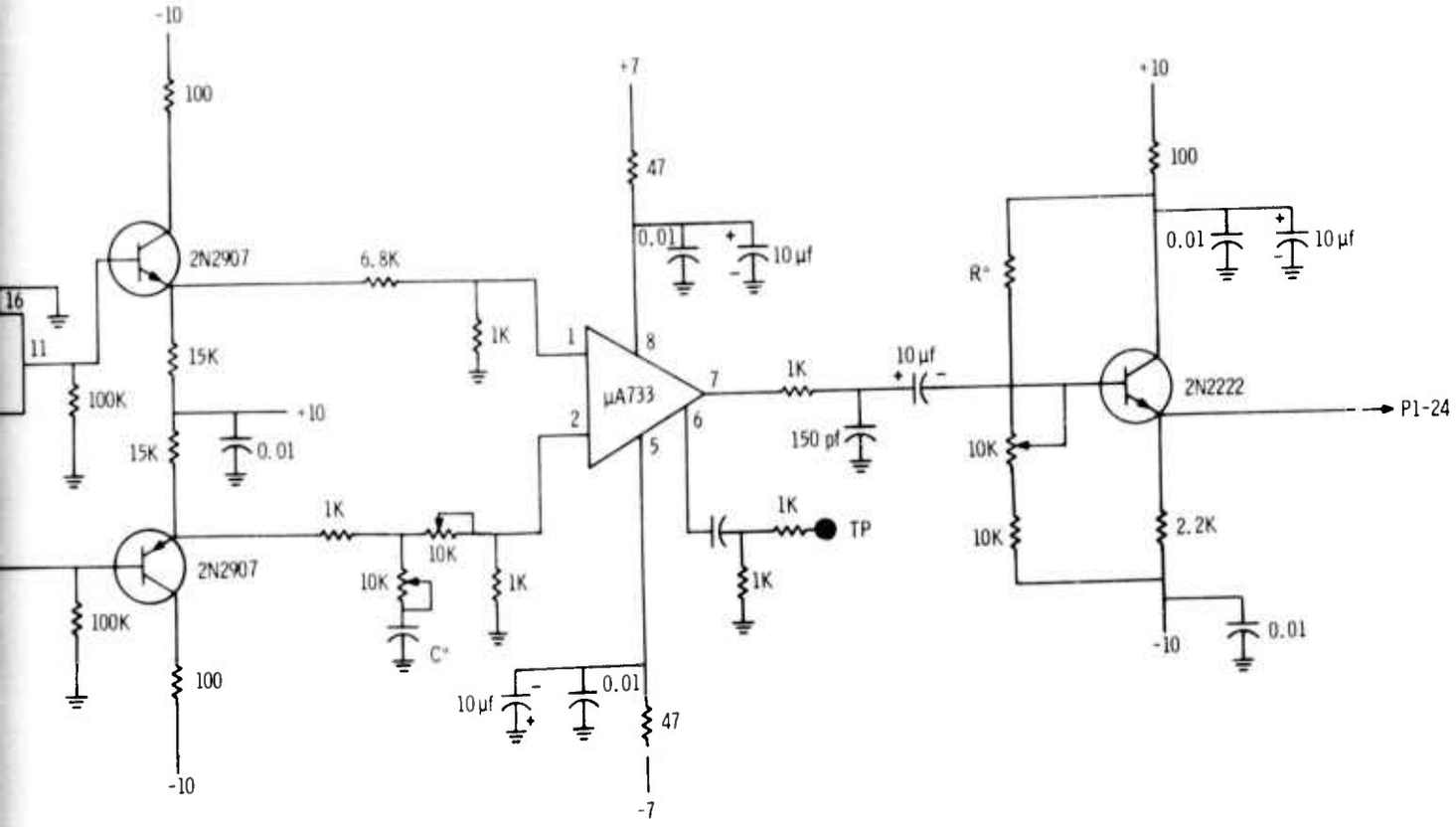


Figure 35. Cancellation Board - I Channel (Sheet 1 of 2)

2



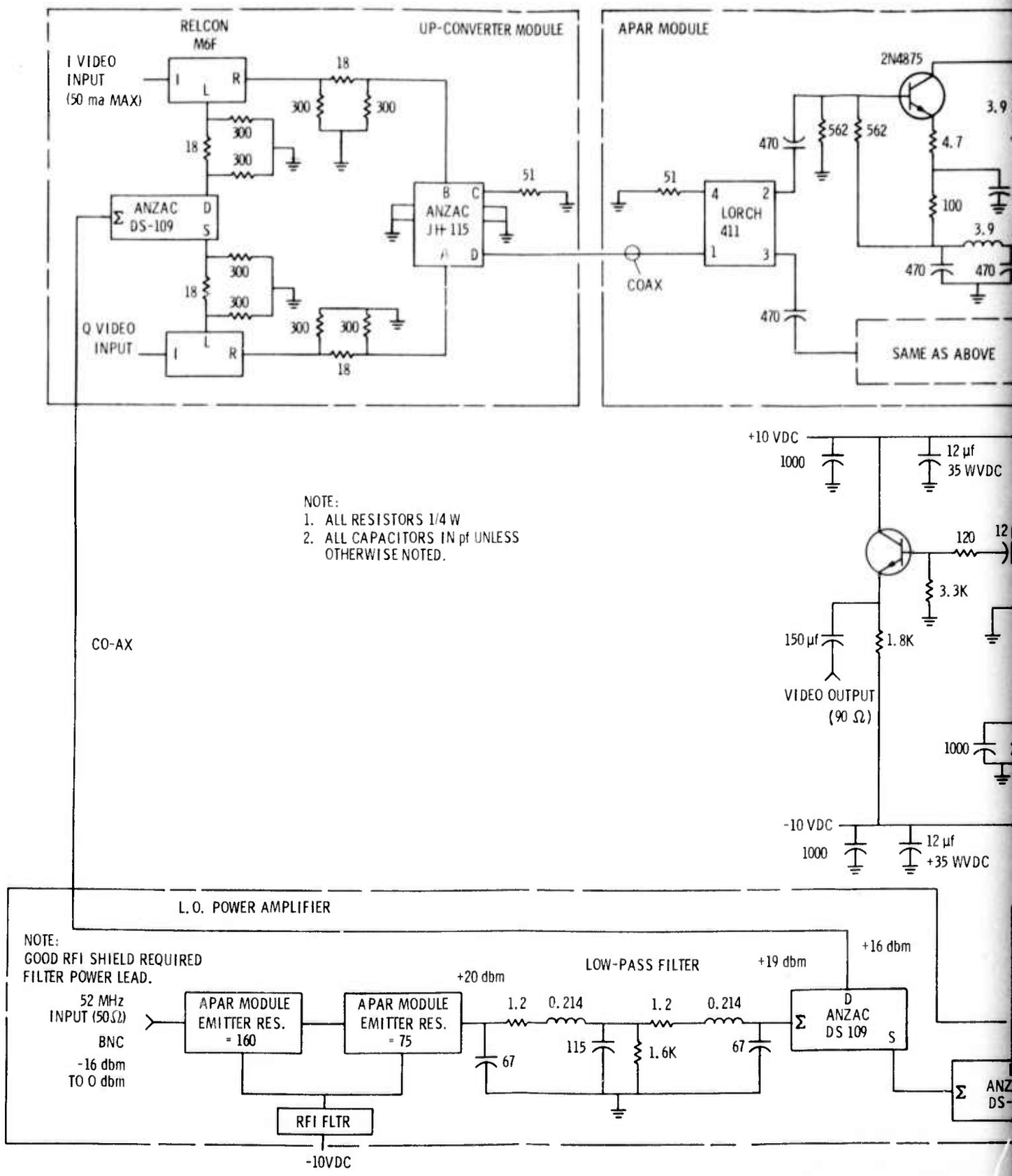
Q Channel
(same as I Channel)



Q Channel
(same as I Channel)

* R AND C DEPEND ON THE PARTICULAR CHANNEL

Figure 35. Cancellation Board - I Channel (Sheet 2 of 2)


RELCON
M6F
UP-CONVERTER MODULE
I VIDEO
INPUT
(50 ma MAX)
ANZAC
DS-109
ANZAC
JH-115
Q VIDEO
INPUT
APAR MODULE
2N4875
LORCH
411
COAX
SAME AS ABOVE
+10 VDC
1000
12 µf
35 WVDC
120
3.3K
150 µf
1.8K
VIDEO OUTPUT
(90 Ω)
-10 VDC
1000
12 µf
+35 WVDC
NOTE:
1. ALL RESISTORS 1/4 W
2. ALL CAPACITORS IN pf UNLESS
OTHERWISE NOTED.
CO-AX
L.O. POWER AMPLIFIER
NOTE:
GOOD RFI SHIELD REQUIRED
FILTER POWER LEAD.
52 MHz
INPUT (50Ω)
BNC
-16 dbm
TO 0 dbm
APAR MODULE
EMITTER RES.
= 160
APAR MODULE
EMITTER RES.
= 75
+20 dbm
LOW-PASS FILTER
+19 dbm
+16 dbm
ANZAC
DS 109
RFI FLTR
-10VDC

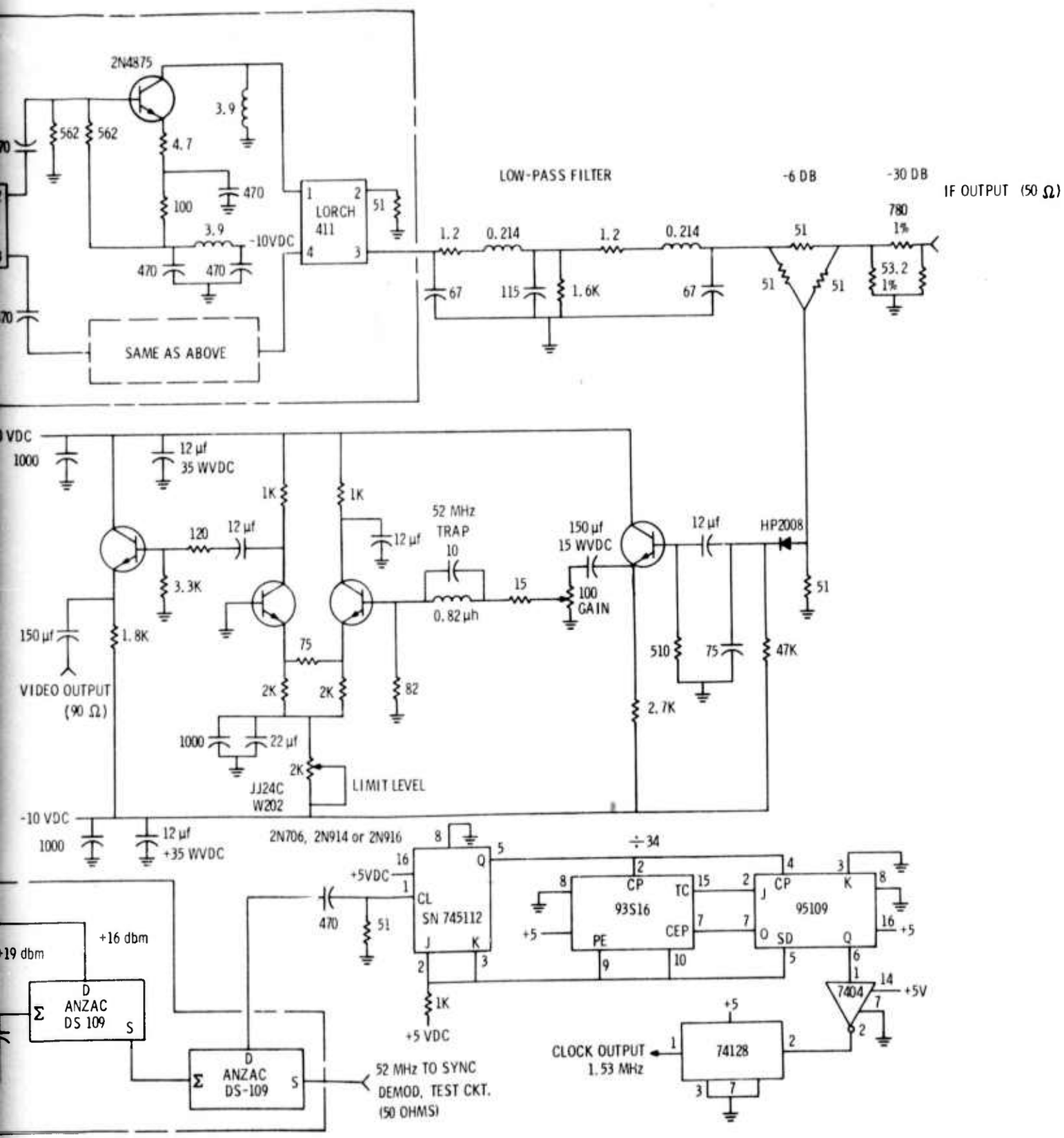
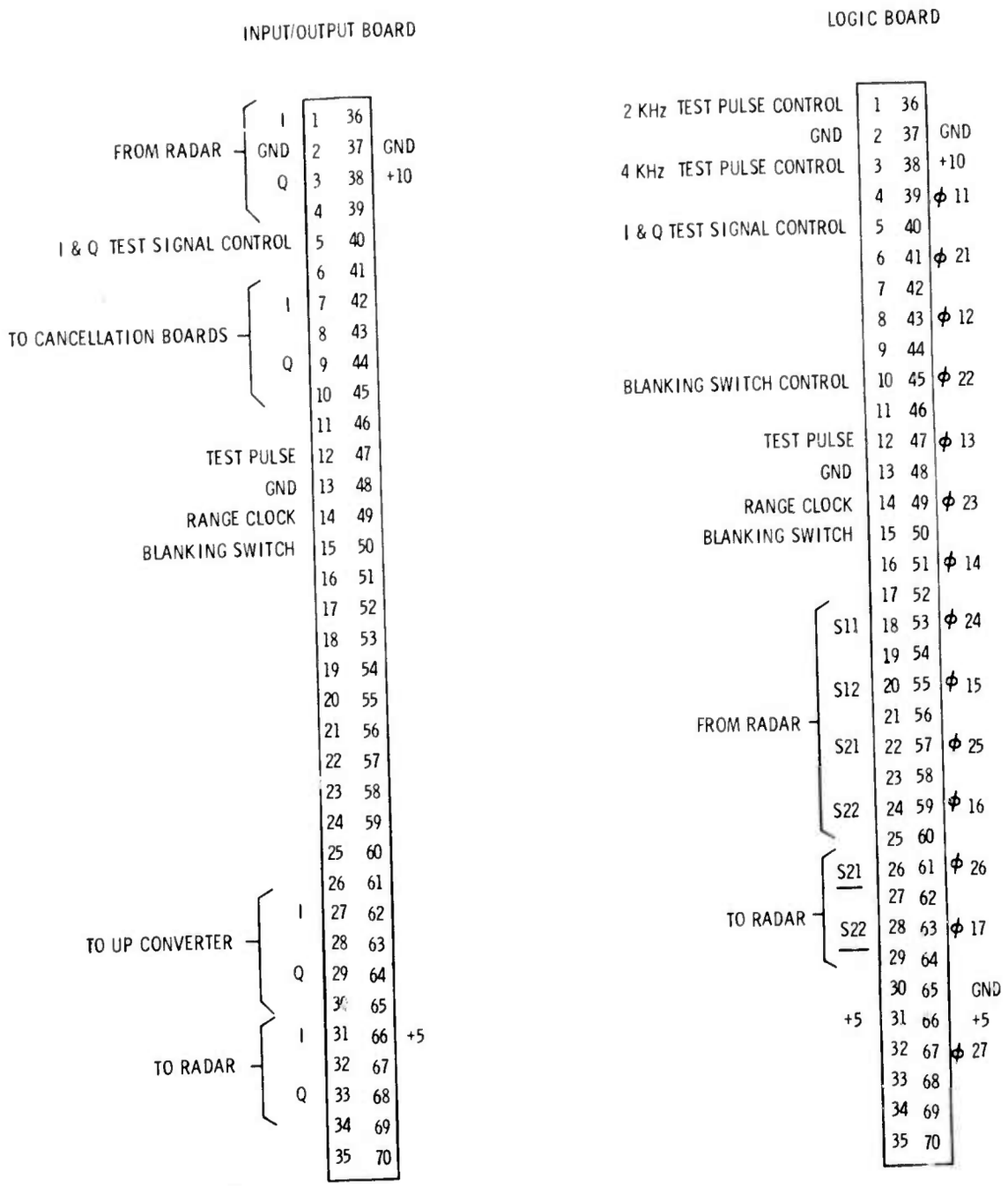


Figure 36. Up Converter/Detector


INPUT/OUTPUT BOARD
FROM RADAR
I
GND
Q
I & Q TEST SIGNAL CONTROL
TO CANCELLATION BOARDS
I
Q
TEST PULSE
GND
RANGE CLOCK
BLANKING SWITCH
TO UP CONVERTER
I
Q
TO RADAR
I
Q
1 36
2 37 GND
3 38 +10
4 39
5 40
6 41
7 42
8 43
9 44
10 45
11 46
12 47
13 48
14 49
15 50
16 51
17 52
18 53
19 54
20 55
21 56
22 57
23 58
24 59
25 60
26 61
27 62
28 63
29 64
30 65
31 66 +5
32 67
33 68
34 69
35 70
LOGIC BOARD
2 KHz TEST PULSE CONTROL
GND
4 KHz TEST PULSE CONTROL
I & Q TEST SIGNAL CONTROL
BLANKING SWITCH CONTROL
TEST PULSE
GND
RANGE CLOCK
BLANKING SWITCH
FROM RADAR
S11
S12
S21
S22
TO RADAR
S21
S22
+5
1 36
2 37 GND
3 38 +10
4 39 ϕ 11
5 40
6 41 ϕ 21
7 42
8 43 ϕ 12
9 44
10 45 ϕ 22
11 46
12 47 ϕ 13
13 48
14 49 ϕ 23
15 50
16 51 ϕ 14
17 52
18 53 ϕ 24
19 54
20 55 ϕ 15
21 56
22 57 ϕ 25
23 58
24 59 ϕ 16
25 60
26 61 ϕ 26
27 62
28 63 ϕ 17
29 64
30 65 GND
31 66 +5
32 67 ϕ 27
33 68
34 69
35 70

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(Shee

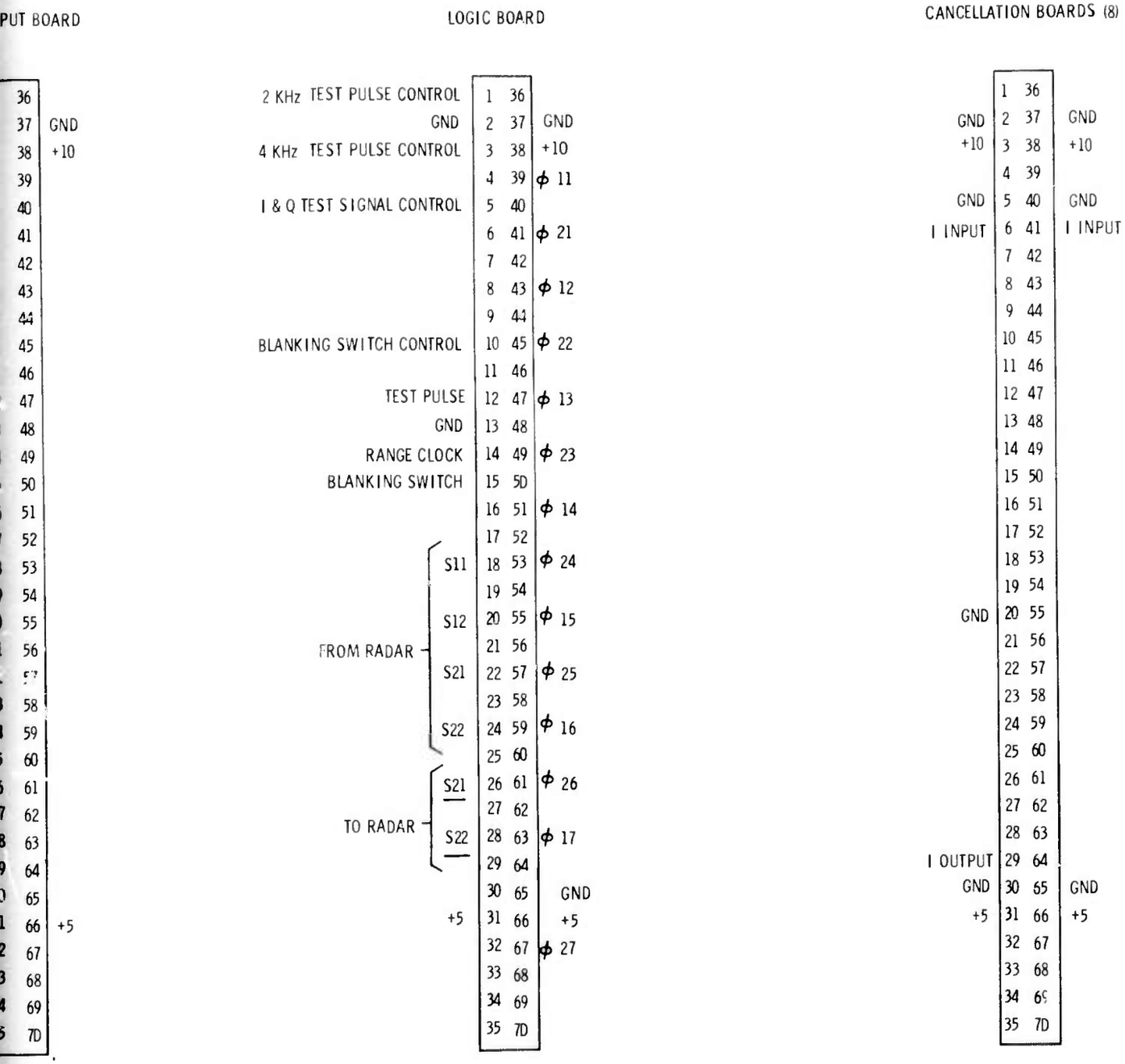

Figure 37. Back Plane Wiring
(Sheet 1 of 2)

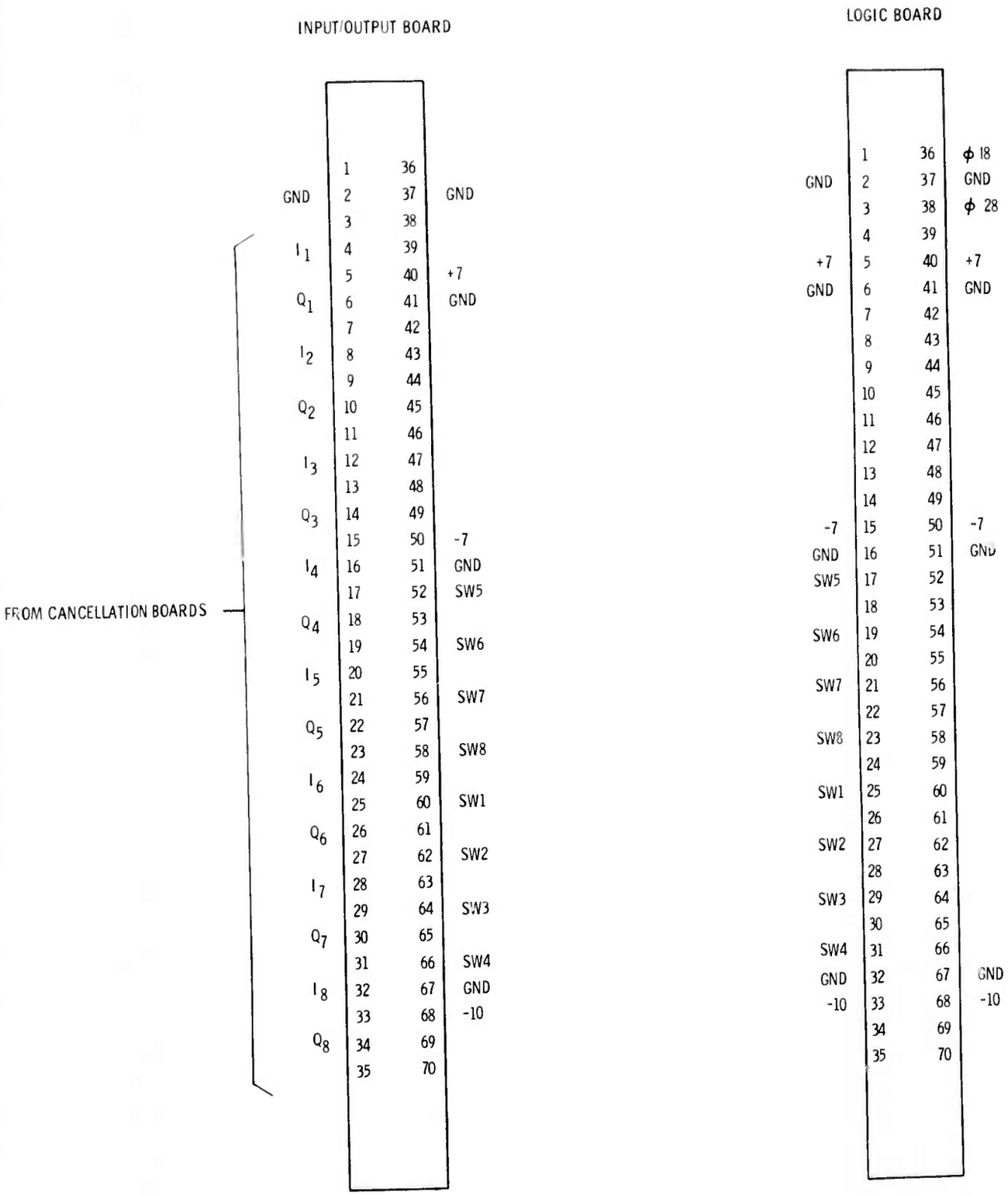
INPUT/OUTPUT BOARD
LOGIC BOARD
FROM CANCELLATION BOARDS
GND
GND
I_1
+7
Q_1
GND
I_2
Q_2
I_3
Q_3
-7
I_4
GND
SW5
Q_4
SW6
I_5
SW7
Q_5
SW8
I_6
SW1
Q_6
SW2
I_7
SW3
Q_7
SW4
I_8
GND
-10
Q_8
1 36
2 37
3 38
4 39
5 40
6 41
7 42
8 43
9 44
10 45
11 46
12 47
13 48
14 49
15 50
16 51
17 52
18 53
19 54
20 55
21 56
22 57
23 58
24 59
25 60
26 61
27 62
28 63
29 64
30 65
31 66
32 67
33 68
34 69
35 70
ϕ 18
GND
ϕ 28
+7
GND
-7
GND
SW5
SW6
SW7
SW8
SW1
SW2
SW3
SW4
GND
-10
GND

Fig
(She

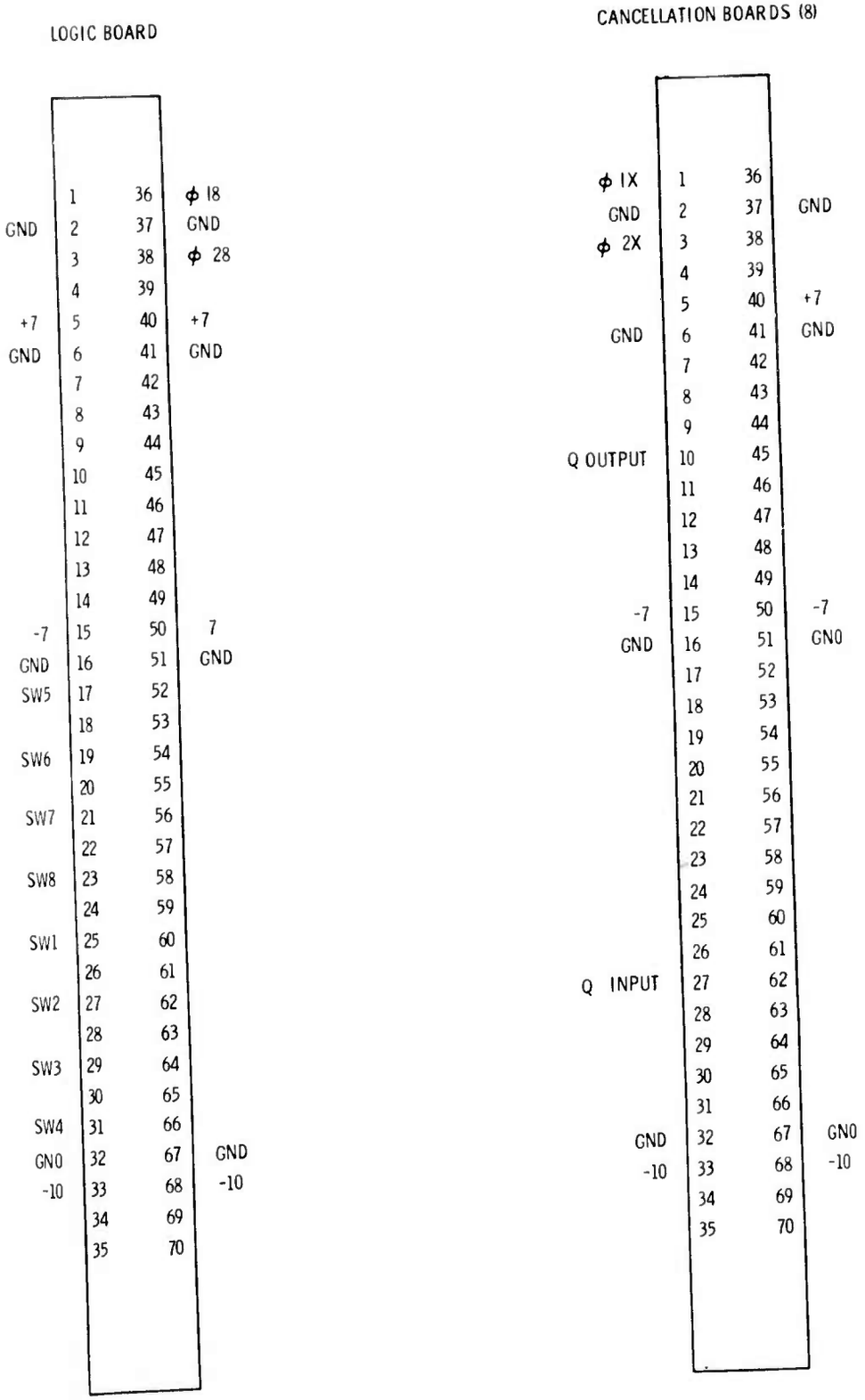

Figure 37. Back Plane Wiring
(Sheet 2 of 2)

APPENDIX B

PARTS LIST FOR DISCRETE SIGNAL MTI

DEVICE	DESCRIPTION	MANUFACTURER
NH0007	Clock Driver	National
SN7476N	J-K Flip-Flop	Texas Instruments
SN74164N	8-bit Shift Register	Texas Instruments
SN74SO4	Schottky Hex Inverter	Texas Instruments
SN7408N	Quad 2-input AND Gate	Texas Instruments
SN7402N	Quad 2-input NOR Gate	Texas Instruments
SN74121N	Monostable Multivibrator	Texas Instruments
SN7413N	Schmitt Trigger	Texas Instruments
SN7400N	Quad 2-input NAND	Texas Instruments
SN7404N	Hex Inverter	Texas Instruments
SN74S140	Schottky Dual 4-input 50-ohm Driver	Texas Instruments
SN74128	Quad 2-input 50-ohm Driver	Texas Instruments
SN74S112	Schottky J-K Flip-Flop	Texas Instruments
μ7B931659X	Modulo-N-Counter	Fairchild
μ7B93S1659X	Schottky Mod-N-Counter	Fairchild
μ7B9S10959X	Schottky J-F Flip-Flop	Fairchild
μ5F7733393	Video Amplifier	Fairchild
DG184BP	Analog Switch	Siliconix
2N2222A	NPN Transistor	National
2N2907A	PNP Transistor N	National
SHM-UH	Sample and Hold	Datel
M6F	Mixer	Relcom
DS-109	Power Splitter	Anzac
JH-115	Quad Hybrid	Anzac

DEVICE	DESCRIPTION	MANUFACTURER
VA SMT 900	5 V Power Supply	Acopian
VA 7M T 500	7 V Power Supply	Acopian
VA 10 MT 450	10 V Power Supply	Acopian
VA 10 MT 750	10 V Power Supply	Acopian

APPENDIX C

PHOTOGRAPHS OF DISCRETE SIGNAL MTI

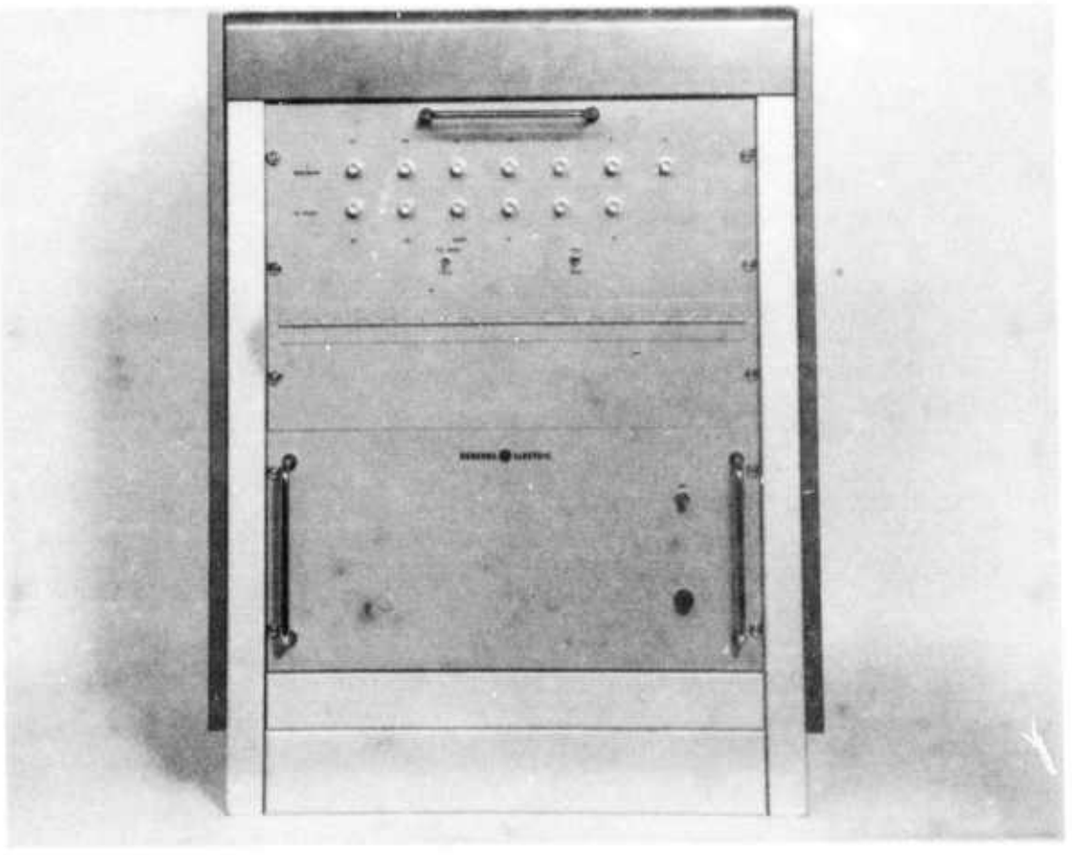

Figure 38. Discrete Signal MTI, Front View (The lower drawer consists of the power supplies, and the upper card cage contains the input/output board, logic board, and eight I and Q channel canceller boards)

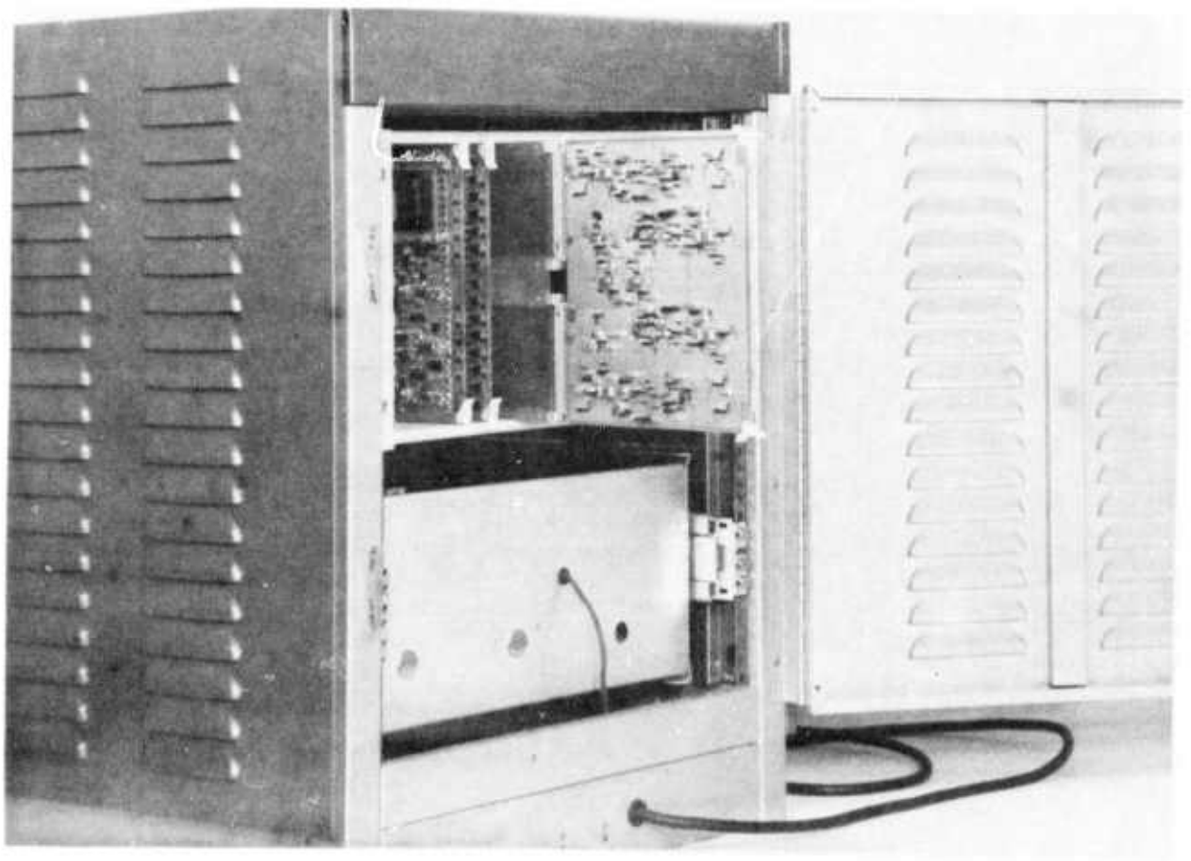

Figure 39. Discrete Signal MTI, Rear View

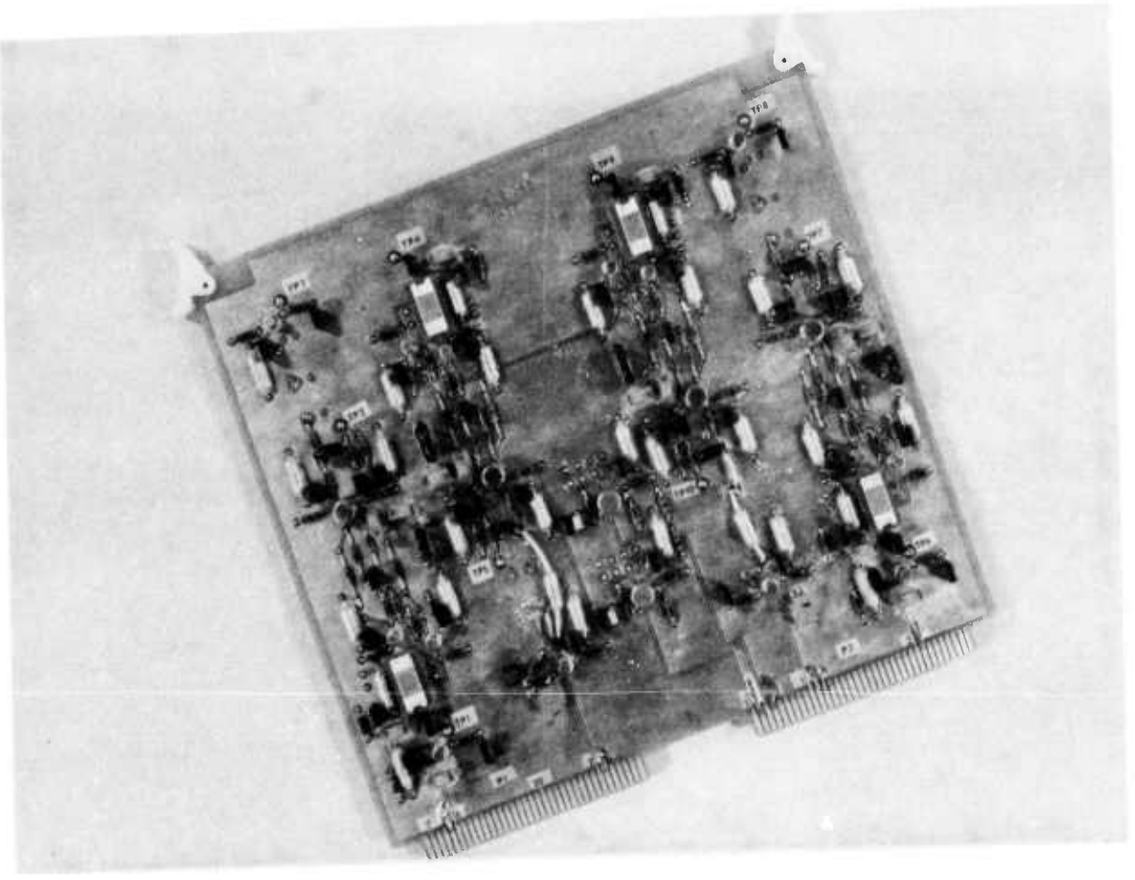

Figure 40. Cancellation Board

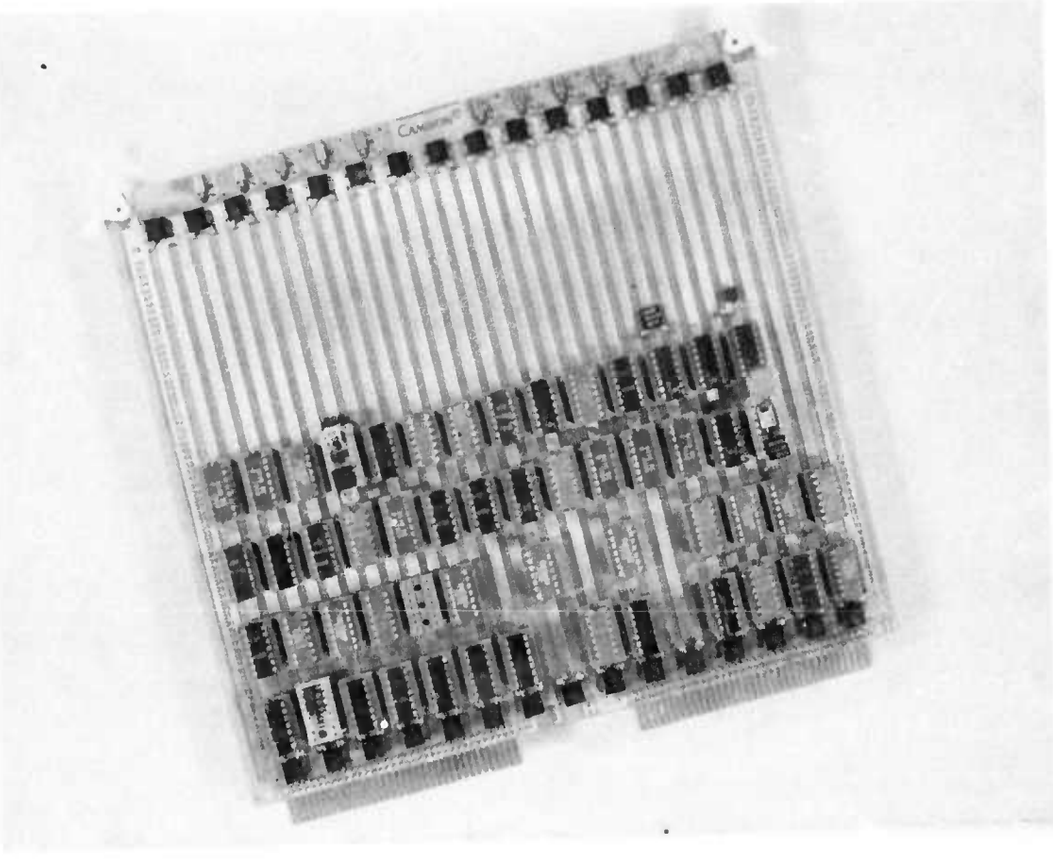

Figure 41. Logic Board

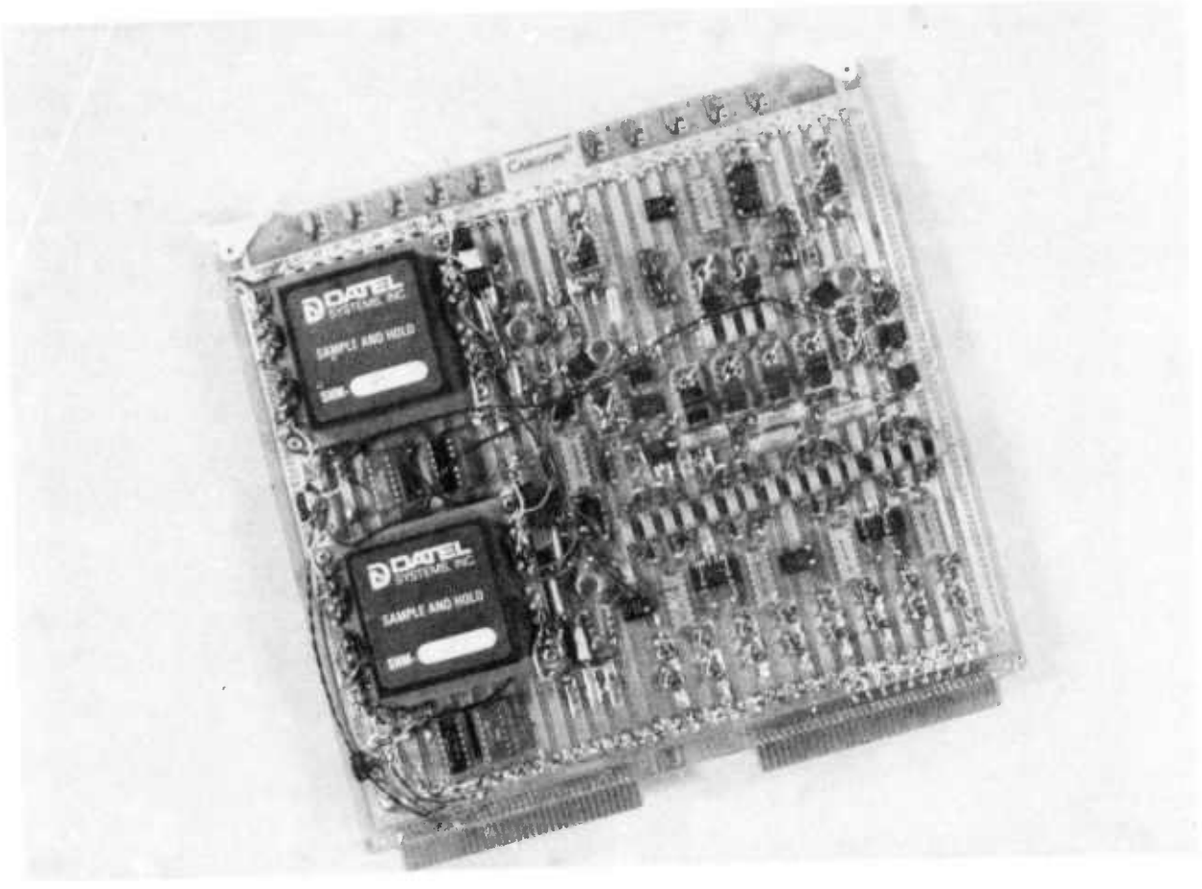

Figure 42. Input/Output Board

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4. TITLE *(and Subtitle)* DISCRETE SIGNAL MOVING TARGET INDICATOR (MTI)		5. TYPE OF REPORT & PERIOD COVERED Final Report 7 March 73 - 7 June 1974 6. PERFORMING ORG. REPORT NUMBER None
7. AUTHOR(s) D.N. Ludington H. Lobenstein		8. CONTRACT OR GRANT NUMBER(s) F30602-73-C-0152
9. PERFORMING ORGANIZATION NAME AND ADDRESS General Electric Company Aerospace Electronic Systems Department Utica, New York 13503		10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS PE 62702F JO 45060187
11. CONTROLLING OFFICE NAME AND ADDRESS Rome Air Development Center (OCTS) Griffiss Air Force Base, New York 13441		12. REPORT DATE October 1974 13. NUMBER OF PAGES 78
14. MONITORING AGENCY NAME & ADDRESS *(if different from Controlling Office)* Same		15. SECURITY CLASS. *(of this report)* Unclassified 15a. DECLASSIFICATION/DOWNGRADING SCHEDULE N/A

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18. SUPPLEMENTARY NOTES

RADC Project Engineer:
William Lee Simkins, Jr. (OCTS)
AC 315 330-4437

19. KEY WORDS *(Continue on reverse side if necessary and identify by block number)*

MTI
Charge Transfer Devices (CTD)
Charge Coupled Devices (CCD)
Bucket Brigade Delay Lines
Delay Line

20. ABSTRACT *(Continue on reverse side if necessary and identify by block number)*

This final technical report describes an experimental R & D program to apply charge transfer device (CTD) technology to the design and fabrication of a three-pulse MTI, and demonstrate its capabilities in an actual radar system. The specified 50 dB cancellation ratio was achieved. The CTD is a sampled data integrated circuit in which samples are stored and processed as discrete packets of charge. Utilizing a continuous range of amplitude, CTD's eliminate the cost, volume, and power penalties inherent in the A/D and D/A conversion

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20. ABSTRACT (continued)

used in digital systems, while retaining the advantages of stability and small size. The design trade-offs necessitated by using devices available at the beginning of the contract, and subsequent limitations are discussed. The present state-of-the-art CTD's would eliminate the need for the multiplexing used for this contract and reduce the hardware by a factor of four. CTD technology offers a stable, low cost alternative to MTI design. In addition, signal processing methods such as pulse compression, correlation, chirp z transforms, and allied techniques are under investigation and should be considered by the system designer.