ABSTRACT

Title of dissertation: BAT AZIMUTHAL ECHOLOCATION USING INTERAURAL LEVEL DIFFERENCES: MODELING AND IMPLEMENTATION BY A VLSI-BASED HARDWARE SYSTEM

Zhiping Shi, Doctor of Philosophy, 2006

Dissertation directed by: Professor Timothy K. Horiuchi
Department of Electrical and Computer Engineering

Bats have long fascinated both scientists and engineers due to their superb ability to use echolocation to fly with speed and agility through complex natural environments in complete darkness. This dissertation presents a neuromorphic VLSI circuit model of bat azimuthal echolocation. Interaural level differences (ILDs) are the cues for bat azimuthal echolocation and are also the primary cues used by other mammals to localize high frequency sounds. The fact that neurons in bats respond to short echoes by one or two spikes strongly suggests that the conventionally used firing rate is an unlikely code. The operation of first spike latency in ILD computation and transformation is investigated in a network of spiking neurons linking the lateral superior olive (LSO), dorsal nucleus of the lateral lemniscus (DNLL), and inferior colliculus (IC). The results of the investigation suggest that spatially distributed first spike latencies can serve as a fast code for azimuth that can be "read-out" by ascending stages. With the hardware echolocation model that uses spike timing representation, we study how multiple echoes can affect bat echoloca-

Report Documentation Page

Form Approved
OMB No. 0704-0188

1. REPORT DATE	2. REPORT TYPE	3. DATES COVERED
2006		**00-00-2006 to 00-00-2006**

4. TITLE AND SUBTITLE	5a. CONTRACT NUMBER
Bat Azimuthal Echolocation Using Interaural Level Differences: Modeling and Implementation by a VLSI-Based Hardware System	5b. GRANT NUMBER
	5c. PROGRAM ELEMENT NUMBER
6. AUTHOR(S)	5d. PROJECT NUMBER
	5e. TASK NUMBER
	5f. WORK UNIT NUMBER
7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES) **University of Maryland, College Park,Department of Electrical and Computer Engineering,College Park,MD,20742**	8. PERFORMING ORGANIZATION REPORT NUMBER
9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)	10. SPONSOR/MONITOR'S ACRONYM(S)
	11. SPONSOR/MONITOR'S REPORT NUMBER(S)

12. DISTRIBUTION/AVAILABILITY STATEMENT
Approved for public release; distribution unlimited

13. SUPPLEMENTARY NOTES

14. ABSTRACT

Bats have long fascinated both scientists and engineers due to their superb ability to use echolocation to fly with speed and agility through complex natural environments in complete darkness. This dissertation presents a neuromorphic VLSI circuit model of bat azimuthal echolocation. Interaural level differences (ILDs) are the cues for bat azimuthal echolocation and are also the primary cues used by other mammals to localize high frequency sounds. The fact that neurons in bats respond to short echoes by one or two spikes strongly suggests that the conventionally used firing rate is an unlikely code. The operation of first spike latency in ILD computation and transformation is investigated in a network of spiking neurons linking the lateral superior olive (LSO), dorsal nucleus of the lateral lemniscus (DNLL) and inferior colliculus (IC). The results of the investigation suggest that spatially distributed first spike latencies can serve as a fast code for azimuth that can be ?read-out? by ascending stages. With the hardware echolocation model that uses spike timing representation, we study how multiple echoes can affect bat echolocation and demonstrate that the response to multiple sounds is not a simple linear addition of the response to single sounds. By developing functional models of the bat echolocation system, we can study the efficient implementation demonstrated by nature. For example, variations among analog VLSI circuit units due to the unavoidable transistor mismatch ? traditionally thought of as a hurdle to overcome ? have been found beneficial in generating the desired diversity of response that is similar to their neural counterparts. This work advocates the use and design of summating and exponentially decaying synapses. A compact and easily controllable synapse circuit has found an application in achieving a linear temporal spike summation by operating with a very short time constants. It has also been applied in modeling a nonlinear intensity-latency trading by working with a long synaptic time constant. We propose a new synapse circuit model that is compatible with those used in computational models and implementable by CMOS transistors operating in the subthreshold region.

15. SUBJECT TERMS

16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT	18. NUMBER OF PAGES	19a. NAME OF RESPONSIBLE PERSON
a. REPORT **unclassified**	b. ABSTRACT **unclassified**	c. THIS PAGE **unclassified**	**Same as Report (SAR)**	**201**	

Standard Form 298 (Rev. 8-98)
Prescribed by ANSI Std Z39-18

tion and demonstrate that the response to multiple sounds is not a simple linear addition of the response to single sounds. By developing functional models of the bat echolocation system, we can study the efficient implementation demonstrated by nature. For example, variations among analog VLSI circuit units due to the unavoidable transistor mismatch – traditionally thought of as a hurdle to overcome – have been found beneficial in generating the desired diversity of response that is similar to their neural counterparts. This work advocates the use and design of summating and exponentially decaying synapses. A compact and easily controllable synapse circuit has found an application in achieving a linear temporal spike summation by operating with a very short time constants. It has also been applied in modeling a nonlinear intensity-latency trading by working with a long synaptic time constant. We propose a new synapse circuit model that is compatible with those used in computational models and implementable by CMOS transistors operating in the subthreshold region.

BAT AZIMUTHAL ECHOLOCATION USING INTERAURAL LEVEL DIFFERENCES: MODELING AND IMPLEMENTATION BY A VLSI-BASED HARDWARE SYSTEM

by

Zhiping Shi

Dissertation submitted to the Faculty of the Graduate School of the
University of Maryland, College Park in partial fulfillment
of the requirements for the degree of
Doctor of Philosophy
2006

Advisory Committee:

Professor Timothy K. Horiuchi, Chair/Advisor
Professor Pamela Abshire
Professor Cynthia F. Moss
Professor Robert W. Newcomb
Professor Shihab A. Shamma

DEDICATION

To my parents.

ACKNOWLEDGMENTS

I wish to express my deep gratitude to my advisor Dr. Timothy Horiuchi for teaching me the fine art of circuit design and introducing me to the fascinating world of neuroscience. His support, encouragement, and guidance have made this dissertation finally possible. I am strongly influenced by his passion about science, excellence in engineering, and sincerity in academia. I have benefited greatly from his teaching about doing scientific research. For example, on numerous occasions he has convinced me that intuition and common sense can lead to insights beyond equations. Many a time, he has pointed out the importance of having a vision for a big picture when working on a large system level project. Yet on many other situations such as debugging a test board or analyzing weird behavior of a circuit, he has so elegantly shown me his sharp observation on subtleties.

I wish to thank Dr. Shihab Shamma, Dr. Cynthia Moss, Dr. Pamela Abshire, and Dr. Robert Newcomb for serving on my dissertation committee and for providing many insightful comments on my dissertation. My special thanks go to Dr. Nicholas DeClaris, who served on my dissertation committee and provided advice and encouragement until the very end but was not able to attend my defense. I also thank Dr. Jonathan Simon for his helpful advice on my work. I am beholden to Dr. Gary Rubloff for his welcoming me to Maryland and teaching me semiconductor manufacturing for the first two years.

I am grateful to many teachers, staff, colleagues and friends who have helped me in different ways over the years. In particular, my technical discussions with people in the Neural Systems Lab, the Auditory Neuroethology Lab, and the Integrated Biomorphic Information Systems Lab have been of enormous help. I have had the good fortune to have Matthew Cheely, Hisham Ahmed Abdalla, and Tarek Massoud to work together with in the lab. They are always ready to give me a hand when I am in difficulty. I would like to acknowledge the contributions to my thesis work from Kaushik Ghose for designing an early version PCB board, Murat Aytekin for providing measured HRTF data of bats, and Jeffrey Lee for designing the microcontroller PIC. I especially thank Matthew Carlberg and Marc Goldman for painstakingly reading and commenting upon the manuscript. I also thank Dorothea Brosius for help in using LaTeX template style files.

I finish my thesis work in a pleasant and supportive family environment. My wife, Jin Sun, has shown me the great value of patience and understanding. Without her care and support, my research would be much more difficult. My parents-in-law have always encouraged me. My daughter Jessica and my son Jeffrey have brought me additional inspiration by their curiosity of the unknown world. I am so indebted to my parents, to whom this dissertation is dedicated.

This work was funded by the Air Force Office of Scientific Research and by the National Science Foundation.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

LIST OF ABBREVIATIONS

AER	address event representation
AVCN	anteroventral cochlear nucleus
CF	constant-frequency
DNLL	dorsal nucleus of the lateral lemniscus
EI	excitatory-inhibitory
EI/F	facilitated EI
FM	frequency-modulated
GBC	globular bushy cell
HRTF	head-related transfer function
IC	inferior colliculus
ILD	interaural level difference
ILDci	the ILD of complete inhibition
ITD	interaural time difference
LSO	lateral superior olive
MNTB	medial nucleus of the trapezoid body
SBC	spherical bushy cell
SC	superior colliculus
SPL	sound pressure level

Chapter 1

Introduction

Bats have long fascinated engineers due to their ability to use an unusual sensory modality known as echolocation to fly in complete darkness with speed and agility through complex natural environments. With the success of radar and underwater sonar, engineers and roboticists have been developing systems that perform echolocation in water and in air for many decades, yet little is known about how computations are performed by their biological counterparts (e.g., toothed whales and microchiropteran bats) and how they are able to outperform even the best man-made systems.

This work describes a modular VLSI implementation of a neural model for emulating the bat azimuthal localization ability with short echolocation sounds. By constructing real-time spiking neural models, we intend to develop tools for experimentation with these neural algorithms in closed-loop robotic systems. By developing functional models of the bat echolocation system, we hope to emulate the efficient implementation demonstrated by nature and suggest new experiments with bats.

1.1 Statement of the Problem

Sound localization, the task for an animal to determine where the sounds it hears come from, is critical for the survival of most animals. Sound localization is particularly important to bats, who rely more than most other mammals on hearing to interact with the external world. Bats localize objects by emitting a short duration ultrasonic frequency sound and listening to echoes from objects. The echo delay provides information about the distance of the object, whereas the amplitude and spectrum of the echo can provide information about the geometrical properties of the object. With two spatially-separated ears, a comparison of arriving signals provides information about the direction of echoes. In this work, we focus on the neural computations underlying azimuthal localization.

While azimuthal localization studies of other larger animals have demonstrated a reliance on a mixture of interaural time differences (ITDs) and interaural level differences (ILDs), bats are believed to be dependent mostly on the interaural level difference cue due to the close spacing of their ears which does not create a significant interaural time difference. On the other hand, at the ultrasonic frequencies that bats use, sounds are significantly attenuated by the head, snout, and body to produce a useful ILD cue for localization. These short wavelengths are also well suited to produce useful reflections from small insects. Such high frequency sounds are, however, quickly attenuated in air and limit the maximum perceptual range of the bat. In addition, bats require specialized cochleae structures to extend their hearing well above 100 kHz.

ILDs are first processed in the lateral superior olive (LSO). ILD information is further processed in the dorsal nucleus of the lateral lemniscus (DNLL) and the inferior colliculus (IC). In spite of a great number of studies on ILD processing in bat brainstem and midbrain in the past several decades, the exact nature of ILD transformations along the pathway from LSO, DNLL to IC remains unclear (Pollak et al., 2003). On the one hand, these three ILD processing centers share numerous similarities. They all contain a large number of neurons receiving excitation from one ear but inhibition from the other ear (EI neurons). Moreover, response properties of IC EI neurons resemble that of neurons in the lower nuclei where the IC EI neurons receive their innervation (Klug et al., 1995). A question would thus be why the IC simply copies the EI properties from its lower stages. On the other hand, numerous studies have revealed that inhibition shapes EI properties in the IC through the convergence of multiple projections from lower stages (Pollak et al., 2002). However, the existence of a series of monaural and binaural pathways that converges in the central nucleus of the inferior colliculus has made the identification of specific interconnections that form EI properties in the IC very difficult due to the limitation of current neurobiological experimental technique.

The bat echolocation system is remarkable for the short time scale at which it must operate. The firing rate of a neuron is conventionally considered to be the metric of the response. The short sonar vocalizations of bats (a few ms) and their fast flight speed (about 2 m/s), however, suggest that the auditory nervous system of the bat does not have the time to average spikes over time. Neurons in the brainstem typically fire only one or two spikes in response to a short duration

echo (Park, 1998). One important element that is missing in our understanding of ILD processing in bat echolocation is the role of timing. While it was hypothesized long ago that intensity can be traded as time and this intensity-latency trading may play a critical role in ILD processing (Yin et al., 1985; Pollak, 1988), it is not until recently that neurobiological experiments have studied indirectly to what extent the intensity-latency trading affect ILD processing in mammals (Irvine et al., 2001; Park et al., 1997; Park, 1998). In particular, the role of spike timing in the response of neurons to realistic stimuli, extended echoes and multiple targets is just now being explored in the neurophysiological literature.

The fact that neurons in the bat respond to short echoes by one or two spikes strongly suggests that it is the population response of these neurons and perhaps the timing, or latency of these spikes that encode the information about the target. Although it is widely accepted that ILDs are the cues for bat azimuthal echolocation, which neural coding scheme is used by bats to compute azimuth in the superior colliculus (SC) or in the cortex remains one fundamental question. While the neural representation of auditory space in the barn owl's IC, especially the role of the external nucleus of inferior colliculus (ICx) is clear (Manley et al., 1988; Cohen and Knudsen, 1999; Gold and Knudsen, 2000), mammals do not seem to have a significant ICx, nor do cells in the ICx have a particularly sharp spatial tuning. The current understanding of coding for auditory space in mammals comes primarily from studies using ferrets and cats (King and Carlile, 1995; Schnupp and King, 1997). Given that auditory information will be used to ultimately drive the SC both directly and via cortex to orient the head and pinnae, it remains a question

how functional spatial tuning can be achieved from the sigmoidal responses of EI cells.

1.2 Motivation and Significance

Understanding how neural systems can perform sound localization has been one of the major goals in auditory neurobiological research (Yin, 2002). The goal of this work is to study bat azimuthal echolocation by a VLSI-based hardware model. In contrast to models seeking to accurately study the biophysics of a single cell (e.g. Zacksenhouse et al., 1998; Szalisznyó, 2006), we emphasize the network dynamics among EI neurons in the LSO, DNLL and IC. A few researchers have also studied ILD processing in the LSO and DNLL using network models (e.g. Reed and Blum, 1990; Reed and Blum, 1999), but those models consider only the steady-state response of neurons. As a result, the role of spike timing in ILD processing has been neglected.

The significance of this work lies in two aspects. First, from the point of view of general neural computation, the short pulse of sound used for echolocation creates a representational challenge for the brain because individual neurons in the bat's auditory system generally do not produce more than one or two spikes in response to a short echo. This constraint on the neural representation of stimuli intensity may hold a key to understanding role of the spike timing in bat ILD processing in particular and in mammalian auditory processing in general. This is timely research given the battles currently raging in the cortical processing community over the role

of spike timing and synchrony in computation. This research aims at contributing to neural computation research by studying the role of spike timing and the importance of synaptic and network dynamics.

Second, by including many of the possible interconnections among the three ILD processing centers – LSO, DNLL, and IC – and with the ability to work with real world signals, this work will be valuable to the bat research community by providing a real-time bat echolocation simulator that can be used to address system-level performance of low-level neural algorithms. Moreover, by the neuromorphic VLSI approach that will be discussed in the next section, this work hopes to benefit the engineering community by illustrating how the bat's superb echolocation abilities are implemented in neural hardware given certain limitations of neural processing.

1.3 Neuromorphic VLSI

Beginning in the early 1980s, Professor Carver Mead at California Institute of Technology advocated an approach that uses the latest CMOS technology to emulate and understand neurobiological circuits. This approach of designing computational systems to emulate the morphology and function of nervous systems has come to be known as neuromorphic engineering (Mead, 1990). Successful examples include a silicon model of the retina and visual cortex (Boahen, 2005), and a silicon model of cochlea and bionic ear (Sarpeshkar, 2006). An example neuromorphic system that integrates both fast sensory processing and fast motor control is a one-dimensional hardware model of the primate oculomotor system (Horiuchi and Koch, 1999).

The growth of the neuromorphic engineering community is to a large extent due to the encouraging results of silicon models of the early auditory system. The pioneering work on the silicon cochlea by Lyon and Mead (1988) has influenced many researchers to pursue the analog VLSI approach. Silicon models of the auditory system include cochlea (Watts et al., 1992; van Schaik et al., 1996; Sarpeshkar et al., 1998), the auditory periphery (Liu et al., 1992), and cochlea nucleus bushy cell (Wittig and Boahen, 2006). Lazzaro proposed a silicon model of azimuthal localization of the barn owl using interaural time differences (Lazzaro and Mead, 1989). A silicon model of amplitude-modulated acoustic stimulus processing in the auditory system involving inner-hair cells, ventral cochlear nucleus, sustained-chopping stellate cells, and coincidence-detecting neurons in the central nucleus of the inferior colliculus was proposed by (van Schaik and Meddis, 1999). This dissertation work seeks to incorporate many of these ideas as part of an ongoing, larger project of neuromorphic VLSI modeling of bat echolocation, constructing a flying bat-sized creature that uses ultrasonic echolocation to both navigate and scrutinize its environment sufficiently to distinguish between obstacles and "insects" (Horiuchi, 2005).

The underlying philosophy and methodology for this dissertation research is to study animal behavior by way of neuromorphic VLSI-based robotics or hardware systems. This methodology is promising because robots can be designed to share the same characteristics of animals: they are both dynamic behaving systems that can carry out various tasks in a complex and ever-changing world. Many will ask the questions: why not just perform computer simulation and what is the added

value for hardware implementation? First, hardware modeling can often provide different perspectives from computer simulation. For example, the complexity of real world input (e.g. the ultrasonic echoes from object) is often difficult to simulate in the computer. The interaction of the sonar device moving in the real environment is also difficult to capture properly. Secondly, biological systems are significantly more efficient in using resources of energy, time, and space to perform very complex tasks. By designing and building hardware systems that must operate under similar constraints as biological systems, we can gain some insight into the tradeoffs and optimizations that evolution has used to produce organisms with brains of unprecedented computational speed, complexity, low power consumption, and small size.

Neuromorphic VLSI modeling uses analog and digital circuits to mimic the massively-parallel computations seen in neural systems. At individual neuron level, neural computation is of relatively low precision. Analog VLSI circuits can easily provide efficient low-precision computations. In addition, the unavoidable mismatch of transistor characteristics on the fabricated die, traditionally a hurdle to overcome, can generate the desired diversity of responses among a population. At the system level, adaptability of connections and parameters are ubiquitous in neural systems. For this, digital technology can provide reconfigurability for spiking neuron outputs.

1.4 Dissertation Overview

The dissertation is organized as follows. Chapter 2 constitutes a summary of the background that is pertinent to the dissertation. We introduce basic concepts in the general context of spatial hearing and fundamental behavior of bat echolocation. This chapter focuses on facts and data from biological literature about ILD processing in the LSO, DNLL and IC.

The neuromorphic VLSI bat azimuthal echolocation system is described in Chapter 3. We first present the system model and the implementation architecture. We then describe a sensor front-end, an operational amplifier based circuit that provides the converging inputs to the LSO from a population of AVCN cells. A CMOS VLSI chip with address-event representation (AER) protocol communication was developed to implement a three-layer spiking neural network model of bat ILD processing in the LSO, DNLL, and IC. Chapter 3 gives a detailed description on the spiking neuron model and its circuit implementation and parameter analysis. Circuits for different EI cells in the LSO, DNLL and IC are given, but the analysis is left for later chapters.

The complete description of our circuit model for ILD computation in the LSO, DNLL and IC is accomplished in Chapter 4 and Chapter 5. In Chapter 4, we discuss mechanisms underlying LSO EI cell's sensitivity to ILD, provide an overview of some existing LSO models, and point out the importance of spike timing in ILD processing. We present an LSO circuit model that employs first spike latency to encode ILD information and show chip test examples of how we can generate a

diversity of LSO EI cell responses. In Chapter 5, we present modeling of EI cells in the DNLL and IC, with an emphasis on how EI properties can be modified or created *de novo* in the IC. We study how more spatially selective properties can be achieved in the IC through the three-layer network transformation. For this purpose, we illustrate our circuit model of facilitated EI cells (EI/F) and show the population response to a real target.

In Chapter 6, utilizing the neuromorphic system with real targets, we explore to what level of detail and accuracy multiple echoes can affect bat's azimuthal echolocation. We approach this question by considering separately whether two targets are on the same side or on different side of the midline of the bat. We show that when there exist objects on the same side of midline of the bat, the neuron's refractory period and subthreshold summation must be considered. For multiple objects on two sides of the midline of of the bat, we show the role of the long-lasting cross-inhibition of the DNLL.

The neuromorphic ILD system described uses a very compact synapse circuit. In order for this synapse circuit to perform temporal spike summation in our LSO modeling, we have to operate the synapse in a very rapidly decaying mode. In Chapter 7 we describe a novel CMOS synapse design that aims at both exponential decaying and linear temporal spike summating. This circuit implements part of a commonly-used kinetic model of synaptic conductance. We show theoretical analysis and experimental data for prototypes fabricated in a commercially-available 1.5μm CMOS process.

In chapter 8 we summarize the contributions of this study to biological mod-

eling as well as to engineering. We suggest some future directions to extend this dissertation work.

Chapter 2

Background

The emphasis of this chapter is to summarize biological data related to processing and transformation of interaural level difference (ILD) in three centers: the lateral superior olive (LSO), the dorsal nucleus of the lateral lemniscus (DNLL) and the inferior colliculus (IC). Basic concepts in the general context of spatial hearing and fundamental behavior of bat echolocation are also introduced.

2.1 Acoustic Cues for Sound Localization

In the most general framework, this research belongs to the domain of spatial hearing, the study of human and animal ability to use sonic cues to estimate the spatial location of a target. The classical duplex theory proposed by Lord Rayleigh is a model for estimating a free-field target's spatial location by two binaural cues: interaural time difference and interaural level difference (Blauert, 1997). An interaural time difference (ITD) is defined as the difference in arrival times of a sound's wavefront at the left and right ears. The interaural level difference (ILD) is defined as the amplitude difference generated between the right and left ears by a sound in the free field due to a frequency-dependent attenuation. This simple duplex

theory successfully explains the perception of azimuth of sounds originating from the horizontal plane, but cannot well specify a unique spatial location in elevation and range. It is now widely thought that there are three acoustical cues to sound source location: ITDs, ILDs, and spectral cues. The spectral cues are primarily for localization of sound along the vertical dimension (Yin, 2002).

When sounds reach the ear, they are transformed due to their interactions with the head, pinnae, and other parts of the body. This transformation is frequency and direction dependent and is often modeled as a linear time-invariant system transfer function known as the head-related transfer function (HRTF). HRTF is defined to be a specific individual's binaural far-field frequency response, as measured from a specific point in the free field to a specific point in the ear canal (Cheng and Wakefield, 2001). As an example of the frequency and direction dependence of the binaural response, we compute the theoretical ILDs from the HRTF for a rigid spherical head model. Fig. 2.1 shows ILD curves of three different frequencies for a rigid sphere of diameter of 2 cm at distance of 1 m. It is computed by Matlab based on the equations listed in Appendix A. We can gain some insights from this figure. First, we see that the ILD curve is frequency dependent; the slope generally increases as frequency increases. Second, there is a range of directions in which ILD (in dB) is a unique mapping of the azimuth. This unique mapping between ILD (in dB) and azimuth direction is the foundation for azimuthal localization using ILD. Third, the interference effects caused by waves propagating in various directions introduce ripples at the edges of the ILD curves, which will produce ambiguity in estimating azimuth.

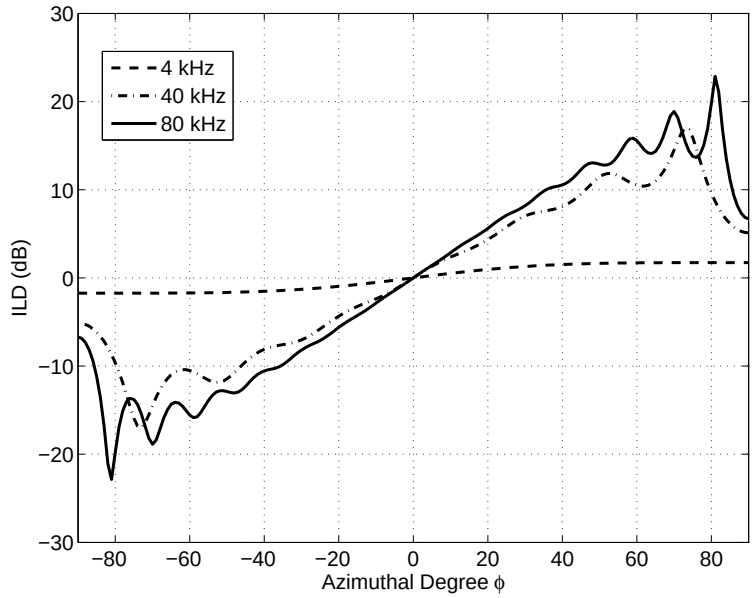


Figure 2.1: Theoretical ILD of the spherical head model. ILD at three frequencies are computed for a sphere of diameter 2 cm at distance of 1 m. The two ears are assumed to be located at $\beta = \pm 90°$. See Appendix A for equations used to plot this figure.

This work studies interaural level differences, the cues for azimuthal localization of high frequency sound (Yin, 2002). Since the term interaural intensity difference (IID) has often been used in place of ILD in the literature (e.g. Park, 1998; Irvine, 1992), we clarify that it is the sound pressure level (SPL) difference between two ears that is measured (Irvine, 1992). The sound pressure level is a measure of the rms pressure of a sound, defined as (Blackstock, 2000)

$$SPL = 20 \log_{10} \frac{p_{rms}}{p_{ref}} dB \tag{2.1}$$

where p_{ref} is a reference pressure. Therefore, ILD can be mathematically defined as the SPL in the ipsilateral (same side of the head) ear minus the SPL in

the contralateral (opposite side of the head) ear, that is

$$\begin{aligned} ILD &= 20\log_{10}\frac{p_{rms\_ipsi}}{p_{ref}} - 20\log_{10}\frac{p_{rms\_contr}}{p_{ref}} \\ &= 20\log_{10}\frac{p_{rms\_ipsi}}{p_{rms\_contr}} \quad (dB) \end{aligned} \tag{2.2}$$

2.2 Bat Echolocation

2.2.1 Characteristics

Echolocating bats are nocturnal mammals with the ability to orient and find food in the complete darkness. This owes to their use of echolocation, a word coined by Griffin to describe the process of locating obstacles by means of echoes (Griffin, 1944). Bat echolocation starts with emitting high frequency sounds. The frequency range of most echolocation signals is 25 to 100 kHz (Moss and Schnitzler, 1995). While some bats use a constant-frequency component preceding a frequency-modulated (FM) signal component ("CF/FM bat"), most bats use short frequency-modulated (FM) calls ("FM bats"). Because CF/FM bats also emit FM signal components, FM pulses may be used for all bats for target echolocation (Grinnell, 1995).

The prey capture process of the bat, in the laboratory or in the field, can be divided into search, approach, and terminal phases (Surlykke and Moss, 2000; Moss and Sinha, 2003). Bats change their pulse design through these three phases. For FM bats, pulses are about 3-12 ms long and are emitted at 2-10 Hz. During the approach phase, FM bats increase pulse repetition rate and shorten pulse duration. In the terminal phase, the pulse repetition rate can be as high as 200 Hz, and

the pulse duration can be as short as 0.5 ms (Grinnell, 1995; Pollak et al., 1977). For CF/FM bats the CF portion of the pulses is progressively shortened such that in some species only FM components of the pulses are left during the final stages (Grinnell, 1995).

Neurons in the bat typically respond to short durations of FM pulses by no more than one spike. In one study on *Eptesicus fuscus*, an FM bat, when using a 2-ms tone burst at the best frequency (BF) or a downward FM sweep encompassing BF, most neurons respond with an average of just one spike for each stimuli presentation (Ferragamo et al., 1998). In that study, 91% of IC neurons responded once per trial for 2-ms FM bursts. Only 7% of IC neurons responded to 2-ms tone burst with several spikes in a chopper-like pattern. But when these neurons stimulated by 2-ms FM sweep, these chopper units responded with only one or two spikes per trial. In studies on the Mexican free-tailed bat, a CF/FM bat that uses CF components for target detection in the search phase but emits short FM sweep pulses for localization during the approach and terminal phases, most neurons in the inferior colliculus typically responded to an FM sweep of about 5 ms duration by no more than four spikes (Pollak et al., 1978; Pollak et al., 1977). All tested neurons in the lateral superior olive (LSO) responded to 2-ms FM sweep by 1-2 spikes (Park et al., 1996).

2.2.2 Cues for Bat Azimuthal Echolocation

The head size of most echolocating bats is small (about 1 to 2 cm). The maximum interaural time differences (ITDs) for most bats are about 50 μs or less (Grinnell, 1995). The fact that some neurons stimulated by high-frequency tones (18-90 kHz) in the auditory system of the echolocating bat *Molossus ater* were found to be sensitive to small ITDs down to $\pm 50 \mu s$ has led to the hypothesis that bats uses both ITDs and ILDs for determining the azimuth of sound source (Harnischfeger et al., 1985). However, we point out the sample size was very small. Only 8 from 76 units in the central nucleus of the inferior colliculus (ICc) and 1 from 74 units in the superior olivary complex (SOC) were found to be sensitive to ITDs of $\pm 50 \mu s$.

The results that some neurons in the bat were sensitive to small ITDs were interpreted differently by Pollak (1988). Specifically, he suggested that the ITD is so small compared with those seen in time-intensity trading that it is inconsequential in shaping the response of a neuron. In his study on the Mexican free-tailed bats, neurons in the inferior colliculus were found to be sensitive to ITDs of 40-60 μs. Pollak explained why ITDs cannot be the cues for azimuth. First, the specific bat under test, the Mexican free-tailed bats have a head width of only 0.8 cm and thus the maximum ITD is only 30 μs. Second, a change of ITD between two azimuths will produce a significant change of ILD that in turn will produce much larger time disparity due to the time-intensity trading. For example, it was estimated that for a change in sound from 20° to 40° would cause a change of ITD from 8 μs to 16 μs and a change of ILD by 13 dB. A change of the azimuth of the sound source from

0 to 20° would create a change of ITD of only about 8 μs, but a change of ILD of 27 dB. The time-intensity trading ratio was measured to be 40 μs/dB so it is clear that the disparity of the arrival time of the actual sounds plays little role in shaping the response properties of these neurons (Pollak, 1988).

Sound frequency is also an important factor. For example, while human subjects can detect ITDs of the carrier component of sound stimuli at very small values (less than 20 μs), this is true only for sound frequencies below about 1.5 kHz (Joris and Yin, 1998). At low frequencies, ITD sensitivity requires phase locking of the auditory nerve fiber to the wavefront. At the ultrasonic frequencies as the bat uses, hair cells of the cochlea are believed to be unable to reliably transmit the phase information. Because of the small head size of the bat and its use of high frequency sound, ILD is considered to be the primary cue for azimuthal echolocation in bats.

Fig. 2.2 shows a measured ILD curve for an *Eptesicus fuscus* bat head (FM bat). It shows the ILD as a function of azimuth at two frequencies (30 kHz and 40 kHz) with an elevation angle of 0°. It shows about ±60° of monotonic azimuth range and a ±30 dB ILD value range. It was reported that in the mustache bat, there is about ±40° monotonic azimuth range and a maximum of ±30 dB ILD range (Park and Pollak, 1994; Fuzessery and Pollak, 1985). In general, the ILD versus azimuth relationship behaves monotonically under 40 kHz (Aytekin et al., 2004), but this relationship becomes more complex above 40 kHz and can cause the monotonic behavior to disappear.

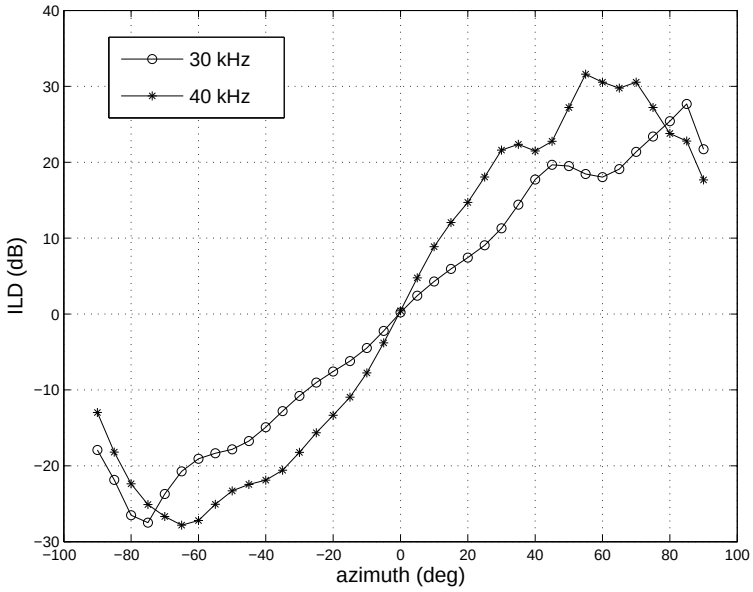


Figure 2.2: Measured ILD versus sound-source azimuth from an echolocating FM bat (*Eptesicus fuscus*). The elevation of the source is 0°. (Courtesy of Murat Aytekin and Cynthia Moss of the Auditory Neuroethology Laboratory, University of Maryland.)

2.3 ILD Processing in Bats

2.3.1 The ILD Processing Pathway

Fig. 2.3 shows ILD processing pathway through the brainstem and midbrain of echolocating bats. ILDs are first coded by neurons in the lateral superior olive (LSO). The LSO receives its principal excitatory inputs from the ipsilateral ear and inhibitory inputs from the contralateral ear (Covey et al., 1991; Park et al., 1997). The excitatory input to the LSO is provided by the spherical bushy cells (SBCs) of the anteroventral cochlear nucleus (AVCN). The neurons in the medial nucleus of the trapezoid body (MNTB) provide glycinergic inhibitory input to the LSO. The MNTB receives excitatory input from globular bushy cells (GBCs) in the contralateral AVCN. The input to MNTB from the globular cell is in a one-to-one

manner that terminates in large calyx of Held (Covey and Casseday, 1995).

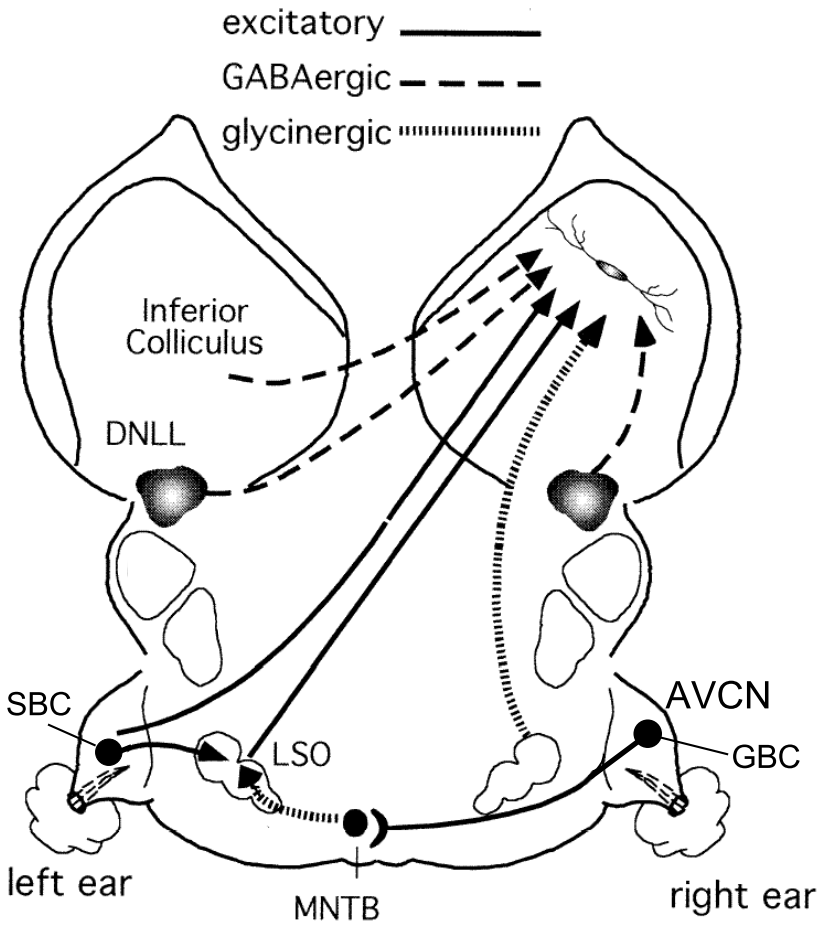


Figure 2.3: The ILD processing pathway through the brainstem and midbrain of the echolocating bat. From neurons in the anteroventral cochlear nucleus (AVCN), ipsilateral excitation and contralateral inhibition (via the medial nucleus of the trapezoidal body, or MNTB) converge on the LSO where the first binaural interaction occurs. The LSO and cochlear nucleus project to both the dorsal nucleus of the lateral lemniscus (DNLL) and to the inferior colliculus (IC) to create responses that allow azimuthal localization. SBC: spherical bushy cell. GBC: globular bushy cell. Adapted from Pollak et al. (2002).

Although the LSO and MNTB in the bat are unusually large relative to the size of the brainstem, the LSO and MNTB are virtually identical to those of other mammals in terms of patterns of connections and patterns of input from the cochlear

nucleus (Covey and Casseday, 1995). It is noteworthy that studies on other mammals reveal that input signals from two sides arrive at the LSO at a small time difference. In spite of the longer path and extra synapse for the input from the contralateral ear, on average, the contralateral signal arrives at the LSO only 0.2 ms later than the ipsilateral signal (Joris and Yin, 1998).

The encoded ILD information is then conveyed from the LSO to ascending nuclei. The dorsal nucleus of the lateral lemniscus (DNLL), shown in black, consists of a large portion of ILD-sensitive neurons. A DNLL cell receives excitation from the contralateral LSO, inhibition from the ipsilateral LSO. A DNLL cell also receives inhibition through commissural connections from the opposite DNLL (Covey, 1993; Yang and Pollak, 1994). The inferior colliculus (IC) also contains a substantial population of ILD-sensitive neurons. An IC cell receives excitation from the contralateral LSO and inhibition from the ipsilateral LSO. An IC cell receives GABAergic inhibition from both sides of the DNLL. In addition, the IC also receives inhibition through commissural connections from the opposite IC and excitatory innervation from a number of lower monaural nuclei (Pollak et al., 2002). The excitatory input to IC from lower monaural nuclei is shown generically as coming from the cochlear nucleus in Fig. 2.3.

2.3.2 The ILD Function

In bat ILD studies, an ILD-sensitive neuron is often characterized by the ILD function: the number of spikes an ILD-sensitive neuron fires for different ILD values.

In this dissertation, we use the convention that positive ILDs indicate that the sound is more intense at the excitatory ear than at the inhibitory ear and that negative ILDs indicate that the sound is more intense at the inhibitory ear. Fig. 2.4 shows an ILD function of a typical IC neuron and LSO neuron.

The smallest ILD that is able to completely suppress the spike activity is referred to as the ILD of complete of inhibition (ILD_{ci}). The ILD_{ci} is shown as the asterisk in each panel in Fig. 2.4. The ILD_{ci} has been found relatively invariant with stimuli changes such as duration and excitatory input level (Park et al., 1997). The ILD_{ci} is found to be the most important index of an ILD-sensitive cell's behavior. It varies among EI cell population in the LSO, DNLL, and IC. It is generally believed that this distribution of ILD_{ci} among neurons codes the azimuth information.

2.3.3 EI Cells in LSO, DNLL and IC

Responses of neurons to binaural inputs can be of several types. Irvine (1992) suggested using a convention system originated from Goldberg and Brown (1969) to classify different neuron response types. In this classification system, neurons are identified by a letter pair that specifies the effect of stimulation of each ear. The letter pair is in the order of contralateral first and ipsilateral second. Letter E means the input is predominantly excitatory, I means the input is predominantly inhibitory, and O for no effect.

The LSO is dominated by IE cells that receive excitation from the ipsilateral ear and inhibition from the contralateral ear. In one study on the mustache bat

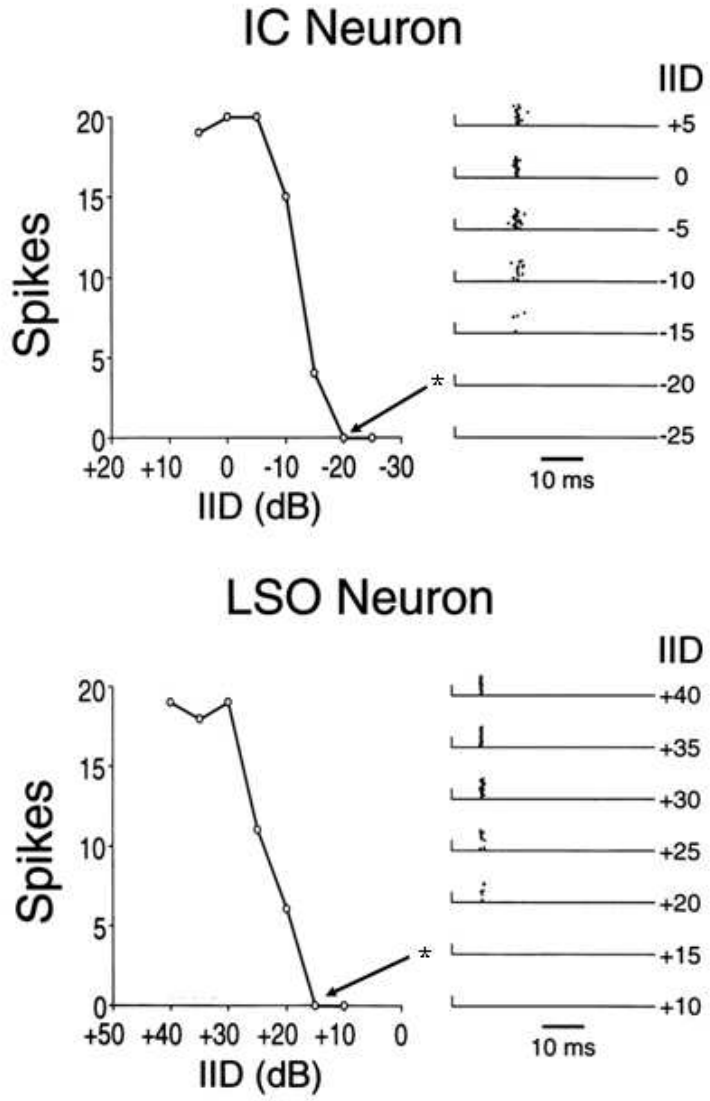


Figure 2.4: Typical ILD functions and corresponding raster plots. Top: ILD (IID in the figure) function (left) and corresponding raster plot (right) for a typical ILD-sensitive neuron from the IC. Bottom: ILD (IID in the figure) function (left) and corresponding raster plot (right) for a typical ILD-sensitive neuron from the LSO. Positive ILDs indicate a greater intensity at the excitatory ear. Stimuli were 2-ms long, 10-kHz downward frequency sweeps centered at each unit's characteristic frequency. Intensity to the excitatory ear was fixed at 20 dB above threshold, whereas the intensity to the inhibitory ear was varied. Each ILD was presented 20 times in pseudorandom order. Adapted from Park (1998).

(CF/FM bat) using pure tones, 93% of units tested were IE cells, and the remainder were EO type cells (Covey et al., 1991). It is noteworthy that most IE cells reach complete inhibition when inhibitory input is sufficiently large. In this study, the ILD of complete inhibition is about 0 dB. In a study on the Mexican free-tailed bat using 2-ms FM stimuli, ILDs of complete inhibition ranged from -40 dB (inhibitory ear more intense) to +20 dB (excitatory ear more intense), with a mean value of -6.6 dB for 50 units.

The large majority of cells in the DNLL are EI cells that receive excitation from the contralateral ear and inhibition from the ipsilateral ear. In one study of mustache bat, 88% of the binaural neurons tested in the DNLL were EI, and 18% of the binaural neurons were EE. 10% of EI neurons showed binaural facilitation and were classified EI/F cells. 86% of EI cells were inhibited by 90-100% when ipsilateral input was sufficiently strong (Markovitz and Pollak, 1994). In one study on *Eptesicus fuscus*, 57% of units tested were EI cells, 10% were EI/F cells, 12% were EE cells, and 16% were monaural type cells (Covey, 1993).

The IC also consists of many EI cells. In one study on Mexican free-tailed bat using 2-ms FM stimuli, the ILD of complete inhibition ranged from -40 dB (inhibitory ear more intense) to +20 dB (excitatory ear more intense), with an average of -18.0 dB. A noteworthy feature of EI cells in the IC is that ILDs of complete inhibition are topographically organized in the ventromedial region of the 60-kHz collicular contour (Wenstrup et al., 1986; Pollak and Park, 1995). In other words, there is a systematic representation of ILD values by the border that separates a region of discharging from a region of inhibited cells. At least 50% of the EI neurons

in the IC are either modified or created *de novo* in the IC through GABAergic inhibitory projections. The EI properties of the remaining IC cells are presumably imposed upon them through an excitatory projections from the contralateral LSO (Pollak et al., 2002). How EI properties can be formed in the IC through different projections from lower nuclei is an important topic of this study.

2.3.4 Spike Latency

While the sound arrival time differences between two ears of echolocating bats are too small to be used as cues for azimuthal echolocation, spike timing nevertheless plays an important role in ILD processing. Spike latency is input intensity dependent. Klug et al. (2000) studied latency as a function of intensity in bat auditory neurons. Fig. 2.5 shows average latency as a function of input intensity for three nuclei of Mexican free-tailed bats. This figure is plotted based on data in Klug et al. (2000). First spike latencies shown in the figure are the average from neuron samples in the LSO, DNLL and IC. The sample size for the LSO, DNLL, and IC are 58, 89, and 164, respectively. As pointed out by Klug et al. (2000), there are three features about the first spike latencies as a function of sound intensity. First, the higher synaptic level a nucleus was at, the greater average latencies regardless of the input intensity. Second, the variability of spike latencies among cells in the IC was greater than its lower nuclei, the LSO and the DNLL. Third, average latencies generally shortened with increasing input intensity in all three nuclei. The only exception to this feature was for the IC at intensity between 40 and 50 dB.

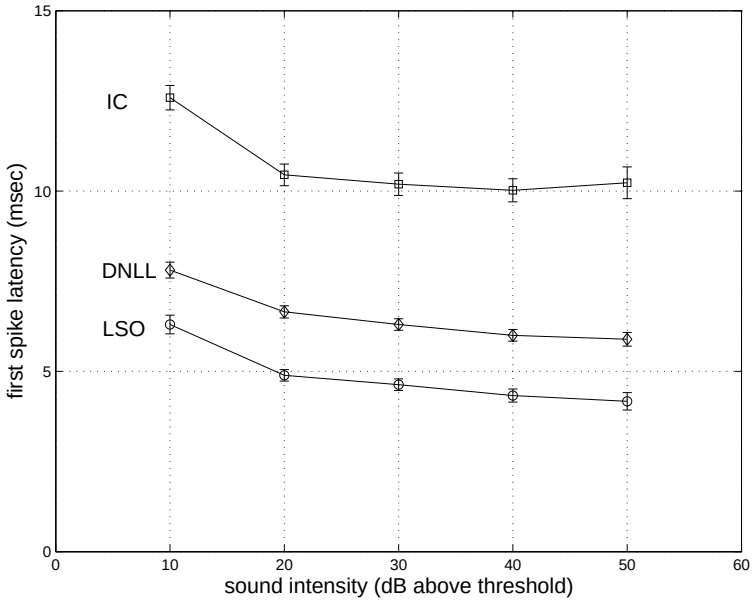


Figure 2.5: First spike latency as a function of excitatory stimuli intensity. Shown are averaged latencies over a sample of neurons in each nuclei. Error bars are standard errors over samples. Plots are based on data from Klug et al. (2000).

The relative timing of excitatory and inhibitory inputs to an EI cell helps to shape the cell's selectivity to ILD inputs. In the LSO of the Mexican free-tailed bat, latencies of inhibition of about half of tested EI cells were several hundred microseconds longer than that of excitation when strengths of excitation and inhibition were equal (Park et al., 1996). A majority of IC cells (88%) tested exhibited mismatched latency (Park, 1998). It is noteworthy that the latency mismatch in both LSO and IC is in one direction – the inhibition arrived later than excitation when the excitation and inhibition had the same strengths.

Chapter 3

Neuromorphic System Design and Analysis

Neuromorphic VLSI design strives to capture the essence of the neural computation in a specific biological system. In this chapter we present a neuromorphic VLSI system that emulates the ILD processing for azimuthal echolocation in bats. Our effort has been toward designing a neuromorphic bat ILD processing system that allows us to test neural algorithms in closed-loop and real-world conditions.

3.1 System and Architecture

We abstract the complex ILD processing in bats by a system model (Fig. 3.1) that includes many of the known connections among the three ILD processing centers — the LSO, DNLL, and IC. Our model is adapted for VLSI implementation, and emphasizes the processing and transformation of ILD information along the pathway through the LSO, DNLL, and IC. We have designed a neuromorphic VLSI based hardware system that mimics bat ILD processing for azimuthal echolocation. The neuromorphic system implements the system model shown in Fig. 3.1 by two forms of electronic design: a custom CMOS VLSI chip and operational amplifier (op amp) based circuits.

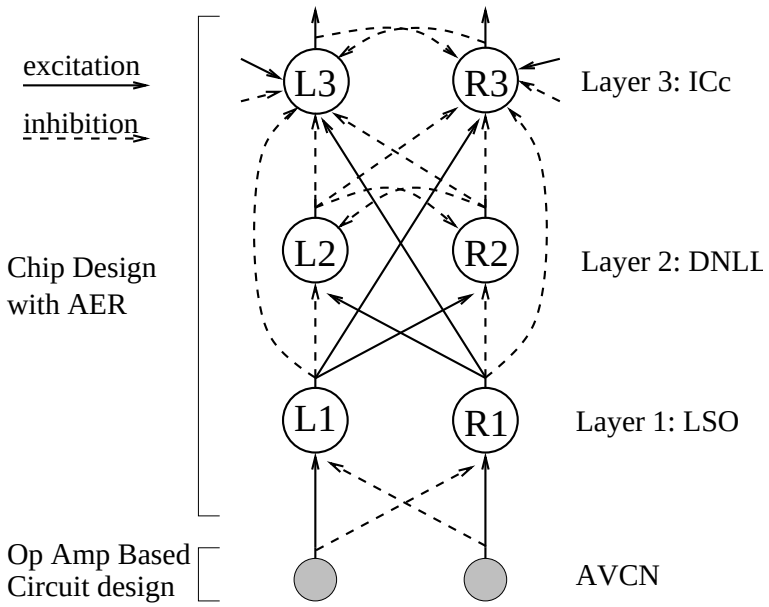


Figure 3.1: System model showing many of the known connections between the different layers of processing from AVCN up to IC. By selecting a subset of these connections, different neuron response types described in the literature can be created.

The three ILD processing stages are modeled by a three layer spiking neural network with connections shown in Fig. 3.1. The LSO is the first layer of the network. Each LSO cell consists of one spiking neuron with two synapses: one excitatory synapse for the input from the ipsilateral AVCN, and one inhibitory synapse for the input from the contralateral AVCN. An LSO cell provides excitatory input to the contralateral DNLL and IC neurons and inhibitory input to the ipsilateral DNLL and IC. In layer 2, each DNLL cell consists of a spiking neuron with one excitatory synapse for the input from the contralateral LSO, two inhibitory synapses: one for the input from the ipsilateral LSO, the other for the input from the opposite DNLL. In layer 3, each IC cell consists of one spiking neuron with one excitatory synapse for the input from the contralateral LSO and four inhibitory synapses for the inputs from the ipsilateral LSO, the ipsilateral and contralateral DNLL, and the

opposite IC. Each IC cell also has an extra excitatory and inhibitory synapse that are available to receive extra external inputs. We use these inputs to implement a particular network configuration that we will discuss later.

The three layer spiking neural network model uses the address-event representation (AER) interface (Boahen, 2000) for spike-based communication. This interface allows reconfigurability as well as a convenient interface for data acquisition. The AVCN in Fig. 3.1 provides the sonar signal input to the chip and was implemented by an op-amp-based circuit that is considered the sensory "front-end" for the chip.

In this section, we describe the architecture of the sensor front-end and the chip separately. We will describe the design and analysis of our front-end and chip with more detail in sections below.

3.1.1 Sensor Front-end

The sensor front-end is an operational amplifier (op amp) based circuit that generates the spiking input to the ILD multi-layer network chip. Fig. 3.2 is the block diagram of the front-end system.

The front-end begins with a sonar head that consists of one ultrasonic speaker and two ultrasonic microphones. Block P is a microcontroller (Microchip PIC 12CE674) that generates a brief 40 kHz pulse signal to drive the speaker. The PIC also sends a control signal to Block D which attenuates the microphone's reception of the outgoing sound. Block A is a two stage amplifier that amplifies the

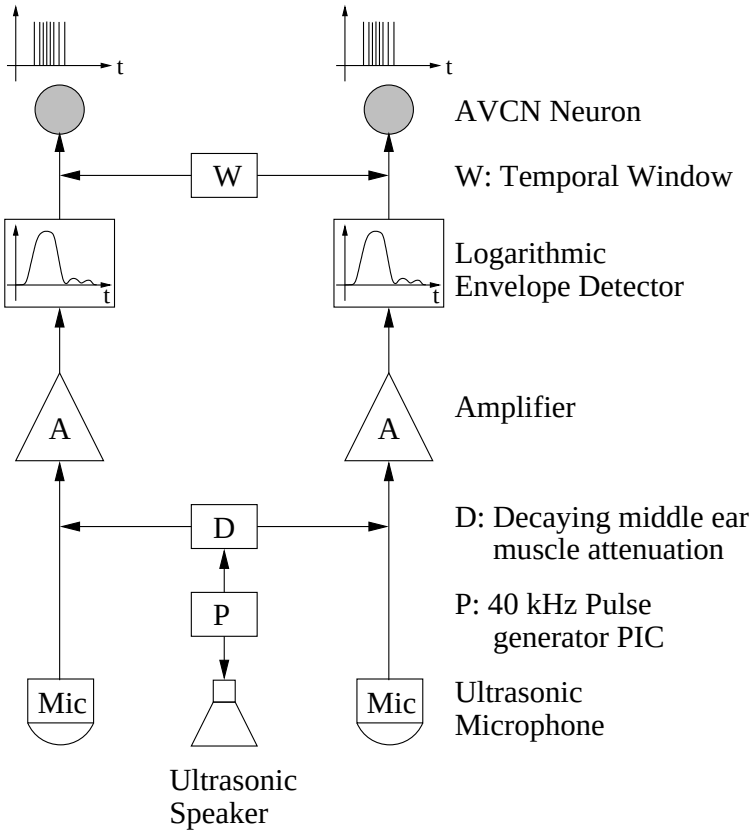


Figure 3.2: Sonar front-end block diagram. Short duration ultrasonic sounds emitted from the speaker produce echoes from objects that are detected and amplified. The amplitude is extracted from the signal and converted to an intensity-dependent pulse train as a simplified model of the cochlea and a population of anteroventral cochlear nucleus (AVCN) cells.

signals to the dynamic range of the envelope detector. We will describe the Envelope Detector and AVCN Neuron blocks in more detail later. Block W is a circuit that generates a temporal window to block out echoes from distant objects in the background objects behind the experiment targets.

3.1.2 Multi-layer Network Chip Architecture

The multi-layer neural network model in Fig. 3.1 has been implemented on a single chip, and its architecture is illustrated in Fig. 3.3. There are three primary

design considerations. First, our chip design should allow many different combinations of ILD processing interconnections. Our chip implementation is not designed for any specific ILD processing pathway; rather, it will be used for exploring how different connections in the multi-layer network affect the processing and transformation of ILD information. Secondly, the chip should be designed to work with different spiking input sources. In this study, the input to the chip is from two representative AVCN neurons, however, we anticipate the need for the chip to work with other inputs, such as a cochlear chip with an AER interface. Thirdly, the chip should be reconfigurable by external circuitry.

For the above considerations, we have designed the chip in two blocks. The first block (bottom box in Fig. 3.3) implements layer 1 and layer 2. We have designed each layer of the network with two arrays of 16 EI cells, one representing the left side of the bat's brain and one for the right. The four arrays of 16 EI cells forms a 4x16 matrix. This block uses a 4x16 AER transmitter for monitoring the spiking outputs as well as for providing the input spikes for the second block. The second block (top box in Fig. 3.3) implements layer 3 of the network model. We have designed layer 3 of the network with two arrays of 16 EI cells, one representing the left side of the bat's brain and one for the right. The two array of 16 EI cells forms a 2x16 matrix. Each cell in layer 3 receives four inputs from layer 1 and 2, through a 4x16 AER Receiver. Note that each address in the receiver is connected to two synapses in layer 3, one synapse on the left side and the other on the right side. The layer 3 output spikes are sent out of the chip using a 2x16 AER transmitter.

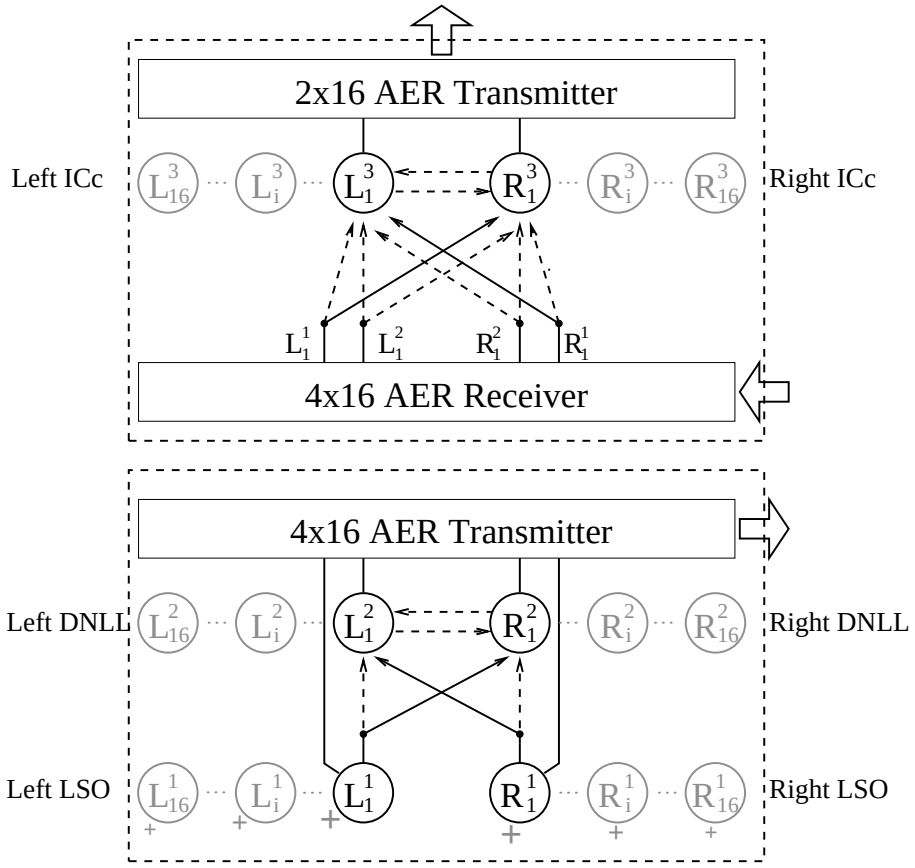


Figure 3.3: The neural connection infrastructure employed in the three-layer network chip. The chip is divided into two parts. The lower box (dotted line) implements layers 1 and 2 of the network with spike train inputs from (off-chip) left and right AVCN circuits. Each layer of the network consists of two arrays of 16 EI cells, one for the left side and one for the right. The 4x16 neurons of layers 1 and 2 communicate their spikes via a 4x16 address-event representation (AER) transmitter circuit. The upper box implements layer 3 which receives its input spikes via a 4x16 AER receiver circuit. Each address in the receiver is connected to two synapses in layer 3, one synapse on the left side and the other on the right side. Layer 3 communicates its output spikes via a 2x16 AER transmitter circuit.

The input spike trains to the chip are from the output of the front-end, the AVCN neurons. Fig. 3.4 illustrates the connection pattern from the AVCN to the LSO. Each LSO cell receives input through an excitatory synapse from the ipsilateral AVCN, and input through an ipsilateral synapse from the contralateral AVCN. Due to the limited number of I/O pins, we chose to use a global inhibitory weight and only vary the excitatory synaptic weight by a linearly spaced polysilicon resistor line inside the chip. This is illustrated by the "+" sign of varying sizes in Fig. 3.4.

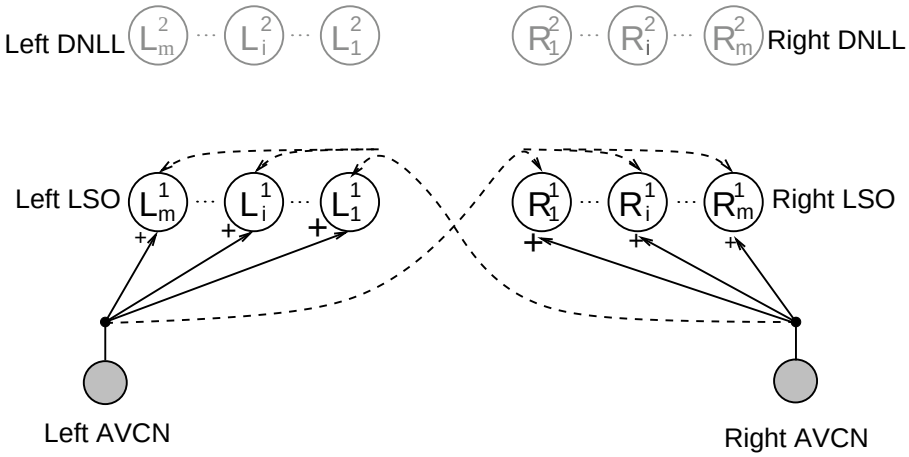


Figure 3.4: The LSO neuron array. Layer 1 (LSO) consists of the left and right halves of the LSO population, each with m neurons. The neurons of the left LSO array receive their inhibition from the right AVCN spike train with identical inhibitory synaptic strengths. The excitation from the left AVCN spike train, however, uses a gradient of excitatory synaptic strengths. Likewise, the neurons of the right LSO array have identical inhibitory synaptic inputs and a gradient of excitatory synaptic inputs.

The circuit was fabricated in a commercially-available 2-poly, 3-metal 1.5 μm technology. The chip test board has two chips installed with an interface to a custom AER "merge" board. We used a microcontroller (Microchip PIC 18F442) to perform this reconfigurable chip interface task.

3.2 Sensor Front-end Design and Analysis

3.2.1 Sonar Head Design

We used 40 kHz narrow-band ultrasonic transducers (Pro-wave Electronics Corporation in Taiwan) to construct the sonar head. We can predict the behavior of such an artificial bat head by analyzing the beam angle data of the microphone (the speaker has the same beam angle pattern). In such a bat head design, we consider three performance measures:

- maximum ILD value
- widest monotonic ILD range
- maximum ITD between two microphones

Fig. 3.5 is a photo of the sonar head design. The 40 kHz ultrasonic speaker is located in the center. The two 40 kHz ultrasonic microphones are located $\pm 35^\circ$ away from the center speaker.

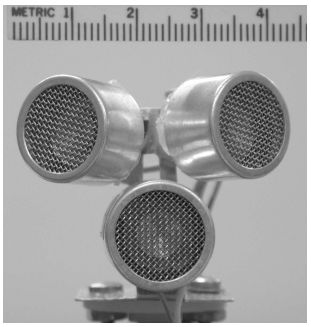


Figure 3.5: Photo of the model sonar head. A 40 KHz ultrasonic speaker is pointed straight forward and two 40 KHz microphones are pointed 35° off-center.

Fig. 3.6 shows the measured ILD as a function of sound source azimuth. In this measurement, a vertically-oriented cylinder of 5 cm diameter was located 80 cm away from the speaker. Such a target produces a 2.5 ms 40 kHz AM signal (See Fig. 3.11 for example waveform). In this ILD measurement, the amplified echo signals (not the envelope signals) are used to represent the sound pressure received at the ear. The RMS values within 2.5 ms of the amplified echo signals are measured from the oscilloscope, and the ILD is computed using Eq. (2.2).

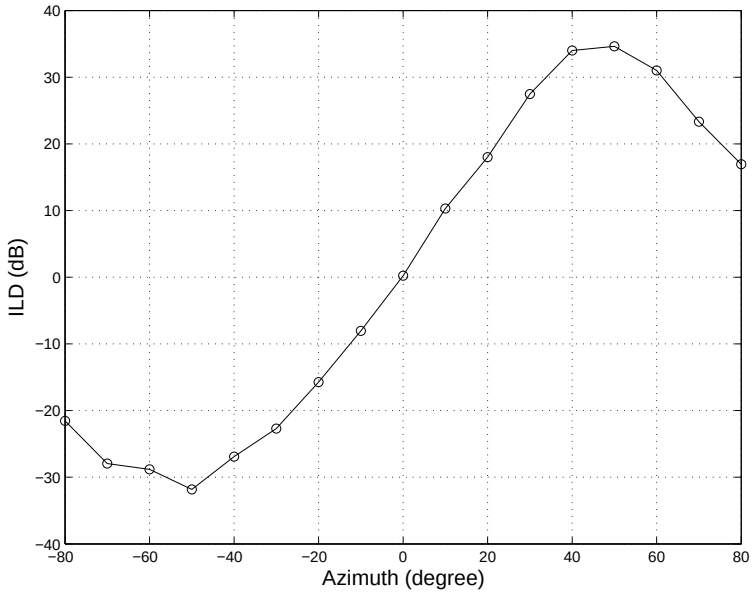


Figure 3.6: The measured ILD versus sound-source azimuth from the model sonar head in Fig. 3.5

3.2.2 Envelope Extraction and Level Representation

The front-end performs envelope extraction and level representation through circuitry with a key component, a monolithic logarithmic amplifier from Analog Device (AD640). This envelope-detecting log amplifier, often referred to as a demodulating logarithmic amplifier, demodulates the AM signal input and reports the

logarithm of the detected envelope at its output.

For an AM input v_{in}, the logarithmic circuit implements a transfer function in the form:

$$v_o = V_y \log_{10} \frac{v_{in}}{V_x} \tag{3.1}$$

where V_x is the intercept voltage (or reference voltage). When v_{in} is at V_x, the output voltage V_o will be zero. V_y is the slope voltage representing volts per decade. We have designed the circuit such that V_y=1 V and for the Sine AM signal used in our system, V_x=20 mV. That is, similar to Eq. (2.1), the circuit implements a level representation by

$$v_o = 20 \log_{10} \frac{v_{in}}{0.02} \quad (dB) \tag{3.2}$$

To illustrate the envelope extraction and level representation, we show two measured traces from the circuit in Fig. 3.7. The input was a 2 ms 40 kHz Sine AM. When its amplitude was 63.2 mV, the logarithmic amplifier output was 0.5 V, which corresponds to 10 dB from Eq. (3.2). Similarly, an input of 200 mV generated an output of 1 V, which was 20 dB.

Fig. 3.8 is the measured transfer function of the logarithmic circuitry. We see that from 20 mV to 2 V (0–40 dB), the logarithmic transformation follows the prediction of the design equation very well. The logarithmic amplifier provides a dynamic range of 50 dB. For our application, where the power supply is +5 Volts, the maximum input range was limited to about 47 dB. When input signal is very small, the output will be saturated at about -250 mV. Similarly, when input signal is very large, the output will be saturated at about 2.2 V.

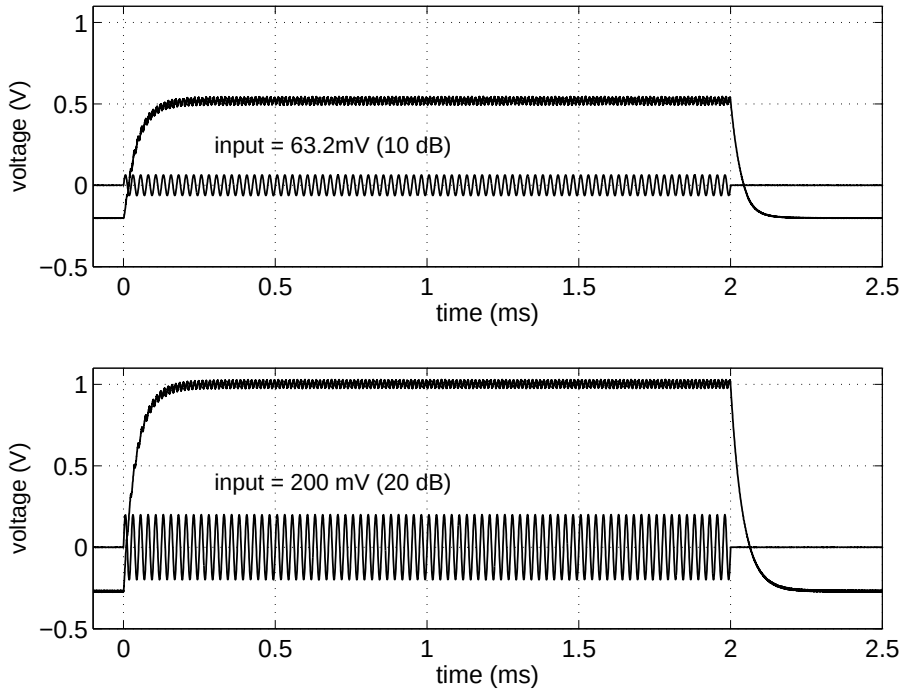


Figure 3.7: Sample logarithmic conversion for 2 ms 40 kHz AM burst. Top: Input is 63.2 mV, corresponding to 10 dB. Bottom: Input is 200 mV, corresponding to 20 dB.

Fig. 3.8 is the measured transfer function of the log circuitry. We see that it achieves about a 45 dB linear range.

3.2.3 AVCN Neuron

Given that echolocating bats use short pulse signals with only a few ms duration in a frequency band, what represents a biologically plausible spike train input for each LSO cell? In biology, a cochlear nucleus neuron would only fire 1-2 spikes and the information would be carried by a population of cells. We use a spike generator circuit that can fire at a very high rate to simulate the effect of converging inputs.

As shown in Fig. 3.9, the envelope voltage signal u(t) is converted by the cur-

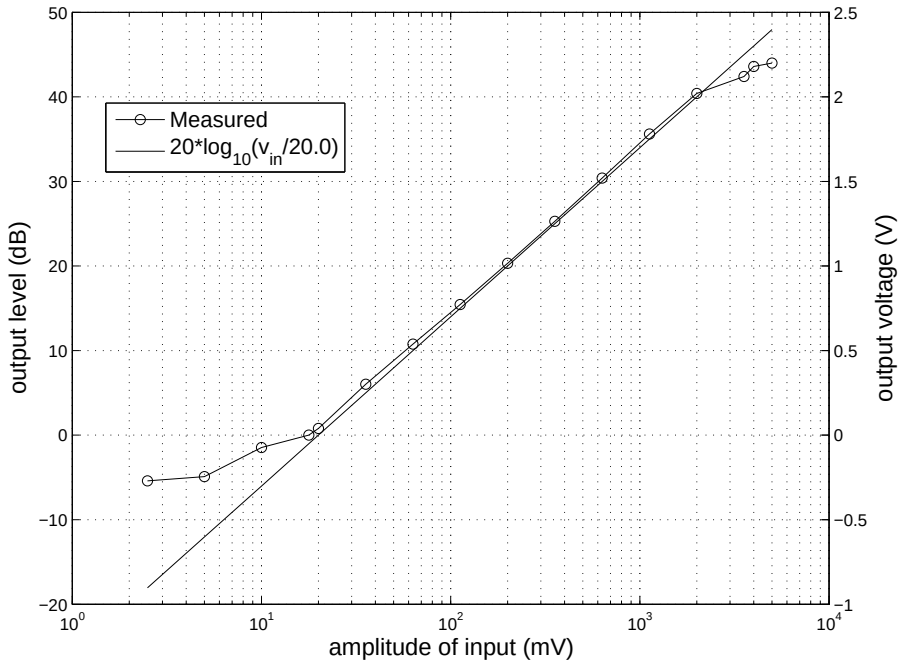


Figure 3.8: The measured transfer characteristic of the logarithmic-envelope circuit. The input signal is a 2 ms duration, 40 KHz sinewave pulse at varying amplitudes. The measured data (solid line with circles) is compared to the design equation (Eq. (3.2), solid line). Note the right Y-axis represents the output in voltage (V), the left Y-axis represents the output in level (dB)

rent controlled current source into a current equal to $A\frac{u(t)}{R}$, which is then integrated on capacitor C. We use a one-shot circuit to generate a voltage pulse of constant width . The one-shot circuit outputs this pulse when the capacitor voltage crosses the threshold voltage and the reset circuit quickly shunts the capacitor voltage to the resting voltage.

If the last spike occurs at time t_n and we neglect the propagation delay and resetting time, then the next spike will come after a time interval δ_n, which can be found as

$$\delta_n = \frac{RC\vartheta}{A\overline{u}(t_n, t_{n+1})} \tag{3.3}$$

where ϑ is the threshold voltage of the one-shot, and $\overline{u}(t_n, t_{n+1})$ is the mean

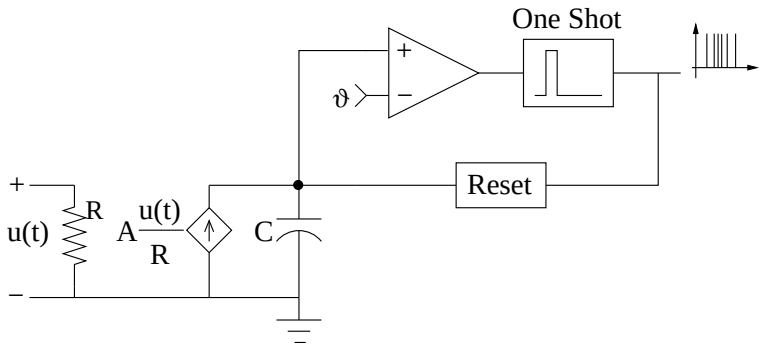


Figure 3.9: Simplified circuit model for the conversion of the envelope amplitude to the AVCN spike train.

value of u(t) in the time interval $[t_n, t_{n+1}]$.

In essence, we design a spike train with spike intervals inversely proportional to the instantaneous intensity of the echo envelope. In practice, we may tune the circuit parameters R, C, ϑ, and A to design the total spike numbers in time duration T by

$$N = \left\lfloor \frac{A \int_0^T u(t)dt}{RC\vartheta} \right\rfloor \tag{3.4}$$

For a tone burst of amplitude U_m with duration T, Eq. (3.4) becomes

$$N = \left\lfloor \frac{AU_mT}{RC\vartheta} \right\rfloor \tag{3.5}$$

Our design considerations about choosing the number N include both biological and circuit related issues. First, because this AVCN spike train represents the input to an LSO cell from a population of AVCN neurons, the number N represents the multiplication of the total number of synapses an LSO cell has and how many spikes it receives on each synapse. While exact information about excitatory and inhibitory convergence onto the bat LSO data is not available, experiments in the gerbil suggest that there are about ten excitatory and eight inhibitory synapses on a single LSO cell (Sanes, 1990).

For circuit considerations, as N increases, the accuracy of envelope information that the spike train represents improves. But there is one restriction from our synapse circuit and LSO model, which will be described in detail in the next chapter. In order for the synapse circuit to perform a linear summation of input spikes, the synapse must have enough time to reset.

Based on these two considerations, we have tuned the AVCN neuron circuit parameters such that a T ms tone burst of amplitude U_m (in dB ref. 20 mV) produces a spike count of:

$$N(t) = \left\lfloor U_m \frac{t}{T} \right\rfloor \tag{3.6}$$

Specifically, since we use a 2 ms tone burst in our test and because our log circuit has a 45 dB dynamic range, we find that this tuning allows the synapse circuit to perform a linear temporal summation. Fig. 3.10 shows the measured output of the AVCN neuron to a 2 ms 40 kHz sinewave AM pulse at various amplitudes.

3.2.4 Front-end Response to Target

We illustrate the response of the designed front-end to real target(s) in Fig. 3.11 and Fig. 3.12. We chose as our target(s) a vertical cylinder of 5 cm diameter. Fig. 3.11 shows a typical response of the front-end system to a single target located at 20° left of the center and 70 cm away from the speaker. The top two panels show the detected and amplified echoes (output from Block A as in Fig. 3.2), left and right side respectively. We show on the lower two panels the logarithmically-encoded envelopes.

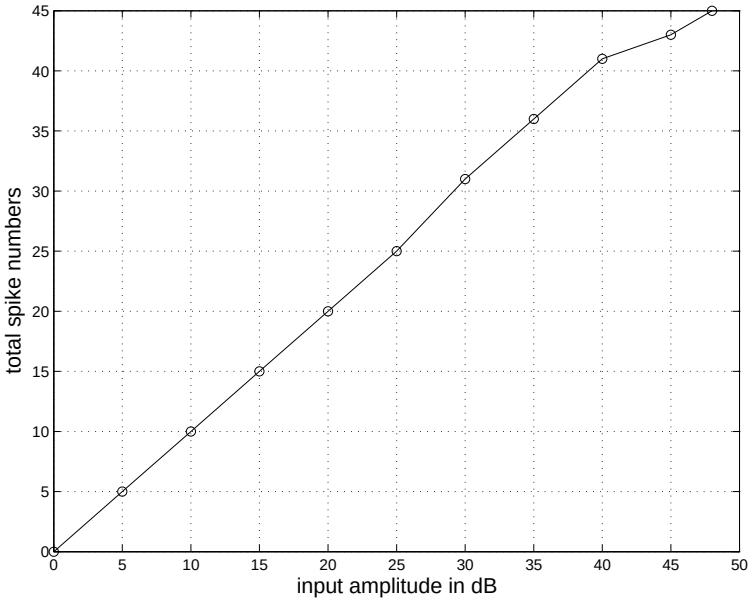


Figure 3.10: AVCN neuron circuit calibration. For the 2 ms, 40 KHz sinewave pulse, the AVCN neuron circuit is calibrated to generate a number of spikes equal to the input amplitude in dB. This demonstrates the logarithmic encoding of the input amplitude to the number of spikes transmitted by the AVCN neuron.

We then show how the front-end system responded after a second target was added at 25° right of the center and 150 cm away from the speaker. From the top two panels, we see that the first target (the closer one), has a larger envelope amplitude. This closer target also interferes with the reception of the second target, as we can observe from the bumps on the envelope waveform of the second target. The bottom two panels show the output from the AVCN neuron, from left to right respectively.

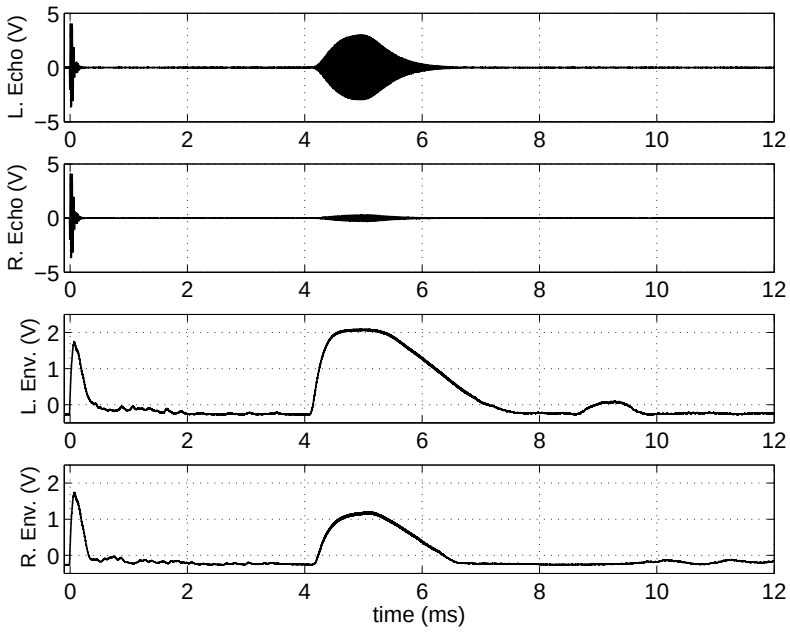


Figure 3.11: Sample traces of the front-end response to a single target. A vertical cylinder 5 cm in diameter is located 70 cm away and 20° left of center. The upper two panels show the amplified left and right microphone signals and the lower two panels show the left and right logarithmically-encoded envelope signals.

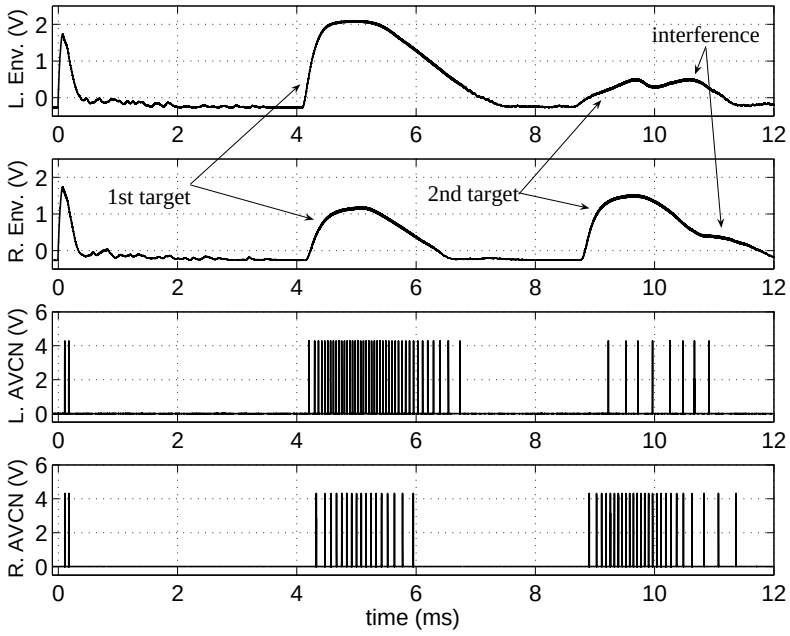


Figure 3.12: Sample traces of the front-end response to two targets. A second, identical cylinder (150 cm away and 25° right of center) is added to the target configuration of Fig. 3.11. The upper two panels show the left and right logarithmically-encoded envelope signals and the lower two panels show the corresponding left and right AVCN spike train outputs.

3.3 Multilayer Network Chip Design and Analysis

3.3.1 Spike Transmission and Communication

The address-event representation (AER) protocol overcomes the limited number of available pads in a chip package and allows modularization for multi-chip designs. We followed the AER protocol that was described in Boahen (2000).

The LSO and DNLL layer (the bottom box of Fig. 3.3) transmit spikes through a two-dimensional (2-D) AER transmitter. Fig. 3.13 shows the architecture of the 2-D transmitter. The 2-D transmitter consists of the X and Y address encoders, the X and Y handshaking circuits, and the X and Y arbiters. Neurons in a 2-D AER transmitter are selected by performing hierarchical row-first column-second arbitration, as shown in Fig. 3.13. First, we use a Y-Arbiter to choose one of Y rows, and then we use a X- Arbiter to choose one of X neurons assigned to that row. Hierarchical arbitration guarantees that only one row is active at any time. The X and Y arbiter is composed of a binary arbiter tree as described in Boahen (2000), and their function is to detect the earliest request among all the requests from the row or the column. The handshaking circuit holds the column or row requests to the arbiter until the acknowledgment signal (*Ack*) arrives. We must logically OR together all requests within each row to generate requests for the row-arbiter and all requests within each column to generate requests for the column-arbiter.

Each active neuron first sends a request to the row (Y) arbiter. When it is chosen, it then sends a request to the column (X) arbiter. Once it is chosen by both arbiters it then sends the request signal (Req) off the chip, and at the same time

generates its address in the encoder and drives onto the bus. Each neuron releases the row- and column-request lines once it has been serviced. A neuron is reset only when both its row and its column are selected.

Fig. 3.13 illustrates a 2-D matrix of transmitting neurons (square boxes), the neuron with address (x,y) that has earliest spike is selected by performing the hierarchical row-first column-second arbitration.

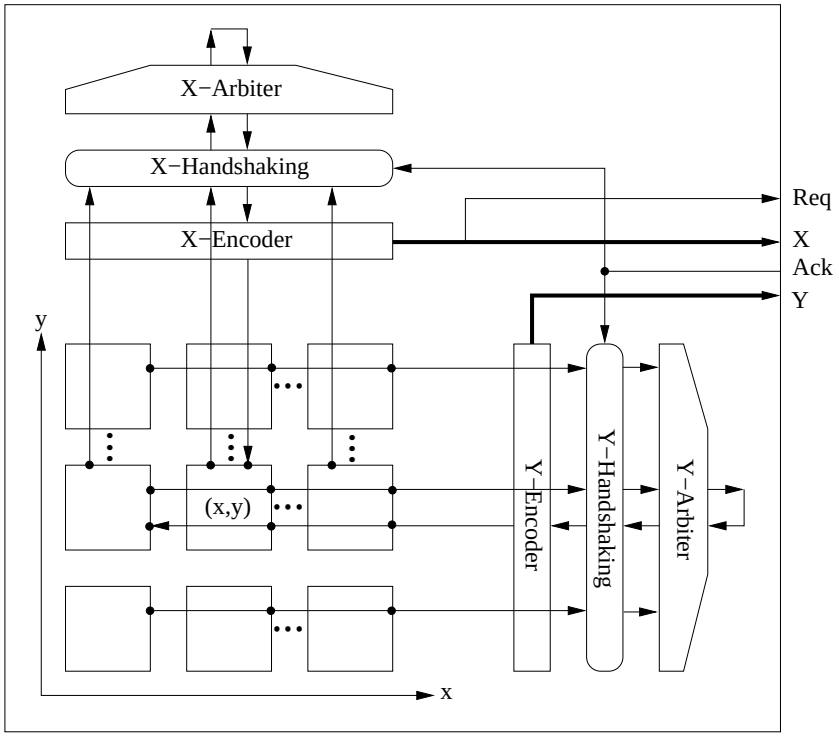


Figure 3.13: Architecture of AER transmitter. The transmitter consists of the X and Y address encoder, handshaking circuit, and arbiter tree. For a 2-D matrix of transmitting neurons (square boxes), the neuron with address (x,y) that has earliest spike is selected by performing the hierarchical row-first column-second arbitration.

Neurons in the IC layer (the upper box of Fig. 3.3) transmit spikes out of the chip by another 2-D transmitter. These IC neurons communicate with the LSO and DNLL neurons through a 2-D AER receiver. Fig. 3.14 shows the architecture of the 2-D receiver. The 2-D AER receiver's structure parallels that of the transmitter.

First, it uses a Y-Decoder to select one of the Y rows, and then it uses an X-Decoder to select one of the X output ports assigned to that row. This hierarchical row-first column-second decoding for 2-D receiver is illustrated in Fig. 3.14 by showing how the synapse with address (x,y) is selected. That is, a synapse is activated only after both its row and its column are selected. Once the synapse is selected, it sends back the acknowledge signal (*Ack*) off the chip.

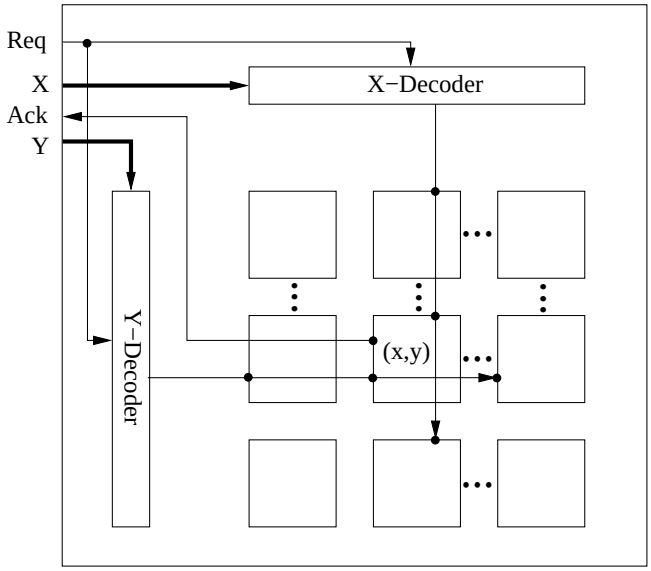


Figure 3.14: Architecture of AER Receiver. For a 2-D matrix of synapses (square boxes), the synapse with address (x,y) is selected by a hierarchical row-first column-second decoding scheme.

The AER circuits we use are similar to those described in Boahen (2000). We omit the details of the AER circuitry in this text.

3.3.2 Neuron Model, Circuit Implementation and Analysis

Among various neuron models, perhaps the integrate-and-fire model is the one that has been most widely used in modeling the dynamics of large-scale networks of spiking neurons. In such a model, the subthreshold process is modeled as a

linear RC circuit that integrates the input synaptic current (with a leakage current proportional to the depolarization). The spike generation is modeled as a threshold process such that when the depolarization crosses the threshold a spike is emitted.

In VLSI implementation, practical on-chip capacitances are on the order of pF due to limited silicon area. To model biological neurons with membrane time constants on the order of ms, hundreds of megohms of resistance would be needed had the RC circuit model been chosen. This large resistance is typically impractical due to size and mismatch considerations. Most VLSI design approaches encourage the use of transistors to implement an adjustable resistance. For these reasons, the integrate-and-fire neuron model in VLSI (referred to as the VLSI integrate-and-fire model in the following text) utilizes a constant current leakage. a theoretical study on the collective behavior of networks with VLSI integrate-and-fire neurons showed that the spike statistics of such neurons appear to be qualitatively similar to conventional RC integrate-and-fire neurons (Fusi and Mattia, 1999). In the following, we first formalize the VLSI integrate-and-fire model and then describe our circuit implementation and an analysis of neuron parameter control.

Fig. 3.15 illustrates the VLSI integrate-and-fire model. The model consists of three components. The first component is for the subthreshold integration of input current on a membrane capacitance $\mathrm{C_m}$ with a constant leakage current I_{lk}. For an input synaptic current $i_s(t)$, the dynamics of membrane voltage $v_m(t)$ is governed by

$$C_m \frac{dv_m(t)}{dt} + I_{lk} = i_s(t) \tag{3.7}$$

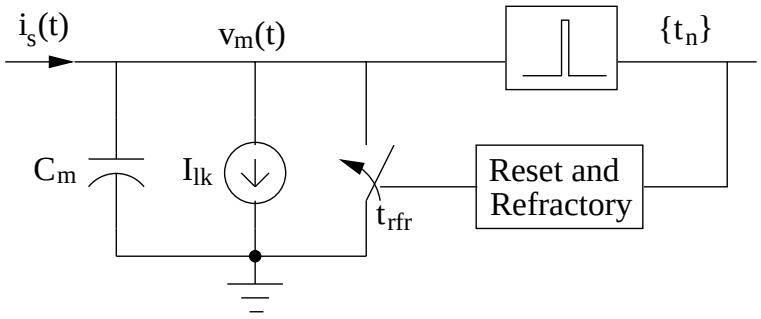


Figure 3.15: The VLSI integrate-and-fire model. Under subthreshold, the neuron integrates the input synaptic current $i_s(t)$ through its membrane capacitance $\mathrm{C_m}$ and a constant leakage current. When the membrane voltage $v_m(t)$ crosses the threshold from below, a narrow pulse is generated and the circuit is short-circuited. Following each spike generation, any input $i_s(t)$ is shunted to ground for a period of time t_{rfr} corresponding to the absolute refractory period of the neuron.

The second component is a threshold process for generating a voltage spike. When the potential $v_m(t)$ reaches the neuron threshold, denoted by V_θ, a narrow pulse is generated. The set of all firing times of the neuron can be described by

$$\{t_n; 1 \leq n \leq N\} = \{t | v_m(t) = V_\theta \;\; and \;\; \frac{dv_m(t)}{dt}\Big| t = t_n > 0\} \tag{3.8}$$

By including the derivative of $v_m(t)$ at t_n being larger than zero, Eq. (3.8) states explicitly that the firing condition is to reach the threshold V_θ from below.

The third component is for neuron reset. Immediately after t_n, the membrane potential is reset to a value corresponding to the rest potential, usually the 0 V (i.e. ground). The reset process can be described by

$$\lim_{\delta \to 0} v(t_n + \delta) = 0 \tag{3.9}$$

The circuit is short-circuited for a period of time corresponding to the absolute refractory period, denoted by t_{rfr}

$$v_m(t) = 0 \quad for \; t_n^+ \leq t \leq t_n^+ + t_{rfr} \tag{3.10}$$

The circuit shown in Fig. 3.16 implements the above VLSI integrate-and-fire neuron model with constant leakage and a controllable refractory period. Transistor sizes for this circuit are listed in Table 3.1. This neuron circuit can be divided into four functional parts. The first part consists of the membrane capacitance C_1 and a constant current leak by transistor M_1. The leakage current is determined by

$$I_{lk} = S_{10} I_{0n} e^{\frac{\kappa_n V_{lk}}{V_T}} \tag{3.11}$$

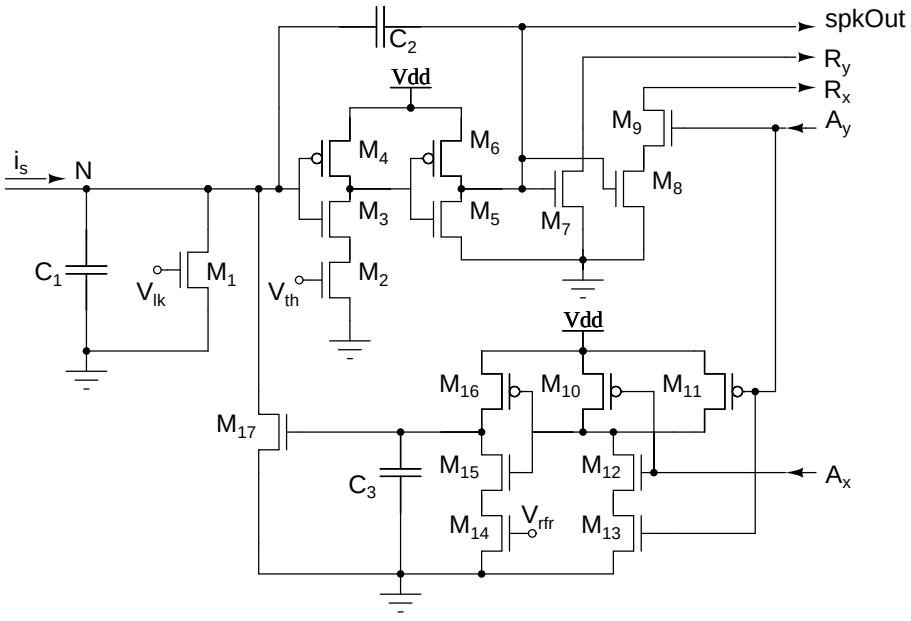


Figure 3.16: The neuron circuit used for neurons in layers 1, 2, and 3. The neuron integrates synaptic current on the membrane capacitance C_1, generates output spikes with the high-gain amplifier ($M_2 - M_6$) and capacitor C_2. To transmit spikes, the neuron generates AER X and Y active-low request signals Rx and Ry with $M_7 - M_9$. The neuron's refractory period is set by $M_{10} - M_{17}$ with capacitor C_3. V_{th} sets the neuron's spiking threshold, V_{lk} sets the membrane leakage, and V_{rfr} sets the refractory period. Transistor sizes are listed in Table 3.1

where $V_T = kT/q$ is the thermal voltage, I_{0n} is a positive constant current when $V_{gs} = V_{bs} = 0$, and S_i is the aspect ratio of the transistor M_i (W_i/L_i). $0 < \kappa_n < 1$ is a parameter specific to the technology.

Table 3.1: Transistor sizes of the neuron circuit

transistor	M_1	M_2	M_3	M_4	M_5	M_6	M_7	M_8	M_9
width (μm)	4.0	4.0	4.0	9.6	4.0	9.6	4.0	4.0	4.0
length (μm)	4.0	4.0	4.0	4.0	1.6	1.6	4.0	4.0	4.0
transistor	M_{10}	M_{11}	M_{12}	M_{13}	M_{14}	M_{15}	M_{16}	M_{17}	
width (μm)	9.6	9.6	4.0	4.0	4.0	4.0	9.6	8.0	
length (μm)	1.6	1.6	1.6	1.6	4.0	4.0	4.0	2.4	

The second part, including transistors $M_2 - M_6$ and capacitor C_2, is the spike generator. *spkOut* is the spike output. V_{th} limits the current of the inverter (M_3 and M_4 and set the threshold of the neuron by

$$V_\theta = Vdd - |V_{tp}| - \frac{V_{th} - V_{tn}}{r} \tag{3.12}$$

where V_{tp} and V_{tn} are the threshold voltage of the PMOS transistor and NMOS transistor, respectively, and

$$r = \sqrt{\frac{\mu_p S_p}{\mu_n S_n}} \tag{3.13}$$

Here, μ_p and μ_n are the mobility of the holes and electrons, respectively. S_p is the aspect ratio of transistor M_4, S_n the aspect ratio of transistor M_2.

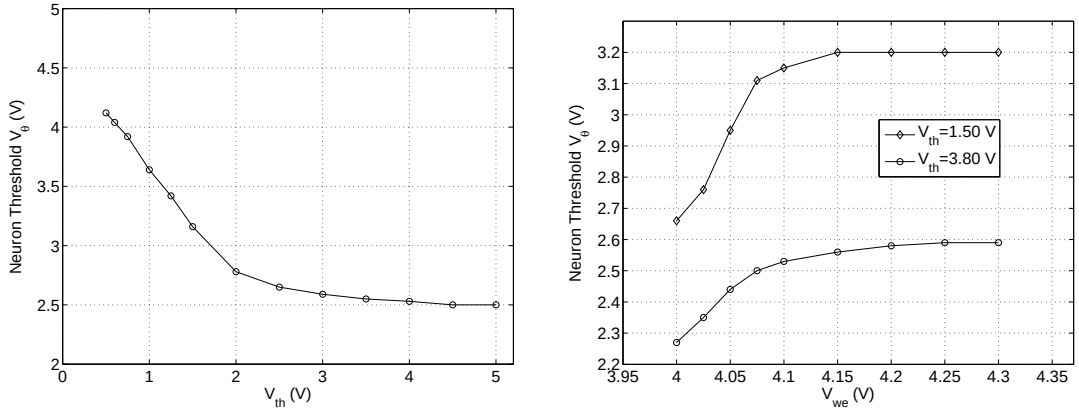
When V_{th} is close to Vdd, transistor M_2 no longer limits the current of the inverter, and the inverter returns to the conventional inverter with the neuron threshold determined by

$$V_\theta = \frac{r(Vdd - |V_{tp}|) + V_{tn}}{1 + r} \tag{3.14}$$

Note r in Eq. (3.14), S_n is the aspect ratio of transistor M_3.

Fig. 3.17 shows the measured neuron threshold data from an example neuron. In Fig. 3.17(a), the V_{th} was varied from 0.5 V to 5.0 V. If V_{th} was well below 0.5 V, M_{11} operates in the deep subthreshold region so that the neuron circuit could not

respond quickly. When V_{th} was below 2 Volts, the neuron's threshold V_θ linearly decreased as V_{th} increased as predicted by Eq. (3.12). When V_{th} was above 2 Volts, V_θ approached the threshold of the conventional inverter as determined by Eq. (3.14).



(a) (b)

Figure 3.17: V_{th} controls the threshold of the neuron. An example neuron received a constant excitatory current from its excitatory synapse. (a) The input current is held constant (V_{we}=4.10 V) but V_{th} was varied from 0.50 V to 5.0 V. (b) V_{th} was held constant at 1.50 V (top trace) and at 3.80 V (bottom trace), but V_{we} was varied from 4 V to 4.3 V. For both (a) and (b), V_{lk}=220 mV, V_{rfr}=350 mV.

We examined the effect of the input current level on the neuron's threshold voltage in Fig. 3.17(b). We observe that synaptic current input level did affect the V_θ. The effect was most apparent when the synaptic weight was in a range from 4.00 to 4.10 V, a range where the transistor was not working in deep subthreshold mode. We point out that this effect of input current level is probably partially due to the fact that the voltage follower and the output pad of the chip has limited response speed. Considering that the synaptic weight for DNLL and IC layer will be kept constant values above 4.15 Volts among the EI cells in those two layers, variation in V_θ due to V_{we} will be negligible. For the LSO layer, the maximum variation in V_{we}

will be within 50 mV so we will ignore the small variation of V_θ among the LSO EI cells in our analysis.

The third part, including $M_{10} - M_{17}$ with capacitor C_3 sets the neuron's refractory period.

$$t_{rfr} = \frac{Vdd}{S_{14} I_{0n}} e^{\frac{-\kappa_n V_{rfr}}{V_T}} \tag{3.15}$$

Fig. 3.18 illustrates how the refractory period is defined and measured in this study. The neuron under test was given a constant excitatory current input from its excitatory synapse. The neurons emitted a spike train with a constant spike interval due to the refractory period. The refractory period t_{rfr} is defined by the time interval beginning from the last spiking time (0) to the time the membrane voltage begins to rise. t_{rfr} was measured as 1 ms in this example.

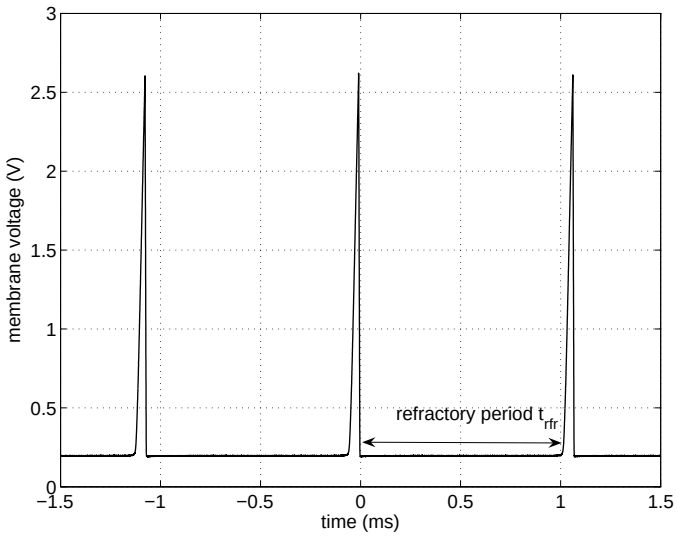
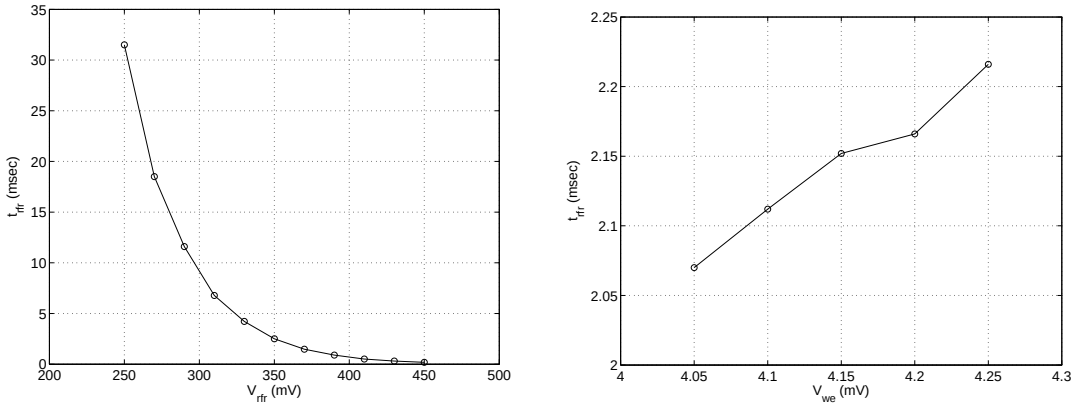


Figure 3.18: Definition and measurement of the refractory period. An example neuron received a constant current from the excitatory synapse. The refractory period t_{rfr} is defined by the time interval beginning from the last spiking time (0) to the time the membrane voltage begins to rise. t_{rfr} was measured as 1 ms in this example.

Fig. 3.19 shows how V_{rfr} controls the refractory period of the neuron. From



(a) (b)

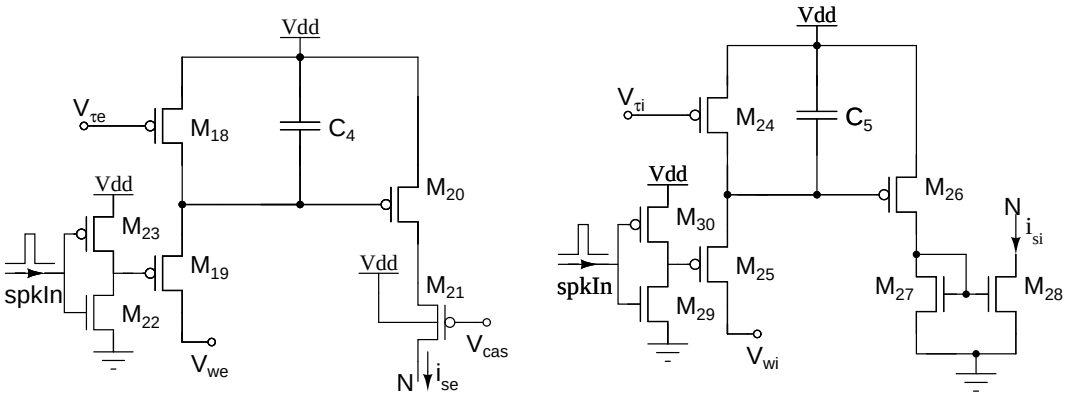
Figure 3.19: V_{rfr} controls refractory period of the neuron. Refractory period was measured from an example neuron receiving a constant excitatory current from its excitatory synapse. (a) V_{rfr} varied from 250 mV to 450 mV. V_{we}=4.10 V, V_{lk}=220 mV. (b) V_{rfr} was held at constant of 355 mV, but V_{we} was varied from 4.05 to 4.25 V.

Fig. 3.19(a), we see that the refractory period t_{rfr} decreases exponentially with V_{rfr}, as predicted by Eq. (3.15). To see to what extent the refractory period is affected by the input current level, we held V_{rfr} constant at 355 mV but varied V_{we} from 4.05 V to 4.25 V. As shown in Fig. 3.19(b), the refractory period changed about 0.15 ms. We point out that the measurement of the refractory period will not be very accurate because the time at which the membrane voltage begins to rise is difficult to define accurately. Considering that the V_{we} among synapses are usually within 50 mV, such a variation with input current level is negligible.

The fourth part, $M_7 - M_9$ generates the X and Y request signals for the 2-D AER system.

3.3.3 Synapse Circuit

We chose a compact and easily controllable synapse circuit that was first introduced by Lazzaro and Wawrzynek (1994). The synapse circuits are shown in Fig. 3.20. When V_w is set below the transistor threshold voltage, this synapse produces a clean exponential decay of the synaptic current, which is an important feature of the biological counterpart and allows current to flow for a short time after the input spike.



(a) excitatory synapse circuit (b) inhibitory synapse circuit

Figure 3.20: Excitatory and inhibitory synapse circuits. Each synaptic circuit is triggered by a spike signal, producing an exponentially-decaying synaptic current. $V_{\tau e}$ and $V_{\tau i}$ set the excitatory and inhibitory synaptic time constants, respectively. V_{we} and V_{wi} set the excitatory and inhibitory synaptic strengths, respectively. The synapse circuit is shielded from the postsynaptic membrane potential by the cascode transistor M_4 (biased by V_{cas}).

$V_{\tau e}$ and $V_{\tau i}$ set the excitatory and inhibitory synaptic time constants, respectively. V_{we} and V_{wi} set the excitatory and inhibitory synaptic strengths, respectively. The synapse circuit is shielded from the postsynaptic membrane potential by the cascode transistor M_4 (biased by V_{cas}).

The LSO and DNLL EI cell will use the synaptic circuits shown in Fig. 3.20

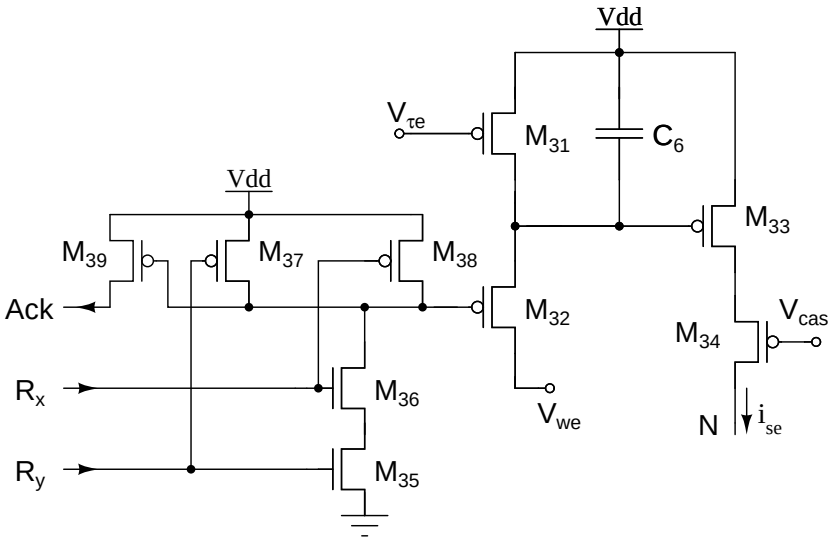
with slight modifications. In the IC layer, an EI cell communicates with LSO layer and DNLL layer through AER interface. The synapses in the IC layer that receive input through AER receiver are called "receiver synapse. Fig. 3.21 is the circuit schematic for the excitatory (a) and inhibitory (b) synapse circuit. The NAND gate formed by transistors M_{35}–M_{38} in (a), or M_{45}–M_{48} in (b) allows a synapse in the IC layer to be activated only when both the row (R_y is high) and the column (R_x is high) are selected. The NAND gate also pulls up the acknowledge signal (Ack) via transistor M_{39} in (a), or M_{40} in (b) right after the synapse is selected.

The synapse circuit for LSO will be used in a different mode from those for DNLL and IC. We leave the circuit analysis to later chapters. Chapter 7 is dedicated to a new synapse model and circuit design.

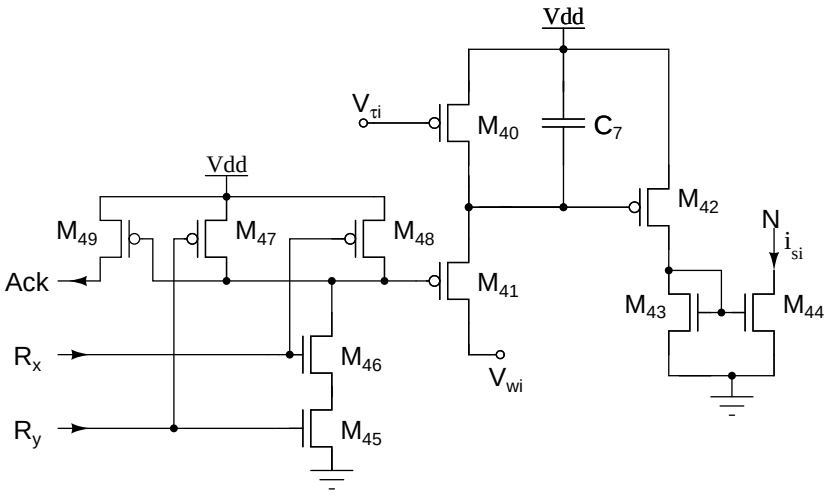
3.3.4 EI Cell Circuits for LSO, DNLL and IC

As described in Fig. 3.1, EI cells interact with each other in the three layer network through different synaptic connections. The same spiking neuron circuit as shown in Fig. 3.16 was used for all the three layers. Depending on the layer it is in, a neuron receives inputs from different synapse circuits to compose an EI cell. Below we give specific circuit connection and synapse circuit parameters for EI cells in LSO, DNLL, and IC.

An LSO EI cell circuit is composed of a neuron circuit, an excitatory synapse circuit ($ESyn_1^1$) and an inhibitory synapse circuit ($ISyn_1^1$), as shown in Fig. 3.22. Here, the upper index denotes the layer, and the lower index denotes the synapse



(a) excitatory synapse circuit



(b) inhibitory synapse circuit

Figure 3.21: Receiver synapse circuit for EI cell in IC layer. (a) Excitatory receiver synapse circuit. (b) Inhibitory receiver synapse. Only when both the row and column are selected (R_y and R_x both high), the synapse is activated through the NAND gate (M_{35}–M_{38} in (a), M_{45}–M_{48} in (b)), and an acknowledgment signal *Ack* is send off chip via the pull-up transistor M_{39} in (a), M_{40} in (b).

number. $ESyn_1^1$ and $ISyn_1^1$ receives the input from ipsilateral AVCN and contralateral AVCN, respectively. Table 3.2 and Table 3.3 list the transistor sizes for $ESyn_1^1$ and $ISyn_1^1$, respectively.

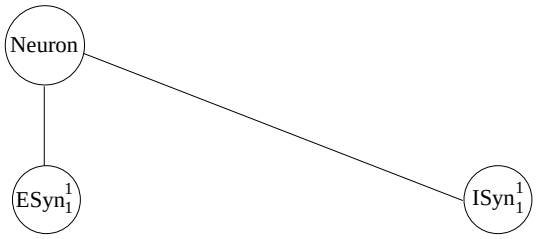


Figure 3.22: LSO EI cell circuit connection. In an LSO EI cell, the neuron circuit is connected to an excitatory synapse $ESyn_1^1$ (circuit shown in Fig. 3.20(a)) and an inhibitory synapse $ISyn_1^1$ (circuit shown in Fig. 3.20(b)).

Table 3.2: Transistor sizes of the LSO excitatory synapse

transistor	M_{18}	M_{19}	M_{20}	M_{21}	M_{22}	M_{23}
width (μm)	24.0	8.0	12.0	4.0	4.0	9.6
length (μm)	2.4	1.6	4.0	4.0	1.6	1.6

Table 3.3: Transistor sizes of the LSO inhibitory synapse

transistor	M_{24}	M_{25}	M_{26}	M_{27}	M_{28}	M_{29}	M_{30}
width (μm)	24.0	8.0	12.0	4.0	4.0	4.0	9.6
length (μm)	2.4	1.6	4.0	4.0	4.0	1.6	1.6

In a DNLL EI cell, the neuron circuit is connected with one excitatory synapse circuit ($ESyn_1^2$) and two inhibitory synapse circuits ($ISyn_1^2$ and $ISyn_2^2$), as shown in Fig. 3.23. $ESyn_1^2$ and $ISyn_1^2$ receives spiking inputs from the contralateral LSO cell and ipsilateral LSO cell, respectively. $ISyn_2^2$ receives spiking inputs from the opposite DNLL cell. Synapse circuits in DNLL are the same as those in the LSO layer, but some difference in transistor sizes. Table 3.4 and Table 3.5 list the transistor sizes for $ESyn_1^2$ and $ISyn_1^2$, respectively.

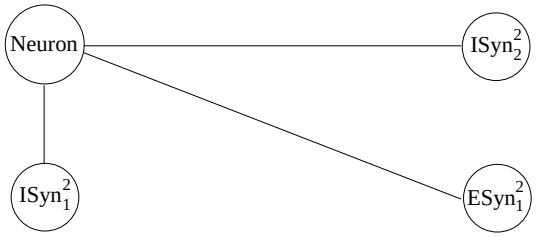


Figure 3.23: DNLL EI cell circuit connection. In a DNLL EI cell, the neuron circuit is connected to one excitatory synapse $ESyn_1^2$ (Fig. 3.20(a) and Table 3.4) and two inhibitory synapse: $ISyn_1^2$ and $ISyn_2^2$ (Fig. 3.20(b) and Table 3.5)

Table 3.4: Transistor sizes of the DNLL excitatory synapse

transistor	M_{18}	M_{19}	M_{20}	M_{21}	M_{22}	M_{23}
width (μm)	8.0	9.6	12.0	4.0	4.0	9.6
length (μm)	4.0	1.6	4.0	4.0	1.6	1.6

An IC EI cell circuit is composed of a neuron circuit, two excitatory synapse circuits ($ESyn_1^3$ and $ESyn_2^3$) and five inhibitory synapse circuits ($ISyn_1^3$ – $ISyn_5^3$), as shown in Fig. 3.24.

Synapses $ESyn_1^3$ and $ISyn_1^3$ receives spike input from contralateral LSO and ipsilateral LSO, respectively. Synapses $ISyn_2^3$ and $ISyn_3^3$ receives spike input from ipsilateral DNLL and contralateral DNLL, respectively. Because the IC layer communicates with LSO layer and DNLL layer through AER interface, these four synapse circuits are different from those in LSO and DNLL layers. The circuit schematic for $ESyn_1^3$ is in Fig. 3.21(a), and the transistor sizes are listed in Table 3.6. The circuit for $ISyn_1^3$ - $ISyn_3^3$ is in Fig. 3.21(b), and transistor sizes are

Table 3.5: Transistor sizes of the DNLL inhibitory synapse

transistor	M_{24}	M_{25}	M_{26}	M_{27}	M_{28}	M_{29}	M_{30}
width (μm)	8.0	9.6	12.0	4.0	4.0	4.0	9.6
length (μm)	4.0	1.6	4.0	4.0	4.0	1.6	1.6

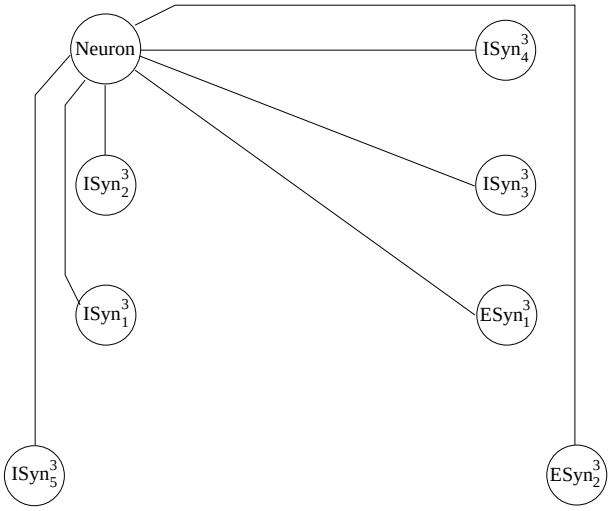


Figure 3.24: IC EI cell circuit connection. In an IC EI cell, the neuron is connected with two excitatory synapse circuits ($ESyn_1^3$ and $ESyn_2^3$) and five inhibitory synapse circuits ($ISyn_1^3$ – $ISyn_5^3$). Synapses $ESyn_1^3$ and $ISyn_1^3$ – $ISyn_3^3$ are receiver synapses with circuit shown in Fig. 3.21. $ISyn_4^3$ is the same as $ISyn_2^2$ in the DNLL layer, $ESyn_2^3$ and $ISyn_5^3$ are the same as those in the LSO layer.

listed in Table 3.7.

Table 3.6: Transistor sizes of the receiver excitatory synapse in the IC layer

transistor	M_{31}	M_{32}	M_{33}	M_{34}	M_{35}	M_{36}	M_{37}	M_{38}	M_{39}
width (μm)	8.0	9.6	12.0	4.0	4.0	4.0	9.6	9.6	9.6
length (μm)	4.0	1.6	4.0	4.0	1.6	1.6	1.6	1.6	1.6

Table 3.7: Transistor sizes of the receiver inhibitory synapse in the IC layer

transistor	M_{40}	M_{41}	M_{42}	M_{43}	M_{44}	M_{45}	M_{46}	M_{47}	M_{48}	M_{49}
width (μm)	8.0	9.6	12.0	4.0	4.0	4.0	4.0	9.6	9.6	9.6
length (μm)	4.0	1.6	4.0	4.0	4.0	1.6	1.6	1.6	1.6	1.6

Synapse $ISyn_4^3$ receives spiking inputs from the opposite IC, the circuit is the same as the one in the DNLL ($ISyn_2^2$). Synapses $ESyn_2^3$ and $ISyn_5^3$ were designed for receiving contralateral AVCN and ipsilateral AVCN input, respectively. The circuits and parameters are the same as those in the LSO layer ($ESyn_1^1$ and $ISyn_1^1$).

3.4 Discussion

We have presented a VLSI-based neuromorphic system that emulates the bat ILD processing system for azimuthal echolocation. Our hardware system contains an op-amp-based front-end and a custom CMOS VLSI chip. The sonar head design achieves a dynamic range of $\pm 45^{\circ}$ azimuth with ± 30 dB peak ILD values. The front-end circuit, by using a fast and accurate logarithmic envelope detector, has achieved envelope extraction and logarithmic transformation for a 45 dB dynamic range. Such a front-end system, due to its success in generating similar ILD behavior as bats (e.g., monotonic ILD function of azimuth, similar range of ILD value, and sound pressure level encoding by spike train), enables us to test the neuromorphic system's performance on various real world signal tests.

We have designed a CMOS VLSI chip that implements a three-layer spiking neural network model of bat ILD processing in the LSO, DNLL, and IC. With 32 neurons for each layer and 96 neurons in total, the chip is able to create the population response of EI cells in three ILD processing centers, and from both sides of the brain. By constructing EI cells with many of the known synaptic connection among different layers, the chip is able to produce different neuron response types described in the literature and test our neural computational algorithm with great flexibility. The chip was fabricated in a commercially-available 1.5 μm technology. All synapses and neurons were designed in the transistor's subthreshold region of operation to lower power consumption.

While AER has conventionally been used for multi-chip communication to

overcome the limited number of I/O pads, we have also used it for both intra-chip and inter-chip communication. Dividing the three layer network into two parts and connecting the two parts through AER interface has several advantages. For example, this allows us to operate layer 1 and layer 2 on one chip, but layer 3 on a second chip. Having two chips running together means more available pads for potentiometers that are necessary to tune various EI cell property and different connections. Also, the AER communication between two parts allows us to test more possible connections among three layers. This is possible because the AER interface is flexibly reconfigurable. With some simple external digital circuitry, spiking neuron re-mapping among three layers can be achieved.

As this study is focused on the ILD processing in the LSO, DNLL and IC, the input to the three layer network has been simplified as two representative AVCN neurons. We used a spike generator circuit that can fire at a very high rate to simulate the converging inputs to the LSO from a population of AVCN cells. As we will see in later chapters, this simplification allows us to analyze the complex ILD computation by some mathematically tractable models.

Although the multilayer chip was designed to include as many connection schemes as possible, only one synapse was used to represent any specific interaction or connection between two neurons. This limitation can be partially reconciled by using the merge PIC for reconfiguration. For example, an IC cell receives excitatory input from the contralateral LSO spiking output via a single excitatory synapse. With the merge PIC, it is easy to re-map the LSO spiking outputs from two chips onto the same target IC cell. With this re-mapping through the AER interface, each

IC cell in layer 3 will equivalently have two synapses receiving excitatory input from the contralateral LSO in layer 1.

Chapter 4

Lateral Superior Olive

The Lateral Superior Olive (LSO) is dominated by EI cells and is the first stage at which ILDs are processed and encoded. ILD computation at the LSO is primarily a subtractive process involving excitation from the ipsilateral ear and inhibition from the contralateral ear. In this chapter we propose an LSO circuit model that employs first spike latency to encode ILD information. Our circuit model is suited for VLSI implementation and aims at generating a diverse population of LSO EI cells.

4.1 Model Considerations

4.1.1 Mechanisms of LSO ILD Sensitivity

Although numerous studies have shown that the initial processing of ILDs in mammals is carried out in the LSO (e.g. Boudreau and Tsuchitani, 1968; Covey et al., 1991), it was only recently that the detailed mechanism that underlies the LSO neuron's sensitivity to ILDs was established. The central question is the role of the neural latency-intensity relationship. In general, the neural response latency decreases with increasing stimulus intensity. This time-intensity trading has been found to play a critical role in ILD processing by EI cells in the superior colliculus

(SC) of cats (Yin et al., 1985) and in the inferior colliculus (IC) of bats (Pollak, 1988). This time-intensity trading in ILD processing leads to the commonly known "latency hypothesis". The formulation of this hypothesis varies, but its central idea can be expressed in this statement: ILDs are converted into neural time differences, and the differences in the timing of inputs at an EI cell affects its sensitivity to ILDs.

In the mustache-bat as well as in the Mexican free-tailed bat, the time-difference between excitation and inhibition to an LSO EI cell has been shown to shape ILD sensitivity (Park et al., 1996; Park et al., 1997). Their data provided evidence that ILDs produce changes in both the timing and the amplitude of synaptic inputs to the LSO EI cell, and that the timing changes help to shape ILD sensitivity functions. In a more recent study of rat LSO EI cell's sensitivity to ILD, Irvine et al. investigated contributions of changes in amplitude and timing of inputs. They concluded that for both click and tone-burst stimuli, the time-intensity trading contributes to the ILD sensitivity but the "strong form" of the latency hypothesis, which asserts that this factor alone accounts for the ILD sensitivity must be rejected (Irvine et al., 2001).

4.1.2 Overview of Some Existent LSO Models

There are only a few ILD models that consider detailed biological structures. Zacksenhouse et al. proposed a computational model of single LSO units that applies point process theory for modeling responses in the LSO of cats to transient and sustained input (Zacksenhouse et al., 1998). The compartmental model is however

not that easy to be extended to multi-layer networks.

Reed and Blum proposed a specific neural network model for the computation and encoding of the azimuthal information by the LSO (Reed and Blum, 1990; Blum and Reed, 1991). Their model used steady state firing rate. As pointed out by Park et al. (1997), Reed and Blum's model implicitly assumes that at the ILD of complete inhibition, latencies of excitation and inhibition are coincident. In other words, they did not consider the timing issue. Based on their experimental data, Park et al. concluded that intensity disparities create differences in response magnitude, latency, and the recruitment of different numbers of cochlear nucleus neurons from the two sides. It is the difference in latencies, the synaptic efficacies, and the threshold of the neuron that determine the ILD of complete inhibition.

4.1.3 Computing with the First Spike Latency

Studies on spike timing as a potential code of sensory stimuli have shown that the timing of individual spikes can carry far more information than the average firing rate alone (Rieke et al., 1997; Heil, 2004). Computing with spike timing rather than the firing rate becomes more necessary when a neural system must respond quickly to a transient stimulus, especially if the neurons involved respond with no more than one spike. Moreover, a recent study on the representation of multiple simultaneous sound-localization cues in the cat inferior colliculus have shown that spike-timing codes enhance the representation of ILD cues to some degree and that temporal coding allows multiple stimulus features to be independently represented

which would not be possible with only a rate code (Chase and Young, 2006).

First spike latency (FSL), the time from the onset of a stimulus to the firing time of the first action potential, has been found to be a fast and reliable encoding of stimuli. For example, using recordings from peripheral human somatosensory nerve fibers, Johansson and Birznieks (2004) demonstrated that the recruitment order of neurons provides a quick, reliable and sufficient ensemble code for discriminating four directions of fingertip force and three different shapes of the surfaces contacting the tip. The sequence of the first spikes in response to mechanical fingertip events provides information about these events faster than the fastest possible rate code and fast enough to account for the speed observed in natural object manipulations.

More relevantly, several recent studies have suggested that the FSL plays a dominant role in modulating sound source location including azimuth (Brugge et al., 1996; Eggermont, 1998). In a study to examine specific features of spike patterns that might transmit information related to sound-source azimuthal location, Furukawa and Middlebrooks (2002) recorded spike trains from neurons in the secondary auditory cortical field of chloralose-anesthetized cats to noise bursts presented from different azimuthal locations, and trained an artificial neural network to identify sound-source location by recognizing the spike patterns. In that study, first-spike latencies appeared to transmit more stimulus-related information than did any other feature of spike patterns. In a condition in which all but the first spike in each pattern were eliminated, transmitted information decreased by an average of only about 11%. In many cases, that condition showed essentially no loss of transmitted information.

Below, we present an LSO circuit model that employs the first spike latency to encode ILD. Our model is based on the latency hypothesis discussed above and the fact that bats respond to short echoes by no more than one spike.

4.2 LSO Circuit Model

4.2.1 Basic Model

As shown in Fig. 3.1, we model an LSO EI cell as a neuron receiving one excitatory spike train and one inhibitory spike train input. We consider inputs to the two ears to be tone bursts of duration T. The excitatory input level is E dB, and the inhibition level I dB. $N_E(t)$ denotes the number of excitatory spikes in [0,t], and $N_I(t)$ the number of inhibitory spikes in [0,t]. From Eq. (3.6),

$$N_E(t) = \left\lfloor \frac{E}{T} t \right\rfloor \tag{4.1}$$

and

$$N_I(t) = \left\lfloor \frac{I}{T} t \right\rfloor \tag{4.2}$$

where the symbol "$\lfloor\rfloor$" represents floor function.

Our LSO EI cell circuit has been designed in such a way that the membrane voltage $v_m(t)$ of the LSO neuron increases by α volts for each excitatory spike, and decreases by β volts for each inhibitory spike. The membrane voltage at time t is thus given by

$$v_m(t) = \alpha \left\lfloor \frac{E}{T} t \right\rfloor - \beta \left\lfloor \frac{I}{T} t \right\rfloor \tag{4.3}$$

Here, we have assumed the leakage current to be very small and can be neglected.

In the following we assume that E and I are relatively large so that the "staircase" function described by Eq. (4.3) can be approximated by

$$v_m(t) = \frac{(\alpha E - \beta I)t}{T} \tag{4.4}$$

We denote V_θ the voltage threshold of the LSO neuron circuit. The time to the first spike can be calculated by

$$t_{spk} = \frac{V_\theta T}{\alpha E - \beta I} \tag{4.5}$$

Although Eq. (4.5) is simple, it provides many insights to the LSO EI cell behavior. Eq. (4.5) can be rewritten in terms of the ILD and the average binaural level (ABL) as

$$t_{spk} = \frac{V_\theta T}{\frac{\alpha+\beta}{2} ILD + (\alpha - \beta) ABL} \tag{4.6}$$

where

$$ILD = E - I \tag{4.7}$$

and

$$ABL = \frac{E + I}{2} \tag{4.8}$$

We see from Eq. (4.6) that the time to the first spike of an LSO cell is related to both ILD and ABL. As the ILD increases, the time to first spike is shorter. Also as the total level between two ears increases, the time to the first spike is shorter. The effect of ABL is weighted by the difference between excitation strength α and inhibition strength β.

In biological ILD experiments as well as in this study, the excitation is kept at a constant value, but the inhibition is changed systematically to produce a range of ILD values. We can now change the format of Eq. (4.5) into

$$t_{spk} = \frac{V_\theta T}{\beta ILD + (\alpha - \beta)E} \tag{4.9}$$

The ILD of complete inhibition can be approximated by having $t_{spk} = T$ which gives

$$ILD_{ci} = \frac{V_\theta - (\alpha - \beta)E}{\beta} \tag{4.10}$$

Eq. (4.10) indicates that ILD_{ci} is dependent on E, the constant excitation level used in the experiment. Only when an LSO EI cell has equal excitation and inhibition strength, i.e., $\alpha = \beta$, is the ILD_{ci} purely determined by its own parameters: the synaptic strength or the neuron threshold.

The ILD of complete inhibition defines the minimum ILD that can inhibit the EI cell. For ILD greater than the ILD_{ci}, an EI cell fires with first spike latency defined by Eq. (4.9). To examine the relationship between t_{spk} and the ILD_{ci}, we can express t_{spk} as a function of the ILD_{ci} by

$$t_{spk} = \frac{T}{1 + \frac{\beta}{V_\theta}(ILD - ILD_{ci})} \tag{4.11}$$

Eq. (4.11) states that t_{spk} is inversely proportional to the difference between the input ILD and an EI cell's ILD_{ci}. When the ILD is equal to ILD_{ci}, the EI cell has the largest spike latency of T. If the ILD is larger than but still close to ILD_{ci}, Eq. (4.11) can be approximated by (because $\frac{1}{1+x} \approx 1 - x$ if x is small)

$$t_{spk} \approx T(1 - \frac{\beta}{V_\theta} ILD + \frac{\beta}{V_\theta} ILD_{ci}) \tag{4.12}$$

Because ILD_{ci} varies among the population of EI cells, for a given input ILD, Eq. (4.11) predicts that cells with smaller ILD_{ci} will fire earlier, cells with greater ILD_{ci} will fire later. Eq. (4.12) explicitly states that an EI cell's firing time is proportional to the cell's ILD of complete inhibition. Therefore, we can expect that the timing pattern among a population of EI cells is simply a reflection of the distribution pattern the ILD of complete inhibition.

4.2.2 Model Discussion

For an excitatory tone burst stimuli of duration T and level of E dB, our model predicts that the first spike latency of an LSO EI cell is proportional to T, but inversely proportional to E. In biological experiments as well as in our model study, the sound stimuli duration is often kept at a constant value. Therefore the response latency of an LSO EI cell is solely dependent on the sound stimuli level. First spike latency has been found to generally shorten with increasing input sound stimuli level (Klug et al., 2000), as we have discussed in Chapter 2. Fig. 2.5 shows the average first spike latency of LSO cells as a function of input sound stimuli level. In our model, latency response variations among the EI population for a given stimuli level can be achieved by allowing differences in membrane voltage threshold (V_θ) or synaptic strength (α).

Often the relation between external stimulus and neural steady state response is a highly compressed function, typically with a logarithmic or power-law dependences (Dayan and Abbott, 2001). In the auditory system, the firing rate of an

auditory nerve fiber is typically a rising monotonic function of stimulus level (see Eq. (2.1) for sound pressure level definition). For many fibers, the firing rate saturates at 40-50 dB above threshold (Brugge, 1992; Sachs and Abbas, 1974). As a consequence, logarithmic transfer function is commonly used for auditory modeling (e.g. Evans, 1975; Shackleton et al., 2000). One complication is that in the bat system, sounds are so short that any one fiber does not fire many spikes and operates solely as an onset response. As a consequence, information about intensity must be carried by the population response or by relative spike timing. In our circuit model, we use a logarithmic encoded envelope voltage to represent the sound pressure level sensed by the ear. To account for a population of AVCN inputs to an LSO EI cell, we have simplified the relation between the number of AVCN spikes and the input level by a function with a linear dynamic range from 0 to about 45 dB. The underlying assumption for this simplification is that the threshold of AVCN neurons is uniformly distributed among AVCN population. While it is known threshold of AVCN neurons varies among population, more detailed data about this statistic is not currently available to us.

4.2.3 Additional Considerations

As we described in Chapter 3, the VLSI integrate-and-fire neuron model we have used has a resting value of zero volt. That is, the membrane voltage cannot be a negative value. To account for this "shunting inhibition" effect, the LSO membrane

voltage can be described as

$$v_m(t) = \left[\frac{(\alpha E - \beta I)t}{T}\right]^+ \tag{4.13}$$

If the inhibitory input is greater than the excitatory input, that is $I > E$, the initial portion of the inhibitory spike train will arrive before the first excitatory spike appears. The number of inhibitory spikes that arrive before the first excitatory spike corresponds to $\left\lfloor \frac{I}{E} \right\rfloor$. To account for this loss in inhibition, the membrane voltage of LSO can be corrected as:

$$v_m(t) = \left[\alpha \left\lfloor \frac{E}{T}t \right\rfloor - \beta \left(\left\lfloor \frac{I}{T}t \right\rfloor - \left\lfloor \frac{I}{E} \right\rfloor \right)\right]^+ \tag{4.14}$$

As studied in Chapter 3, our VLSI integrate-and-fire model has a constant current leakage I_{lk} determined by Eq. (3.11). To include this leakage current, the membrane voltage of the LSO can be described by

$$v_m(t) = \left[\alpha \left\lfloor \frac{E}{T}t \right\rfloor - \beta \left(\left\lfloor \frac{I}{T}t \right\rfloor - \left\lfloor \frac{I}{E} \right\rfloor \right) - I_{lk}t\right]^+ \tag{4.15}$$

4.2.4 Circuit Analysis and Design Consideration

For a narrow spike input that arrives at t=0, the excitatory synapse (circuit schematic in Fig. 3.20(a)) outputs an exponentially decaying synaptic current that can be expressed as

$$i_{se}(t) = I_{me} e^{\frac{-t}{\tau_e}} \tag{4.16}$$

with

$$I_{me} = I_{0p} S_{20} e^{\frac{\kappa(Vdd - V_{we})}{V_T}} \tag{4.17}$$

and

$$\tau_e = \frac{C_4 V_T}{\kappa I_{0p} S_{18}} e^{\frac{-\kappa(Vdd - V_{\tau_e})}{V_T}} \tag{4.18}$$

where S_i is the aspect ratio ($\frac{W}{L}$) of transistor i, V_T is the thermal voltage. The membrane voltage rises asymptotically to a steady-state value. The increased amount of membrane voltage as denoted as α in Eq. (4.3) can be found as

$$\alpha = \frac{C_4 S_{20} V_T}{C_1 S_{18}} e^{\frac{\kappa(V_{\tau_e} - V_{we})}{V_T}} \tag{4.19}$$

For the inhibitory synapse as shown in Fig. 3.20(b), due to the parasitic capacitance, the current mirror formed by transistor M_{27}–M_{28} cannot rapidly produce an exact copy of the current on transistor M_{26}. Nevertheless, we ignore the effect of the parasitic capacitance and assume that the current mirror generate an ideal copy of the current on transistor M_{26}. Under this assumption, for a narrow spike input that arrives at t=0, the inhibitory synapse produces a current described by:

$$i_{si}(t) = -I_{mi} e^{\frac{-t}{\tau_i}} \tag{4.20}$$

with

$$I_{mi} = I_{0p} S_{26} e^{\frac{\kappa(Vdd - V_{wi})}{V_T}} \tag{4.21}$$

and

$$\tau_i = \frac{C_5 V_T}{\kappa I_{0p} S_{24}} e^{\frac{-\kappa(Vdd - V_{\tau_i})}{V_T}} \tag{4.22}$$

The inhibitory current causes the membrane voltage of the neuron to decay exponentially and ultimately reach a steady state value. The decreased amount of membrane voltage as denoted as β in Eq. (4.3) can be found to be

$$\beta = \frac{C_5 S_{26} V_T}{C_1 S_{24}} e^{\frac{\kappa(V_{\tau_i} - V_{wi})}{V_T}} \tag{4.23}$$

One assumption behind our LSO model is that for each input spike, the membrane voltage increases or decreases by a constant step. Because the membrane voltage step requires a certain settling time, this assumption requires that both τ_e and τ_i be small such that even at the maximum input level (the spike train is densest), the membrane voltage will settle before next input spike arrives. The pin $V_{\tau e}$ or $V_{\tau i}$ controls the synapse time constant. From Eq. (4.18) and Eq. (4.22), the smaller the $V_{\tau e}$ or $V_{\tau i}$, the less τ_e or τ_i is. From Eq. (4.19) or Eq. (4.23), however, decreasing $V_{\tau e}$ or $V_{\tau i}$ also reduces α or β. If $V_{\tau e}$ or $V_{\tau i}$ is too small, V_{we} or V_{wi} must be correspondingly small so that the LSO neuron will reach threshold. In order for V_{we} or V_{wi} to be within or close to the subthreshold region of transistors, we should choose the maximum $V_{\tau e}$ or $V_{\tau i}$ that allows $v_m(t)$ to reach steady state even at the densest spike train input. Because our front-end has a logarithmic envelope extraction block with a 50 dB dynamic range, we have determined that setting $V_{\tau e} = V_{\tau i} = 4.17V$ will allow $v_m(t)$ to reach steady state with a 50 dB input.

4.2.5 Test Results

We first show how the circuit model works by measuring the LSO response to a 2 ms, 40 kHz tone burst beginning at time zero. The excitation and inhibition levels used were 20 dB and 10 dB, respectively. As shown in Fig. 4.1, the 20 dB excitatory input generates a spike train of 20 spikes (top panel), and the 10 dB inhibitory input generates a spike train of 10 spikes (second panel). For each excitatory AVCN spike input, the LSO membrane voltage (bottom panel) jumps up by a constant value but

drops down by a smaller constant value for each inhibitory AVCN spike. Shown in the third panel is the measured excitatory synapse voltage (Vsyn is the voltage on C_4 in Fig. 3.20(a)). We see that its fast response produces a short time-constant synaptic current that allows the LSO membrane voltage to reach steady state before the next input spike.

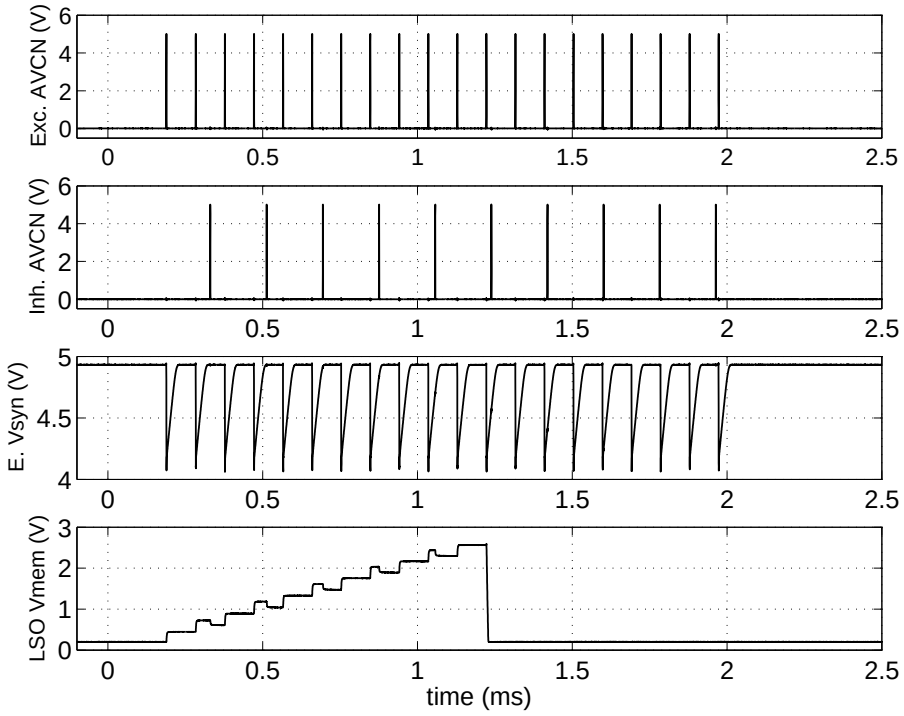


Figure 4.1: Example LSO neuron voltage traces measured from the chip in response to excitatory and inhibitory spike trains. Excitatory input spikes (upper panel) produce downward excursions of Vsyn (third panel; Vsyn is the voltage on C_4 in Fig. 3.20(a)). These excursions produce rapid, exponentially-decaying current pulses that are integrated on the membrane capacitance and appear as abrupt, rising steps in the membrane potential(bottom panel). In similar fashion, the inhibitory inputs (second panel) spikes produce downward steps in the membrane potential.

We tested our model of Eq. (4.5) by measuring from the chip one LSO cell's first spike latencies corresponding to different ILD values. During the measurement, the excitation was kept at a constant value of 40 dB. While the inhibition was varied from 0 to 40 dB. Three different excitatory synaptic weights were used: V_{we} =4.050,

4.065, and 4.075V. The measured results are shown as dots in Fig. 4.2, and the predictions from Eq. (4.5) are plotted as solid line.

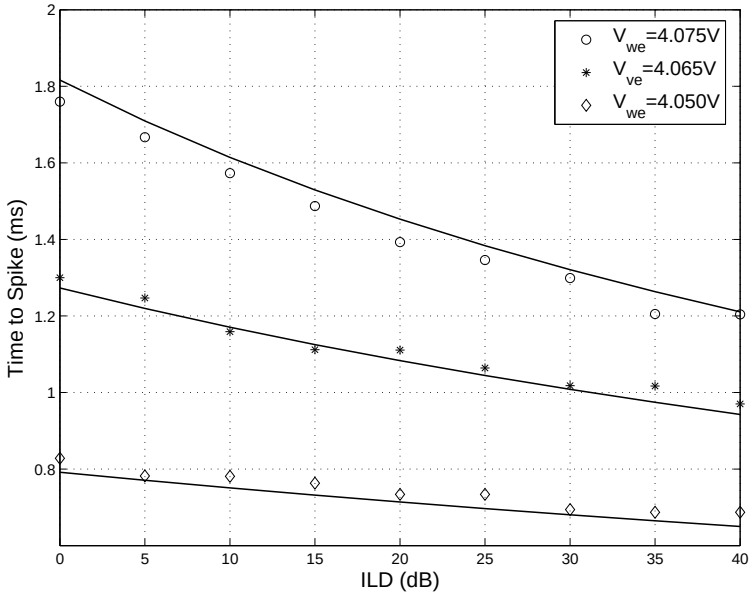


Figure 4.2: Time to first spike of LSO versus ILD at three different V_{we}. Solid lines are predicted by Eq. (4.9) with α and β measured from the chip.

4.3 Generating the LSO Population Response

As the first stage to code ILD, the goal of the circuit model of LSO is to achieve a distributed population response among LSO cells, including different ILDs of complete inhibition and different spike latencies. In this section, we examine the population response profile of the LSO layer from our chip test.

4.3.1 Experimental Setup

In many biological experiments which test ILD selectivity, tiny microphones are used as earphones fitted with probe tubes that are placed in the funnel of each

pinna of the tested animal. Different ILD values are obtained through two input schemes.

Scheme 1: Excitatory input is kept at a constant level but inhibition is varied.

Scheme 2: Inhibitory input is kept at a constant level but the excitation is varied.

For example, Park (1998) used a constant level of excitation but varied the level of inhibition, whereas Irvine et al. (2001) used a constant level of inhibition but varied the excitation. Normally, in biological experiments EI neurons from only one side of the brain are measured.

We point out that when one input scheme (e.g. Scheme 1) is applied on one side of the brain and data is collected, cells on the other side of the brain are under a different input scheme (e.g. Scheme 2). We will see that when cells are measured under different input schemes they exhibit some differences in their ILD functions.

In our experiments, stimuli were 2 ms 40 kHz AM pulse generated from two function/arbitrary waveform generators (Agilent 33120A). Stimuli were applied on the input ends of the "Logarithmic Envelope Detector" of the front-end (see Fig. 3.2). The stimuli on the right was kept at a constant value of 10 dB and the stimuli on the left varied from 0 to 45 dB in 5 dB steps, Each input combination was presented 20 times, with a time interval of 250 ms (4 Hz). Digital events including spike timing and neuron addresses were recorded with a logic analyzer (Agilent 16702B). We also used an oscilloscope to monitor the neuron membrane voltage output from scanner.

We performed two experiments with the circuit parameters listed in Table 4.1. We first focus our discussion on experimental setup No. 1. In this experiment, all

LSO cells were set to the same conditions (V_{we} for cell 1 and cell 16 were set as the same value). We intend to show that the variations inside an analog chip (such as transistor mismatch and routing variations) result in a distributed LSO population ILD response. We use experiment setup No. 2 as a comparison but omit detailed discussion.

Table 4.1: LSO Population Response Circuit Parameters Setup

Setup No.	V_{we1}	V_{we16}	V_{wi}	$V_{\tau e}$	$V_{\tau i}$
1	4.024	4.024	4.065	4.170	4.170
2	4.024	4.022	4.052	4.170	4.170

4.3.2 Sample Cell Response

We first examine the ILD functions of two cells on the left and right sides of LSO. The top of Fig. 4.3 shows the typical ILD function measured among the LSO cells. There are some common features among all the LSO ILD functions. First, if the excitation is strong, the LSO cell will fire one single spike per trial and thus 20 spikes in total 20 trials. Second, if the inhibition is strong, an LSO cell will be completely inhibited. For most of the LSO cells tested under these conditions, the transition in the ILD function curve is steep, as in the case of cell #1 for the left LSO and cell #1 and #7 in the right LSO. Cell #7 has a transition point at ILD=15 dB, at which this cell fired 13 spikes in a total of 20 trials.

For the spike latency results as shown at the bottom of Fig. 4.3, we first examine the bottom left plot. For the left LSO, the inhibitory input was kept constant, but the excitation was varied. We see that spike latency decreases as the

excitatory input increases. The intensity-latency trade off of cell #7 can be read as 100 μsec/dB from ILD=15 dB to 20 dB, but 50 μsec/dB from ILD=15 dB to 35 dB. At ILD = 15 dB, spike latency of the cell #7 was very close to 2 ms, the largest latency it could have been. This timing result was in accordance with that of the ILD function shown on the top left: cell #7 fired 13 times during 20 trials. This cell was at the edge of complete inhibition.

From the timing information shown for the right LSO on the bottom right, we see that increase inhibition in general increase spike latency. We point out that at ILD = 0 dB, an excitatory spike will arrive almost coincidently with an the inhibitory spike. From measurements we know that the amount of membrane voltage increases will be about 10% less than that if the excitatory spike does not arrive in coincidence with inhibitory spike. Because of this, at ILD = 0 dB, spike latency will have some extra positive value. For this reason, the latency curve for cell #7 jumped a little at ILD = 0.

4.3.3 LSO Population Response

From the analysis of the two sample cells above, we have come to realize that although all the LSO cells were tested under the same conditions (as can be seen from Table 4.1), cell #1 and cell #7 have different ILD complete inhibition and different spike timing. In fact, all of the LSO cells in the chip behave differently in the sense that they may have different ILD_{ci} and different spike latencies. We examine the population profile in Fig. 4.4 and present the population data in three

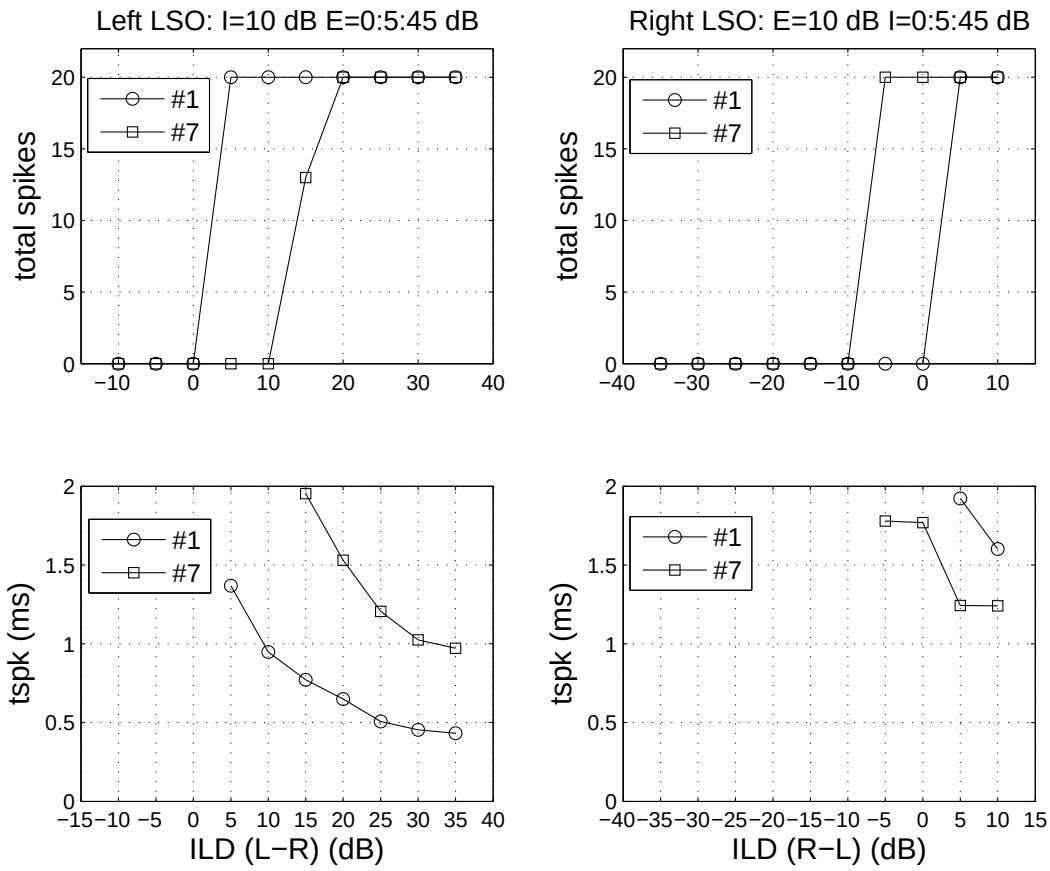


Figure 4.3: Example LSO ILD function and spike timing. Top: ILD functions for two LSO cells. Bottom: Average spike latencies. Left column for left LSO, right column for right LSO. Stimuli were 2 ms 40 kHz AM pulse. Left stimuli varied from 0 to 45 dB at 5 dB steps, right stimuli was kept at constant of 10 dB. 20 trials performed.

ways. First, we plot the histogram of ILD complete inhibition from the 16 cells in the left and right LSO (top panel). Second, we plot out specifically the ILD_{ci} for each cell (middle panel). Third, we plot the total number of cells that fired for a given ILD input, as shown in the bottom panel.

From the histogram of the ILD of complete inhibition, we see that ILD_{ci} varied among the population, our chip successfully generated a distribution of ILD responses in the SO population. The left LSO and right LSO, due to the different

input variation scheme, exhibited different distribution patterns. The left LSO ILD_{ci} were distributed amongst the positive ILD values, centered around 10 dB. The right LSO ILD_{ci} were distributed toward negative ILD values.

What caused the cells on either side to exhibit different values of ILD_{ci}? Transistor mismatch is one reason. For cell #1 and cell #16, the excitatory synaptic weight of these two cells were set exactly the same by an external power supply (V_{we1}=V_{we16}=4.024 V). While the left LSO cell #1 and cell #16 have the same ILD_{ci} of 0 dB (middle left), the right LSO cell #1 and cell #16 had different ILD_{ci} values: 0 dB and 5 dB, respectively.

The distribution of ILD_{ci} among 16 cells, although no systematic ordering by the cell number could be seen in the middle right plot, did code ILD in a clear way: the total number of LSO cells fired changes systematically with the input ILD. This is clearly demonstrated in the bottom panels. There is a range where the total number of LSO cells fired increases monotonically with ILD.

We present an LSO population spike timing raster display in Fig. 4.5. Shown are rater plots for 20 trials, for 8 different ILD inputs. From this group of timing results, we observe the following points.

1. As the input to the left LSO increased from 0 to 35 dB, the trend across the LSO population was that number of left LSO cells that fired increased, but the number of the right LSO cells fired decreased. Also, the left LSO spike latencies decreased while the right LSO spike latencies increased.

2. Because the excitatory strength was relatively strong, we see that jitter in the

spike latency among different trials were very small.

3. To a large extent, the pattern of spike latencies among the 16 LSO cells in either side resemble the pattern of the ILD of complete inhibition among those cells. This can be seen from the plot for "L=0 dB R=10 dB" in comparison with the middle right panel of Fig. 4.4, and the plot for "L=35 dB R=10 dB" in comparison with the middle left panel of Fig. 4.4.

4. Although the left cell #l and cell #16 had the same ILD_{ci}, as we discussed above, their spike timing was different. This can be seen most clearly in the plot for "L=15 dB R=10 dB", which showed more than 0.5 ms difference in spike latency. This confirms that mismatch of transistors is one source of variations in the population response to ILD.

5. The two LSO arrays are not symmetrical. Rather, the right LSO array showed stronger response. This can be seen in the plot for "L=10 dB R=10 dB", where none of the left LSO cells fired but 9 of the right LSO cells fired. This imbalance between the two sides of the chip may be due to physical paths of wiring in the layout and the placement of a scanner only on the left LSO array.

Last, we show one more profile from a slightly different circuit setup in Fig. 4.6. The specific circuit parameters are listed in Table 4.1 as Setup No. 2. The major difference is that the inhibition strength was increased, and a slightly different excitatory strength among the 16 cells was used. We omit detailed discussion for the results for this experiment.

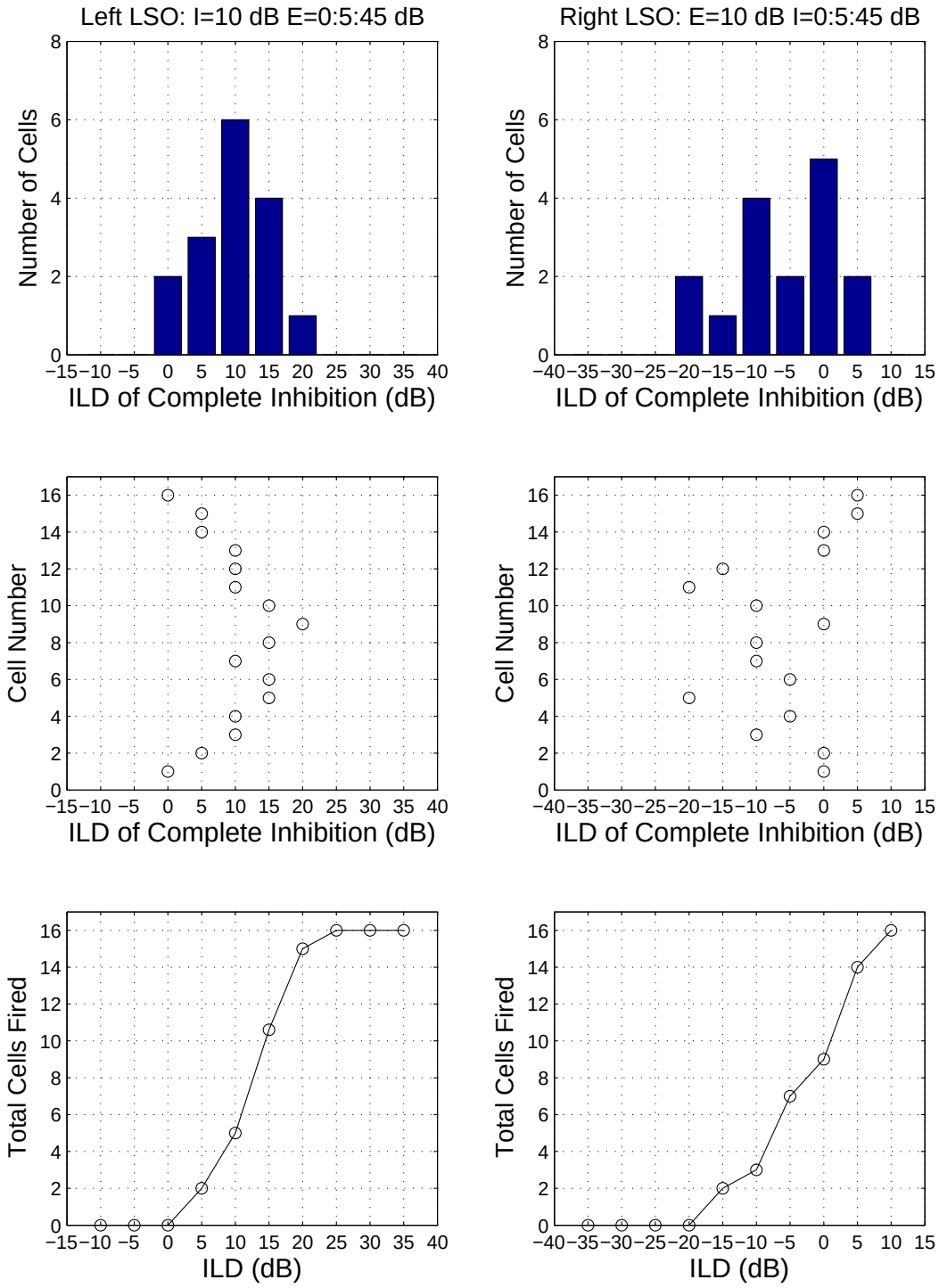


Figure 4.4: LSO population response profile. Top: Histogram of ILD complete inhibition among 16 cells. Middle: ILD complete inhibition of each 16 cells. Bottom: Total number of cells fired at given ILD input. Left column for left LSO, right column for right LSO. Stimuli were 2 ms 40 kHz AM pulse. Left stimuli varied from 0 to 45 dB in 5 dB step, right stimuli was kept constant at 10 dB. This data was compiled from 20 trials.

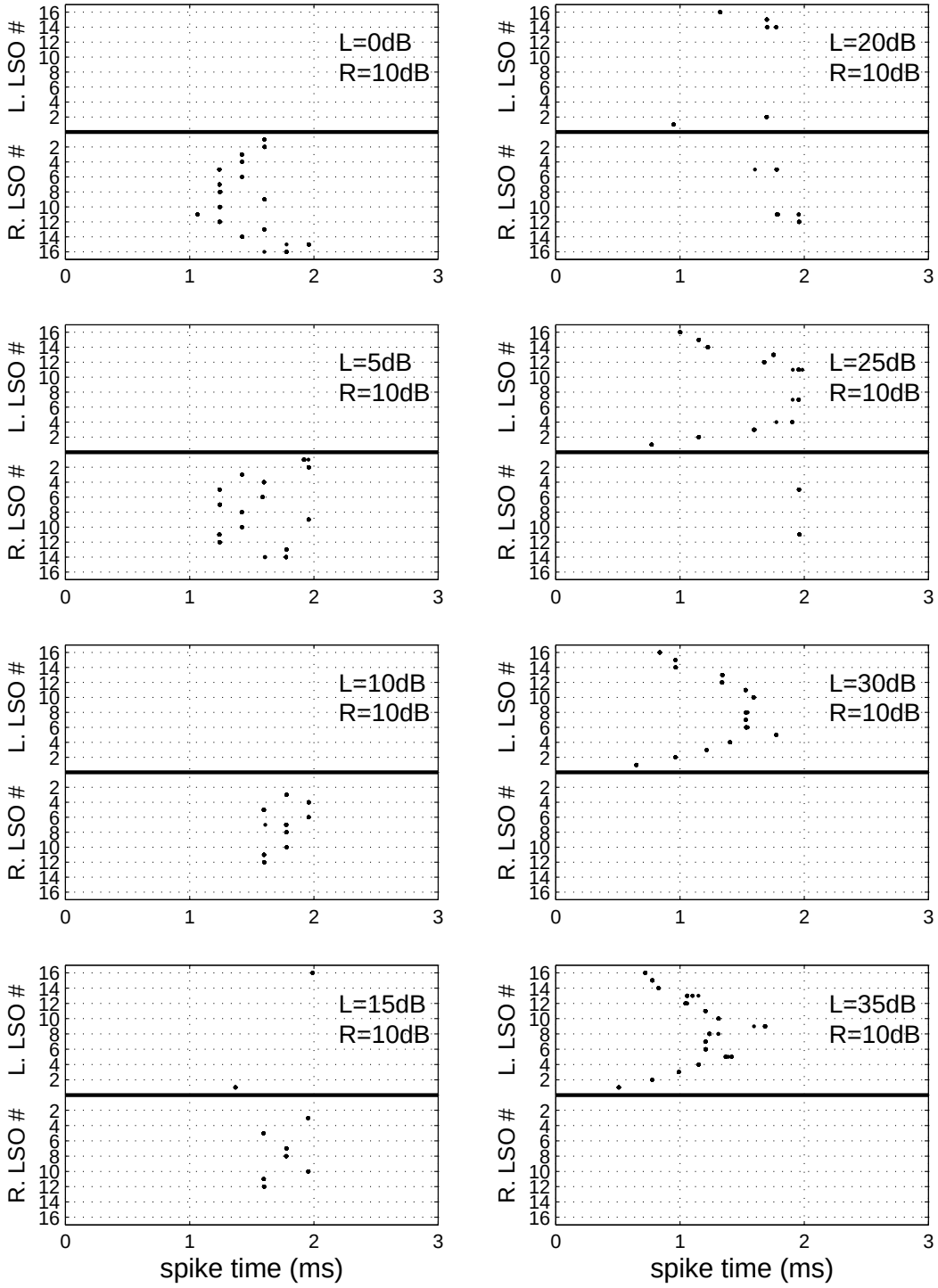


Figure 4.5: LSO spike timing raster display for 8 different ILD inputs. Shown are raster plots from 20 trials.

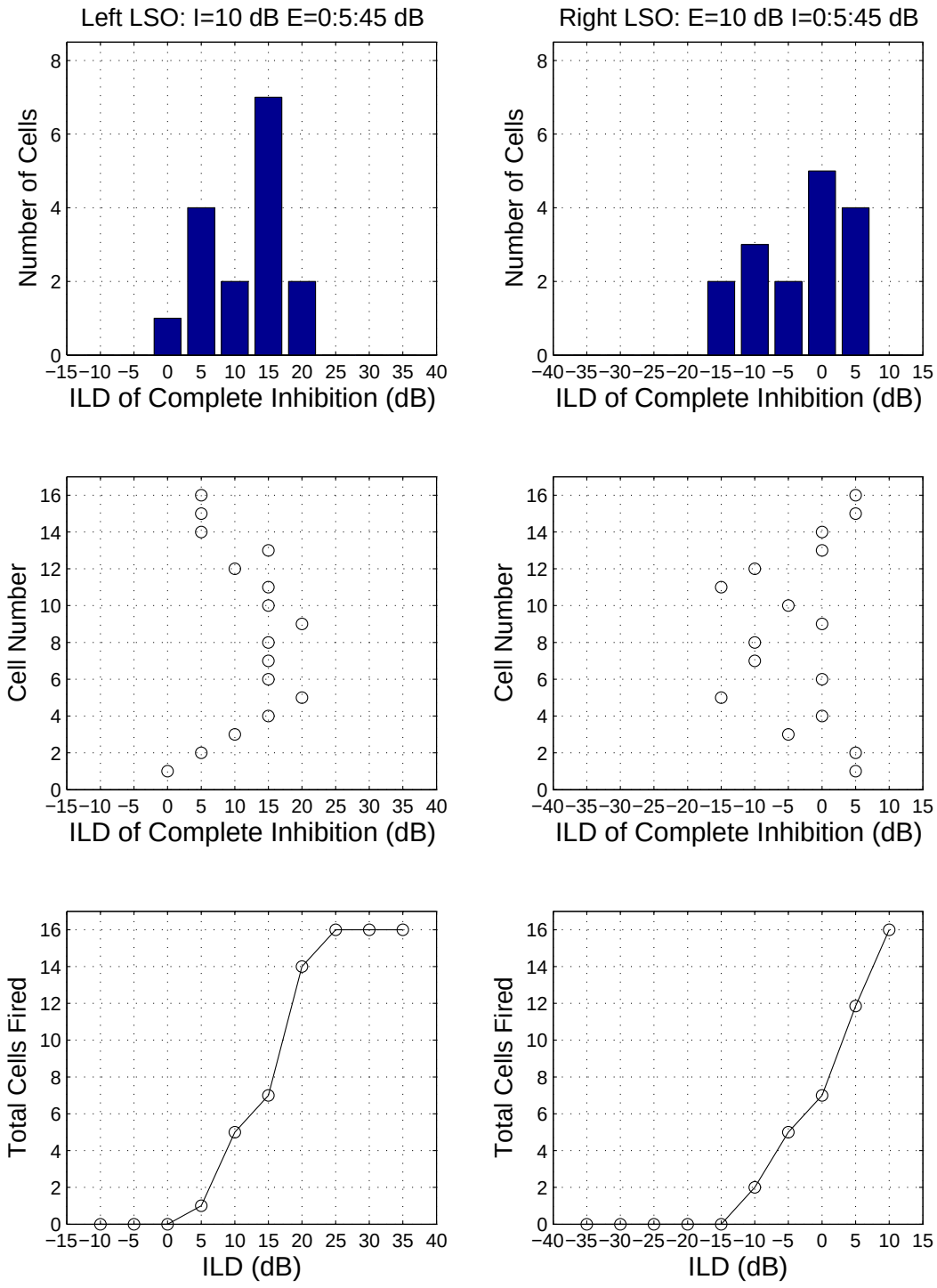


Figure 4.6: LSO population response profile for circuit parameters setup No. 2. Top: Histogram of ILD complete inhibition among 16 cells. Middle: ILD complete inhibition of each 16 cells. Bottom: Total number of cells fired at given ILD input. Left column for left LSO, right column for right LSO. Stimuli were 2 ms 40 kHz AM pulse. Left stimuli varied from 0 to 45 dB in 5 dB steps, right stimuli was kept constant at 10 dB. This data was compiled from 20 trials.

4.4 Discussion

We have proposed a circuit model that employs the first spike latency for the ILD computation in the bat LSO. Our model is based on the current understanding of the mechanism that underlies an EI cell's sensitivity to ILD. Our model is also inspired by recent research results showing that spike timing can provide more information than a firing rate code. Such a spiking neural model emphasizes the importance of timing between the excitatory and inhibitory spike trains and the output of the LSO cell carries this timing information to the next stage.

Our model provides a unified scheme between the two most important parameters of EI cells: the spike timing of an EI cell and its ILD complete inhibition. Under the simplified modeling scheme, we have shown that the first spike latency of an EI cell and its ILD of complete inhibition are correlated. The finding that the pattern of spike timing among the population is simply a reflection of the distribution of the ILD of complete inhibition contributes to the bat ILD research community at least in two aspects. First, it strongly suggests that spike timing information should be studied together with the ILD of complete inhibition. We say this because most biological studies on bat ILD to date have focused on an EI cell's ILD of complete inhibition. There are no studies that relate the spike timing with the ILD_{ci}. Second, it suggests that the spike timing of each cell and the timing pattern among the population may code the azimuth. We say this because it is commonly believed that ILD_{ci} codes the azimuth information. Logically then, the timing distribution may code the azimuth.

Our model simplifies ILD computation at the LSO as a linear superposition of excitation and inhibition and a nonlinear shunting effect from inhibition when the membrane voltage is zero. We achieve this linear superposition of excitation and inhibition by using a compact synapse that operates on a very short time scale in response to each input spike. This linear subtraction is, however, an approximation of the "staircase" function. We have thus identified a need for a synapse circuit that allows linear temporal spike summation. We will present our effort toward designing this type of synapse in Chapter 7.

The diversity of ILD responses in the population of LSO cells was achieved by virtue of the nature of analog VLSI circuits fabrication. To mimic the massively-parallel computations seen in neural systems, neuromorphic VLSI modeling use analog circuits for neural computation and use digital circuits for spike transmission and communication. The mismatch of transistor characteristics on the fabricated die is unavoidable, especially for transistors operating at the subthreshold region. Variations among analog circuit units have been traditionally thought of hurdle to overcome. Analog circuit designers used to resolve this issue by using large transistors or designing mismatch-tolerant circuitry using high-gain feedback circuits. This study suggests that variations in analog VLSI circuit can be beneficial in generating the desired diversity of responses that are similar to their neural counterparts. This idea has been discussed in Merolla and Boahen (2006). In their case, the clusters of neural activity in a two-layer recurrent network of spiking neurons are pinned to certain locations due to transistor mismatch in a fabrication die.

Chapter 5

Dorsal Nucleus of the Lateral Lemniscus and Inferior Colliculus: Network Transformation

As in the LSO, the DNLL and inferior colliculus (IC) consist of a large portion of EI cells. EI response patterns to different ILDs are initially created in the LSO are then imposed onto ascending stages through a strong, crossed excitatory projection. Substantial modification of EI properties can also occur at the IC by ipsilaterally evoked inhibition. In this chapter, we present our circuit model of ILD processing and transformation in the DNLL and IC. Our focus is on illustrating how EI properties in the IC can be formed in multiple ways.

5.1 Inheriting ILD Properties from the LSO

About half of the EI cell population in either the DNLL or IC inherit their ILD properties from the LSO, through the strong excitatory projection from the LSO to the opposite DNLL and IC (Klug et al., 1995; Pollak et al., 2002). Such EI cells in the DNLL and the IC are termed "copy cells" in this work.

5.1.1 Circuit Model

Fig. 5.1 shows the network connection of copy cells in our circuit model. Each left LSO cell L_i^1 drives an opposite DNLL cell R_i^2 and IC cell R_i^3 (i=1,...16) through an excitatory synapse. Similarly, each right LSO cell drives a left DNLL cell and left IC cell. Each DNLL and IC neuron receives only an excitatory projection from the corresponding neuron in the opposite LSO. In this type of network, EI properties are created in the LSO and are conferred onto upper layers if the excitatory synaptic strength is sufficient to produce one output spike in response to one input spike.

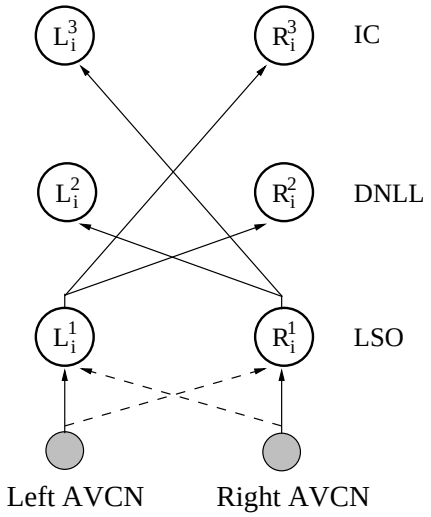


Figure 5.1: The "copy cell" network connection. Each DNLL and IC neuron only receives an excitatory projection from its opposite LSO (i = 1, ... , 16). In this type of network, EI properties are created in the LSO and are conferred onto upper layers if the excitatory synaptic strength is sufficient to produce one output spike with one input spike.

If a copy cell in either DNLL or IC receives an excitatory spike at time t_0. This spike input will produce an excitatory synaptic current in the form

$$i_{se}(t) = I_{me} e^{-\frac{t-t_0}{\tau_e}} \tag{5.1}$$

where I_{me} and τ_e are defined by Eqs. (4.17) and Eq. (7.11), respectively.

If the leakage current is small, the time to the first spike is

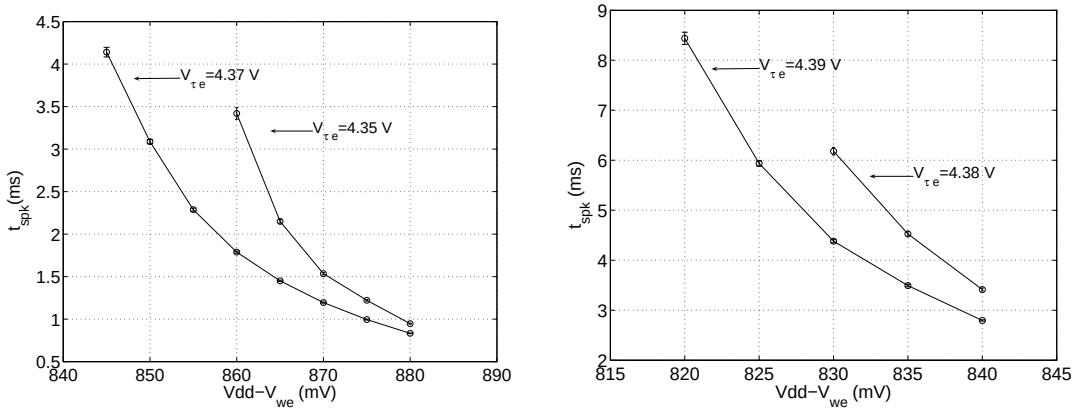
$$t_{spke} = t_0 + \tau_e \ln(\frac{\tau_e I_{me}}{\tau_e I_{me} - C_m V_\theta}) \tag{5.2}$$

where V_θ is the neuron's threshold voltage, and C_m is the neuron's membrane capacitance.

Spike latency has been reported to increase in stages along the ascending pathway; DNLL neurons normally have latencies greater than in the LSO, and IC neurons normally have greater latencies than DNLL (Klug et al., 2000). Eq. (5.2) states that in order to increase spike latency, one can either decrease I_{me} by reducing the synaptic strength $Vdd - V_{we}$, or increasing synaptic time constant τ_e by increasing $V_{\tau e}$. Fig. 5.2 shows how we can achieve different spike latency by controlling two synaptic circuit parameters: the synaptic weight V_{we} and the synaptic time constant $V_{\tau e}$.

5.1.2 Chip Test Example

We illustrate how DNLL and IC EI cells can inherit their ILD properties from the LSO by showing one specific test example. In the test, the LSO layer was configured in the same way as setup No. 1 in Section 4.3.1. The stimuli were 2 ms long 40 kHz AM pulses and were applied on the input ends of the "Logarithmic Envelope Detector" of the front-end (see Fig. 3.2). Stimuli on the right were kept constant at 10 dB, stimuli on the left were varied from 0 to 45 dB in 5 dB steps. Each ILD combination was presented 20 times, with a time interval of 250 ms (4 Hz). For the LSO, all cells were set with $V_{we} = 4.024V$, $V_{wi} = 4.065V$, $V_{\tau e} = V_{\tau i} = 4.172V$.



(a) DNLL Copy Cell

(b) IC Copy Cell

Figure 5.2: Circuit parameters that control spike latency of the copy cell. For two fixed synaptic constants controlled by $V_{\tau e}$, spike latency increases as synaptic strength $Vdd - V_{we}$ decreases. (a) Spike latency in a range between 1 to 3 ms achieved for a DNLL copy cell. (b) Spike latency in a range between 3 to 9 ms achieved for a IC copy cell. Stimuli were 2 ms long 40 kHz AM tone bursts. Shown are average spike latencies over 50 trials, with error bars for the standard deviation.

For the DNLL, all cells were set with $V_{we} = 4.133V$, $V_{\tau e} = 4.356V$. For the IC, all cells were set with $V_{we} = 4.170V$, $V_{\tau e} = 4.378V$. The leak current parameters for all neurons were set with $V_{lk} = 0.219V$.

Fig. 5.3 shows the population response from one chip. We see that with the connection scheme of Fig. 5.1, the DNLL and IC cells "copied" their ILD properties from the LSO. For this particular test, excitatory strength were set relatively large so that each DNLL and IC cell could copy its ILD property from the LSO faithfully.

Next we examine ILD tuning curves and spike latency. We picked out three typical cells (cell #1, #2, and #7 from the 16 cell array). In Fig. 5.4, the left column shows the typical ILD tuning curves of these three cells. We see that the ILD_{ci} are at 0 dB, 5 dB and 10 dB for cells #1, #2, and #7, respectively. Correspondingly, cell #1, #2, #7 in the left DNLL and the left IC have the same ILD_{ci} as their LSO

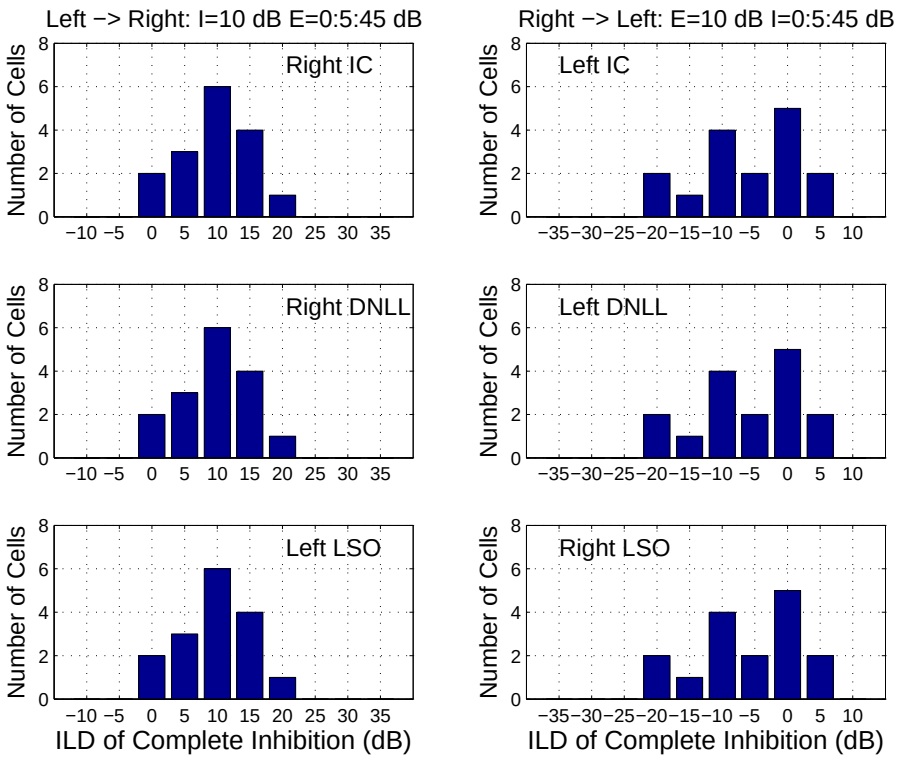


Figure 5.3: Histograms of the copy cell population response in a chip-wide test. Left column: The left LSO neuron population generate EI responses (lower-left panel) and right DNLL neurons (middle-left panel) and right IC neurons (upper-left panel) inherit their ILD properties from these cells. ILD is defined as Left - Right. Right column: Right LSO neuron population individually generate EI responses (lower-right panel) and left DNLL neurons (middle-left panel) and left IC neurons (upper-left panel) inherit their ILD properties from these cells. ILD is defined as Right - Left.

cells. In the right column, we show the spike latency for cell #1 at different ILDs. The solid line with circles shows the mean values of spike latency over the 20 trials. The standard deviation (known as spike jitter) for each ILD value over 20 trials is shown as error bars on the plot. We see that as the latency increases from the LSO to the IC, the spike jitter also increases.

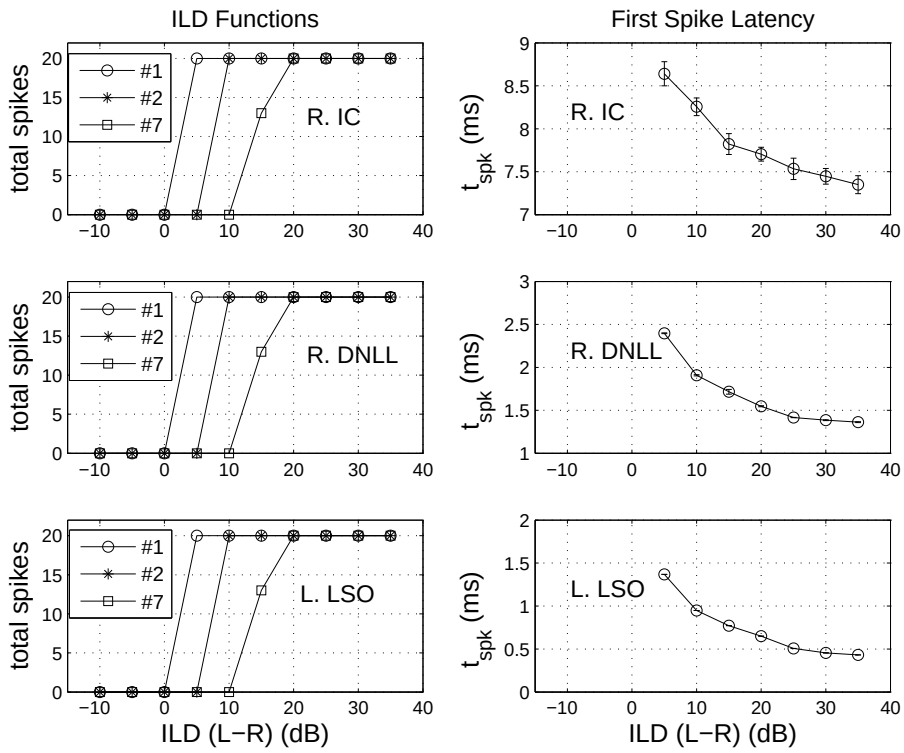


Figure 5.4: ILD turning curves of three copy cells and spike latency for copy cell #1. Left column: ILD functions for cell #1, #2 and #7. Right column: Average spike latency over 20 trials of cell #1, with error bar showing standard deviation. Note the different time scales for each plot of t_{spk}.

5.2 EI Cell Modified from Lower Stages

The EI properties that are first formed in the LSO and then imposed on IC can be substantially modified by ipsilaterally driven inhibition. We call this type of EI neuron a "modified cell" in the text. One well known source for the ipsilaterally evoked inhibition is from the contralateral DNLL, and the resultant modification is to shift the ILD_{ci} toward more positive ILD values (Park and Pollak, 1993; Pollak et al., 2002).

5.2.1 Circuit Model

Fig. 5.5 illustrates a specific network connection for a representative right IC cell. This right IC cell receives excitatory input from the left LSO and thus inherits the EI properties first formed in the LSO. The inhibitory input to this right IC cell is from the left DNLL via the right LSO. This ipsilaterally driven inhibitory input modifies the EI properties inherited from the left LSO.

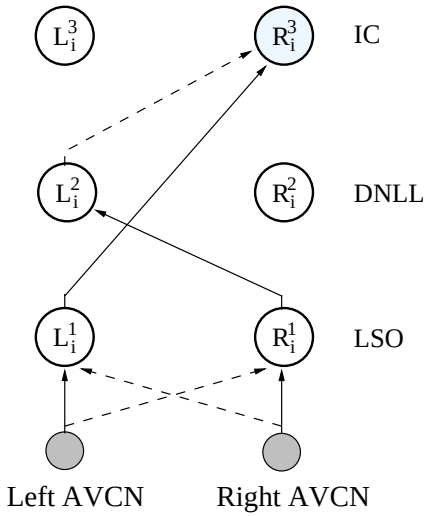


Figure 5.5: The "modified cell" network connection. A representative right IC cell receives its excitatory input from contralateral LSO and thus inherit its EI property from the LSO. The ipsilaterally driven inhibitory input from the contralateral DNLL via ipsilateral LSO, however, will modify the EI properties of this right IC cell.

In our LSO model, an LSO EI cell receives a spike train that encodes sound intensity information. We trade spatial summation (spikes from various AVCN neurons) for temporal summation by a linear synapse circuit. In modeling the EI circuit in the DNLL and IC, each EI cell is driven by one excitatory and one inhibitory synapse for each input neuron. Although our AER structure and our PIC microcontroller-based, reconfigurable design allow us to map multiple inputs to one target neuron, in this work we have focused on an EI cell in the DNLL or IC that

receives a single spike from each input.

Spike latencies of LSO neurons carry information about the stimulus sound intensity, as can be seen from Eq. (4.5). The ILD response property of an EI cell in the DNLL or IC, receiving excitation and inhibition from different pathways, will depend on the relative time difference between excitation and inhibition as well as the properties of its inputs.

We consider an EI cell in the DNLL or the IC layer that receives a single excitatory spike and a single inhibitory spike. As illustrated by Fig. 5.6, if the excitatory synapse is strong enough to produce a postsynaptic spike at time t_{spke}, then the conditions exist for an inhibitory spike to prevent or shift the time of the spike. For what maximum delay of inhibition (t_d) will the EI cell be suppressed?

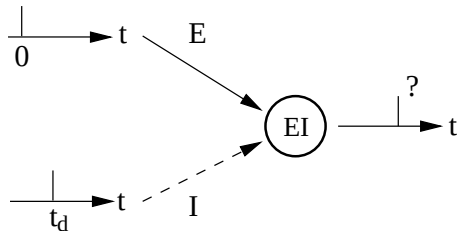


Figure 5.6: The arrival time of an inhibitory spike modifies the EI properties. An excitatory spike arrives at time zero and causes the EI cell to fire. An inhibitory spike arrives at time t_d. This delay between excitation and inhibition carries sound intensity information, and determines the EI cell's response property.

Consider an inhibitory spike arriving at a time delay t_d, and assume the ideal form

$$i_{si}(t) = I_{mi} e^{\frac{-(t-t_d)}{\tau_i}} \tag{5.3}$$

In terms of circuit design, how do we choose I_{mi} and τ_i to modify the EI neuron? We consider first a special case when $\tau_e = \tau_i$.

If $\tau_e = \tau_i$, then the minimum I_{mi} to inhibit the EI neuron is

$$\tau_e I_{me} - \tau_i I_{mi} = C_m V_\theta \tag{5.4}$$

We point out that there is one interesting property for this special case: any inhibitory spike arriving before t_{spke} will inhibit the EI neuron. Because of this, the maximum t_d is t_{spke}, and can be found as

$$t_d = \tau_e \ln\left(\frac{I_{me}}{I_{mi}}\right) \tag{5.5}$$

Such a design is simple and will have the greatest time window (because $t_d = t_{spke}$). But it has the drawback that it loses the intensity-latency coding information of the inhibitory spike. If it is necessary to have an inhibitory spike that arrives earlier than t_{spke} to continue carrying intensity information, we may select a τ_i larger than τ_e.

For $\tau_i > \tau_e$, the idea is to arrange for the EI neuron to have a peak voltage value which increases as t_d increases. The peak value occurs at time t_θ when $i_{se}(t_\theta) = i_{si}(t_\theta)$. The maximum t_d is such that the EI neuron's membrane voltage reaches the voltage threshold V_θ, and can be found as

$$t_d = \tau_i \ln\left(\frac{I_{me}}{I_{mi}}\right) + (\tau_e - \tau_i) \ln\left[\frac{(\tau_e - \tau_i) I_{me}}{\tau_i I_{mi} - \tau_e I_{me} + C_m V_\theta}\right] \tag{5.6}$$

Because we have

$$\lim_{\tau_i \to \tau_e} (\tau_e - \tau_i) \ln\left[\frac{(\tau_e - \tau_i) I_{me}}{\tau_i I_{mi} - \tau_e I_{me} + C_m V_\theta}\right] = 0 \tag{5.7}$$

Eq. (5.6) reverts to Eq. (5.5) when $\tau_i = \tau_e$.

In Fig. 5.7, we show how an IC cell that receives an excitatory spike at time zero and an inhibitory spike with time delay t_d can produce a different response.

For each t_d, 100 trials were performed. In synapse 1, $V_{we} = 4.170V$, $V_{wi} = 4.220V$, $V_{\tau e} = 4.350V$, $V_{\tau i} = 4.360V$, and $V_{lk} = 0.241V$. We see at 50% firing probability, t_d is about 0.9 ms. In synapse 2, $V_{we} = 4.200V$, $V_{wi} = 4.230V$, $V_{\tau e} = 4.390V$, $V_{\tau i} = 4.410V$, and $V_{lk} = 0.241V$. For these parameters, we see at 50% firing probability, t_d is about 2.3 ms.

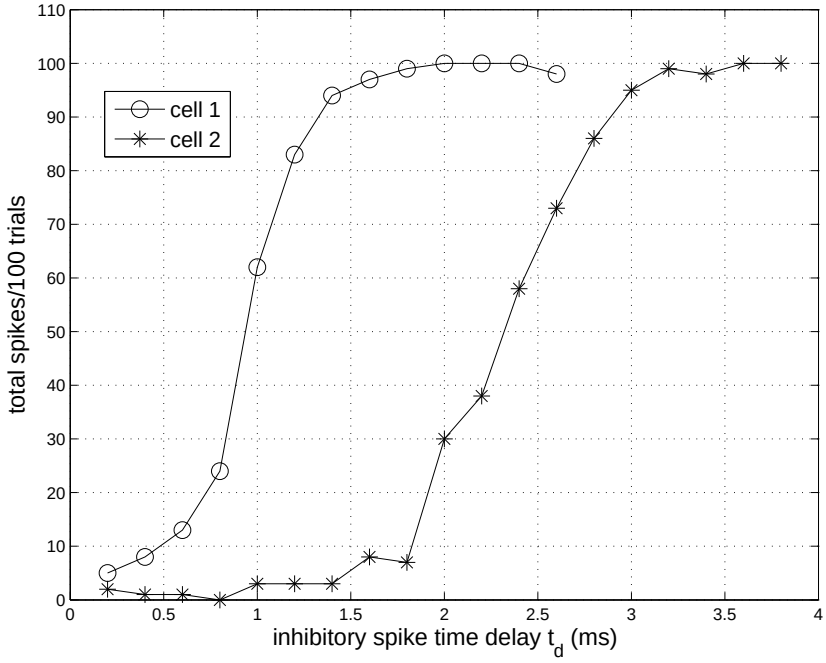


Figure 5.7: Time differences between the excitatory input spike and inhibitory input spike affect the EI properties being transmitted from below. When EI neurons in layer 3 (IC) receive an excitatory spike at time = 0 and receive an inhibitory spike with a time delay t_d, the inhibition has narrow window of time during which it is capable of suppressing the neuron. For each t_d, 100 trials were performed.

5.2.2 Modified Cell Test Example

We present one example of data from our circuit model of the modified cell. We focus on one representative right IC cell whose network connection is shown in Fig. 5.5. In the test, the excitatory input (input to the left side) was kept constant

at 20 dB. The inhibitory input (input to the left side) varied from 0 to 45 dB. Each combination of ILD input was presented 20 times. The LSO were set with $V_{we} = 4.040V$, $V_{wi} = 4.103V$, $V_{\tau e} = V_{\tau i} = 4.172V$. The DNLL was set with $V_{we} = 4.150$ V, $V_{wi} = 4.147$ V, $V_{\tau e} = 4.362$ V, $V_{\tau i} = 4.168$ V. The IC cell was set with $V_{we} = 4.171$ V, $V_{wi} = 4.132V$, $V_{\tau e} = 4.370V$ and $V_{\tau i} = 4.371$ V. The leak parameter, V_{lk}, was set to be 0.220V for all neurons.

Fig. 5.8 shows ILD functions and spike latencies from the test. In the left column, we see that the left LSO had an ILD_{ci} of -10 dB, the right LSO had an ILD_{ci} of 5 dB. The left DNLL inherited its ILD properties from the right LSO and thus had a ILD_{ci} of 5 dB. The convergent projections from the left LSO and left DNLL caused the right IC cell to have a ILD_{ci} of 0 dB, which was a +10 dB shift from that of the left LSO input.

The right column of Fig. 5.8 shows the mean spike latencies and standard deviation (error bars) over 20 trials. For ILDs from 5 to 20 dB, the right IC cell fired with latencies within 5 to 6 ms. Because there was no inhibitory input from the left DNLL, this IC cell simply relayed the EI properties formed in the left LSO. The latency-intensity trading in this IC cell was caused by the LSO cell. This can be seen from the fact that the curve in the right top panel is parallel to the curve in the right bottom panel. For ILDs from 0 to -25 dB, the left DNLL fired. We see that the left DNLL spike latencies were less than 4 ms. That is, the inhibitory input from the left DNLL cell arrived at the IC before it would fire. Our circuit model and the specific circuit parameters assured that such an inhibitory spike will prevent the IC cell from firing. The latency-intensity slope from 0 to -5 dB is greater than

that from -10 to -25 dB. From 0 to -5 dB, increasing intensity from the right side caused right LSO spike latency to decrease. At the same time, it also caused the left LSO spike latency to increase. From -5 to -25 dB, however, the latency-intensity relationship in the IC was simply a copy of the right LSO properties due to the lack of inhibition from the left LSO.

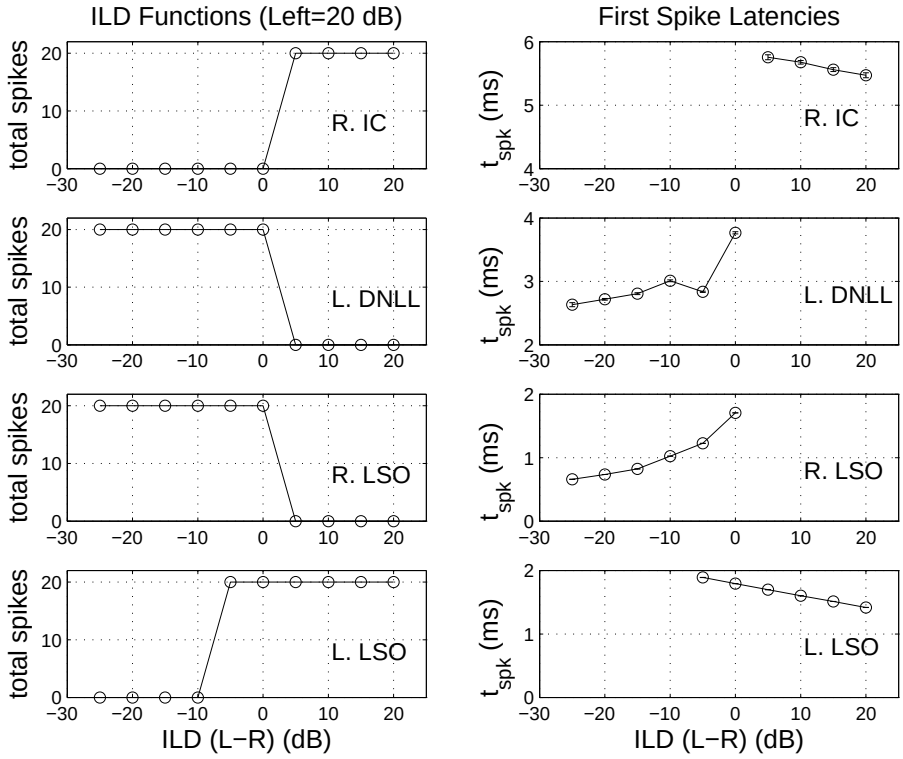


Figure 5.8: Example EI cell modified in the IC. Left: ILD functions. Right: Mean spike latency and standard deviation (error bar) over 20 trials. The right IC cell receives excitation from the left LSO and inhibition from the left DNLL. These convergent projections resulted in a right shift of ILD_{ci} from -10 dB in the left LSO to 0 dB in the right IC. Note the different time scales used in each plot of t_{spk}.

5.3 EI Cell Created *De Novo*

EI cells can also be created *de novo* in the IC. We refer to this type of EI cell in the IC as "*de novo* cell" in this text. The *de novo* creation in the IC is through

an excitatory input from a lower monaural nucleus on the contralateral side and an ipsilateral inhibitory input either from ipsilateral LSO, or contralateral DNLL (Klug et al., 1995; Park and Pollak, 1993). The real source of the lower monaural input is unknown, but it has been suggested that inputs from the cochlear nucleus may play this role. Below, we study how EI properties can be created anew with contralateral AVCN input, and ipsilateral inhibition through the contralateral DNLL.

5.3.1 Circuit Model

Fig. 5.9 illustrates a specific network connection scheme for a representative *de novo* EI cell. The right IC cell receives excitation from the left AVCN, and the inhibition from the left DNLL, which in turn is excited by the ipsilateral LSO.

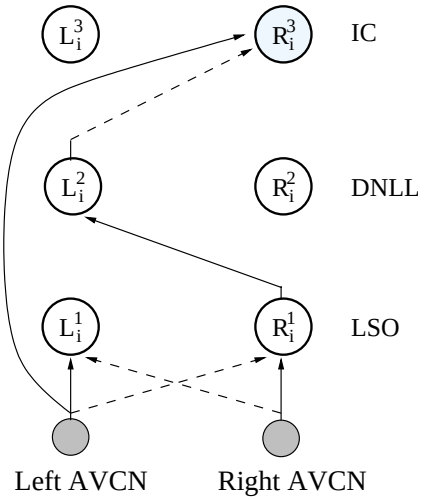


Figure 5.9: The "*de novo* cell" network connection. An representative right IC cell receives its excitatory input from contralateral AVCN. The inhibitory input to the IC cell is from contralateral DNLL via ipsilateral LSO.

Assume this IC cell receives only excitation from contralateral AVCN. For

input level E (dB), the AVCN spike count is

$$N_E(t) = \left\lfloor E\frac{t}{T} \right\rfloor \tag{5.8}$$

If E = 1 dB, there is only one single AVCN spike occurs at time t=T. If the leakage current is small, the membrane voltage of the EI cell will be

$$v_m(t) = \frac{\tau_e I_{me}}{C_m}(1 - e^{-\frac{t-T}{\tau_e}}) \tag{5.9}$$

If $E > 1$ dB, there will be $N_E = \lfloor E \rfloor$ spikes in duration of T. To achieve large spike latency for the IC EI cell, the synaptic time constant τ_e is large. Because the stimuli duration T is much smaller than τ_e , the synaptic current decay is small before next spike comes. So if $E >> 1$ dB, AVCN spike train generates a constant synaptic current of amplitude I_{me} with duration of $\frac{N_E-1}{N_E}T = \frac{E-1}{E}T$. The neuron membrane voltage will be

$$v_m(t) = \frac{E-1}{E}\frac{TI_{me}}{C_m} + \frac{\tau_e I_{me}}{C_m}(1 - e^{-\frac{t-T}{\tau_e}}) \tag{5.10}$$

And the time to the first spike can be found as

$$t_{spke} = T + \tau_e \ln\left[\frac{\tau_e I_{me}}{(\tau_e + \frac{E-1}{E}T)I_{me} - C_m V_\theta}\right] \tag{5.11}$$

Fig. 5.10 shows the first spike latency measured from a sample *de novo* IC cell in the chip. Stimulus was 2 ms 40 kHz AM tone burst. Shown are averaged spike latency over 20 trials for two example circuit parameters. We see the spike latency decreases as input excitation level increases. Within the first 10 dB, the latency reduces sharply as excitation level increases. Above 15 dB, latency-intensity trading is much smaller and falls almost linearly as excitation increases.

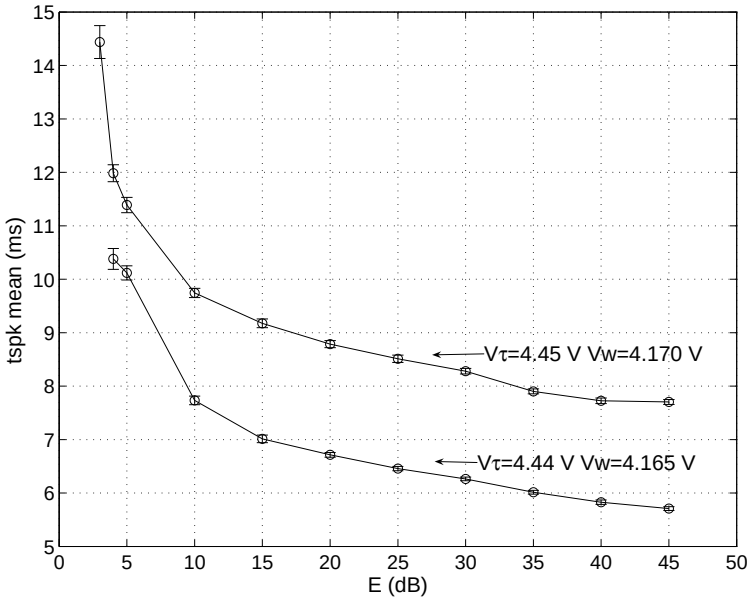


Figure 5.10: Spike latency of a *de novo* IC cell driven by contralateral AVCN. Shown are averaged spike latency and standard deviation (error bar) under 20 trials for two example circuit parameters.

If an ipsilateral inhibitory input is evoked, the IC cell will receive inhibition from the contralateral DNLL. We will show next how the EI properties can be created in the IC when binaural inputs are applied.

5.3.2 Chip Test Example

We present one test example of our circuit model of the *de novo* cell. We focus on one representative right IC cell whose network connection is shown in Fig. 5.9. In the test, the excitatory input (input to the left side) was kept constant at 20 dB. The inhibitory input (input to the left side) varied from 0 to 45 dB. The LSO were set with $V_{we} = 4.033V$, $V_{wi} = 4.091V$, $V_{\tau e} = V_{\tau i} = 4.172V$. DNLL was set with $V_{we} = 4.134$ V, $V_{\tau e} = 4.355$ V. The IC cell was set with $V_{we} = 4.182$ V, $V_{wi} = 4.292$ V, $V_{\tau e} = 4.448$ V and $V_{\tau i} = 4.457$ V. All LSO and DNLL neurons leakage were set

with $V_{lk} = 0.220$ V. All IC neurons leakage were set with $V_{lk} = 0.219$ V.

Fig. 5.11 shows ILD tuning curves and spike latency. In the left column, we see that the left LSO had an ILD_{ci} of -15 dB, and the right LSO had an ILD_{ci} of 5 dB. The right DNLL inherited an ILD_{ci} of 5 dB from the right LSO. The right IC cell, receiving excitatory input directly from left AVCN and inhibitory input from left DNLL, formed its EI property in the IC anew by exhibiting an ILD function that was different from either left LSO or right LSO.

It is noteworthy that for this test example, the right IC cell cannot be said to be in "complete inhibition" even when the inhibition level was at maximum value. We may gain some more insight from the right column of Fig. 5.11 which shows the timing information. At an ILD of 0 dB, the left DNLL started to fire. We see at this inhibition level, the inhibitory spike from the left DNLL did not prevent the IC cell fire (the IC cell still fired 19 times out of 20 trials). Rather, the effect of the inhibitory spike was to delay the firing time of the IC cell (from about 7 ms at 5 dB to 10 ms at 0 dB). Further increasing inhibition level resulted in less spike firing probability and greater spike latency.

5.4 Facilitated EI (EI/F) Cells

Facilitated EI (EI/F) cells are the most spatially selective cells in the IC: they respond maximally in a particular spatial region (i.e. a small range of ILD). In one study of mustache bats, 30% of EI cells in the inferior colliculus were classified as EI/F neurons (Park and Pollak, 1993). EI/F cells provide us with an interesting

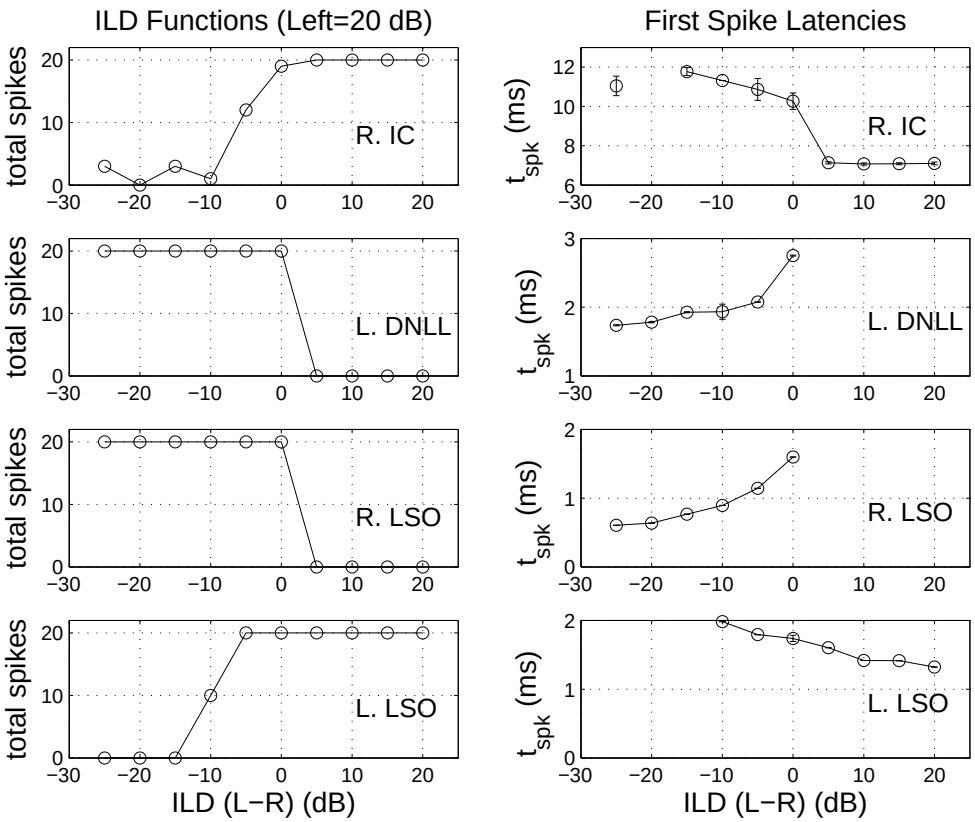


Figure 5.11: Example EI cell created *de novo*. Left: ILD functions under 20 trials. Right: Mean spike latency and standard deviation (error bar) over 20 trials. The right IC cell receives excitatory from the left AVCN and inhibitory input from left DNLL. This convergent projections resulted in the ILD function created *de novo* in the IC, as can be seen different from that of either left LSO or right LSO. Note the different time scales used in each plot of t_{spk}.

case of how the bat can transform the sigmoidal ILD curve in the LSO into delta-like (sharper) ILD tuning curve through the ILD processing network.

5.4.1 Possible EI/F Cell Connections

In biological experiments on mustache bat, excitatory intensity at the contralateral ear produced lower firing rate in IC EI/F cells than that of the conventional EI cells. A contralateral GABAergic projection from some lower monaural nucleus was accounted for this lower firing rate. When the excitatory intensity was

fixed and the ipsilateral inhibitory intensity was increased, the firing rate of the EI/F cell initially increased by at least 25%. Increasing ipsilateral inhibitory intensity further would reduce the cell's firing rate as conventional EI cell would (Park and Pollak, 1993; Park and Pollak, 1994).

Our interest is to know if sigmoidal ILD functions from conventional EI cells can be transformed into delta-like ILD tuning curves through the LSO–DNLL–IC network. As our circuit model is based on the first spike latency, we ignore the feature that contralateral input produce low spike counts found in the mustache bat experiments using long stimuli input. We focus on the most distinguishing feature of the EI/F cell: the facilitation of response during a narrow range. The real source of the facilitation has not been well established (Pollak et al., 2002), but have been thought likely from the ipsilateral DNLL (Park and Pollak, 1993; Park and Pollak, 1994; Pollak et al., 2002).

Fig. 5.12 illustrates one possible connection scheme of an EI/F cell. To explain how an EI/F cell can be formed in the IC, we use one left IC cell as an example. The left DNLL and IC cell receive excitation from the right LSO cell, and thus inherit (copy) the ILD function from the LSO. The inhibition from the left LSO to the DNLL, however, will modify the DNLL's ILD property. The DNLL cell will be inhibited when the left LSO fires a spike. Because of this, the left DNLL's ILD function will be that of the right LSO ILD function subtracted from that of left LSO. Similarly, the left IC cell can be modified by the left DNLL.

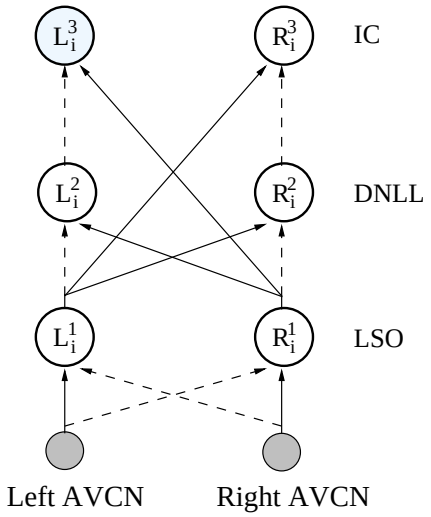


Figure 5.12: The EI/F cell network connection. In this scenario, specific left and right LSO cells are chosen to converge onto a DNLL neuron in layer 2. Their excitatory and inhibitory connections produce a shifted ILD curve that is then used to further shape the response of an IC neuron in layer 3.

5.4.2 Chip Test Example

We present one test example of our circuit model of the EI/F cell. We focus on one representative left IC cell whose network connection is shown in Fig. 5.12. Stimuli was 2 ms 40 kHz AM tone burst. In the test, the excitatory input (input to the right side) was kept constant at 20 dB, the inhibitory input (input to the left side) varied from 0 to 45 dB. The LSO were set with $V_{we} = 4.054$ V, $V_{wi} = 4.120$ V, $V_{\tau e} = V_{\tau i} = 4.172$ V. The DNLL was set with $V_{we} = 4.150 = V_{wi} = 4.150$ V, $V_{\tau e} = 4.360 = V_{\tau i} = 4.360$ V. The IC cell was set with $V_{we} = 4.170$ V, $V_{wi} = 4.089$ V, $V_{\tau e} = 4.380$ V and $V_{\tau i} = 4.330$ V. All LSO and DNLL neurons leakage were set with $V_{lk} = 0.219$ V, all IC neurons leakage were set with $V_{lk} = 0.222$ V

Fig. 5.13 shows ILD tuning curves and spike latency. In the left column, we see that the right LSO had an ILD_{ci} of -20 dB, and that the right LSO had an ILD_{ci} of 5 dB. Because of this, the left DNLL, which first inherited an ILD_{ci} of

-20 dB from the right LSO, had been modified as an ILD_{ci} of 0 dB (at which ILD value the left LSO fired and thus inhibited the left DNLL). Similarly, the left IC cell first inherited ILD function from the right LSO cell, but then modified by the left DNLL. The whole network connection scheme as shown in Fig. 5.12 resulted in an EI/F behavior, which shows the maximum response within -20 to 5 dB range.

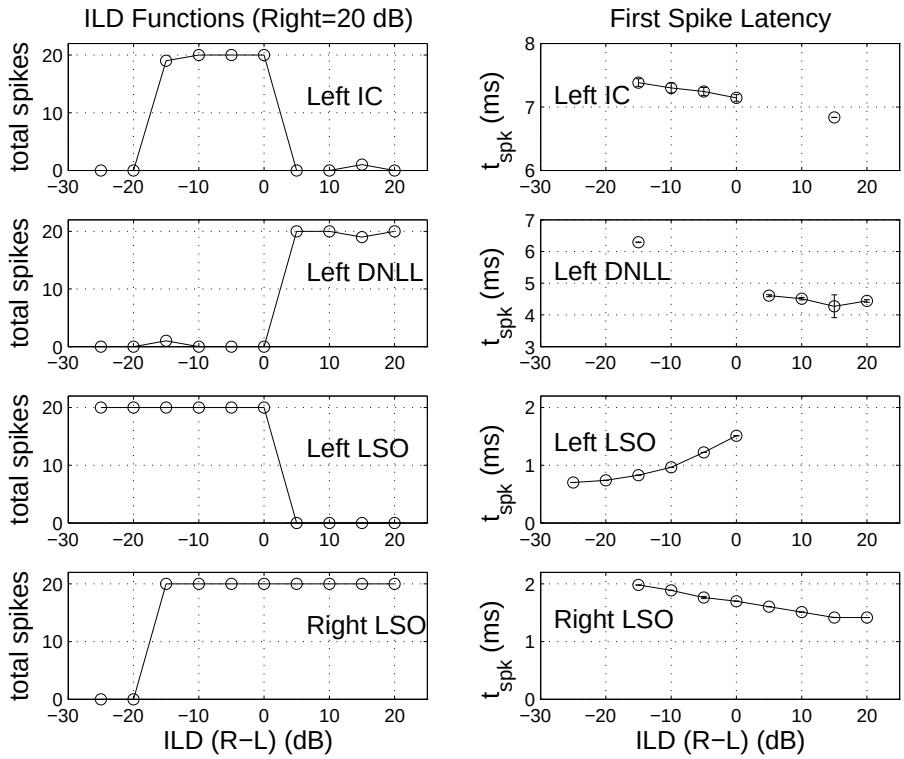


Figure 5.13: Example EI/F cell test results. The left IC neuron responded to a limited range of ILDs due to the the EI/F configuration of the network. Left: ILD functions. Right: Average spike latencies and standard deviation (error bar). 20 trials performed. Note the different time scales used in each plot of t_{spk}.

5.4.3 Real Target Test

We test our neuromorphic bat ILD system by its response to a single target and we focus on how the three layer network can transform the sigmoidal ILD

function in the LSO to the delta-like ILD function in the IC. We placed the target, a vertically-oriented cylinder with diameter of 5 cm, 90 cm in front of the sonar head. The azimuth of the target was varied from $-70°$ (left) to $70°$ (right), in steps of $5°$. For the whole experiment, 20 trials for each azimuth were performed, and each trial was separated by a 250 ms interval. The circuit parameter setup was basically the same as that described in the above EI/F single cell experiment. The LSO were set with $V_{we1} = V_{we16} = 4.047$ V, $V_{wi} = 4.115$ V, $V_{\tau e} = V_{\tau i} = 4.172$ V. The DNLL was set with $V_{we} = 4.146$ V, $V_{wi} = 4.150$ V, $V_{\tau e} = 4.368$ V, $V_{\tau i} = 4.356$ V. The IC cell was set with $V_{we} = 4.170$ V, $V_{wi} = 4.086$ V, $V_{\tau e} = 4.378$ V and $V_{\tau i} = 4.332$ V. All LSO and DNLL neurons leakage were set with $V_{lk} = 0.219$ V, all IC neurons leakage were set with $V_{lk} = 0.222$ V

We can examine the population response of all 16 right LSO cells and all 16 left IC cells by two measures. First, at each azimuth, we measured how many total spikes were generated across all 16 cells over total 20 trials. If each neuron responded at each trial, then the total spikes would be 320. The test result over this measure is shown on the top of Fig. 5.14. We see that the right LSO cell array faithfully responded to the target on the right region, and its response extended to about $20°$ of the left. The IC cell array, because of the network connection of Fig. 5.12, responded in a highly focused region, left $25°$ to right $15°$.

Second, we use a measure that at each azimuth how many neurons fired more than 50% of the time over 20 trials (that is more than ten spikes over 20 trials). This is plotted at the bottom of Fig. 5.14. We see, for example, at $-20°$, there are 9 IC cells fires that fired more than 10 spikes over 20 trials.

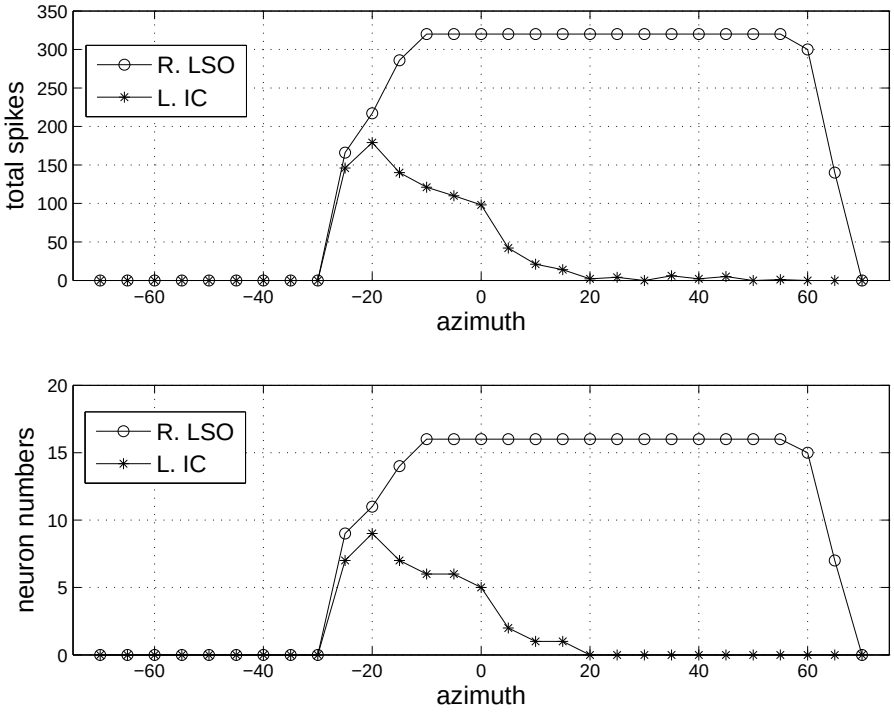


Figure 5.14: Population response of all 16 right LSO cells and 16 left IC cells. A target 90 cm away was placed at azimuth from left $-70°$ to right $70°$. The left IC cell responded only on a highly focused azimuth range. Top: Total spikes across 16 cells over 20 trials at different azimuth. Bottom: Total number of neurons responded more than half of 20 trials.

Next we examine the spike latency information among the population of the right LSO and the left IC. Fig. 5.15 show raster plots for 20 trials which the target was placed at three different azimuths. To clearly show the raster plots, these three figures are plotted within a time window from 5 to 13 ms. Outside this time window there was no spike activity.

The top panel of Fig. 5.15 is a raster plot for the case when the target was located at right $15°$. All 16 right LSO cell fired one spike per trial. Only cell 1 of the left IC fired at this location. The middle panel shows that when the target was moved to the center, all 16 right LSO cells continued to fire a spike for each trial, and 5 left IC cells fired more than 50% of the time (see Fig. 5.14). As shown in the

bottom panel, when the target was at left 20°, only 11 right LSO cells fired more than 50% of the time, but that of left IC cells increased to 9.

It is worth noting some features of spike latencies among cells in the LSO layer and the IC layer. First, for each neuron, the jitter of an LSO cell was smaller than that of an IC cell when the target was within the cell's receptive field. However, with the target moving out of the receptive field, the jitter of the LSO cell became as large as that of an IC cell. This is clearly shown by the bottom panel of Fig. 5.15. Secondly, spike latency varied among the population, even though all of the LSO cells and IC cells were set at the same parameters, respectively. While the latency among the 16 LSO cells were distributed within 1 ms range, the latency among 16 IC cells varied in a time window larger than 3 ms.

5.5 Implications for Possible Azimuth Codes

Auditory spatial representation in the mammalian brain remains a topic for debate and the search for an auditory space map in mammalian cortex has not been encouraging. In bats, perhaps the most noteworthy finding is that EI cells in the 60 kHz isofrequency contour of the mustache bat inferior colliculus code sound source azimuth in a topographical way. The 50% points in the ILD functions of EI cells across the isofrequency contour were found to change systematically (Wenstrup et al., 1986). This finding has led to a model that the border that separates the active EI cells from the silent EI cells codes the azimuth (Wenstrup et al., 1988; Pollak and Park, 1995). Alternatively, azimuth could be represented by the extent of activation

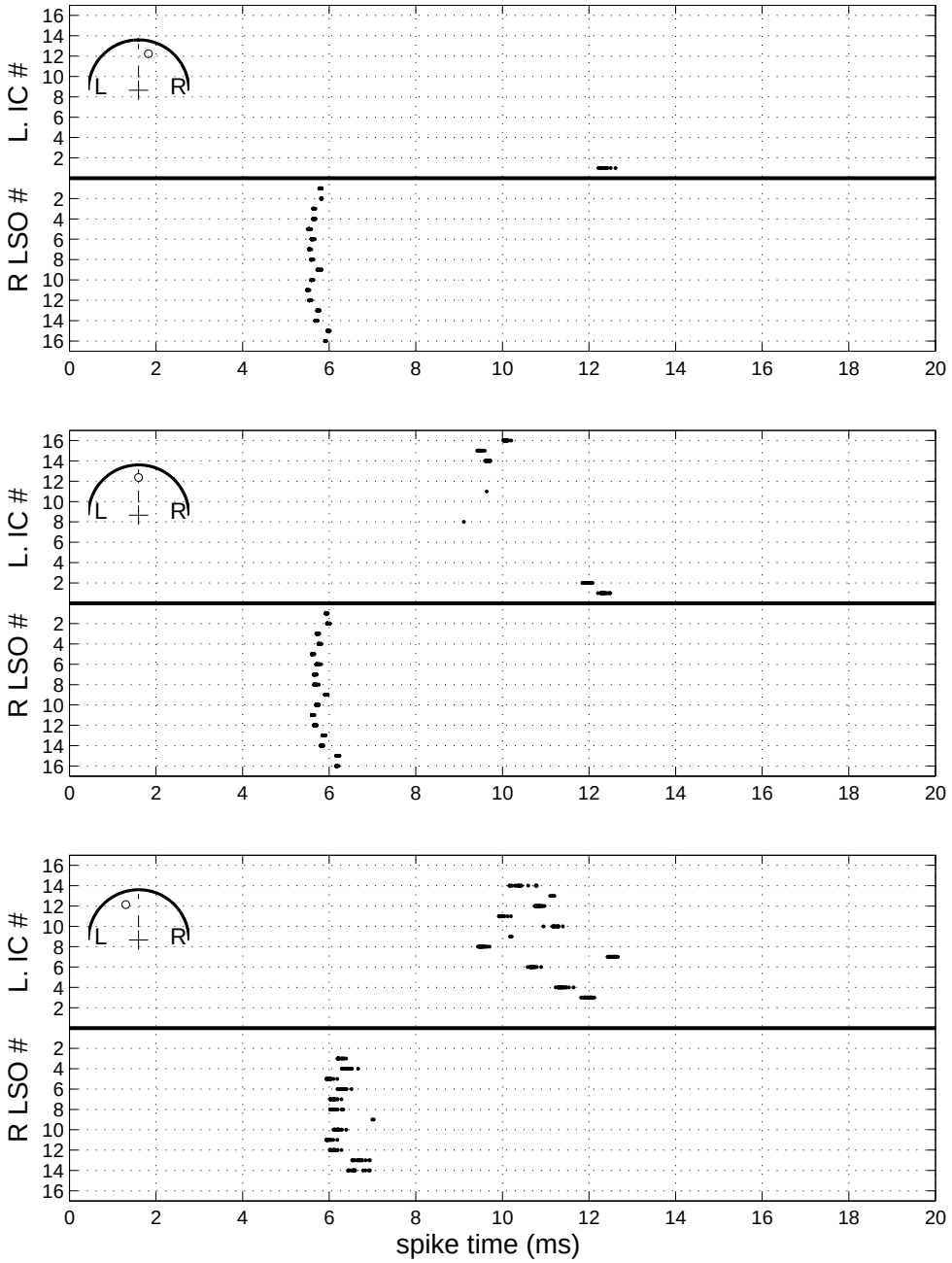


Figure 5.15: Raster plot of the LSO and IC cells for a target at three azimuths. Top: Target was 15° right to and 90 cm away from the speaker. Middle: Target was at center and 90 cm away from the speaker. Bottom: Target was 20° left to and 90 cm away from the speaker. Because all the left IC cells were configured as EI/F cells, they responded selectively to a limited azimuthal locations and showed maximum response to the target at the left 20°. 20 trials performed. The inset on the left upper corner in each panel shows the relative location(s) of the target(s).

of the EI cell population (Irvine, 1992).

However, such a topographical coding of azimuth has not been found in either the LSO or the inferior colliculus of the FM bat *Eptesicus fuscus* (Covey et al., 1991; Grothe et al., 1996). Considering that spatial receptive field properties of IC cells are correlated with many parameters, such as sound pressure level, frequency spectrum, pinnae movements, modulation pattern and movement of the sound source, we may expect that it is unlikely that unambiguous information about the sound location is coded by individual IC neurons.

Our circuit model of ILD processing in bats suggests that a distributed population response of EI cells represented by the first spike latencies could code for the azimuth. A distribution o f first spike latencies are first formed in both the left LSO and the right LSO. The first spike latencies of the LSO EI cells are then transformed through the network connections among the LSO, DNLL and IC. It is conceivable that the latency distribution created in the IC are further transformed by ascending stages and form another distribution of latencies in neurons in the superior colliculus or cortex. There are some general trends for the population response as we have revealed in this chapter and in Chapter 4. These general trends include: 1) the population of firing neurons increases, 2) the spike latencies shorten with increasing input sound stimuli level, and 3) as sound stimuli level at one ear increases, the number of active EI neurons increases on one side of the brain but decreases on the other side.

Recent studies on AI neurons in cat supports the idea that a distribution of

first spike latencies among neurons can code for azimuth. A study using virtual space receptive field (VSRF) techniques concluded that a substantial proportion of recorded AI cells in cats exhibited a gradient of first spike latency within the VSRF, with the shortest latencies found in the core of the VSRF and longer latencies more distant from the core (Brugge et al., 1996). In another study on cat AI neurons, relative latencies referenced to population minima was found to allow a sound stimuli level tolerant representation of azimuth (Eggermont, 1998).

5.6 Discussion

By illustrating how EI properties in the IC can be formed through different circuitry and network connections, we have completed our model description. We have shown that by selecting a subset of the connections in our neuromorphic VLSI circuit model of bat ILD processing in the LSO, DNLL and IC, different neuron response types described in the literature can be created. We have modeled EI cells in the DNLL or IC to inherit the EI properties established at the LSO by way of a single excitatory synapse receiving a single spike. We have modeled EI properties that are modified at the IC by way of a single inhibitory spike, with its arrival time to determine the modification on the EI properties. By using only single synapse each for excitation and inhibition we could reduce chip design complexity and focus our study on various combinations of connection among layers.

The circuitry that links the LSO, DNLL and IC provides us a good model for studying neural networks. We can now review our modeling work in terms

of neural networks. Our study had been focused on a layered network of spiking neurons (spiking neuron network). The input layer (layer 0) has been simplified as two nodes: one for left AVCN population input, the other for the right AVCN population input. The output layer (layer 3) has been modeled as 32 nodes, with 16 nodes for the left IC neurons, another 16 nodes for the right IC neurons. The LSO and DNLL can be considered as the "hidden layer", consist of 32 nodes for each layer. Where in some neural network literature, the term "feedfoward network" has been loosely used, the feedforward neural network actually refers to a network in which the only interconnections are from a layer to its immediately ascending layer (e.g. Mehrotra et al., 2000). In the network we are studying, connections between layers are not restricted from one to its immediately ascending layer. For example, there exist connections from layer 1 to layer 3, as well as layer 0 to layer 3. There are also inner layer connections, such as the cross-inhibition between two opposite DNLL nodes (layer 2) and two IC nodes (layer 3). Therefore, the architecture of the four layer neural network we are studying is a recurrent neural network. We have thus identified a four layer recurrent spiking neuron network that can be a good case study for the neural network research community.

We have illustrated how ILD information can be processed and transformed by a network of spiking neurons. Spiking neuron networks (SNN) represents a new class of computational models and can exhibit computationally more powerful than traditional neural networks of comparable size (Maass, 1997; Maass, 1999). A question specifically associated with the network in our study (but is of interest to theoretical neural network research in general) is: for given analog binaural inputs (the

sound pressure level differences between two ears), how can a population of spiking neurons react to represent, process, and transform the information about stimuli through such a network? In Chapter 3, we have demonstrated that in layer 1, the LSO layer, the first spike latency carries the information about the analog stimuli inputs in a continuous function. The ILD of complete inhibition defines the minimum ILDs that cause a neuron to be silent. In this chapter, we have shown that a network of such cells can copy EI property onto ascending stages (copy cell), can right shift the ILD functions established in the LSO, can convert the sigmoidal ILD functions into delta like ILD functions (EI/F cell). In next chapter, we will demonstrate that the cross-inhibition due to the inner layer connection in the DNLL will play an important role in ILD processing of multiple echoes.

Our model study suggests that one function of the copy cell is to produce necessary spike latency. If the only measure used for characterizing EI properties is the ILD of complete inhibition, as is often assumed in neurophysiological experiments, it would be natural to ask why a large population of EI cells in the IC simply inherit their EI properties from the LSO. When we work on both ILD_{ci} and spike latency, we can easily understand that a copy cell not only copies the ILD_{ci} from LSO, but it also transforms the spike latency needed for further ILD processing. In this sense, this type of cell can be called a "relay cell". Such latency transformation is necessary for at least two reasons. First, neurons exhibit larger average spike latencies as their location getting higher along the ascending pathways. An inhibitory spike coming too late or too soon will have no effect. That is, spike inputs react each other in some time window. Second, because the time difference between excitation

and inhibition can modify the EI properties, the spike latency modulated by the synaptic process of a copy cell may play an important role.

Our model study supports some hypotheses about interconnections among ILD pathways proposed by biological research community. Specifically, our model study on the modified cell supports the hypothesis that the contralateral DNLL can modify an IC cell's EI properties, and the effect of this modification is to shift the IC cell's ILD of complete inhibition to a more positive ILD value. Our model study on the *de novo* cell supports the hypothesis that EI properties can be created anew by way of a contralateral excitatory input from a lower monaural nucleus and an ipsilateral inhibitory input from contralateral DNLL. Our model study on the EI/F cell supports the hypothesis that the ipsilateral DNLL input can produce the facilitation response. In addition, our model study on the EI/F cell suggests that if short stimuli are used, EI/F cells can be formed by way of a cross excitatory input from LSO and an inhibitory input from the ipsilateral DNLL.

Chapter 6

ILD Processing of Multiple Echoes

Bats navigate and capture prey in naturally cluttered environments. To what level of detail and accuracy do echolocating bats perceive cluttered environments remains a challenging question to answer for the whole bat research community. In this chapter we extend our earlier study of ILD processing of a single target in previous chapters to multiple targets. We first study the effect of multiple objects presented on the same side of the midline of the bat, where we will point out how the neuron's refractory period and subthreshold summation must be considered. We then study the effects of multiple objects on opposite sides of the midline of the bat, where we show the role of the long-lasting cross-inhibition of the DNLL.

6.1 Effects of Refractory Period and Leakage Current

In previous chapters, we have studied EI cells in LSO, DNLL and IC using a VLSI integrate-and-fire model. The VLSI integrate-and-fire model, as described in Chapter 3, consists of three functional components: a subthreshold process of integration of input current on a membrane capacitance C_m with a constant leakage current I_{lk}, a threshold process for generating a voltage spike, and a process for reset

and refractory period. Our ILD model is based on first spike latency. To prevent interactions between two consecutive trials, we have chosen a large time interval between trials (250 ms or 4 Hz), as is the common practice in biological experiments reported in literature (e.g. Park (1998)). Under this scheme the reset and refractory period of the neuron prevent the neuron from firing more than one spike for each target. Because of the large time interval between two trials, the leakage current of the neuron will discharge the membrane capacitance down to its resting potential before the next stimuli.

In this section, we will show that when multiple targets are considered, the subthreshold process and the refractory period of the neuron will have a significant effect on a bat's ILD processing, even with the same large inter-stimulus interval.

6.1.1 Conceptual Illustration of the Hypothesis

In this subsection, we illustrate what will happen when multiple objects exist on the same side of the bat. As the speed of sound is about 340 m/sec, a distance of 17 cm between two targets will result in an echo time difference of 1 ms as perceived by the bat. As shown in Fig. 6.1, target #2 is close to target #1 on the same side, target #3 is far from target #1. We propose three hypotheses:

1. A closer target (as target #1) that stimulate some EI cells to fire will prevent those same EI cells from responding to a farther target on the same side (e.g. target #2), if the two targets are within or around a range difference corresponding to the travel distance of sound during the refractory period.

2. Because of the subthreshold summation of membrane voltage, the existence of target #2 may cause some EI cells to fire that would not fire if target #1 were presented alone.

3. The more that the two targets are separated (as target #3 related to target #1), the less significant the above two effects will be.

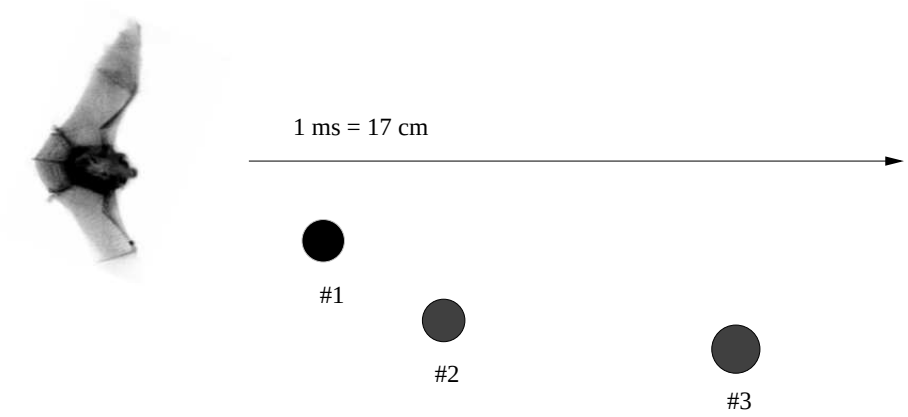


Figure 6.1: Multiple targets on the same side of the midline of the bat. Three objects are on the same side of the bat. Object #2 is close to object #1, object #3 is far from object #1. The hypotheses predict that the EI cells' responses to object #2 will be affected due to their refractory periods and subthreshold summation processes. Responses to object #3 will be affected less due to the larger separation from object #1.

6.1.2 LSO Population Response to Multiple Objects

We first show a typical LSO population response to one object and then to two objects that are only 20 cm apart. For experiments in this section, we used two vertical cylinders with the same diameter of 5cm as targets. We performed five trials for each condition, using a large inter-trial interval of 250 ms (4 Hz) to avoid any interactions between trials. LSO cells were set with $V_{we1} = 4.060$ V, $V_{we16} = 4.100$

V, $V_{wi} = 4.080$ V, $V_{\tau e} = V_{\tau i} = 4.170$ V. The leakage parameter for all neurons was set to $V_{lk} = 0.220$ V. We set the refractory period for all the neurons to be about 1 ms by setting $V_{rfr} = 0.350$ V. We do not have refractory period information for the LSO. The refractory period of 1 ms has been used by Llano and Feng (2000) for a computational model study of the thalamus of little brown bat (*Myotis lucifugus*).

The experiment results are shown in Fig. 6.2. The top panel shows the population response to object #1 alone, that was located 30° right of center and 80 cm away. Since the object was located to the right, cells 1-12 of the right LSO cells fired in all five trials. The middle panel shows the response when object #2 alone was located 40° right of center, 100 cm away. In this case, all the twelve cells still fired except for cell 9.

The bottom panel shows results for two objects presented simultaneously. We observe that because object #2 was further away than object #1, it did not change the system's response to the first object in any significant sense. Object #1, however, did affect the response to the right LSO to object #2 in at least two significant ways. First, cells 1-8 and 10-12, which fired when object #2 was presented alone, no longer fire. We point out that these missing spikes are a result of the refractory period of the neurons. Second, cell 13 and 14 of the right LSO, which did not fire when object #1 or object #2 was presented alone, were now activated. This is due to residual (but decaying) membrane charge remaining from the inputs during the response to the first object.

We performed another experiment by separating the two objects by a larger distance: 70 cm apart. The results are shown in Fig. 6.3. The top panel of Fig. 6.3

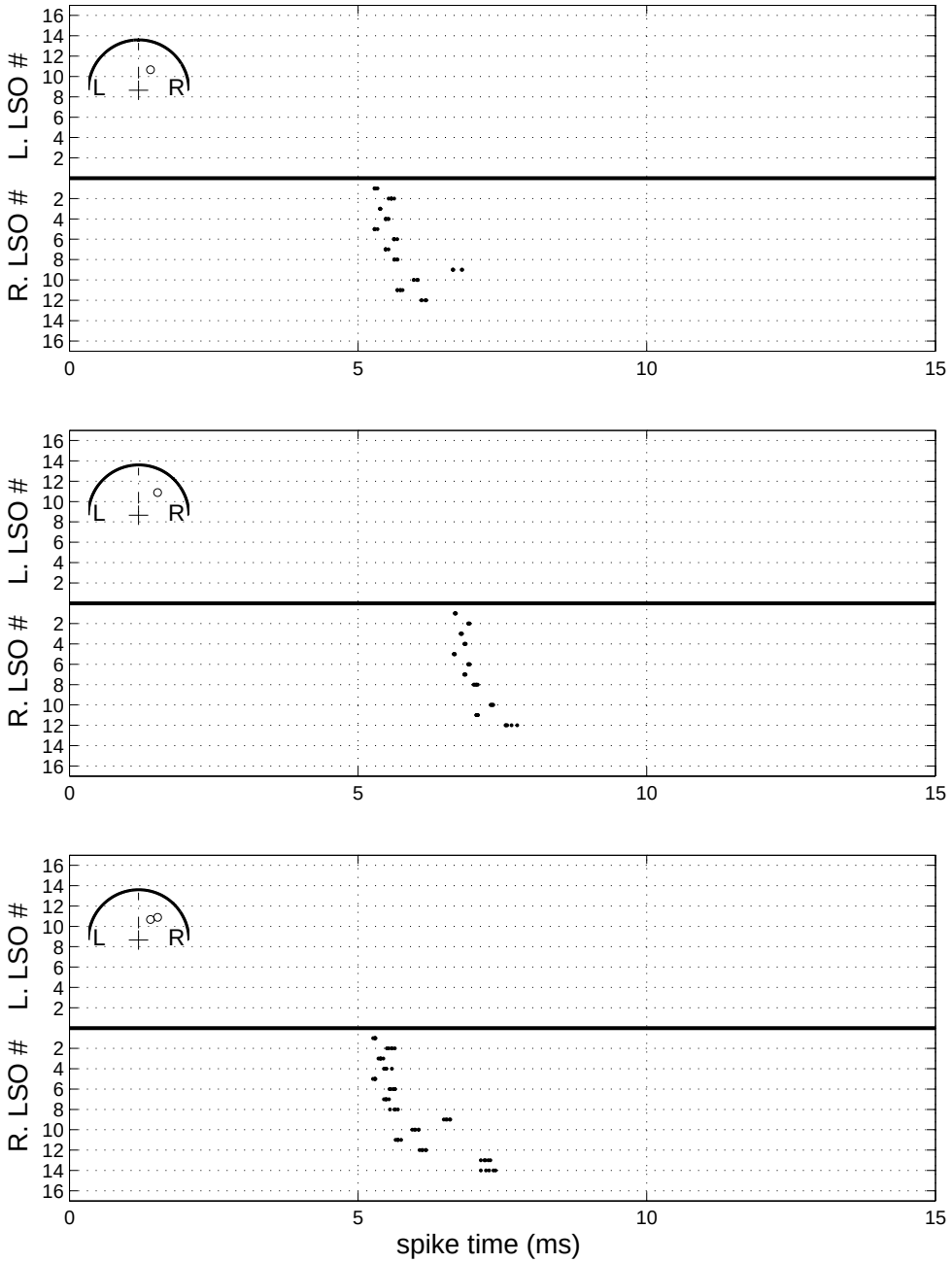


Figure 6.2: LSO population response to two objects that were close to each other. Top: Object #1 alone was located at 30° right of the midline and 80 cm away from the speaker. Middle: Object #2 alone was located at 40° right of the midline and 100 cm away from the speaker. Bottom: Object #1 and object #2 were both present. Objects were vertical cylinders with a diameter of about 5 cm. Shown are raster plots with 5 trials. The inset on the left upper corner in each panel shows the relative location(s) of the target(s).

shows the population response when object #1 alone was located 30° right of center, 80 cm away. The middle panel shows the response when object #2 was located 40° right of center, 150 cm away. Because of the larger distance from the speaker, cell 9, 10, and 12 did not fire in comparison with the top panel.

The bottom panel shows the response when the two objects were presented simultaneously. As we can predict, the right LSO EI cells' response to object #2 were much less affected by the refractory period compared with Fig. 6.2. This is true because the cells that fired when object #2 was alone still fired when both objects were presented. As for the subthreshold summation, we see that cell 13 and 14 of the right LSO, which did not fire when object #1 or object #2 was presented alone, were now activated.

There are two unexpected results from this experiment. The first is that cell 11 that fired when object #2 was alone (middle panel) no longer fired when both objects were presented. There are two possible explanations for this. First, the late spike timing of cell 11 as shown in the middle panel indicates that the cell barely reached the threshold. Second, even though we set all the neurons' refractory period control parameter the same, the mismatch among the transistors would cause the refractory period of each neuron circuit to be slightly different.

The second unexpected result is that cell 16 fired when both objects were presented (bottom panel). This is in contrast to Fig. 6.2. While in general we would expect that the subthreshold summation effect decreases as the distance between two objects increases, in reality there are other second-order factors that may affect the neuron's response. Among many possible factors, we point out that multi-path

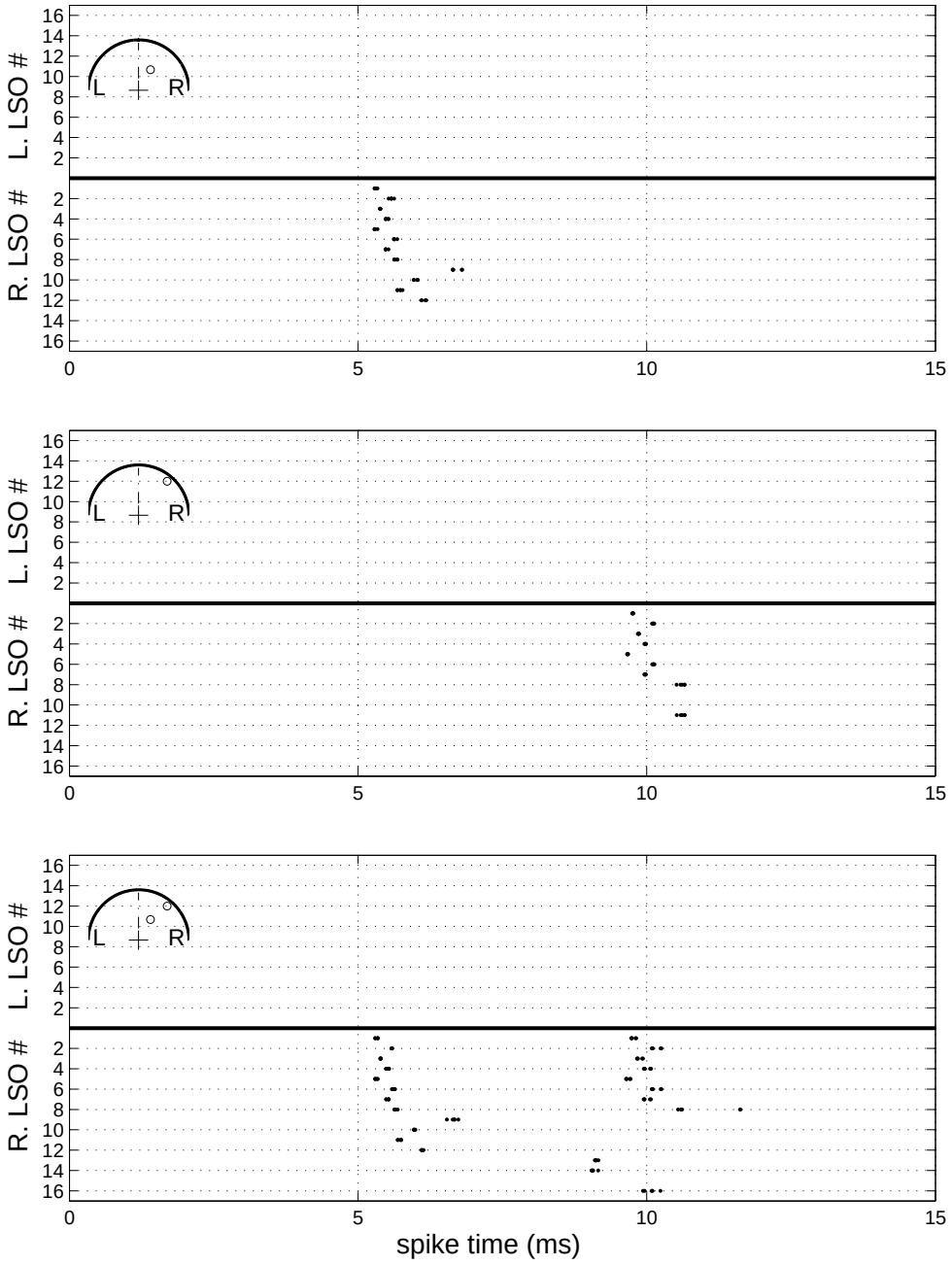


Figure 6.3: LSO population response to two objects that were far apart. Top: Object #1 alone was located at 30° right of the midline and 80 cm away from the speaker. Middle: Object #2 alone was located at 40° right of the midline and 150 cm away from the speaker. Bottom: Object #1 and object #2 were both present. Objects were vertical cylinders with diameter of about 5 cm. Shown are raster plots with 5 trials. The inset on the left upper corner in each panel shows the relative location(s) of the target(s).

echoes that bounce off of the targets themselves and background noise are additional sources of input.

The unexpected results in the bottom panel is unlikely to be due to the precision of object placement during the two experiments. In fact, objects were placed in the following order:

1. Place object #2 at 40° right to and 100 cm away from the speaker (results: middle panel of Fig. 6.2).

2. Place object #1 at 30° right to and 80 cm away from the speaker (results: bottom panel of Fig. 6.2).

3. Remove object #2 (results: top panels of Fig. 6.2 and Fig. 6.3).

4. Place object #2 at 40° right to and 150 cm away from the speaker (results: bottom panel of Fig. 6.3).

5. Remove object #1 (results: middle panel of Fig. 6.3).

6.2 DNLL Long-lasting Cross-inhibition

6.2.1 Long-lasting Cross-inhibition is a Key Feature of the DNLL

As we have reviewed in Chapter 2, the DNLL is distinguished from the LSO by at least two features. First, the DNLL is dominated by GABAergic neurons, such that projections from the DNLL are mainly inhibitory. Second, unlike LSO,

the DNLL on each side of the midline projects inhibition reciprocally (via the commissure of Probst).

Biological studies in mustache bats (Yang and Pollak, 1994; Yang and Pollak, 1998) as well as in Mexican free-tailed bats (Burger and Pollak, 2001) have shown that inhibition in the DNLL, evoked by stimulation of the ear ipsilateral to it is long-lasting; the inhibition often lasts for many milliseconds after the end of the signal that evoked it. Persistent inhibition in the DNLL can be evoked either by tone bursts or by brief FM sweeps, provided the FM signal sweeps through the best frequency of the DNLL cells. In one study of Mexican free-tailed bats, the average persistent inhibition evoked by 2 ms FM signals, measured in 21 DNLL neurons, was 13 ms and ranged from 4 to 38 ms. In 8 of the 21 neurons, persistent inhibition evoked by both 2 ms tone bursts and 2 ms FM sweeps were measured. Tone bursts usually caused a slightly longer inhibition than did FM sweeps. In these eight neurons, the average FM-evoked inhibitory persistence was 12 ms, whereas the average tone-evoked inhibitory persistence was 17 ms (Burger and Pollak, 2001).

This long-lasting cross-inhibition indicates that the DNLL must play an important role in the ILD processing of multiple sounds. Fig. 6.4 illustrates how long-lasting cross-inhibition in the DNLL may affect a bat's response to multiple objects on both sides of the midline. In our example, a near object (object #1) is located on the left side of the bat. This object will excite the left LSO cell (L_i^1) which excites the right DNLL cell (R_i^2). Because the cross-inhibition that the left DNLL cell (L_i^2) receives from the right DNLL can persist many milliseconds, the left DNLL cell cannot be excited by the further object (object #2) that would nor-

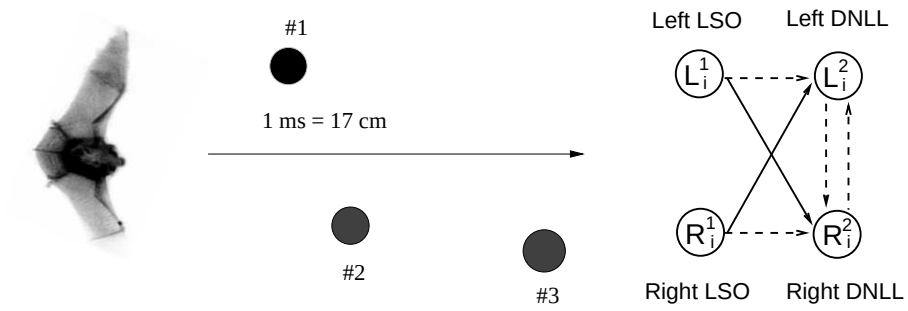


Figure 6.4: Multiple targets on two sides of the bat. A near object (object #1) is located on the left side of the bat. The long-lasting cross inhibition in DNLL will affect the DNLL EI cells' responses to further objects located on the right side. Object #3 will be less affected because of the large distance from object #1. The LSO-DNLL interconnection is also shown. A DNLL cell, e.g. L_i^2 (i=1, .., m), receives excitation from the contralateral LSO (R_i^1), inhibition from the ipsilateral LSO (L_i^1), and the cross inhibition from the opposite DNLL, R_i^2 . Solid line for excitation, dotted line for inhibition.

mally excite the cell if it was presented alone. The duration of inhibition is clearly a function of the time constant of the inhibitory synapse and the recovery time of the neuron. Note that the influence of previous inputs is not limited to simply preventing cells from firing or not, it also changes the initial conditions of cells that respond to subsequent echoes.

In spite of the importance of the DNLL in auditory processing, there are only a few detailed biological models that include the DNLL, owing perhaps to the lack of neurophysiological data from the DNLL. We will demonstrate, with our neuromorphic bat ILD processing system, how the DNLL responds differentially to spatially-separated sound sources depending upon their order of arrival.

6.2.2 DNLL Population Responses to Multiple Objects

As in Section 6.1.2, we chose two vertical cylinders with the same diameter of 5 cm for this set of experiments. We performed five trials for each condition, using a large inter-trial interval of 250 ms (4 Hz) to avoid any interactions between trials. The LSO cell was set with $V_{we1} = 4.029$ V, $V_{we16} = 4.045$ V, $V_{wi} = 4.041$ V, $V_{\tau e} = V_{\tau i} = 4.170$ V. The DNLL cell was set with $V_{we} = 4.140$ V, $V_{wi1} = 4.147$ V and $V_{\tau i1} = 4.170$ V for the ipsilateral LSO input, $V_{wi2} = 4.085$ V and $V_{\tau i2} = 4.362$ V for the opposite DNLL input. Both LSO and DNLL neuron leak current parameter and refractory period were set with $V_{lk} = 0.220$ V, $V_{rfr} = 0.350$ V, respectively.

We first show a typical LSO and DNLL population response to one object and then to two objects that are 80 cm apart. In this experimental design, a preceding sound was obtained by putting an object 45° left of center and 80 cm away, while the trailing sound was created by an object at 40° right of center and 160 cm from the speaker.

Fig. 6.5 shows the raster plots for five trials of the above experiment. In this plot it is easy to see the temporal relationship between the LSO and DNLL. The top panel in Fig. 6.5 shows the response to the near object (preceding sound) alone. As the object is located to the left side and is close to the sonar head, all LSO cells except cell 9 fired one spike for each trial. These left LSO cells projected excitation across the midline to the right DNLL cell and caused the right DNLL cells to fire one spike per trial.

The middle panel shows the response to the further object (trailing sound

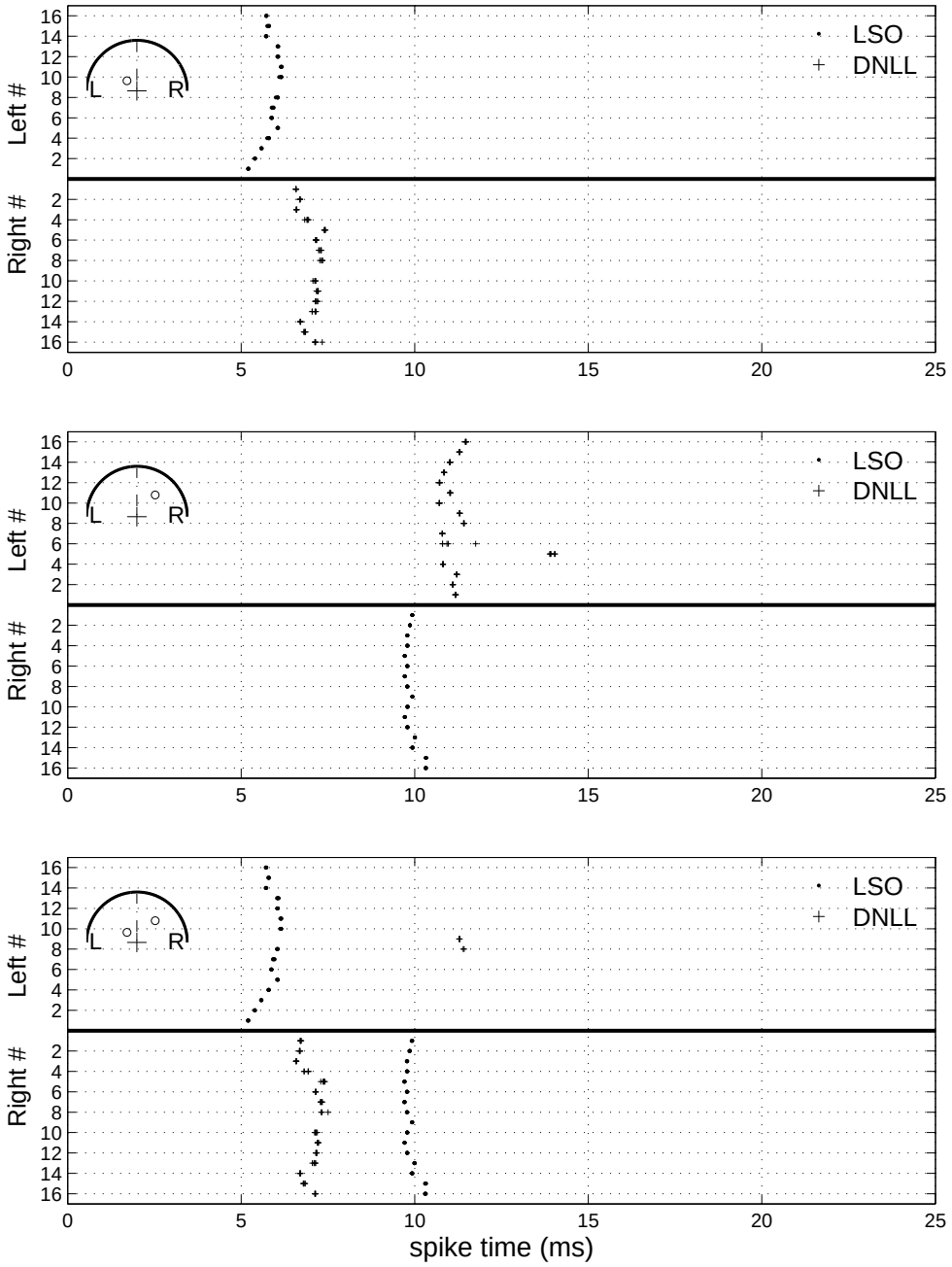


Figure 6.5: DNLL response to two objects that were close to each other. Top: Object #1 alone was located at left (45°) and 80 cm away from the speaker. The left LSO cell fired and in turn excited the right DNLL. Middle: Object #2 alone was located at right (40°) and 160 cm away from the speaker, it excited the the right LSO cells and in turn drove the left DNLL cells to fire. Bottom: When both objects were present, most of the left DNLL cells were inhibited from the opposite DNLL cells (right DNLL). Shown are raster plots with 5 trials. The inset on the left upper corner in each panel shows the relative location(s) of the target(s).

alone). As the object was located to the right side, all right LSO cells fired one spike for each trial. These right LSO cells projected excitation across the midline to the left DNLL cell and caused the left DNLL cells to fire one spike per trial.

The bottom panel shows the results when we presented the two objects simultaneously. The left DNLL cells, whose excitation come from the right LSO, were mostly inhibited by the opposite DNLL. The left DNLL cell #9 fired faithfully 5 times during 5 trials because there was no cross inhibition from the right DNLL cell #9 (see top panel). By checking the individual data points, we know that left DNLL cell #8 fired 2 times during 5 trials. We also know that the right DNLL cell #8 fired only 4 times during 5 trials. For the two spikes of the left DNLL cell #8, one was due to the missing spike of the right DNLL cell #8 (so that there was no cross inhibition).

In our second experimental design, we placed object #2 40° to the left of the midline and 250 cm away from the speaker. The object #1 was the same as in the first experiment. The distance between the two objects was 170 cm, corresponding to a 10 ms echo time difference.

Fig. 6.6 shows the raster plots for five trials of the second experiment. From the middle panel that shows the response to the further object (trailing sound alone), we see that most right LSO cells (cells 1-14) fired. Again, these right LSO cells projected excitation across the midline to the left DNLL and cause the left DNLL cells to fire.

In the multiple target case (bottom panel), most of the left DNLL cells that fired previously when the trailing sound was presented alone fired again. Only left

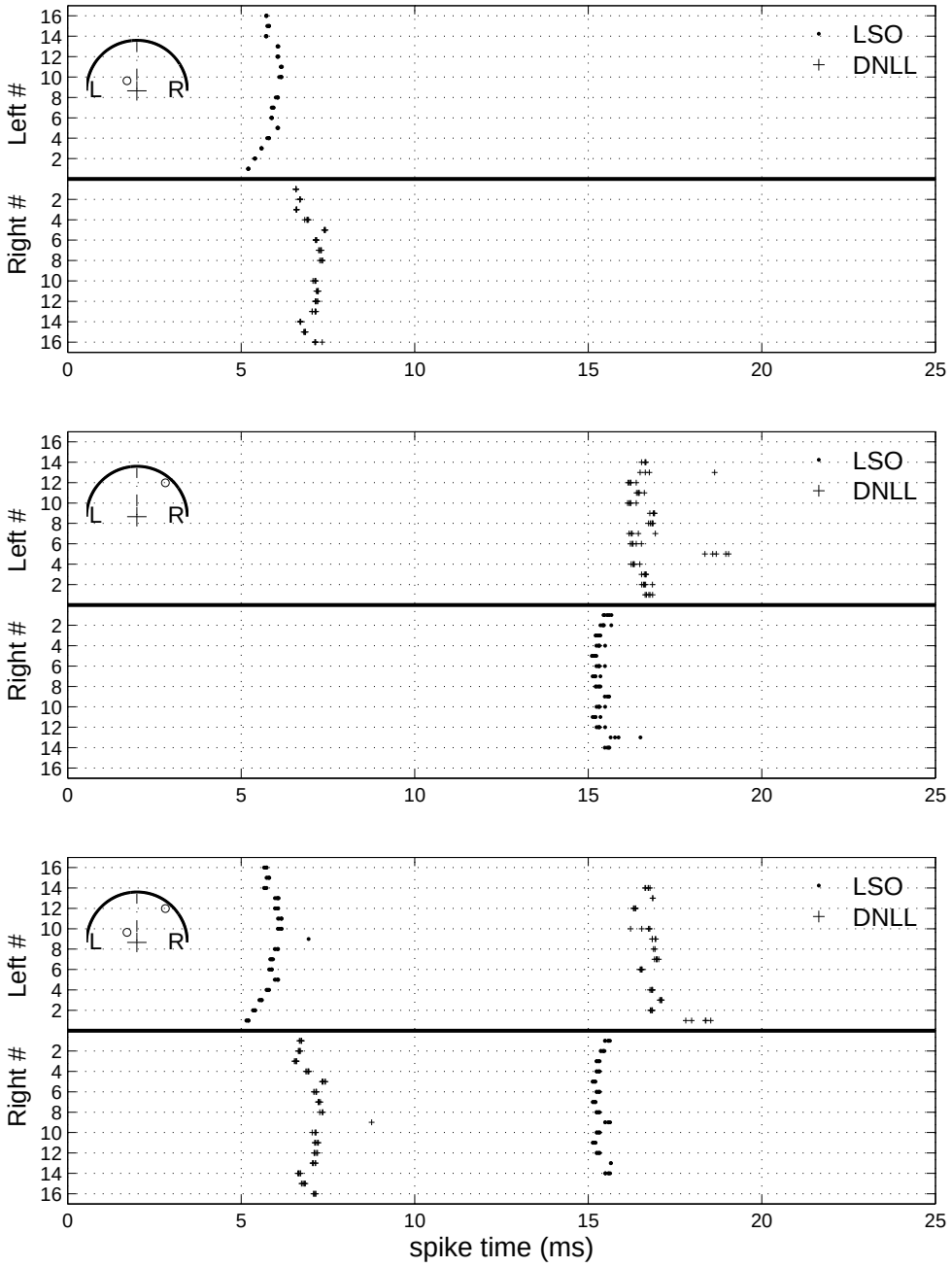


Figure 6.6: DNLL response to two objects that were far apart. Top: Object #1 alone was located at left (45°) and 80 cm away from the speaker. The left LSO cell fired and in turn excited the right DNLL. Middle: Object #2 alone was located at right (40°) and 250 cm away from the speaker; it excited the right LSO cells and in turn drove the left DNLL cells to fire. Bottom: When both objects were present, most of the left DNLL cells still fired due to the large distance between two objects. Shown are raster plots with 5 trials. The inset on the left upper corner in each panel shows the relative location(s) of the target(s).

DNLL cells #5 and #11 were silent to the second object due to the still activated cross inhibition from the opposite DNLL.

6.3 Impact of DNLL's Long-lasting Inhibition on the Inferior Colliculus

6.3.1 Auditory Pathways to Inferior Colliculus Cells

As we stated in Chapter 2 and Chapter 5, EI cells in the inferior colliculus (IC) can be formed in various ways. One particularly relevant type of cell is one in which the EI property is formed *de novo* in the IC. For this type of EI cell, stimulation of the ear contralateral to the IC drives a lower monaural nucleus, assumed here to be the cochlear nucleus, which provides the excitation to the IC. Stimulation of the ear ipsilateral to the IC excites the contralateral DNLL, which then provides the inhibition that suppresses the contralaterally evoked excitation in the IC.

Fig. 6.7 shows the specific network connection of such an IC cell. This network connection is based on the hypothesis about the impact of the DNLL's long-lasting inhibition on the IC proposed by Burger and Pollak (2001). In the following discussion, we will focus on an IC cell on the right side. The IC cell receives its excitation from the contralateral ear, represented by left AVCN input. The inhibitory input to the IC is from the contralateral DNLL which is excited from the stimulation of the ipsilateral ear through the left LSO. This inhibitory input to IC from the DNLL cell, L_i^2, can be inactivated by the cross-inhibition from the opposite DNLL cell, R_i^2, that is stimulated by a preceding contralateral sound.

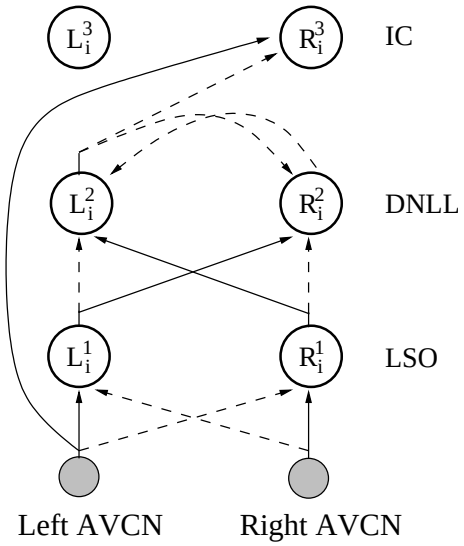


Figure 6.7: Network connection of IC EI cells that are affected by DNLL's long-lasting cross inhibition. Shown is an representative IC cell on the right side. The IC cell receives its excitation from contralateral ear, represented by left AVCN input. The inhibitory input to the IC is from the contralateral DNLL which is excited from the stimulation of the ipsilateral ear through the left LSO. This inhibitory input to IC from the DNLL L_i^2, can be can be inactivated by the cross-inhibition from the DNLL R_i^2 that is stimulated by a preceding contralateral object. Solid line for excitation, dotted line for inhibition.

6.3.2 Experiment Design and Results

To illustrate the DNLL's long-lasting cross-inhibition on the IC EI cell's response to multiple targets, we focus on a single IC EI cell with its network connection shown in Fig. 6.7. Specifically, we work with a single *right* IC EI cell. As in Section 6.1.2, we chose two vertical cylinders with the same diameter of 5 cm. We performed five trials for each condition, using a large inter-trial interval of 250 ms (4 Hz) to avoid any interactions between trials.

We performed two experiments. In the first experiment, the two targets were close enough to each other in range such that the long-lasting cross-inhibition of the DNLL was still active. In the second experiment, by placing the second object

further away from the first object, the long-lasting cross-inhibition of the DNLL was weak if not zero. In both the experiments, the circuit parameters were set as follows. The LSO cell was set with $V_{we} = 4.030$ V, $V_{wi} = 4.080$ V, $V_{\tau e} = 4.174$ V $V_{\tau i} = 4.172$ V. The DNLL cell was set with $V_{we} = 4.140$ V, $V_{wi1} = 4.147$ V and $V_{\tau i1} = 4.170$ V for ipsilateral LSO input, $V_{wi2} = 4.093$ V and $V_{\tau i2} = 4.362$ V for for opposite DNLL input. Both the LSO and DNLL neuron leak current parameter was set with $V_{lk} = 0.220$ V. Both the LSO and DNLL refractory period parameter was set with $V_{rfr} = 0.348$ V. The IC cell was set with $V_{we} = 4.176$ V, $V_{wi} = 4.130$ V, $V_{\tau e} = 4.435$ V, $V_{\tau i} = 4.457$ V. The IC neuron leak current and refractory period were set as $V_{lk} = 0.220$ V, $V_{rfr} = 0.348$ V, respectively.

Fig. 6.8 shows the raster plots for five trials of the experiment when two targets were 120 cm apart. In this plot it is easy to see the temporal relationship between the LSO, DNLL and IC. The top panel in Fig. 6.8 shows the response to the near object (preceding sound) alone, which was located 45° to the left and 80 cm away from the speaker. As the object is located at the left side and is close to the sonar head, the left LSO cell consistently fired one spike for each trial. The left LSO cell projected excitation across the midline to the right DNLL cell and caused the right DNLL cell to fire a spike per trial. This left object also caused the right IC cell to fire.

The middle panel shows the response to object #2 alone that was located 15° to the right and 200 cm away from the speaker. As the object was located on the right side, the right LSO cell fired one spike for each trial. The right LSO cell projected excitation across the midline to the left DNLL cell and caused the

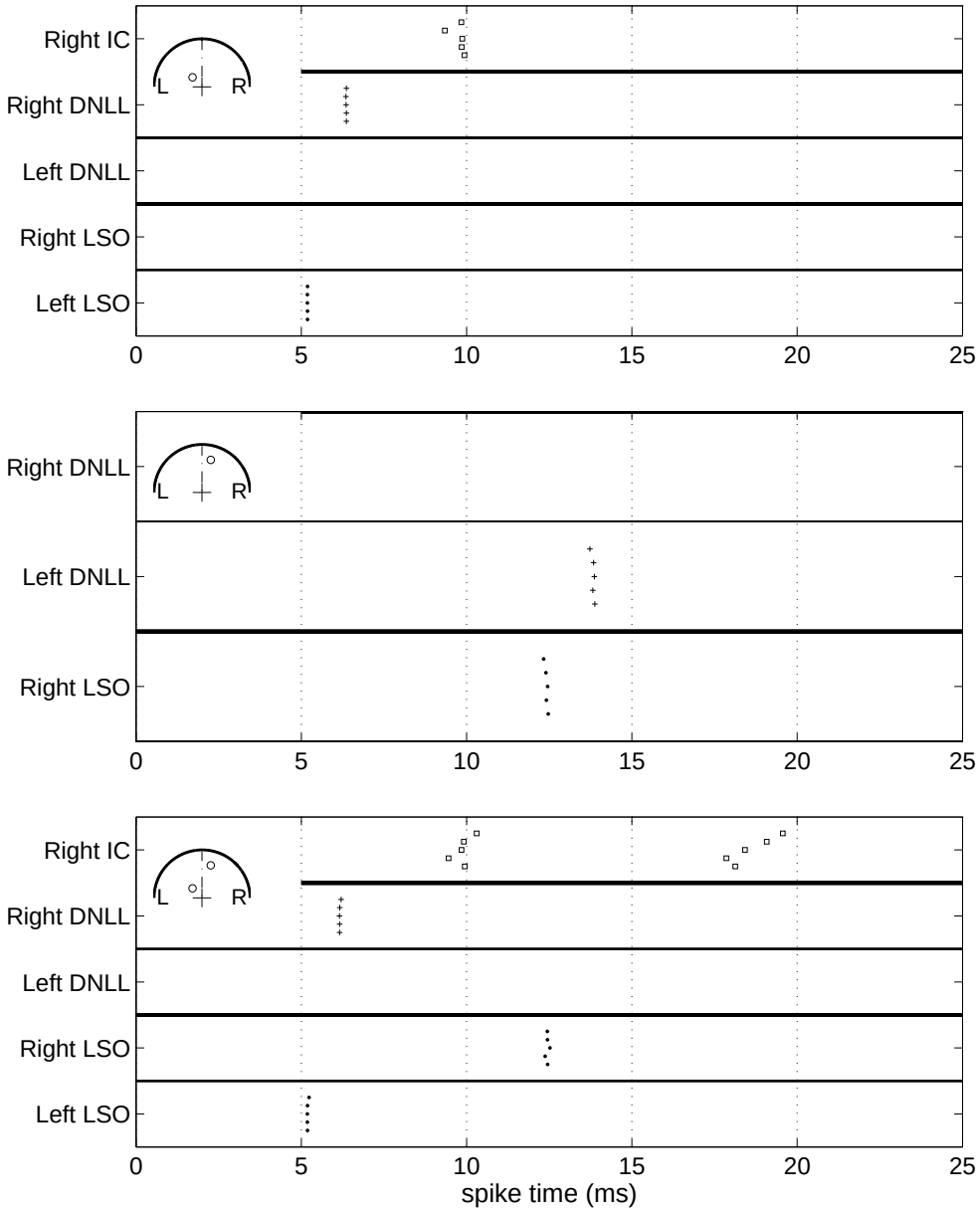


Figure 6.8: IC response to two objects that were 120 cm apart. Top: Object #1 alone was located at left (45°) and 80 cm away from the speaker. The left LSO cell fired and in turn excited the right DNLL. Middle: Object #2 alone was located at right (15°) and 200 cm away from the speaker; it excited the right LSO cell and in turn drove the left DNLL cell to fire. Bottom: When both objects presented, the left DNLL cell was inhibited from the opposite DNLL cell (right DNLL). This disinhibition of DNLL allows the right IC cell to respond to object #2. Shown are raster plots with 5 trials. The inset on the left upper corner in each panel shows the relative location(s) of the target(s).

left DNLL cell to fire a spike per trial. Because the right IC cell was configured to receive inhibitory input from the left DNLL cell, it was inhibited and did not fire in response to object #2.

The bottom panel shows the results when we presented the two objects simultaneously. The left DNLL cell that fired in response to object #2 alone, was now silent due to the cross-inhibition from the opposite DNLL cell. The right IC cell, deprived of inhibition from the left DNLL, effectively acted as a monaural cell and fired 5 times during the 5 trials.

Fig. 6.9 shows the raster plots for five trials of the experiment when the two targets were 170 cm apart. The top panel in Fig. 6.9 shows the response to the near object (preceding sound) alone that was located 45° to the left and 80 cm away from the speaker. The results have been explained above.

The middle panel shows the response to object #2 alone that was located 15° to the right and 250 cm away from the speaker. As the object was located on the right side, the right LSO cell fired one spike for each trial. The right LSO cell projected excitation across the midline to the left DNLL cell and caused the left DNLL cell to fire one spike per trial. Because the right IC cell was configured to receive inhibitory input from the left DNLL cell, it was inhibited and did not fire in response to object #2.

The bottom panel shows the results when we presented the two objects simultaneously. The left DNLL cells that fired to the trailing sound alone still fired due to the large distance between two objects. We see that the right IC cell was silent because its inhibitory input from the left DNLL was no longer deprived.

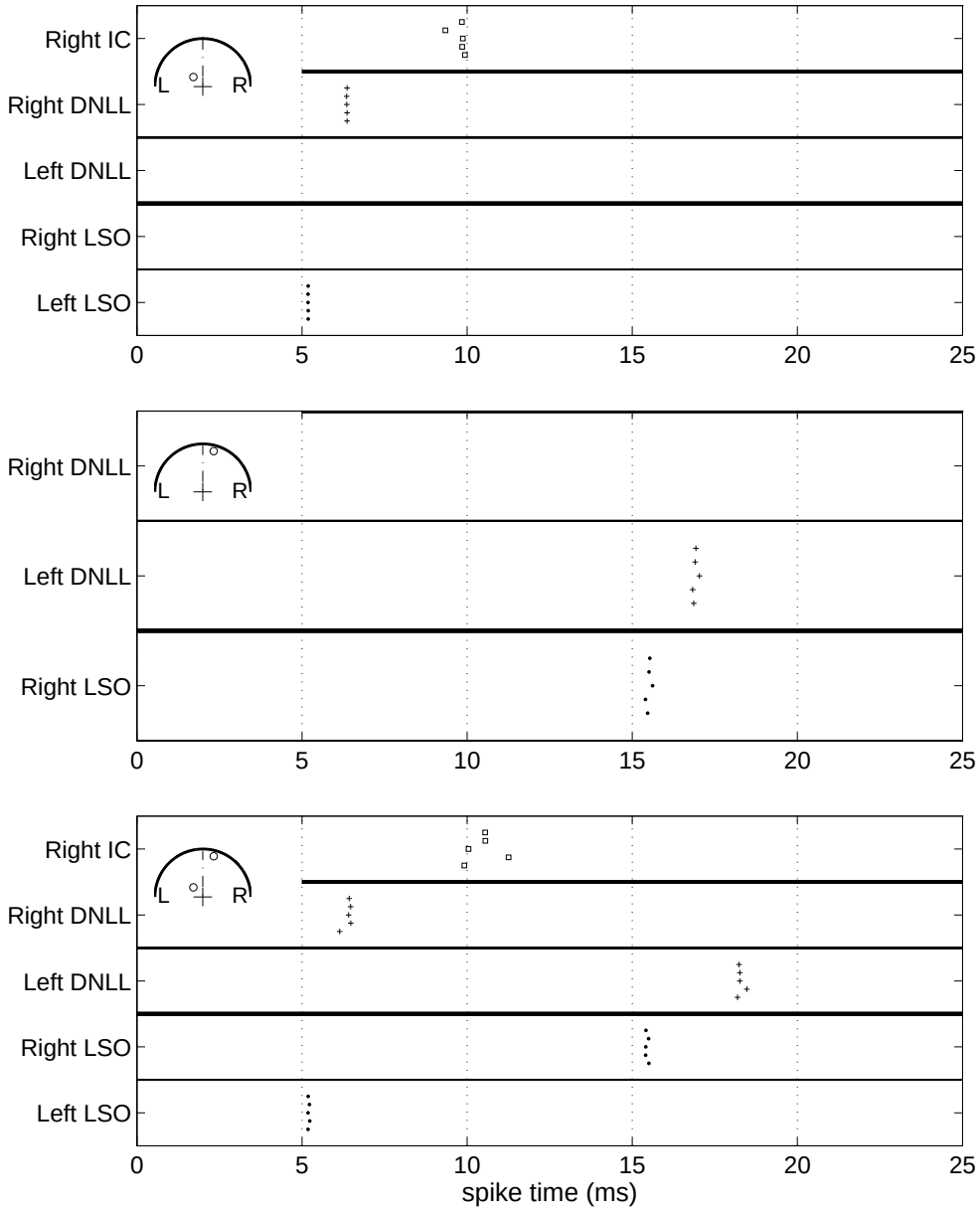


Figure 6.9: IC response to two objects that were 170 cm apart. Top: Object #1 alone was located at left (45°) and 80 cm away from the speaker. The left LSO cell fired and in turn excited the right DNLL. Middle: Object #2 alone was located at right (15°) and 250 cm away from the speaker, it excited the the right LSO cell and in turn drove the left DNLL cell to fire. Bottom: When both objects were presented, because the larger distance between two objects, the left DNLL cell was *not* inhibited from the opposite DNLL cell (right DNLL) . Thus the the right IC cell was inhibited by its inhibitory DNLL input and not fired to respond to object #2. Shown are raster plots with 5 trials. The inset on the left upper corner in each panel shows the relative location(s) of the target(s).

By checking some details from Fig. 6.8 and Fig. 6.9, we may gain some insights on how spike timing plays a critical role in auditory processing. Comparing the middle panel with the bottom panel for the left DNLL's spike timing, we see that when both objects were presented, the long-lasting cross-inhibition from the right DNLL was unable to inhibit the left DNLL, but it shifted the left DNLL's spikes to a later time (about 1 ms delay). If we check the bottom panel of Fig. 6.8 for the spike timing of the right IC cell, we see that the shifted left DNLL spikes timing were very close to the right IC cell's. It is possible that the left DNLL spikes can be shifted to behind those of right IC's so that the right IC cannot be inhibited. This can be due to either slightly different distance of two objects, or variations among the populations, or spike time jitter.

6.4 Discussion

In this chapter we have demonstrated a functioning hardware model of the bat LSO-DNLL-IC network which responds to multiple real sonar echoes using a spiking representation. We have demonstrated that the response of these anatomically justified network models to realistic stimuli is not a simple linear addition of the responses to single stimuli. In one case, we have shown the effects of a simple refractory period and subthreshold summation. In another case, we have shown the effect of long-lasting cross-inhibition of the DNLL in the network circuit.

We have proposed that when there exist multiple objects on the same side of the bat, the neuron's refractory period and subthreshold summation may have significant

effect on an EI cell's response to multiple sound sources. We have used a 1 ms refractory period for our test and have demonstrated that two targets separated by about 20 cm will be significantly affected. While we have only shown experimental results for the LSO population response, we point out that similar results can be predicted for DNLL and IC as well.

We have demonstrated that when there exist multiple objects on both sides of the midline of the bat, the long-lasting cross-inhibition between the left and right DNLL can alter its spatial selectivity to multiple sounds (objects). We have used an inhibition duration of about 10 ms for the DNLL in our experiments. We have demonstrated that for this inhibition duration, a close target will have a significant influence on the bat's response to a farther target on the other side of the midline of the bat, if the distance between the two targets is within 170 cm. We have also shown that the influence of previous echoes is not limited to simply preventing cells from firing or not, if also changes the initial conditions of cells that respond to subsequent echoes. In general, as pointed out by Burger and Pollak (2001), the long-lasting inhibition in the DNLL suggests that it may play an important role in the processing of ILDs that change over time.

We have demonstrated that a neuromorphic VLSI-based hardware system can help in exploring understanding biology. In the case of multiple sounds on the same side of the bat, we have demonstrated that we can propose a hypothesis and then test our hypothesis using this neuromorphic ILD system. In the case of the long-lasting cross-inhibition in the DNLL, we have demonstrated that we can use this neuromorphic system to test a hypothesis proposed by biological community. While

it is still extremely difficult (if not impossible) for a biologist to perform experiments with a known connection from LSO-DNLL-IC, our multi-layer network system can perform various tasks with different combinations of these connections. Also, to date there are no biological experiments on multiple sounds from real targets that have been reported as we have presented here.

Chapter 7

Design of the Summating and Exponentially Decaying Synapse

Synapses are a critical element of biologically-realistic, spike-based neural computation, serving the role of communication, computation, and memory. The neuromorphic ILD system described in previous chapters used a very compact synapse circuit. We achieved linear temporal spike summation in our LSO modeling work by operating the synapse in a very rapidly decaying mode. In this chapter we describe a novel CMOS synapse design that separately controls quiescent leak current, synaptic gain, and time-constant of decay. This circuit implements part of a commonly-used kinetic model of synaptic conductance. We show theoretical analysis and experimental data for prototypes fabricated in a commercially-available 1.5μm CMOS process.

7.1 Introduction

The interactions between neurons in the brain take place through connections termed synapse (Shepherd, 1979). Synapses are a critical element in neural computation (Koch, 1999). In the field of neuromorphic VLSI design, there are perhaps as many different synapse circuit designs in use as there are brain areas being modeled.

This diversity of circuits reflects the diversity of the synapse's computational function. In many computations, a narrow, square pulse of current is all that is necessary to model the synaptic current. In other situations, a longer post-synaptic current profile is desirable to extend the effects of extremely short spike durations (e.g., in address-event systems (Mahowald, 1994; Mortara, 1998; Deiss et al., 1999; Boahen, 1997)), or to create a specific time window of interaction (e.g., for coincidence detection or for creating delays (Cheely and Horiuchi, 2003)).

Temporal summation or more complex forms of inter-spike interaction are also important areas of synaptic design that focus on the response to high-frequency stimulation. Recent designs for fast-synaptic depression (Rasche and Hahnloser, 2001; McEwan and van Schaik, 2000; Boegerhausen et al., 2003) and time-dependent plasticity (Hafliger et al., 1997; Indiveri, 2002) are good examples of this where some type of memory is used to create interaction between incoming spikes. Even simple summation of input current can be very important in address-event systems where a common strategy to reduce hardware is to have a single synapse circuit mimic inputs from many different cells. A very popular design for this purpose is the "current-mirror synapse" (Boahen, 1997) that is used extensively in its original form or in new extended forms (Rasche and Hahnloser, 2001; Boegerhausen et al., 2003) to expand the time course of current and to provide summation for high-frequency spiking. This circuit is simple, compact, and stable, but couples the leak, part of the synaptic gain, and the decay "time-constant" to one control parameter. This is restrictive and often more control is desirable. Alternatively, the same components can be arranged to give the user manual-control of the decay to produce a true

exponential decay when operating in the subthreshold region (see Fig. 7 (b) in Lazzaro and Wawrzynek (1994)). This circuit, however, does not provide good summation of multiple synaptic events.

Only recently, silicon synapse circuit employing current-mode first order dynamics has been proposed. Shi and Horiuchi (2004) proposed a silicon synapse model and a circuit that utilized current-mode feedback to implement first-order dynamics. The model was based on the kinetic model of synaptic conductance proposed by Destexhe et al. (1994b). Arthur and Boahen (2004) reported a new CMOS synapse circuit that implemented the current mode first order dynamics differently.

In this chapter we describe a new CMOS synapse circuit that utilizes current-mode feedback to produce a first-order dynamical system. In the following sections, we describe the kinetic model of synaptic conductance, describe the circuit implementation and function, provide a theoretical analysis and finally compare our theory against testing results. We also discuss the use of this circuit in various neuromorphic system contexts and conclude with a discussion of the circuit synthesis approach.

7.2 Proposed Synapse Model

We consider a network of spiking neurons, each of which is modeled by the integrate-and-fire model or the Spike Response Model (Gerstner and Kistler, 2002; Maass, 1999). Synaptic function in such neural networks are often modeled as a spike-triggered, time-varying current. The functional form of this current could be

a δ function, or a limited jump at the time of the spike followed by an exponential decay. Perhaps the most widely used function in detailed computational models is the α-function, a function of the form $\frac{t}{\tau}e^{-\frac{t}{\tau}}$, introduced by Rall (1967).

A more general and practical framework is the neurotransmitter kinetics description proposed by Destexhe et al. (1994b). This approach can synthesize a complete description of synaptic transmission, as well as give an analytic expression for a post-synaptic current in some simplified schemes. For a two-state ligand-gated channel model, the neurotransmitter molecules, T, are taken to bind to post-synaptic receptors modeled by the first order kinetic scheme (Destexhe et al., 1994a):

$$R + T \underset{\beta}{\overset{\alpha}{\rightleftharpoons}} TR^* \tag{7.1}$$

where R and TR^* are the unbound and the bound form of the post-synaptic receptor, respectively. α and β are the forward and backward rate constants for transmitter binding. In this model, the fraction of bound receptors, r, is described by the equation:

$$\frac{dr}{dt} = \alpha[T](1 - r) - \beta r \tag{7.2}$$

If the transmitter concentration [T] can be modeled as a short pulse, then r(t) in Eq. (7.2) is a first order linear differential equation.

We propose a synapse model that can be implemented by a CMOS circuit working in the subthreshold region of operation. Our model matches Destexhe et al.'s equations for the time-dependent conductance, although we assume a fixed driving potential. In our synapse model, the action potential is modeled as a narrow digital pulse. The pulse width is assumed to be a fixed value t_{pw}, however, in practice

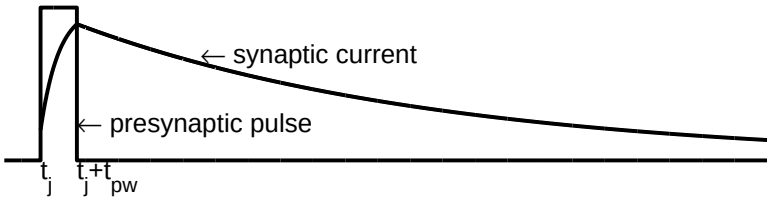


Figure 7.1: Synapse model. The action potential (spike) is modeled as a pulse with width t_{pw}. The synapse is modeled as first order linear system with synaptic current response described by Eqs. (7.3) and (7.4)

t_{pw} may vary slightly from pulse to pulse.

Fig. 7.1 illustrates the synaptic current response to a single pulse in such a model:

1. A presynaptic spike occurs at t_j, during the pulse, the post-synaptic current is modeled by:

$$i_{syn}(t) = i_{syn}(t_j) + i_{syn}(\infty)(1 - e^{-\frac{t-t_j}{\tau_r}}) \tag{7.3}$$

2. After the presynaptic pulse terminated at time $t_j + t_{pw}$, the post-synaptic current is modeled by:

$$i_{syn}(t) = i_{syn}(t_j + t_{pw})e^{-\frac{t-t_j-t_{pw}}{\tau_d}} \tag{7.4}$$

7.3 Circuit Synthesis and Analysis

7.3.1 The Synthesis Approach

Lazzaro and Wawrzynek (1994) present a very simple, compact synapse circuit that has an exponentially-decaying synaptic current after each spike event. The synaptic current always resets to the maximum current value during the spike and

is not suitable for the summation of rapid bursts of spikes. Another simple and widely used synapse is the current-mirror synapse that has its own set of practical problems related to the coupling of gain, time constant, and offset parameters. Our circuit is synthesized from the clean exponential decay from Lazzaro's synapse and concepts from log domain filtering (Seevinck, 1990; Frey, 1996) to convert the nonlinear characteristic of the current mirror synapse into an externally-linear, time-invariant system (Tsividis, 1997).

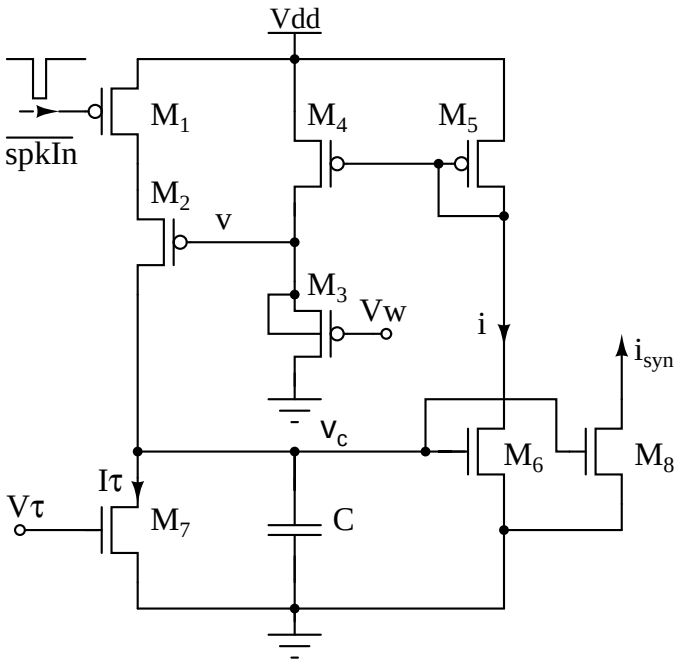


Figure 7.2: The basic synapse circuit. The pin "$\overline{spkIn}$" receives the spike input as a negative logic pulse. The pin "i_{syn}" is the synaptic current output. There are two control parameters. The input voltage V_w adjusts the weight of the synapse and the input voltage V_τ sets the time constant. The bodies of NMOS transistors are connected to ground, and the bodies of PMOS transistors are connected to Vdd except for M_3.

7.3.2 Basic Circuit Description

The synapse circuit consists of eight transistors and one capacitor as shown in Fig. 7.2. All transistors are operated in the subthreshold region. Input voltage spikes are applied through an inverter (not shown), onto the gate of the PMOS M_1. V_τ sets the current through M_7 that determines the time constant of the output synaptic current as will be shown later. V_w controls the magnitude of the synaptic current, so it determines the synaptic weight. The voltage on the capacitor is converted to a current by transistor M_6, sent through the current mirror $M_4 - M_5$, and into the source follower $M_3 - M_4$. The drain current of M_8, a scaled copy of current through M_6 produces the output current. This particular output can be connected to a neuron's membrane capacitance to act as an inhibitory current. A simple PMOS transistor with the same gate voltage as M_5 can provide an excitatory synaptic current for an excitatory version of the synapse.

7.3.3 Circuit Analysis

We perform an analysis of the circuit by studying its response to a single spike. Assuming a long transistor so that the Early effect can be neglected, the behavior of a NMOS transistor working in the subthreshold region can be described by (Mead, 1989; Vittoz and Fellrath, 1977)

$$i_{ds} = SI_{0n} e^{\frac{\kappa_n v_{gs}}{V_T}} e^{\frac{(1-\kappa_n) v_{bs}}{V_T}} (1 - e^{\frac{-v_{ds}}{V_T}}) \tag{7.5}$$

where $V_T = kT/q$ is the thermal voltage, I_{0n} is a positive constant current when $V_{gs} = V_{bs} = 0$, and $S = \frac{W}{L}$ is the ratio of the transistor width and length.

$0 < \kappa_n < 1$ is a parameter specific to the technology, and we will assume it is constant in this analysis. We assume that all transistors are operating in saturation ($v_{ds} > 4V_T$). We also neglect any parasitic capacitances.

The PMOS source follower $M_3 - M_4$ is used as a level shifter. Detailed discussion on use of source followers in the subthreshold region has been discussed in Liu et al. (2002). Combined with a current mirror $M_4 - M_5$, this subcircuit implements a logarithmic relationship between i and v (as labeled in Fig. 7.2):

$$v = V_w + \frac{V_T}{\kappa_p} \ln(\frac{i}{I_{0p}} \frac{S_4}{S_3 S_5}) \tag{7.6}$$

Consistent with the translinear principle, this logarithmic relationship will make the current through M_2 proportional to $\frac{1}{i}$.

For simplicity, we assume a spike begins at time t=0, and the initial voltage on the capacitor C is $v_c(0)$. The spike ends at time $t = t_{pw}$. When the spike input is on ($0 < t < t_{pw}$), the dynamics of the circuit for a step input is governed by

$$C\frac{dv_c(t)}{dt} = \frac{S_2 S_3 S_5 I_{op}^2}{S_4 S_6 I_{0n}} e^{\frac{\kappa_p (V_{dd} - V_w)}{V_T}} e^{\frac{-\kappa_n v_c(t)}{V_T}} - I_\tau \tag{7.7}$$

$$I_\tau = S_7 I_{on} e^{\frac{\kappa_n V_\tau}{V_T}} \tag{7.8}$$

With the aid of transformation

$$i_{syn}(t) = S_8 I_{on} e^{\frac{\kappa_n v_c(t)}{V_T}} \tag{7.9}$$

Eq. (7.7) can be changed into a linear ordinary differential equation for $i_{syn}(t)$:

$$\frac{di_{syn}(t)}{dt} + \frac{\kappa_n I_\tau}{C V_T} i_{syn}(t) = \frac{S_2 S_3 S_5 S_8 \kappa_n I_{op}^2}{S_4 S_6 C V_T} e^{\frac{\kappa_p (Vdd - V_w)}{V_T}} \tag{7.10}$$

In terms of the general solution expressed in (7.3), we have

$$\tau = \frac{CV_T}{\kappa_n I_\tau} \tag{7.11}$$

$$i_{syn}(0) = S_8 I_{0n} e^{\frac{\kappa_n v_c(0)}{V_T}} \tag{7.12}$$

$$i_{syn}(\infty) = \frac{S_2 S_3 S_5 S_8 I_{op}^2}{S_4 S_6 I_\tau} e^{\frac{\kappa_p (Vdd - Vw)}{V_T}} \tag{7.13}$$

and the synaptic current time course follows

$$i_{syn}(t) = S_8 I_{0n} e^{\frac{\kappa_n v_c(0)}{V_T}} + \frac{S_2 S_3 S_5 S_8 I_{op}^2}{S_4 S_6 I_\tau} e^{\frac{\kappa_p (Vdd - Vw)}{V_T}} (1 - e^{-\frac{t - t_j}{\tau}}) \tag{7.14}$$

When the spike input is off ($t > t_{pw}$) and we neglect the leakage current from M_2, then $i_{syn}(t)$ will exponentially decay with the same time constant defined by (7.11). That is,

$$i_{syn}(t) = i_{syn}(t_{pw}) e^{-\frac{(t - t_{pw})}{\tau}} \tag{7.15}$$

7.4 Test of the Basic Synapse Circuit

7.4.1 Comparison of Theory and Measurement

We have fabricated a chip containing the basic synapse circuit as shown in Fig. 7.2 through MOSIS in a commercially-available 1.5 μm, double poly fabrication process. The transistors sizes are listed in Table 7.1. In order to compare our theoretical prediction with chip measurement, we first estimate the two transistor parameters κ and I_0 by measuring the drain currents from test transistors on the same chip. The current measurements were performed with a Keithley 6517A electrometer. κ and I_0 are estimated by fitting Eq. (7.5) (and PMOS with PMOS i-v

equation) through multiple measurements of (vgs, ids) points through linear regression. The two parameters are found to be $\kappa_n = 0.67$, $I_{0n} = 1.32 \times 10^{-14} A$, $\kappa_p = 0.77$, $I_{0p} = 1.33 \times 10^{-19} A$. In estimating these two parameters as well as to compute our model predictions, we estimate the effective transistor width for the wide transistors (e.g. M_8 with m=20).

Table 7.1: Transistor sizes of the basic synapse circuit

transistor	M_1	M_2	M_3	M_4	M_5	M_6	M_7	M_8
width (μm)	2.4	8.0	40.0	4.0	4.0	4.0	4.0	200.0
length (μm)	1.6	4.0	4.0	4.0	4.0	4.0	4.0	4.0

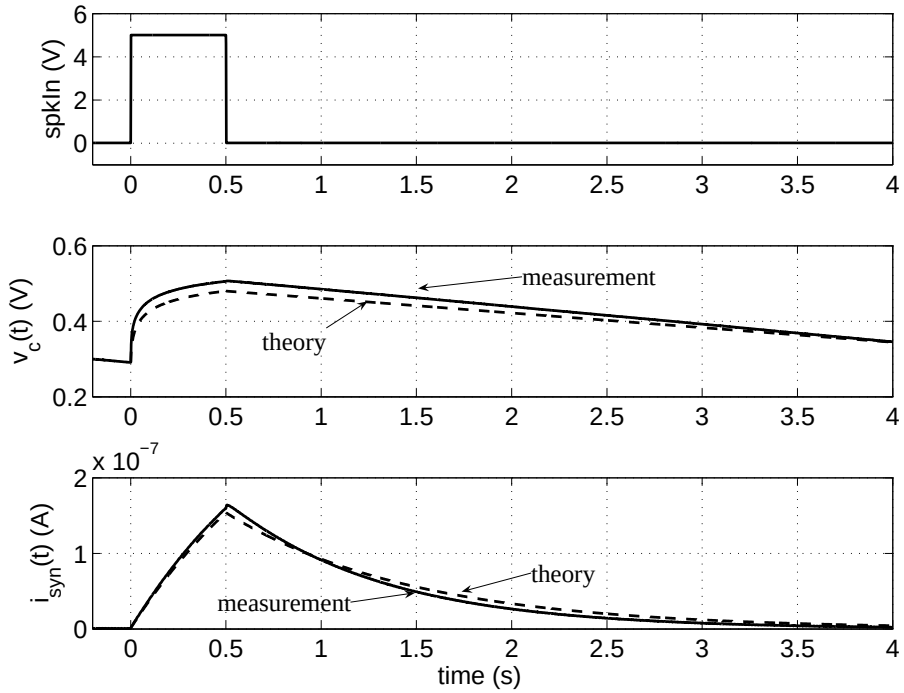


Figure 7.3: Comparison between model prediction and measurement. To illustrate the detailed time course, we used a large spike pulse width. We set $V_\tau = 0$ and $V_w = 3.85V$.

Fig. 7.3 illustrates our test results compared against the model prediction. We used a very wide pulse to exaggerate the details in the time response. Note that as

the time constant is so large, the $i_{syn}(t)$ rises almost linearly during the spike. In this case, $V_w = 3.85V$.

7.4.2 Tuning of Synaptic Strength and Time Constant

The synaptic time constant is solely determined by the leak current through transistor M_7. The control is achieved by turning the pin V_τ. In Fig. 7.4, we show how various synaptic time constant can be achieved by varying the pin V_tau. We also observed that the synaptic current magnitude increased as its time constant increased.

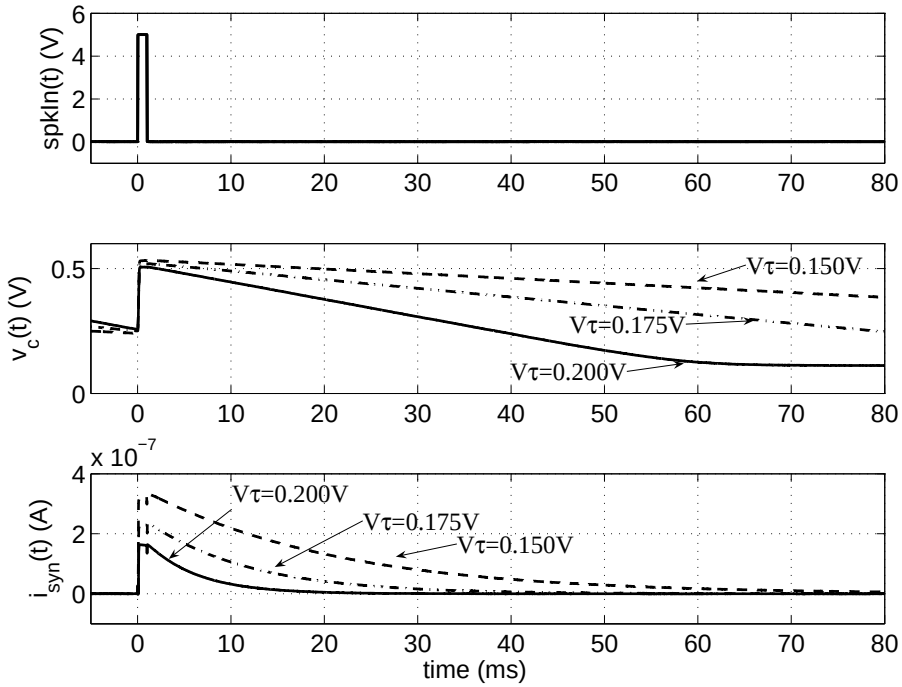


Figure 7.4: Changing the time constant τ. Keeping $V_w = 3.7V$ constant, but changing V_τ. Spike pulse width is set as 1 ms.

The synaptic strength is controlled by Vw (which is also coupled with I_τ) as can be seen from Eq. (7.13). In Fig. 7.5, we present our test results that illustrate

how the various synaptic strengths can be achieved by tuning the V_w. Note that the three decaying traces in the middle panel are in parallel indicates the time constants were not changed as we varied V_w.

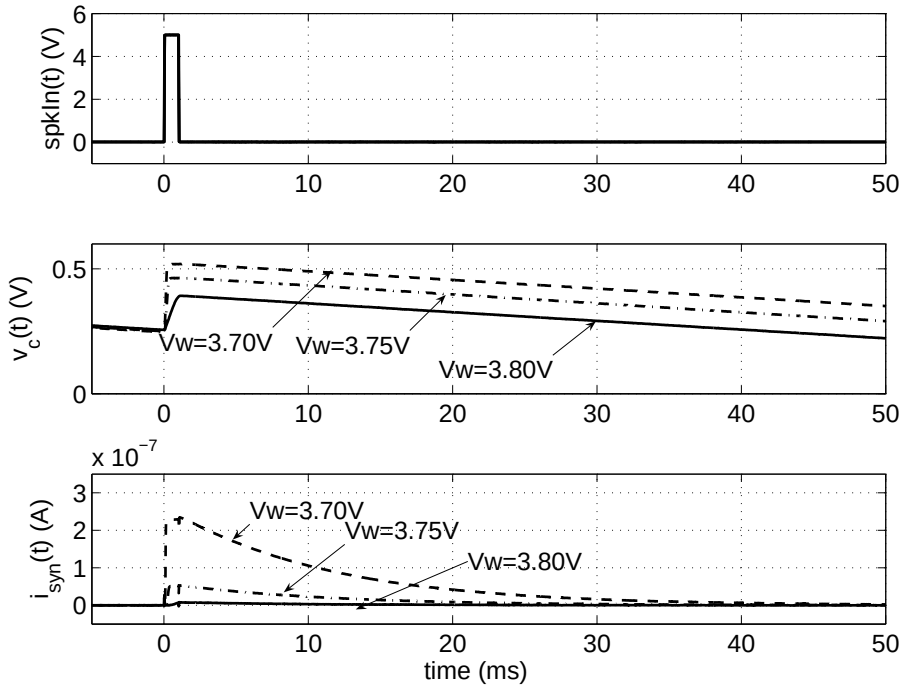


Figure 7.5: Changing the synaptic strength. Keeping $V_\tau = 0.175V$, but changing V_w. Spike pulse width is set as 1 ms.

7.4.3 Spike Train Response

The exponential rise of the synaptic current during a spike naturally provides the summation and saturation of incoming spikes. Fig. 7.6 illustrates this behavior in response to an input spike train of fixed duration.

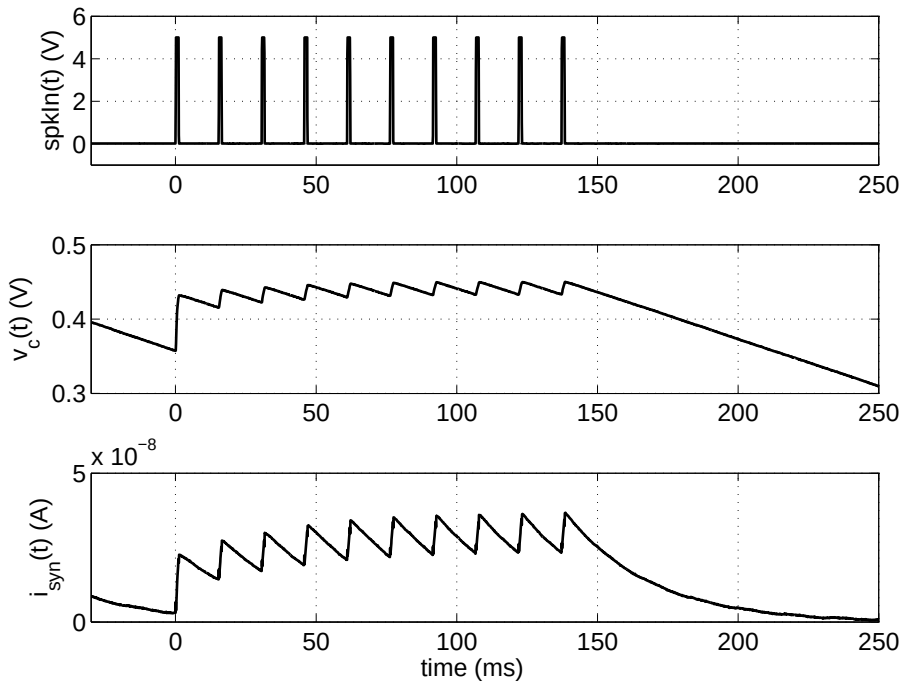


Figure 7.6: Response to spike train inputs. The spike pulse width is set as 1 ms, and period 15 ms. $V_w = 3.73V$, $V_\tau = 131mV$.

7.4.4 Nonidealities

In the above analysis, we have made two simplifications. First, we must assume that all transistors are in saturation. This will not always be true for transistor M_7 in Fig. 7.2. M_7 will be in the triode region of operation when $v_c(t) < 4V_T$, as described by Eq. (7.5) making the synaptic current response faster than predicted by Eq. (7.3) when $v_c(t)$ has settled to below 100 mV.

The second simplification is that we have ignored all parasitic capacitances. These capacitances become significant at very low current levels due to a slower response in the feedback loop. If a spike arrives when $v_c(t)$ is nearly zero, the transconductance (g_m) of the transistors in the feedback loop are still very small (below pA) and the loop responds with a delay. The $v_c(t)$ and thus $i_{syn}(t)$ are no

longer a simple first-order dynamic system. A simple solution for this is to bias the potential of the source of transistor M7 at some positive value V_b, so that $v_c(t)$ discharges only down to V_b, maintaining a quiescent current in the loop.

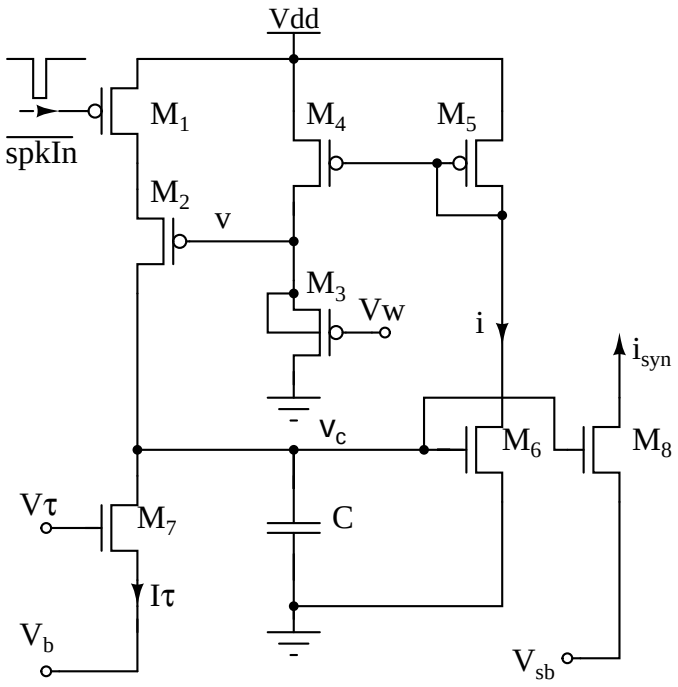


Figure 7.7: Synapse circuit with quiescent current. Pin V_b is added to bias the source of transistor M_7 at some positive value. Pin V_{sb} controls the quiescent level of synaptic current $i_{syn}(t)$. Connect pin V_{sb} to pin V_b will remove the the quiescent current of $i_{syn}(t)$ due to the voltage V_b. The bodies of NMOS transistors are connected to ground, and the bodies of PMOS transistors are connected to Vdd except for M_3.

Fig. 7.7 is the modified basic synapse circuit (Fig. 7.2). Pin V_b is added to bias the source of transistor M_7 at some positive value. Because of the bias of V_b, when spike input is off, the voltage $v_c(t)$ will no longer stays around zero but around the value of V_b. A positive value of v_c without spike input means the output synaptic current i_{syn} has a constant value. If this leakage current is not desired, pin V_{sb} should be connected to pin V_b.

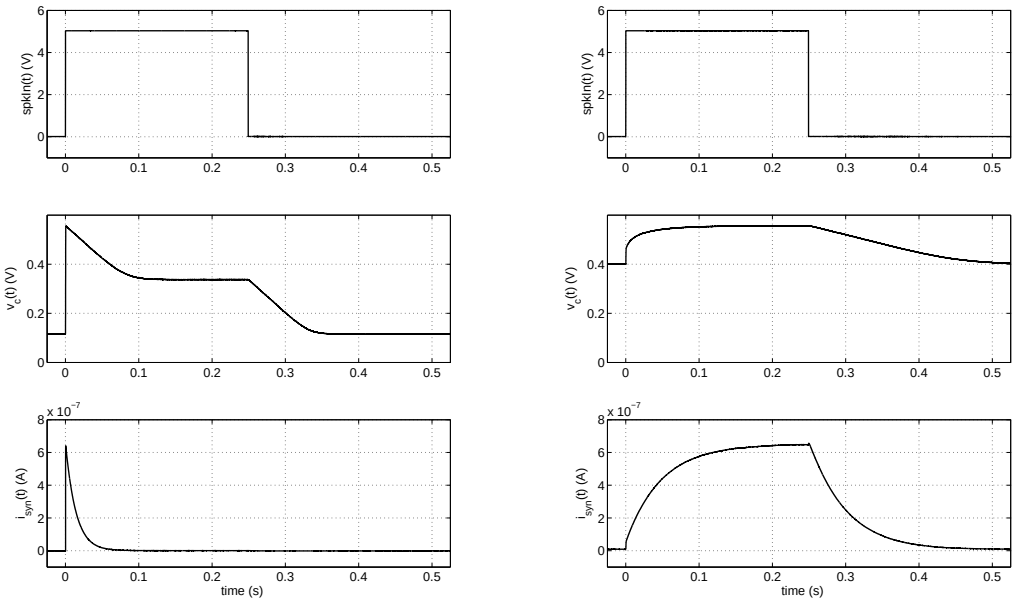
Fig. 7.8 shows the test results from a chip fabricated through MOSIS in a

Table 7.2: Transistor sizes of the synapse circuit with quiescent current

transistor	M_1	M_2	M_3	M_4	M_5	M_6	M_7	M_8	M_9
width (μm)	2.4	12.0	80.0	4.0	4.0	4.0	4.0	200.0	2.4
length (μm)	1.6	4.0	4.0	4.0	4.0	4.0	12.0	4.0	1.6

commercially-available 1.5 μm, double-poly fabrication process. Transistor sizes for this synapse circuit are listed in Table 7.2. Fig. 7.8(a) illustrates why such a current level control is needed to have the synapse circuit to work with first order dynamics. If V_b was set to zero (source of transistor M_7 was connected to ground), when an input spike was on, the voltage $v_c(t)$ (middle panel) rapidly rose to a peak value and then decayed to some constant value. The synaptic current (bottom panel) did not follow the exponentially rising time course as predicted by Eq. (7.14).

Fig. 7.8(b) shows the effect of the quiescent current control. When V_b was set at 300 mV, the synaptic current rose and saturated exponentially. In practice, a V_b value of 200 to 350 mV is needed to have the circuit to operate without noticeable delay in the loop. We note that in Fig. 7.8(a), $v_c(0)$ was 0.1 V (rather than 0.0 V). This 0.1 V shift was due to the use of a voltage follower inside the chip (for measurement purpose). Similarly, in Fig. 7.8(a), $v_c(0)$ was 0.4 V rather than 0.3 V. We also notice that although in both cases $v_c(0)$ was not zero, $i_{syn}(0)$ appears to be zero in both Fig. 7.8(a) and (b).



(a) (b)

Figure 7.8: Effect of the quiescent current. (a) Without current level control. V_b=0. (b) With current level control. $V_b = 0.30V$. In both (a) and (b), $V_{sb} = 0V$

7.5 Synapse Circuit with Two Time Constants

7.5.1 Theory and Circuit

As seen in Eq. (7.11), the time constant of $i_{syn}(t)$ for both the the rising and decaying phases, is solely determined by the constant current flowing through transistor M_7. This is not in agreement with the biological counterpart, as biological synapses usually have a faster rising phase than its decaying phase. In our circuit application, because the spike pulse width is much smaller than the spike interval, the same time constant can be a problem. In this section, we propose a synapse circuit that allows the separation of the rising time constant from the decaying time constant.

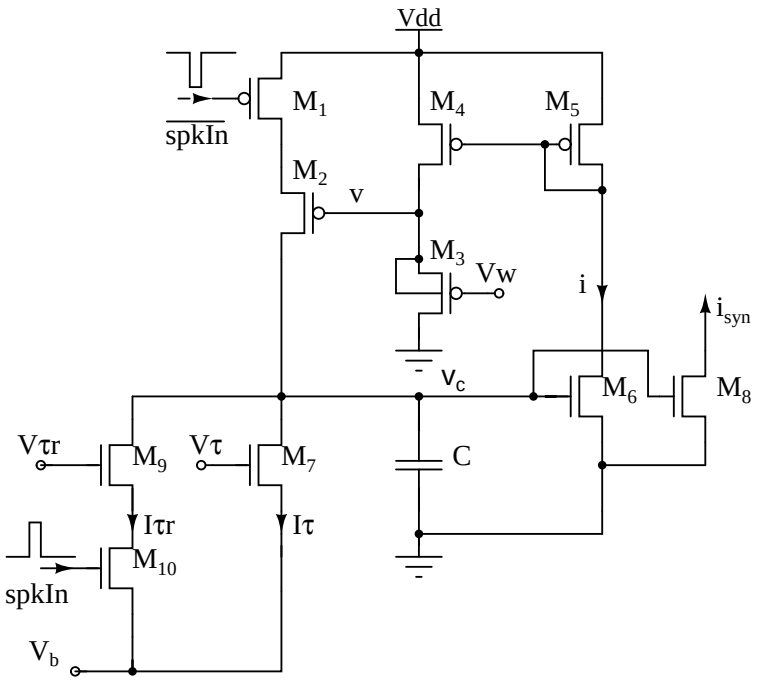


Figure 7.9: Synapse circuit with two time constants. Transistors M_9 and M_{10} are added to provide a second current branch when spike input (spkIn) is on. V_b provides the necessary current level to start the feedback loop.

Fig. 7.9 is the synapse circuit with two time constants. Transistors M_9 and M_{10} are added to form a second current branch. When the spike input is on, transistor M_9 provides a constant current $I_{\tau r}$ in addition to the current I_τ. When the spike input is off, the branch of transistors M_9 and M_{10} is open circuit, circuit Fig. 7.9 returns to the same mode as the basic circuit of Fig. 7.2. That is, the decaying phase of the synapse circuit is the same as that of the basic one-time-constant circuit. Therefore, the decaying time constant is

$$\tau_d = \frac{CV_T}{\kappa_n I_\tau} \tag{7.16}$$

And the rising time constant is

$$\tau_r = \frac{CV_T}{\kappa_n (I_{\tau r} + I_\tau)} \tag{7.17}$$

From Eq. (7.13), we know that increasing I_τ will decrease $i_{syn}(\infty)$. That is true

because adding a current branch also means the current that charges the capacitor is decreased. This coupling of τ_r and $i_{syn(\infty)}$ requires us to increase both the synaptic strength (by reducing V_w) and the leakage current (by increasing $V_{\tau r}$).

7.5.2 Test Results

We test the circuit from a chip fabricated through MOSIS in a commercially-available 1.5 μm, double poly fabrication process. The transistors sizes are listed in Table 7.3.

Table 7.3: Transistor sizes of the synapse circuit with two time constants

transistor	M_1	M_2	M_3	M_4	M_5	M_6	M_7	M_8	M_9	M_{10}
width (μm)	2.4	4.0	16.0	4.0	16.0	4.0	4.0	200.0	4.0	2.4
length (μm)	1.6	1.6	1.6	4.0	1.6	4.0	4.0	4.0	4.0	1.6

Fig. 7.10 illustrates how we can vary τ_r but keep τ_d constant. In the test, the V_τ was held constant at 0.650 V, but $V_{\tau r}$ was varied. We see first because of $V_{\tau r}$, the rising phase was faster than the decaying one. This is especially true where $V_{\tau r}$ was 0.750 V, in which case the rising synaptic current had reached steady state within the 1 ms spike. The decaying phase, however, was still far from the steady state even after 10 ms. Secondly, we note that when $V_{\tau r}$ varied, the decaying phase kept the same time constant as can be found by the fact that the two decaying traces in the middle panel were in parallel.

Fig. 7.11 illustrates how such a two time constant synapse respond to a spike train. By setting the rising time constant smaller than decaying one, the synapse was able to respond quickly to narrow spike - 0.1 ms pulse width in the test.

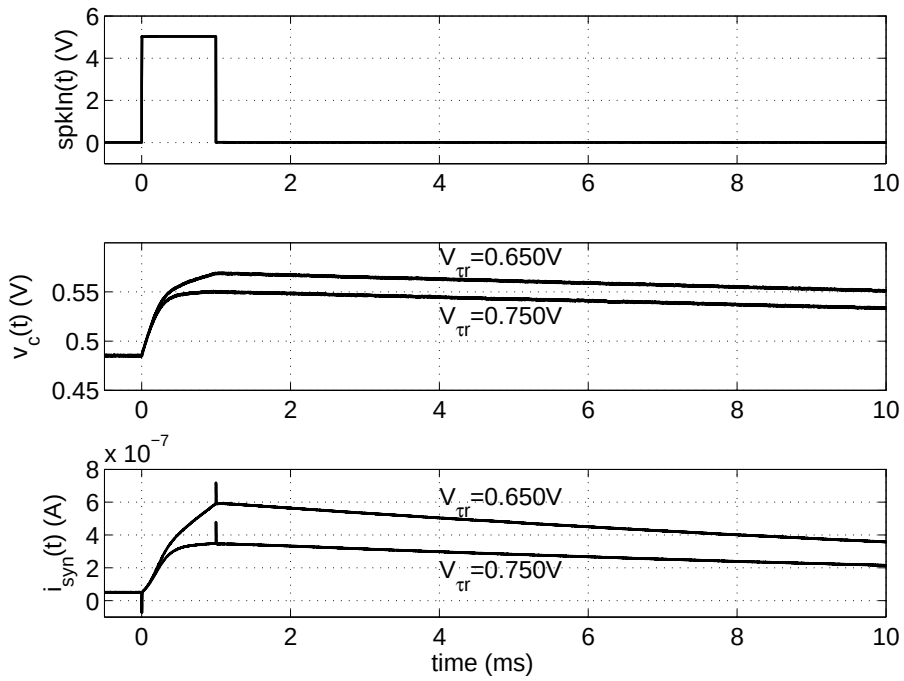


Figure 7.10: Varying τ_r with a fixed τ_d. $V_{\tau r}$ varied from 0.650 V (top trace) to 0.750 V (bottom trace). Note that the two decaying traces in the middle panel were in parallel indicated that the decaying time constant was not affected when the rising time constants were changed. The pulse width was 1 ms. V_τ=0.650 V, V_b=0.350 V, V_w=3.90 V

7.6 Toward a Linear Summating Synapse

7.6.1 Theory and Circuit

The exponentially rising time course in either the single time-constant synapse circuit (Fig. 7.2) or the two time-constant synapse circuit (Fig. 7.9) allows linear temporal summation of spikes only at small time interval. Because of the saturation of synaptic current, the later a second spike comes, the smaller the additional synaptic current it produces. While this feature may find various applications, there are situations where linear spike temporal summation is desired.

From our analysis of the basic synapse circuit (Fig. 7.2), the rising and de-

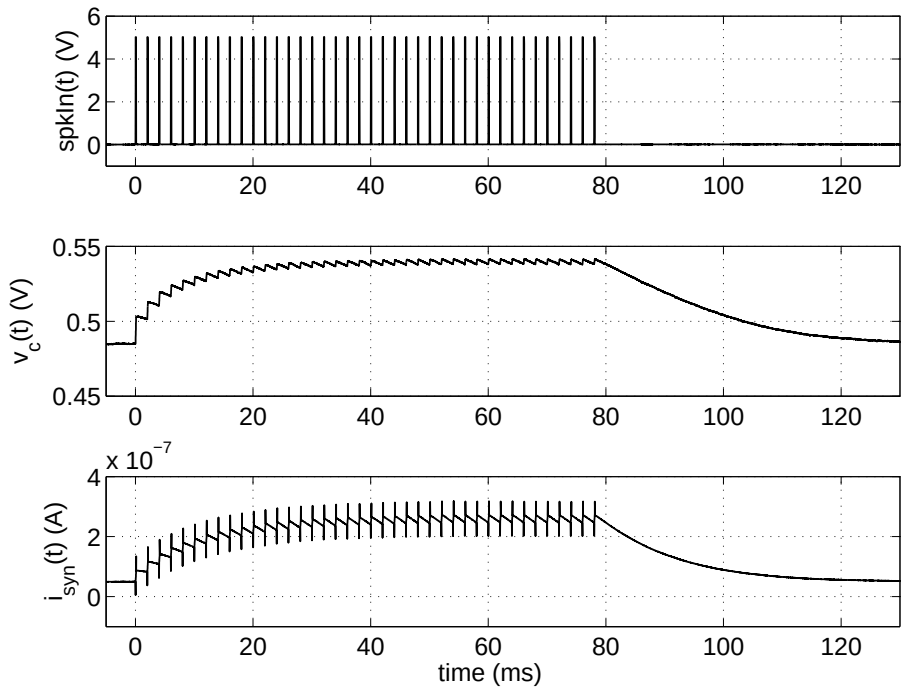


Figure 7.11: Response of the two time constant synapse to an input spike train. $V_{\tau r} = 0.700V$, $V_\tau = 0.650V$. By having a faster rising phase, the synapse circuit was able to respond to narrower spike, 0.1 ms pulse width in this test. The train consisted of 40 spikes in total with an interval of 2 ms. $V_w = 3.875V$, $V_b = 0.350V$.

caying time course of synaptic current have the same time constant determined by Eq. (7.11). This time constant is simply determined by the leakage current I_τ, the current controlled by transistor M_7.

Linear temporal summation requires that the rising synaptic current is linear function of time. We may achieve this by an exponentially rising synaptic current with infinite time constant. From Eq. (7.14), we can show that

$$\lim_{I_\tau \to 0} i_{syn}(t) = \frac{S_2 S_3 S_5 S_8 I_{op}^2}{S_4 S_6} e^{\frac{\kappa_p (Vdd - Vw)}{V_T}} t + S_8 I_{0n} e^{\frac{\kappa_n v_c(0)}{V_T}} \tag{7.18}$$

To implement this idea, we add a switching transistor onto the branch that produce the current I_τ. Fig. 7.12 is the proposed linear summating synapse circuit. Transistor M_9 is added to switch off the current when the input spike is on, and

switch on the current I_τ when the input spike is off.

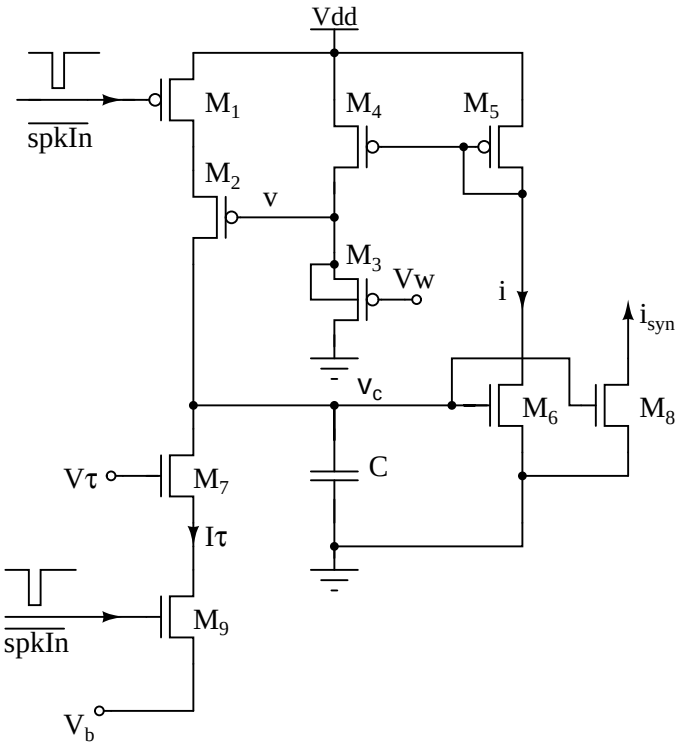


Figure 7.12: A linearly summating synapse circuit. Transistor M_9 switches off the branch current when the input spike is on. When the input spike is off, transistor M_9 is on and the branch current is I_τ. The bodies of NMOS transistors are connected to ground, and the bodies of PMOS transistors are connected to Vdd except for M_3.

Of course, I_τ never goes to zero in reality. When transistor M_9 is off, the branch current I_τ is about the order of I_{0n}. We can estimate the order of this rising time constant by using $\kappa_n = 0.5$, $I_{0n} = 1.0 \times 10^{-14}A$, $C = 500 \times 10^{-15}F$, and $V_T = 0.025V$. From Eq. (7.11), this gives a rising time constant of 2.5 s. This large time constant will enable spikes coming within a few hundred ms time frame to perform a linear temporal summation through this synapse circuit.

7.6.2 Test Results

We have fabricated a chip containing the linear summating synapse circuit as shown in Fig. 7.12 through MOSIS in a commercially-available 1.5 μm, double-poly fabrication process. The transistors sizes are listed in Table 7.4.

Table 7.4: Transistor sizes of the linear summating synapse circuit

transistor	M_1	M_2	M_3	M_4	M_5	M_6	M_7	M_8	M_9
width (μm)	2.4	12.0	80.0	4.0	4.0	4.0	4.0	200.0	2.4
length (μm)	1.6	4.0	4.0	4.0	4.0	4.0	12.0	4.0	1.6

In Fig. 7.13, we demonstrate the circuit response to a very wide single spike with pulse width of 100 ms. When the input spike is on, the synaptic current (the bottom panel) rises linearly as time increases. In fact, because the rising time constant is a couple of seconds, this synaptic current would have continued to rise linearly until the transistors left subthreshold. The fact that the synaptic current is linear function of time means that the voltage $v_c(t)$ is a natural logarithmic function of time, as shown in the middle panel in Fig. 7.13. When the spike is off, the synaptic current decays exponentially and reaches steady state within 100 ms.

Next, we show the synapse response to a spike train. The test result is shown in Fig. 7.14. The spike train has 10 spikes with spike interval of 5 ms. In order to show clearly each rising phase, we chose a 2 ms pulse width, a relatively long duration comparing with both biological spike times and spike durations in many neuromorphic applications (e.g. AER systems). From the bottom panel, we see for each spike, the synaptic current rises a constant value. However, large switching transients can be seen from the measurement. In this prototype circuit, no special

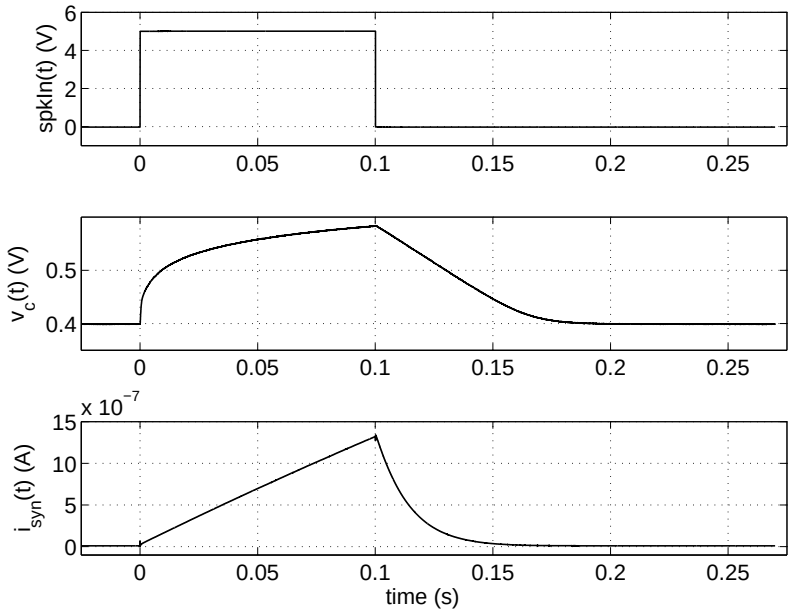


Figure 7.13: Response to a single spike of the linear summating synapse. When spike is on, the synaptic current is linear function of time. When the spike is off, the synaptic current is exponentially decaying with time constant determined by Eq. (7.11). For this test, The spike pulse width is set as 100 ms. $V_w = 3.70V$, $V_\tau = 700mV$, $V_b = 300mV$.

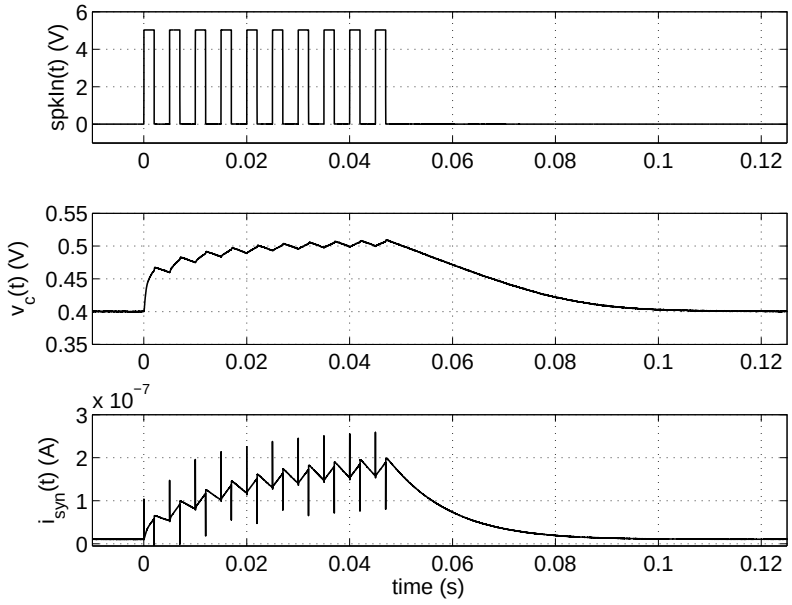


Figure 7.14: Response of the linearly summating synapse to an input spike train. The input is spike train of 10 spikes, with pulse width of 2 ms and spike interval of 5 ms. Circuit settings are the same as in Fig. 7.13

design for minimizing switching transients has been considered.

7.7 Discussion

We have proposed a new synapse model and a specific CMOS implementation of the model. We have demonstrated a prototype circuit that exhibit the same first-order dynamics that are utilized by Destexhe et al. (Destexhe et al., 1994b; Destexhe et al., 1994a) to describe a kinetic model description of receptor-neurotransmitter binding for a more efficient computational description of the synaptic conductance. The synapse model, by employing first-order dynamics and the separation of time constants for the rise and decay phases, provides an easily controlled exponential decay and a natural summation and saturation of the synaptic current. By using simple first-order dynamics, our synapse circuit model can give the circuit designer an analytically tractable function for use in large, complex, spiking neural network system designs. The current-mirror synapse, in spite of its use in many existing applications, has been found to be an inconvenient computational unit due to its nonlinearity.

The synthesis methodology was current-mode feedback with the subthreshold exponential characteristic of the MOSFET. We have successfully applied the log-domain synthesis approach (which has been actively used for filter design) for a synapse design that works in large signal mode. The exponential characteristic of the MOSFET provides an efficient substrate for implementation of the model. The subthreshold mode of operation also allows our synapse circuit to produce

similar current amplitudes, time constants as its biological counterpart. Because all transistors in our synapse circuit operate in subthreshold, the circuit consumes very little power.

We have achieved linear temporal spike summation by designing a synapse with a large rising time constant. Linear summation of synaptic current over an input spike train means that when a spike is on, the synaptic current rising linearly as time. The linearly rising synaptic current in our circuit model is an approximation to an exponentially rising dynamics with very large time constant. While our purpose of designing such a linearly summating synapse is to use it in address-event systems to mimic inputs from many different cells to reduce hardware, we point out that linear summation exists in biological neurons. Recently, it has been reported that two excitatory inputs sum linearly, and this linear summation is independent of input dendritic position (Cash and Yuste, 1998).

The need to use a quiescent current (V_b) indicates that the first-order model is an approximation. In our theoretical analysis, we have ignored all parasitic effects which can play a significant role in the circuit behavior. Indeed, the need to use current control pin V_b indicates that nonidealities exist. Although we have demonstrated the effect of current control by some positive bias of the source voltage of transistor M_7, we have not addressed another important issue - the switching transients. For example, as the source follower $M_3 - M_4$ provides the gate voltage of M_2, switching through M_1 will affects the circuit behavior due to parasitic capacitance. Switching transients can been seen in all the test results, including the basic synapse circuit, the two time constant circuit, and the linearly summating synapse

circuit. The successful application of the proposed synapse circuit depends on if we can largely on reducing these switching transients.

Our first-order dynamics synapse was achieved at the cost of silicon area. This is especially true when utilized in an AER system, where the spike duration can be less than a microsecond. Because our linearity is achieved by employing the CMOS subthreshold current characteristic, working with very narrow pulses will mean the use of very large transistor widths to get large charging currents. Therefore, our synapse circuit operates best at these current levels and longer spike durations.

Chapter 8

Conclusion and Future Work

8.1 Contributions

8.1.1 Contributions to Biological Modeling

This dissertation study has led us to believe that ILD processing in the bat brainstem and midbrain represents an exceptionally interesting subject that invites more scientific endeavors. We have identified two important reasons why it is worth further exploration. First, it is good candidate for the study of first spike latency as a possible neural code. Second, the circuitry that links AVCN, LSO, DNLL, and IC can be considered a classic four layer spiking neural network for more extensive studies. Compared with other studies that investigated the possible roles of spike timing in coding the information about sound location (e.g. Eggermont, 1998; Furukawa and Middlebrooks, 2002), this study contributes to neural computation research by showing how first spike latency as a neural code operates in a specific auditory system, especially how first spike latency can be processed and transformed by a multilayer recurrent spiking neural network.

This work improves our understanding of the neural mechanism that underlies ILD processing using a model that computes with spike timing. We suggest that

one function of the copy cell that forms a large portion of EI cells in both DNLL and IC is to generate the necessary spike latency for processing ILD at each ascending stage. Intensity-latency trading has been shown to be a natural outcome for a neural code that computes with spike timing, and we have demonstrated explicitly how it works in our "modified cell" model in the IC. The finding that first spike latency of an EI cell in the LSO is inherently related to its ILD of complete inhibition shed some light on how azimuth is encoded in the bat. First, if the ILD of complete inhibition codes the azimuth as is currently believed by the biological community, the first spike latencies from a population of EI neurons will also likely be a code for the azimuth of the sound source. Second, as suggested by Covey (2000), one of the principles for any possible population codes for auditory process is it must necessarily incorporates a time dimension. We suggest that spatially distributed first spike latencies that inherently represent a distributed ILD of complete inhibition among the EI population can serve as a fast azimuth code that can be easily "read-out" by ascending stages.

This modeling work differs from other ILD models by working with real world signals and by having addressed ILD processing of multiple sound sources. We have shown that when multiple sound sources are present, both an individual neuron's properties and the interaction from other cells via the network connections must be considered. We have proposed and shown that a neuron's refractory period and sub-threshold summation may have a significant effect on its response to multiple sound sources located on the same side of the midline of the bat. We have demonstrated with real targets to what extent the long-lasting cross-inhibition in the DNLL can

alter the spatial selectivity of EI cells to multiple sounds located on both sides of the midline of the bat. To date there are no biological experiments on multiple sounds from real targets as we have presented here.

This work represents another example neuromorphic hardware model that can be a valuable tool for neurobiologists. With this functioning hardware model of the bat LSO-DNLL-IC network that includes much of the detail of known interconnections among layers, we have demonstrated that while it is still extremely difficult (if not impossible) for a biologist to perform experiment with known connections from LSO-DNLL-IC, our multi-layer network system can perform various tasks with different combinations of connections. This study provides support for some hypotheses about interconnections among ILD pathways proposed by the biological research community. For example, our model has confirmed that the contralateral DNLL can modify an IC cell's EI properties and the effect of this modification is to shift the IC cell's ILD of complete inhibition to a more positive ILD value. This neuromorphic model can be used to further test other hypotheses. ILD processing is not a computation unique to bats, it is a significant feature for high frequency sound localization in other mammals. Our model, by extension, captures many aspects of ILD computation in these systems as well.

8.1.2 Contributions to Engineering

Designing a machine to detect target azimuth may be not a challenging task in the eyes of modern engineers. But designing a small, low power and quickly

responding flying vehicle that localizes targets solely by sonar is by no means a trivial task. This work contributes to the engineering community by illustrating how bats solve the azimuthal location problem by employing acoustic cues (ILDs) and utilizing active sonar detection (echolocation).

The success of engineering work often relies on the correct selection of key elements and optimization of design architecture. One of the key elements in the front-end system is the logarithmic envelope detector (AD640 from Analog Device). Logarithm computation has traditionally used diodes or bipolar transistors. This device physics based (p-n junction) logarithmic computation, although it is small in area and easy in design, is only suitable for DC signals or low frequency signals. The logarithmic envelope detector that we chose to use (AD640), however, can work with high frequencies (120 MHz in our case), is stable over a large temperature range, and does the envelope extraction and logarithmic encoding in one device. Such a device is recommendable to the neuromorphic engineering community where logarithmic computation prevails. As for design structure, while AER has conventionally been used for multi-chip communication to overcome the limited number of I/O pads, this work serves as a good example where AER can be used for both intra-chip and inter-chip communication. As is shown in this work, dividing the whole chip into two functional parts and connecting the two parts with virtual wires (AER) has the advantage of more possible connections among layers by the aid of reconfigurable circuitry.

This work has demonstrated that variations among units in an analog VLSI circuit due to the inevitable transistor mismatch can generate the desired diversity

of response found in their neural counterparts. This idea has recently been discussed by Merolla and Boahen (2006). We have shown that a population of LSO cells with a distributed ILD of complete inhibition can be achieved by utilizing the variations in transistor characteristics along an array of EI cells using the same circuit parameter voltages. This result suggests that rather than increasing transistor sizes to overcome fabrication mismatch among transistors in a die, neuromorphic VLSI designers can consider designing large arrays of small mismatched circuit units to produce a diversity of responses. This, of course, also means that some external digital reconfigurable circuitry will be necessary to re-route signals accordingly.

This work advocates the use and design of summating and exponentially decaying synapses. To this end, we contribute to the neuromorphic engineering community in two aspects. First, we have identified and chosen a very compact and easily controllable synapse circuit. We have perhaps made the fullest use of this synapse to date. We successfully achieved linear temporal spike summation in our LSO modeling work by operating the synapse in a very rapidly decaying mode. Using the same synapse with a long synaptic time constant, we also apply it to modeling a nonlinear intensity-latency trading in the "*de novo*" cell. We have demonstrated that by selecting such an exponentially decaying synapse, we were able to propose a circuit model that is mathematically tractable. Second, we promote this type of synapse by proposing a synapse model that is both compatible with those used in computational models and implementable by CMOS transistors operating in subthreshold region.

8.2 Future Work

We have described a modular VLSI implementation of a neural model for the azimuthal localization of short echolocation sounds. Before we suggest future directions for extending this modular work, we point out two important projects that can be done without much modification or new development.

8.2.1 Further Projects with the Current neuromorphic system

The first project would be a study of ILD processing on moving sounds. This dissertation work has demonstrated the impact of long-lasting cross-inhibition between the two DNLL regions on the response of the IC to multiple echoes from both sides of the acoustic midline of the bat. It has been suggested that the long-lasting cross-inhibition from the DNLL may play an important role for moving sound. For example, a sound source moving from the contralateral side into the ipsilateral side may evoke stronger response in the IC than a sound source moving from the ipsilateral side to the contralateral side (Burger and Pollak, 2001). The fact that bats fly while they perform echolocation tasks suggests that studies of how bats respond to moving targets is very important. Some neurophysiological experiments on the encoding of moving sound sources in the bat's brainstem and the inferior colliculus have shown many different properties not seen in those using static stimuli (e.g. Schlegel, 2002; Wilson and O'Neill, 1998). With a sonar head that can turn with a controllable speed, or with a target that can be moved at given speed, our neuromorphic ILD processing system will be ready for exploring how EI cells in the

brainstem and midbrain encode not only azimuth, but also dynamic features such as velocity and movement direction.

The second important project would be a study of ILD processing on consecutive sonar pulses. This dissertation study has concentrated on the neural response to a single sonar pulse (stimuli were separated by large inter-pulse interval). Bats perform echolocation by emitting a train of pulses with an increasing repetition rate from the initial search stage to final capture stage. A neuron's recovery cycle determines its ability to follow repetitive sound pulses. It has been found that the recovery cycle of the neurons in the IC of *Eptesicus fuscus* is azimuth dependent: most IC neurons have a longer recovery cycle time for ipsilateral sound pulses than for contralateral sound pulses. This azimuth-dependent recovery cycle of IC neurons has been suggested to be due to residual GABAergic binaural inhibition that varies with azimuth (Lu et al., 1998; Zhou and Jen, 2004). Using the current neuromorphic system that includes most of the known connections to the IC, it will be interesting to investigate the mechanism underlying this azimuth-dependent recovery cycle and its functional role in bat azimuthal localization.

8.2.2 Limitations of the Current System and Long-term Expansion

To model ILD computation at the LSO EI cell, we used a spiking neuron with one excitatory synapse and one inhibitory synapse. The inputs to the LSO were modeled as being from two representative AVCN neurons. The dense spike train from the AVCN neurons requires that the synapse circuit works in a rapid mode

to achieve linear operation. The use of a very short synaptic time constant for the synapse circuit means that the first spike latency of the LSO EI cell is much shorter than desired. To have enough current to drive the neuron to fire, the use of this small synaptic time constant requires either using a larger synaptic strength parameter, or a larger transistor aspect ratio in chip design. This drawback of this synapse circuit we used has led to a new synapse circuit design as described in Chapter 7. Our new synapse circuit needs some more work before it can be applied to the system. First, it works best for pulse widths in the millisecond range. In an AER system, pulse width can be less than a microsecond. This limitation can be overcome by either using pulse extending circuitry in connection with the synapse circuit, or implementing the first-order dynamic using different circuitry from using the feedback approach as those described in Chapter 7. Second, switching current can cause large transients in the circuit that will affect synaptic computation. Circuit design techniques to minimize these switching transients need to be investigated.

The LSO-DNLL-IC CMOS chip was designed to investigate how various EI properties can be achieved through different network connections. Although most known connections among the three ILD processing centers have been included, only one synapse was used to represent any specific interaction or connection between two neurons. An inter-chip AER structure was chosen to achieve reconfigurable network operation. Experimental results using the current chip will serve as a guide for future chip designs. We may design EI neuron circuits in the DNLL and the IC layer that have multiple synapses for each particular type. Using the copy cell as an example, we may wish to have each DNLL or IC copy cell receive excitatory

inputs from multiple (e.g. four) LSO EI cells. We may also wish to combine the two functional parts into one by removing the inter-chip AER structure. Removing the inter-chip AER structure can save some pads and therefore allow the design a larger population of neurons.

For the longer-term expansion of the current system, we consider three major directions. First, the design of a wide-band sonar system using a wide-band ultrasonic speaker and microphones for the sonar head, and a front-end with multiple frequency channels. Second, the integration of a cochlear chip that can provide AVCN population input to the LSO-DNLL-IC chip. Third, work with other modular implementations for range localization and elevation localization.

Appendix A

Theoretical ILD of the Spherical Head Model

Equations necessary to plot Fig. 2.1 in Section 2.1 are listed in this appendix. The HRTF for the rigid spherical model is first defined. All the formula is from Duda and Martens (1998). The ILD is defined mathematically in the last.

For a complex sinusoidal point source of the form $S_\omega e^{-i\omega t}$, the free-field pressure at a distance r from the source is given by

$$p_{ff}(r,\omega,t) = -i\omega\frac{\rho_0 S_\omega}{4\pi r}e^{i(kr-\omega t)} \tag{A.1}$$

where $k = \omega/c$, ω is the radian frequency (rad/s), c the ambient speed of sound (m/s), ρ_0 the density of air (kg/m^3). The presence of the sphere diffracts the sound wave and modifies the pressure field. The pressure on the surface of sphere of a radius of a can be found as

$$p_s(r,a,\omega,\theta,t) = \frac{i\rho_0 c S_\omega}{4\pi a^2}\Psi e^{-i\omega t} \tag{A.2}$$

where Ψ is the infinite series expansion

$$\Psi = \sum_{m=0}^{\infty}(2m+1)P_m(\cos\theta)\frac{h_m(kr)}{h'_m(ka)},\ r > a \tag{A.3}$$

Here P_m is the Legendre polynomial of degree m, h_m is the mth-order spherical Hankel function, h'_m the derivative of h_m with respect to its argument. θ is the angle of incidence, that is, the angle between the ray from the center of the sphere

to the source and the ray to the measurement point on the surface of the sphere. The normal incidence corresponds to $\theta = 0°$. It is usually convenient to use the normalized frequency by

$$\mu = ka = f\frac{2\pi a}{c} \tag{A.4}$$

and the normalized distance by

$$\rho = \frac{r}{a} \tag{A.5}$$

The "head-related transfer function" (HRTF) $H(\rho, \mu, \theta)$ that relates the pressure that would be present at the center of the sphere in free filed to the pressure that is actually developed at the surface of the sphere can be found as

$$H(\rho, \mu, \theta) = \frac{p_s}{p_{ff}} = -\frac{\rho}{\mu}e^{-i\mu\rho}\sum_{m=0}^{\infty}(2m+1)P_m(\cos\theta)\frac{h_m(\mu\rho)}{h'_m(\mu)},\ \rho > 1 \tag{A.6}$$

Assuming the two ears are located at $\pm\beta$ azimuthal degree, the far-field interaural level difference (ILD) for a sound source at azimuth ϕ is defined as

$$ILD(\rho, \mu, \phi) = 20\log_{10}\left(\frac{|H(\rho, \mu, \beta - \phi)|}{|H(\rho, \mu, \beta + \phi)|}\right) \tag{A.7}$$

BIBLIOGRAPHY

Arthur JV, Boahen K (2004) Recurrently connected silicon neurons with active dendrites for one-shot learning In *Proceedings of IEEE International Joint Conference on Neural Networks*, Vol. 3, pp. 1699 – 1704.

Aytekin M, Grassi E, Sahota M, Moss CF (2004) The bat head-related transfer function reveals binaural cues for sound localization in azimuth and elevation. *J. Acoust. Soc. Am.* 116:3594–3605.

Blackstock DT (2000) *Fundamentals of Physical Acoustics* Wiley, John & Sons, Inc., New York.

Blauert J (1997) *Spatial hearing (revised edition)* MIT Cambridge, MA, MA.

Blum JJ, Reed MC (1991) Further studies of a model for azimuthal encoding: Lateral superior olive neuron response curves and development processes. *J. Acoust. Soc. Am.* 90(4):1968–1978.

Boahen K (2005) Neuromorphic microchips. *Scientific American* 292(5):56–63.

Boahen KA (1997) The retinomorphic approach: adaptive pixel-parallel amplification, filtering, and quantization. *Journal of Analog Integrated Circuits and Signal Processing* 13:53–68.

Boahen KA (2000) Point-to-point connectivity between neuromorphic chips using address-events. *IEEE Trans. Circuits Syst. II* 47:416–434.

Boegerhausen M, Suter P, Liu S (2003) Modeling short-term synaptic depression in silicon. *Neural Computation* 15:331–348.

Boudreau JC, Tsuchitani C (1968) Binaural interaction in the cat superior olivary s-segment. *J. Neurophysiol.* 31:442–454.

Brugge JF (1992) An overview of central auditory processing. In Fay RR, Popper AN, editors, *The Mammalian Auditory Pathway: Neurophysiology*, pp. 1–33. Springer-Verlag, New York.

Brugge JF, Reale RA, Hin J (1996) The structure of spatial receptive fields of neurons in primary auditory cortex of the cat. *J. Neurosci.* 16:4420–4437.

Burger RM, Pollak GD (2001) Reversible inactivation of the dorsal nucleus of the lateral lemniscus reveals its role in the processing of multiple sound sources in the inferior colliculus of bats. *J. Neurosci.* 21:4830–4843.

Cash S, Yuste R (1998) Input summation by cultured pyramidal neurons is linear and position-independent. *J. Neurosci.* 18:10–15.

Chase SM, Young ED (2006) Spike-timing codes enhance the representation of multiple simultaneous sound-localization cues in the inferior colliculus. *J. Neurosci.* 26(15):3889–3898.

Cheely M, Horiuchi T (2003) Analog VLSI models of range-tuned neurons in the bat echolocation system. *EURASIP Journal, Special Issue on Neuromorphic Signal Processing and Implementations* 7:649–658.

Cheng CI, Wakefield GH (2001) Introduction to head-related transfer functions (HRTFs): representations of HRTFs in time, frequency, and space. *J. Audio Eng. Soc.* 49:231–249.

Covey E (1993) Response properties of single units in the dorsal nucleus of the lateral lemniscus and paralemniscal zone of an echolocating bat. *J. Neurophysiol.* 69:842–859.

Covey E (2000) Neural population coding and auditory temporal pattern analysis. *Physiology & behavior* 69:211–220.

Covey E, Casseday JH (1995) The lower brainstem auditory pathways. In Popper AN, Fay RR, editors, *Hearing by Bats. Springer Handbook of Auditory Research*, pp. 235–295. Springer-Verlag, New York.

Covey E, Vater M, Casseday JH (1991) Binaural properties of single units in the superior olivary complex of the mustached bat. *J. Neurophysiol.* 66:1080–1093.

Dayan P, Abbott LF (2001) *Theoretical Neuroscience* MIT Press, Cambridge, MA page 18.

Deiss S, Douglas R, Whatley A (1999) A pulse-coded communications infrastructure for neuromorphic systems In Mass W, Bishop C, editors, *Pulsed Neural Networks*, pp. 157–178. MIT Press, Cambridge, MA.

Destexhe A, Mainen ZF, Sejnowski TJ (1994a) An efficient method for computing synaptic conductances based on a kinetic model of receptor binding. *Neural Computation* 6:14–18.

Destexhe A, Mainen ZF, Sejnowski TJ (1994b) Synthesis of models for excitable membranes, synaptic transmission and neuromodulation using a common kinetic formalism. *Journal of Computational Neuroscience* 1:195–230.

Duda RO, Martens WL (1998) Range dependence of the response of a spherical head model. *J. Acoust. Soc. Am.* 104(5):3048–3058.

Eggermont JJ (1998) Azimuth coding in primary auditory cortex of the cat. ii. relative latency and interspike interval representation. *J. Neurophysiol.* 80:2151–2161.

Evans EF (1975) Cochlear nerve and cochlear nucleus. In Keidel W, Neff WD, editors, *Handbook of Sensory Physiology, Vol. 5/2*, pp. 1–108. Springer Verlag, Berlin, second edition.

Ferragamo MJ, Haresign T, Simmons JA (1998) Frequency tuning, latencies, and responses to frequency-modulated sweeps in the inferior colliculus of the echolocating bat, *Eptesicus fuscus*. *J Comp Physiol [A]* 182(1):65–79.

Frey DR (1996) Exponential state space filters: A generic current mode design strategy. *IEEE Trans. Circuits Syst. I* 43:34–42.

Furukawa S, Middlebrooks J (2002) Cortical representation of auditory space: information-bearing features of spike patterns. *J. Neurophysiol.* 87:1749–1762.

Fusi S, Mattia M (1999) Collective behavior of networks with linear (VLSI) integrate-and-fire neurons. *Neural Computation* 11:633–652.

Fuzessery ZM, Pollak GD (1985) Determinants of sound location selectivity in bat inferior colliculus: a combined dichotic and free-field stimulation study. *J. Neurophysiol.* 54:757–781.

Gerstner W, Kistler WM (2002) *Spiking Neuron Models: Single Neurons, Populations, Plasticity* Cambridge University Press, Cambridge, UK.

Goldberg JM, Brown PB (1969) Response of binaural neurons of dog superior olivary complex to dichotic tonal stimuli: some physiological mechanisms of sound localization. *J. Neurophysiol.* 32(4):613–636.

Griffin DR (1944) Echolocation in blind men, bats, and radar. *Science* 100:589–590.

Grinnell AD (1995) Hearing in bats: an overview In Popper AN, Fay RR, editors, *Hearing by Bats. Springer Handbook of Auditory Research*, pp. 1–36. Springer-Verlag, New York.

Grothe B, Covey E, Casseday JH (1996) Spatial tuning of neurons in the inferior colliculus of the big brown bat: effects of sound level, stimulus type and multiple sound sources. *J. Comp. Physiol. A Sens. Neural Behav. Physiol.* 179:89–102.

Hafliger P, Mahowald M, L.Watts (1997) A spike based learning neuron in analog VLSI In Mozer MC, Jordan MI, Petsche T, editors, *Advances in Neural Information Processing Systems*, Vol. 9, pp. 692–698. MIT Press, Cambridge, MA.

Harnischfeger G, Neuweiler G, Schlegel P (1985) Interaural time and intensity coding in superior olivary complex and inferior colliculus of the echolocating bat *Molossus ater*. *J Neurophysiol.* 53:89–109.

Heil P (2004) First-spike latency of auditory neurons revisited. *Current Opinion in Neurobiology* 14:461–467.

Horiuchi T, Koch C (1999) Analog VLSI-based modeling of the primate oculomotor system. *Neural Computation* 11(1):243–265.

Horiuchi TK (2005) "Seeing" in the dark: neuromorphic VLSI modeling of bat echolocation. *IEEE Signal Processing Magazine* 22(5):134–139.

Indiveri G (2002) Neuromorphic bistable VLSI synapses with spike-timing-dependent plasticity In Mozer MC, Jordan MI, Petsche T, editors, *Advances in Neural Information Processing Systems*, Vol. 15. MIT Press, Cambridge, MA.

Irvine DRF (1992) Physiology of the auditory brainstem In Fay RR, Popper AN, editors, *The Mammalian Auditory Pathway: Neurophysiology*, pp. 153–231. Springer-Verlag, New York.

Irvine DRF, Park VN, McCormick L (2001) Mechanisms underlying the sensitivity of neurons in the lateral superior olive to interaural intensity differences. *J Neurophysiol* 86:2647–2666.

Johansson RS, Birznieks I (2004) First spikes in ensembles of human tactile afferents code complex spatial fingertip events. *Nat. Neurosci.* 7:170–177.

Joris PX, Yin TCT (1998) Envelope coding in the lateral superior olive. III. comparison with afferent pathways. *J. Neurophysiol.* 79:253–269.

Klug A, Park TJ, Pollak GD (1995) Glycine and GABA influence binaural processing in the inferior colliculus of the mustache bat. *J. Neurophysiol.* 74:1701–1713.

Klug A, Khan A, Burger RM, Bauer EE, Hurley LM, Yang L, Grothe B, Halvorsen MB, Park TJ (2000) Latency as a function of intensity in auditory neurons: influences of central processing. *Hearing Research* 148:107–123.

Koch C (1999) *Biophysics of Computation: Information Processing in Single Neurons* Oxford University Press, New York.

Lazzaro J, Mead C (1989) A silicon model of auditory localization. *Neural Computation* 1:41–70.

Lazzaro JP, Wawrzynek J (1994) Low-power silicon axons, neurons, and synapses In Zaghloul ME, Meador JL, Newcomb RW, editors, *Silicon Implementations of Pulse Coded Neural Networks*, pp. 153–164. Kluwer Academic Publishers, Norwell, MA.

Liu SC, Kramer J, Indiveri G, Delbruck T, Douglas R (2002) *Analog VLSI: Circuits and Principle* The MIT Press, Cambridge, MA.

Liu W, Andreou AG, Goldstein MH (1992) Voiced-speech representation by an analog silicon model of the auditory periphery. *IEEE Trans. Neural Networks* 3:477 – 487.

Llano DA, Feng AS (2000) Computational models of temporal processing in the auditory thalamus. *Biol. Cybern.* 83:419–433.

Lu Y, Jen PS, Wu M (1998) GABAergic disinhibition affects responses of bat inferior collicular neurons to temporally patterned sound pulses. *J. Neurophysiol.* 79:2303–2315.

Lyon RF, Mead C (1988) An analog electronic cochlea. *IEEE Trans. Acoust., Speech, Signal Processing* 36:1119 – 1134.

Maass W (1997) Networks of spiking neurons: the third generation of neural network models. *Neural Networks* 10:1659–1671.

Maass W (1999) Computing with spiking neurons In Maass W, Bishop CM, editors, *Pulsed Neural Networks*, pp. 55–85. MIT Press, Cambridge, MA.

Mahowald M (1994) *An Analog VLSI System for Stereoscopic Vision* Kluwer Academic, Norwell, MA.

Markovitz NS, Pollak GD (1994) Binaural processing in the dorsal nucleus of the lateral lemniscus. *Hear. Res.* 73:121–140.

McEwan A, van Schaik A (2000) A silicon representation of the Meddis inner hair cell model In *Proceedings of the ICSC Symposia on Intelligent Systems & Application (ISA'2000)* paper 1544-078.

Mead C (1989) *Analog VLSI and Neural Systems* Addison-Wesley, Reading, MA.

Mead C (1990) Neuromorphic electronic system In *Proc. IEEE*, Vol. 78 (10), pp. 1629–1636.

Mehrotra K, Mohan CK, Ranka S (2000) *Elements of Artificial Neural Networks* MIT Press, Cambridge, MA, second edition.

Merolla PA, Boahen K (2006) Dynamic computation in a recurrent network of heterogeneous silicon neuron In *IEEE International Symposium on Circuits and Systems.* In press.

Mortara A (1998) A pulsed communication/computation framework for analog VLSI perceptive systems In Land TS, editor, *Neuromorphic Systems Engineering*, pp. 217–228. Kluwer Academic Publishers, Norwell, MA.

Moss CF, Schnitzler HU (1995) Behavioral studies of auditory information processing. In Popper AN, Fay RR, editors, *Hearing by Bats. Springer Handbook of Auditory Research*, pp. 87–145. Springer-Verlag, New York.

Moss CF, Sinha SR (2003) Neurobiology of echolocation in bats. *Current Opinion in Neurobiology* 13:751–758.

Park TJ (1998) IID sensitivity differs between two principle centers in the interaural intensity difference pathway: the LSO and the IC. *J. Neurophysiol.* 79:2416–2431.

Park TJ, Grothe B, Pollak GD, Schuller G, Koch U (1996) Neural delays shape selectivity to interaural intensity differences in the lateral superior olive. *J. Neurosci.* 16:6554–6566.

Park TJ, Monsivais P, Pollak GD (1997) Processing of interaural intensity differences in the LSO: role of interaural threshold differences. *J. Neurophysiol.* 77:2863–2878.

Park TJ, Pollak GD (1993) GABA shapes sensitivity to interaural intensity disparities in the mustache bat s inferior colliculus: Implications for encoding sound location. *J. Neurosci.* 13:2050–2067.

Park TJ, Pollak GD (1994) Azimuthal receptive fields are shaped by gabaergic inhibition in the inferior colliculus of the mustache bat. *J. Neurophysiol.* 72:1080–1102.

Pollak GD, Burger RM, Klug A (2003) Dissecting the circuitry of the auditory system. *Trends Neurosci.* 26(1):33–39.

Pollak GD, Marsh DS, Bodenhamer R, Souther A (1977) Echo-detecting characteristics of neurons in the inferior colliculus of unanesthe- tized bats. *Science* 196:675–678.

Pollak GD, Marsh DS, Bodenhamer R, Souther A (1978) A single-unit analysis of inferior colliculus in unanesthetized bats: response patterns and spike-count functions generated by constant-frequency and frequency-modulated sounds. *J. Neurophysiol.* 41(3):677–691.

Pollak GD (1988) Time is traded for intensity in the bat's auditory system. *Hear. Res.* 36:107–124.

Pollak GD, Burger RM, Park TJ, Klug A, Bauer EE, Park TJ (2002) Roles of inhibition for transforming binaural properties in the brainstem auditory system. *Hearing Research* 168:60–78.

Pollak GD, Park TJ (1995) The inferior colliculus In Popper AN, Fay RR, editors, *Hearing by Bats. Springer Handbook of Auditory Research*, pp. 296–367. Springer-Verlag, New York.

Rall W (1967) Distinguishing theoretical synaptic potentials computed for different soma-dendritic distributions of synaptic inputs. *J. Neurophys.* 30:1138–1168.

Rasche C, Hahnloser RHR (2001) Silicon synaptic depression. *Biol. Cybern.* 84:57–62.

Reed MC, Blum JJ (1990) A model for the computation and encoding of azimuthal information by the lateral superior olive. *J. Acoust. Soc. Am.* 88:1442–1453.

Reed MC, Blum JJ (1999) Model calculations of steady-state responses to binaural stimuli in the dorsal nucleus of the lateral lemniscus. *Hear. Res.* 136:13–28.

Rieke F, Warland D, de Ruyter van Steveninck R, Bialek W (1997) *Spikes. Exploring the Neural Code* MIT Press, Cambridge.

Sachs MB, Abbas PJ (1974) Rate versus level functions for auditory-nerve fibers in cats: tone-burst stimuli. *J. Acoust. Soc. Am.* 56:1835–1847.

Sanes DH (1990) An in vitro analysis of sound localization mechanisms in the gerbil lateral superior olive. *J. Neurosci.* 10:3494–3506.

Sarpeshkar R (2006) Brain power: Borrowing from biology makes for low-power computing. *IEEE Spectrum* 43(5):24–29.

Sarpeshkar R, Lyon RF, Mead C (1998) A low-power wide-dynamic-range analog VLSI cochlea. *Analog Integrated Circuits and Signal Processing* 16(3):245–274.

Schlegel PA (2002) Encoding of sound motion by binaural brainstem units in a Horseshoe bat. *Neurosci Res.* 43:343–362.

Seevinck E (1990) Companding current-mode integrator: A new circuit principle for continuous time monolithic filters. *Electron. Letts.* 26:2046–2047.

Shackleton TM, McAlpine D, Palmer AR (2000) Modeling convergent input onto interaural-delay-sensitive inferior colliculus neurones. *Hearing Research* 149:199–215.

Shepherd GM (1979) *The Synaptic Organization of the Brain* Oxford University Press, New York, second edition.

Shi RZ, Horiuchi T (2004) A summating, exponentially-decaying CMOS synapse for spiking neural systems In Thrun S, Saul L, Schölkopf B, editors, *Advances in Neural Information Processing Systems*, Vol. 16, pp. 1003–1010. MIT Press, Cambridge, MA.

Surlykke A, Moss CF (2000) Echolocation behavior of big brown bats, *Eptesicus fuscus*, in the field and the laboratory. *J. Acoust. Soc. Am.* 108:2419–2429.

Szalisznyó K (2006) Role of hyperpolarization-activated conductances in the lateral superior olive: a modeling study. *J. Comput. Neurosci.* 20(2):137–152.

Tsividis Y (1997) Externally linear, time-invariant systems and their application to companding signal processors. *IEEE Trans. Circuits Syst. II* 44:65–85.

van Schaik A, Fragniere E, Vittoz E (1996) Improved silicon cochlea using compatible lateral bipolar transistors In Touretzky DS, Mozer MC, Hasselmo ME, editors, *Advances in Neural Information Processing Systems*, Vol. 8, pp. 671–677. MIT Press, Cambridge, MA.

van Schaik A, Meddis R (1999) Analog very large-scale integrated (VLSI) implementation of a model of amplitude-modulation sensitivity in the auditory brainstem. *J Acoust. Soc. Am.* 105 (Pt. 1):811–821.

Vittoz EA, Fellrath J (1977) CMOS analog integrated circuits based on weak inversion operation. *IEEE J. Solid-State Circuits* 12:224–231.

Watts L, Kerns DA, Lyon RF, Mead CA (1992) Improved implementation of the silicon cochlea. *IEEE J. Solid-State Circuits* 27:692 – 700.

Wenstrup JJ, Fuzesserty ZM, Pollak GD (1988) Binaural interactions in the mustache bat's inferior colliculus. II. determinants of spatial responses among 60-khz EI units. *J. Neurophysiol.* 60:1384–1404.

Wenstrup JJ, LS LSR, Pollak GD (1986) Binaural response organization within a frequency-band representation of the inferior colliculus: implications for sound localization. *J. Neurosci.* 6:962–973.

Wilson WW, O'Neill WE (1998) Auditory motion induces directionally dependent receptive field shifts in inferior colliculus neurones. *J. Neurophysiol.* 79:2040–2062.

Wittig JHJ, Boahen K (2006) Silicon neurons that phase-lock In *IEEE International Symposium on Circuits and Systems.* In press.

Yang L, Pollak GD (1994) The roles of GABAergic and glycinergic inhibition on binaural processing in the dorsal nucleus of the lateral lemniscus of the mustache bat. *J. Neurophysiol.* 71:1999–2013.

Yang L, Pollak GD (1998) Features of ipsilaterally evoked inhibition in the dorsal nucleus of the lateral lemniscus. *Hear. Res* 122:125–141.

Yin T (2002) Neural mechanisms of encoding binaural localization cues in the auditory brainstem In Oertel D, Popper AN, Fay RR, editors, *Integrative functions in the mammalian auditory pathway*, pp. 99–159. Springer-Verlag, New York.

Yin TCT, Hirsch JA, Chan JCK (1985) Responses of neurons in the cat's superior colliculus to acoustic stimuli. II. A model of interaural intensity sensitivity. *J. Neurophysiol.* 53:746–758.

Zacksenhouse M, Johnson DH, Williams J, Tsuchitani C (1998) Single-neuron modeling of LSO unit responses. *J. Neurophysiol.* 79:3098–3110.

Zhou X, Jen PS (2004) Azimuth-dependent recovery cycle affects directional selectivity of bat inferior collicular neurons determined with sound pulses within a pulse train. *Brain Res.* 1019:281–288.