# PULSED POWER SWITCHING OF A 4 MM x 4 MM SIC THYRISTOR

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### Abstract

While silicon carbide (SiC) is beginning to make its way into the low voltage (300-1200 V) commercial power diode market, its capabilities in pulse power applications have yet to be proven. A previous investigation by the U.S. Army Research Laboratory (ARL) of SiC GTOs suggested that this emerging technology could provide pulsed current densities 40 to 60 times greater than is obtainable in silicon-based switches [1]. This study continues that earlier work by examining 4 mm x 4 mm 4H-SiC thyristors designed by CREE Inc. to reach 1 kV and 4 kA. These devices were successfully switched up to 3.89 kA with a current density reaching 56.1 kA/cm<sup>2</sup>, a specific rate-of-current-rise of 49 kA/µs/cm<sup>2</sup> (for peak rise-time 7.8 kA/us) and a pulse-width ranging from 2.0  $\mu$ s to 2.6  $\mu$ s. The thyristors were tested at both single shot and repetitive switching rates up to 5 Hz. Device characteristics were mapped on a curve tracer at different stages of testing, and the failure of each thyristor was analyzed.

### I. INTRODUCTION

Silicon carbide (SiC) is recognized as a possible replacement for silicon in multiple electronics applications because of its electrical and material characteristics. 4H-SiC has a higher saturation level of electron mobility (along the c-axis, on which bilayers of Si and C are stacked) and greater temperature tolerance (thermal conductivity of 3.0-3.8 W/cm<sup>•</sup>K), as well as high electric breakdown strength ( $2.2x10^6$  V/cm parallel to the c-axis at 1 kV) [2].

The performance of the SiC thyristors characterized in this study should be an improvement on that of the earlier generation of SiC GTOs evaluated at ARL. These thyristors are optimized for turn-on, associated with more rapidly spreading current and heat dissipation [3, 4]. Also, their increased size allows a greater area of current flow, raising both the peak attainable current and maximum rise-time for a single device.

## **II. EXPERIMENTAL PROCEDURE**

#### A. Device Design

The thyristors tested in this study have a 4H-SiC layered structure and an interdigitated anode and gate design (which is shown in figure 1). The active area of the mesa is  $0.07 \text{ cm}^2$ . They turn on with a negative current applied to the gate relative to the anode.



Figure 1. Interdigitated anode and gate design by Cree, Inc.

Devices were characterized on a programmable curve tracer prior to circuit testing. They had a typical anode-gate forward voltage drop of 2.6-2.8 V and a reverse anode-gate voltage holdoff of at least 17 V. The best devices started with anode-to-cathode current leakage of less than 5  $\mu$ A at 1000 V, but since circuit testing to peak current need not exceed 700 V, devices that showed small leakage at lower voltage levels were also used.



Figure 2. Packaged SiC thyristor.

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The devices characterized were obtained from three CREE Inc. wafers and packaged at ARL (as shown in figure 2). The pitches, or distances between repeating gate patterns, varied among 25  $\mu$ m, 28  $\mu$ m, and 40  $\mu$ m. The wafer number and pitch did not seem to affect the test results obtained for each thyristor, though those probetested within the wafers above 1100 V at CREE were able to reach higher voltage and current levels in the circuit. The interior package space around the bond wires and the die was filled with a silicon-based potting compound to ensure voltage isolation.

### **B.** Device Evaluation

The evaluation circuit was originally designed to reach a peak current of 4 kA at 1 kV with a 50% pulse-width of 2-3  $\mu$ s. After preliminary thyristor testing, the circuit was redesigned to reach the peak current at a lower voltage level with roughly the same pulse-width to ensure that the applied voltage was not limiting device performance. A schematic of this layout can be seen in figure 3. A photo of the circuit is shown in figure 4.



Figure 3. Schematic of the testing circuit.



Figure 4. View of the testing circuit.

Four paralleled capacitors provided 20  $\mu$ F of storage. A 1 kV, 20 mA power supply was used to charge the capacitors through a protective diode and a charging resistor of 6.25 kΩ. For each shot, a 5  $\mu$ s signal was sent to the driver board which then applied a maximum anode-to-gate current of 1.2 A. The anode and gate connections were tied by 5 Ω of resistance. The capacitors discharged through the switch into a load of 0.11 Ω. The goal for the first stage of testing was to determine the peak attainable current for these devices. The goal for the second stage of testing was to see how many high current pulses the thyristors could survive at repetitive rates.

To establish the peak current for these devices, ten thyristors were tested by increasing  $V_{AK}$  in 50 V increments until failure. Current and rise-time values were relatively constant at a given voltage during testing of each device, but the maximum voltage or current that each individual switch could survive varied. The devices were removed from the circuit and characterized on a curve tracer at regular intervals to monitor degradation. Failure was defined as the point at which the thyristor would begin to self-trigger or when the anode-cathode leakage current began to limit voltage held by the capacitors.

Testing at a repetitive rate was conducted up to 5 Hz at various currents in the same circuit configuration. Eight thyristors were evaluated during this stage of analysis. The charging resistance was decreased to 5 k $\Omega$  for more rapid charging. After every 1000 shots, a thyristor was characterized with the curve tracer. Switching waveforms were captured using an oscilloscope, and at the end of each stage of testing, data from all thyristors were compared and analyzed.

## **III. RESULTS AND DISCUSSION**

### A. Single-shot Data

The measurements monitored during each test shot included the differential voltage from anode to cathode, the voltage drop across the load resistor, and the gate current. The maximum anode voltage applied in the final circuit design of Figure 3 was 660 V. The maximum voltage measured across the load during that test was 430 V. This value was divided by the load resistance (0.11  $\Omega$ ) to calculate a peak current of 3.9 kA. A graph of this maximum current data may be seen in figure 5.



Figure 5. Peak current reached with SiC thyristor.

Overwhelming anode-cathode leakage current would not allow the applied voltage to be raised any higher, and the 660 V shot was repeated once before the switch began to self-trigger. The maximum 10%-90% rise-time of current was 7.8 kA/µs or 49 kA/µs/cm<sup>2</sup>.

The anode to gate current utilized for triggering was a square wave of 1.2 A amplitude. It was noted, though,

that as anode voltage was increased from 0 V, the shape of this current waveform changed. As seen in figure 6, the initial current fell to about 600 mA and then dipped a few amperes below zero at higher voltages. The gate voltage was briefly monitored to verify that it never fell below zero. After initially floating with the anode, the gate voltage appeared to follow the cathode partway through the pulse. Since the thyristors continued to trigger properly, the gate current was left alone.



Figure 6. Changing gate current.

Table 1 shows the results of the single-shot testing for six devices.

Table 1. Single-shot test data.								
Device	Voltage	Current	<b>Rise-time</b>	Density				
Number	(V)	(A)	(kA/µs)	$(kA/cm^2)$				
219	500	2760	5.1	39.4				
3210	650	3850	7.2	55.0				
3317	450	2470	5.5	35.3				
328	660	3930	7.8	56.1				
339	550	3050	6.0	43.6				
427	600	3270	6.9	46.7				

Table 1. Single-shot test data

#### B. Repetitive-Shot Data

The SiC thyristors were pulsed at repetitive rates of 1 Hz and 5 Hz. It was found that at a peak current of 1 kA, devices could survive greater than 10,000 pulses at 1 Hz. Once current was increased to 1.5 kA or 2 kA, though. anode-to-cathode voltage holdoff usually began to drop before 1000 shots could be completed. One device (#228) was tested at a rate of 5 Hz and survived 10,000 switches at both 1 kA and 1.45 kA levels. Attempts to further decrease the charging resistor did not enable the capacitors to charge to higher voltage levels at this pulsing rate. It was decided that the limiting factor for charging was the 20 mA power supply being used for this series of tests.

Table 2 details the repetitive-shot performance of each thyristor. Current values listed varied by as much as  $\pm 70$ A from one shot to another depending on exact anode voltage.

Table 2.     Repetitive-shot test data.								
Device	Voltage	Current	# of	f				
Number	(V)	(A)	Pulses	(Hz)				
413	100	500	1000	1				
"	200	1000	1000	1				
"	280	1500	1000	1				
"	370	2000	1000	1				
438	200	1000	1000	1				
218	280	1500	1000	1				

1000

1000

1450

3000

2000

10.000

10.000

10,000

1

1000

1

5

5

1

1

228

"

2322

327

V.

200

200

270

550

370

370 2000 1000 338 1 211 370 2000 94 1 Pulsing at currents above 1 kA likely accelerated device degradation because the linear increase in energy would generate excess heat in the SiC material that could not escape the packaging. This, in turn, would reduce voltage holdoff. It was noted, for example, that at shot #1000 with device #327, the peak current was only 1930 A instead of the intended 2 kA. This drop in load current can be seen in the graph of figure 7. The capacitors in the test circuit could not maintain the 370 V being applied. When #327 was subsequently characterized on the curve tracer, it revealed that it was already leaking 200 µA of current with only 45 V applied at the anode, suggesting milliamperes of anode-to-cathode current leakage at 370



Figure 7. Changing load current of device #327 as a function of pulse accumulation.

One thyristor (#211) was packaged and tested without any of the silicon-based potting compound to try to determine whether thermal insulation from the compound was a limiting factor in testing. Initial curve tracer testing showed that the device could handle at least 650 V without any arcing. When pulsed at 1 Hz at 2 kA, device #211 began self triggering at a lower voltage after 94 intentional pulses. Analysis on the curve tracer showed the anode-gate junction and the anode-cathode junction

were nearly shorted. Further testing with unpotted devices and more efficient heat sinking is planned.

#### C. Failure Analysis

Single-shot testing of the thyristors continued until each device failed in the circuit. Successful switching at a given current was followed by a drop in anode holding voltage, and the device would begin to self-trigger. When returned to the curve tracer, the thyristor would show a large increase in the slope of the anode-cathode leakage current, in some cases leaking 50 µA at applied voltages under 10 V. This increase in leakage current was gradual as the thyristors were tested at higher and higher applied voltages, but once a peak voltage and current were reached, the degradation rate became more severe. Figure 8 depicts this form of degradation. Avalanching anodecathode leakage seems to be the main source of damage and in some thyristors it resulted in anode-gate shorting within the device because of the anode and gate being tied at the driver. Prior to testing, device #339 had no anodecathode leakage current until beyond 1000 V. After circuit testing up to 300 V (1.6 kA), the thyristor was returned to the curve tracer and showed leakage of about 1  $\mu$ A at an applied voltage of 1000 V. After testing up to 500 V (2.8 kA), the leakage was up to 10 µA at only 330 V. The device failed after one 550 V (3.1 kA) test shot and behaved like a resistor with a voltage/current slope of 1.2 V/100  $\mu$ A, or the equivalent of 12 k $\Omega$ .



Figure 8. Increasing anode-cathode leakage for device #339.

Repetitive-shot testing of the thyristors generally continued until each device's characterized anode-cathode leakage was judged to be too great for another thousand test shots at the chosen level. Devices #2322 and #211 (as listed in table 2) failed in the midst of testing. The former thyristor mentioned was the only one used to attempt pulsing at 3 kA and 1 Hz. Considering that some devices survived single shots at greater currents, it is likely that in this case, failure after one 3 kA shot was the result of an issue particular to this device, such as expanding micropipes [1, 2]. The failure of the unpotted device #211 could have been for the same reason, but more unpotted devices will be tested for further analysis. Device degradation was minimal when pulsed at 1 kA at both 1 Hz and 5 Hz. When profiled on the curve tracer prior to testing, switch #438 already showed 14  $\mu$ A of anode-cathode leakage, so its poor performance at 1 kA cannot be compared to that of devices #413 and #228, which started off fully-blocking up to 1000 V.

The fact that thyristor #228 survived tens of thousands of pulses at 1 kA without detrimental degradation further suggests that the effects of increasing current are more damaging to the devices than the number or the frequency of pulses. The short pulse-width used in this study and the rapid heat dissipation of the SiC material allow for repetitive pulsing, while the peak power limits single-shot performance of the devices.

### **IV. SUMMARY**

The purpose of this study was to determine the pulsed switching capabilities of the 4 mm x 4 mm SiC thyristor. The peak single shot performance was 3.9 kA of current with a peak power of 540 kW and a current density of 56.1 kA/cm<sup>2</sup>. The best rise-time attained was 7.8 kA/µs or 49 kA/µs/cm<sup>2</sup>. Successful repetitive rate testing of 10,000 shots was completed up to 5 Hz and 1.45 kA. While the peak current and rise-time met initial goals, it was hoped that the thyristors could be pushed to higher current densities and repetitive-rate current levels. Testing continues with these ambitions in mind. Ultimately, it is desirable to model the heat dissipation, vary the pulse-width and rise-time, and improve packaging for higher levels of dissipation to further study the limits of these SiC thyristors.

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#### **VI. REFERENCES**

 S.B. Bayne and D. Ibitayo, "Evaluation of SiC GTOs for Pulse Power Switching," 14<sup>th</sup> IEEE International Pulsed Power Conference, June 15-18, 2003, pp. 135-138.
"Silicon Carbide Substrates: Product Specifications," Cree, Inc., Durham, NC, Version MAT-CATALOG.00D, Revised Jan. 2005.

[3] B. Jayant Baliga, Power Semiconductor Devices. Boston: PWS Publishing Co., 1996.

[4] S. H. Ryu, A. K. Agarwal, R. Singh and J. W. Palmour, "3100 V, Asymmetrical, Gate Turn-Off (GTO) Thyristors in 4H-SiC," IEEE Electron Device Letters, vol. 22, pp. 127-129, 2001.