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14. ABSTRACT
This project has investigated fundamental physics of electron energy filtering occurring at room temperature as well as its applications to practical devices such as room-temperature single-electron transistors and ultralow energy consumption transistors. We have experimentally demonstrated, for the first time, that a quantum well energy level can filter out energetic electrons that are present at the Fermi-Dirac distribution tail, thereby effectively suppress the Fermi-Dirac electron thermal excitations, producing energy-filtered cold electrons at room temperature. The effective temperature of the energy-filtered cold electrons was 45 Kelvin at room temperature. A comprehensive microscopic model has been developed to describe the underlying mechanisms of the energy filtering and numerical calculations are in excellent agreement with experimental findings. The energy filtering has been applied to single-electron transport and clear Coulomb staircases and Coulomb oscillations have been demonstrated at room temperature. A new architecture of energy-filtered cold electron transistors has been designed and fabricated using optimized materials/processes.

15. SUBJECT TERMS
Electron energy filtering, Cold-electron transport, quantum well, quantum dot, single-electron transistor, tunnel transistor, energy-efficient electronics

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ONR Final Report

Energy-Filtered Tunnel Transistor: A New Device Concept Toward Extremely-Low Energy Consumption Electronics

(Grant No: N00014-12-1-0492)

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I. Introduction and Background

Excessive heat dissipation (or power consumption) of modern integrated circuits is an undesirable effect that imposes substantial limitations on functioning of many electronic devices. For example, the level of heat dissipation/power consumption of smart phones, tablets, and laptops is such that it prohibits a continuous and prolonged operation of these devices, requiring a frequent recharging (*e.g.*, once a day). A large power consumption of electronic devices requires large energy storage in batteries, increasing the battery weights that soldiers carry in their missions or the weights of remote controlled equipment such as unmanned aerial vehicles (UAVs). Therefore, a technology that enables electronic devices to operate with extremely small energy consumption promises a broad range of commercial, military and space applications.

The root cause of heat dissipation of the current metal-oxide-semiconductor field-effect transistors (MOSFETs) is the thermal excitation of electrons that obeys thermodynamics, *i.e.*, the Fermi-Dirac energy distribution of electrons. The thermally excited electrons at the tail of the Fermi-Dirac distribution can overcome the energy barrier set in the OFF state of the MOSFETs. This causes substantial OFF state leakage currents even after the gate voltage is reduced below the threshold voltage, resulting in large heat dissipation or energy consumption for integrated circuits. The challenge for this large heat dissipation is that its root cause is an intrinsic phenomenon of thermodynamics (Fermi-Dirac distribution) that cannot be directly manipulated.

Previous studies have demonstrated that it is possible to indirectly suppress electron thermal excitations by utilizing discrete energy levels present in quantum dots (QDs)[1-3]. Here the electrons are made to pass through the QD energy level and this discrete level serves as an energy filter, allowing only those electrons whose energies match with the discrete QD level to pass through. It has been experimentally demonstrated that this energy filtering can lower the effective temperature of electrons. Until now, the energy filtering has been demonstrated only when the entire system is cooled to very low temperatures, typically below 1 Kelvin. For practical applications, however, the energy filtering and effective suppression of electron thermal excitations will need to function at room temperature.

This project aimed to investigate a new method that can effectively suppress electron thermal excitations at room temperature and to fabricate device structures in which energy-suppressed cold electrons are transported through device components at room temperature. An important feature of our approach is that the quantum states for the energy filtering are formed in a quantum well of a very thin (~2 nm) layer, so that their energy level spacing is made to be much larger than the room temperature thermal energy, enabling the electron energy filtering and cold-electron transport to function even at room temperature. Fabrication of device structures that enable cold-electron transport at room temperature is demonstrated. A comprehensive microscopic model of the cold-electron transport is provided along with numerical calculations. Application of the energy-filtered cold electron transport to single-electron transistors is demonstrated. Device architecture for a large-scale fabrication of energy-filtered tunnel transistors for energy-efficient electronics is presented. Process and material developments for this transistor architecture are presented.

II. Accomplishments

II.A. Summary of Accomplishments

We have demonstrated that electron energy filtering through a quantum well energy level can effectively suppress electron thermal excitations at room temperature. The effective electron temperature from the energy filtering can reach ~45 Kelvin at room temperature without any external cooling. A comprehensive understanding for the mechanism of the cold electron transport has been made. Numerical codes for the cold-electron transport have been developed and numerical calculations have been performed. The energy-filtered cold electron transport has been applied to single-electron transistors. Clear single electron transport phenomena, Coulomb staircases and Coulomb oscillations, have been demonstrated at room temperature, in which cold electrons having effective electron temperature of ~45 K are transported in accordance with Coulomb blockade effect at room temperature. New device architecture that utilizes cold-electron transport for ultra-low energy consumption electronics has been designed in a configuration that enables a large-scale fabrication. Materials and process developments for this new device architecture have been completed. Details for these accomplishments are described below.

II.B. Experimental Demonstration of Energy-Filtered Cold Electron Transport at Room Temperature

II.B.1. Quantum Well Energy Filter Structure

An important element of our approach that makes the energy filtering possible at room temperature is that the level spacing of our quantum well energy filter is made appreciably larger (> 250 meV) than the room temperature thermal energy, ~25 meV. The large level spacing can be obtained in the quantum well if the layer thickness of the quantum well is made only of a couple of nanometers and the quantum well depth about a couple of electron volts. We have made this quantum well structure using native chromium oxide (Cr_2O_3; thickness: ~2 nm) which is in contact with a SiO_2 layer. Independent measurements have demonstrated a quantum well formation in the Cr/ Cr_2O_3/SiO_2 system with a quantum well depth of ~1 eV (see section II.D), which leads to large (>250 meV) quantum well level spacing.

We have used the quantum well energy filter structure made of $Cr/Cr_2O_3/SiO_2$ system to inject energy-suppressed electrons to discrete levels of a semiconductor nanocrystal (quantum dot: QD) and demonstrated energy-filtered cold electron transport at room temperature. The device structure used in this study is schematically displayed in Fig. 1a and its associated energy diagram in Fig. 1b. Its basic configuration is the double-barrier tunneling junction (DBTJ) structure, but the quantum well energy filter is placed between the metal electrode (Cr) and the tunneling barrier (SiO_2). The effect of energy filtering on the electron transport through QD energy levels has been investigated.

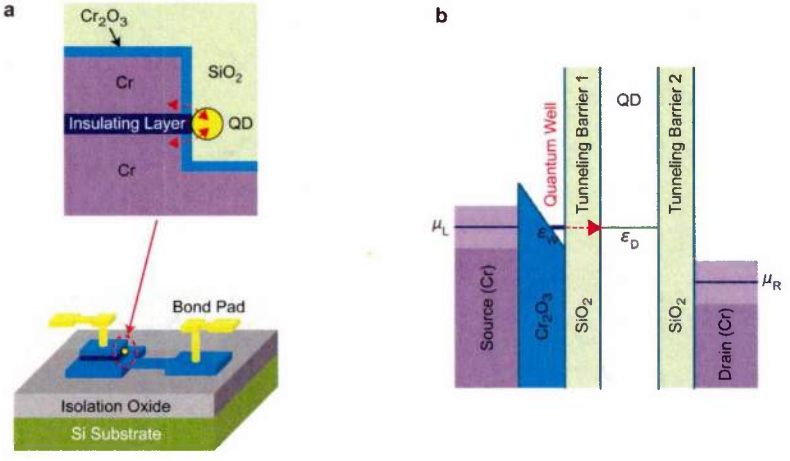

Figure 1. A device to study energy-filtered cold electron transport at room temperature. a. The device structure. **b.** Energy diagram for energy-filtered cold electron transport. The quantum well is formed in the conduction band of the Cr_2O_3 layer through band bending (detail in Section II.D) and a quantum well state serves as an energy filter.

II.B.2. *I-V* Measurements

The *I-V* measurement of the fabricated devices has demonstrated the effectiveness of the energy filtering through a quantum well energy level, Fig. 2a. The sharp current changes (indicated by the arrows in Fig. 2a) correspond to the alignment of the discrete state of the quantum well with CdSe quantum dot levels. The sharp current changes in the positive voltages come from CdSe quantum dot levels in the conduction band and those in the negative voltages from valence band levels of the CdSe quantum dot. The zero conductance region shown in the voltage range from ~-1.1 V to ~1.1 V originates from the band gap of the CdSe quantum dot. The sharp current changes demonstrate that the

electron energy filtering in our device structure is working very well at room temperature since the Fermi-Dirac thermal smearing would have wiped out the distinct current changes if it were the usual double-barrier tunneling junction device that has no energy filter. The *I-V* characteristics that would result from the usual double-barrier tunneling junctions are displayed in Fig. 2b.

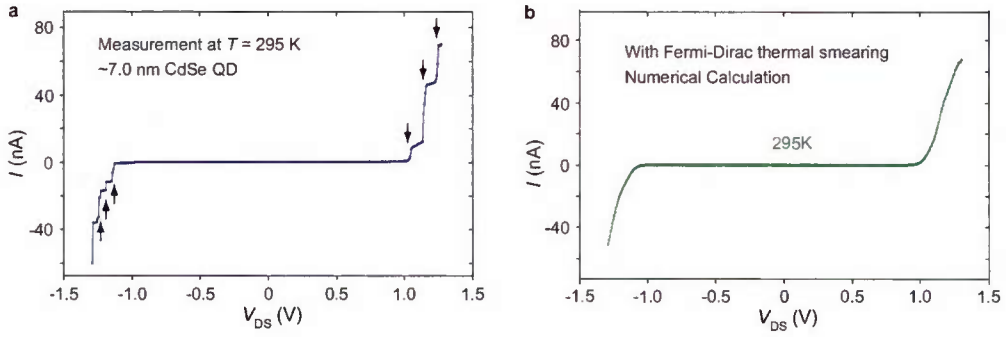

Figure 2. Demonstration of the energy-filtered cold electron transport at room temperature ~7.0 CdSe nanocrystal was used as the QD. **a.** *I-V* measurement at room temperature for the device having the quantum dot energy filter in Fig. 1. Sharp current changes (indicated by the arrows) correspond to the alignment of the discrete level of the quantum well energy filter with the energy level of the CdSe QD. The arrows in the positive voltages correspond to the alignment with the CdSe QD levels in the conduction band and those in the negative voltages correspond to the alignment with the CdSe QD levels in the valence band. The zero conductance region between ~ -1.1 V and ~1.1 V corresponds to the band gap of the ~7.0 nm CdSe QD. **b.** The calculated *I-V* for the usual double-barrier tunneling junction structure (having no energy filter) at room temperature. Due to the Fermi-Dirac thermal smearing, no sharp current changes are seen.

II.B.3. Differential Conductance (*dI/dV*) Measurements

We have also independently verified the energy-filtered cold electron transport by measuring the differential conductance using lock-in technique. The lock-in measurements directly provide the differential conductance (*dI/dV*), where the electron tunneling from a quantum well energy level to a QD state produces a peak in the *dI/dV* plot. Here the widths of the differential conductance peaks are directly related to effective temperatures of the tunneling electrons that are transported through the device components; the smaller the peak width, the lower the effective electron temperature. The differential conductance measurement for a device with a ~7 nm CdSe QD is shown in Fig. 3. Each peak corresponds to an alignment of the discrete level of the quantum well energy filter with an energy level of the CdSe QD; *s*, *p*, and *d* are for the first three CdSe QD levels in the conduction band and h_1, h_2, and h_3 are for the first three CdSe QD levels

in the valence band. We observe that the widths of the peaks are extremely small, which demonstrates the effectiveness of our energy filtering; their full widths at half maximums (FWHMs) are only ~18 meV at room temperature. It should be noted that under the usual condition of electron thermal excitation, no peaks would have existed at room temperature due to the Fermi-Dirac thermal smearing. The extremely small FWHM of ~18 meV corresponds to an effective electron temperature of ~45 Kelvin; under the usual Fermi-Dirac thermal smearing, the ~18 meV FWHM can only be achieved when the entire device is cooled to ~45 Kelvin (details on the effective electron temperature are given in Section II.B.4 and Section II.B.5). This low effective electron temperature demonstrates that our electron energy filtering through the quantum well energy state works very well at room temperature.

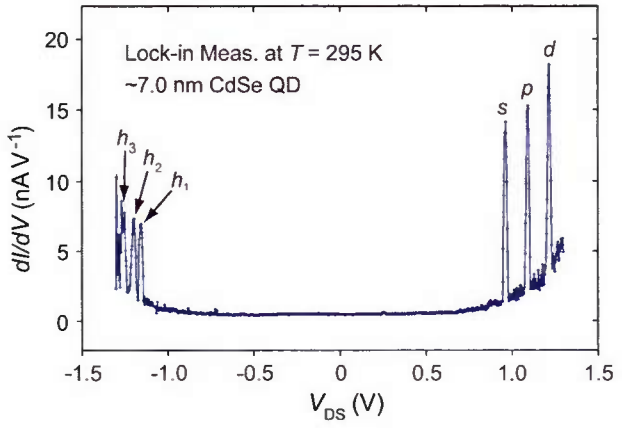

Figure 3. Differential conductance measurement for the energy-filtered cold electron transport device using the lock-in technique. Measurement was carried out at room temperature. The widths of the differential conductance peaks are extremely small; their full widths at half maximums (FWHMs) are only ~18 meV at room temperature, which demonstrates the effectiveness of the energy filtering. *s*, *p*, *d* and h_1, h_2, h_3: the first three CdSe quantum dot levels in the conduction and valence band, respectively. The extremely small FWHM of ~18 meV corresponds to an effective electron temperature of ~45 Kelvin.

The differential conductance (*dI/dV*) measurements were highly reproducible. Figure 4 displays repeated *dI/dV* measurements at room temperature for the same ~7 nm CdSe device shown in Fig. 3. The measurements were carried out many times over a period of several days. The measurements repeatedly produce the same peaks (with the same widths) in the conduction and valence bands.

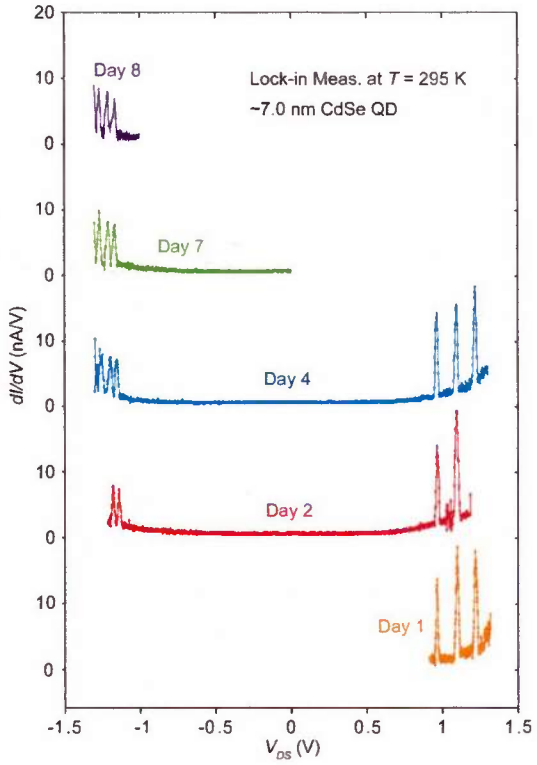

Figure 4. Reproducibility of the device characteristics of the energy-filtered cold electron devices. Differential conductance measurements (lock-in) for ~7 nm CdSe QD at room temperature. Different colors represent repeated differential conductance measurements at different times.

II.B.4. Temperature Dependence of Electron Energy Filtering

We also investigated the temperature dependence of the energy-filtered cold electron transport at varying temperatures ranging from 77 K to 295 K (here the temperature refers to the temperature of the thermal bath with which the entire device is equilibrated). Detailed experimental data on the role of the temperature were essential in obtaining comprehensive mechanical understanding for the energy-filtered cold electron transport, which will be detailed in Section II.C.

First we show in Fig. 5 the *I-V* characteristics measured at 77 K for a device unit with ~5.5 nm CdSe QD. We note that the current changes (indicated by the arrows) are more abrupt compared to those measured at room temperature shown in Fig. 2a. This indicates that the effective electron temperature becomes much smaller as the bath temperature with which the device is equilibrated is lowered to 77 K. To assess the abruptness of these current changes accurately and quantitatively, we carried out the direct differential conductance measurements using the lock-in technique at varying

temperatures ranging from 77 K to 295 K. Figure 6a displays the temperature dependence of the peak width of the differential conductance for a unit with ~7.0 nm CdSe QD. We find that for a given temperature, the peak widths remain the same for all *s*, *p*, and *d* peaks. The peak width decreases as the temperature is lowered. The same measurements were performed for a unit with ~5.5 nm CdSe QD; the peak widths are the same for a given temperature and they decrease as the temperature is lowered. We find that the FWHMs are almost the same for a given temperature without regard to the QD size and specific QD level.

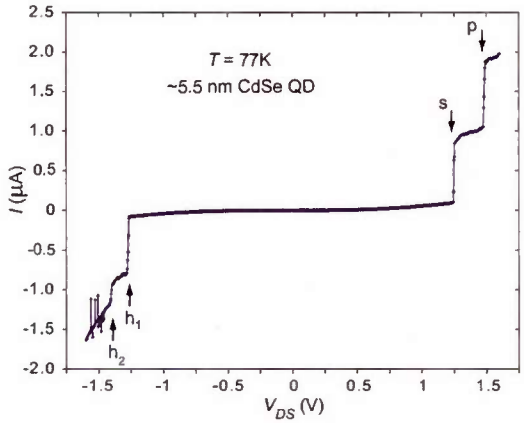

Figure 5. *I-V* characteristics for a unit with ~5.5 nm CdSe QD at 77 K. The arrows indicate the positions where abrupt changes of the electrical current occurred. More abrupt current changes (see the arrows) are observed at 77 K compared to the current changes at room temperature shown in Fig. 2a. Labels *s*, *p* and h_1, h_2 indicate the first two levels in the conduction and valence band of the CdSe QD, respectively.

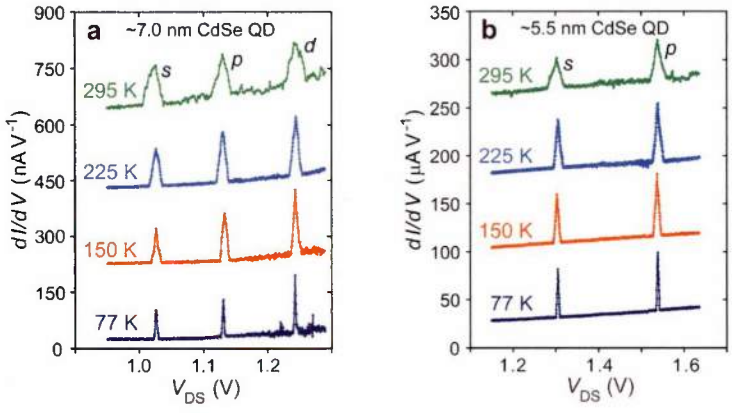

Figure 6. Temperature dependence of the widths of the differential conductance peaks. a. For a unit with ~7.0 nm CdSe QD. **b.** For a unit with ~5.5 nm CdSe QD. Peaks in the conduction band of the CdSe QD (indicated by *s*, *p*, or *d*) were examined. For a given temperature, the FWHMs of the peaks are almost the same without regard to the QD sizes (7.0 nm or 5.5 nm) and QD levels (*s*, *p*, or *d*).

The temperature dependence of the FWHMs of the differential conductance peaks in Fig. 6 is summarized in Fig. 7. We find that the FWHM decreases linearly with decreasing temperature. We note that the FWHMs are extremely small; they are ~16 meV at 295K and decrease to ~3 meV at 77K. The FWHMs in the usual double-barrier tunnel junctions are much larger (at least 6 times)[4] than those obtained in Fig. 6 and Fig. 7. The much suppressed FWHMs in Fig. 7 directly prove the much lowered electron temperatures of our fabricated devices. The effective temperatures of the energy-filtered cold electrons are detailed in the following section.

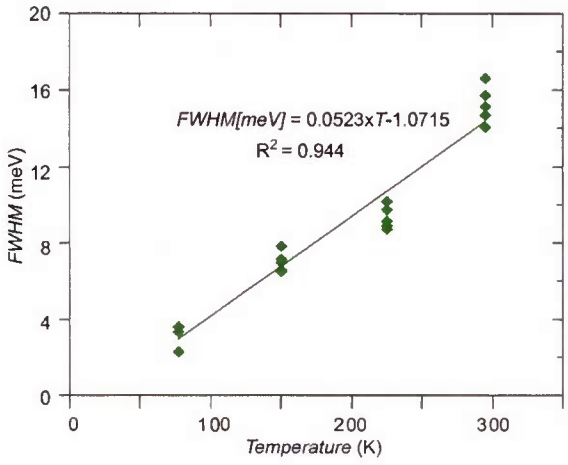

Figure 7. Temperature dependence of the FWHMs of the differential conductance peaks. The data points are from Fig. 6. A linear relationship is observed between the temperature and FWHM. The line is a linear regression fit with R^2 value of 0.944.

II.B.5. Effective Electron Temperature of Energy-Filtered Cold Electrons

The width of the differential conductance peak for the usual double-barrier tunneling junction (DBTJ) has a one-to-one relationship with the temperature (temperature of the thermal bath); the higher the temperature, the larger is the width of the differential conductance peak. Therefore, a FWHM value can be used as a direct measure for an effective electron temperature; the smaller the FWHM, the lower the effective electron temperature.

We first obtain quantitative relationships between the FWHMs and temperatures for the case of the usual DBTJ. Their energy diagrams are displayed in Fig. 8a and 8b with zero and positive source-drain biases, respectively. We first calculate its *I-V*

characteristics that would result from the Fermi-Dirac distribution of electrons. We then obtain the differential conductance *dI/dV* by differentiating the *I-V*, from which the FWHM of the *dI/dV* peak is obtained analytically. We consider the case in which there is no charge accumulation at the QD, *i.e.,* we consider the shell tunneling regime[5,6]. Since there is no charge accumulation Γ_1 is much smaller than Γ_2 (Γ_1 and Γ_2: the tunneling rate through tunneling barrier 1 and tunneling barrier 2, respectively); once an electron tunnels from the source to the QD, it tunnels out to the drain before the other electron from the source tunnels into the QD. The current is then determined by Γ_1 (the slower rate). $\Gamma_1(E,V)$, the electron tunneling rate from the source to the QD at electron energy E and voltage bias V, is given by[7]

$$\Gamma_1(E,V) = 2\frac{2\pi}{\eta}\rho_S(E)\rho_{QD}(E+\eta eV)\left|T(E)\right|^2 f(E) \qquad (1)$$

where $\rho_S(E)$ and $\rho_{QD}(E)$ are the density of states for the source electrode and the QD, respectively, $f(E)$ is the Fermi-Dirac distribution function of the source with Fermi level at μ_S, η is the voltage division factor and $\left|T(E)\right|^2$ is the tunneling transmission probability.

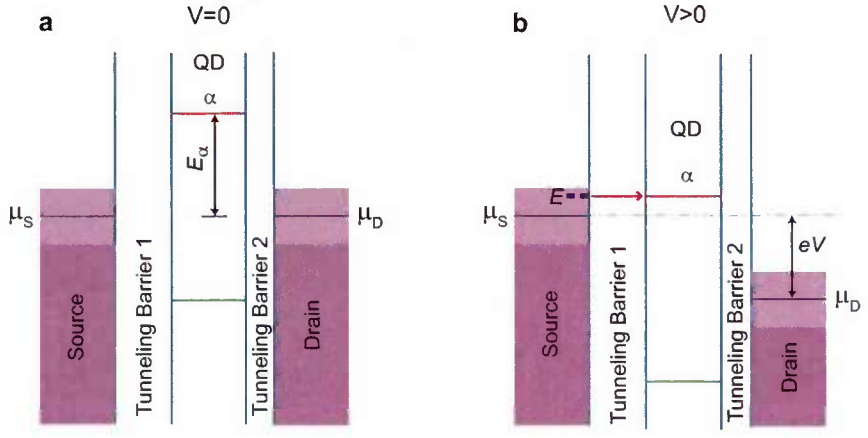

Figure 8. The energy diagram for a DBTJ at a zero voltage bias (a) and a positive voltage bias (b). The lightly shaded areas in the electrodes schematically represent the Fermi-Dirac thermal smearing at non-zero temperatures. When a voltage bias is applied as in **b**, an electron with energy E (which may be different from the source Fermi level μ_S) can tunnel into the QD if E aligns with the QD energy level α. For a bias voltage V, the voltage drops across the tunneling barrier 1 and 2 are ηV and $(1-\eta)V$, respectively, where η is the voltage division factor[5,8] ($\eta = C_2/(C_1+C_2)$, where C_1 and C_2 are the junction capacitances for barrier 1 and barrier 2, respectively).

The electrical current $I(V)$ is obtained by integrating $\Gamma_1(E,V)$ with respect to E,

$$I(V)=e\int_0^\infty \Gamma_1(E,V)dE=\frac{4\pi e}{\hbar}\int_0^\infty \rho_S(E)\rho_{QD}(E+\eta eV)|T(E)|^2 f(E)dE \quad (2)$$

where e is the charge of an electron. We simplify equation (2) by approximating $\rho_S(E)$ and $T(E)$ with $\rho_S(E_F)$ and $T(E_F)$, respectively, where E_F ($\approx\mu_S$) is the Fermi energy of the source electrode[7];

$$I(V)\cong\frac{g_0}{e}\int_0^\infty \rho_{QD}(E+\eta eV)f(E)\,dE \quad (3)$$

$$\text{where } g_0=\frac{4\pi e^2}{\hbar}\rho_S(E_F)|T(E_F)|^2 \quad (4)$$

The discrete energy level of the QD is represented by $\rho_{QD}(E)$ with the delta function,

$$\rho_{QD}(E)=\delta(E-(E_\alpha+\mu_S)) \quad (5)$$

where E_α is the energy for the QD level α (with its reference energy at μ_S; see Fig. 8a). From equations (3)-(5), we have

$$I(V)\cong\frac{g_0}{e}f(E_\alpha+\mu_S-\eta eV)=\frac{g_0}{e}\frac{1}{e^{(E_\alpha-\eta eV)/kT}+1} \quad (6)$$

Equation (6) indicates that with no electron accumulation at the QD the I-V is governed by the Fermi-Dirac distribution in the electrode. Figure 9 shows the I-V characteristics at 295 K.

Now, the differential conductance dI/dV is obtained from equation (6) as

$$\frac{dI(V)}{dV}=\frac{\eta g_0}{kT}\frac{e^{(E_\alpha-\eta eV)/kT}}{\left[e^{(E_\alpha-\eta eV)/kT}+1\right]^2} \quad (7)$$

Figure 10 shows the dI/dV. The maximum dI/dV is obtained when $V=E_\alpha/\eta e$,

$$\left(\frac{dI}{dV}\right)_{\max}=\left.\frac{dI(V)}{dV}\right|_{V=\frac{E_\alpha}{\eta e}}=\frac{1}{4}\frac{\eta g_0}{kT} \quad (8)$$

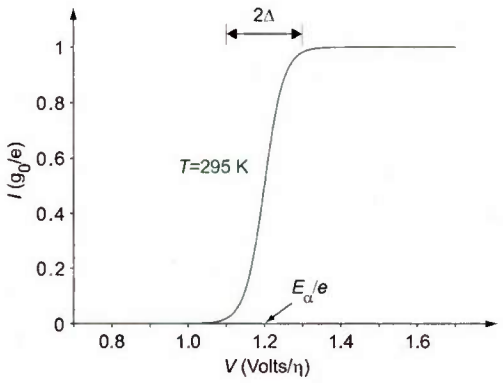

Figure 9. *I-V* characteristics resulting from the Fermi-Dirac thermal smearing. The *I-V* relationship from equation (6) with the QD energy level E_α at 1.2 eV and T = 295 K. Δ = ~90 mV.

The voltages V_{HM}^{+} and V_{HM}^{-} (see Fig. 10) that give the half of the $(dI/dV)_{max}$ can be obtained from equations (7) and (8) and solving the following equation,

$$\frac{\eta g_0}{kT}\frac{e^{(E_\alpha-\eta eV)/kT}}{\left[e^{(E_\alpha-\eta eV)/kT}+1\right]^2}=\frac{1}{2}\left(\frac{dI}{dV}\right)_{\max}=\frac{1}{2}\left(\frac{1}{4}\frac{\eta g_0}{kT}\right) \tag{9}$$

By solving equation (9), we have

$$V_{HM}^{+}=\frac{E_\alpha}{\eta e}-\frac{kT}{\eta e}\ln\left(3-2\sqrt{2}\right)$$
$$V_{HM}^{-}=\frac{E_\alpha}{\eta e}-\frac{kT}{\eta e}\ln\left(3+2\sqrt{2}\right) \tag{10}$$

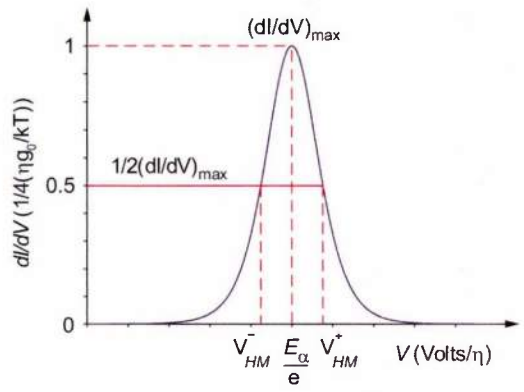

Figure 10. The differential conductance, dI(V)/dV, that results from the Fermi-Dirac thermal smearing. The dI/dV relationship from equation (7). V_{HM}^{+} and V_{HM}^{-} are the bias voltages that give the half of the maximum differential conductance value.

The FWHM (in energy unit) is then

$$FWHM = \eta e\left(V_{HM}^{+} - V_{HM}^{-}\right)$$
$$= kT[\ln(3+2\sqrt{2}) - \ln(3-2\sqrt{2})]$$
$$= 3.52549kT \qquad (11)$$

This linear relationship between FWHM and temperature, equation (11), is plotted in Fig. 11 as the blue line.

The FWHMs in Fig. 7, which were measured from the devices with the quantum well energy filter, are replotted in Fig. 11 in green. The FWHMs with energy filtering are much smaller than those with the usual Fermi-Dirac smearing. The effective electron temperatures for the devices having the energy filter can be defined as those temperatures that produce the same FWHMs under the usual Fermi-Dirac smearing. For example, the FWHM for the energy-filtered device at 295 K is ~16 meV. The same FWHM is produced for the device with the usual Fermi-Dirac smearing when the temperature is lowered to ~45K. The effective electron temperature of the energy-filtered electrons is then ~45 K at room temperature (bath temperature: 295 K).

The relationship between the effective electron temperature of the energy-filtered cold electrons and the bath temperature can be obtained as follows. From the measured FWHMs in Fig. 7, we have

$$FWHM\,[meV] = 0.0523 \times T - 1.0715 \qquad (12)$$

Then, the effective electron temperature of the energy-filtered electrons can be obtained from Equations (11) and (12) as

$$T_{eff} = [0.0523 \times T\,(\text{bath temp.}) - 1.0715]/[3.52549 \times k] \qquad (13)$$

From equation (13) we have effective electron temperatures of 47 K, 35 K, 22 K and 10 K when the bath temperatures are 295 K, 225 K, 150 K and 77 K, respectively.

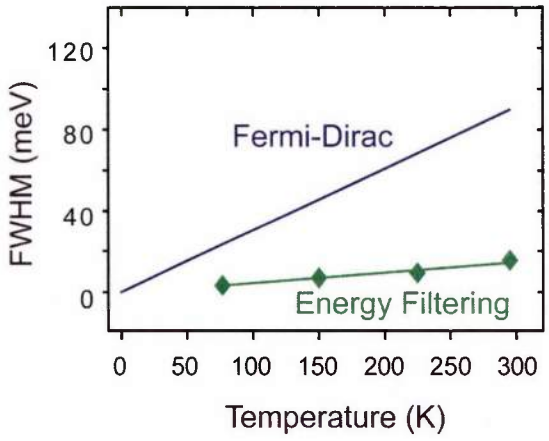

Figure 11. The FWHM and the effective electron temperature of the energy-filtered cold electrons. The FWHM vs. temperature relationship is displayed for the case of the usual Fermi-Dirac smearing (blue) and energy-filtered cold electron transport (green). From these relationships, the effective electron temperature of the energy-filtered cold electron can be obtained, to give the equation (13).

II.B.6. Application of the Energy-Filtered Cold Electron Transport

The energy-filtered cold electron transport has profound technical implications. If this method can be properly implemented into electron systems/devices whose operations are limited by the Fermi-Dirac thermal excitation, the electron energy filtering could substantially relieve those thermal limitations. As an application example, we fabricated energy-filtered single-electron transistors in which tunneling events of energy-filtered cold electrons are controlled by the Coulomb blockade effect of single electrons.

We fabricated such single-electron transistors (SETs) in which the energy-filtered cold electron transport was implemented. The SETs were fabricated with the configuration shown in Fig. 1, but with two alterations: (1) the CdSe QD was replaced by a metal nanoparticle (~10 nm Au nanoparticle) and (2) a gate electrode was added using the configuration reported previously, in which the gate encompasses the periphery of the source/insulating layer/drain stack in Fig. 1a[9]. The *I-V* characteristics of the fabricated SETs are displayed in Fig. 12. Figure 12a shows measured source/drain *I-V* characteristics at temperatures (bath temperatures) ranging from 10 K to 295 K. Coulomb staircases are clearly observed for all temperature ranges including room temperature. The most important feature of these Coulomb staircase observations is that the Coulomb staircase at 10K is almost unchanged even if the temperature is raised to room temperature (295 K). This shows that the energy filtering in the SET is working very

effectively. For comparison, the *I-V* characteristics of SETs under the usual single-electron transport (without the energy filtering) are displayed in Fig. 12b (calculated using orthodox theory). We find that the Coulomb staircase is wiped out even at 100 K due to the Fermi-Dirac thermal smearing. The effectiveness of the energy filtering is also found for the Coulomb oscillations. Figure 12c shows the *I-V* characteristics (source-drain current *vs.* gate voltage) of the fabricated SET at temperatures ranging from 10K to 295K. Clear Coulomb oscillations are observed for all temperatures examined. Again, it is important to note that the Coulomb oscillations at 10K very much prevails even at 295K with only a little thermal smearing observed, which demonstrates the effectiveness of the energy-filtered cold electron transport. In comparison, the Coulomb oscillations under the usual single-electron transport (without the energy filtering) are displayed in Fig. 12d. The Coulomb oscillations are almost wiped out at 100K due to the Fermi-Dirac thermal smearing and no Coulomb oscillations are detected at 200K and 295K.

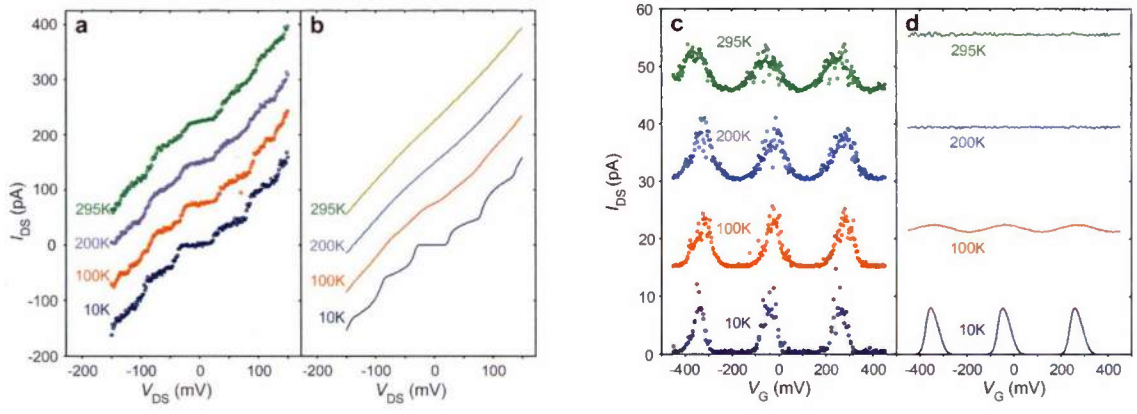

Figure 12. Application of energy-filtered cold electron transport to single-electron transistors. a. Coulomb staircases (measured) at temperatures from 10K to 295K (temperatures indicated are the bath temperatures). Clear Coulomb staircases are observed even at room temperature, demonstrating the effectiveness of the energy filtering in the SET. **b.** Coulomb staircases under the usual single-electron transport (without energy filtering) calculated using orthodox theory. Coulomb staircase is wiped out even at 100K due to the Fermi-Dirac thermal smearing. **c.** Coulomb oscillations (measured) at temperatures from 10K to 295K. The source-drain voltage: 10 mV. Clear Coulomb oscillations are observed up to the room temperature. **d.** Coulomb oscillations under the usual single-electron transport (without energy filtering) calculated using orthodox theory. The Coulomb oscillations were wiped out at 200K and 295K.

The experimental demonstrations that the low-temperature Coulomb staircases and Coulomb oscillations are well preserved even at room temperature, in Fig. 12a and Fig. 12c, can be explained by the fact that the energy-filtered electrons are much colder than the thermal bath (the temperature at which the experiments were carried out). Effective electron temperatures of energy-filtered cold electrons are ~45, ~30, and ~15 K for the bath temperatures of 295, 200, and 100 K, respectively (from equation (13)). These low electron temperatures explain the experimental observations of Coulomb staircases and Coulomb oscillations (Fig. 12a and Fig. 12c) extremely well. This is shown in Fig. 13 in which the orthodox theory calculations (red lines) at these low effective temperatures faithfully reproduce all the experimental Coulomb staircase and Coulomb oscillation data.

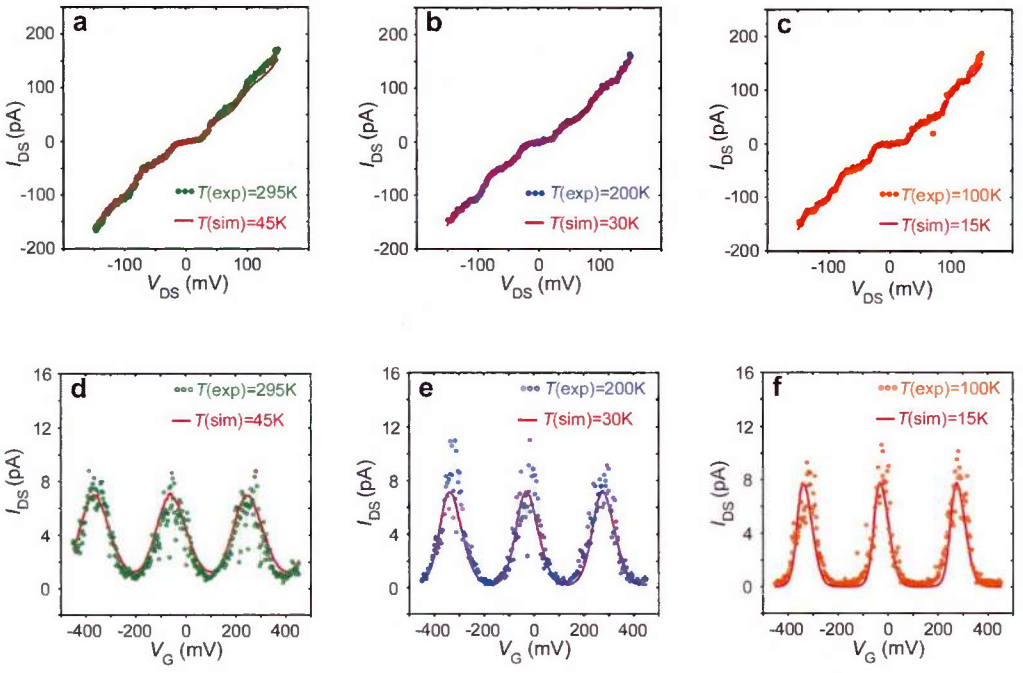

Figure 13. The effect of low effective electron temperature on the Coulomb staircases and Coulomb oscillations in SETs. a-c. Coulomb staircases. **d-f.** Coulomb oscillations. The low effective temperatures of the energy-filtered cold electrons enabled Coulomb staircases and Coulomb oscillations even the bath temperatures (experimental temperatures) were much higher. The effective electron temperatures of the energy-filtered cold electrons well explain the observed Coulomb staircases and Coulomb oscillations. *T*(exp): the bath temperature at which the experimental measurement was carried out. *T*(sim): the effective electron temperature at which the calculations with orthodox theory were carried out.

The benefit of having low-temperature electros is clear in the SET example demonstrated: the requirement of liquid He cooling can be lifted, yet the low-temperature SET performance remains. This demonstration for the application of energy-filtered cold electron transport opens up new possibilities that energy-filtered cold electrons can be used in many devices whose functionalities or performances are limited by electron thermal excitations.

II.C. Comprehensive Mechanical Understanding of Energy-Filtered Cold Electron Transport

We have investigated detailed mechanisms for the energy-filtered cold electron transport and developed a comprehensive microscopic model. Numerical calculations were made based on this model and the calculated results agree very well with the experimental findings. The modeling and its numerical calculations are detailed below.

II.C.1. Modeling

We model the electron transport as sequential tunneling between adjacent device components, Fig. 14a. The device components are source (L), a quantum well (QW), a quantum dot (QD), and drain (R). Tunneling barrier 1 separates the QW and the QD, and tunneling barrier 2 separates the QD and the drain (R). Electrons tunnel between the adjacent components in a sequential manner. The QW on the drain side does not contribute to the energy filtering since under the condition $\varepsilon_D > \mu_R$, electrons in the QD will tunnel out to the drain anyway without regard to the presence of QW in the drain side. For simplicity, the model does not include the QW on the drain side.

The tunneling rates between the adjacent components are defined as $\Gamma_L^{\pm}(i_W)$, $\Gamma_D^{\pm}(i_W)$, $\Gamma_W^{\pm}(i_D)$ and $\Gamma_R^{\pm}(i_D)$ (see Fig. 14a). $\Gamma_L^{\pm}(i_W)$ is the tunneling rate when the number of electrons in the QW *before* the tunneling is i_W, where the superscript "+" and "–" represents an electron is added to the QW and subtracted from the QW, respectively, and the subscript "L" represents the electron addition and subtraction is through the source electrode (L). Other rates are defined with the same manner as follows. $\Gamma_D^{\pm}(i_W)$ is the rate for an electron to tunnel from the QD to the QW ("+") or from QW to QD ("–") when the number of electrons in the QW *before* tunneling is i_W. $\Gamma_W^{\pm}(i_D)$ is the rate for an electron

to tunnel from the QW to the QD ("+") or from QD to QW ("–") when the number of electrons in the QD level *before* tunneling is i_D. $\Gamma_R^{\pm}(i_D)$ is the rate for an electron to tunnel from the drain electrode (R) to the QD ("+") or from QD to R ("–") when the number of electrons in the QD *before* the transport is i_D.

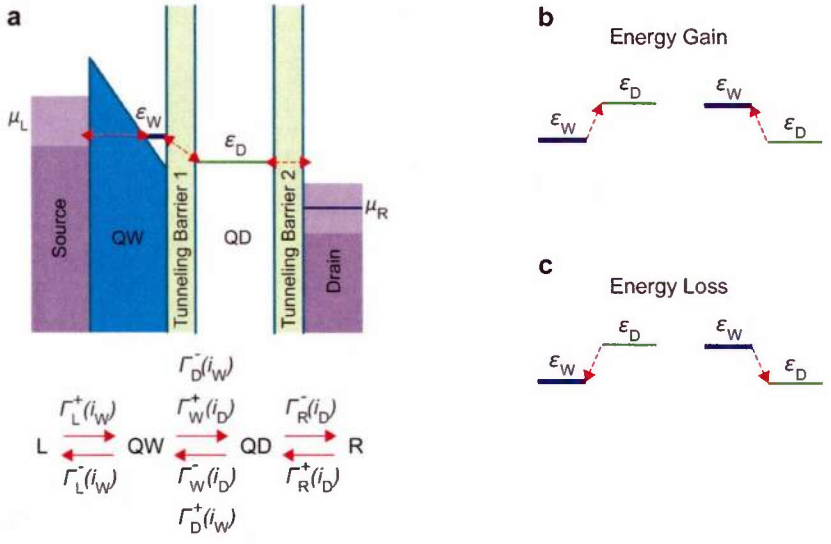

Figure 14. Modeling for the energy-filtered cold electron transport. **a.** Energy diagram. Electrons are transported from Source to Drain through sequential tunneling between device components. The device components are the source (L), a quantum well (QW), a quantum dot (QD), and the drain (R). The tunneling rates between device components are defined in the text. **b-c.** Schematic of an inelastic tunneling in which an electron gains (**b**) and loses (**c**) the energy, respectively.

For the electron transport between the QW and the QD, we also include inelastic electron tunneling processes in which an electron gains or loses its energy in the tunneling (Fig. 14b and 14c). We assume that an electron can gain the energy in the tunneling only through the phonon absorption[10,11], Fig. 14b. The tunneling probability of the inelastic tunneling through phonon absorption $\gamma_{absorp}(\varepsilon, T)$ is given by[10,11]

$$\gamma_{absorp}(\varepsilon, T) = n(|\varepsilon|, T)\, A(|\varepsilon|) \tag{14}$$

where $\varepsilon<0$ (we define $\varepsilon<0$ for the energy gain), $n(|\varepsilon|, T)$ is the Bose-Einstein distribution function of phonon population, $n(\varepsilon\ (>0),\ T) = 1/(e^{\varepsilon/kT} - 1)$, where T is the absolute temperature and k is the Boltzmann constant and $A(\varepsilon)$ is the Einstein A coefficient for

spontaneous emission of phonons[10]. The total tunneling probability includes the contribution by the elastic tunneling $\gamma_{\text{elastic}}(\varepsilon)$, for which the lifetime broadening with the Lorentzian distribution[3,12,13] is assumed and is given by

$$\gamma_{\text{elastic}}(\varepsilon) = \frac{2}{\hbar}\left(\frac{\hbar T_{\text{elastic}}}{2}\right)^2 \frac{\frac{\hbar T_{\text{elastic}}}{2}}{\varepsilon^2 + \left(\frac{\hbar T_{\text{elastic}}}{2}\right)^2} \tag{15}$$

where $\hbar$ is the reduced Planck constant and T_{elastic} is the elastic tunneling probability when the QW energy level and QD energy level align exactly (*i.e.*, when ε=0). The total tunneling probability $\gamma(\varepsilon<0, T)$ is then

$$\begin{aligned}\gamma(\varepsilon<0, T) &= \gamma_{\text{absorp}}(\varepsilon, T) + \gamma_{\text{elastic}}(\varepsilon) \\ &= n(|\varepsilon|, T)\, A(|\varepsilon|) + \frac{2}{\hbar}\left(\frac{\hbar T_{\text{elastic}}}{2}\right)^2 \frac{\frac{\hbar T_{\text{elastic}}}{2}}{\varepsilon^2 + \left(\frac{\hbar T_{\text{elastic}}}{2}\right)^2} \\ &= 1/(e^{|\varepsilon|/kT} - 1)\, A(|\varepsilon|) + \frac{2}{\hbar}\left(\frac{\hbar T_{\text{elastic}}}{2}\right)^2 \frac{\frac{\hbar T_{\text{elastic}}}{2}}{\varepsilon^2 + \left(\frac{\hbar T_{\text{elastic}}}{2}\right)^2}\end{aligned} \tag{16}$$

An inelastic electron transport in which electron loses the energy can occur through a phonon emission and other energy relaxation processes (e.g., defect-assisted relaxation, interface-roughness scattering and impurity scattering)[13-19], which we represent by $\gamma_{\text{emiss}}(\varepsilon,T)$ and $\gamma_{\text{relax}}(\varepsilon)$, respectively. The tunneling probability through phonon emission $\gamma_{\text{emiss}}(\varepsilon, T)$ is given by[10,11]

$$\begin{aligned}\gamma_{\text{emiss}}(\varepsilon, T) &= [\, n(\varepsilon, T)+1\,]\, A(\varepsilon) \\ &= [1/(e^{\varepsilon/kT} - 1) + 1]\, A(\varepsilon)\end{aligned} \tag{17}$$

The total tunneling probability in which an electron loses the energy in the tunneling (ε>0) is then

$$\gamma(\varepsilon>0, T) = \gamma_{emiss}(\varepsilon, T) + \gamma_{elastic}(\varepsilon) + \gamma_{relax}(\varepsilon)$$

$$= [1/(e^{\varepsilon/kT} - 1) + 1]\, A(\varepsilon) + \frac{2}{\hbar}\left(\frac{\hbar T_{elastic}}{2}\right)^2 \frac{\frac{\hbar T_{elastic}}{2}}{\varepsilon^2 + \left(\frac{\hbar T_{elastic}}{2}\right)^2} + \gamma_{relax}(\varepsilon) \qquad (18)$$

Now, we define $P_W(i_W)$ as the probability that the number of electrons that occupy the QW level is i_W, where i_W can be either 0, 1 or 2. Likewise, we define $P_D(i_D)$ as the probability that the number of electrons that occupy the QD level is i_D, where i_D can be either 0 or 1 (since single electron charging energy for our CdSe QDs is larger than 100 meV, the state with two electrons occupied is treated as a different state from that with one electron occupied). Then, the tunneling rates $\Gamma_L^{\pm}(i_W)$, $\Gamma_D^{\pm}(i_W)$, $\Gamma_W^{\pm}(i_D)$ and $\Gamma_R^{\pm}(i_D)$ are related to the tunneling probabilities $\gamma(\varepsilon<0, T)$ and $\gamma(\varepsilon>0, T)$ and the occupation probabilities $P_W(i_W)$ and $P_D(i_D)$ as follows:

$$\Gamma_L^{+}(0) = f_L(\varepsilon_W) \times D_L(\varepsilon_W) \times T_L \qquad (19)$$

$$\Gamma_L^{+}(1) = f_L(\varepsilon_W) \times D_L(\varepsilon_W) \times T_L \qquad (20)$$

$$\Gamma_L^{-}(1) = [1 - f_L(\varepsilon_W)] \times D_L(\varepsilon_W) \times T_L \qquad (21)$$

$$\Gamma_L^{-}(2) = [1 - f_L(\varepsilon_W)] \times D_L(\varepsilon_W) \times T_L \qquad (22)$$

$$\Gamma_D^{+}(0) = \gamma(\varepsilon_D - \varepsilon_W, T) \times P_D(1) \qquad (23)$$

$$\Gamma_D^{+}(1) = \gamma(\varepsilon_D - \varepsilon_W, T) \times P_D(1) \qquad (24)$$

$$\Gamma_D^{-}(1) = \gamma(\varepsilon_W - \varepsilon_D, T) \times P_D(0) \qquad (25)$$

$$\Gamma_D^{-}(2) = \gamma(\varepsilon_W - \varepsilon_D, T) \times P_D(0) \qquad (26)$$

$$\Gamma_W^+(0) = \gamma(\varepsilon_W - \varepsilon_D, T) \times [P_W(1) + P_W(2)] \quad (27)$$

$$\Gamma_W^-(1) = \gamma(\varepsilon_D - \varepsilon_W, T) \times [P_W(0) + P_W(1)] \quad (28)$$

$$\Gamma_R^+(0) = f_R(\varepsilon_D) \times D_R(\varepsilon_D) \times T_R \quad (29)$$

$$\Gamma_R^-(1) = [1 - f_R(\varepsilon_D)] \times D_R(\varepsilon_D) \times T_R \quad (30)$$

where $f_L(E)$ and $f_R(E)$ are the Fermi-Dirac functions with chemical potential μ_L and μ_R for source (L) and drain (R) electrode, respectively, ε_W and ε_D are the energies of the QW and the QD states, respectively, T_L is the tunneling probability for electron tunneling between the source (L) and the QW, T_R is the tunneling probability for electron tunneling between the QD and the drain (R), $D_L(E)$ and $D_R(E)$ are the density of states for the source and the drain electrodes, respectively. As shown in equations (19)-(30), the tunneling rates $\Gamma_L^{\pm}(i_W)$, $\Gamma_D^{\pm}(i_W)$, $\Gamma_W^{\pm}(i_D)$ and $\Gamma_R^{\pm}(i_D)$ are determined by the positions of μ_L, ε_W, ε_D and μ_R , which in turn are determined by the voltage bias V applied between the source and the drain. Their relationships are $\mu_L - \mu_R = eV$, $\Delta(\varepsilon_W - \varepsilon_D) = \eta eV$ and $\Delta(\varepsilon_D - \mu_R) = (1- \eta)eV$.

At steady state, the transition rates between two adjacent configurations are the same (the net transition is zero). For two QW configurations with $i_W = 0$ and $i_W = 1$, for example, the transition rates between the two are the same:

$$P_W(0) \times [\Gamma_L^+(0) + \Gamma_D^+(0)] = P_W(1) \times [\Gamma_L^-(1) + \Gamma_D^-(1)] \quad (31)$$

Likewise, the transition rates between two QW configurations with $i_W = 1$ and $i_W = 2$ are the same, which gives:

$$P_W(1) \times [\Gamma_L^+(1) + \Gamma_D^+(1)] = P_W(2) \times [\Gamma_L^-(2) + \Gamma_D^-(2)] \quad (32)$$

Also, the transition rates between the two QD configurations are the same:

$$P_D(0) \times [\Gamma_W^+(0) + \Gamma_R^+(0)] = P_D(1) \times [\Gamma_W^-(1) + \Gamma_R^-(1)] \quad (33)$$

The summation of the probabilities must be the unity:

$$P_W(0) + P_W(1) + P_W(2) = 1 \tag{34}$$

and $$P_D(0) + P_D(1) = 1 \tag{35}$$

Since we have 5 equations, (31)-(35), and 5 unknowns, $P_W(0)$, $P_W(1)$, $P_W(2)$, $P_D(0)$ and $P_D(1)$, the simultaneous equations can be solved. For a given set of tunneling rates $\Gamma_L^{\pm}(i_W)$, $\Gamma_D^{\pm}(i_W)$, $\Gamma_W^{\pm}(i_D)$ and $\Gamma_R^{\pm}(i_D)$ for a specific V, we numerically solve the simultaneous equations (31)-(35) and obtain $P_W(0)$, $P_W(1)$, $P_W(2)$, $P_D(0)$ and $P_D(1)$. The electrical current I is then given by

$$I(V) = e \times [P_D(1) \times \Gamma_R^-(1) - P_D(0) \times \Gamma_R^+(0)] \tag{36}$$

where e is the charge of an electron. The dI/dV is obtained by numerical differentiation of the $I(V)$.

II.C.2. Numerical Calculations

We carried out numerical calculations using the model above. For functions $A(\varepsilon)$, $\gamma_{relax}(\varepsilon)$ and $\gamma_{elastic}(\varepsilon)$ in equations (14)-(18), we used the functional forms shown in Fig. 15. The other parameters used are as follows: $T_L \times D_L(\varepsilon_W) = 1.43\times10^{11}$ [sec^{-1}] and $T_R \times D_R(\varepsilon_D) = 1.43\times10^{11}$ [sec^{-1}], where constant values of T_L, T_R, D_L and D_R were assumed; $\mu_L = 0$ (reference energy zero), $\varepsilon_W = 0$, $\varepsilon_D = E_S - \eta eV$ (where E_S is the position of the s-level at V=0; $V_S = E_S/(\eta e)$) and $\mu_R = -eV$; η: the voltage division factor. The functional form for $A(\varepsilon)$ in Fig. 15a is based on the experimental and theoretical studies on phonon emission/absorption[10,11]. Its characteristics are that its value is zero when energy ε is zero ($A(0) = 0$), reaches a maximum, and then decreases to zero. For our system where nanoparticle diameter is ~10 nm, 20 meV was used as the effective Debye cutoff energy (beyond which $A(\varepsilon)$ is zero)[11]. The $\gamma_{relax}(\varepsilon)$ includes contributions from all relaxation

paths such as interface-roughness scattering, impurity scattering and defect-assisted relaxation[13-19]. For $\gamma_{relax}(\varepsilon)$, we used the functional forms shown in Fig. 15b with relaxation rates on the order of ~10^{12} [sec^{-1}]. This value is based on the literature, where experimental and theoretical studies show that the carrier relaxation rate can be as high as or exceed 10^{12} [sec^{-1}][14-17,20]. For the elastic tunneling rate $\gamma_{elastic}(\varepsilon)$, we used the Lorentzian form[3,12,13], Fig. 15c.

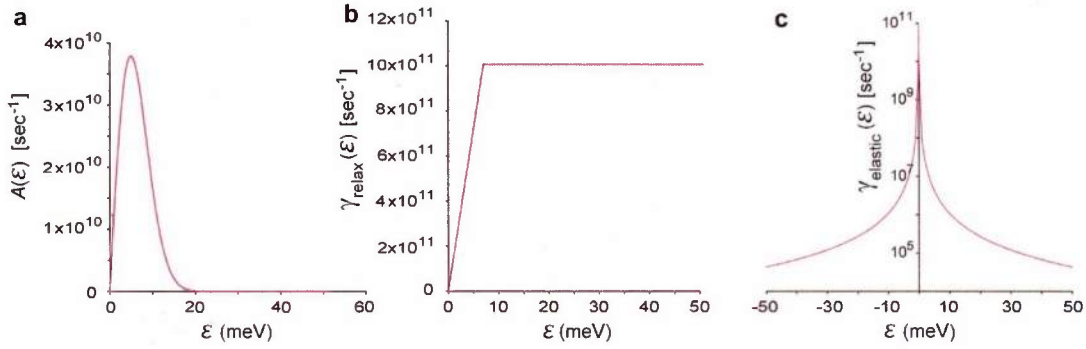

Figure 15. Functions used in the numerical calculations. a. $A(\varepsilon)$. **b.** $\gamma_{relax}(\varepsilon)$. **c.** $\gamma_{elastic}(\varepsilon)$.

We numerically solved the equations (31)-(35) and obtained the *I(V)*. Figure 16a-16d show the resulting *I(V)* at varying temperatures, 295, 225, 150, and 77 K, respectively. The abrupt current changes at $V=V_s$ are due to the alignment of the quantum well level of the energy filter with a quantum dot energy state. The energy filtering resulted in very abrupt changes of currents for all the temperatures investigated. The differential conductances were obtained by numerically differentiating the *I-V*'s in Fig. 16a-16d. The resulting *dI/dV*'s are displayed in Fig. 16e-16h. These show very sharp differential conductance peaks at all temperatures from 295K to 77K, with the peak sharper with decreasing temperature; the FWHM of the peak is only ~13 mV/η (η: the voltage division factor) at 295K and it decreases to ~5 mV/η at 77K.

Figure 17 compares the experimentally measured FWHMs of the differential conductance peaks (from Figs. 6 & 7) with the numerically calculated FWHMs (from Fig. 16e-16h). We find a very good agreement between the experiment and model calculations.

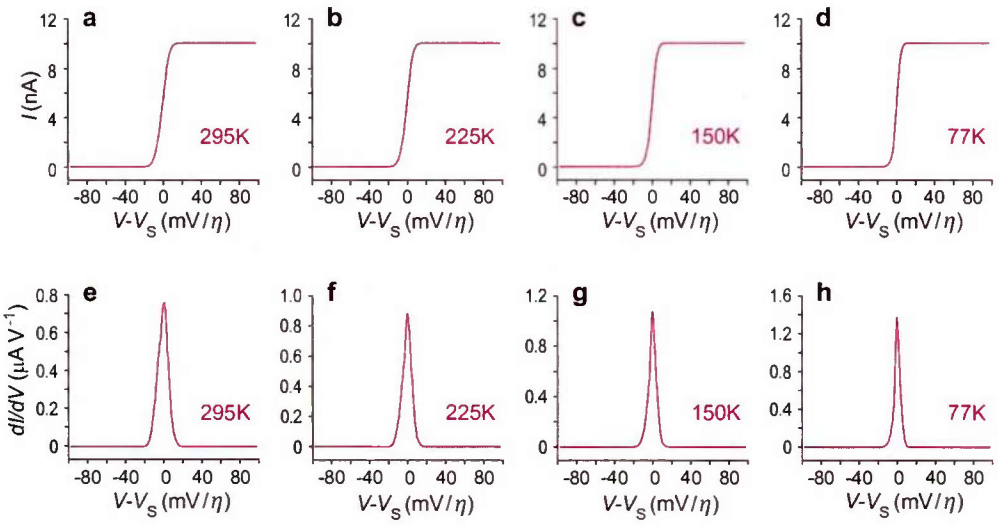

Figure 16. Numerical calculations. a-d. Numerically calculated *I-V*'s at 295, 225, 150, and 77 K, respectively. Functions in Fig. 15 were used for $A(\varepsilon)$, $\gamma_{relax}(\varepsilon)$, and $\gamma_{elastic}(\varepsilon)$. Other parameters used are: $T_L \times D_L(\varepsilon_W) = 1.43\times10^{11}$ [sec^{-1}] and $T_R \times D_R(\varepsilon_D) = 1.43\times10^{11}$ [sec^{-1}], where constant values of T_L, T_R, D_L and D_R were assumed. $\mu_L = 0$ (reference energy zero), $\varepsilon_W = 0$, $\varepsilon_D = E_S - \eta eV$ (where E_S is the position of the *s*-level at V=0; $V_S = E_S/(\eta e)$) and $\mu_R = -eV$. η: the voltage division factor. **e-h.** Numerically calculated differential conductances *dI/dV*'s at 295, 225, 150, and 77 K, respectively. These were obtained by numerically differentiating the *I-V*'s in **a-d**.

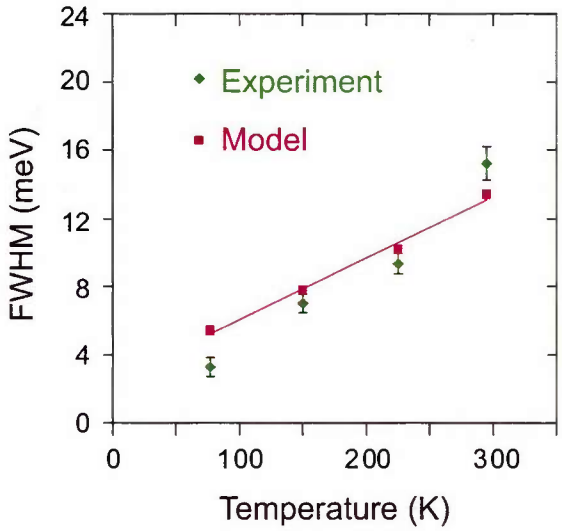

Figure 17. Comparison between the experimental results and model calculations. The experimental data are from Fig. 6 and Fig. 7. The model values are from Fig. 16e-16h. Very good agreement is found between the experiment and model calculations.

II.D. Direct Measurement of the Band Bending of Cr_2O_3 Quantum Well

The energy band bending of Cr_2O_3 layer produces a triangular quantum well as schematically displayed in Fig. 1b. It would be important to independently verify this quantum well formation in the Cr_2O_3 layer and measure the amount of band bending, *i.e.*, the depth of the quantum well. For this, we fabricated a metal-insulator-semiconductor (MIS) structure, Fig. 18, in which the insulator is composed of Cr_2O_3/SiO_2 layers and carried out capacitance-voltage (*C-V*) measurements of the fabricated MIS units. The *C-V* measurements provide the flat band voltages V_{FB} of the MIS structure and the flat band voltage shifts ΔV_{FB} with differing Cr_2O_3 thicknesses directly measure the energy band bending of the Cr_2O_3 layer.

The MIS units in Fig. 18 were fabricated as follows. A *p*-type Si substrate (sheet resistance: 1-25 Ω•cm) was used as the semiconductor material. On top of the Si substrate, 5 nm SiO_2 layer was sputter-deposited using AJA Orion UHV System with a deposition rate of 0.17 nm per minute at room temperature. On top of the SiO_2 layer, a Cr_2O_3 layer was sputter-deposited *in-situ* with a deposition rate of 0.25 nm per minute at room temperature. The Cr_2O_3 layer had three different thicknesses: 0 nm (no Cr_2O_3 layer), 2 nm and 5 nm, Fig. 18. The top metal electrode was then made using photolithography, Cr metal deposition and lift-off.

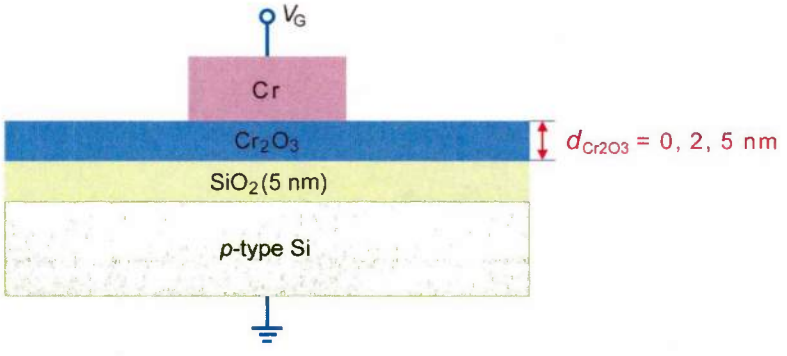

Figure 18. Metal-insulator-semiconductor (MIS) structure for a direct measurement of the energy band bending of the Cr_2O_3 layer. The Cr_2O_3 layer thickness d_{Cr2O3} : 0 nm (no Cr_2O_3), 2 nm and 5 nm.

The *C-V* measurements were carried out using Agilent 284A LCR Meter and Agilent 4155C Semiconductor Parameter Analyzer. An AC modulation frequency of 1 MHz was used for the *C-V* measurements. Figure 19a shows the measured *C-V* characteristics of the MIS units with varying Cr_2O_3 layer thicknesses d_{Cr2O3}. The *C-V* data in Fig. 19a-19b show that the flat band voltages V_{FB} become more negative with increasing Cr_2O_3 layer thicknesses d_{Cr2O3}. (Here the flat band voltages V_{FB} is defined as the gate voltage at which $C/C_0 = 0.8$, where C/C_0 is the normalized capacitance and C_0 is the total capacitance ($1/C_0 = 1/C_{cr2O3} + 1/C_{SiO2}$)). We find a linear relationship between the flat band voltage shifts V_{FB} and the Cr_2O_3 layer thicknesses d_{Cr2O3}. This linear relationship is in good agreement with the known relationship between the flat band shift and the dielectric layer thickness[21-24]:

$$\Delta V_{FB}(d_{Cr2O3}) = -Q_i/C_{Cr2O3} = -(Q_i/\varepsilon_{Cr2O3}) \times d_{Cr2O3}$$

, where Q_i is effective interface charge density at the Cr_2O_3/SiO_2 interface, C_{Cr2O3} is the capacitance per unit area of the C_{Cr2O3} layer and ε_{Cr2O3} is the permittivity of Cr_2O_3.

From the *C-V* measurements in Fig. 19a, we conclude the following. First, the negative shift of V_{FB} with increasing d_{Cr2O3} shows that the band bending of the Cr_2O_3 energy band occurs in a direction that forms a triangular quantum well; *i.e.*, the Cr_2O_3 energy band goes down as it approaches the Cr_2O_3/SiO_2 interface. Second, from the linear relationship in Fig. 19b, the flat band shift ΔV_{FB} for the 2 nm Cr_2O_3 (approximate native chromium oxide thickness) is -1.1 V:

$$\begin{aligned}\Delta V_{FB}\,(d_{cr2O3} = 2\text{ nm}) &= V_{FB}\,(d_{cr2O3} = 2\text{ nm}) - V_{FB}\,(d_{cr2O3} = 0\text{ nm}) \\ &= -0.5327 \times 2 = -1.0624\text{ [V]}.\end{aligned}$$

These *C-V* measurements of the MIS structure demonstrate that a triangular quantum well is formed due to the band bending of the Cr_2O_3 layer and the depth of the quantum well is -1.1 eV.

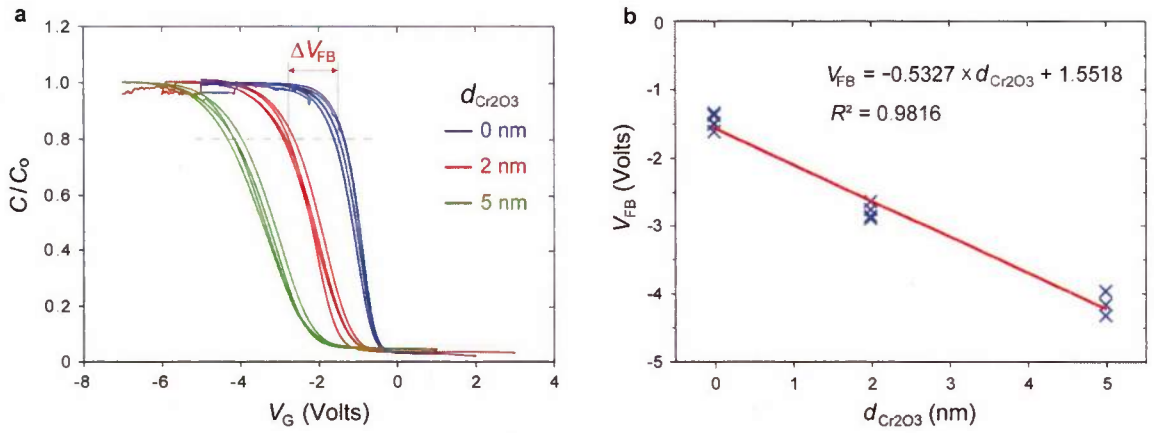

Figure 19. Measured *C-V* characteristics for the MIS units with varying Cr_2O_3 layer thicknesses d_{cr2O3}. a. *C-V* characteristics for the MIS units with Cr_2O_3 layer thickness d_{cr2O3} = 0 nm (blue), 2 nm (red) and 5 nm (green). Each line is the measured *C-V* data from a different MIS unit. The flat band voltage V_{FB} is defined as the voltage V_G at which the C/C_o is 0.8 (the dashed line). ΔV_{FB} (in red in **a**) is the flat band voltage shift for d_{cr2O3} = 2 nm, *i.e.*, $\Delta V_{FB} = V_{FB}$ (d_{cr2O3} = 2 nm) – V_{FB} (d_{cr2O3} = 0 nm). C/C_o: normalized capacitance, where C_o is the total capacitance of the Cr_2O_3/SiO_2 layers ($1/C_o = 1/C_{Cr2O3} + 1/C_{SiO2}$). **b.** Measured flat band voltages V_{FB} as a function of Cr_2O_3 layer thickness d_{cr2O3}. The V_{FB}'s are from the *C-V* measurements in **a**. A linear relationship is found with R^2 value of 0.98.

II.E. Design of Vertically Configured Energy-Filtered Cold-Electron Transistor and Its Large-Scale Fabrication

II.E.1. Device Configuration and Fabrication

We demonstrated the energy-filtered cold electron transport using the configuration shown in Fig. 1, where a semiconductor nanoparticle (a QD) was used as a central semiconductor. For large-scale manufacturing, however, this device configuration may not be directly used as the placement of QDs was carried out by random attachment, whose yield was not 100 percent. We have therefore designed new device architecture that allows a large-scale fabrication of energy-filtered cold-electron devices. Figure 20 schematically displays this architecture in which the device components, the source, a quantum well, first tunneling barrier, a semiconductor layer, second tunneling barrier, and the drain, are arranged in vertical configuration. This transistor structure can be defined using conventional CMOS-compatible processes such as photolithography, dielectric depositions and etching, allowing a large-scale parallel fabrication.

We have developed processes and materials needed to construct the transistor configuration in Fig. 20, and fabricated the transistors in parallel processing. Briefly,

transistors were fabricated in parallel processing that involved 5 photomask steps. The fact that the structure in Fig. 20 can be fabricated using the photolithography and other CMOS-compatible processes makes the large-scale fabrication possible. The first photomask step was to define source electrodes on a silicon wafer. Layers of films were then deposited in a sequence of the first tunneling barrier, a semiconductor layer and the second tunneling barrier. The quantum well was spontaneously formed between the source and the first tunneling barrier layer due to energy band bending (Section II.D). This was followed by defining the drain electrodes using the second photomask step. The deposited layers were etched using the drain as a hardmask. This was followed by defining the gate electrodes using third photomask step. The devices were then passivated using insulating oxide. The via holes were etched using fourth photomask step and reactive ion etching (RIE). The electrical connections were made using the fifth photomask step and metal deposition, which produced bond pads that made electrical contacts with source, drain, and gate electrodes through the via holes. The electrical characterizations of the fabricated transistors are currently being performed.

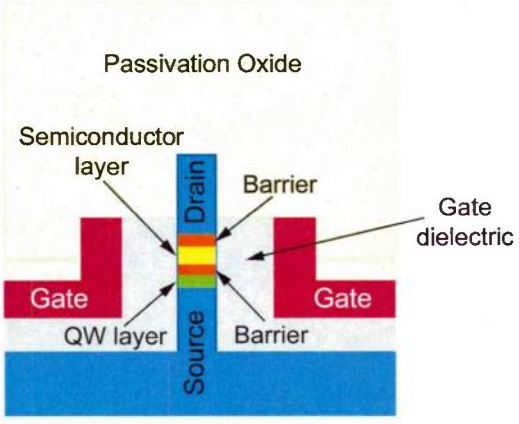

Figure 20. Schematic of a vertically configured energy-filtered cold-electron transistor. Schematic is not to scale. The device components are arranged in vertical configuration.

II.E.2. Process Development for High-Quality Material Layers

For transistors in Fig. 20 to function as designed, it is essential that the device components are made of high-quality materials, especially the thin dielectric films as their thicknesses are only a few nanometers; the tunneling barrier thickness is of a couple of nanometers, semiconductor layer thickness is less than 5 nm, and the gate dielectric

thickness is just a few nanometers. Substantial amount of efforts have been put to develop optimized processes and to obtain high-quality films. These films are PECVD (plasma-enhanced chemical vapor deposition) SiO_2 layers for tunneling barriers, PECVD amorphous Si (a-Si) for the semiconductor layer, sputtered SiO_2 layers for gate dielectrics and passivation layers, and sputtered HfO_2 layers for the gate dielectrics. Process parameters were optimized in a direction to lower the deposition rate as the low deposition rates typically produce high quality films. The film qualities were electrically characterized by measuring the breakdown electric fields.

For the PECVD SiO_2 deposition, we have found that the deposition temperature and the gas flow rates play a critical role on the film quality, as assessed by the film uniformity, roughness, and breakdown electric fields. After systematic optimization of the temperature, the flow rate of SiH_4, and the flow rate ratio of SiH_4/N_2O, we have obtained optimized deposition conditions for high quality PECVD SiO_2 films. The optimized deposition parameters are summarized as follows: (a) Substrate temperature: 380 °C, (b) Gas flow rates: 10 sccm SiH_4, 179 sccm N_2O, and 250 sccm N_2, (c) Pressure: 1000 mTorr, (d) ICP (inductively-coupled plasma) power: 500 W, and (e) RF (radio frequency) power (bottom electrode): 30 W.

For the semiconductor layer material in Fig. 20, we have developed a PECVD process to deposit amorphous silicon (a-Si) layer. We have systematically investigated the effect of temperature (ranging from 200 °C to 300 °C), the pressure, the gas flow rate of SiH_4 on the film quality. We have found that the flow rate of SiH_4 and substrate temperature play critical roles on the film quality; with high substrate temperature (>250 °C) and/or high SiH_4 flow rate (>20 sccm), the film became rough (corrugation > 5 nm) as measured from atomic force microscopy (AFM). We found that reducing the substrate temperature to 200 °C (with SiH_4 flow rate of 20 sccm) is very critical to achieve smooth films (corrugation < 1 nm). The AFM image in Fig. 21 demonstrates that the surface corrugation of the PECVD a-Si film is less than 1 nm. The breakdown electric field has also been measured to be ~2 MV/cm. The optimal process parameters obtained for PECVD a-Si films are as follows: (a) Substrate temperature: 200 °C, (b) Gas flow rates: 20 sccm SiH_4, (c) Pressure: 300 mTorr, (d) ICP (inductively-coupled plasma) power: 50-100 W, and (e) RF (radio frequency) power (bottom electrode): 0 W.

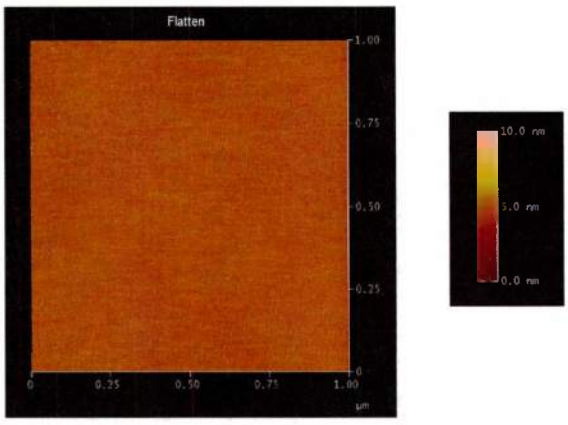

Figure 21. AFM image of PECVD-grown amorphous silicon film. Surface corrugation: <1 nm. Deposited a-Si film thickness: ~45 nm.

We have also developed a high quality HfO_2 film for the gate dielectric in Fig. 20. The HfO_2 films were obtained using the RF sputtering process at room temperature. Here, the addition of O_2 gas to Ar played an important role on the film quality[25]. Our optimized HfO_2 sputter deposition conditions are as follows: (a) Gas flow: 50 sccm Ar, 10 sccm O_2, (b) Pressure: 15 mTorr, and (c) RF power: 150 W.

For the gate dielectric material and also for the passivation layer in Fig. 20, we have developed a sputtered SiO_2 deposition process. As in the HfO_2 sputter deposition, the inclusion of the oxygen has also been found important for the SiO_2 sputter deposition. The sputter was carried out at room temperature. Our optimized process parameters for sputtered SiO_2 deposition are as follows: (a) Gas flow: 35 sccm Ar, 15 sccm O_2, (b) Pressure: 10 mTorr, and (c) RF power: 100 W.

II.F. Controlled Placement of Nanoparticles for Drain Mask Formation

We can make the lateral dimension of the transistor in Fig. 20 very small by defining the drain electrode using a nanoparticle mask instead of a photomask. The reduced lateral dimension can greatly increase the transistor packing density. To use this nanoparticle mask for large-scale fabrications, the individual nanoparticle needs to be placed on an exact target location on a single-particle level. This single-particle placement was previously demonstrated by our group using citrate-passivated Au nanoparticles[26], but the amount of charges on the Au nanoparticle surface was controlled in a limited way as the surface charges were obtained through physisorbed citrate ions.

An active control of the electric charges on the nanoparticle surface would provide more detailed leverage on the inter-nanoparticle interactions and nanoparticle-substrate interactions. For precise and reliable control of the electrical charges on the Au nanoparticle surface, we chemically attached single-stranded DNA molecules (negatively charged) onto the Au nanoparticle surfaces. The amount of attached single-stranded DNA per nanoparticle was controlled, thereby the total electrical charges on the nanoparticle. With the surface charge of the nanoparticle well controlled, the single-particle level placement was carried out on a large area, as needed for practical device fabrications.

The controlled attachment of single-stranded DNA molecules to Au nanoparticle surface was performed with procedure shown in Fig. 22. The staring nanoparticles were citric acid or tannic acid passivated Au nanoparticles (purchased from Nanocomposix or Ted Pella). With an introduction of FSN (fluorosurfactant by DuPont) to the Au nanoparticle colloid, the citric or tannic acid on the Au nanoparticle surfaces were replaced by the FSN[27]. Thiol-terminated (-SH) single-stranded DNA in NaCl solution was then introduced to the FSN-coated Au nanoparticle colloid, in which the single-stranded DNA replaced a portion of FSN through the formation of chemical bonding between thiol group of the DNA and the Au surface. The amount of DNA attachment was controlled by the NaCl concentration; higher NaCl concentration makes DNA to DNA electrostatic repulsion weaker due to increased screening, which allows more DNA molecules to approach toward Au nanoparticle surface, promoting the DNA attachment on the Au nanoparticle surface. With NaCl concentration of 0.45 M, the number of DNA molecules attached on a 30 nm Au nanoparticle was ~230 (separately measured using DNA molecules functionalized with fluorescent marker).

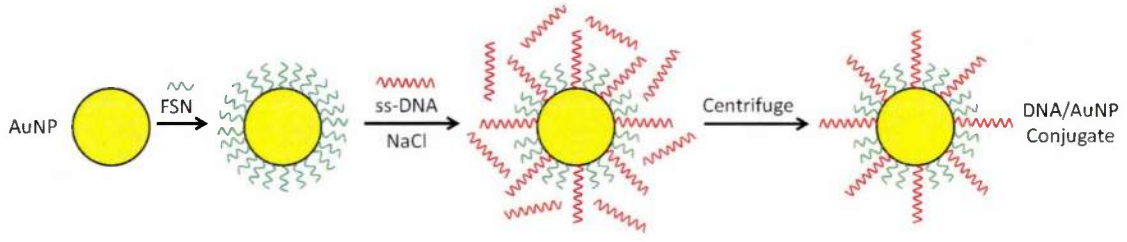

Figure 22. Procedure to attach single-stranded DNA molecules onto Au nanoparticle surface.

With the number of DNA molecules (therefore the electrical charges) on the Au nanoparticle well controlled, the use of the DNA-conjugated Au nanoparticles for the drain mask was investigated. The goal was to acquire the capability of placing individual Au nanoparticles onto target drain positions on a single-particle level (*i.e.*, to place exactly one nanoparticle on each drain position) on a large scale and over a large area. We first fabricated electrostatic guiding templates which were made of an Au film on a SiO_2 substrate with the Au film containing circular holes as shown in Fig. 23. The electrostatic guiding structure was made by functionalizing the Au surface with SAMs (self-assembled monolayers) of 16-mercaptohexadecanoic acid (MHA; negatively charged) and the SiO_2 surface (circular holes) with SAMs of aminopropyltriethoxysilane (APTES: positively charged). With an introduction of DNA-functionalized Au nanoparticles, the negatively- and positively- charged SAMs electrostatically guided the Au nanoparticles to the circle centers, Fig. 23. Once a circular hole was occupied by a Au nanoparticle, further attachment of nanoparticles to the same circular hole was prevented as the already placed nanoparticle changed the electrostatic landscape such that it deterred the approach of the other nanoparticles to the same hole[26]. This self-terminating single-particle placement can only be obtained with well-balanced electrostatic interactions between Au nanoparticles as well as the interactions between Au nanoparticle and the charged substrate. With systematic investigation of the effects of

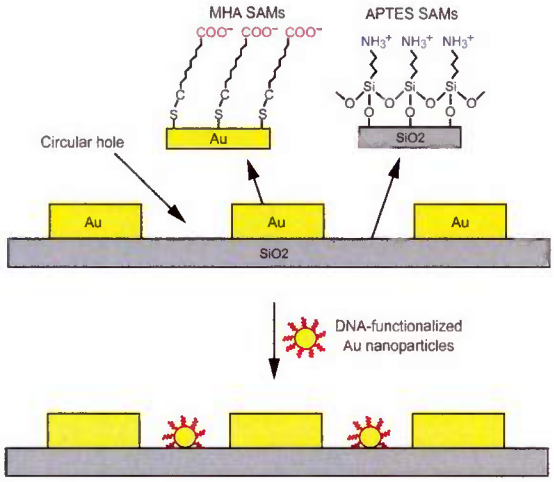

Figure 23. Schematic for single-particle level placement of Au nanoparticles. The electrostatic guiding structure is made using positively- and negatively- charged SAMs. MHA: 16-mercaptohexadecanoic acid (negatively charged); APTES: aminopropyltriethoxysilane (positively charged).

buffer ion concentrations and its pH on the self-terminating single-particle placement, the optimized conditions were obtained, with 1 mM for the ion concentration of the phosphate buffer (PB) and with 7.5 for the pH. The SEM images in Fig. 24 demonstrate the successful single-particle level placement of Au nanoparticles. Here DNA-functionalized ~30 nm Au nanoparticles were used with circular templates having diameter of ~120 nm. This demonstrates the feasibility of using the single-particle placement for defining nanoscale drain masks and reducing the lateral dimension of transistors.

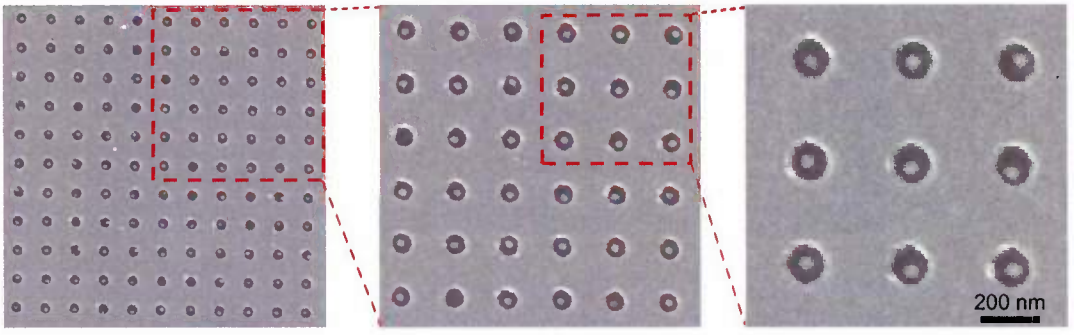

Figure 24. SEM images demonstrating the large-area single-particle placement. White dots: DNA-functionalized 30 nm Au nanoparticles.

II.G. Summary

This project has investigated fundamental physics of electron energy filtering occurring at room temperature as well as its applications to practical devices such as room-temperature single-electron transistors and ultralow energy consumption transistors. We have experimentally demonstrated, for the first time, that an energy level in a quantum well can filter out energetic electrons that are present at the Fermi-Dirac distribution tail, thereby effectively suppress the Fermi-Dirac electron thermal excitations, producing energy-filtered cold electrons at room temperature. The *I-V* measurements and also differential conductance measurements using the lock-in technique have shown that the effective electron temperature can become as low as 45 Kelvin at room temperature without any external cooling. We have also investigated the underlying mechanisms of the experimentally observed cold-electron transport and have obtained a comprehensive microscopic model for the energy-filtered cold electron

transport. We have carried out numerical calculations based on the model and they were in excellent agreements with the experimental *I-V* and experimental differential conductance data. Practical applications of the cold-electron transport have been pursued for two electronic devices, 1) room-temperature single-electron transistors, and 2) ultralow energy consumption transistors. For the first, we have fabricated room-temperature single-electron transistors that have 10 nm Au nanoparticles as the Coulomb islands. The energy filtering lowered the effective electron temperature to 45 Kelvin at room temperature, enabling single-electron transport at room temperature; their *I-V* characteristics have demonstrated clear Coulomb staircases and Coulomb oscillations at room temperature. For the second, we have designed energy-filtered cold electron transistor architecture in vertical configurations that enable large-scale and large-area fabrications. The vertical arrangement of device layers (source, quantum well, first tunneling barrier, semiconductor layer, second tunneling barrier, and drain) allows their sub-nanometer scale thickness control (e.g., 1 nm tunneling barrier) over a large area, permitting wafer-scale parallel fabrications. Optimized processes to produce high quality films (e.g., SiO_2, HfO_2, and amorphous Si) for the transistor components have also been developed. Using 5 photomask steps and using optimized materials/processes, we have fabricated the energy-filtered cold electron transistor structure, whose electrical characterizations are currently under way. A method to define nanoscale drain masks has been developed, in which DNA-functionalized Au nanoparticles are electrostatically guided and placed on target drain positions with nanoscale precision.

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III. Publications and Presentations

III.A. Publications/Patents

1. P. Bhadrachalam, R. Subramanian, V. Ray, L.-C. Ma, W. Wang, J. Kim, K. Cho, and S.J. Koh, "Energy-filtered cold electron transport at room temperature", *Nature Communications*, Vol. 5, 4745, 2014
2. S.J. Koh, "Energy-Filtered Cold Electron Devices and Methods", International Application (PCT), Filed on 2/3/15
3. S.J. Koh, "Energy-Filtered Cold Electron Transistor", U.S.PATENT Pending, Filed on 8/2/14
4. S.J. Koh, P. Bhadrachalam, L.-C. Ma, "Energy-Filtered Cold Electron Devices for Ultralow-Power-Dissipation Electronics", U.S.PATENT Pending, Filed on 2/4/14

III.B. Presentations

1. **(Invited)** S.J. Koh, "Cold-Electron Transistor for Energy Efficient Electronics", THERMEC'2016 International Conference on Processing & Manufacturing of Advanced Materials, Graz, Austria, May 2016 (scheduled future talk)
2. **(Invited)** S.J. Koh, "Cold-Electron Transport at Room Temperature: Toward Ultralow Energy Consumption Electronics", Collaborative Conference on 3D and Materials Research (CC3DMR) 2016, Incheon/Seoul, South Korea, June 2016 (scheduled future talk)
3. **(Invited)** S.J. Koh, "Electron Energy Filtering for Energy Efficient Electronics", TMS Annual Meeting, Orlando, Florida, March 2015
4. **(Invited)** S.J. Koh, "Cold Electron Transport at Room Temperature: Toward Ultralow Power Consumption Electronics", Seoul National University, S. Korea, January 2015
5. **(Invited)** S.J. Koh, "Cold Electron Transport at Room Temperature: Toward Extremely-Low Heat Dissipation Electronics", SungKyunKwan University, S. Korea, January 2015
6. P. Bhadrachalam, R. Subramanian, V. Ray, L.-C. Ma, W. Wang, J. Kim, K. Cho, S.J. Koh, "Electron Energy Filtering and Cold Electron Transport at Room Temperature: A Route towards Realization of Ultralow-Power-Dissipation Electronics", 5th North

Texas Inter-University Materials Science and Engineering Symposium, Arlington, Texas, April 2014 (**The Best Paper Award (1st place)**)

7. P. Bhadrachalam, R. Subramanian, K. Cho, J. Kim, S.J. Koh, "Effect of Phonon Emission and Absorption in Electron Tunneling through Double Quantum Dots", TMS Annual Meeting, San Antonio, Texas, March 2013 (**Best Graduate Student Paper Award in Nanomaterials (3rd place)**)
8. M. Teimouri, P. Bhadrachalam, S.J. Koh, "Single-Particle Placement Using DNA-Conjugated Nanoparticles", TMS Annual Meeting, San Antonio, Texas, March 2013
9. **(Keynote)** S.J. Koh, "Toward Large-Scale Fabrication of Nanoscale Devices", 2012 KSEA Central Texas Regional Conference, Austin, Texas, May 2012