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2D Crystal Semiconductors New Materials for GHz-THz Devices

Debdeep Jena
UNIVERSITY OF NOTRE DAME DU LAC

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Debdeep Jena
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http://djena.engineering.cornell.edu

Dear Dr. Goretta,

Please find attached our final report for the AFOSR grant on 2D crystal electronics. As per our discussions, the report has the collected publications that resulted from the work, and succinctly summarizes what was achieved as part of this three-year effort.

We remain highly grateful to AFOSR for giving us the opportunity to work on this exciting field of research. Please do not hesitate to ask if you have any questions or concerns.

Yours sincerely,

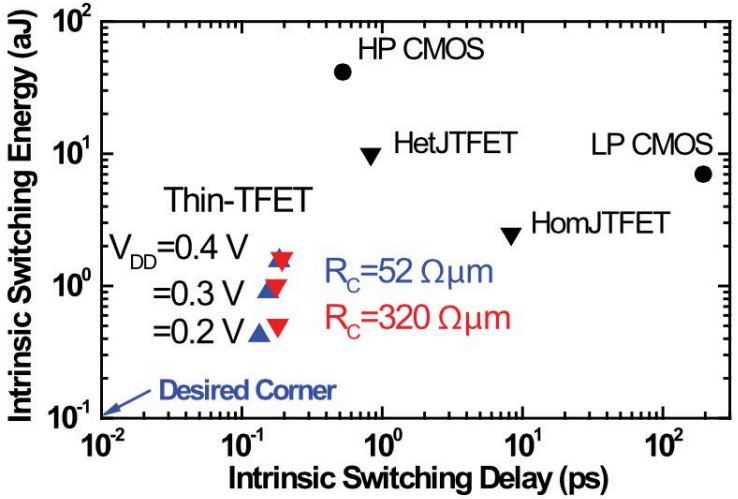
Debdeep Jena

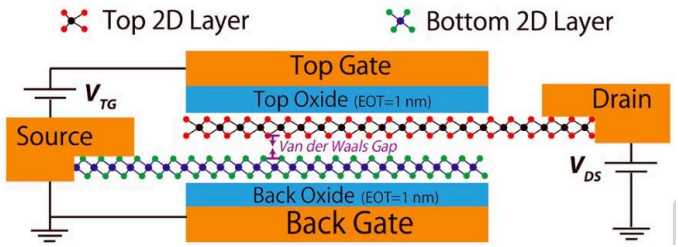
April 3, 2015, Ithaca, NY

Debdeep Jena (djena@cornell.edu) & Co-PI Huili (Grace) Xing
Professor, Departments of ECE and MSE
Cornell University, Ithaca, NY USA 14853

2D Crystal GHz-THz Devices

Debdeep Jena & Grace Xing (Notre Dame)





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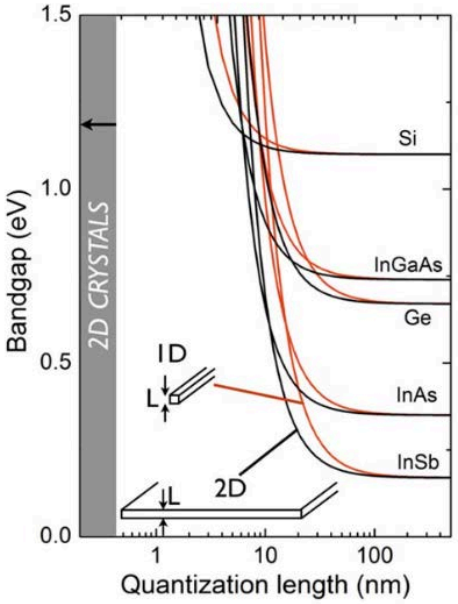
Two-Dimensional Heterojunction Interlayer Tunneling Field Effect Transistors (Thin-TFETs)



Goal: *2D crystals GHz-THz devices*

Bottlenecks & Solutions

Transport: *Tunneling vs mobility*

Contacts: *High Rc*

Epitaxy: *Control of defects*

Related publications with AFOSR support:

1) *IEEE JEDS, 2015, to appear*
2) *JAP 115 074508 (2014)*
3) *APL 102 132102 (2013)*
4) *IEEE Proceedings, 101, 1585 (2013)*

2D Crystal GHz-THz Devices

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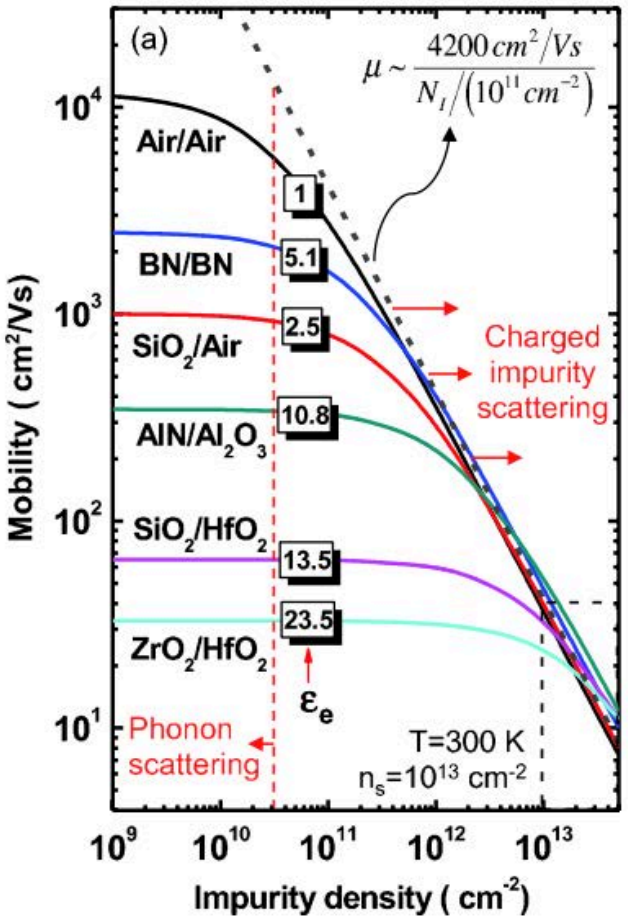

PHYSICAL REVIEW X **4,** 011043 (2014)

Charge Scattering and Mobility in Atomically Thin Semiconductors

Nan Ma* and Debdeep Jena

Department of Electrical Engineering, University of Notre Dame, Notre Dame, Indiana 46556, USA

(Received 25 October 2013; revised manuscript received 16 February 2014; published 18 March 2014)

This award allowed us to do the following for the first time:

1) *Identify the major scattering mechanisms limiting mobility*
2) *Identify methods to improve carrier transport in 2D Crystal semiconductors.*

Goal: *2D crystals GHz-THz devices*

Bottlenecks & Solutions

Transport: *Tunneling vs mobility*

Contacts: *High Rc*

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2D Crystal GHz-THz Devices

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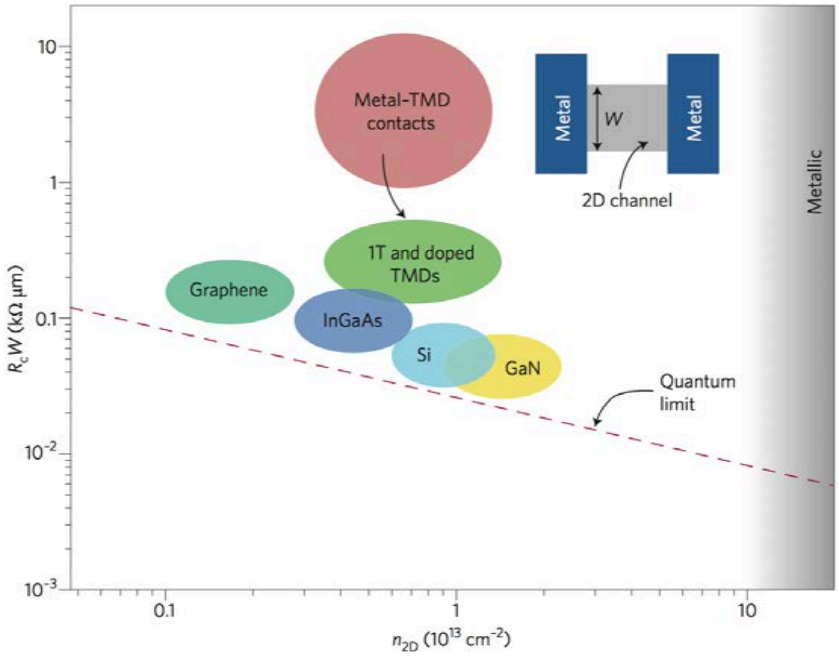
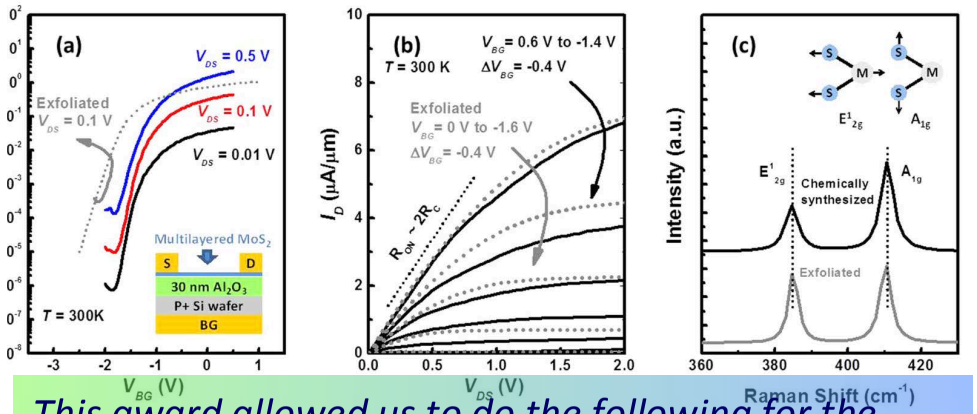


Figure 1 | Contact resistances for various semiconductor materials against the quantum limits for crystalline materials. Using a 1T metallic phase to interface MoS_2 with metals shifts the performance of TMD-based transistors closer to the quantum limit predicted by Landauer and Sharvin. The inset shows a typical transistor configuration.



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Bottlenecks & Solutions
Transport: *Tunneling vs mobility*
Contacts: *High contact resistance*
Epitaxy: *Control of defects*

Related publications with AFOSR support:

1) *APL 102 043116 (2013)*
2) *Nature Materials 13 1076 (2014)*

INVITED PAPER

Tunneling Transistors Based on Graphene and 2-D Crystals

Graphene-based tunneling transistors and how these compare to 2-D transistors made from the GaAs/AlGaAs materials systems is the topic of discussion in this paper.

By Debdeep Jena, *Member IEEE*

ABSTRACT | As conventional transistors become smaller and thinner in the quest for higher performance, a number of hurdles are encountered. The discovery of electronic-grade 2-D crystals has added a new "layer" to the list of conventional semiconductors used for transistors. This paper discusses the properties of 2-D crystals by comparing them with their 3-D counterparts. Their suitability for electronic devices is discussed. In particular, the use of graphene and other 2-D crystals for interband tunneling transistors is discussed for low-power logic applications. Since tunneling phenomenon in reduced dimensions is not conventionally covered in texts, the physics is developed explicitly before applying it to transistors. Though we are in an early stage of learning to design devices with 2-D crystals, they have already been the motivation behind a list of truly novel ideas. This paper reviews a number of such ideas.

KEYWORDS | Graphene; semiconductors; transistor; tunneling

I. INTRODUCTION

Semiconductors come in many crystal forms. Since their discovery in the early 20th century, the semiconductors used in electronic and optical devices are of the 3-D crystal form. Three-dimensional crystal semiconductors have remained at the heart of such devices from the earliest "cat's whisker" detectors [1] to the latest billion-transistor silicon complementary metal–oxide–semiconductor (CMOS) [2], [3] and quantum-well (QW) lasers [4]. As the understanding of the physics of electron transport and electron–photon coupling sharpened, it became clear that controlling the potential energy landscape of electrons could lead to massive boosts in device functionality and performance.

The first level of direct control of the "energy-band diagrams" was by chemical doping, which involved replacing a small number of atoms of the 3-D semiconductor by those with higher or lower valence. The next advance involved varying the chemical nature of the crystal along specific directions, which marked the birth of semiconductor heterostructures [5]. These advances taught electrons "new tricks," and made possible the smallest and fastest electronic switches [6], high-density memories, and the most efficient light-emitting diodes (LEDs) and lasers [7]. These devices form the bedrock of computation, data storage, solid-state lighting, and communication in today's information age.

At this time, in the early part of the 21st century, these building blocks based on traditional device concepts are approaching their performance limits. Therefore, new ideas and new materials are necessary. For example, photonic crystal, metamaterial, and plasmonic concepts are advancing the area of optoelectronic devices beyond what was thought possible before [8], [9]. Strong light–matter interaction has been exploited to demonstrate polariton lasers that take advantage of Bose–Einstein condensation at room temperature for ultralow threshold lasing [10].

Similarly, for electronic switching devices, a number of approaches are being taken to address the future beyond scaling. Conventional field-effect and bipolar transistors operate on the basis of energy filtering of electrons (or holes) flowing over a barrier. The barrier is electrostatically controlled with a voltage. In an electrostatically well-designed device, all of the control voltage is spent in

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The author is with the University of Notre Dame, Notre Dame, IN 46556 USA (e-mail: djena@nd.edu).

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moving the barrier. The electrons carrying the current are spread in a band according to the Fermi–Dirac distribution, with a Boltzmann tail in energy. The energy filtering thus leads to a current dependence of the form $I \sim \exp[qV/k_BT]$, where q is the electron charge, V is the voltage, T is the temperature, and k_B is the Boltzmann constant. When operated in this fashion, the current cannot be changed any steeper than $S \sim (k_BT/q)\ln 10 \sim$ 60 mV/decade. This subthreshold swing (SS) "limit" is often referred to as the "thermal limit" or the "Boltzmann limit" (though Boltzmann did not set this limit). We refer to this condition as the SS limit to avoid confusion.

An electronic switch must have its ON- and OFF-states clearly demarcated for performing digital (Boolean) logic. Let us say this demarcation is set to $I_{ON}/I_{OFF} = 10^4$. To achieve it, a voltage supply of at least 4×60 mV $= 0.24$ V is necessary. Since the speed of switching and the dynamic and static power dissipation of transistors are strong functions of the supply voltage, the SS limit sets a floor of minimum power dissipation. This issue is described in sufficient detail in a number of recent articles that motivate the search for new materials and ideas for going beyond the SS limit [11]–[13].

Now there is nothing particularly fundamental about the SS limit. Devices that do not operate on the traditional transistor mechanism exist today and operate below the SS limit. An example is a nanoelectromechanical system (NEMS), which is the analog of a mechanical relay. Substantial progress has been made in this area [14]. Due to mechanical moving parts, these devices are currently slow, but are expected to improve with scaling.

A number of relatively new ideas are being explored at this time for switching devices beyond the SS limit. Some exploit impact ionization to obtain sub-SS limit operation [15], [16]. Other devices aim to use correlated electron effects; for example, if electrons can be made to "pair up" similar to Cooper pairs in superconductors, but at room temperature, the SS limit would be cut in half. If the control voltage could be internally "stepped up" through novel ferroelectric gates, sub-SS limit devices can be realized [17]. Other routes involve the internal transduction of the voltage into other state variables such as strain, spin, or electron localization [18]. Among these strategies, a transistor concept based on interband tunneling transport has emerged as an attractive candidate for switching. This paper will focus on this device. The tunneling field-effect transistor (TFET) can be realized in traditional 3-D crystal semiconductors and their heterostructures.

However, since the discovery of graphene in 2004, device engineers have a new class of materials in 2-D crystals at their disposal. In this paper, we discuss possible realizations of TFETs with 2-D crystals, and compare them with 3-D crystal counterparts. In the process of this discussion, a number of novel features of 2-D crystals will emerge that distinguish them from traditional 3-D crystal semiconductors. These novel features of the new material family offer a compelling case for investigating them further. To motivate their suitability for electronic devices, we first discuss the various 2-D crystal materials and their properties. We do so against the backdrop of their ubiquitous 3-D crystal semiconductor counterparts.

II. TWO-DIMENSIONAL CRYSTALS

Two-dimensional crystals exploded into the limelight in 2004 with the remarkable reports of the isolation of atomically thin graphene [19]–[21]. What is often overlooked is that the early reports [22] also presented evidence of the isolation of single-layers of BN—an insulator or a wide-bandgap semiconductor, MoS_2—a traditional semiconductor, and $NbSe_2$—a superconductor with possible charge-density wave electronic phases. Single layers of the cuprate high-T_c superconductors were also isolated. It is interesting to note that the voltage "scaling" of silicon CMOS processors stalled around the same time, marking the move toward multicore processors [23]. One of the reasons for paradigm shift was the unsustainable increase in dynamic and OFF-state power dissipation due to the SS limit and high-frequency operation. Whether 2-D crystals can help in this arena remains to be seen. We first discuss a few properties of 2-D crystals and their suitability for electronic devices.

Fig. 1 is a schematic representation of the structure of crystals of various dimensions. The bottom row shows the atomic building blocks. The first column shows the ubiquitous 3-D crystal semiconductors. The second column shows the emerging family of 2-D crystals and their many variants. The third and fourth columns indicate ideal 1-D and 0-D structures. Atomic chains have been investigated for their transport properties [24], and a benzene ring can be considered either as an atomic "ring," or even a basic 2-D crystal unit. An atom is a perfect 0-D structure in which electrons are localized in all three dimensions. We note that the electrons in an atom still move in 3-D, but their energy spectra are discrete and gapped; they do not form bands that are necessary for transport. It is in this sense that they are 0-D. We focus our attention on 2-D crystals, and their differences from 3-D crystal semiconductors.

The building blocks for 3-D semiconductors are typically tetrahedrally bonded atoms. The lattice is 3-D, and the basis typically consists of two atoms. For example, electrons in 3-D crystals from group IV elements (Si, Ge, etc.) occupy [core] ms^2mp^2 orbitals, where m is the row number in the periodic table, and [core] represents the core electrons that do not participate in chemical bonding directly. Electrons from the outermost s and p orbitals of nearest neighbor atoms pair up to form sp^3 bonds. An sp^3 bond is inherently 3-D, and so is the

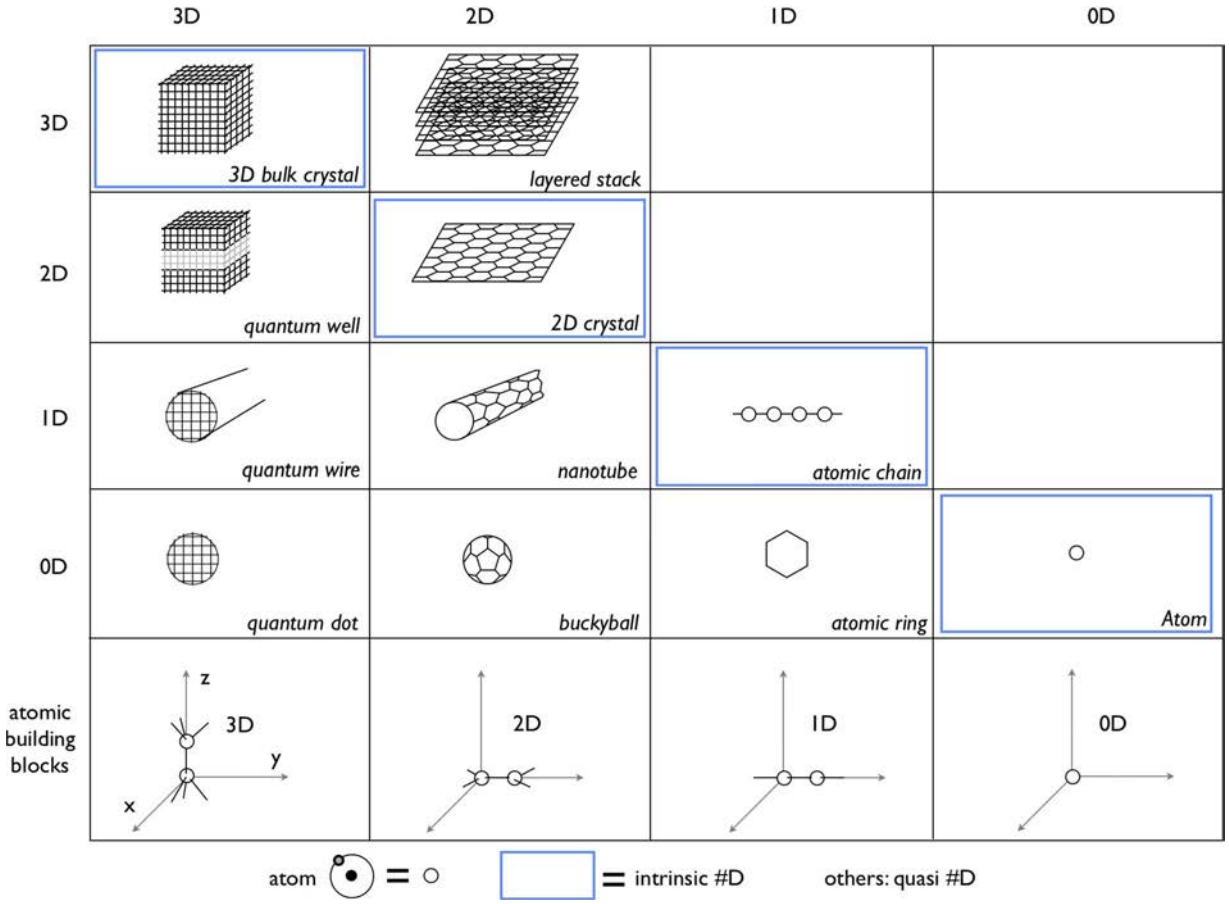

Fig. 1. *A schematic representation of "crystals" of the many spatial dimensions that result from various building blocks. The building blocks contain atomic bases that form 3-D bonds in the first column, 2-D planar bonds in the second column, and 1-D linear bonds in the third column. The ideal 0-D structure is an atom in the fourth column.*

resulting semiconductor crystal. The natural crystal is thus a bulk 3-D semiconductor. A termination such as a surface results in dangling bonds, a fraction of which might reconstruct.

The corresponding building block of a 2-D crystal consists of a *planar* 2-D lattice. For graphene and BN, the basis consists of two atoms attached to a hexagonal planar lattice. These chemical bonds in the two-atom basis for graphene and BN are of the sp^2 type. So the chemical bonds of their basis are *also* planar. In the second column of Fig. 1, the underlying planar structure of 2-D crystals is shown. Attached to each point of intersection is one carbon atom for graphene, alternating B and N atoms for BN, and a basis of X-M-X for transition metal dichalcogenides (TMDs). TMD 2-D crystals share the same planar lattice geometry of graphene and BN. But the basis of TMD 2-D crystals consists of three atoms of the form MX_2, where M is the transition metal chemically bonded to two chalcogenide atoms X. The chemical bonds in TMD 2-D crystals (e.g., MoS_2, WSe_2, WS_2, etc.) involve s-, p-, and d-orbitals, and the two M-X bonds stick out of the center 2-D plane containing the transition metal atom M [25]. Thus, unlike its lattice, the basis of TMD 2-D crystals is not perfectly planar. Recent reports also indicate the possible existence of 2-D forms of Si (silicene), Ge (germanene), and possibly AlN and GaN [26]–[28], [102]. Single layers of 2-D crystals are typically less than 1 nm in thickness. An exotic form of a 2-D crystal semiconductor may also exist when two surfaces of topological insulators come close to each other [29]. These materials have been less explored than the others discussed here.

Unlike a perfect 3-D crystal, a perfect 2-D crystal has no broken/dangling bonds on its surface. The quasi-low-dimensional structures formed from 3-D crystals such as 2-D nanomembranes, 1-D nanowires, and 0-D nanocrystals are still volume elements deriving from 3-D bonding, and necessarily have dangling bonds on their surfaces. These broken bonds may be passivated by either dielectrics, or by lattice-matched or strained heterostructures. In contrast, the various dimensional structures deriving from 2-D crystals are "hollow" and are "all-surface."

Two-dimensional crystal sheets may be stacked to form 3-D structures with weak van-der-Waal's interlayer bonding. They can be rolled up into quasi-1-D nanotubes, or into 0-D buckyballs (C_{60}). The symmetry of a 2-D crystal is broken at its *edge*. Similar to the surface state reconstruction or passivation of the surfaces of 3-D crystals, the edge states can reconstruct and tie up the dangling bonds. For special cases, such as in buckyballs, the chemical bonding is seamless and there are no broken bonds. Indeed, the icosahedral geometry of the buckyball belongs to one of the five platonic solids, which have mathematically represented "perfection" in shape since the earliest times [30], [31].

For electronic devices using field effect, the *absence of dangling bonds* is a major advantage for planar 2-D crystals, since electrons trapped in them serve to shield electric field lines from entering the bulk of the corresponding 3-D semiconductors. We now discuss the electronic properties of 2-D crystals and compare them to those of 3-D crystal semiconductors.

A. Electronic Properties of 2-D Crystals

The electronic orbitals that form the family of 2-D crystals are shown in Fig. 2. Electron states at the conduction and valence band edges of 3-D semiconductors derive from various admixtures of sp^3 bonds. For direct-gap semiconductors such as GaAs and GaN, the conduction band edge is mostly s-like. The spherical symmetry of the s-orbitals imparts electrons in the conduction band their isotropic nature. The electronic states at the valence band edge on the other hand are more p-like. Because p-orbitals are directional, the hole effective mass is anisotropic. The imbalance of the nature of chemical bonding in 3-D crystals semiconductors thus also results in an *asymmetry* in the curvature or the effective mass of the conduction and valence band states. In modern complementary logic devices, symmetry is a highly desirable characteristic. The degree of asymmetry between, for example, nMOS and pMOS devices dictates the geometry and layout of circuits that could be considerably simplified by symmetry.

The covalent bonds in graphene and BN are of the sp^2 kind. They are responsible for the structural properties of the crystal. The leftout p_z orbital sticks out of the 2-D plane. The electrons in these orbitals can hop between nearest neighbors, leading to the electronic conductivity and optical properties of such crystals. In graphene and BN, the structural properties such as thermal conductivity and mechanical stability derive from the covalent sp^2 bonds. But the electronic and optical properties derive from the delocalized p_z orbitals. There is a wide energy separation between the sp^2 and p_z energy bands. In this sense, the electronic properties of such 2-D crystals have a different origin than their structural properties. This is in contrast to 3-D semiconductors, where the structural and electronic properties derive from the same sp^3 electronic band states.

Electrons in 3-D crystals can be quantum-mechanically confined to move in 2-D and 1-D, or localized in 0-D by chemical and geometrical constraints in heterostructures, as shown in the first column in Fig. 1. This is achieved by taking advantage of energy band offsets around the bandgap. Conduction band offsets ΔE_C confine electrons, and valence band offsets ΔE_V confine holes. We note here

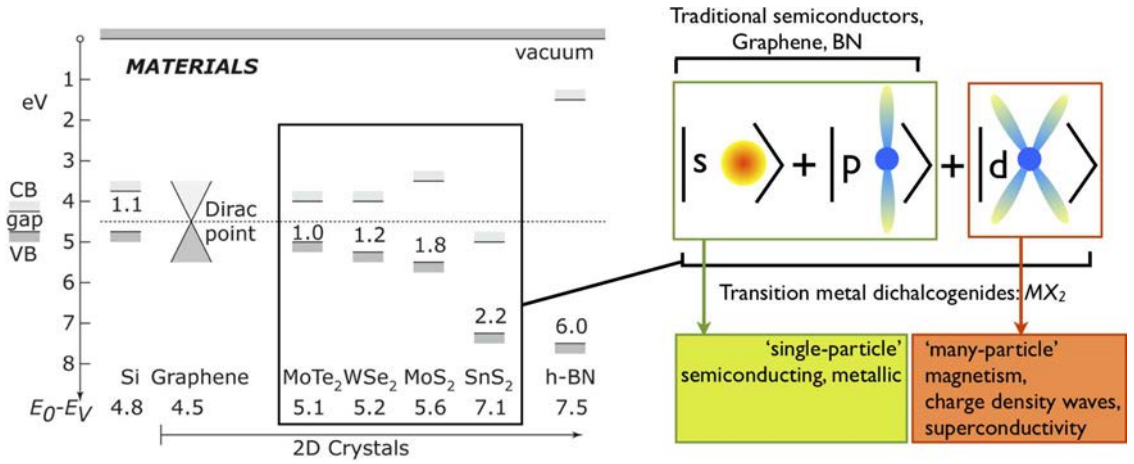

Fig. 2. *Energy band alignments of various 2-D crystals compared to silicon. The relative energy band offsets of graphene, BN, and transition-metal dichalcogenides are shown. The numbers at the center indicate the respective bandgaps reported at this time, but are subject to refinement with further experiments. An energy scale from the vacuum level is also indicated, showing a work function (or electron affinity) of intrinsic zero-gap 2-D graphene to be ~4.5 eV. The conduction and valence band edge states of Si, graphene, and BN are formed of linear combinations of |s>- and |p>-orbitals, whereas those of the transition-metal dichalcogenide 2-D crystals involve |d>-orbital states at the band edges. The presence of d-orbital states near the Fermi level implies that some of these 2-D crystals can exhibit electronic phenomena that require many-particle effects such as magnetism and superconductivity.*

that the 2-D confinement of electrons in a quantum well in a 3-D crystal leads to a quasi-2-D electron gas (2-DEG). This means there are multiple 2-D electronic subbands whose spacing in energy grows as the inverse square of the spatial confinement. In sharp contrast, there is just *one* band for 2-D electron systems in single-layer 2-D crystals, since the electron wave function cannot spread sufficiently out of the plane in equilibrium.

The energy bandgaps and the band lineups of a few 2-D crystals are shown in Fig. 2. The figure also indicates the chemical bonding schemes that characterize them, along with their relative positions with respect to the vacuum energy level [32]–[34]. A distinctive feature of the 2-D crystals is that their energy gap windows are not populated by surface states in sufficiently crystalline sheets, as is necessarily the case for 3-D crystals. Thus, the measurements of their band alignments are relatively simpler, as described in [33].

Graphene is a zero-bandgap semiconductor, with the energy dispersion $E(k_x, k_y) = \pm\hbar v_F|\mathbf{k}|$, where $\hbar$ is the reduced Planck's constant, $v_F = 10^8$ cm/s is called the Fermi velocity, and $|\mathbf{k}| = \sqrt{k_x^2 + k_y^2} = 2\pi/\lambda$ is the electron wave vector. The dispersion is taken around the Dirac points in the band structure, which are located at the twofold degenerate K-points in the k-space, as shown in Fig. 3. These states are similar to the conduction band edge or valence band edge states of 3-D semiconductors. The positive branch is the conduction band, and the negative branch is the valence band. We note the perfect symmetry of the bands, which is quite distinct from traditional 3-D semiconductors. This symmetry is special, and has an important bearing on tunneling transistors discussed later. The energy bandgap is zero. The density of states (DOS) of 2-D graphene is given by $\rho_{gr}^{2\text{-D}}(E) = [g_s g_v/2\pi(\hbar v_F)^2] \times |E|$, where $g_s = 2$ is the spin degeneracy and $g_v = 2$ is the valley degeneracy [35].

Two-dimensional BN has an energy bandgap of ~6.0 eV as a consequence of the broken crystal symmetry in the basis, but its band extrema also occur at the K-points in the Brillouin zone. Thus, it has the same valley degeneracy as graphene. The effective mass characterizing the symmetric conduction and valence bands of 2-D BN is $m^* \sim 0.6m_0$, where m_0 is the free-electron mass [36]. The DOS of 2-D BN looks like those of conventional 2-DEGs, $\rho_{\text{BN}}^{2\text{-D}}(E) = (g_s g_v m^*/\pi\hbar^2) \times \theta[E - E_C]$. The major difference is the absence of higher subbands owing to the absence of atoms out of the plane.

The bandstructures of 2-D crystal semiconductors of the TMD family are being evaluated at this time [37], [38]. Initial experiments and theoretical models point out that they too have their band extrema at the K-points. The conduction and valence bands in single-layer TMDs appear less symmetric than graphene and BN, but much more symmetric than traditional 3-D semiconductor crystals. Effective masses ranging from $m^* \sim 0.34m_0 - 0.76m_0$ have been calculated, and are expected to undergo refinement through experimental measurements [39].

Two-dimensional crystal sheets typically occur in nature in their stacked layered forms. The band structures of the multilayer variants of graphene, BN, and TMDs are distinct from the single-layer counterparts. The bandgap of a stacked 2-D crystal is smaller than the single layer [40], [41]. For example, graphite becomes a semimetal with a negative bandgap. Similarly, when 2-D crystals are used to form 1-D nanotubes (Fig. 1), quasi-1-D subbands appear, and the bandgaps increase due to additional quantum confinement. The DOS then acquires van Hove singularities in a manner similar to quasi-1-D nanowires or quantum wires formed of 3-D semiconductor crystals. In this paper, we maintain focus on single-layer 2-D crystals and occasionally mention their quasi-1-D and quasi-3-D variants when they appear in context. The discussion of the electronic band structures of 2-D crystals leads us naturally to a point where we can gauge their suitability for electronic devices. We start by discussing their suitability for traditional field-effect transistors (FETs).

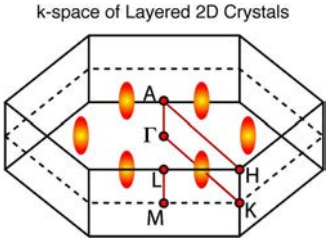

Fig. 3. *The k-space picture of 2-D crystals such as graphene, BN, and the transition-metal dichalcogenide MX_2 compounds. A good understanding of the k-space picture is important for choosing the right materials for device applications, and especially important for tunneling transistors. Since the real-space lattice is hexagonal in the 2-D plane, so is the k-space lattice. Since the interlayer separation is larger than the in-plane lattice constant, the hexagonal Brillouin zone is shorter in the vertical direction. The important high-symmetry points are labeled. Graphene, BN, and single-layer MoS_2 have their conduction band edge and valence band edges at the K-points, which leads to twofold degeneracy. The conduction band edge of multilayer MoS_2 at this point is believed to be along the $\Gamma - K$ minimum as shown, which makes it an indirect-bandgap semiconductor, and imparts to it a valley degeneracy of 6 by symmetry, similar to silicon.*

B. Suitability of 2-D Crystals for Traditional Transistors

The operation of a FET hinges on electrostatics and transport of charge carriers. FETs based on 3-D crystal semiconductors have been scaled to ~10 s of nanometer channel lengths in the quest to achieve higher performance. As the source/drain separations have been scaled, it has become necessary to reduce the channel thickness. This requirement is driven by the need for a gate metal to exercise electrostatic control over mobile electrons and holes. If the gate is farther away from the carriers than the S/D distance, it loses control over them. The device then

cannot be switched on or off as effectively as is needed for the transistor to operate in a circuit. This necessity is at the root of the reason for the move to silicon-on-insulator (SOI) and FinFET type of topologies [42]. The silicon channels have thus become more 2-D in SOI structures [43], and closer to 1-D in FinFETs and nanowire geometries.

A quantitative statement of the importance of electrostatics is obtained from a solution of the Poisson equation for a FET. For a FET with a semiconductor layer of thickness t_s of dielectric constant ε_s gated through an insulator of thickness t_{ox} and dielectric constant ε_{ox}, the Poisson equation for the electric potential V takes the form $\partial_x^2 V \sim V/l^2$, where $l = \sqrt{t_s t_{ox}(\varepsilon_s/\varepsilon_{ox})}$ is the characteristic "scaling length" [44]. This length determines the smallest distances over which electric potential may be dropped. Therefore, for scaling to the smallest lengths, high-K insulators and ultrathin channels are desirable. This argument, in conjunction with the absence of dangling bonds and the associated interface traps highlights the attractive feature of 2-D crystals for ultrascaled FETs based on electrostatics arguments alone. Furthermore, 2-D crystal insulators such as BN can eliminate dangling bonds altogether in planar FET geometries.

As the channels of 3-D semiconductors are thinned down, the roughness of the surfaces causes degradation of the carrier transport due to surface-roughness scattering. The root of this form of scattering is the effect of the roughness on the quantization of energy levels. For example, in a SOI structure of thickness t, the quantization energy of subbands varies as $E \sim \hbar^2/m^* t^2$. Variation of the layer thickness by Δt leads to a perturbation of the subband edge by $\Delta E \sim (2\hbar^2/m^* t^3)\Delta t$. Since the scattering rate is proportional to the square of the perturbation, the mobility degrades as $\mu \sim t^6$, i.e., roughly as the sixth power of the width [45]. Thus, for very thin layers of a 3-D semiconductor, such as those used in ultrathin body (UTB) transistors, the transport properties suffer from the surface roughness. Two-dimensional crystals offer an ideal solution to this problem. Two-dimensional crystals are intrinsically of an atomically thin body (ATB) nature. When sufficiently pure, they do not have surface roughness. The attractiveness of TMD 2-D crystal semiconductors was brought to sharp focus with the demonstration of single-layer MoS_2 FETs [46]. A FET with 10^8 ON/OFF ratio at room temperature and electron mobility of $\sim$200 cm^2/Vs was achieved with a single layer of MoS_2 2-D crystal of thickness < 1 nm. The SS was close to ideal, thanks to the absence of broken bonds and associated interface traps. Such performance has never been measured in devices made from 3-D crystals of the same thickness. Though the initial results look promising, the dynamic range and reliability of the performance metrics will be assessed carefully in the next few years.

Additional novel features of charge transport in 2-D crystals that have been predicted and recently observed include dielectric-mediated carrier mobilities. The basic premise is that the Coulomb interaction $V \sim q/4\pi\varepsilon r$ between charged impurities and mobile channel carriers is mediated by the dielectric constant ε of the space separating them. In 3-D semiconductors, the Coulomb interaction is dominated by the bulk dielectric constant of the semiconductor itself (i.e., $\varepsilon = \varepsilon_s$) since the charged impurity and the charge carrier are effectively buried inside and in close proximity. On the other hand, in 2-D crystals, most of the electric field lines connecting the charged impurity to the mobile carrier actually lie *outside* the 2-D crystal itself, in the surrounding dielectric. This effectively provides an external knob to damp Coulomb scattering and improve carrier mobilities, since $\varepsilon \sim \varepsilon_{ox}$ for this interaction [47]. Use of high-K dielectrics has been observed to damp scattering and improves charge mobility in 2-D crystals such as graphene [48], [49] and MoS_2 [46]. The exact mechanisms likely also include phonons.

At this time, the understanding of transport in 2-D crystals is evolving. It is clear that the interactions that limit charge transport in 3-D semiconductors and heterostructures were intrinsic to the 3-D crystal itself. But for 2-D crystals, these interactions can be tuned based on what we put around them. This is because in 2-D crystals we have direct access to the electrons, their spins, and atomic vibrations to an unprecedented degree. As our understanding of these mechanisms evolves, the level of direct access to the physical properties may well prove to be *the* defining factor that differentiates 2-D crystal devices from their 3-D counterparts. This feature is simultaneously an advantage *and* a challenge, since noise and reliability of the desired nanoscale devices must be robust for usability.

C. Possibility of 2-D Crystal Heterostructures

Heterostructures based on 3-D crystals take advantage of energy band offsets that originate from differences in chemical composition. The concept of quasi-electric fields in heterostructures breaks the symmetry of electrical forces acting on electrons and holes. In a semiconductor of constant chemical composition (uniformly doped, or p-n homojunctions), the electric force acting on electrons and holes is the same. This is not true in a heterostructure [5]. This broken symmetry is central to quantum confinement and high oscillator strengths that have led to high-efficiency LEDs and lasers. QW FETs and even the MOSFET gain from the concept of quantum confinement. In graded-base heterostructure bipolar transistors (HBTs), the broken symmetry is central in speeding up electrons with a quasi-electric field in the same region in space where there is no field acting on holes [50]. Examples of such heterostructures based on 3-D crystal semiconductors include SiGe/Si, AlGaAs/GaAs/InGaAs, and AlGaN/GaN/InGaN material systems. Except in special cases, most of such 3-D crystal heterostructures have strain due to the lattice mismatch. Strain can be desirable for affecting the carrier

transport or as the driving force for the formation of quantum dots by the Stranksi–Krastanov mechanism during epitaxy. Strain can often be undesirable, since it can lead to relaxation and defect formation beyond certain critical thicknesses.

Heterostructures based on 2-D crystals are at their infancy. However, a number of interesting features are likely to emerge in them. Initial demonstrations of in-plane 2-D crystal heterostructures such as graphene seamlessly connected to BN have been experimentally observed, and provide exciting opportunities in device design [51]. Hybrid heterostructures composed of 2-D crystals such as graphene placed on 3-D semiconductors such as silicon have been used to demonstrate new device concepts. One recent example is a graphene–Si Schottky diode where graphene may be thought of as the Schottky "metal" contact. However, unlike a typical metal, the Fermi level of graphene can be tuned with a third gate electrode, which leads to a variable Schottky-barrier height [52]. This idea was used to demonstrate a variable-barrier transistor (or the so-called "Barristor").

Out-of-plane or vertical heterostructures are also realized when 2-D crystals are stacked on each other. Such heterostructures do not suffer from lattice mismatch requirements, since there are no interlayer covalent bonds. The weak van der Waal's interlayer bonding in principle allows unstrained integration of 2-D crystal layers of different material properties. One may envision vertical heterostructures of 2-D crystal metals, semiconductors, insulators, and perhaps a wider range of materials. Due to the absence of broken bonds, the interfaces are expected to be pristine and devoid of electronic trap states. Interlayer transport of electrons would involve tunneling. The rotational alignment of the 2-D crystal layers might play an important role in such heterostructures. These features are currently under investigation, and are certain to lead to a range of new applications. Initial demonstrations of a graphene–BN–graphene and graphene–MoS_2–graphene heterostructures tunneling transistors have been recently reported [53]. A proposed device called the bilayer pseudospin FET (BiSFET) is based on many-body excitonic condensation of electron–hole pairs in closely spaced layers of graphene. It falls under the category of vertical 2-D crystal heterostructures [54]. Its single-particle counterpart, a tunneling transistor that takes advantage of the symmetry of the bandstructure of some 2-D crystals, is called the "SymFET" [55]. These tunneling devices that are rooted in 2-D crystals are described in Section V.

D. Maturity of 2-D Crystals and Material Challenges

Since the field of 2-D crystal semiconductors is relatively young, a short discussion of the material challenges is necessary. Since the initial demonstrations in 2004, the large-area growth capability of single-layer graphene has expanded rapidly [21]. At this time, epitaxial single-layer graphene on several-inch-diameter SiC wafers are available [56], [57]. Chemical vapor deposition (CVD)-grown graphene has been realized on metals, and transferred to other substrates [58]. Nanoribbons have been fabricated on CVD-grown graphene [59]. CVD-grown graphene has shown promise for larger area crystals than epitaxial graphene, which is limited to the size of the starting 3-D crystal substrate. The crystal quality is not perfect yet, but as was the case in the development of 3-D crystals, there is reason to believe it will undergo drastic improvements in the near future.

Similarly, BN 2-D crystals have been grown by CVD, as have electronic-grade MoS_2 and WS_2 layered materials [60]–[62]. However, it is also important to realize that most forms of 2-D crystals have been produced in large volumes in their layered forms [63]. They have already found industrial applications in chemical catalysis (MoS_2, graphite), lithium–ion batteries (lithium cobaltate and layered carbon), lubricants (MoS_2), neutron moderation in nuclear reactors (graphite), and thermally and mechanically refractory crucibles used in much of electronic material and device processing (BN and graphite). The development of electronic grade counterparts thus is expected to heavily leverage the considerable prior existing knowledge and industrial base for these materials.

A major immediate challenge is to develop methods of doping and controlling the Fermi level in 2-D crystals. Possible methods with TMD 2-D crystals include chemical substitutional doping, and/or modulation doping by taking advantage of the rich intercalation chemistry of such layered materials. Since doping control is intimately connected to the ability to form low-resistance contacts, this challenge assumes increased importance.

The development of electronic grade 2-D crystals is expected to be rapid. The first active device applications are expected to be in traditional FETs. For example, TMD-based transistors offer attractive routes to large-area thin-film transistors (TFTs) by virtue of low SS values and respectable mobilities when compared to organic semiconductors and 3-D oxide materials [64]. But can they offer new functionalities for high-performance devices beyond what is being envisioned with 3-D crystal semiconductors? To address that question, we focus the rest of the paper on one of the possible candidates for high-performance and low-power energy-efficient logic devices: the tunnel FET (TFET).

III. TUNNELING TRANSPORT IN SEMICONDUCTORS

Following the motivation provided earlier, we start with a short introduction to tunneling transport and its incorporation into the heart of the transistor operation. The discussion starts with an evaluation of the effect of dimensionality on interband Zener tunneling [65], [66].

Consider the $p - i - n$ junction shown in Fig. 4. We make some simplifying assumptions that allow us to zone

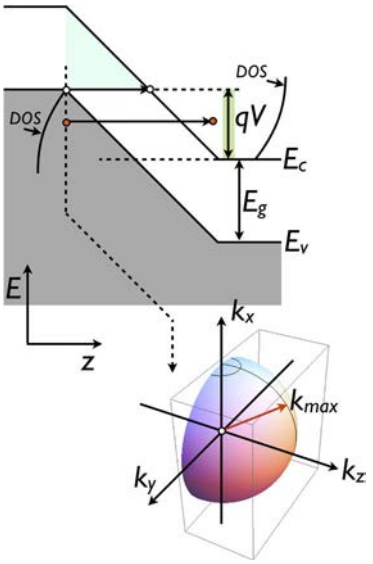

Fig. 4. *Interband tunneling in a reverse-biased $p-i-n$ junction diode. Most TFETs use the reverse-bias Zener tunneling as the mechanism of current conduction in their ON-states. The current may be calculated by integrating over the k-states at the injection point as outlined in the text.*

into the relevant physics immediately. Assume the doping in the p- and n-sides are just enough to align the Fermi levels at the respective band edges. Then, under no bias, $E_V^p = E_c^n$ and no net current flows across the junction. Under the application of a reverse bias voltage V, a finite energy window is created for electrons since $E_V^p - E_C^n = qV$. Within this energy window, electrons from the valence band can tunnel into the conduction band on the other side, as indicated.

The current is calculated by summing the individual contributions by each k-state electron. There are many approaches to evaluate currents, but none is as transparent as the formalism in the k-space. To illustrate, we write the tunneling current as

$$I_T = q\frac{g_s g_v}{L}\sum_k v_g(k)(f_v - f_c)T \tag{1}$$

where $g_s = 2$ is the spin degeneracy and g_v is the valley degeneracy. L is the macroscopic length along the electric field (which will cancel out), $v_g(k) = \hbar^{-1}\nabla E(k)$ is the group velocity of carriers in the band $E(k)$, f_v, f_c are the Fermi–Dirac occupation factors of the valence and conduction bands, and T is the tunneling probability. The sum is over k-states for electrons that are allowed to tunnel. We illustrate the clarity of this approach by using the same expression for evaluating Zener tunneling currents for $p-i-n$ junctions made of 3-D, 2-D, and 1-D crystals. We first consider semiconducting crystals that have a bandgap. Then, we remove the bandgap criteria to allow for special cases such as graphene.

The tunneling probability is obtained by the Wentzel–Kramers–Brillouin (WKB) approximation [67]. For electrons in the valence band of the p-side with transverse kinetic energy $E_\perp = \hbar^2 k_\perp^2/2m_v^*$, the WKB tunneling probability is given by [68]

$$T_{\mathrm{WKB}} = \exp\left[-\frac{4\sqrt{2m_R^*}(E_g + E_\perp)^{\frac{3}{2}}}{3q\hbar F}\right] \approx T_0 \exp\left[-\frac{E_\perp}{\overline{E}}\right] \tag{2}$$

where $T_0 = \exp[-4\sqrt{2m_R^*}E_g^{3/2}/3q\hbar F]$, $\overline{E} = q\hbar F/2\sqrt{2m_R^* E_g}$, F is the (constant) electric field in the junction, and m_R^* is the reduced effective mass given by $m_R^* = m_c^* m_v^*/(m_c^* + m_v^*)$. This expression is found to be consistent with experimental results [69]. Note that the tunneling probability of electrons is lowered exponentially with their transverse kinetic energy. To evaluate the tunneling current, we attach this tunneling probability to each electronic k-state, and sum it over all electrons incident on the tunneling barrier.

Three-dimensional semiconductors: Consider the case when the $p-i-n$ junction is made of 3-D crystal semiconductors. In Fig. 4, we concentrate on a particular 2-D plane as shown by the dashed line, at the $p-i$ junction. Half of the electrons in the valence band in that plane move to the right in the $+k_z$ direction, as indicated in the hemisphere in the k-space. Since there are negligible electrons in the conduction band in that plane, the current there must be carried by electrons in the valence band. But which of these right-going electrons are allowed to tunnel through the gap? In the absence of phonon scattering, tunneling is an elastic process. This enforces the energy requirement

$$E_v^p - \frac{\hbar^2}{2m_v^*}\left(k_{xp}^2 + k_{yp}^2 + k_{zp}^2\right) = E_c^n + \frac{\hbar^2}{2m_c^*}\left(k_{xn}^2 + k_{yn}^2 + k_{zn}^2\right) \tag{3}$$

with the additional requirement that the lateral momentum be conserved. To simplify the analytical treatment, and in preparation for 2-D crystals, we further assume that the bands are symmetric, i.e., $m_c^* \approx m_v^* = 2m_R^*$. The energy and momentum conservation requirements thus lead to the relation

$$2k_\perp^2 + k_{zp}^2 = \frac{4m_R^* qV}{\hbar^2} - k_{zn}^2 \tag{4}$$

where $k_\perp^2 = k_{xp}^2 + k_{yp}^2$. Let us define $k_{\max}^2 = 4m_R^* qV/\hbar^2$. Since there is an electric field in the z-direction, momentum in that direction will not be conserved. For the

electron to emerge on the right (n-)side, k_{zn} must be nonzero, and thus $k_{zn}^2 \geq 0$, which implies

$$2k_{\perp}^2 + k_{zp}^2 \leq k_{\max}^2. \tag{5}$$

The above condition defines a restricted volume Ω_T of the k-space hemisphere for electron states that are allowed to tunnel. We are now in a position to evaluate the tunneling current for 3-D semiconductor $p-i-n$ junctions. In the expression for the tunneling current [see (1)], the group velocity term is that of the valence band k-state $v_g(k) = \hbar k_z/m_v^*$. We skip the p- or n-subscripts, since it is clear that the electrons tunnel from the valence band. The expression for the tunneling current is then

$$I_T = q\frac{g_s g_v}{L_z}\sum_{(k_x,k_y,k_z)\in\Omega_T}\frac{\hbar k_z}{m_v^*}(f_v - f_c)T_0\exp\left[-\frac{\hbar k_{\perp}^2}{2m_v^*\overline{E}}\right]. \tag{6}$$

The sum over k-states is converted into an integral via the recipe $\sum_k(\ldots) \rightarrow L_xL_yL_z/(2\pi)^3 \times \int dk_x dk_y dk_z(\ldots)$. To evaluate the tunneling current in the restricted volume, we use spherical coordinates $(k_x, k_y, k_z) = (k\sin\theta\cos\phi, k\sin\theta\sin\phi, k\cos\theta)$ to obtain the restricted k-space volume $k^2 \leq k_{\max}^2/(1+\sin^2\theta)$. This relation is representative of the "filtering" brought about by the requirements of energy and momentum conservation. Electrons incident normal to the junction have no transverse momentum. For them $\theta = 0$, and they are allowed to tunnel. The number of electron states allowed to tunnel reduces as their transverse directed momentum increases. The current carried by these states with transverse momentum is further damped by the $\exp[-E_{\perp}/\overline{E}]$ factor, leading to further filtering and momentum collimation.

To evaluate the current, the integral in k-space should be evaluated. To simplify the evaluation in 3-D without losing much accuracy, we assume $f_v - f_c \approx 1$ for the energy window of current-carrying electrons. This relation is exact at 0 K, and remains an excellent approximation even at room temperature. The tunneling current *density* is then given by

$$\begin{aligned} J_T^{3\text{-D}} &= \frac{I_T^{3\text{-D}}}{L_xL_y} \\ &= q\frac{g_s g_v \hbar}{(2\pi)^3 m_v^*}T_0 \times \int_{\phi=0}^{2\pi} d\phi \int_{\theta=0}^{\frac{\pi}{2}} d\theta \sin\theta\cos\theta \\ &\quad \times \int_{k=0}^{\frac{k_{\max}}{\sqrt{1+\sin^2\theta}}} dk\cdot k^3 \exp\left[-\frac{\hbar^2k^2}{2m_v^*\overline{E}}\sin^2\theta\right] \end{aligned} \tag{7}$$

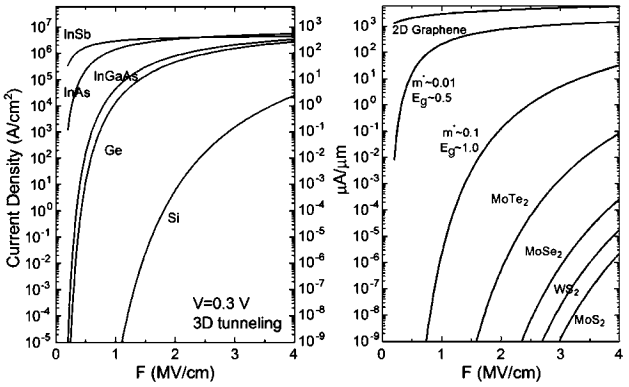

Fig. 5. *Calculated interband tunneling current densities in a few 3-D and 2-D semiconductor crystal $p-n$ junctions. The left figure shows the calculated tunneling current densities in reverse-biased $p-n$ homojunctions. If the current per unit area is assumed constant for a layer thickness of 10 nm, then the effective current per unit width is shown in the right axis of the left plot. This estimation neglects quantization. The right figure shows the calculated tunneling current per unit widths of some 2-D crystals. The transition metal dichalcogenides have low current densities due to high bandgaps, whereas 2-D graphene has the highest current density. Two-dimensional tunneling currents for two small bandgap and effective masses are also shown.*

where the k-space integral is evaluated over the restricted volume Ω_T. The units are in current per unit area (A/cm^2), as it should be. The integral yields an analytical result. Using the symmetric band approximation $m_c^* \approx m_v^* = 2m_R^*$, we get

$$J_T^{3\text{-D}} = \frac{q^2 g_s g_v\sqrt{2m_R^*}F}{8\pi^2\hbar^2\sqrt{E_g}}T_0\left[qV - 2\overline{E}\left\{1-\exp\left(-\frac{qV}{2\overline{E}}\right)\right\}\right] \tag{8}$$

where the symbols have been defined earlier. For extremely small reverse bias voltages $qV \ll 2\overline{E}$, the tunneling current varies as $J_T^{3\text{-D}} \sim V^2$ to leading order. For larger voltages when $qV \gg 2\overline{E}$, $J_T^{3\text{-D}} \sim V$ and this is the condition used in most TFETs. The expression for the tunneling current shows the dependences on various band structure and junction parameters explicitly.

The calculated interband tunneling current densities for 3-D semiconductors are shown in Fig. 5(left) for a reverse bias voltage of 0.3 V. As is evident, the smaller bandgaps of InSb and InAs favor high tunneling current densities that approach $\sim 10^6$ A/cm^2. If we assume that the body thickness of the $p-i-n$ junction is 10 nm, the effective current per unit width is also shown in the right axis of Fig. 5(left). However, this value of the current does not account for the increase in the bandgap due to quantization, which we address shortly. We now apply the same technique for calculating tunneling currents in 2-D crystal semiconductors.

Two-dimensional semiconductors: The same recipe is repeated for 2-D crystals. If the transport is along the x-direction, the transverse momentum component consists of one component k_y, and the restricted k-space volume is given by $2k_y^2 + k_x^2 \le k_{\max}^2$. The interband tunneling current *per unit width* in a 2-D crystal $p-i-n$ junction then evaluates to

$$J_T^{2\text{-D}} = \frac{qg_s g_v\sqrt{2m_R^*\overline{E}}}{2\pi^2\hbar^2}T_0 \times \left[(qV-\overline{E})\sqrt{\pi}\,\mathrm{Erf}\left[\sqrt{\frac{qV}{2\overline{E}}}\right] + \sqrt{qV\cdot 2\overline{E}}\exp\left[-\frac{qV}{2\overline{E}}\right]\right] \quad (9)$$

where $\mathrm{Erf}[\ldots]$ stands for the error function, and $\overline{E} = q\hbar F/2\sqrt{2m_R^* E_g}$ as before. For extremely small reverse bias voltages $qV \ll 2\overline{E}$, the tunneling current varies as $J_T^{2\text{-D}} \sim V^{3/2}$ to leading order. For larger voltages when $qV \gg 2\overline{E}$, $\mathrm{Erf}[\ldots] \to 1$, and we get a linear dependence of the tunneling current on the reverse-bias voltage $J_T^{2\text{-D}} \approx (q^2 g_s g_v\sqrt{2\pi m_R^*\overline{E}}/2\pi^2\hbar^2)T_0 V$. We note that the units are in current per unit width (mA/μm), as should be the case for 2-D crystals. In quasi-2-D systems, multiple subbands may be involved in transport. Then, we sum the current from each subband with the respective band parameters.

For the special case of 2-D graphene, the band structure is conical, and the bandgap is zero. The interband tunneling probability for a graphene in-plane $p-n$ junction is given by $T(E,\theta) = \exp[-\pi E^2\sin^2\theta/q\hbar v_F F]$, where θ is the angle between the incident electron momentum and the junction electric field F, and E is the electron energy [70]. The requirement of lateral momentum conservation effectively opens a bandgap proportional to the lateral momentum of electrons. The doping in the p- and n-graphene regions are such that the Fermi level to Dirac point energies are E_{Fp} and E_{Fn}, respectively, and the junction "depletion width" is L_{pn}. The reverse-bias tunneling current in the 2-D graphene $p-n$ junction is then given by [71]

$$J_T^{Gr} = \frac{q^2 V}{\pi^2\hbar}\sqrt{\frac{E_{Fp}+E_{Fn}-qV}{\hbar v_F L_{pn}}}. \quad (10)$$

Let us assume that the applied reverse bias voltage is small compared to the degeneracy energies, and approximate the junction field by $qF \sim (E_{Fp}+E_{Fn})/L_{pn}$. Then, we obtain an approximate expression for the interband reverse-bias tunneling current per unit width in 2-D graphene $p-n$ junctions to be $J_T^{Gr} \sim (q^2\sqrt{qF}/\pi^2\hbar\sqrt{\hbar v_F})V$.

The interband tunneling current densities of various 2-D crystals are plotted in Fig. 5(right). The material constants (bandgaps and effective masses) are obtained from [39]. The values of tunneling currents for transition-metal dichalcogenides are low owing to their large bandgaps. For example, the current density approaches $\sim$0.1 μA/μm for $MoTe_2$ at a high field of 4 MV/cm. The tunneling current density of 2-D graphene is the highest ($\sim$several mA/μm), but it lacks a bandgap. As new 2-D crystals come to the fore, it is desirable to have smaller bandgaps for boosting the current, as indicated by the two curves corresponding to hypothetical 2-D crystals with bandgaps of 0.5 and 1.0 eV, respectively. Such small-bandgap materials could be intrinsic 2-D crystals, or derived from interaction-induced bandgap of Dirac-cone surface states in thin topological insulator materials [29]. Another possibility is in bilayer graphene, where breaking the layer symmetry by vertical electric fields opens a small bandgap [72]–[74]. It is clear that at this stage the currently available TMD family of 2-D crystal semiconductors can enable tunneling transistors. But for in-plane tunneling geometries, the current densities will be low. This feature can be effectively addressed by either narrower gap 2-D crystal semiconductors, or by interlayer tunneling device geometries. We address interlayer tunneling devices in Section V, after discussing the treatment of tunneling in 1-D semiconductors.

One-dimensional semiconductors: For 1-D tunneling, we obtain an exact analytical result even when we include the Fermi–Dirac occupation factors in the source and the grain sides of the $p-i-n$ junction. In the ideal 1-D case, $E_\perp = 0$ since electrons cannot have transverse momentum. When a voltage V is applied, $f_v = 1/(1+\exp[(E-qV)/kT])$ and $f_c = 1/(1+\exp[E/kT])$ are the occupation functions of the source and drain sides. The interband tunneling current is evaluated by the same prescription followed for the 3-D and 2-D cases to be [75]

$$I_T^{1\text{-D}} = \frac{q^2}{h}g_s g_v T_0 \times \frac{kT}{q}\ln\left[\frac{1}{2}\left\{1+\cosh\left(\frac{qV}{kT}\right)\right\}\right]. \quad (11)$$

Note the explicit appearance of the Landauer conductance in the expression. This expression for tunneling current holds for quasi-1-D semiconductors such as semiconducting nanowires, carbon nanotubes, or semiconducting graphene nanoribbons (GNRs). The appropriate WKB tunneling probability should be used. For nanowires made from conventional 3-D semiconductor crystals, the probability is $T_0 = \exp[-4\sqrt{2m_R^*}E_g^{3/2}/3q\hbar F]$ as before. For CNTs and GNRs, the unconventional band structure is captured in a modified WKB tunneling probability, which is given by $T_0 = \exp[-\pi E_g^2/4q\hbar v_F F]$, where v_F is the Fermi velocity [75]. If there are multiple subbands involved in the transport, we add the currents from each subband with the right bandgap.

Fig. 6 shows the effect of quantization on bandgaps of 3-D crystals on the left, and the calculated 1-D

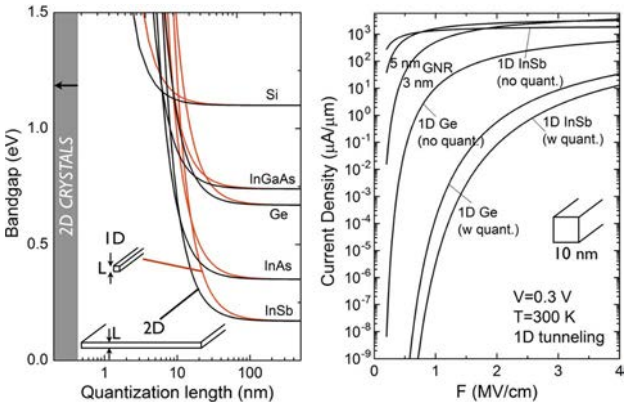

Fig. 6. *The effect of quantization on the bandgap of some 3-D crystals. The plot is generated assuming a particle-in-a-box quantization, and is meant to illustrate the approximate trends. The effect of quantization is the most severe for narrow bandgap semicondctors. The increase in bandgap will reduce interband tunneling currents. The right figure shows the 1-D tunneling currents for GNRs, and InSb and Ge. Note the large reduction of current due to quantization effects in Ge and especially in InSb. A major advantage of 2-D crystals is their inherently thin nature. In addition, their large effective masses make them robust to quantization effects when rendered 1-D.*

semiconductor tunneling current densities on the right. The effect of quantization is to increase the bandgap, in turn reducing the interband tunneling current. The right figure shows the current densities of "1-D" semiconductors such as graphene nanoribbons (GNRs) and Ge and InSb nanowires. The tunneling current densities of GNRs are the highest of all materials calculated that possess bandgaps. The effect of quantization on Ge and InSb nanowire 1-D $p-n$ junction structures is evident from the precipitous drop in the interband tunneling currents in them.

The increase in the bandgap for both 2-D and 1-D confinement is calculated using a simple particle-in-a-box model with the band-edge effective masses of the 3-D semiconductors. The values are meant to be representative of the trends; more accurate electronic structure calculations should be used for direct validation. However, it is clear that as 3-D crystals are scaled in thickness (for making them 2-D) or in diameter (for making them 1-D), the corresponding increase in bandgap is rapid. Large bandgap semiconductors are more robust to quantization since they possess heavier effective masses. This is a dilemma for the scaling of tunneling transistors. As shown in the shaded region in the left of Fig. 6, 2-D crystals are typically of ~nanometer thicknesses and span bandgaps from 0 eV (graphene) to several eVs (BN). This regime remains inaccessible to 3-D crystal semiconductors due to quantization. It is possible to access this regime with 3-D semiconductors only if the band structure allows for extreme anisotropies [76], but such highly desirable properties are yet to be demonstrated in 3-D crystal semiconductors.

IV. TUNNELING TRANSISTORS WITH 3-D CRYSTALS

The unified view of tunneling transport discussed in the last section provides a framework for comparative studies of the effect of dimensionality on tunneling transistors. Based on the discussion of transport in two-terminal tunnel junctions, we now discuss the electrostatics and device embodiments of the corresponding three-terminal TFETs.

In a TFET, a gate terminal electrostatically controls the energy-band alignment of the $p-n$ junction, as indicated in Fig. 7. In the OFF-state of the device, electrons in the valence band of the source are energetically forbidden to tunnel to the drain since the channel length exponentially damps the direct source-to-drain tunneling probability. To turn the device on, the gate pushes the channel bands to align the conduction band edge of the channel region with the valence band of the source. Electrons can now tunnel through the tunneling barrier, which is much smaller than the OFF-state. The goal therefore is to allow a large current to flow in the ON-state, while cutting the current off as much as possible in the OFF-state.

The performance requirements of a TFET are indicated schematically in Fig. 7. Compared to a MOSFET, the steeper SS slope of a TFET enables a higher ON-current at a smaller gate overdrive voltage. This feature is expected to enable scaling of the voltage supply V_{DD} to lower values while maintaining a substantial ON/OFF ratio. The issues of electrostatics and transport have been discussed at length in various articles [12], [69]. We refer the reader to these articles for detailed historical perspectives and further technical details. Here, we qualitatively discuss a few embodiments and issues with TFETs realized with 3-D crystal semiconductors. The discussion naturally motivates the case for 2-D crystal realizations of the device.

The electric field lines emanating from the gate metal of a TFET need to access the $p-n$ junction. Therein lies a dilemma for TFETs based on 3-D crystal semiconductors. As shown in Fig. 8, if the tunneling current flows in the lateral direction and the gate field is vertical, the channel needs to be thinned down to exercise substantial electrostatic control over the entire junction thickness. As the

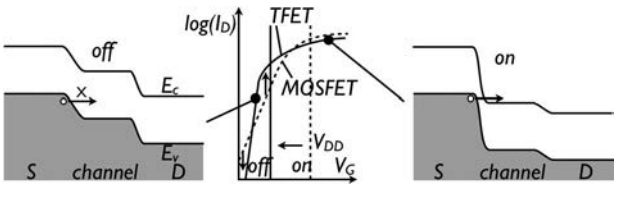

Fig. 7. *TFET operation and requirements. The left figure shows the OFF-state energy-band diagram of the TFET along the tunneling direction. The right figure shows the ON-state. The channel band is controlled by the gate. TFETs are expected to lower the supply voltage V_{DD} since a steeper SS swing leads to a higher ON-current at a smaller voltage, as shown in the middle.*

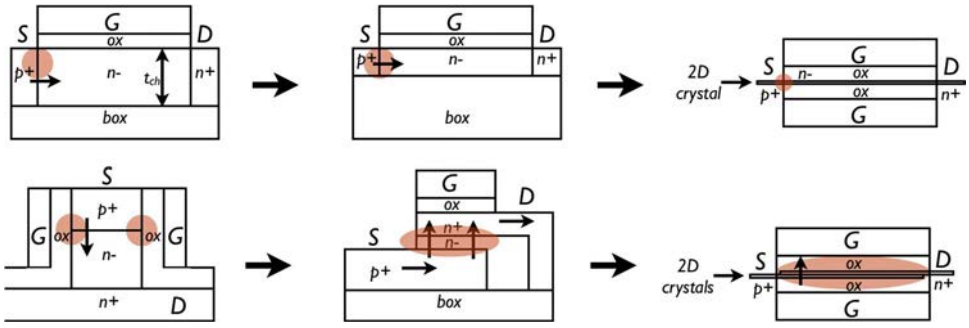

Fig. 8. *Schematic representation of various topologies of TFETs. The top row shows TFETs where the tunneling current flows laterally in the $p^+ - n^- - n^+$ junction. The circles are indications of the region in space where most of the interband tunneling current flows. Since the gate is on the top, parts of the junction farther away from it are not effectively gated in the top left TFET. The top middle geometry is the same as the left, but with a thinner channel for more uniform electrostatic gate control of tunneling current. The right figure on the top row is the 2-D crystal realization of the lateral TFET. As the channel thickness is reduced in 3-D semiconductors, quantum confinement increases the bandgap and reduces the tunneling current. This is avoided in 2-D crystals. To increase the net current, vertical TFETs are being considered. The bottom row indicates some realizations of TFETs in which the tunneling current flows vertically. The left figure shows a side-gate geometry, and the middle figure is a geometry in which the current flow is not over a "line," but an "area," as shown by the shaded ellipse. The right figure shows the realization of a vertical double-gate TFET with p^+ and n^+ 2-D crystal layers. It highlights the electrostatic advantage and simplicity.*

channel thickness is scaled down, quantum confinement increases the bandgap, and thus the interband tunneling current reduces (see Fig. 6). A 2-D crystal does not suffer from such a problem, and thus offers a way to fight quantization effects. In addition, it offers a solution to surface state related trap states, and simpler integration of double-gate geometries, as indicated in Fig. 8.

A number of TFETs with subthreshold slopes less than the SS limit of 60 mV/decade have been demonstrated, proving the feasibility of the concept. Such devices have been made with 3-D crystal semiconductors (Si, Ge, etc.) as well as with carbon nanotubes [77]–[80]. However, for most realizations, the ON-state current falls below the $\sim$1 mA/μm range necessary for high-performance operation. Low ON-current TFETs can enable various new applications where performance (speed) requirements are not as critical as the requirement of low power consumption. For high-performance TFETs, various approaches are being pursued to increase the ON-current. These approaches involve using heterojunctions that have staggered or broken-gap band alignments, or through changes in the device topology. An approach based on the device topology is indicated in Fig. 8.

The shaded regions in Fig. 8 indicate the location of current flow. To increase the tunneling current per unit width, it is necessary to increase the net *area* of tunneling current flow. The vertical geometries shown in Fig. 8 allow this change [81], [82]. The gate field effect is in the *same* direction as the tunneling current flow in such devices. The tunneling current follows a nonlinear path (shaped like an "S") laterally from the source, vertically into the drain, and then out laterally into the drain. The device geometry requires careful processing. For this geometry, two layers of 2-D crystals, one doped *p*-type and the other *n*-type, promise efficient vertical scaling and electrostatic control as shown in the figure. It may also enable a simplification of the processing requirements.

V. TUNNELING TRANSISTORS WITH 2-D CRYSTALS

The 2-D crystal realizations of TFETs discussed here involve *in-plane* tunneling for the lateral device and *interlayer* tunneling in the vertical TFET. We discuss them in greater detail here. Note that due to the relatively early phase of material development, we estimate and project the performance advantages in cases where experimental results are not available yet.

A. In-Plane Tunneling: 2-D Crystal Semiconductors

The in-plane interband tunneling currents calculated in Fig. 5 show that smaller bandgap semiconductor 2-D crystals are required for boosting the ON-state current of the devices. Low-power TFETs are realizable with the transition-metal dichalcogenide semiconductors. The effective masses of the conduction and valence band edges of TMD 2-D crystals have been calculated to be rather symmetric. For example, the electron effective mass of MoS_2 is $\sim$0.57, and the hole effective mass is $\sim$0.66 [39]. The symmetry in the band structure is expected to lead to symmetric performance of nTFETs and pTFETs, which would be essential for complementary logic circuits.

It has been found that multilayer versions of TMD 2-D crystals have smaller bandgaps than the single-layer counterpart, and are generally of indirect bandgap nature [40], [41]. This is also true when one considers single-layer graphene (direct bandgap) and graphite (which is a semimetal). Furthermore, it has recently been reported that

carrier inversion can be achieved in multilayer TMD crystals by the field effect. A hole channel was observed in a nominally *n*-type layered semiconductor [64]. Consider a few-layer stack of 2-D TMD crystals. By using two gates, it is possible to create an electron channel at one interface and a hole channel in the other. These channels can be placed several nanometers apart by controlling the number of layers. The wave function overlap between these states is small at no bias owing to the high effective mass for carrier motion between planes. The geometry then allows for a TFET similar to the vertical structure shown in Fig. 8, but without the need to chemically dope the individual layers. A major challenge in such structures is in the formation of ohmic contacts to the individual layers. Note that such a device has also been recently proposed for thin layer Si [83]. The realization with multilayer version of 2-D crystals can be an alternative approach that can leverage the robustness against quantization effects, and relative insensitivity to surface and interface trap effects.

B. In-Plane Tunneling: 2-D Graphene

As shown in Fig. 5, the ON-state interband tunneling current density in 2-D graphene is the highest due to the absence of a bandgap. For the same reason, it is difficult to obtain the OFF-state condition using monolayer 2-D graphene. Field-tunable bandgaps in bilayer graphene have been proposed as a possible approach to achieving ON/OFF ratios in TFETs [84]. There have also been recent reports of the observation of negative differential resistance in monolayer 2-D graphene FETs [85]. The proposed mechanism responsible for such behavior relies entirely on gate electrostatics and the unique band structure with the zero-gap nature of 2-D graphene. More experimental work and understanding of NDR mechanisms in 2-D graphene can lead to useful device applications in the analog arena to complement TFETs. To decrease the OFF-state current for in-plane tunneling devices, it is necessary to create bandgaps in graphene. One approach is to use CNTs or lithographically patterned GNRs, which is discussed next.

C. In-Plane Tunneling: CNTs and GNRs

One of the early reports of sub-60-mV/decade SS slope TFET behavior was observed in semiconducting carbon nanotubes at room temperature [80]. Analysis of the device performance for CNT TFETs [86] and GNR TFETs [87] shows that they are attractive for desirable ON-currents, ON/OFF ratios, and sub-60-mV/decade SS slopes. CNTs do not have edge states, and are the most attractive from a performance viewpoint. Bandgap control, chemical doping, and patterned assembly on large wafers still remain challenging for CNTs, though rapid progress is being made [88].

Their close cousins, GNRs are also highly attractive candidates for TFETs. For example, Fig. 9 shows the device structure, energy band diagrams, and the projected device characteristics of complementary GNR TFETs. The inclusion of parasitic elements to the intrinsic model still maintains a high performance. GNRs can be integrated on planar surfaces, and can be made lithographically in

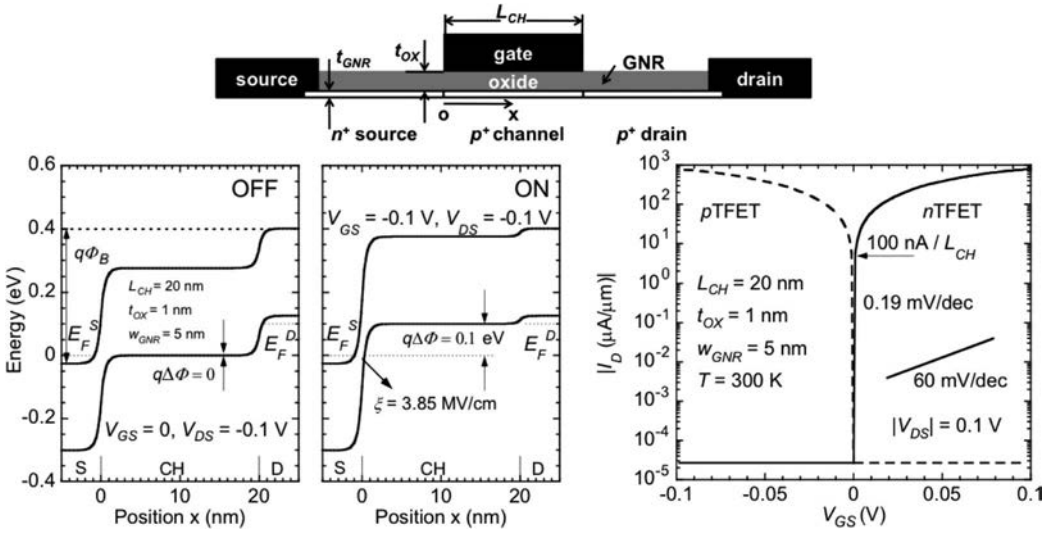

Fig. 9. *A proposed GNR TFET geometry, energy band diagram, and the calculated transistor transfer curves. The device structure consists of a GNR p – n junction that is gated through an insulator from the top gate. The energy band diagrams are for a 20-nm-long channel device with a 5-nm-wide GNR. The energy band diagrams indicate the OFF- and ON-states of the device, where the channel potential is moved with the gate voltage. The resulting transfer curve shows a high ON-current, a low OFF-current, and a low SS slope, below the 60-mV/decade limit. Though the calculations are for an ideal case, they represent the attractiveness of GNRs as possible candidates for TFETs. The figure has been adapted from [87].*

parallel arrays to boost the net current in a realistic TFET device geometry. The available dangling bonds at the edges can be used to chemically dope them; initial reports indicate this possibility [89]. The major challenges at this stage for the realization of GNR TFETs lie in the narrowness of the GNR widths necessary to avail high-performance levels. The energy bandgap of a semiconducting GNR of width W is $E_g \sim 1.4/W$ eV, where W is in nanometers. Based on theoretical estimates, GNRs of widths ≤ 10 nm are necessary. The line-edge roughness that might result from process variations for the thinnest GNRs can degrade the performance of GNR TFETs, as has been analyzed in [90]. On the other hand, advances in process control in the fabrication of thin films in Si FinFETs can be effectively leveraged for fabrication of wafer-scale GNRs. A number of variants of the GNR TFETs have also been proposed to improve the device performance [91]–[95].

The symmetry of the band structure of CNTs and GNRs is a major advantage that allows for the realization of nTFETs and pTFETs on equal footing. Combined with the scaling advantages that stem from their atomically thin body nature, they are highly desirable for nanoscale TFETs. The approach to high-performance TFETs using 3-D crystal semiconductors is taking the path toward materials with successively smaller bandgaps to increase the ON-current. The approach with graphene, CNTs, and GNRs is from the other extreme, where we start from zero bandgap and very high ON-currents, and now need to open bandgaps controllably to lower the OFF-current. While this is an attractive and complementary approach, 2-D crystals also offer the possibility of *interlayer* tunneling transistors, which we discuss now.

D. Interlayer Tunneling Devices, BiSFETs, and SymFETs

Electron tunneling out of the plane of a 2-D crystal is under intense scrutiny at this time [96]. The electronic band structure of the 2-D crystal is defined in the plane but not out of it. The conventional approach to tunneling calculations requires the knowledge of band parameters such as the effective mass of the evanescent band structure in the direction of the tunneling. Since this feature is not well defined for 2-D crystals, it is more feasible to use scattering rate formalisms for quantitative calculations of interlayer tunneling. The Bardeen transfer-Hamiltonian approach, used in scanning tunneling microscopy [97], [98] and in superconducting Josephson junctions [99] allows such evaluation. We do not derive the quantitative results here, but refer the reader to recent articles that approach the subject of interlayer tunneling using the Bardeen method.

A prototype interlayer-tunneling device is a graphene–insulator–graphene (GIG) junction. In a recent work [100], the interlayer tunneling current in such a GIG junction was explicitly evaluated using the Bardeen method. The predicted I–V characteristics are rather remarkable, and highlight the strong role of the symmetry of the band structure of graphene.

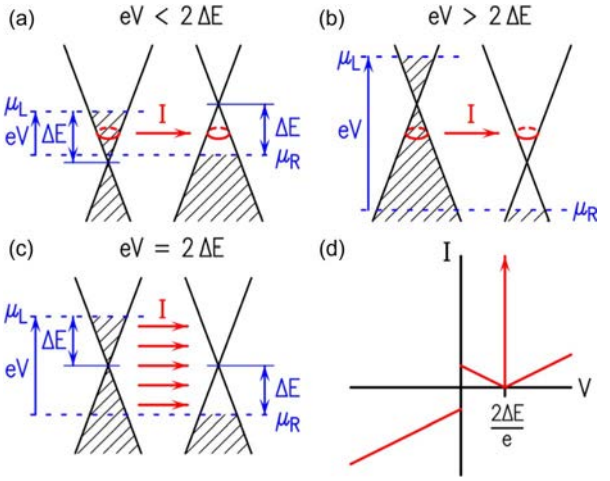

Fig. 10. *Band alignments of GIG interlayer tunnel junctions under various bias conditions from [100]. The graphene layers are doped to form a $p-n$ junction. In (a) and (b), the symmetry of the band structure restricts electrons at only one energy to carry interlayer current due to the requirement of transverse momentum conservation. A special case occurs when the Dirac points align: electrons at all energies are now allowed to tunnel, leading to a spike in the current, as shown schematically in (d).*

Fig. 10 shows the energy band alignments and projected device performance of a GIG interlayer tunnel junction device. The two graphene layers are "independent" in the sense that they do not form a bilayer, and they are doped p- and n-type as captured by their Fermi level degeneracies. Ohmic contacts are made to the two layers independently. A voltage is applied across the junction. When the Dirac points of the two layers are misaligned, a small interlayer tunneling current flows. The circles indicated on the Dirac cones in Fig. 10(a) and (b) show the states that participate in the interlayer tunneling process. Electrons that have energy halfway between the Dirac points carry the current. This is because transverse momentum conservation requires the radii of the iso-energy circles to be the same in both layers.

However, at the particular voltage when the Dirac points align, as shown in Fig. 10(c), electrons at *all* energies are now allowed to tunnel, leading to a large spike in the current. This is schematically shown in Fig. 10(d) as a Dirac-delta function. A quantitative evaluation leads to broadening, but with a very large NDR effect. Note that the peak would be much smaller if the band structure was not symmetric. Since then the requirement of transverse momentum conservation would restrict the current to flow at a particular energy, and a collective tunneling condition as in Fig. 10(c) cannot be achieved. The large tunneling current peak is a direct consequence of the symmetric band structure of 2-D graphene.

The GIG $p-n$ junction structure can be connected to gates to realize an interlayer-tunneling transistor. Such a device, called the symmetric-FET (SymFET) has been recently proposed [55]. In addition to performing logic operations, the inherently fast tunneling feature and large NDR promises to also enable analog applications such as high-harmonic generation, and high-speed oscillator design. Note that the SymFET device structure is similar to gated RTD structures [101] realized in 3-D semiconductor heterostructures, but takes advantage of the band structure symmetry of graphene to deliver a stronger NDR behavior. The first experimental report of such a structure did not show NDR, but exhibited TFET-like behavior with a few orders ON/OFF ratio at room temperature. The structure used consisted of graphene–BN–graphene and graphene–MoS_2–graphene heterostructures [53].

The SymFET structure is based on single-particle tunneling. Realistic fabrication of the device calls for rotational alignment of the graphene layers. By adjusting the interlayer distance and the carrier densities, the Coulombic forces between the electrons and the holes in the two graphene layers can be made strong enough to form excitonic quasi-particles. Under suitable bias conditions, the interlayer current flow can take a collective many-body form triggered by a Bose–Einstein condensation of the excitons. The condensate can boost the interlayer current significantly. The proposed device, called the bilayer pseudospin FET (BiSFET) is insensitive to the rotational alignment of the two graphene layers. It has been shown that if the BISFET can be realized, it can perform digital logic by consuming many orders of magnitude lower energy than conventional MOSFETs [54]. The SymFET and the BiSFET are fundamentally new types of devices with no direct analogs to conventional semiconductors. This is because of their unique band structures and their 2-D crystal nature. Their discussion is an ideal point to end this review paper and to wrap up with a few concluding remarks.

VI. FUTURE PERSPECTIVES AND CONCLUSION

The emergence of 2-D crystal materials has marked a new phase for the development of semiconductor devices. It may rank at the same level as the origin and proliferation of heterostructures in 3-D semiconductors. The materials and the resulting devices are at their infancy, as are many device ideas based on tunneling that are at proposal stages. But the novelty the family of 2-D crystal has brought to the field becomes evident by the string of new device concepts based on tunneling. The addition of graphene with its unique band structure, BN as a 2-D crystal insulator, and transition-metal dichalcogenides with material properties ranging from semiconducting to metallic and superconducting casts a much wider net than has been possible with conventional materials. The possibility of integration of diverse material properties in 2-D crystal heterostructures has breathed new life into existing paradigms of electronic device technologies. This is an exciting time when creative ideas are needed to exploit the power of this new material system. Though it is impossible to predict the exact path forward, we can be sure that electronic devices that go far beyond the current state of the art will result from the new material family. ■

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REFERENCES

[1] M. Riordan and L. Hoddeson, *Crystal Fire*. New York, NY, USA: Norton, 1998, pp. 88–90.

[2] S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices*, 3rd ed. New York, NY, USA: Wiley-Interscience, 2006.

[3] J. S. Kilby, "Turning potential into realities: The invention of the integrated circuit," *Nobel Lecture*, 2000.

[4] Z. I. Alferov, "Nobel lecture: The double heterostructure concept and its applications in physics, electronics, and technology," *Rev. Mod. Phys.*, vol. 73, pp. 767–782, Oct. 2001.

[5] H. Kroemer, "Nobel lecture: Quasielectric fields and band offsets: Teaching electrons new tricks," *Rev. Mod. Phys.*, vol. 73, pp. 783–793, Oct. 2001.

[6] D. H. Kim, B. Brar, and J. A. del Alamo, "$f_T = 688$ GHz and $f_{max} = 800$ GHz in $L_g = 40$ nm $In_{0.7}Ga_{0.3}As$ MHEMTs with $g_m(max) > 2.7$ mS/μm," in *IEEE Int. Electron Devices Meeting Tech. Dig.*, 2011, pp. 319–322.

[7] S. Pimputkar, J. S. Speck, S. P. DenBaars, and S. Nakamura, "Prospects for LED lighting," *Nature Photon.*, vol. 3, pp. 180–182, 2009.

[8] J. D. Joannopoulus, S. G. Johnson, and J. N. Winn, *Photonic Crystals: Molding the Flow of Light*, 2nd ed. Princeton, NJ, USA: Princeton Univ. Press, 2008.

[9] W. Cai and V. Shalaev, *Optical Metamaterials: Fundamentals and Applications*, 1st ed. New York, NY, USA: Springer-Verlag, 2009.

[10] S. Christopoulos, G. Baldassarri Hoger von Hogersthal, A. J. D. Grundy, P. G. Lagoudakis, A. V. Kavokin, J. J. Baumberg, G. Christman, R. Butte, E. Feltin, J.-F. Carlin, and N. Grandjean, "Room-temperature polariton lasing in semiconductor microcavities," *Phys. Rev. Lett.*, vol. 98, pp. 126405-1–126405-4, Mar. 2007.

[11] T. N. Theis and P. M. Solomon, "It's time to reinvent the transistor!" *Science*, vol. 327, pp. 1600–1601, Mar. 2010.

[12] A. M. Ionescu and H. Riel, "Tunnel field-effect transistors as energy-efficient electronic switches," *Nature*, vol. 479, pp. 329–337, Nov. 2011.

[13] T. N. Theis and P. M. Solomon, "In quest of the "next switch": Prospects for greatly reduced power dissipation in a successor to the silicon field-effect transistor," *Proc. IEEE*, vol. 98, no. 12, pp. 2005–2014, Dec. 2010.

[14] T.-J. King, D. Markovic, V. Stojanovic, and E. Elon, "MEMS switches for low-power logic," *IEEE Spectrum*, pp. 38–43, Apr. 2012.

[15] K. Gopalakrishnan, P. B. Griffin, and J. D. Plummer, "I-MOS: A novel semiconductor device with a subthreshold slope lower than kT/q," in *IEEE Int. Electron Devices Meeting Tech. Dig.*, 2002, pp. 289–292.

[16] M. T. Bjork, O. Hayden, H. Schmid, H. Riel, and W. Reiss, "Vertical surround-gated silicon nanowire impact ionization field-effect transistors," *Appl. Phys. Lett.*, pp. 142 110–142 292, 2007.

[17] S. Salahuddin and S. Datta, "Use of negative capacitance to provide voltage amplification for low power nanoscale devices," *Nano. Lett.*, vol. 8, pp. 405–410, 2008.

[18] D. Newns, B. Elmegreen, X. H. Liu, and G. Martyna, "A low-voltage high-speed electronic switch based on piezoelectric

transduction," *J. Appl. Phys.*, vol. 111, pp. 084509-1–084509-18, 2012.

[19] K. S. Novoselov, A. K. Geim, S. V. Morozov, D. Jiang, Y. Zhang, S. V. Dubonos, I. V. Grigorieva, and A. A. Firsov, "Electric field effect in atomically thin carbon films," *Science*, vol. 306, pp. 666–669, 2004.

[20] Y. Zhang, Y. W. Tan, H. Stormer, and P. Kim, "Experimental observation of the quantum Hall effect and Berry's phase in graphene," *Nature*, vol. 438, pp. 201–204, 2005.

[21] C. Berger, Z. Song, X. Li, X. Wu, N. Brown, C. Naud, D. Mayou, T. Li, J. Hass, A. N. Marchenkov, E. H. Conrad, P. N. First, and W. A. de Heer, "Electronic confinement and coherence length in patterned epitaxial graphene," *Science*, vol. 312, pp. 1191–1196, 2006.

[22] K. S. Novoselov, D. Jiang, F. Schedin, T. J. Booth, V. V. Khotkevich, S. V. Morozov, and A. K. Geim, "Two-dimensional atomic crystals," *Proc. Nat. Acad. Sci.*, vol. 102, pp. 10451–10453, 2005.

[23] D. J. Frank, R. H. Dennard, E. Nowak, P. M. Solomon, Y. Taur, and H.-S. P. Wong, "Device scaling limits of Si MOSFETs and their application dependencies," *Proc. IEEE*, vol. 89, no. 3, pp. 259–288, Mar. 2001.

[24] A. I. Yanson, G. R. Bollinger, H. E. van den Brom, N. Agrait, and J. M. van Ruitenbeek, "Formation and manipulation of a metallic wire of single gold atoms," *Nature*, vol. 395, pp. 783–785, 1998.

[25] R. H. Friend and A. D. Yoffe, "Electronic properties of intercalation complexes of the transition metal dichalcogenides," *Adv. Phys.*, vol. 36, pp. 1–94, 1987.

[26] P. Vogt, P. D. Padova, C. Quaresima, J. Avila, E. Frantzeskakis, M. C. Asensio, A. Resta, B. Ealet, and G. Le Lay, "Silicene: Compelling experimental evidence for graphene-like two-dimensional silicon," *Phys. Rev. Lett.*, vol. 108, pp. 1055501-1–1055501-5, 2012.

[27] Z. Ni, Q. Liu, K. Tang, J. Zheng, J. Rhou, R. Qin, Z. Gao, D. Yu, and J. Lu, "Tunable bandgap in silicene and germanene," *Nano Lett.*, vol. 12, pp. 113–118, 2012.

[28] C. L. Freeman, F. Claeyssens, N. L. Allan, and J. H. Harding, "Graphitic nanofilms as precursors to Wurtzite films: Theory," *Phys. Rev. Lett.*, vol. 96, pp. 066102-1–066102-4, 2006.

[29] J. Chang, L. F. Register, and S. K. Banerjee, "Possible applications of topological insulator thin films for tunnel FETs," in *IEEE Device Res. Conf. Tech. Dig.*, 2012, pp. 31–32.

[30] H. W. Kroto, J. R. Heath, S. C. O'Brien, R. F. Curl, and R. E. Smalley, "C_{60}: Buckminsterfullerene," *Nature*, vol. 318, pp. 162–163, 1985.

[31] M. Atiyah and P. Sutcliffe, "Polyhedra in physics, chemistry and geometry," *Milan J. Math.*, vol. 71, pp. 33–58, 2003.

[32] R. Wang, Q. Zhang, W. Li, I. Calizo, T. Shen, C. A. Richter, A. R. Hight-Walker, X. Liang, A. Seabaugh, D. Jena, H. G. Xing, D. J. Gundalch, and N. V. Nguyen, "Determination of graphene work function and graphene-insulator-semiconductor band alignment by internal photoemission spectroscopy," *Appl. Phys. Lett.*, vol. 101, pp. 022105-1–022105-4, 2012.

[33] W. Monch, "Valence-band offsets and Schottky barrier heights of layered semiconductors explained by interface-induced gap states," *Appl. Phys. Lett.*, vol. 72, pp. 1899–1901, 1998.

[34] R. Schlaf, O. Lang, C. Pettenkofer, and W. Jaegermann, "Band lineup of layered semiconductor heterointerfaces prepared by van der Waals epitaxy: Charge transfer correction term for the electron affinity rule," *J. Appl. Phys.*, vol. 85, pp. 2732–2753, 1999.

[35] T. Fang, A. Konar, H. Xing, and D. Jena, "Carrier statistics and quantum capacitance in graphene sheets and ribbons," *Appl. Phys. Lett.*, vol. 91, pp. 092109-1–092109-3, 2007.

[36] K. Watanabe, T. Taniguchi, and H. Kanda, "Direct-bandgap properties and evidence for ultraviolet lasing of hexagonal boron nitride single crystal," *Nature Mater.*, vol. 3, pp. 404–409, 2004.

[37] K. Wood and J. B. Pendry, "Layer method for band structure of layer compounds," *Phys. Rev. Lett.*, vol. 31, pp. 1400–1403, 1973.

[38] K. Kaasbjerg, K. S. Thygesen, and K. W. Jacobsen, "Phonon-limited mobility in n-type single-layer MoS_2 from first principles," *Phys. Rev. B*, vol. 85, pp. 115317-1–115317-16, 2012.

[39] L. Liu, S. B. Kumar, and J. Guo, "Performance limits of monolayer transition metal dichalcogenide transistors," *IEEE Trans. Electron Devices*, vol. 58, no. 9, pp. 3042–3047, Sep. 2011.

[40] K. F. Mak, C. Lee, J. Hone, J. Shan, and T. F. Heinz, "Atomically thin MoS_2: A new direct-gap semiconductor," *Phys. Rev. Lett.*, vol. 105, pp. 136805-1–136805-4, 2010.

[41] A. Splendiani, L. Sun, Y. Zhang, T. Li, J. Kim, C.-Y. Chim, G. Galli, and F. Wang, "Emerging photoluminescence in monolayer MoS_2," *Nano Lett.*, vol. 10, pp. 1271–1275, 2010.

[42] D. Hisamoto, W. C. Lee, J. Kedzierski, H. Takeuchi, K. Asano, C. Kuo, E. Anderson, T. J. King, J. Bokor, and C. Hu, "FinFET-A self-aligned double-gate MOSFET scalable to 20 nm," *IEEE Trans. Electron Devices*, vol. 47, no. 12, pp. 2320–2325, Dec. 2000.

[43] G. Tsutsui, M. Saitoh, and T. Hiramoto, "Experimental study on superior mobility in [110]-oriented UTB SOI pMOSFETs," *IEEE Electron Device Lett.*, vol. 26, no. 11, pp. 836–838, Nov. 2005.

[44] R. S. Muller, T. I. Kamins, and M. Chan, *Device Electronics for Integrated Circuits*, 3rd ed. New York, NY, USA: Wiley, 2003, pp. 485–487.

[45] H. Sakaki, T. Noda, K. Hirakawa, and T. Matsusue, "Interface roughness scattering in GaAs/AlAs quantum wells," *Appl. Phys. Lett.*, vol. 51, pp. 1934–1936, 1987.

[46] B. Radisavljevic, A. Radenovic, J. Brivio, V. Giacometti, and A. Kis, "Single-layer MoS_2 transistors," *Nature Nanotechnol.*, vol. 6, pp. 147–150, 2011.

[47] D. Jena and A. Konar, "Enhancement of carrier mobility in semiconductor nanostructures by dielectric engineering," *Phys. Rev. Lett.*, vol. 98, pp. 136805-1–136805-4, 2007.

[48] C. Jang, S. Adam, J. H. Chen, E. D. Williams, S. Das Sarma, and M. S. Fuhrer, "Tuning the effective fine structure constant in graphene: Opposing effects of dielectric screening on short- and long-range potential screening," *Phys. Rev. Lett.*, vol. 101, pp. 146805-1–146805-4, 2008.

[49] A. K. M. Newaz, Y. S. Puzyrev, B. Wang, S. Pantelides, and K. I. Bolotin, "Probing charge scattering mechanisms in suspended graphene by varying its dielectric environment," *Nature Commun.*, vol. 3, pp. 7341–7346, 2012.

[50] H. Kroemer, "Two integral relations pertaining to the electron transport through a bipolar transistor with a nonuniform energy gap in the base region," *Solid State Elecron.*, vol. 28, pp. 1101–1103, 1985.

[51] L. Ci, L. Song, C. Jin, D. Jariwala, D. Wu, Y. Li, A. Srivastava, Z. F. Wang, K. Storr, L. Balicas, F. Liu, and P. M. Ajayan, "Atomic layers of hybridized boron nitride and graphene domains," *Nature Mater.*, vol. 9, pp. 430–435, 2010.

[52] H. Yang, J. Heo, S. Park, H. J. Song, D. H. Seo, K. E. Byun, P. Kim, I. Yoo, H. J. Chung, and K. Kim, "Graphene barristor, a triode device with a gate-controlled Schottky barrier," *Science*, vol. 336, pp. 1140–1143, 2012.

[53] L. Britnell, R. V. Gorbachev, R. Jalil, R. D. Belle, F. Schedin, A. Mischenko, T. Georgiou, M. I. Katsnelson, L. Eaves, S. V. Morozov, N. M. R. Peres, J. Leist, A. K. Geim, K. S. Novoselov, and L. A. Ponomarenko, "Field-effect tunneling transistor based on vertical graphene heterostructures," *Science*, vol. 335, pp. 947–950, 2012.

[54] S. K. Banerjee, L. F. Register, E. Tutuc, D. Reddy, and A. H. MacDonald, "Bilayer pseudospin field-effect transistor (BiSFET): A proposed new logic device," *IEEE Electron Device Lett.*, vol. 30, no. 2, pp. 158–160, Feb. 2009.

[55] P. Zhao, R. M. Feenstra, G. Gu, and D. Jena, "SymFET: A proposed symmetric graphene tunneling field-effect transistor," in *IEEE Device Res. Conf. Tech. Dig.*, 2012, pp. 33–34.

[56] G. Gu, S. Nie, R. M. Feenstra, R. P. Devaty, W. J. Choyke, W. K. Chan, and M. G. Kane, "Field effect in epitaxial graphene on a silicon carbide substrate," *Appl. Phys. Lett.*, vol. 90, pp. 253507-1–253507-3, 2007.

[57] J. S. Moon, D. Curtis, M. Hu, D. Wong, C. McGuire, P. M. Campbell, G. Jernigan, J. L. Tedesco, B. VanMil, R. Myers-Ward, C. Eddy, and D. K. Gaskill, "Epitaxial-graphene RF field-effect transistors on Si-face 6H-SiC substrates," *IEEE Electron Device Lett.*, vol. 30, no. 6, pp. 650–652, Jun. 2009.

[58] X. Li, W. Cai, S. Kim, J. Nah, D. Yang, R. Piner, A. Velamakanni, I. Jung, E. Tutuc, S. K. Banerjee, L. Colombo, and R. S. Ruoff, "Large-area synthesis of high-quality and uniform graphene films on copper foils," *Science*, vol. 324, pp. 1312–1314, 2009.

[59] W. S. Hwang, K. Tahy, X. Li, H. G. Xing, A. C. Seabaugh, C. Y. Sung, and D. Jena, "Transport properties of graphene nanoribbon transistors on chemical-vapor-deposition grown wafer-scale graphene," *Appl. Phys. Lett.*, vol. 100, pp. 203107-1–203107-3, 2012.

[60] L. Song, L. Ci, H. Lu, P. Sorokin, C. Jin, J. Ni, A. G. Kvashnin, D. G. Kvashnin, J. Lou, B. I. Yakobson, and P. M. Ajayan, "Large scale growth and characterization of atomic hexagonal boron nitride layers," *Nano Lett.*, vol. 10, pp. 3209–3215, 2010.

[61] Y. H. Lee, X. Q. Zhang, W. Zhang, M. T. Chang, C. T. Lin, K. D. Chang, Y. C. Yu, J. T. W. Wang, C. S. Chang, L. J. Li, and T. W. Lin, "Synthesis of large-area MoS_2 atomic layers with chemical vapor deposition," *Adv. Mater.*, vol. 24, pp. 2320–2325, 2012.

[62] W. S. Hwang, M. Remskar, R. Yan, V. Protasenko, K. Tahy, S. D. Chae, P. Zhao, A. Konar, H. G. Xing, A. C. Seabaugh, and D. Jena, "Transistors with chemically synthesized layered semiconductor WS_2 exhibiting 10^5 room temperature modulation and ambipolar behavior," *Appl. Phys. Lett.*, vol. 101, pp. 013107-1–013107-4, 2012.

[63] J. M. Martin, C. Donnet, T. Le Mogne, and T. Epicier, "Superlubricity of molybdenum disulphide," *Phys. Rev. B.*, vol. 48, pp. 10583–10586, 1993.

[64] S. Kim, A. Konar, W. S. Hwang, J. H. Lee, J. Lee, J. Yang, C. Jung, H. Kim, J. B. Yoo, J. Y. Choi, Y. W. Jin, S. Y. Lee, D. Jena, W. Choi, and K. Kim, "High-mobility, low-power thin-film transistors based on multilayer MoS_2 crystals *Nature Commun.*, article 1011, DOI: 10.1038/ncomms2018.

[65] C. Zener, "A theory of the electrical breakdown of solid dielectrics," *Proc. R. Soc. Lond. A.*, vol. 145, pp. 523–529, 1934.

[66] C. Wittig, "The Landau-Zener formula," *J. Phys. Chem. B*, vol. 109, pp. 8428–8430, 2005.

[67] R. Shankar, *Principles of Quantum Mechanics*, 2nd ed. New York, NY, USA: Plenum, 1994, pp. 435–449.

[68] S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices*, 3rd ed. New York, NY, USA: Wiley-Interscience, 2006.

[69] A. C. Seabaugh and Q. Zhang, "Low-voltage tunnel transistors for beyond CMOS logic," *Proc. IEEE*, vol. 98, no. 12, pp. 2095–2110, Dec. 2010.

[70] V. Cheianov and V. I. Fal'ko, "Selective transmission of Dirac electrons and ballistic magnetoresistance of n-p junctins in graphene," *Phys. Rev. B.*, vol. 74, pp. 041403(R)-1–041403(R)-4, 2006.

[71] T. Fang, "Carrier transport in graphene, graphene nanoribbons, and GaN HEMTs," Ph.D. dissertation, Dept. Electr. Eng., Univ. Notre Dame, Notre Dame, IN, USA, 2012.

[72] E. McCann, "Asymmetry gap in the electronic band structure of bilayer graphene," *Phys. Rev. B*, vol. 74, pp. 161403(R)-1–161403(R)-4, 2006.

[73] Y. Zhang, T. T. Tang, C. Girit, Z. Hao, M. C. Martin, A. Zettl, M. F. Crommie, Y. R. Shen, and F. Wang, "Direct observation of a widely tunable bandgap in bilayer graphene," *Nature*, vol. 459, pp. 820–823, 2009.

[74] F. Xia, D. B. Farmer, Y. M. Lin, and P. Avouris, "Graphene field-effect transistors with high on/off current ratio and large transport band gap at room temperature," *Nano Lett.*, vol. 10, pp. 715–718, 2010.

[75] D. Jena, T. Fang, Q. Zhang, and H. Xing, "Zener tunneling in semionducting nanotube and graphene nanoribbon p-n junctions," *Appl. Phys. Lett.*, vol. 93, pp. 112106-1–112106-3, 2008.

[76] M. Rodwell, W. Frensley, S. Steiger, E. Chagarov, S. Lee, H. Ryu, Y. Tan, G. Hegde, L. Wang, J. Law, T. Boykin, G. Klimek, P. Asbeck, A. Kummel, and J. N. Schulman, "III-V FET channel designs for high current densities and thin inversion layers," in *IEEE Device Res. Conf. Tech. Dig.*, 2010, pp. 149–152.

[77] W. Y. Choi, B. G. Park, J. D. Lee, and T. K. K. Liu, "Tunneling field-effect transistors (TFETs) with subthreshold swing (SS) less than 60 mV/dec," *IEEE Electron Device Lett.*, vol. 28, no. 8, pp. 743–745, Aug. 2007.

[78] S. H. Kim, H. Kam, C. Hu, and T. K. K. Liu, "Germanium-source tunnel field-effect transistors with record high Ion/Ioff," in *Proc. Very Large Scale Integr. (VLSI) Technol. Symp.*, 2009, pp. 178–179.

[79] F. Mayer, C. L. Oryer, J. F. Damlencourt, K. Romanjek, F. Andrieu, C. Tabone, B. Previtali, and S. Deleonibus, "Impact of SOI,$Si_{1-x}Ge_x$OI and GeOI substrates on CMOS compatible tunnel FET performance," in *IEEE Int. Electron Device Meeting Tech. Dig.*, 2008, pp. 163–166.

[80] J. Appenzeller, Y. M. Lin, J. Knoch, and P. Avouris, "Band-to-band tunneling in carbon nanotube field-effect transistors," *Phys. Rev. Lett.*, vol. 93, pp. 196805-1–196805-4, 2004.

[81] C. Hu, "Reduce IC power consumption by $> 10\times$ with a green transistor?" in *IEEE Device Res. Conf. Tech. Dig.*, 2009, pp. 9–10.

[82] R. Li, Y. Lu, G. Zhou, Q. Liu, S. D. Chae, T. Vasen, W. S. Hwang, Q. Zhang, P. Fay, T. Kosel, M. Wistey, H. Xing, and A. Seabaugh, "AlGaSb/InAs tunnel field-effect transistor with on-current of 78 μA/μm at 0.5 V," *IEEE Electron Device Lett.*, vol. 33, no. 3, pp. 363–365, Mar. 2012.

[83] L. Lattanzio, L. De Michielis, and A. M. Ionescu, "Complementary germanium electron-hole bilayer tunnel FET for sub-0.3 V operation," *IEEE Electron Device Lett.*, vol. 33, no. 2, pp. 167–169, Feb. 2012.

[84] G. Fiori and G. Iannaccone, "Ultralow-voltage bilayer graphene tunnel FET," *IEEE Electron Device Lett.*, vol. 30, no. 10, pp. 1096–1098, Oct. 2009.

[85] Y. Wu, D. B. Farmer, W. Zhu, S. J. Han, C. D. Dimitrakopoulos, A. A. Bol, P. Avouris, and Y. M. Lin, "Three-terminal graphene negative differential resistance devices," *ACS Nano.*, vol. 6, pp. 2610–2616, 2012.

[86] J. Knoch and J. Appenzeller, "Tunneling phenomena in carbon nanotube field-effect transistors," *Phys. Stat. Solidi (A)*, vol. 205, pp. 679–694, 2008.

[87] Q. Zhang, T. Fang, H. Xing, A. Seabaugh, and D. Jena, "Graphene nanoribbon tunnel transistors," *IEEE Electron Device Lett.*, vol. 29, no. 12, pp. 1344–1346, Dec. 2008.

[88] M. S. Arnold, A. A. Green, J. F. Hulvat, S. I. Stupp, and M. C. Hersam, "Sorting carbon nanotubes by electronic structure using density differentiation," *Nature Nanotechnol.*, vol. 1, pp. 60–65, 2006.

[89] X. Wang, X. Li, L. Zhang, Y. Yoon, P. K. Weber, H. Wang, J. Guo, and H. Dai, "N-doping of graphene through electrothermal reactions with ammonia," *Science*, vol. 324, pp. 768–771, 2009.

[90] M. Luisier and G. Klimeck, "Performance analysis of statistical samples of graphene nanoribbon tunneling transistors with line edge roughness," *Appl. Phys. Lett.*, vol. 94, pp. 223505-1–223505-3, 2009.

[91] S. O. Koswatta, S. J. Koester, and W. Haensch, "On the possibility of obtaining MOSFET-like performance and sub-60-mV/dec swing in 1D broken-gap tunnel transistors," in *IEEE Int. Electron Device Meeting Tech. Dig.*, 2010, pp. 3222–3230.

[92] K. T. Lam, D. Seah, S. K. Chin, S. B. Kumar, G. Samudra, Y. C. Yeo, and G. Liang, "A simulation study of graphene-nanoribbon tunneling FET with heterojunction channel," *IEEE Electron Device Lett.*, vol. 31, no. 6, pp. 555–557, Jun. 2010.

[93] H. Da, K. T. Lam, G. Samudra, S. K. Chin, and G. Liang, "Graphene nanoribbon tunneling field-effect transistors with a semiconducting and a semimetallic heterojunction channel," *IEEE Trans. Electron Devices*, vol. 59, no. 5, pp. 1454–1461, May 2012.

[94] Y. Yoon and S. Salahuddin, "Barrier-free tunneling in a carbon heterojunctions transistor," *Appl. Phys. Lett.*, vol. 97, pp. 033102-1–033102-3, 2010.

[95] D. Sarkar, M. Krall, and K. Banerjee, "Electron-hole duality during band-to-band tunneling process in graphene-nanoribbon tunnel-field-effect-transistors," *Appl. Phys. Lett.*, vol. 97, pp. 236109-1–236109-3, 2010.

[96] S. Agarwal and E. Yablonovitch, "Pronounced effect of pn-junction dimensionality on tunnel switch sharpness." [Online]. Available: arXiv:1109.0096

[97] J. Bardeen, "Tunneling from a many-particle point of view," *Phys. Rev. Lett.*, vol. 6, pp. 57–59, 1961.

[98] R. M. Feenstra, Y. Dong, M. P. Semstiv, and W. T. Masselink, "Influence of tip-induced band bending on tunneling spectra of semiconductor surfaces," *Nanotechnology*, vol. 18, pp. 044105-1–044105-7, 2007.

[99] V. Ambegaokar and A. Baratoff, "Tunneling between superconductors," *Phys. Rev. Lett.*, vol. 10, pp. 486–489, 1963.

[100] R. M. Feenstra, D. Jena, and G. Gu, "Single-particle tunneling in doped graphene-insulator-graphene junctions," *J. Appl. Phys.*, vol. 111, pp. 043711-1–043711-10, 2012.

[101] J. A. Simmons, M. A. Blount, J. S. Moon, S. K. Lyo, W. E. Baca, J. R. Wendt, J. L. Reno, and M. J. Hafich, "Planar quantum transistor based on 2D-2D tunneling in double quantum well heterostructures," *J. Appl. Phys.*, vol. 84, pp. 5626–5634, 1998.

[102] H. Sahin, S. Cahangirov, M. Topsakal, E. Bekaroglu, E. Akturk, R. T. Senger, and S. Ciraci, "Monolayer honeycomb structures of group-IV elements and III-V binary compounds: First-principles calculations," *Phys. Rev. B.*, vol. 80, pp. 155453-1–155453-12, 2009.

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Charge Scattering and Mobility in Atomically Thin Semiconductors

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The electron transport properties of atomically thin semiconductors such as MoS_2 have attracted significant recent scrutiny and controversy. In this work, the scattering mechanisms responsible for limiting the mobility of single-layer semiconductors are evaluated. The roles of individual scattering rates are tracked as the two-dimensional electron gas density is varied over orders of magnitude at various temperatures. From a comparative study of the individual scattering mechanisms, we conclude that all current reported values of mobilities in atomically thin transition-metal dichalcogenide semiconductors are limited by ionized impurity scattering. When the charged impurity densities are reduced, remote optical phonon scattering will determine the ceiling of the highest mobilities attainable in these ultrathin materials at room temperature. The intrinsic mobilities will be accessible only in clean suspended layers, as is also the case for graphene. Based on the study, we identify the best choices for surrounding dielectrics that will help attain the highest mobilities.

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Two-dimensional (2D) layered crystals such as single layers of transition-metal dichalcogenides represent the thinnest possible manifestations of semiconductor materials that exhibit an energy band gap. For example, a single-layer (SL) MoS_2 is around ~0.6 nm thick and exhibits an energy band gap of around ~1.8 eV [1]. Such semiconductor layers differ fundamentally from ultrathin heterostructure quantum wells or thin membranes carved out of three-dimensional (3D) semiconductor materials because there are, in principle, no broken bonds, and no roughness over the 2D plane. In heterostructure quantum wells, the electron mobility suffers from variations in the quantum-well thickness. A classic "sixth-power law" from Sakaki *et al.* [2] shows that since the quantum-mechanical energy eigenvalues in a heterostructure quantum well of thickness L go as $\varepsilon \sim 1/L^2$, variations in thickness ΔL lead to perturbations of the energy $\Delta\varepsilon \sim -2\Delta L/L^3$. Since the scattering rate depends on the square of $\Delta\varepsilon$, the roughness-limited mobility degrades as $\mu_R \sim L^6$. When L reduces from about ~7 to ~5 nm for example, μ_R reduces from about 10^4 to 10^3 cm^2/Vs in GaAs/AlAs quantum wells at 4.2 K [2]. Though low-temperature mobilities exceeding 10^6 cm^2/Vs have been achieved in such heterostructures by scrupulous cleanliness and design to reduce roughness scattering, the statistical variations in the quantum-well thickness during the epitaxial growth process pose a fundamental limit to electron mobility.

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Because of the absence of intrinsic roughness in atomically thin semiconductors, the expectation is that higher mobilities should, in principle, be attainable. However, recent measurements in MoS_2 and similar semiconductors [3–5] exhibit rather low mobilities in single layers, which are, in fact, lower than in their multilayer counterparts. Many-particle transport effects can appear in transition-metal dichalcogenides under special conditions because of the contribution of highly localized d-orbitals to the conduction and valence-band-edge eigenstates. Collective effects have been observed in multilayer structures, such as charge-density waves [6,7] and the appearance of superconductivity at extremely high metallic carrier densities [8] under extreme conditions. We do not discuss such collective phenomena here. Instead, we focus on single-particle transport in single-layer MoS_2; the only many-particle effect included is free-carrier screening. In this work, we perform a comprehensive study of the scattering mechanisms that limit electron mobility in atomically thin semiconductors. The mobility is calculated in the relaxation-time approximation (RTA) of the Boltzmann transport equation. The results shed light on the experimentally achievable electron mobility by designing the surrounding dielectrics and lowering the impurity density. The findings thus offer useful guidelines for future experiments.

With the advent of graphene, it was realized that for ultrathin semiconductors, the dielectric environment plays a crucial role in electron transport. It has now been demonstrated that the dielectric mismatch significantly modifies the Coulomb potentials inside a semiconductor thin layer [9–12]. Electrons in the semiconductor can also remotely excite polar-optical-phonon modes in the dielectrics [13–19]. Such long-range interactions become stronger as the thickness of the semiconductor layer decreases. Thus,

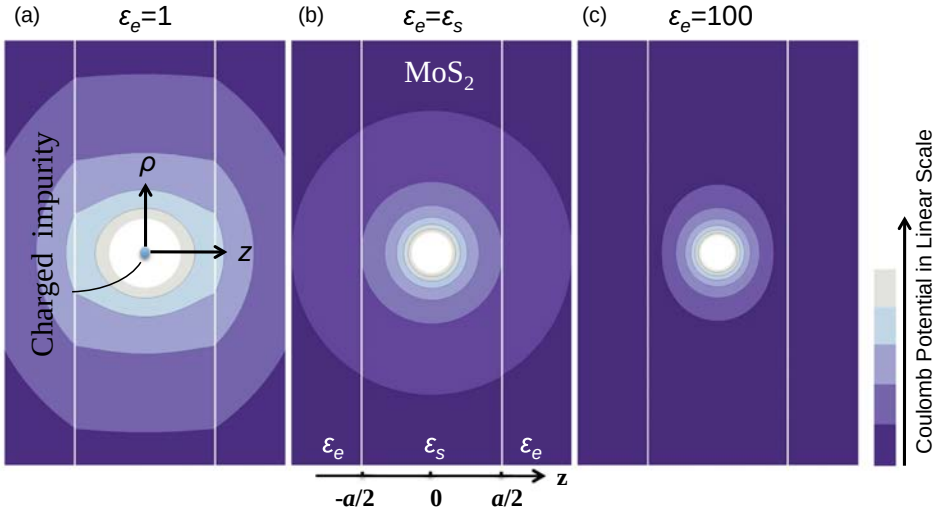

FIG. 1. Coulomb potential contours due to an on-center point charge for three different dielectric environments: $\varepsilon_e = 1, 7.6\,(=\varepsilon_s), 100$.

one can expect the dielectric environment to significantly affect electron transport properties in SL gapped semiconductors. In this work, we take SL MoS_2 as a case study to investigate such effects. The results and conclusions can be extended to other SL gapped semiconductors.

We first study the effect of the dielectric environment on Coulomb scattering of carriers from charged impurities located inside the MoS_2 single layer. Figure 1(a) shows a point charge located at the center ($z_0 = 0$) of a SL MoS_2 of thickness a. Assuming the surrounding dielectric provides a large energy barrier for confining electrons in the MoS_2 membrane, we consider scattering of electrons within the conduction band minima at the K point, i.e., in the ground state. The envelope function of mobile electrons is then $\psi_{\vec{k}}(\vec{\rho}, z) = \chi(z)e^{i\vec{k}\cdot\vec{\rho}}/\sqrt{S}$, where $\chi(z) = \sqrt{2/a}\cos(\pi z/a)$, S is the 2D area, $\vec{k}$ is the in-plane 2D wave vector, and $\vec{\rho}$ is the in-plane location vector of the electron from the point charge. The dielectric mismatch between the MoS_2 (relative dielectric constant ε_s) layer and its environment (ε_e) creates an infinite array of image charges at points $z_n = na$, where $n = \pm 1, \pm 2\ldots$ [9,10,20]. The nth point charge has a magnitude of $e\gamma^{|n|}$, where $\gamma = (\varepsilon_s - \varepsilon_e)/(\varepsilon_s + \varepsilon_e)$. These image charges contribute to the net electric potential seen by the electron, which is given by

$$V_{\text{unsc}}^{\text{CI}}(\rho, z) = \sum_{n=-\infty}^{\infty} \frac{e\gamma^{|n|}}{4\pi\varepsilon_0\varepsilon_s\sqrt{\rho^2 + |z - z_n|^2}}. \quad (1)$$

where e is the elementary charge, and ε_0 is the vacuum permittivity. Figure 1 shows the net unscreened Coulomb potential contours in the dielectric/MoS_2/dielectric system with three different ε_e. The Coulomb interaction is strongly enhanced for a low-κ dielectric environment and is damped for the high-κ case.

When a point charge is located inside a 3D semiconductor, its Coulomb potential is lowered by the dielectric constant of the semiconductor host alone. For thin semiconductor layers, the Coulomb potential is determined by the dielectric constants of both the semiconductor itself and the surrounding dielectrics. When a high density of mobile carriers is present in the semiconductor, the Coulomb potential is further screened. For atomically thin semiconductors, understanding the dielectric mismatch effect on the free-carrier screening of scattering potentials is necessary. At zero temperature, static screening by the 2D electron gas is captured by the Lindhard function [21]:

$$\varepsilon_{2d}(q, \omega \to 0) = 1 + \frac{e^2}{2\varepsilon_0\varepsilon_s q}\Pi(q, \omega \to 0)(\Phi_1 + \Phi_2), \quad (2)$$

where q is the 2D scattering wave vector, and Π is the polarizability function at zero temperature [22],

$$\Pi(q, \omega \to 0) = \frac{g_s g_v m^*}{2\pi\hbar^2}\left\{1 - \Theta[q - 2k_F]\sqrt{1 - \left(\frac{2k_F}{q}\right)^2}\right\}, \quad (3)$$

where g_s, g_v are the spin and valley degeneracy factors, respectively, m^* is the electron mass, k_F is the Fermi wave vector, and $\Theta[\ldots]$ is the Heaviside unit-step function. The function Φ_1 is the form factor, and Φ_2 is the dielectric mismatch factor, which are defined by the equations [23]

$$\Phi_1 = \int \chi^2(z)dz \int \chi^2(z')\exp(-q|z - z'|)dz', \quad (4)$$

$$\Phi_2 = \frac{2\chi_+\chi_-\exp(-qa)(\varepsilon_e - \varepsilon_s)^2 - (\chi_-^2 + \chi_+^2)(\varepsilon_e^2 - \varepsilon_s^2)}{\exp(qa)(\varepsilon_e + \varepsilon_s)^2 - \exp(-qa)(\varepsilon_e - \varepsilon_s)^2}, \quad (5)$$

where $\chi_\pm = \int dz \exp(\pm qz)\chi^2(z)$. The free-carrier screening is taken into account by dividing the unscreened

scattering matrix elements by ε_{2d}. Equation (2) can be recast as the Thomas-Fermi formula: $\varepsilon_{2d} = 1 + q_{\mathrm{TF}}^{\mathrm{eff}}/q$, in analogy to the case in the absence of a dielectric mismatch. Here, $q_{\mathrm{TF}}^{\mathrm{eff}}$ corresponds to the Thomas-Fermi screening wave vector q_{TF}^{0} without a dielectric mismatch. Figure 2(a) shows the ratio $q_{\mathrm{TF}}^{\mathrm{eff}}/q_{\mathrm{TF}}^{0}$ that captures the effect of the dielectric mismatch on screening at zero temperature. The 2D electron density is $n_s \sim 10^{12}$ cm^{-2} in this figure. As can be seen, the free-carrier screening is weakened by a high-κ dielectric, and it is enhanced in the low-κ case. This dependence is opposite to the effect of the dielectric environment on the net unscreened Coulomb interaction.

The momentum relaxation rate $(\tau_m)^{-1}$ due to elastic scattering mechanisms is evaluated using Fermi's golden rule in the form

$$\frac{1}{\tau_m} = \frac{2\pi}{\hbar}\int \frac{d^2k'}{(2\pi)^2}\frac{|M_{kk'}|^2}{\varepsilon_{2d}^2}(1-\cos\theta)\delta(E_k - E_{k'}), \quad (6)$$

where $M_{kk'}$ is the matrix element for scattering from state k to k', θ is the scattering angle, and E_k and $E_{k'}$ are the electron energies for states k and k', respectively. For the charged impurity scattering momentum relaxation rate $(\tau_m^c)^{-1}$, the scattering matrix element is evaluated as

$$M_{kk'} = \frac{e^2}{2\varepsilon_0\varepsilon_s S}\frac{1}{q}\times 4\left\{\frac{\gamma}{\exp(qa)-\gamma}\frac{4\pi^2\sinh(\frac{qa}{2})}{4\pi^2(qa)+(qa)^3} + \frac{2[1-\exp(-\frac{qa}{2})]\pi^2+(qa)^2}{4\pi^2(qa)+(qa)^3}\right\}. \quad (7)$$

Figure 2(b) shows $(\tau_m^c)^{-1}$ with the impurity density of $N_I \sim 10^{12}$ cm^{-2}. ε_e and n_s are varied over 2 orders of magnitude to map out the parameter space. Evidently, $(\tau_m^c)^{-1}$ still reduces monotonically with increasing ε_e because the weakening of the unscreened Coulomb potential is stronger.

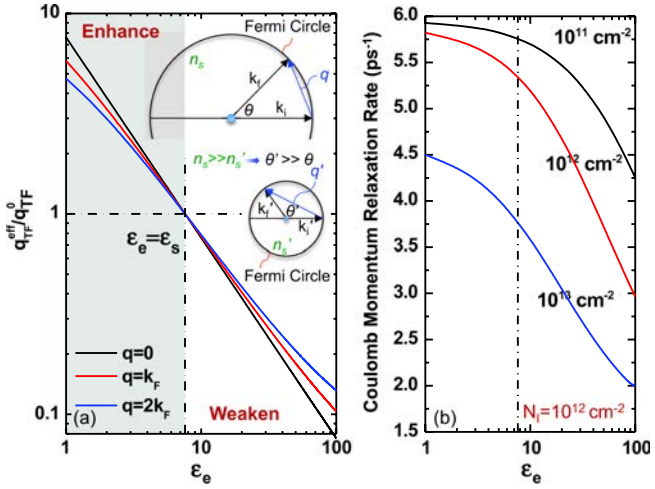

FIG. 2. Effect of dielectric mismatch on the (a) free-carrier screening and (b) Coulomb momentum relaxation rate at zero temperature. The inset of (a) shows schematically the scattering angle for different electron densities.

The reduction of $(\tau_m^c)^{-1}$ for a high-κ environment is much enhanced for high $n_{s'}$, as indicated in Fig. 2(b). When ε_e varies from 1 to 100, $(\tau_m^c)^{-1}$ decreases about ~1.4 times for $n_s \sim 10^{11}$ cm^{-2}, and about ~2.6 times for $n_s \sim 10^{13}$ cm^{-2}. From the perspective of screening, notice from Fig. 2(a) that in a low-κ environment, $q_{\mathrm{TF}}^{\mathrm{eff}}$ is higher for small-angle scattering events. This means the smaller the scattering angle, the stronger is the screening. Thus screening favors randomizing the electron momentum. A high-κ environment reverses this process: small angle scattering events are weakly screened, and thus such scattering events are favored. Thus, as ε_e increases, the electron transport become more directional. Though $q_{\mathrm{TF}}^{\mathrm{eff}}$ decreases, the net screening efficiency increases. These tendencies are enhanced as n_s increases. From the scattering potential point of view, a higher n_s leads to a larger Fermi wave vector k_F. As shown schematically in the inset of Fig. 2(a), the same $q = |\mathbf{k}_i - \mathbf{k}_f|$ with high n_s corresponds to a smaller scattering angle than a lower-n_s case, leading to a reduced $(\tau_m^c)^{-1}$. This effect on the Coulomb scattering matrix element is multiplied by the dielectric mismatch factor; thus, a high-n_s system shows stronger ε_e dependence at zero temperature.

For finite temperatures, following Maldague [22,24,25], the static polarizability function is

$$\Pi(q,T,E_F) = \int_0^\infty \frac{\Pi(q,\omega\to 0)}{4k_BT\cosh^2[(E_F-E)/2k_BT]}dE, \quad (8)$$

where E_F is the Fermi energy and k_B is the Boltzmann constant. Figure 3(a) shows the calculated temperature-dependent polarizability normalized to the zero-temperature value at different n_s. The electron gas is less polarizable at higher temperatures and lower n_s. Polarizability is caused by the spatial redistribution of the electron gas induced by the Coulomb potential; thus, it is proportional to n_s. As temperature increases, the thermal energy randomizes the electron momenta, accelerating the transition of the electron system back into an equilibrium distribution, consequently weakening the polarization. The decrease of polarizability reduces the free-carrier screening. Figure 3(b) shows the temperature-dependent Coulomb-scattering-limited mobility (μ_{imp}) at two different n_s. The dielectric mismatch effect is more significant for low n_s because of the fast decrease of the polarizability with increasing temperature. For high n_s, on the other hand, the dielectric mismatch effect is not as drastic. The shape of the temperature-dependent μ_{imp} curve is highly dependent on the polarizability and n_s. Consequently, if the electron transport is dominated by impurity scattering, one can infer n_s from the shape of the temperature dependence of the electron mobility.

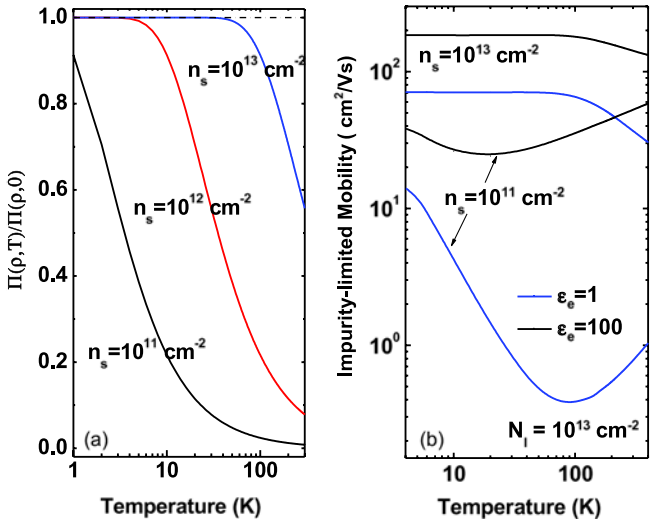

FIG. 3. (a) The normalized polarizability and (b) impurity-limited mobility at different electron densities as a function of temperature.

Much interest exists in using atomically thin semiconductors as possible channel materials for electronic devices, in which such layers are in close proximity to dielectrics. To that end, we investigate both the intrinsic and extrinsic phonon scattering in SL MoS_2. Kaasbjerg *et al.* [26] have predicted the theoretical intrinsic phonon-limited mobility ($\mu_{i-\mathrm{ph}}$) of SL MoS_2 from first principles using a density-functional-based approach. They estimated a room-temperature upper limit for the experimentally achievable mobility of about 410 $\mathrm{cm}^2/\mathrm{Vs}$, which weakly depended on n_s. Their estimate did not include the effects of free-carrier screening and dielectric mismatch. In light of the strong effect of these factors on the Coulomb scattering, we evaluate $\mu_{i-\mathrm{ph}}$ in MoS_2 in the Boltzmann transport formalism with the modified free-carrier screening. The material parameters for SL MoS_2 were obtained from Ref. [27]. The momentum relaxation rate due to quasielastic scattering by an acoustic phonon is given by

$$\frac{1}{\tau_m^{\mathrm{ac}}} = \frac{\Xi_{\mathrm{ac}}^2 k_B T m^*}{2\pi\hbar^3 \rho_s v_s^2} \int_{-\pi}^{\pi} \frac{(1-\cos\theta)d\theta}{\varepsilon_{2d}^2}, \tag{9}$$

where ρ_s is the areal mass density of SL MoS_2, v_s is the sound velocity, and Ξ_{ac} is the acoustic deformation potential. For inelastic electron-optical phonon interactions, the momentum relaxation rate in the RTA is obtained by summing the emission and absorption processes,

$$\frac{1}{\tau_m^{\mathrm{op}}} = \frac{\Theta[E_k - \hbar\omega_{\mathrm{op}}^{\nu}]}{\tau_{\mathrm{op}}^{+}} + \frac{1}{\tau_{\mathrm{op}}^{-}}, \tag{10}$$

where $\omega_{\mathrm{op}}^{\nu}$ is the frequency of the νth optical-phonon mode. The momentum relaxation rates with superscripts "+" and "−" are associated with phonon emission and absorption, respectively. For optical deformation potentials (ODP) [26],

$$\frac{1}{\tau_{0-\mathrm{ODP}}^{\pm}} = \frac{D_0^2 m^* (N_q + \frac{1}{2} \pm \frac{1}{2})}{4\pi\hbar^2 \rho_s \omega} \int_{-\pi}^{\pi} \frac{(1-(k'/k)\cos\theta)d\theta}{\varepsilon_{2d}^2}, \tag{11}$$

$$\frac{1}{\tau_{1-\mathrm{ODP}}^{\pm}} = \frac{D_1^2 m^* (N_q + \frac{1}{2} \pm \frac{1}{2})}{4\pi\hbar^2 \rho_s \omega} \int_{-\pi}^{\pi} \frac{q^2(1-(k'/k)\cos\theta)d\theta}{\varepsilon_{2d}^2}, \tag{12}$$

where D is the optical deformation potential, $N_q = 1/[\exp(\hbar\omega/k_B T) - 1]$ is the Bose-Einstein distribution for optical phonons of energy $\hbar\omega$, and the subscripts 0 and 1 denote the zero- and first-order ODP, respectively.

The scattering rate by polar-optical (LO) phonons is given by the Fröhlich interaction [28],

$$\frac{1}{\tau_{\mathrm{LO}}^{\pm}} = \frac{e^2 \omega m^*}{8\pi\hbar^2} \frac{1}{\varepsilon_0} \left(\frac{1}{\varepsilon_\infty} - \frac{1}{\varepsilon_s}\right) \left(N_q + \frac{1}{2} \pm \frac{1}{2}\right) \times \int_{-\pi}^{\pi} \frac{1}{q} \Phi_1 \frac{(1-(k'/k)\cos\theta)d\theta}{\varepsilon_{2d}^2}, \tag{13}$$

where ε_∞ is the high-frequency relative dielectric constant, and Φ_1 is the form factor defined by Eq. (4).

Figure 4(a) shows the n_s-dependent screened $\mu_{i-\mathrm{ph}}$ at room temperature. For comparison, the unscreened $\mu_{i-\mathrm{ph}}$ is

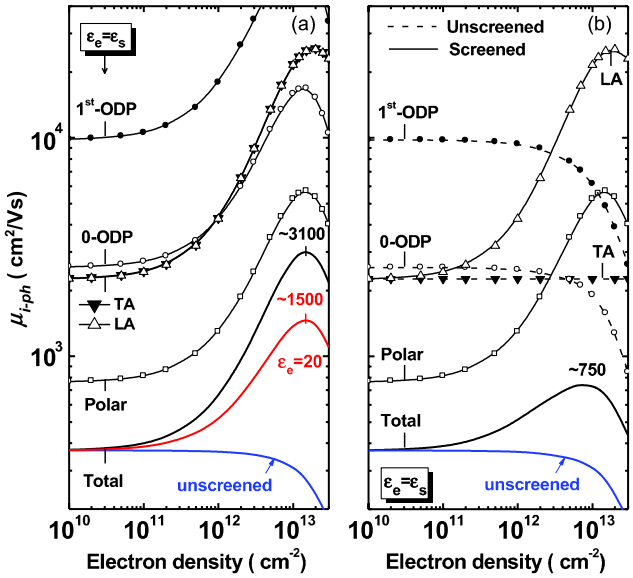

FIG. 4. Electron mobility in MoS_2 due to intrinsic phonon scattering at room temperature with the electron-phonon interaction (a) fully screened and (b) partially screened. The dashed lines show mobilities limited by unscreened phonon modes, and the solid lines show the mobilities limited by fully screened modes.

also shown as a reference (blue line). The unscreened values remain effectively constant (about 380 cm^2/Vs) over the range of n_s of interest (10^{11}–10^{13} cm^{-2}). This is in agreement with the previous predictions (320–410 cm^2/Vs) [26,29]. However, the screened increases sharply with increasing n_s. As can be seen in Fig. 4(a), introducing a high-κ dielectric leads to a reduction of $\mu_{i-\mathrm{ph}}$; the highest values of $\mu_{i-\mathrm{ph}}$ reduce from 3100 to 1500 cm^2/Vs as ε_e increases from about ~7.6 to about ~20. The strong dependence of $\mu_{i-\mathrm{ph}}$ on the dielectric environment is entirely due to the dielectric-mismatch effect on free-carrier screening since the unscreened phonon-scattering matrix element is not affected by ε_e. Over the entire range of n_s, longitudinal optical phonon scattering is dominant. This finding is different from previous works on multilayer MoS_2 transport where the room-temperature $\mu_{i-\mathrm{ph}}$ was determined by homopolar phonon scattering [30–32].

We have used the static dielectric function for calculating the screened interactions due to different modes of phonons in the limit $\omega \to 0$. Scattering mechanisms via long-range Coulomb interactions, such as charged impurities, polar-optical phonons, and piezoelectric acoustic phonons, can be effectively screened by free carriers. However, free carriers may not respond to rapidly changing scattering potentials originating from short-range interactions. There are arguments about to what extent the short-range deformation potentials induced by acoustic (ADP) and optical phonons (ODP) are screened by free carriers. Boguslawski and Mycielski [33] argue that in a single-valley conduction band, the deformation potentials (both ADP and ODP) are screened in the same way as the macroscopic (long-range) phonon potentials. But for multivalley semiconductors (Ge), only the longitudinal acoustic (LA) mode of the ADP can be effectively screened by free carriers. The free-carrier screening of the transverse acoustic (TA) mode ADP and ODP can, to a good approximation, be neglected. [34]. In SL MoS_2, Kaasbjerg *et al.* [27] have argued that the LA mode of the ADP can be treated as screened by the long-wavelength dielectric function, while the screening of the TA mode ADP by free carriers can be neglected.

Figure 4(b) highlights the effect of the partially screened electron-phonon interaction compared to the fully screened version in Fig. 4(a). For the plot in Fig. 4(b), we have screened the polar-optical and LA phonon scattering as in Fig. 4(a), and we leave the TA and ODP interactions unscreened. The highest $\mu_{i-\mathrm{ph}}$ reached by free-carrier screening effects is reduced to about 750 cm^2/Vs by not screening the DP modes. The mobility is dominated by the polar-optical phonon interaction at low carrier density and by TA and ODP at moderate and high densities. The scattering of electrons due to piezoelectric phonons is not considered because it is relevant only at very low temperatures and because there are still uncertainties in the piezoelectric coefficients of SL MoS_2 [27,35].

In both cases, the calculated room-temperature $\mu_{i-\mathrm{ph}}$ are much higher than reported experimental values, implying that there is still much room for improvement of mobilities in atomically thin semiconductors. For the rest of this work, we use the fully screened intrinsic phonon scattering, as shown in Fig. 4(a). To pinpoint the most severe scattering mechanisms limiting the mobility in current samples, we discuss an extrinsic phonon-scattering mechanism at play in these materials, again motivated by similar processes in graphene.

Electrons in semiconductor nanoscale membranes can excite phonons in the surrounding dielectrics via long-range Coulomb interactions, if the dielectrics support polar vibrational modes. Such "remote phonon" or "surface-optical" (SO) phonon scattering has been investigated recently for graphene and found to be far from negligible [15–17]. SO phonon scattering can severely degrade electron mobility; however, this process has not been studied systematically in atomically thin semiconductors. The electron-SO phonon interaction Hamiltonian is [15,17,18]

$$H_{e-\mathrm{SO}} = eF_\nu \sum_q \left[\frac{e^{-qz}}{\sqrt{q}}\left(e^{i\vec{q}\cdot\vec{\rho}}a_q^{\nu+} + e^{-i\vec{q}\cdot\vec{\rho}}a_q^{\nu}\right)\right], \quad (14)$$

where $a_q^{\nu+}(a_q^{\nu})$ represents the creation (annihilation) operator for the νth SO phonon mode. Neglecting the dielectric response of the atomically thin MoS_2 layer in lieu of the surrounding media, the electron-SO phonon coupling parameter F_ν is

$$F_\nu^2 = \frac{\hbar\omega_{\mathrm{SO}}^{\nu}}{2S\varepsilon_0}\left(\frac{1}{\varepsilon_{ox}^{\infty}+\varepsilon_{ox'}^{\infty}} - \frac{1}{\varepsilon_{ox}^{0}+\varepsilon_{ox'}^{\infty}}\right), \quad (15)$$

where $\varepsilon_{\mathrm{ox}}^{\infty}$ ($\varepsilon_{\mathrm{ox}}^{0}$) is the high- (low-) frequency dielectric constant of the dielectric hosting the SO phonon, and $\varepsilon_{\mathrm{ox}'}^{\infty}$ is the high-frequency dielectric constant from the dielectric on the other side of the membrane. The frequency of the SO phonon $\omega_{\mathrm{SO}}^{\nu}$ is [17,36]

$$\omega_{\mathrm{SO}}^{\nu} = \omega_{\mathrm{TO}}^{\nu}\left(\frac{\varepsilon_{\mathrm{ox}}^{0}+\varepsilon_{\mathrm{ox}'}^{\infty}}{\varepsilon_{\mathrm{ox}}^{\infty}+\varepsilon_{\mathrm{ox}'}^{\infty}}\right)^{1/2}, \quad (16)$$

where $\omega_{\mathrm{TO}}^{\nu}$ is the νth bulk transverse optical-phonon frequency in the dielectric. The scattering rate due to the SO phonon is then given by

$$\frac{1}{\tau_{\mathrm{SO}}^{\pm}} = \frac{32\pi^3 e^2 F_\nu^2 m^* S}{\hbar^3 a^2}\left(N_q + \frac{1}{2} \pm \frac{1}{2}\right) \times \int_{-\pi}^{\pi} \frac{1}{q}\frac{\sinh^2\left(\frac{aq}{2}\right)}{(4\pi^2 q + a^2 q^3)^2}\frac{(1-(k'/k)\cos\theta)d\theta}{\varepsilon_{2d}^2}. \quad (17)$$

Table I summarizes the parameters for some commonly used dielectrics.

Figure 5 shows the room-temperature electron mobility for various dielectric environments for two representative temperatures, 100 K and 300 K. N_I and n_s are both about 10^{13} cm^{-2}. The solid lines show the net mobility by combining the scattering from charged impurities, and intrinsic and SO phonons, whereas the dashed lines show the cases neglecting the SO phonons. When SO phonon scattering is absent, the electron mobility is limited almost entirely by $\mu_{\rm imp}$, which increases with ε_e because of the reduction of Coulomb scattering by dielectric screening. The addition of the SO phonon scattering does not change things much at 100 K, except for the highest ε_e case (HfO_2/ZrO_2). But it drastically reduces the electron mobility at room temperature, as is evident in Fig. 5. For instance, neglecting SO phonon scattering, one may expect that by using HfO_2/ZrO_2 as the dielectrics instead of SiO_2/air, the RT mobility $\mu_{\rm imp}$ should improve from about ~45 to 80 cm^2/Vs. However, when the SO phonon scattering is in action, the mobility in the $HfO_2/MoS_2/ZrO_2$ structure is actually degraded to around 25 cm^2/Vs, even lower than the SiO_2/air case. Thus, SL MoS_2 layers suffer from enhanced SO phonon scattering if they are in close proximity to high-κ dielectrics that allow low-energy polar vibrational modes.

To calibrate our calculations, we study the temperature-dependent electron mobility for SL MoS_2 embedded between SiO_2 and HfO_2 and compare the calculations with reported experimental results. This structure is often used in top-gated MoS_2 field effect transistors (FETs); thus, understanding the transport in it provides a pathway to understanding the device characteristics. In Fig. 6(a), the blue curves indicate calculated values of $\mu_{\rm imp}$ with different N_I, and the red line shows the SO phonon-scattering limited mobility ($\mu_{\rm SO}$), with $n_s \sim 10^{13}$ cm^{-2}. The temperature-dependent $\mu_{\rm SO}$ of each SO phonon mode follows the Arrhenius rule: $\mu_{\rm SO} \propto \exp(\hbar\omega_0/k_BT)$, and the net $\mu_{\rm SO}$ is dominated by the softest phonon mode with the lowest energy. The black curves indicate the net mobilities considering all scattering mechanisms discussed in this work. The open squares are the experimental results measured by the Hall effect on SL MoS_2 FETs from Ref. [4]. The N_I and n_s necessary to fit the data are indicated in Fig. 6(a). At low temperatures, the experimental electron mobility in SL MoS_2 is entirely limited by $\mu_{\rm imp}$. This is really not unexpected; it took several decades of careful epitaxial growth and ultraclean control to achieve the high mobilities in III-V semiconductors at low temperatures. Based on this study, we predict

TABLE I. SO phonon modes for different dielectrics.

	SiO_2[a]	AlN[a]	BN[b]	Al_2O_3[a]	HfO_2[a]	ZrO_2[a]
$\varepsilon_{ox}^{\infty}$	3.9	9.14	5.09	12.53	23	24
$\varepsilon_{ox}^{\infty}$	2.5	4.8	4.1	3.2	5.03	4
ω_{SO}^{1}	55.6	81.4	93.07	48.18	12.4	16.67
ω_{SO}^{2}	138.1	88.5	179.1	71.41	48.35	57.7

[a]Ref. [15]
[b]Ref. [37]

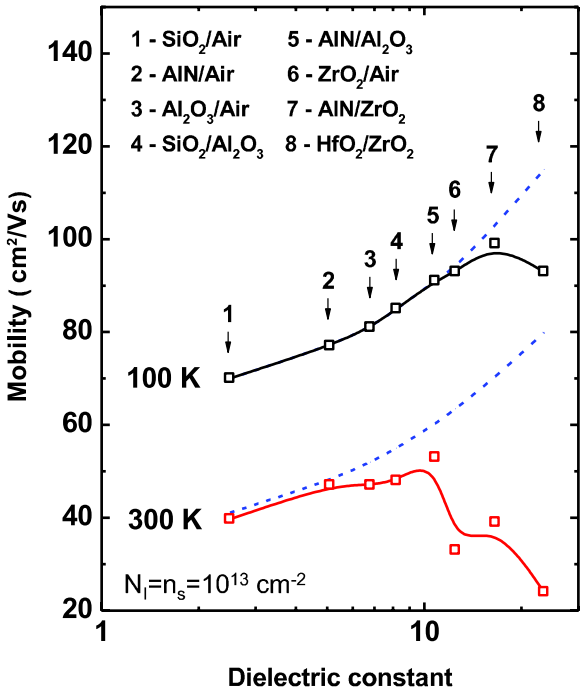

FIG. 5. Electron mobility as a function of an environment dielectric constant. Dashed lines show the mobility without considering the SO phonons.

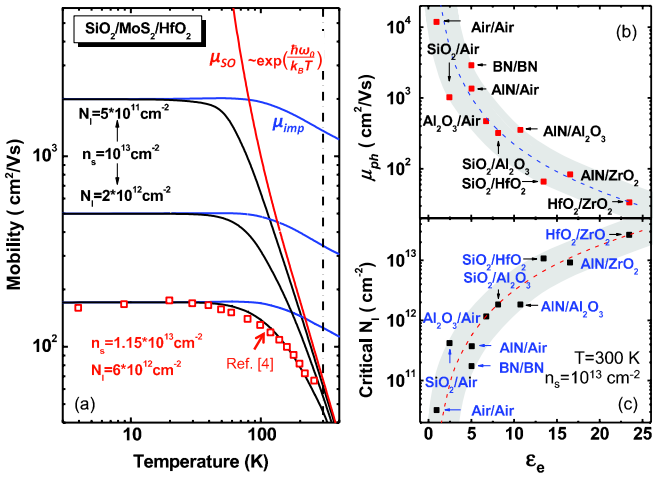

FIG. 6. (a) Temperature-dependent electron mobility (black lines) in $SiO_2/MoS_2/HfO_2$ structure. The blue lines indicate $\mu_{\rm imp}$ and the red lines show $\mu_{\rm SO}$. Open squares show experimental results from single-layer MoS_2 FETs from Ref. [4]. (b) Room-temperature phonon-determined electron mobilities$\mu_{\rm ph}$ and (c) the critical impurity densities $N_{\rm cr}$ corresponding to $\mu_{\rm imp} = \mu_{\rm ph}$ in SL MoS_2 surrounded by different dielectrics. Dashed lines show the fitted $\mu_{\rm ph}$ and $N_{\rm cr}$.

that the low-temperature mobilities in atomically thin semiconductors can be significantly improved by lowering the impurity density. The room-temperature mobility in III-V semiconductors is limited by intrinsic polar-optical phonon scattering. For comparison, we find that for SL MoS_2, the room-temperature mobility is considerably degraded by SO phonon scattering, even with N_I as high as 6×10^{12} cm^{-2}, as shown in Fig. 6. When SO phonon scattering is absent, the room-temperature mobility is expected to be about 130 cm^2/Vs with $N_I = 6 \times 10^{12}$ cm^{-2}, but the measured values are typically lower (about 50 cm^2/Vs). Consequently, using HfO_2 as gate dielectrics can modestly improve $\mu_{\rm imp}$. However, the strong SO phonon scattering that comes with HfO_2 can severely decrease the high-temperature electron mobility in clean MoS_2 with low charged impurity densities.

An important question then is, which dielectric can help improve the room-temperature electron mobility in SL MoS_2? To answer that question, in Fig. 6(b), we plot the room-temperature (intrinsic + SO) phonon-limited electron mobility ($\mu_{\rm ph}$) in SL MoS_2 surrounded by different dielectrics. From the overall trend, $\mu_{\rm ph}$ decreases with increasing ε_e, and suspended SL MoS_2 shows the highest potential electron mobility (over 10,000 cm^2/Vs). It is worth noting that if the scattering of electrons by intrinsic phonons is only partially screened, as shown in Fig. 4(b), the highest achievable mobility in SL MoS_2 will be an order lower (around 1000 cm^2/Vs). However, these high values are attainable in suspended SL MoS_2. Because $\mu_{\rm ph}$ for MoS_2 surrounded by high-κ materials is dominated by SO phonon scattering, the values do not vary much. The critical impurity densities ($N_{\rm cr}$) corresponding to $\mu_{\rm imp} = \mu_{\rm ph}$ are shown in Fig. 6(c). As long as $N_I \geq N_{\rm cr}$, $\mu_{\rm imp}$ completely masks $\mu_{\rm ph}$. When $N_I < N_{\rm cr}$, the electron mobility becomes dominated by phonons and moves towards the upper limit. High $\mu_{\rm ph}$ indicates a greater potential for attaining higher electron mobilities. However, we also need the sample to be highly pure. In high-κ environments that support low-energy polar vibrational modes, there is not as much room for improving the electron mobility as in low-κ structures. A compromise is seen for Aluminum Nitride (AlN)- and Boron Nitride (BN)-based dielectrics, which by virtue of the light atom N, allows high-energy optical modes in spite of their polar nature. From Figs. 6(b) and 6(c), one can obtain two useful relationships for single-layer MoS_2: $\mu_{\rm ph} \sim 35000/\varepsilon_e^{2.2}$ cm^2/Vs and $N_{\rm cr} \sim 10^{10}\varepsilon_e^{2.5}$ cm^{-2}, with n_s set at a typical on-state carrier density of 10^{13} cm^{-2}, as shown by dashed lines. These empirical relations should guide the proper choice of dielectrics and the maximum allowed impurity densities.

To further illustrate the relative importance of SO phonon and charged impurity scattering in SL MoS_2, we vary N_I and n_s in different dielectric environments and check the changing trends of electron mobilities at room temperature. Figure 7(a) shows the net electron mobilities in SL MoS_2 as a function of N_I with $n_s = 10^{13}$ cm^{-2}. Figures 7(b) and 7(c) show the electron mobility as a function of n_s for $N_I = 10^{11}$ and 10^{13} cm^{-2}. The electron mobility is weakly dependent on the dielectric environment at high N_I ($>10^{13}$ cm^{-2}), as shown in the dashed box in the bottom right corner of Fig. 7(a). Within this window, high-κ dielectrics can improve the mobility, but only very nominally because the unscreened mobilities are already quite low. When N_I is lowered below about 10^{12} cm^{-2}, a low-κ environment shows higher electron mobility. For most of the dielectric environments, when $N_I > 10^{12}$ cm^{-2}, the mobility fits the following empirical impurity-scattering-dominated relationship: $\mu \approx 4200/[N_I/10^{11}\ {\rm cm}^{-2}]\,{\rm cm}^2/{\rm Vs}$, as shown by the dashed line in Fig. 7(a). Using this expression, one can estimate N_I from measured electron mobility for high n_s. As n_s decreases, electron mobilities in different dielectric environments start to separate from each other, as shown in Fig. 7(c). In this case, the electron mobilities can fit the following relationship: $\mu \approx \frac{3500}{N_I/10^{11}\,{\rm cm}^{-2}}[A(\varepsilon_e) + (\frac{n_s}{10^{13}\,{\rm cm}^{-2}})^{1.2}]\,{\rm cm}^2/{\rm Vs}$ for $n_s < 10^{13}$ cm^{-2}, shown as dashed lines in Fig. 7(c). $A(\varepsilon_e)$ is a fitting constant depending on ε_e, and some values are listed in the inset table of Fig. 7(c). High-κ dielectrics with low-energy phonons (HfO_2, ZrO_2) severely degrade the electron mobility over the entire N_I range because of the dominant effect of SO phonon scattering. Note that the dielectric mismatch effect can be slightly overestimated here since we have assumed the thickness of the dielectric to be infinite [25]. In top-gated FETs, the top dielectric could be very thin. Thus, the capability of improving electron mobility by high-κ dielectrics can be even less significant. Since most applications require high mobilities,

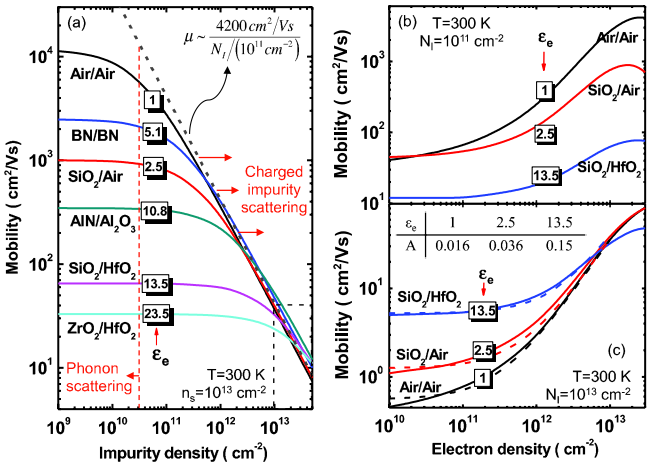

FIG. 7. The room-temperature net electron mobilities in SL MoS_2, considering all kinds of scattering mechanisms as a function of (a) N_I with fixed n_s at 10^{13} cm^{-2}; (b) and (c) n_s with N_I fixing at 10^{11} and 10^{13} cm^{-2}, respectively. The numbers on the curves show the average dielectric constant of the surrounding dielectrics. Dashed lines show the fitted electron mobilities.

high n_s, and high ε_e to be present simultaneously in the same structure for achieving the highest conductivities, AlN/Al_2O_3 or BN/BN encapsulation emerges as the best compromise among the dielectric choices considered here. One can also conceive of dielectric heterostructures, with a few BN layers closest to MoS_2 to damp out the SO phonon scattering, followed by higher-κ dielectrics to enhance the gate capacitance for achieving high carrier densities. All this, however, requires ultraclean MoS_2 to start with, with N_I well below 10^{12} cm^{-2} to attain the high room-temperature mobilities, about 1000 cm^2/Vs. The presence of high impurity densities will always mask the intrinsic potential of the materials, and this is the most important challenge moving forward.

In conclusion, carrier transport properties in atomically thin semiconductors are found to be highly dependent on the dielectric environment and on the impurity density. For current 2D crystal materials, electron mobilities are mostly dominated by charged impurity scattering. Remote phonons play a secondary role at high temperature depending on the surrounding dielectrics. The major point is that the mobilities achieved to date are far below the intrinsic potential in these materials. High-κ gate dielectrics can increase the electron mobility only for samples infected with very high impurity densities. Clean samples with low-κ dielectrics show much higher electron mobilities. AlN- and BN-based dielectrics offer the best compromise if a high-mobility and high-gate capacitance are simultaneously desired, as is the case in field-effect transistors. The truly intrinsic mobility limited by the atomically thin semiconductor itself can only be achieved in ultraclean suspended samples, as is the case for graphene.

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[1] K. F. Mak, C. Lee, J. Hone, J. Shan, and T. F. Heinz, *Atomically Thin* MoS_2*: A New Direct-Gap Semiconductor*, Phys. Rev. Lett. **105**, 136805 (2010).

[2] H. Sakaki, T. Noda, K. Hirakawa, M. Tanaka, and T. Matsusue, *Interface Roughness Scattering in GaAs/AlAs Quantum Wells*, Appl. Phys. Lett. **51**, 1934 (1987).

[3] D. Jariwala, V. K. Sangwan, D. J. Late, J. E. Johns, V. P. Dravid, T. J. Marks, L. J. Lauhon, and M. C. Hersam, *Band-like Transport in High Mobility Unencapsulated Single-Layer* MoS_2 *Transistors*, Appl. Phys. Lett. **102**, 173107 (2013).

[4] B. Radisavljevic and A. Kis, *Mobility Engineering and a Metal–Insulator Transition in Monolayer* MoS_2, Nat. Mater. **12**, 815 (2013).

[5] H. Fang, S. Chuang, T. C. Chang, K. Takei, T. Takahashi, and A. Javey, *High-Performance Single Layered* Wse_2 *p-FETs with Chemically Doped Contacts*, Nano Lett. **12**, 3788 (2012).

[6] J. A. Wilson, F. J. Di Salvo, and S. Mahajan, *Charge-Density Waves in Metallic, Layered, Transition-Metal Dichalcogenides*, Phys. Rev. Lett. **32**, 882 (1974).

[7] A. H. Castro Neto, *Charge Density Wave, Superconductivity, and Anomalous Metallic Behavior in 2D Transition Metal Dichalcogenides*, Phys. Rev. Lett. **86**, 4382 (2001).

[8] J. T. Ye, Y. J. Zhang, R. Akashi, M. S. Bahramy, R. Arita, and Y. Iwasa, *Superconducting Dome in a Gate-Tuned Band Insulator*, Science **338**, 1193 (2012).

[9] D. Jena and A. Konar, *Enhancement of Carrier Mobility in Semiconductor Nanostructures by Dielectric Engineering*, Phys. Rev. Lett. **98**, 136805 (2007).

[10] A. Konar and D. Jena, *Tailoring the Carrier Mobility of Semiconductor Nanowires by Remote Dielectrics*, J. Appl. Phys. **102**, 123705 (2007).

[11] A. K. M. Newaz, Y. S. Puzyrev, B. Wang, S. T. Pantelides, and K. I. Bolotin, *Probing Charge Scattering Mechanisms in Suspended Graphene by Varying Its Dielectric Environment*, Nat. Commun. **3**, 734 (2012).

[12] S.-L. Li, K. Wakabayashi, Y. Xu, S. Nakaharai, K. Komatsu, W.-W. Li, Y.-F. Lin, A. Aparecido-Ferreira, and K. Tsukagoshi, *Thickness-Dependent Interfacial Coulomb Scattering in Atomically Thin Field-Effect Transistors*, Nano Lett. **13**, 3546 (2013).

[13] K. Hess and P. Vogl, *Remote Polar Phonon Scattering in Silicon Inversion Layers*, Solid State Commun. **30**, 807 (1979).

[14] B. T. Moore and D. K. Ferry, *Remote Polar Phonon Scattering in Si Inversion Layers*, J. Appl. Phys. **51**, 2603 (1980).

[15] A. Konar, T. Fang, and D. Jena, *Effect of High-κ Gate Dielectrics on Charge Transport in Graphene-Based Field Effect Transistors*, Phys. Rev. B **82**, 115452 (2010).

[16] J.-H. Chen, C. Jang, S. D. Xiao, M. Ishigami, and M. S. Fuhrer, *Intrinsic and Extrinsic Performance Limits of Graphene Devices on* SiO_2, Nat. Nanotechnol. **3**, 206 (2008).

[17] S. Fratini and F. Guinea, *Substrate-Limited Electron Dynamics in Graphene*, Phys. Rev. B **77**, 195415 (2008).

[18] M. V. Fischetti, D. A. Neumayer, and E. A. Cartier, *Effective Electron Mobility in Si Inversion Layers in MOS Systems with a High-κ Insulator: The Role of Remote Phonon Scattering*, J. Appl. Phys. **90**, 4587 (2001).

[19] L. Zeng, Z. Xin, S. Chen, G. Du, J. F. Kang, and X. Y. Liu, *Remote Phonon and Impurity Screening Effect of Substrate and Gate Dielectric on Electron Dynamics in Single Layer* MoS_2, Appl. Phys. Lett. **103**, 113505 (2013).

[20] M. Kumagai and T. Takagahara, *Excitonic and Nonlinear-Optical Properties of Dielectric Quantum-Well Structures*, Phys. Rev. B **40**, 12 359 (1989).

[21] F. Stern, *Calculated Temperature Dependence of Mobility in Silicon Inversion Layers*, Phys. Rev. Lett. **44**, 1469

(1980); , *Polarizability of a Two-Dimensional Electron Gas*, Phys. Rev. Lett. **18**, 546 (1967).

[22] K. Hirakawa and H. Sakaki, *Mobility of the Two-Dimensional Electron Gas at Selectively Doped n-type* $Al_xGa_{1-x}As/GaAs$ *Heterojunctions with Controlled Electron Concentrations*, Phys. Rev. B **33**, 8291 (1986).

[23] B. A. Glavin, V. I. Pipa, V. V. Mitin, and M. A. Stroscio, *Relaxation of a Two-Dimensional Electron Gas in Semiconductor Thin Films at Low Temperatures: Role of Acoustic Phonon Confinement*, Phys. Rev. B **65**, 205315 (2002).

[24] P. Maldague, *Many-Body Corrections to the Polarizability of the Two-Dimensional Electron Gas*, Surf. Sci. **73**, 296 (1978).

[25] Z.-Y. Ong and M. V. Fischetti, *Mobility Enhancement and Temperature Dependence in Top-Gated Single-Layer* MoS_2, Phys. Rev. B **88**, 165316 (2013).

[26] K. Kaasbjerg, K. S. Thygesen, and K. W. Jacobsen, *Phonon-Limited Mobility in n-Type Single-Layer* MoS_2 *from First Principles*, Phys. Rev. B **85**, 115317 (2012).

[27] K. Kaasbjerg, K. S. Thygesen, and A.-P. Jauho, *Acoustic Phonon Limited Mobility in Two-Dimensional Semiconductors: Deformation Potential and Piezoelectric Scattering in Monolayer* MoS_2 *from First Principles*, Phys. Rev. B **87**, 235312 (2013).

[28] B. L. Gelmont and M. Shur, *Polar Optical-phonon Scattering in Three- and Two-dimensional Electron gases*, J. Appl. Phys. **77**, 657 (1995).

[29] X. Li, J. T. Mullen, Z. Jin, K. M. Borysenko, M. Buongiorno Nardelli, and K. W. Kim, *Intrinsic Electrical Transport Properties of Monolayer Silicene and* MoS_2 *from First Principles*, Phys. Rev. B **87**, 115418 (2013).

[30] S. Kim, A. Konar, W.-S. Hwang, J. H. Lee, J. Lee, J. Yang, C. Jung, H. Kim, J.-B. Yoo, J.-Y. Choi *et al.*, *High-Mobility and Low-Power Thin-Film Transistors Based on Multilayer* MoS_2 *Crystals*, Nat. Commun. **3**, 1011 (2012).

[31] R. Fivaz and E. Mooser, *Electron-Phonon Interaction in Semiconducting Layer Structures*, Phys. Rev. **136**, A833 (1964).

[32] R. Fivaz and E. Mooser, *Mobility of Charge Carriers in Semiconducting Layer Structures*, Phys. Rev. **163**, 743 (1967).

[33] P. Boguslawski and J. Mycielski, *Is the Deformation Potential in Semiconductors Screened by Free Carriers?* J. Phys. C **10**, 2413 (1977).

[34] P. Boguslawski, *Screening of the Deformation Potential by Free Electrons in the Multivally Conduction Band*, J. Phys. C **10**, L417 (1977).

[35] K.-A. N. Duerloo, M. T. Ong, and E. J. Reed, *Intrinsic Piezoelectricity in Two-Dimensional Materials*, J. Phys. Chem. Lett. **3**, 2871 (2012).

[36] S. Q. Wang and G. D. Mahan, *Electron Scattering from Surface Excitations*, Phys. Rev. B **6**, 4517 (1972).

[37] V. Perebeinos and P. Avouris, *Inelastic Scattering and Current Saturation in Graphene*, Phys. Rev. B **81**, 195442 (2010).

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Two-Dimensional Heterojunction Interlayer Tunneling Field Effect Transistors (Thin-TFETs)

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ABSTRACT Layered 2-D crystals embrace unique features of atomically thin bodies, dangling bond free interfaces, and step-like 2-D density of states. To exploit these features for the design of a steep slope transistor, we propose a Two-dimensional heterojunction interlayer tunneling field effect transistor (Thin-TFET), where a steep subthreshold swing (SS) of ~14 mV/dec and a high on-current of ~300 μA/μm are estimated theoretically. The SS is ultimately limited by the density of states broadening at the band edges and the on-current density is estimated based on the interlayer charge transfer time measured in recent experimental studies. To minimize supply voltage V_{DD} while simultaneously maximizing on currents, Thin-TFETs are best realized in heterostructures with near broken gap energy band alignment. Using the $WSe_2/SnSe_2$ stacked-monolayer heterostructure, a model material system with desired properties for Thin-TFETs, the performance of both *n*-type and *p*-type Thin-TFETs is theoretically evaluated. Nonideal effects such as a nonuniform van der Waals gap thickness between the two 2-D semiconductors and finite total access resistance are also studied. Finally, we present a benchmark study for digital applications, showing the Thin-TFETs may outperform CMOS and III–V TFETs in term of both switching speed and energy consumption at low-supply voltages.

INDEX TERMS Tunnel FET, 2-D crystals, transport model, steep slope, subthreshold swing (SS), layered materials, benchmarking.

I. INTRODUCTION

Tunnel Field Effect Transistors (FETs) are perceived as promising electronic switches that may enable scaling the supply voltage V_{DD} down to 0.5 V or lower by reducing the subthreshold swing (SS) below 60 mV/dec at room temperature.

To date, numerous Tunnel FETs have been demonstrated, among which heterostructures with near broken gap band alignment are favored in order to achieve sub-60 mV/dec SS and high on currents simultaneously [1]. Tunnel FETs also require a very strong gate control over the channel region to obtain sub-60 mV/dec SS values; this in turn demands ultra-thin body or nanowire structures, where size induced quantization enlarges the bandgap and impedes the realization of near broken gap alignment [2]–[4]. Layered 2D crystals, such as monolayers of transition metal dichalcogenides (TMD) MX_2 (e.g., M = Mo, W; X = S, Se, Te) and other metal chalcogenides MX_x (e.g., M = Ga, Sn; X = O, S, Se) offer a native thickness of about 0.6 nm with a variety of bandgaps and band-alignments [4], [5]. Furthermore, 2D crystals possess a sharp turn on of density of states at the band edges and have no surface dangling bonds thus potentially enabling a low interfacial density of state, which are highly desired for achieving a sharp SS [6]. Recent experimental results show that the band alignment in stacked-monolayer 2D crystal heterostructures can be tuned by an external electric field perpendicular to the heterojunction plane [7] and the charge transfer in stacked-monolayer 2D

crystal heterojunctions is reasonably fast [8]. In such a context, we propose the Two-dimensional Heterojunction Interlayer Tunneling FET (Thin-TFET) based on a vertical arrangement of 2D layered materials. In particular, we discuss both *n*-type and *p*-type Thin-TFETs employing a promising material system of 2H-WSe_2 and 1T-$SnSe_2$. Our simulations suggest that very competitive SS values and a high on-current can be achieved in the Thin-TFETs. Along with the low intrinsic gate-to-drain and gate-to-source capacitances in comparison to CMOS and p-i-n III-V TFETs benchmarked in Section III-D, the Thin-TFETs enable fast switching and low energy consumption. The effect of a non-uniform van der Waals gap thickness and the external source and drain total access resistance are also discussed. At the end of the paper, we will also share some insights on the experimental realization of Thin-TFETs derived from the ongoing investigations in our laboratory.

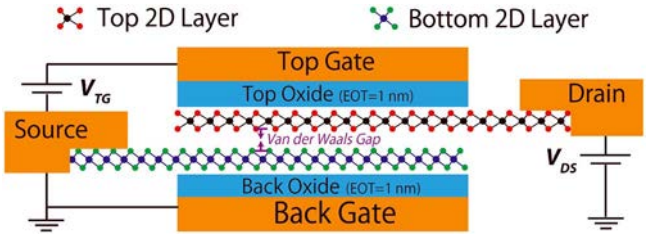

FIGURE 1. Schematic device cross section of a Thin-TFET.

II. DEVICE STRUCTURE AND MODELING APPROACH

The Thin-TFET device structure is shown in Fig. 1, where the bottom and top 2D semiconductors act as the source and the drain respectively. A van der Waals gap separates the top and bottom 2D semiconductors and the thickness of the van der Waals gap is defined as the distance from the center of the chalcogenide atom in the top 2D layer to the center of the nearest chalcogenide atom in the bottom 2D layer (see Fig. 1). The device working principle can be explained as follows: take the *p*-type Thin-TFET as the example, when the conduction band edge of the bottom 2D semiconductor E_{CB} is higher than the valence band edge of the top 2D semiconductor E_{VT} (see Fig. 2), tunneling from the bottom layer is inhibited and the device is nominally off. When a negative top gate voltage pulls E_{VT} above E_{CB} (see Fig. 3(a)), a tunneling window is opened thus current can flow.

To calculate the band alignment between E_{CB} and E_{VT} along the direction perpendicular to the 2D semiconductors we first use Gauss's law and write [9]

$$\begin{aligned} C_{TOX}V_{TOX} - C_{vdW}V_{vdW} &= e(p_T - n_T + N_T) \\ C_{BOX}V_{BOX} + C_{vdW}V_{vdW} &= e(p_B - n_B + N_B) \end{aligned} \quad (1)$$

where e is the magnitude of an electron charge, $C_{T(B)OX}$ is the capacitance per unit area of top (back) oxide, and C_{vdW} is the capacitance per unit area of the van der Waals gap. $V_{T(B)OX}$ and V_{vdW} are the corresponding potential drops. $n(p)_{T(B)}$ is the electron (hole) density in the top (bottom) 2D semiconductor layer, and N_T, N_B are the net chemical doping concentrations (donor minus acceptor) in the layers, which are set to zero in this work. The potential drops can be written in terms of the top gate V_{TG}, back gate V_{BG}, and drain-source voltage V_{DS} (which sets the split of the quasi-Fermi levels in the top and bottom semiconductor layers), and of the material properties as

$$\begin{aligned} eV_{vdW} &= eV_{DS} - e\phi_{p,B} - e\phi_{n,T} + E_{GB} + \chi_{2D,B} - \chi_{2D,T} \\ eV_{TOX} &= eV_{TG} + e\phi_{n,T} - eV_{DS} + \chi_{2D,T} - e\Phi_{M,T} \\ eV_{BOX} &= eV_{BG} - e\phi_{p,B} + E_{GB} + \chi_{2D,B} + e\Phi_{M,B} \end{aligned} \quad (2)$$

where we define $e\phi_{n,T(B)}=E_{CT(B)}-E_{FT(B)}$ and $e\phi_{p,T(B)}=E_{FT(B)}-E_{VT(B)}$, E_{GB} is the energy gap in the bottom 2D semiconductor and $E_{FT(B)}$ is the Fermi level in the top and bottom layers, $\chi_{2D,T(B)}$ is the electron affinity of the top (bottom) 2D semiconductor, and $\Phi_{M,T(B)}$ is the metal workfunction of the top (back) gate (see Fig. 2).

Using the effective mass approximation and assuming that the majority carriers of the two 2D semiconductors are at thermodynamic equilibrium with their Fermi levels [10], the carrier densities can be written as

$$n(p) = \frac{g_v m_c^* \left(m_v^*\right) k_B T}{\pi \hbar^2} \ln\left[\exp\left(-\frac{q\phi_{n,T}(\phi_{p,B})}{k_B T}\right) + 1\right] \quad (3)$$

where g_v is the valley degeneracy and $m_c^*(m_v^*)$ is the conduction (valence) band effective mass, and the rest of the parameters assume their common meanings.

By inserting Eqs. 2 and 3 in Eq. 1 we obtain two equations determining $\phi_{n,T}$, $\phi_{p,B}$ and thus the band alignment.

We calculate the tunneling current by using the transfer-Hamiltonian method [11], which was also recently revisited for resonant tunneling graphene transistors [12], [13]. We here summarize the basic equations; a more thorough discussion can be found in our earlier work [9]. The tunneling current density, J_T, is expressed as [9]:

$$\begin{aligned} J_T = {} & \frac{g_v e\,|M_{B0}|^2 A}{4\pi^3\hbar} \mathrm{e}^{-2\kappa T_{vdW}} \\ & \times \int_{\mathbf{k}_T}\int_{\mathbf{k}_B} d\mathbf{k}_T\, d\mathbf{k}_B\, S_F(q)\, S_E(E_B - E_T)\,(f_B - f_T) \end{aligned} \quad (4)$$

where κ is the decay constant of the wave-function in the van der Waals gap [12], [13], T_{vdW} is the thickness of the van der Waals gap, $\mathbf{k}_{T(B)}$, $E_{T(B)}$ and $f_{T(B)}$ are the wave-vector, the energy and Fermi occupation function in the top (bottom) 2D semiconductor and M_{B0} is the tunneling matrix element [9], which is a property of the material system and is further discussed in Section III. Equation 4 assumes that in the tunneling process electrons interact with a random scattering potential, whose spectrum is taken as $S_F(q) = \pi L_C^2/(1+\mathbf{q}^2 L_C^2/2)^{3/2}$, where $q=|\mathbf{k}_T-\mathbf{k}_B|$ and L_C is the correlation length. The scattering relaxes the momentum conservation, i.e., allowing tunneling for $\mathbf{k}_B \neq \mathbf{k}_T$. A similar $S_F(q)$ has been used to analyze the resonance linewidth in graphene tunneling transistors [13]. The S_F(q) may be representative of different scattering mechanisms that are discussed

in [9] and [13]. The energy broadening in the 2D semiconductors is described by $S_E(E)=\exp(-E^2/\sigma^2)/(\sqrt{\pi}\sigma^2)$, where σ is the energy broadening parameter [9].

Finally, after discussing the intrinsic device performance, the contact resistance is included in our model by self-consistently calculating the tunnel current density and the voltage drop on the total access resistance. The effect of the lateral resistance in the intrinsic Thin-TFET has been discussed in our prior work [14]. The key finding is that: when the tunnel current is sufficiently low ($\sim$1 μA/μm in the sub-threshold region), the tunnel junction resistance associated with the vertical current flow is much higher than the lateral resistance of the 2D semiconductor source and drain layers; as a result, the current distribution across the junction is rather uniform laterally in the sub-threshold region.

III. SIMULATION RESULTS AND DISCUSSIONS

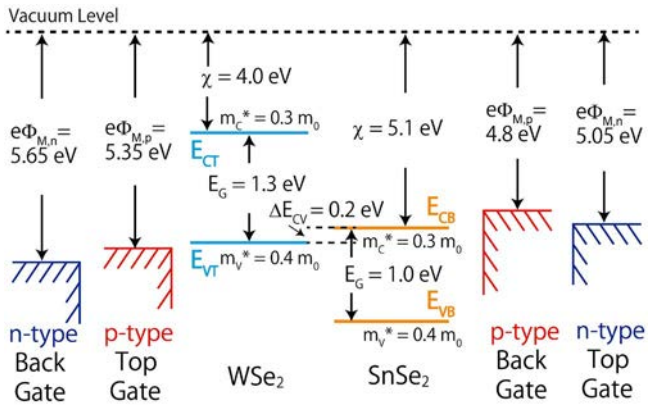

FIGURE 2. An example to realize both *n*-type and *p*-type Thin-TFETs using one pair of 2-D semiconductors (2H-WSe_2 and 1T-$SnSe_2$) with near broken gap band alignment. For the *n*-type Thin-TFET, $SnSe_2$ is the top (i.e., drain) 2-D layer and WSe_2 is the bottom (i.e., source) 2-D layer, along with the top and back gate labeled as *n*-type in blue. While for the *p*-type Thin-TFET, WSe_2 is the top (i.e., drain) 2-D layer and $SnSe_2$ is the bottom (i.e., source) 2-D layer, along with the top and back gate labeled as *p*-type in red; band gaps, electron affinities, effective masses are shown for WSe_2 and $SnSe_2$. The *n*-type and *p*-type metal work functions are tuned to give symmetric threshold voltages for the *n*-type and *p*-type Thin-TFETs.

A. MATERIAL SYSTEM AND N-TYPE & P-TYPE THIN-TFETS

Out of various 2D semiconductors studied by density function theory calculations [5] and experimental efforts, we chose the trigonal prismatic coordination monolayer (2H) WSe_2 and the octahedral coordination (CdI_2 crystal structure) monolayer (1T) $SnSe_2$ (see Fig. 2). $WSe_2/SnSe_2$ stacked-monolayer heterojunction can potentially form a near broken band alignment, which reduces the voltage drop in the van der Waals gap in the on-state condition [1]. Since there is no experimental band alignment reported for *monolayer* WSe_2 and $SnSe_2$, the band alignment of the $WSe_2/SnSe_2$ system used in this work are based on the existing experimental results of *multilayer* WSe_2 and $SnSe_2$ [15]–[17], while their approximated effective masses are based on the DFT results of monolayer WSe_2 and $SnSe_2$ [5] (see Fig. 2).

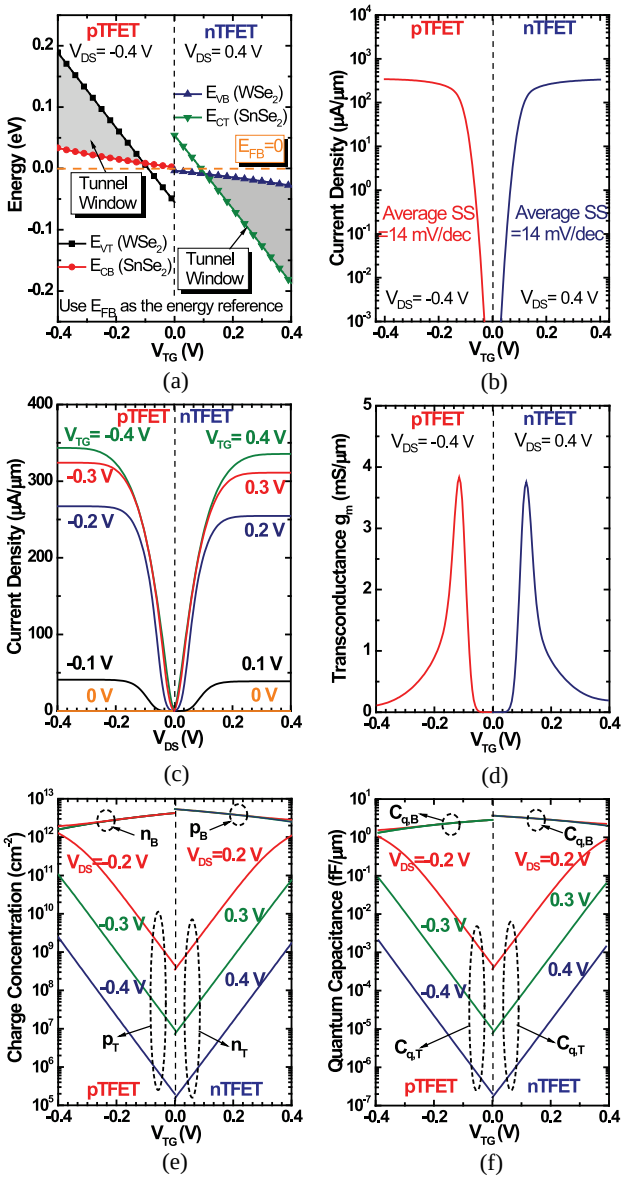

FIGURE 3. For the *n*-type and *p*-type Thin-TFETs shown in Fig. 2. (a) Band alignment versus V_{TG}. (b) Current density versus V_{TG}, the average SS is calculated from 10^{-3} μA/μm to 10 μA/μm. (c) Current density versus V_{DS} at various V_{TG}. (d) Transconductance versus V_{TG}. (e) Carrier concentration in the top and bottom 2-D layers versus V_{TG} at various V_{DS}. (f) Quantum capacitances of the top and bottom 2-D layers versus V_{TG} at various V_{DS}.

Following the complex band method [18], we assume the effective barrier height E_B of the van der Waals gap is 1 eV and the electron mass in the van der Waals gap is the free electron mass m_0, thus the decay constant is $\kappa = \sqrt{2m_0E_B/\hbar} = 5.12\ \text{nm}^{-1}$. In our model, we set the scattering correlation length L_C in $S_F(q)$ to L_C=10 nm, which is also consistent with the value employed in [13]; the energy broadening σ is set to be 10 meV. M_{B0} in Eq. 4 is directly related to the interlayer charge transfer time τ across the van der Waals gap, which can be written as [19]

$$\tau^{-1} = \frac{2\pi}{\hbar}\rho|M_{B0}|^2 e^{-2\kappa T_{vdW}} S_F(q) \qquad (5)$$

where $\rho=g_v m^*/\pi\hbar^2$ is the density of states (DOS). As can be seen from Eq. 5 and the expression of the scattering potential spectrum $S_F(q)$ (given after Eq. 4), due to scattering in our model, τ increases with increasing q, which is the magnitude of the wave-vector difference across the van der Waals gap defined as $q=|\mathbf{k}_T-\mathbf{k}_B|$. In a recent experiment, a charge transfer time of 25 fs has been observed across the van der Waals gap between a stacked-monolayer MoS_2/WS_2 heterostructure, which, according to Eq. 5, gives us M_{B0} ~0.02 eV when q=0. We recognize that the charge transfer time might be different for different 2D heterojunctions, nevertheless, this experimentally determined charge transfer time is a reasonable value to use for the first pass estimate. Thus, we choose M_{B0}=0.02 eV in all following simulations.

Throughout this work, the gate length is set to be 15 nm, the back gate and source are grounded. An effective oxide thickness (EOT) of 1 nm is used for both the top and back oxide, which gives a top (back) oxide capacitance C_{TG} (C_{BG}) of 0.518 fF/μm. The thickness of the van der Waals gap is set to 3.5 Å, unless specified otherwise. We assume the relative dielectric constant of the van der Waals gap is 1.0, therefore the van der Waals gap capacitance C_{vdW} is 0.38 fF/μm. The external total access resistances are considered after the intrinsic device performance is discussed first (Figs. 3 and 4).

The example material systems for *n*-type and *p*-type Thin-TFETs based on the stacked-monolayer WSe_2 and $SnSe_2$ are shown in Fig. 2. The metal work functions are tuned to obtain a symmetric threshold voltage for the *n*-type and the *p*-type Thin-TFET. Fig. 3(a) shows the band alignment versus V_{TG}. V_{TG} can effectively control the vertical band alignment in the device by controlling primarily the band edge of the top (i.e., drain) layer while having a weak effect on the band edge of the bottom (i.e., source) layer, so that a tunneling window is modulated. Fig. 3(b) shows I_D versus V_{TG} transfer curves with very compelling average SS of ~14 mV/dec averaged from 10^{-3} μA/μm to 10 μA/μm. The I_D versus V_{DS} family curves are shown in Fig. 3(c). I_D saturates for V_{DS} when V_{DS}>~0.2 V. The superlinear onset is also observed and the so called V_{DS} threshold voltage increases at lower V_{TG} [20]. A peak transconductances of ~4 mS/μm is observed around V_{TG}=0.12 V (Fig. 3(d)), which are much larger than ~0.8 mS/μm reported peak transconductances of 10 nm Fin-FET [21]. In Fig. 3(e), the top gate changes the carrier concentrations of the top 2D semiconductor much faster than of the bottom 2D semiconductor under different V_{DS}. The ability to efficiently change a hole (electron) concentration in the top 2D semiconductor while keeping a high electron (hole) concentration in the bottom 2D semiconductor is vital to achieve good electrostatics control of these Thin-TFETs. The quantum capacitance associated with the top and bottom semiconductor layers can be expressed as Eq. 6:

$$C_{Q,T(B)} = -\left[\frac{e\partial p_{T(B)}}{\partial \phi_{p,T(B)}} + \frac{e\partial n_{T(B)}}{\partial \phi_{n,T(B)}}\right] \quad (6)$$

The quantum capacitances are plotted in Fig. 3(f) under various bias conditions.

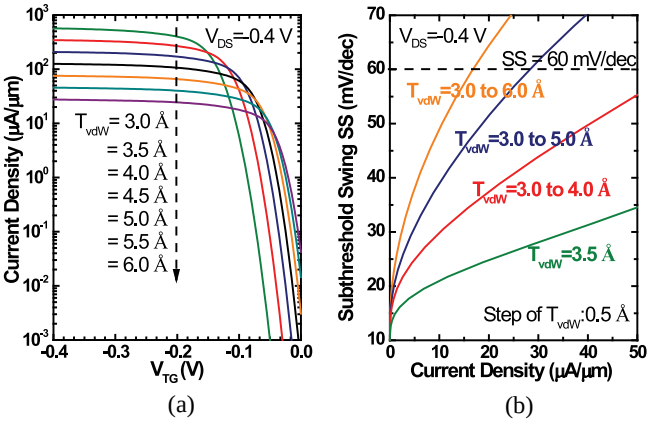

FIGURE 4. Effect of van der Waals gap thickness variation on a *p*-type Thin-TFET. (a) Tunnel current density versus V_{TG} for different van der Waals gap thicknesses T_{vdW}. (b) Differential SS versus current density assuming an evenly distributed van der Waals gap thickness T_{vdW} in the specified range.

B. EFFECTS OF NONUNIFORM VAN DER WAALS GAP THICKNESS AND ACCESS RESISTANCE

Due to the nature of van der Waals bonds, the van der Waals gap thickness is subject to intercalation of atoms/ions, interlayer rotational misalignment between 2D layers etc. For instance, in bilayer mechanically stacked Molybdenum Disulfide (MoS_2) with an interlayer twist, a maximum variation of 0.59 Å [22] was experimentally verified in the van der Waals gap thickness [22]. Surface roughening due to ripples in 2D crystals or roughness of the underlying substrates can also introduce van der Waals gap variations [23]. Meanwhile, tunneling probability is very sensitive to the tunneling distance, namely the van der Waals gap thickness in a Thin-TFET, which makes it important to investigate effects of a non-uniform van der Waals thickness. First, the Thin-TFET I-V curves are calculated by varying the van der Waals gap thickness T_{vdW} from 3.0 Å to 6.0 Å and a step of 0.5 Å (which is roughly half of the Se covalent radius [24]). The results are shown in Fig. 4(a) for a *p*-type Thin-TFET: the on current density decreases and the threshold voltage moves towards 0 when increasing the T_{vdW}. We note that, as long as the T_{vdW} is uniform, the SS remains as steep as ~14 mV/dec. However, for a non-uniform T_{vdW}, SS will degrade. To estimate its impact, an evenly distributed T_{vdW} over several ranges is used in the calculated differential SS shown in Fig. 4(b). For example, for a 2D heterojunction with an evenly distributed T_{vdW} from 3.0 Å to 5.0 Å and a step of 0.5 Å, we take the corresponding I_D-V_{TG} curve for each T_{vdW} (i.e., 3.0 Å, 3.5 Å, 4.0 Å, 4.5 Å, and 5.0 Å) shown in Fig. 4(a) and average them over the T_{vdW} range to obtain the overall I_D-V_{TG} curve for the calculation of SS. Fig. 4(b) shows that up to 1 Å variation in T_{vdW} is tolerable, resulting in a sub-60 mV/dec SS over a decent current window (up to 50 μA/μm). Depending on how Thin-TFETs are

fabricated, the T_{vdW} non-uniformity may have different distributions. Our first look at its impact in this work highlights the importance to precisely control T_{vdW}.

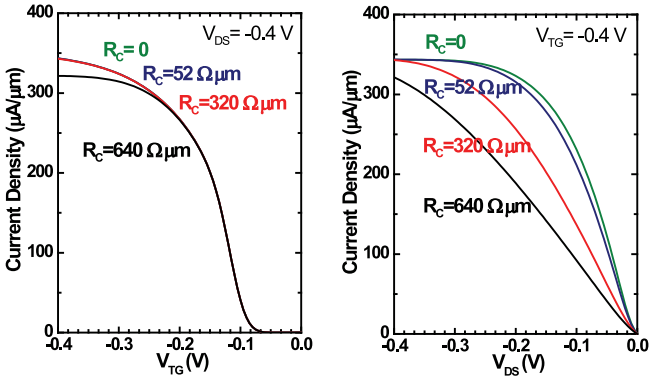

FIGURE 5. Effect of total access resistance on a *p*-type Thin-TFET. (a) I_D versus V_{TG}. (b) I_D versus V_{DS} with various total access resistance R_C values.

A finite total access resistance has a critical impact on ultrascaled transistors. To date, how to minimize the total access resistance in 2D crystal based device still remains an open question. In Fig. 5, we show its effects on Thin-TFET by assuming several values for the total access resistance R_C. At a sufficiently high $|V_{DS}|$ of 0.4 V, maximum I_D is almost the same for a R_C of up to 320 $\Omega\mu$m; a higher R_C decreases maximum I_D appreciably. Understandably, a lower R_C is necessary for a lower V_{DD}. In an ideal 2D conductor, the quantum limit of the total access resistance is inversely proportional to the square root of the carrier concentration; e.g., $\sim$52 $\Omega\mu$m for a carrier concentration of 10^{13} cm^{-2} [25]. Thus the access region of 2D semiconductors can be degenerately doped to minimize R_C.

C. CAPACITANCE EVALUATION

The gate-to-drain and gate-to-source capacitances (i.e., C_{GD}, C_{GS}) can be readily calculated from the capacitance network shown in Fig. 6.

The quantum capacitances $C_{Q,T(B)}$ of the top (bottom) 2D semiconductor are defined in Eq. 6 and indicated as the red non-linear capacitances in Fig. 6. First we define C_S as:

$$1/C_S \equiv 1/C_{vdW} + 1/(C_{Q,B} + C_{BG}) \tag{7}$$

Then, C_{GD} and C_{GS} can be written as Eqs. 8:

$$C_{GS} = \frac{C_{TG}C_S}{C_{TG} + C_{Q,T} + C_S}$$
$$C_{GD} = \frac{C_{TG}C_{Q,T}}{C_{TG} + C_{Q,T} + C_S} \tag{8}$$

Due to the symmetry in these *p*-type and *n*-type Thin-TFETs as well as the similar hole and electron effective mass in these 2D crystals, we expect similar C-V characteristics for the *p*-type and *n*-type Thin-TFETs. In Fig. 7 we plot the calculated C-V curves for the *p*-type Thin-TFETs shown in

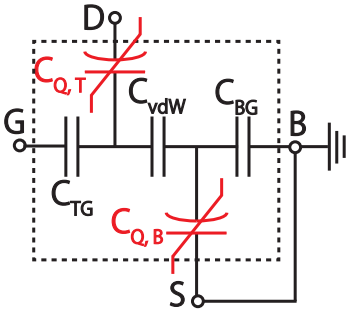

FIGURE 6. Capacitance network model of the Thin-TFET.

Fig. 2. In the linear region of the I_D-V_{DS} family of curves, C_{GD} is significant, where the drain is coupled with the top gate to modulate the tunnel current. From the linear region to the saturation region, C_{GD} drops to be near zero while C_{GS} increases to its maximum. What is worthy noting is that the magnitude of a Thin-TFET capacitance is smaller than CMOS and III-V TFET benchmarked in Section III-D for a given gate oxide EOT thus capacitances, which stem from the serially connected capacitance components as shown in Fig. 6. The capacitance model is useful for implementing the Thin-TFET into circuit simulations.

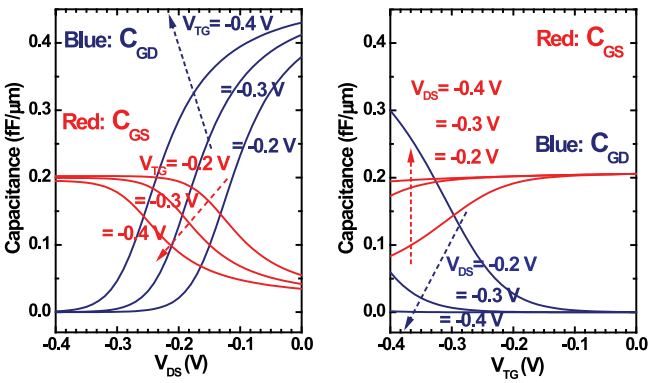

FIGURE 7. For the *p*-type Thin-TFET. (a) C_{GD} and C_{GS} versus V_{DS} at $V_{TG} = -0.2, -0.3, -0.4$ V. (b) C_{GD} and C_{GS} versus V_{TG} at $V_{DS} = -0.2, -0.3, -0.4$ V.

D. BENCHMARKING

The Semiconductor Research Corporation (SRC) Nanoelectronic Research Initiative (NRI) has supported research on beyond CMOS devices as reported by Bernstein *et al.* [26] As part of the initiative, the projected performance of the beyond-CMOS devices and the CMOS of the same technology node was compared, i.e., benchmarked. The benchmarking activity has continued by Nikonov and Young [27], [28]. Thin-TFET being proposed by us primarily under the support of SRC STARnet, we participated in the recent benchmarking using the Nikonov and Young (N&Y) methodology.

The N&Y methodology uses basic device performance parameters such as operating voltage ($V_{DD} = |V_{DS}|$), saturation current (I_{Dsat}), and average gate capacitance ($C_{G,avg}$),

to project logic switching energy and delay. The change of the net charge under the gate ($\Delta Q=q\Delta n_s$) when V_{TG} switches from 0 to V_{DD} is the sum of the change of the net charge in the top 2D semiconductor and the bottom 2D semiconductor. The average gate capacitance ($C_{G,avg}$) is defined as $\Delta Q/V_{DD}$. Here we take the *p*-type Thin-TFET as an example, I_{Dsat} and $C_{G,avg}$ are provided in Table 1 for a few V_{DD} values of 0.2, 0.3, and 0.4 V and a few total access resistance R_C values of 52 and 320 $\Omega\mu$m. The device parameters for High Performance (HP) CMOS, Low Power (LP) CMOS, InAs Homojunction TFET (HomJTFET) and InAs/GaSb Heterojunction TFET (HetJTFET) are taken from Ref. [28] and we use the same geometrical parameters for all the devices as shown in Table 1, while neglecting the contact capacitance.

The intrinsic switching delay t_{int} and the intrinsic switching energy E_{int} are calculated by [28]:

$$t_{int} = \frac{C_{G,avg}V_{DD}}{I_{Dsat}}$$
$$E_{int} = C_{G,avg}WV_{DD}^2 \quad (9)$$

In Fig. 8, we plot the projected values of t_{int} and E_{int} of the devices listed in Table 1.

TABLE 1. Benchmarking parameters.

Parameters for Thin-TFETs with various V_{DD} and R_C						
V_{DD} (V)	0.2		0.3		0.4	
R_C ($\Omega\mu$m)	52	320	52	320	52	320
I_{Dsat} (μA/μm)	263	233	325	317	349	348
ΔQ (fC/μm^2)	2.34	2.80	3.33	3.72	4.30	4.47
$\Delta n_s \times 10^{12}$(/cm^{-2})	1.46	1.75	2.08	2.32	2.69	2.79
$C_{G,avg}$ (fF/μm)	0.175	0.210	0.167	0.186	0.161	0.168
Parameters for HP/LP CMOS and HetJ/HomJ TFET [28]						
	V_{DD} (V)		I_{Dsat} (μA/μm)		$C_{G,avg}$ (fF/μm)	
HP CMOS	0.73		1805		1.29	
LP CMOS	0.3		2		1.29	
HetJTFET	0.4		500		1.04	
HomJTFET	0.2		25		1.04	
Geometrical Parameters for Benchmarking						
Half-pitch (F) (nm)	EOT (nm) (nm)		Gate Length (L) (nm)		Gate Width (W) (nm)	
15	1		15		60	

As far as the intrinsic switching energy-delay product is concerned, the Thin-TFET shows distinct energy consumption and performance advantages. For instance, Thin-TFET operation at a V_{DD} as low as 0.2 V is fast because its current is still significantly high. The most distinguishing feature of a Thin-TFET is its low intrinsic capacitance in comparison to the other devices. This advantage will be less significant when device parasitics become dominant in completed circuits.

It is observed that the Thin-TFET intrinsic switching energy-delay product moves toward the desired corner when decreasing V_{DD} from 0.4 V to 0.2 V. This is an unusual but favorable behavior for ultrascaled switches. In the case of 15 nm CMOS, I_D is roughly proportional to V_{DD}. While in the ON state of Thin-TFET, I_D has much weaker dependence on V_{TG} (see Fig. 5(a)) than CMOS, thus V_{DD} to I_D ratio actually decreases when scaling down V_{DD} from 0.4 V to 0.2 V.

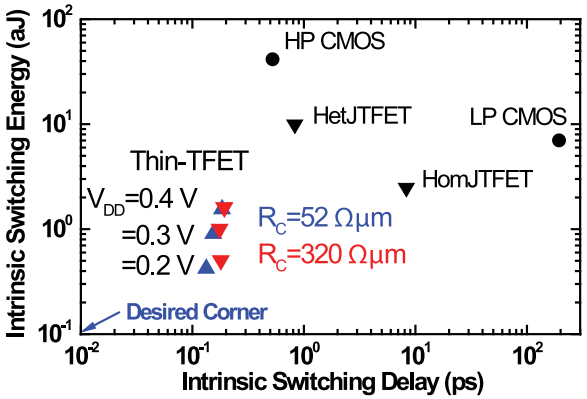

FIGURE 8. Intrinsic switching energy and delay for HP CMOS, LP CMOS, HetJTFET, HomJTFET, and Thin-TFETs with V_{DD} = 0.2, 0.3, 0.4 V, and R_C = 52, 320 $\Omega\mu$m.

Therefore, given that $C_{G,avg}$ stays roughly the same (increasing slightly with decreasing V_{DD}), the intrinsic switching time t_{int} slightly decreases when decreasing V_{DD}.

E. EXPERIMENTAL INSIGHTS

Since our proposal of Thin-TFET in 2012 [29] that is derived from our III-V TFET design [1], several key challenges have been identified along our pursuit in experimental demonstration of Thin-TFETs [30]. The foremost is the scarcity of electronic-grade layered materials and knowledge of their properties, in particular, the semiconductor heterojunctions with near broken gap alignment. The reasonably well-characterized material properties in the literature are largely based on bulk layered materials. An exponentially growing number of publications in the recent years on monolayer and few-layer materials are mainly theoretical calculations or based on exfoliation of naturally occurring crystals or synthesized by chemical vapor transport, which typically contains a few atomic percent of defects (impurities, vacancies etc). Both chemical vapor deposition and molecular beam epitaxy [31] are actively pursued by the community to grow electronic grade layered materials.

Besides lack of high quality layered materials and heterojunctions, the fabrication development of Thin-TFET is also challenging. It inherits all the fundamental fabrication challenges of a TFET including doping profile, alignment especially gate registry, gate dielectrics, ohmic contacts. Atomic layer deposition has been improved over years to achieve good quality gate dielectrics on 2D crystals [32]. Using 2D dielectrics such as hexagonal boron nitride as the gate dielectrics has also been pursued [33]. Third, low resistance ohmic contacts to 2D crystal are vital to device performance. Various techniques such as external chemical doping [34], internal chemical doping [35], electrostatic doping such as ion doping [36] and phase-engineering from the semiconductor phase to the metallic phase of a 2D crystal [37], have been implemented to reduce the contact resistances. Furthermore, Thin-TFETs demand true precision layer number control since the properties of nearly all

layered materials critically depend on the layer number when the layer number is in the range of 1-3 nm.

IV. CONCLUSION

A new tunnel transistor, Thin-TFET, has been proposed and a model material system identified. Simulations based on the transfer Hamiltonian method suggest that Thin-TFETs can achieve desired sub-threshold swing (SS) and high on-current. A uniform van der Waals gap thickness and low total access resistance are vital to optimize the Thin-TFET performance. The benchmark study shows Thin-TFETs may have distinct advantages over CMOS and III-V TFETs in term of both performance and energy consumption at low supply voltages.

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REFERENCES

[1] G. Zhou *et al.*, "Novel gate-recessed vertical InAs/GaSb TFETs with record high I_{ON} of 180 μA/μm at V_{DS} = 0.5 V," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, 2012, pp. 32–36.

[2] S. Brocard, M. Pala, and D. Esseni, "Design options for heterojunction tunnel FETs with high on current and steep sub-V_T slope," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, 2012, pp. 5.4.1–5.4.4.

[3] Y. Lu *et al.*, "Performance of AlGaSb/InAs TFETs with gate electric field and tunneling direction aligned," *IEEE Electron Device Lett.*, vol. 33, no. 5, pp. 655–657, May 2012.

[4] D. Jena, "Tunneling transistors based on graphene and 2-D crystals," *Proc. IEEE*, vol. 101, no. 7, pp. 1585–1602, Jul. 2013.

[5] C. Gong *et al.*, "Band alignment of two-dimensional transition metal dichalcogenides: Application in tunnel field effect transistors," *Appl. Phys. Lett.*, vol. 103, no. 5, Jul. 2013, Art. ID 053513.

[6] S. Agarwal and E. Yablonovitch, "Using dimensionality to achieve a sharp tunneling FET (TFET) turn-on," in *Proc. 69th Annu. Device Res. Conf. (DRC)*, Santa Barbara, CA, USA, 2011, pp. 199–200.

[7] P. Rivera *et al.*, "Observation of long-lived interlayer excitons in monolayer $MoSe_2$-WSe_2 heterostructures," *Nat. Commun.*, 2014. [Online]. Available: http://arxiv.org/abs/1403.4985

[8] X. Hong *et al.*, "Ultrafast charge transfer in atomically thin MoS2/WS2 heterostructures," *Nat. Nanotechnol.*, vol. 9, no. 9, pp. 682–686, 2014. [Online]. Available: http://dx.doi.org/10.1038/nnano.2014.167

[9] M. Li, D. Esseni, G. Snider, D. Jena, and H. G. Xing, "Single particle transport in two-dimensional heterojunction interlayer tunneling field effect transistor," *J. Appl. Phys.*, vol. 115, no. 7, 2014, Art. ID 074508.

[10] D. Esseni, P. Palestri, and L. Selmi, *Nanoscale MOS Transistors: Semi-Classical Transport and Applications*. New York, NY, USA: Cambridge Univ. Press, 2011.

[11] J. Bardeen, "Tunnelling from a many-particle point of view," *Phys. Rev. Lett.*, vol. 6, pp. 57–59, Jan. 1961.

[12] R. M. Feenstra, D. Jena, and G. Gu, "Single-particle tunneling in doped graphene-insulator-graphene junctions," *J. Appl. Phys.*, vol. 111, no. 4, 2012, Art. ID 043711.

[13] L. Britnell *et al.*, "Resonant tunnelling and negative differential conductance in graphene transistors," *Nat. Commun.*, vol. 4, Apr. 2013, Art. ID 1794.

[14] M. O. Li, D. Esseni, D. Jena, and H. G. Xing, "Lateral transport in two-dimensional heterojunction interlayer tunneling field effect transistor (Thin-TFET)," in *Proc. 72nd Annu. Device Res. Conf. (DRC)*, Santa Barbara, CA, USA, 2014, pp. 17–18.

[15] R. Schlaf, C. Pettenkofer, and W. Jaegermann, "Band lineup of a SnS_2/$SnSe_2$/SnS_2 semiconductor quantum well structure prepared by van der Waals epitaxy," *J. Appl. Phys.*, vol. 85, no. 9, pp. 6550–6556, 1999.

[16] R. Schlaf, O. Lang, C. Pettenkofer, and W. Jaegermann, "Band lineup of layered semiconductor heterointerfaces prepared by van der Waals epitaxy: Charge transfer correction term for the electron affinity rule," *J. Appl. Phys.*, vol. 85, no. 5, pp. 2732–2753, 1999.

[17] L. Upadhyayula, J. Loferski, A. Wold, W. Giriat, and R. Kershaw, "Semiconducting properties of single crystals of n- and p-type tungsten diselenide (WSe_2)," *J. Appl. Phys.*, vol. 39, no. 10, pp. 4736–4740, 1968.

[18] C. Sergio, Q. Gao, and R. M. Feenstra, "Theory of graphene–insulator–graphene tunnel junctions," *J. Vac. Sci. Technol. B*, vol. 32, no. 4, 2014, Art. ID 04E101.

[19] K. T. Lam, G. Seol, and J. Guo, "Operating principles of vertical transistors based on monolayer two-dimensional semiconductor heterojunctions," *Appl. Phys. Lett.*, vol. 105, no. 1, 2014, Art. ID 013112.

[20] L. De Michielis, L. Lattanzio, and A.-M. Ionescu, "Understanding the superlinear onset of tunnel-FET output characteristic," *IEEE Electron Device Lett.*, vol. 33, no. 11, pp. 1523–1525, Nov. 2012.

[21] B. Yu *et al.*, "FinFET scaling to 10 nm gate length," in *Proc. Int. Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, 2002, pp. 251–254.

[22] A. M. van der Zande *et al.*, "Tailoring the electronic structure in bilayer molybdenum disulfide via interlayer twist," *Nano lett.*, vol. 14, no. 7, pp. 3869–3875, 2014.

[23] J. Brivio, D. T. L. Alexander, and A. Kis, "Ripples and layers in ultrathin MoS2 membranes," *Nano Lett.*, vol. 11, no. 12, pp. 5148–5153, 2011. [Online]. Available: http://dx.doi.org/10.1021/nl2022288

[24] W. M. Haynes, *CRC Handbook of Chemistry and Physics*. Boca Raton, FL, USA: CRC Press, 2012.

[25] D. Jena, K. Banerjee, and G. H. Xing, "2D crystal semiconductors: Intimate contacts," *Nat. Mater.*, vol. 13, no. 12, pp. 1076–1078, Dec. 2014. [Online]. Available: http://dx.doi.org/10.1038/nmat4121

[26] K. Bernstein, R. Cavin, W. Porod, A. Seabaugh, and J. Welser, "Device and architecture outlook for beyond CMOS switches," *Proc. IEEE*, vol. 98, no. 12, pp. 2169–2184, Dec. 2010.

[27] D. Nikonov and I. Young, "Uniform methodology for benchmarking beyond-CMOS logic devices," in *Proc. Int. Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, 2012, pp. 25.4.1–25.4.4.

[28] D. Nikonov and I. Young, "Overview of beyond-CMOS devices and a uniform methodology for their benchmarking," *Proc. IEEE*, vol. 101, no. 12, pp. 2498–2533, Dec. 2013.

[29] *The Center for Low Energy Systems Technology (LEAST) Proposal, University of Notre Dame, submitted to Semiconductor Research Corporation (SRC)*, 2012.

[30] S. Xiao, M. Li, A. Seabaugh, D. Jena, and H. Xing, "Vertical heterojunction of MoS2 and WSe2," in *Proc. 72nd Annu. Device Res. Conf. (DRC)*, Santa Barbara, CA, USA, 2014, pp. 169–170.

[31] S. Vishwanath *et al.*, "Molecular beam epitaxy of layered material superlattices and heterostructures," *Bull. Amer. Phys. Soc.*, vol. 59, no. 1, Mar. 2014.

[32] L. Cheng *et al.*, "Atomic layer deposition of a high-k dielectric on MoS_2 using trimethylaluminum and ozone," *ACS Appl. Mater. Interf.*, vol. 6, no. 15, pp. 11834–11838, 2014.

[33] T. Roy *et al.*, "Field-effect transistors built from all two-dimensional material components," *ACS Nano*, vol. 6, no. 8, pp. 6259–6264, 2014.

[34] H. Fang *et al.*, "High-performance single layered WSe_2 p-FETs with chemically doped contacts," *Nano Lett.*, vol. 12, no. 7, pp. 3788–3792, 2012.

[35] L. Yang *et al.*, "High-performance MoS_2 field-effect transistors enabled by chloride doping: Record low contact resistance (0.5 k$\Omega\cdot\mu$m) and record high drain current (460 μA/μm)," in *Proc. Symp. VLSI Technol. Dig. Tech. Papers*, Honolulu, HI, USA, 2014, pp. 1–2.

[36] H. Xu, E. Kinder, S. Fathipour, A. Seabaugh, and S. Fullerton-Shirey, "Reconfigurable ion doping in 2H-Mote2 field-effect transistors using PEO: CsClO4 electrolyte," in *Proc. 41st Int. Symp. Compd. Semicond. (ISCS)*, Montpellier, France, 2014.

[37] R. Kappera *et al.*, "Phase-engineered low-resistance contacts for ultrathin MoS_2 transistors," *Nat. Mater.*, vol. 13, no. 12, pp. 1128–1134, 2014. [Online]. Available: http://dx.doi.org/10.1038/nmat4080

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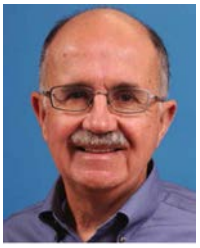

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Comparative study of chemically synthesized and exfoliated multilayer MoS_2 field-effect transistors

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We report the realization of field-effect transistors (FETs) made with chemically synthesized multilayer 2D crystal semiconductor MoS_2. Electrical properties such as the FET mobility, subthreshold swing, on/off ratio, and contact resistance of chemically synthesized (s-) MoS_2 are indistinguishable from that of mechanically exfoliated (x-) MoS_2, however, flat-band voltages are different, possibly due to polar chemical residues originating in the transfer process. Electron diffraction studies and Raman spectroscopy show the structural similarity of s-MoS_2 to x-MoS_2. This initial report on the behavior and properties of s-MoS_2 illustrates the feasibility of electronic devices using synthetic layered 2D crystal semiconductors. © *2013 American Institute of Physics*. [http://dx.doi.org/10.1063/1.4789975]

Two-dimensional (2D) crystal materials are receiving increased attention for future electronic devices. Short-channel effects in modern transistors originate from the 3-dimensional (3D) nature of the gate control; introduction of 2D materials in the channel significantly improves the gate electrostatics. Graphene is a true 2D material,[1] but its lack of a bandgap results in high leakage in the off-state in conventional transistor geometries. Alternative switching mechanisms[2–4] could enable electronic switching with high on-off current ratios. 2D transition-metal dichalcogenide (TMD) materials such as MoS_2,[5,6] WSe_2,[7,8] and WS_2 (Refs. 9 and 10) have drawn considerable attention due to the presence of a bandgap, in contrast to graphene. Prior studies of TMD multilayered materials have been conducted using exfoliated layers,[5–9] similar to the initial work with graphene.[1] The size and quality of naturally occurring exfoliated layered semiconductor materials are limited and uncontrollable, so it is important to develop synthetic techniques. Multilayer TMDs, like graphite, are excellent solid lubricating materials and have been chemically synthesized in large volumes, but have not been investigated intensively for transistors[11–13] except in very recent work.[14] Here, we report the fabrication and demonstration of chemically synthesized multilayer (s-) MoS_2 field-effect transistors (FETs) and compare the properties with exfoliated (x-) MoS_2 FETs.

s-MoS_2 flakes were grown by an iodine-transport method from previously synthesized MoS_2 (0.6 g) at 1060 K in an evacuated silica ampoule at a pressure of 10^{-3} Pa, and with temperature gradient of 6.8 K/cm. The volume concentration of iodine was 11 mg/cm^3. After 21 days of growth, the silica ampoule was slowly cooled to room temperature at a rate of 30 °C/h. The MoS_2 flakes were then dispersed by sonication in isopropyl alcohol (IPA) and transferred onto a 30 nm thick atomic-layer-deposited (ALD) Al_2O_3 dielectric on a $p+$ Si substrate held at 100 °C until dry. For comparison, x-MoS_2 flakes were released and transferred from bulk MoS_2 using scotch tape. The height of the MoS_2 flakes are in the range of 20–40 nm. Source and drain contacts were defined by electron beam lithography (EBL) using Ti/Au (5/100 nm) contacts. The devices were annealed at 300 °C for 3 h under Ar/H_2 flow to decrease the contact resistance. A schematic cross-sectional image of the back-gated (BG) MoS_2 device is shown in the inset of Fig. 1(a).

Figure 1(a) shows the measured drain current, I_D, per unit gate width, versus the back-gate-to-source voltage, V_{BG}, at room temperature for a multilayer s-MoS_2 channel at three drain biases. The gate modulation is $\sim 10^5$ and the gate leakage current is much lower (less than 1 pA/μm) than the drain current. This large gate modulation relative to graphene is attributed to the presence of a bandgap. The device shows clear *n*-type behavior indicating accumulation of electrons (*n*-type conductivity) for positive back-gate bias. The comparative transfer curves of x-MoS_2 FETs are also shown in Fig 1(a). s-MoS_2 and x-MoS_2 FETs show highly similar transfer characteristics. The extracted field-effect mobilities of both x-MoS_2 and s-MoS_2 FETs are $\sim$30 cm^2/V s at room temperature. The subthreshold swing (SS) of the x-MoS_2 FET is 200 mV/dec. and that of the s-MoS_2 FET is 190 mV/dec. The average values of the FET mobility of each type of both x-MoS_2 and s-MoS_2 are $\sim$15 cm^2/V s and the SS of those are $\sim$170 mV/dec. Another s-MoS_2 (W/L = 1/2 μm) FET is compared with x-MoS2 and electrical properties still work out to be similar.

The subthreshold swing is similar for the s-MoS_2 and x-MoS_2 FETs, but higher than the ideal Boltzmann limit of 60 mV/dec. The similar SS suggests that the interface charge leading to the higher subthreshold swing likely arises from

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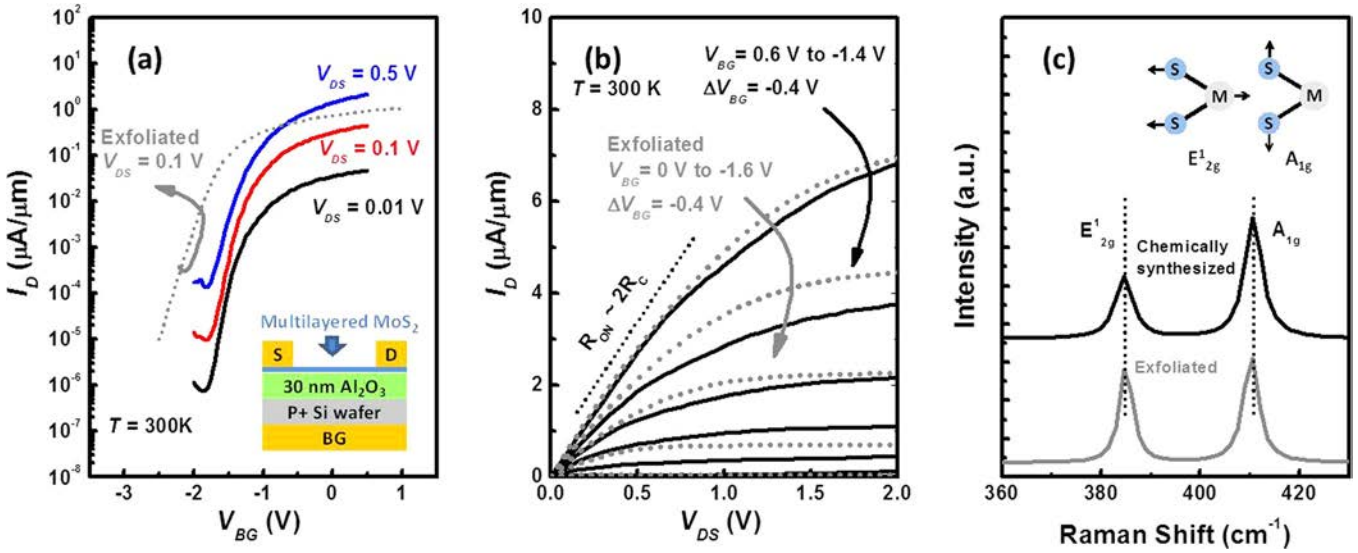

FIG. 1. Transport properties and Raman spectroscopy of FETs of s-MoS_2 with W/L = 1/2 μm and x-MoS_2 with W/L = 5/1.5 μm. (a) Drain current, I_D, per unit gate width vs. back-gate voltage, V_{BG}, of s-MoS_2 at various drain voltages, V_{DS}. The transfer curve of an x-MoS_2 is also shown for comparison, dotted line. (b) Common source transistor characteristics comparing s-MoS_2 (solid lines) and x-MoS_2 (dashed lines) FETs. (c) Raman spectra (λ_{exc} = 488 nm) of both s-MoS_2 and x-MoS_2 materials with a laser power of 1.5 mW and a spot size of 0.5-1 μm. The inset sketch shows the two primary vibrational modes in MoS_2 leading to the two peaks in the Raman spectrum.

traps in the Al_2O_3 dielectric, which are identical for the s-MoS_2 and x-MoS_2 FETs. The major difference between s-MoS_2 and x-MoS_2 FETs is in the threshold voltage. The flat-band voltage of the x-MoS_2 FETs is higher than that of s-MoS_2 by approximately 1 V. The possible reasons for this shift could be (a) different unintentional doping densities in s-MoS_2 and x-MoS_2, or (b) scotch tape residue-induced-charges possibly leading to a higher flat-band voltage for the x-MoS_2 compared to the s-MoS_2 FETs, which do not experience the tape exfoliation procedure. Identifying the precise reason for this threshold shift requires further work.

The family of I_D-V_{DS} curves at various V_{GS} in Fig. 1(b) shows typical transistor behavior including a linear increase of current at low V_{DS} and current saturation at high V_{DS}. The behavior shows desirable transistors attributes such as ohmic contacts, current saturation, and good gate electrostatic control. However, the current levels are in the μA/μm regime for micron long gate-lengths, which is low. The reason for the low current is a high contact resistance. The contact resistances of both s-MoS_2 and x-MoS_2 FETs in this work were extracted to be ~80 Ω mm at low V_{DS}. This value is comparable to the ~69 reported for exfoliated MoS_2 FETs.[6] This is an extremely high value, and currently holds back the performance of the FETs. The observation here is that s-MoS_2 and x-MoS_2 FETs have similar contact resistances, and are both high. A significant increase in the current drive of the FETs is expected if the contact resistance can be lowered to 1 Ω mm regime or lower, as is the case in Si and III–V FETs. The contact resistance can be lowered using a low work function metal like Sc.[15]

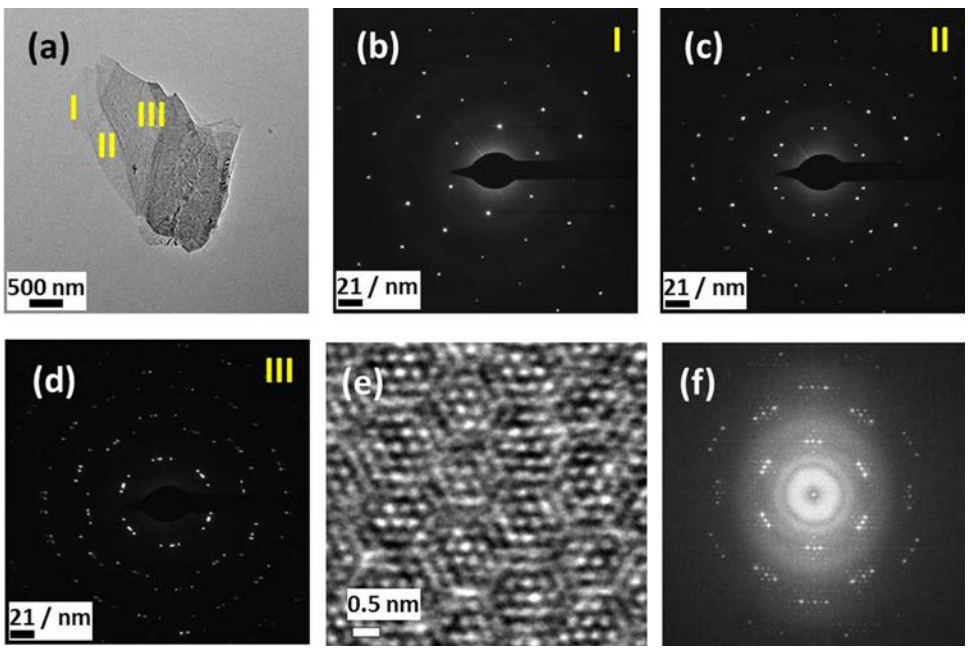

FIG. 2. (a) TEM of the s-MoS_2 multilayers. TEM electron diffraction patterns from (b) region I revealing the single crystal layer, (c) region II revealing the superposition of two single crystal layers with rotation, and (d) region III revealing the superposition of four single crystal layers with different rotations. The electron diffraction patterns reveal that the lattice parameter of s-MoS_2 is 0.32 nm. (e) An atomic-scale Moiré pattern of s-MoS_2 multilayers. (f) FFT from the image of (e), indicating three different crystal layers with different rotational angles.

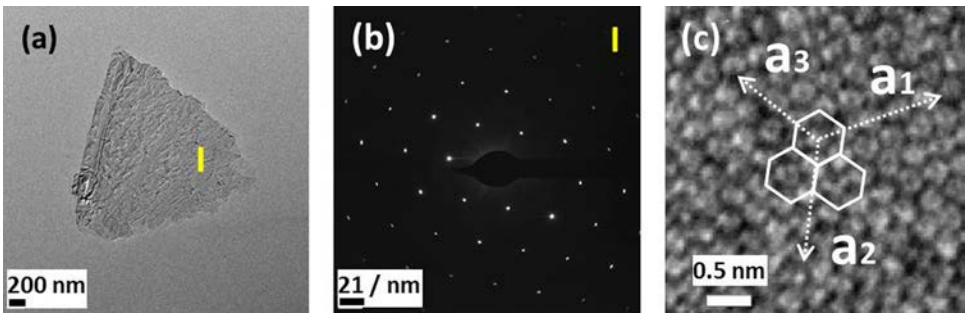

FIG. 3. (a) TEM of the x-MoS_2 multilayers. (b) Electron diffraction pattern from region I revealing the single crystal layer. (c) HR TEM image of region I. A lattice constant of 0.32 nm can be obtained from (b) and (c).

The measured Raman spectra shown in Fig. 1(c) at an excitation wavelength, λ_{exc}, of 488 nm are highly similar between s-MoS_2 and x-MoS_2 flakes. The spectrum exhibits two peaks: one in the $E_{2g}{}^1$ range, corresponding to in-plane vibrations at $\sim$385 cm^{-1}, and the other in the A_{1g} range corresponding to out-of-plane vibrations at $\sim$410 cm^{-1}. Since the Raman spectrum and transport properties are almost identical for s-MoS_2 and x-MoS_2, this confirms the overall similarity of chemically-synthesized and exfoliated MoS_2. In order to further investigate the atomic properties of s-MoS_2, transmission electron microscopy (TEM) was performed. The information obtained from s-MoS_2 is shown in Fig. 2 and compared with that of x-MoS_2 in Fig. 3.

Figure 2(a) shows the morphology of the s-MoS_2 on a TEM grid where a single crystal layer region (I), a superposition of two single crystal layer with rotation (II), and superposition of four single crystal layers with rotation (III) are clearly resolved. The corresponding TEM electron diffraction patterns are shown in Figs. 2(b)–2(d), respectively, showing the number of spots corresponding to the number of layers and the angular separation superimposed on the hexagonal lattice pattern. The electron diffraction patterns in Figs. 2(b)–2(d) reveal that s-MoS_2 flakes retain the crystal symmetry and lattice constant, $\sim$0.32 nm, when compared with that of x-MoS_2 in Fig. 3. A high-resolution (HR) TEM image is shown in Fig. 2(e) and its fast Fourier transform (FFT) is shown in Fig. 2(f). The FFT shows that the Moiré pattern in the image is due to three different crystal layers superimposed with different angles.

For comparison, the morphology of x-MoS_2 on the TEM grid and the electron diffraction pattern with a high-resolution TEM image are shown in Figs. 3(a)–3(c), respectively. The measurement confirms again a lattice parameter of x-MoS_2 of $\sim$0.32 nm which is identical to that of s-MoS_2 and that of bulk MoS_2.[16] The single-layer region is clearly resolved in the electron diffraction pattern, and the high-resolution atomic image clearly resolves the hexagonal crystal structure of single-layer MoS_2.

In summary, chemically synthesized MoS_2 transistors were fabricated and characterized, and compared with exfoliated MoS_2. The electronic and structural properties of chemically synthesized layers were found to be highly similar to exfoliated MoS_2. In particular, the transistor characteristics of s-MoS_2 were found to be almost identical to that of the x-MoS_2 in terms of FET mobility, subthreshold swing, on/off ratio, and contact resistance. TEM electron diffraction patterns and Raman measurements prove that the crystal symmetries and structural properties of s-MoS_2 are also identical to that of x-MoS_2. Though a number of issues need to be resolved before TMD crystals deliver high-performance transistors, this initial report shows that synthetic procedures can also realize high-quality channel material.

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[1]K. S. Novoselov, A. K. Geim, S. V. Morozov, D. Jiang, Y. Zhang, S. V. Dubonos, I. V. Grigorieva, and A. A. Firsov, Science **306**, 666 (2004).
[2]Q. Zhang, T. Fang, H. Xing, A. Seabaugh, and D. Jena, IEEE Electron Device Lett. **29**, 1344 (2008).
[3]R. M. Feenstra, D. Jena, and G. Gu, J. Appl. Phys. **111**, 043711 (2012).
[4]L. Britnell, R. V. Gorbachev, R. Jalil, B. D. Belle, F. Schedin, A. Mishchenko, T. Georgiou, M. I. Katsnelson, L. Eaves, S. V. Morozov, N. M. R. Peres, J. Leist, A. K. Geim, K. S. Novoselov, and L. A. Ponomarenko, Science **335**, 947 (2012).
[5]B. Radisavljevic, A. Radenovic, J. Brivio, V. Giacometti, and A. Kis, Nat. Nanotechnol. **6**, 147 (2011).
[6]S. Kim, A. Konar, W. S. Hwang, J. H. Lee, J. Lee, J. Yang, C. Jung, H. Kim, J. B. Yoo, J. Y. Choi, Y. W. Jin, S. Y. Lee, D. Jena, W. Choi, and K. Kim, Nat. Commun. **3**, 1011 (2012).
[7]V. Podzorov, M. E. Gershenson, Ch. Kloc, R. Zeis, and E. Bucher, Appl. Phys. Lett. **84**, 3301 (2004).
[8]H. Fang, S. Chuang, T. C. Chang, K. Takei, T. Takahashi, and A. Javey, Nano Lett. **12**, 3788 (2012).
[9]D. Braga, I. G. Lezama, H. Berger, and A. F. Morpurgo, Nano Lett. **12**, 5218 (2012).
[10]W. S. Hwang, M. Remskar, R. Yan, V. Protasenko, K. Tahy, S. D. Chae, P. Zhao, A. Konar, H. Xing, A. Seabaugh, and D. Jena, Appl. Phys. Lett. **101**, 013107 (2012).
[11]Y. Shi, W. Zhou, A.-Y. Lu, W. Fang, Y.-H. Lee, A. L. Hsu, S. M. Kim, K. K. Kim, H. Y. Yang, L.-J. Li, J.-C. Idrobo, and J. Kong, Nano Lett. **12**, 2784 (2012).
[12]Y.-H. Lee, X.-Q. Zhang, W. Zhang, M.-T. Chang, C.-T. Lin, K.-D. Chang, Y.-C. Yu, J. T.-W. Wang, C.-S. Chang, L.-J. Li, and T.-W. Lin, Adv. Mater. **24**, 2320 (2012).
[13]Y. Zhan, Z. Liu, S. Najmaei, P. M. Ajayan, and J. Lou, Small **8**, 966 (2012).
[14]H. Wang, L. Yu, Y.-H. Lee, W. Fang, A. Hsu, P. Herring, M. Chin, M. Dubey, J. Kong, and T. Palacios, in *IEEE International Electron Devices Meeting* (2012), p. 4.6.1.
[15]S. Das, H.-Y. Chen, A. V. Penumatcha, and J. Appenzeller, Nano Lett. **13**, 100 (2013).
[16]P. A. Young, J. Phys. D: Appl. Phys. **1**, 936 (1968).

Interband tunneling in two-dimensional crystal semiconductors

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Interband quantum tunneling of electrons in semiconductors is of intense recent interest as the underlying transport mechanism in tunneling field-effect transistors. Such transistors can potentially perform electronic switching with lower energy than their conventional counterparts. The recent emergence of two-dimensional (2D) semiconducting crystals provides an attractive material platform for realizing such devices. In this work, we derive an analytical expression for understanding tunneling current flow in single-layer 2D crystal semiconductors in the k-space. We apply the results to a range of 2D crystal semiconductors, and compare it with tunneling currents in three-dimensional semiconductors. We also discuss the implications for tunneling devices. © *2013 American Institute of Physics*. [http://dx.doi.org/10.1063/1.4799498]

Two-dimensional (2D) crystals of graphene were first isolated in 2004.[1] The unique electronic and optical properties of graphene have been extensively studied since then.[2] Electronic transistors have been proposed with graphene for ultra-low power switching.[3–5] These proposed devices either exploit the symmetric zero-bandgap Dirac-cone bandstructure of graphene or require the opening of energy bandgaps by quantum confinement. Soon after the isolation of graphene, *semiconducting* 2D crystals were reported.[6–8] 2D crystal semiconductors have been found in the transition metal dichalcogenide (TMD) material family, and the list is expected to expand in the future.[9] Taking advantage of an energy bandgap, ultrathin channels, and absence of broken bonds, conventional field-effect transistors (FETs) using 2D crystal semiconductors have shown high promise in initial investigations.[7,10]

A number of electronic switching devices have been proposed recently to address the power-dissipation problems of FETs.[11] Among the proposed devices, the tunneling FET (or TFET) has emerged as an attractive candidate. These devices take advantage of the potential of interband Zener-tunneling of electrons to beat the Boltzmann thermal limit of switching of 60 mV/decade. Initial experimental demonstrations show much promise.[12–14] The availability of 2D semiconducting crystals with bandgaps begs the question whether TFETs with attractive properties can be realized with them. Such 2D crystal TFETs, if realized, can take advantage of the ultrathin nature of the layers, and the absence of broken bonds to enable scaling of such devices to much smaller dimensions than three-dimensional (3D) crystal semiconductors. A critical metric for TFETs is the on-state current, which is limited by interband tunneling of electrons. To date, interband tunneling in purely 2D semiconducting crystal junctions has not received sufficient attention, certainly not to the extent it has for 3D semiconductor p-n junctions since Zener's[15] and Esaki's works.[16] In this work, we solve this problem. We derive an analytical expression for the tunneling current in 2D crystal semiconductors. The expression highlights the dependence of the tunneling current on the material parameters of the 2D crystal semiconductor, such as its bandgap and effective masses. We apply the results to a range of 2D crystals, and discuss the implications for device applications.

Consider the 2D crystal *p-i-n* junction shown schematically in Fig. 1(a) with ohmic contacts to the *p*- and *n*-doped regions. The contacts would form the source and drain contacts of the corresponding TFET. We do not address the experimental challenges of doping and electrostatic gating in this work and focus exclusively on evaluating the two-terminal tunneling current. Assume the doping in the *p*- and *n*-sides aligns the Fermi levels to the respective band-edges. Then, under no applied bias, $E_v^p = E_c^n$, and no net current flows across the junction. Here, E_v^p is the valence-band edge on the *p*-side and E_c^n is the conduction-band edge on the *n*-side. Under the application of a reverse bias voltage V, a finite energy window is created for electrons since $E_v^p - E_c^n = qV$. Within this energy window, electrons from the valence band can tunnel into the conduction band on the other side, as indicated in Fig. 1(b).

The electric current is obtained by summing the individual quantum-mechanical probability current contributions by each k-state electron, and multiplying it by q, the electron charge. The tunneling current is thus given by

$$I_T = q\frac{g_s g_v}{L_x}\sum_k v_g(k)(f_v - f_c)T_{wkb}, \tag{1}$$

where $g_s = 2$ is the spin degeneracy and g_v is the valley degeneracy for 2D crystal single layers. Single-layer TMD 2D crystals have been found to have a direct bandgap with two valleys at the K and K' points of the Brillouin zone similar to 2D graphene,[17] so we use $g_v = 2$. L_x is the macroscopic length along the electric field (which will cancel out), $v_g(k) = \hbar^{-1}\nabla E(k)$ is the group velocity of carriers in the band $E(k)$, f_v, f_c are the occupation functions of the valence and conduction bands, respectively, and T_{wkb} is the interband tunneling probability given by the Wentzel-Kramers-Brillouin (WKB) approximation. The sum is over all k-state electrons that are allowed to tunnel. We note here that the tunneling probability may be obtained by various means such as the Landau-Zener approach, Bardeen's transfer Hamiltonian, or direct numerical evaluation by integration over evanescent

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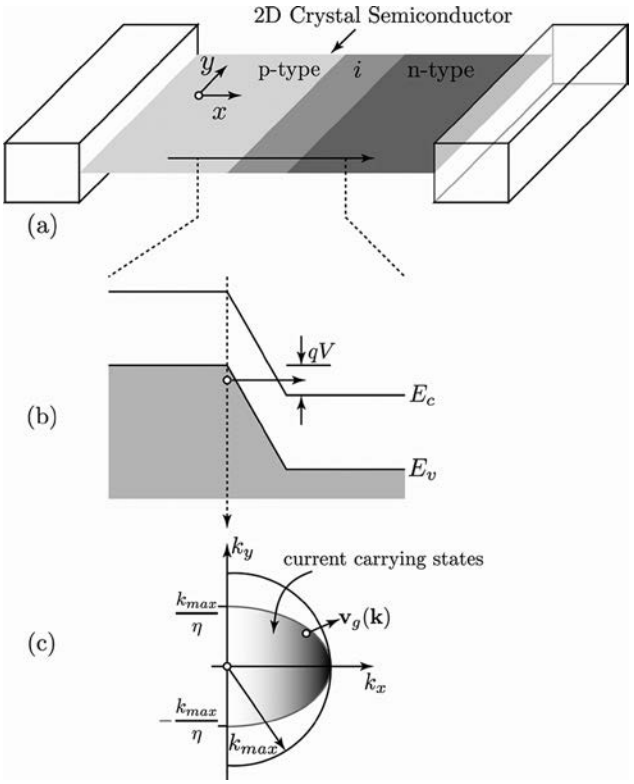

FIG. 1. Schematic depiction of a 2D crystal *p-i-n* junction (a), the energy band-diagram (b), and the **k**-space distribution of current densities (c). The **k**-states contributing to interband tunneling current and the group velocity are indicated.

k-states in the bandgap. Since the results from the analytical WKB approach are not vastly different from the alternate approaches, we use this approach.

The tunneling probability T_{wkb} is obtained by the WKB approximation in the following manner. For 2D crystals, electrons in the valence band of the *p*-side have a transverse kinetic energy $E_y = \hbar^2 k_y^2/2m_v^*$, where $\hbar k_y$ is the transverse quasi-momentum and m_v^* is the valence band effective mass. The WKB tunneling probability is then given by[18]

$$T_{WKB} = \exp\left[-\frac{4\sqrt{2m_R^*}(E_g + E_y)^{3/2}}{3q\hbar F}\right] \approx T_0 \exp\left[-\frac{E_y}{\bar{E}}\right], \quad (2)$$

where $T_0 = \exp[-4\sqrt{2m_R^*}E_g^{3/2}/3q\hbar F]$ is the tunneling probability of perpendicularly incident electrons, $\bar{E} = q\hbar F/2\sqrt{2m_R^* E_g}$, F is the (constant) electric field in the junction, and m_R^* is the reduced effective mass given by $m_R^* = m_c^* m_v^*/(m_c^* + m_v^*)$. m_v^*, m_c^* are the effective masses of electrons of the valence and conduction bands, respectively. The above expression is found to be consistent with experimental results.[18] Note that the tunneling probability of electrons is lowered *exponentially* with their transverse kinetic energy as a consequence of lateral momentum conservation in the tunneling process. We neglect phonon emission or absorption processes here. To evaluate the tunneling current, we attach this tunneling probability to each electronic *k*-state and sum it over all electrons incident on the tunneling barrier.

In Fig. 1, we concentrate on a particular 1D line as shown by the dashed line, at the *p-i* junction, which is the source side. Half of the electrons in the valence band in that line move to the right in the $+k_x$ direction, as indicated in the semi-circle in the *k*-space in Fig. 1(c). Since there are negligible electrons in the conduction band in that line, the current there must be carried by electrons in the valence band. Which of these right-going electrons are allowed to tunnel through the gap? In the absence of phonon scattering, tunneling is an elastic process. This enforces the energy conservation requirement

$$E_v^p - \frac{\hbar^2}{2m_v^*}(k_{xp}^2 + k_{yp}^2) = E_c^n + \frac{\hbar^2}{2m_c^*}(k_{xn}^2 + k_{yn}^2), \quad (3)$$

with the additional requirement that the lateral momentum be conserved, i.e., $k_{yp} = k_{yn} = k_y$. The energy and momentum conservation requirements thus lead to the relation

$$k_{xp}^2 + \frac{m_v^*}{m_R^*}k_y^2 = \frac{2m_v^* qV}{\hbar^2} - \frac{m_v^*}{m_c^*}k_{xn}^2. \quad (4)$$

Let us define $k_{\max}^2 = 2m_v^* qV/\hbar^2$ and $\eta^2 = m_v^*/m_R^*$. Note that $k_{\max}$, the radius of the semi-circle in the *k*-space shown in Fig. 1(c), is controlled by the applied voltage. Since there is an electric field in the *x*-direction, the momentum in that direction will not be conserved. For the electron to emerge on the right (*n*-)side, k_{xn} must be non-zero, and thus $k_{xn}^2 \geq 0$, which implies

$$k_{xp}^2 + \eta^2 k_y^2 \leq k_{\max}^2. \quad (5)$$

The above condition defines a restricted elliptical area A_T of the *k*-space semi-circle for electron states that are allowed to tunnel, as shown in Fig. 1(c). We can now evaluate the tunneling current for 2D semiconductor *p-i-n* junctions. In the expression for the tunneling current (Eq. (1)), the group velocity term is that of the valence band *k*-state $v_g(k) = \hbar k_x/m_v^*$. We skip the *p*-subscripts, since it is clear that the electrons tunnel from the valence band of the *p*-side. The expression for the tunneling current is then

$$I_T = q\frac{g_s g_v}{L_x}\sum_{(k_x,k_y)\in A_T}\frac{\hbar k_x}{m_v^*}(f_v - f_c)T_0 \exp\left[-\frac{\hbar^2 k_y^2}{2m_v^*\bar{E}}\right]. \quad (6)$$

The sum over *k*-states is converted into an integral via the standard recipe $\sum_k(\ldots) \rightarrow L_x L_y/(2\pi)^2 \times \int dk_x dk_y(\ldots)$. Due to the "filtering" brought about by the requirements of energy and momentum conservation (Eq. (5)), the *k*-space integral is evaluated over the restricted area A_T. The tunneling current *per unit width* or the *current density* is then given by

$$J_T^{2D} = \frac{I_T}{L_y} = \frac{qg_s g_v \hbar T_0}{(2\pi)^2 m_v^*}\int_{-k_{\max}/\eta}^{+k_{\max}/\eta} dk_y \times \exp\left[-\frac{\hbar^2 k_y^2}{2m_v^*\bar{E}}\right]\int_0^{\sqrt{k_{\max}^2 - \eta^2 k_y^2}} dk_x k_x (f_v - f_c). \quad (7)$$

Electrons incident normal to the junction have no transverse momentum, and carry most of the tunneling current. The

number of electron states allowed to tunnel reduces as their transverse directed momentum increases, as shown schematically in Fig. 1(c). The current carried by these states with transverse momentum is further damped by the $[-E_y/\bar{E}]$ factor, leading to further filtering and momentum collimation. The maximum tunneling current is carried by states closest to $(k_x, k_y) = (k_{\max}, 0)$ as indicated by the shading in the figure.

To evaluate the current, the integral in k-space should be evaluated. At $T \to 0\text{K}$, $f_v - f_c \approx 1$, for the energy window of current-carrying electrons. This relation remains an excellent approximation at room temperature. The interband tunneling current per unit width (μA/μm) in a 2D crystal p-i-n junction then evaluates to

$$J_T^{2D} = \frac{q^2}{h}\left(\frac{g_s g_v T_0}{2\pi}\right)\sqrt{\frac{2m_v^*\bar{E}}{\hbar^2}} \times \left[\sqrt{\pi}\left(V - \frac{V_0}{2}\right)\text{Erf}\left(\frac{\sqrt{V}}{\sqrt{V_0}}\right) + \sqrt{\frac{V}{V_0}}\exp\left(-\frac{V}{V_0}\right)\right], \tag{8}$$

where Erf[…] stands for the error function, and we have defined $V_0 = \eta^2\bar{E}/q$. Equation (8) is the central result of this work. The expression shows the dependences on various bandstructure and junction parameters explicitly. For small reverse bias voltages $V \ll V_0$, the tunneling current varies as $J_T^{2D} \sim V^{3/2}$ to leading order. This is consistent with a recent report investigating dimensionality effects on tunneling.[19] For larger voltages when $V \gg V_0$, Erf[…] $\to 1$, and we get a linear dependence of the tunneling current on the voltage

$$J_T^{2D} \approx \left[\frac{q^2}{h}\left(\frac{g_s g_v}{2\pi}\right)\sqrt{\frac{2\pi m_v^*}{\hbar^2}\cdot\frac{qhF}{\sqrt{8m_R^* E_g}}} \times T_0\right]V, \tag{9}$$

where the Landauer quantum of conductance is split off. The entire square root term is an effective wavevector with units of inverse length, leading to units of current per unit width. The corresponding current density for tunneling current in 3-dimensional semiconductors is given by $J_T^{3D} \approx \left[\frac{q^2}{h}\left(\frac{g_s g_v}{2\pi}\right)\left(\sqrt{\frac{2m_R^* E_g}{\hbar^2}}\frac{qF}{E_g}\right) \times T_0\right]V$ with units of current per unit area. The WKB term is similar for 2D and 3D crystals. The prefactor for 3D semiconductors goes as $\sim F\sqrt{m^*/E_g}$, whereas for 2D crystals, it goes as its square root $\sim\sqrt{F\sqrt{m^*/E_g}}$. In quasi-2D systems, multiple subbands may be involved in transport. Then, we sum the current from each subband with the respective band parameters. When the temperature T is high, the assumption $f_v - f_c \approx 1$ may no longer be suitable. In that case, the 2D tunneling current becomes

$$J_T^{2D} = \frac{q g_s g_v T_0 k_B T}{(2\pi)^2\hbar}\int_{-k_{\max}/\eta}^{+k_{\max}/\eta} \times \text{Ln}\left\{\frac{(e^{\beta(qV-\eta^2E_y)} + e^{-\beta E_y})(1+e^{\beta(qV-E_y)})}{(e^{\beta(qV-\eta^2E_y)} + e^{\beta(qV-E_y)})(1+e^{-\beta E_y})}\right\} \times \exp\left[-\frac{E_y}{\bar{E}}\right]dk_y, \tag{10}$$

where $\beta = 1/k_B T$ and k_B is the Boltzmann constant. We have not simplified this expression analytically, but the numerical evaluation is discussed. The interband tunneling current densities of various 2D crystals at $T = 4\,\text{K}$ and $300\,\text{K}$ are plotted as solid and dashed lines in Fig. 2(a), respectively. As is evident, the temperature dependence is rather weak. The material constants (bandgaps and effective masses) are obtained from Refs. 17 and 20. We note that the field F is determined by the choice of doping, bandgap, external dielectrics, and in the case of a 3-terminal TFET geometry, the gate voltage.

The tunneling current densities for MoS_2 and the family of TMDs are found to be low owing to their large bandgaps. For example, the current density approaches $\sim 0.1\ \mu\text{A}/\mu\text{m}$ for $MoTe_2$ at a high field of 4 MV/cm. The tunneling current density of 2D graphene can be higher (~few mA/μm), but it lacks a bandgap. For TFET applications, 2D crystals with smaller bandgaps are necessary for boosting the current. For example, tunneling currents for 2D crystals with bandgaps of 0.5 eV and 1.0 eV with corresponding lower effective masses

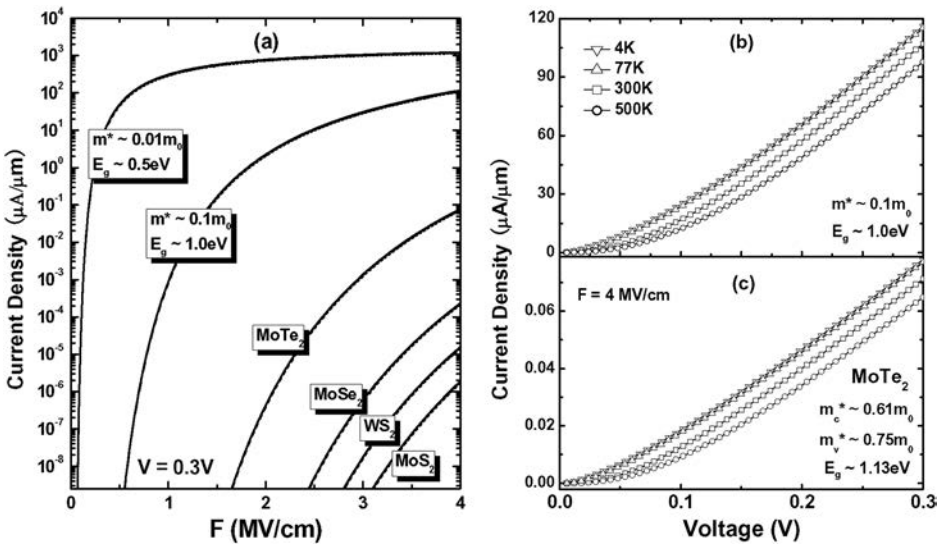

FIG. 2. (a) Interband tunneling current density for various 2D crystal semiconductors at a reverse bias of V = 0.3 V. The solid lines are at $T = 4\,\text{K}$, and the dashed lines at $T = 300\,\text{K}$, and the temperature dependence is weak. (b) Current-voltage curves at various temperatures at a junction field $F = 4$ MV/cm for a 2D crystal semiconductor with band parameters indicated. (c) Same as (b), but for the 2D crystal $MoTe_2$.

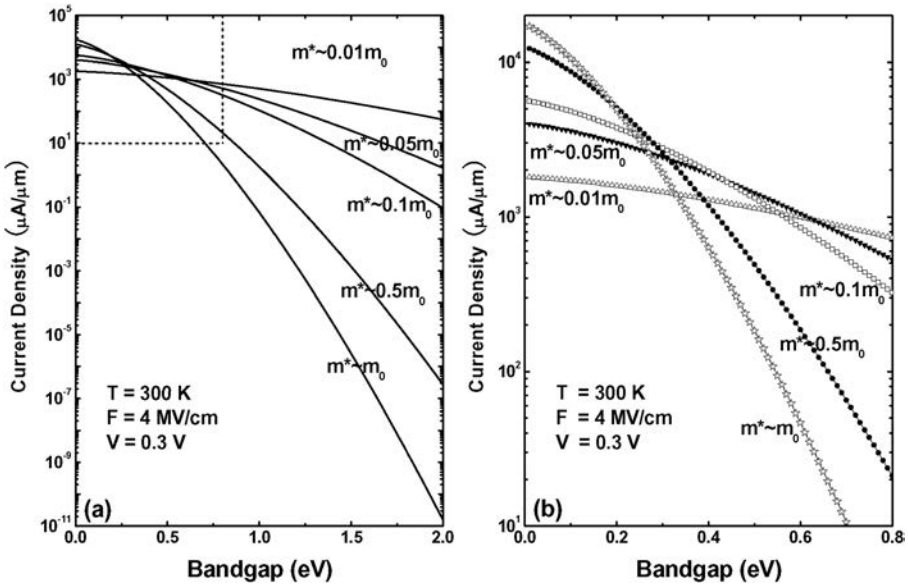

FIG. 3. (a) Interband tunneling currents for 2D crystal semiconductors as a function of the energy bandgap for various effective mass parameters. (b) The high current part of (a) zoomed in for more details.

are plotted in Fig. 2(a). The currents for such crystals exceed $\sim 100\ \mu A/\mu m$ at the highest junction fields, and thus can be attractive for high-performance TFET applications. Such small-bandgap materials could be intrinsic 2D crystals or derived from interaction-induced bandgap of Dirac-cone surface states in thin topological insulator materials.[21] Another possibility is in bilayer graphene, where breaking the layer symmetry by vertical electric fields opens a small bandgap.

The tunneling current of $MoTe_2$ and a 2D semiconductor crystal with $E_g = 1.0\,eV$ and $m^* = 0.1m_0$ (m_0 is free electron mass) as a function of the voltage at different temperatures is shown in Figs. 2(b) and 2(c). Note the $J_T^{2D} \sim V^{3/2}$ dependence at low voltages, the approximately linear relation $J_T^{2D} \sim V$ at high voltages, and the rather weak temperature dependence. Note that the current for the small effective mass 2D crystal is orders of magnitude higher than $MoTe_2$ in Figs. 2(b) and 2(c), even though their bandgaps are similar. Is this always true? Comparing the material parameters of Figures 2(b) and 2(c)), a natural question is the relative importance of effective masses and bandgaps. For III-V 3D semiconductors, the effective masses are proportional to the bandgaps, as would be expected from interband repulsive interaction from basic perturbation theory.[22] The equivalent picture is not clear yet for 2D semiconducting crystals. Therefore, we discuss all possibilities by treating the effective mass and bandgap as independent material parameters. Fig. 3 shows the interband tunneling currents in 2D crystals at a high junction field for various bandgaps, plotted for a range of effective masses.

As is evident from Fig. 3(a), there is a tradeoff in the choice of effective mass and bandgap for maximizing the tunneling current. Fig. 3(b) zooms in to highlight this crossover. For high-performance TFETs for digital switching applications, currents exceeding 100 $\mu A/\mu m$ are highly desirable. For 2D crystals semiconductors with bandgaps smaller than $\sim 0.3-0.4\,eV$, a choice of a *higher* effective mass will maximize the interband tunneling current, far exceeding typical transistor on-currents for high-performance switching. But for larger bandgaps, a *lower* effective mass is more desirable. It is essential that TFET devices *switch off*, which may be problematic for 2D crystals with very small bandgaps. For high-performance TFETs, 2D crystals with bandgaps in the ~ 0.6-$0.7\,eV$ range and effective masses of 0.1-$0.5m_0$ can thus be potentially very attractive.

On the other hand, there are various low-power applications of wider bandgap 2D crystals that do not require high on-currents, as long as they can beat the Boltzmann limit of 60 mV/decade. Such applications may include low-power sensors.[23] Other applications are expected to emerge as such devices become available. For such applications, the low tunneling currents of TMD 2D crystals might be actually turned into an advantage. We summarize this work by hoping that the analytical evaluation of tunneling currents in 2D crystals will be found useful for guiding the choice of the right materials for the specific applications. The analytic expression of the current vs. voltage can also form the backbone for compact modeling and design of 2D crystal TFETs when combined with the device electrostatics.

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[1]K. S. Novoselov, D. Jiang, F. Schedin, T. J. Booth, V. V. Khotkevich, S. V. Morozov, and A. K. Geim, Proc. Natl. Acad. Sci. U.S.A. **102**, 10451 (2005).
[2]K. S. Novoselov, V. I. Fal'ko, L. Colombo, P. R. Gellert, M. G. Schwab, and K. Kim, Nature **490**, 192 (2012).
[3]Q. Zhang, T. Fang, A. C. Seabaugh, H. G. Xing, and D. Jena, IEEE Electron Device Lett. **29**, 1344 (2008).
[4]S. K. Banerjee, L. F. Register, E. Tutuc, D. Reddy, and A. H. MacDonald, IEEE Electron Device Lett. **30**, 158 (2009).
[5]P. Zhao, R. M. Feenstra, G. Gu, and D. Jena, IEEE Trans. Electron Devices **60**, 951 (2013).
[6]A. Ayari, E. Cobas, O. Ogundadegbe, and M. S. Fuhrer, J. Appl. Phys. **101**, 014507 (2007).
[7]B. Radisavljevic, A. Radenovic, J. Brivio, V. Giacometti, and A. Kis, Nature Nano. **6**, 147 (2011).
[8]Q. H. Wang, K. Kalantar-Zadeh, A. Kis, J. N. Coleman, and M. S. Strano, Nature Nano. **7**, 699 (2012).
[9]C. Ataca, H. Şahin, and Ciraci, J. Phys. Chem. C **116**, 8983 (2012).
[10]S. Kim, A. Konar, W. S. Hwang, J. H. Lee, J. Lee, J. Yang, C. Jung, H. Kim, J. B. Yoo, J. Y. Choi *et al.*, Nat. Commun. **3**, 1011 (2012).
[11]T. N. Theis and P. M. Solomon, Proc. IEEE **98**, 2005 (2010).

[12]G. Zhou, R. Li, T. Vasen, M. Qi, S. Chae, Y. Lu, Q. Zhang, H. Zhu, J.-M. Kuo, T. Kosel *et al*., IEEE IEDM Tech. Dig. **2012**, 32.6.1–32.6.4.
[13]G. Dewey, B. Chu-Kung, J. Boardman, J. M. Fastenau, J. Kavalieros, R. Kotlyar, W. K. Liu, D. Lubyshev, M. Metz, N. Mukherjee *et al*., IEEE IEDM Tech. Dig. **2011**, 33.6.1–33.6.4.
[14]J. Appenzeller, Y. M. Lin, J. Knoch, and Ph. Avouris, Phys. Rev. Lett. **93**, 196805 (2004).
[15]C. Zener, Proc. R. Soc. London, Ser. A **145**, 523 (1934).
[16]L. Esaki, Phys. Rev. **109**, 603 (1958).
[17]H. Peelaers and C. G. Van de Walle, Phys. Rev. B **86**, 241401(R) (2012).
[18]A. C. Seabaugh and Q. Zhang, Proc. IEEE **98**, 2095 (2010).
[19]S. Agarwal and E. Yablonovitch, preprint arXiv:1109.0096.
[20]L. Liu, S. B. Kumar, and J. Guo, IEEE Trans. Electron Devices **58**, 3042 (2011).
[21]J. Chang, L. F. Register, and S. K. Banerjee, IEEE DRC Tech. Digest **2012**, 31–32.
[22]H. Kroemer, *Quantum Mechanics For Engineering, Materials Science, and Applied Physics* (Prentice Hall, New Jersey, 1994).
[23]D. Sarkar and K. Banerjee, Appl. Phys. Lett. **100**, 143108 (2012); D. Sarkar, H. Gossner, W. Hansch, and K. Banerjee, Appl. Phys. Lett. **102**, 023110 (2013).

devices. Furthermore, separation and recombination of photoinduced electron–hole pairs at a heterojunction interface are primary mechanisms governing the operation of solar cells, photodetectors and light-emitting devices. Both Gong and collaborators and Duan and colleagues managed to electrically address the lateral heterojunctions and perform transport measurements to investigate their electrical behaviour. Even though the contacted structures are not predefined in shape and thus are far from optimized devices, rectifying behaviour across the junctions was clearly observed, showing a concrete proof of principle. Both groups also showed clear evidence of the photoresponse of the heterojunctions in their transport measurements. Similarly, charge recombination at the lateral heterojunctions has been characterized in the three studies by means of photoluminescence imaging, which revealed an enhanced emission response at the interline between the materials in all cases. Mastering the in-plane growth of different TMDs down to the single-atom level could enable the synthesis of laterally quantum-confined systems, with promise of exciting physics. Also, this could open up opportunities for a wide range of devices, including complementary logic circuits, high-frequency devices and photodetectors.

Whereas the lateral junctions show scope for miniaturization, the development of larger scale vertical heterojunctions will prove crucial for commercial applications in light emission and light harvesting. Large-scale photodiodes using vapour-phase-grown MoS_2 transferred to silicon wafers have been realized already[12]. They have shown impressive performance and have also revealed that using vapour-phase-grown materials allows tuning of the optical response of the device. However, the *in situ* growth of a bilayer heterojunction could largely improve on this, in particular by engineering pristine interfaces that are not achievable by transfer techniques. Further optimization of the CVD process will lead to better control over the grown structures and over the interface quality. Future work will extend these approaches towards other material sets with arresting discoveries yet to come. ❐

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References

1. Geim, A. K. *Science* **324,** 1530–1534 (2009).
2. Novoselov, K. S. *et al. Nature* **438,** 197–200 (2005).
3. Geim, A. K. & Grigorieva, I. V. *Nature* **499,** 419–425 (2013).
4. Radisavljevic, B. & Kis, A. *Nature Mater.* **12,** 815–820 (2013).
5. Fang, H. *et al. Proc. Natl Acad. Sci. USA* **111,** 6198–6202 (2014).
6. Pospischil, A., Furchi, M. M. & Mueller, T. *Nature Nanotech.* **9,** 257–261 (2014).
7. Roy, K. *et al. Solid State Commun.* **175–176,** 35–42 (2013).
8. Gong, Y. *et al. Nature Mater.* **13,** 1135–1142 (2014).
9. Huang, C. *et al. Nature Mater.* **13,** 1096–1101 (2014).
10. Duan, X. *et al. Nature Nanotech.* http://dx.doi.org./10.1038/nnano.2014.222 (2014).
11. Miyata, Y. *et al. Appl. Phys. Express* **5,** 085102 (2012).
12. Yim, C. *et al. Sci. Rep.* **4,** 5458–5462 (2014).

2D CRYSTAL SEMICONDUCTORS

Intimate contacts

High electrical contact resistance had stalled the promised performance of two-dimensional layered devices. Low-resistance metal–semiconductor contacts are now obtained by interfacing semiconducting MoS_2 layers with the metallic phase of this material.

Debdeep Jena, Kaustav Banerjee and Grace Huili Xing

Transistors and lasers made of semiconductor materials power the information age by providing the building blocks for electronic switching, amplification and photonic communication. The electronic and photonic properties of the semiconductor play a primary role in determining the performance of such devices, yet comparable importance resides in the way this material interfaces with the external metallic circuits. A high electrical resistance due to a high energy barrier — the Schottky barrier — encountered by the charge carriers moving through the metal–semiconductor contacts saps the energy efficiency, and significantly degrades the performance of the device.

Semiconductor researchers are excited about the potential of transition metal dichalcogenide (TMD) layered semiconductors. For device applications, the excitement is fuelled by the dream of improving device performance by using a semiconductor channel that is potentially one monolayer thick[1]. The first generation of field-effect transistors made from MoS_2 and related TMDs have shown promise, but trail the silicon and III–V semiconductor analogues significantly in performance. A high contact resistance is the root cause. Writing in *Nature Materials*, Rajesh Kappera and colleagues now report an unconventional method to address this problem head-on[2], based on the local conversion of MoS_2 semiconducting layers into a metal that lowers the barrier to the charges flowing in the external circuits.

The traditional method to lower the contact resistance between a metal and a semiconductor relies on an intermediate layer, usually a heavily doped semiconductor that helps charge carriers from the metal to be injected in the conduction and valence bands of the semiconductor. The metal is chosen based on its workfunction, so that it creates a low Schottky barrier height with the semiconductor contact region, whereas heavy doping reduces the thickness of the barrier, enabling a significant fraction of electrons to quantum mechanically tunnel through it. However, chemical doping has proven challenging with TMD semiconductors. In their work, Kappera *et al.* exploit the fact that MoS_2 exists in two crystalline phases: the 2H and 1T types, which differ in their stacking geometry. The 1T phase is obtained by twisting one set of the 2H Mo–S tetrahedron by a 60° rotation. The stable 2H structural phase has a semiconducting behaviour and is desired as the channel of the transistor. The 1T phase is structurally metastable, but can be stabilized if electrons are pumped into it — it then becomes metallic because of a half-filled *d*-orbital band. This electronic stabilization of the metallic 1T phase can be achieved by converting the 2H phase by various routes, for example by irradiation with an electron beam[3]. Kappera and

colleagues use a chemical technique, treating the MoS_2 with an organometallic solution containing *n*-butyl lithium. Lithium donates electrons to the 2H MoS_2 converting it into the 1T metallic phase. The chemical process achieves the phase transition selectively: covered areas are left semiconducting, and exposed areas become metallic, as confirmed by extensive chemical, structural and optical analytical characterization. When the solution is washed away, the 1T region is likely to attract immobile positive charges and remain stable. Such a semiconductor-to-metal phase-transition process can be amenable in a device fabrication environment.

The team then used this process to make batches of transistors — the test structures have 1T metallic MoS_2 source–drain contact areas interfacing gold pads, and the control structures have direct gold–2H semiconductor MoS_2 contacts. In the test devices, the contact resistance was found to drop from ~1–10 kΩ μm to ~0.2–0.3 kΩ μm. As a result, the performance of the 1T contact transistors was significantly superior across the board of metrics: the drive current, the sharpness of switching and the gain all improved. The researchers also find that the 1T contact transistors have a much higher reproducibility and yield compared with their 2H contact counterparts. The transistor characteristics are also less sensitive to the workfunction of the metals, suggesting that the contacts' performance now mainly depends on the 1T/2H interface. Other TMD semiconductors have similar metallic counterparts, implying the same principle potentially applies to them.

The phase-engineering approach to making low-resistance ohmic contacts to TMD semiconductor materials is thus an exciting advance that addresses a critical problem holding back potential applications. As with any new study, a list of unknowns remains to be worked out. By itself, the 1T metallic phase of MoS_2 is negatively charged — meaning the identity of the neutralizing positive charges that are presumably immobile remains to be determined and controlled. The nature of the 1T–2H metal–semiconductor junction, the band alignments, and a potential way to contact the valence band for hole conduction need to be developed. The barrier between the metal and 1T phase due to weak van der Waals bonding needs to be investigated. The lateral diffusion of the organometallic lithium solution under the covered areas can convert part of the desired 2H MoS_2 channel into the 1T phase, whereas the chemical conversion of the exposed regions is not perfect; alternative ways to seal the channel during the chemical

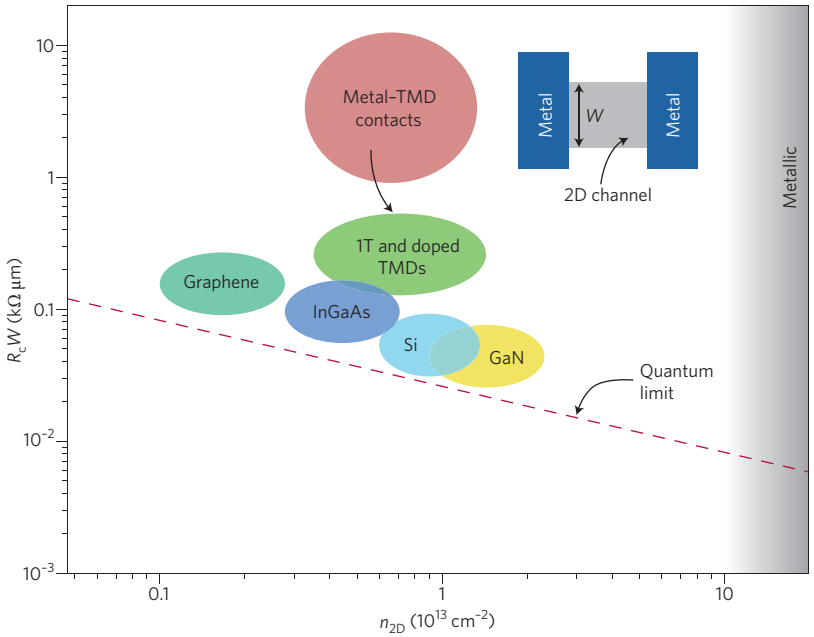

Figure 1 | Contact resistances for various semiconductor materials against the quantum limits for crystalline materials. Using a 1T metallic phase to interface MoS_2 with metals shifts the performance of TMD-based transistors closer to the quantum limit predicted by Landauer and Sharvin. The inset shows a typical transistor configuration.

treatment and achieve complete phase transformation in the contact areas need to be investigated. And as the researchers state, the stability of the 1T contacts under high-performance operation — for example when large currents are driven through the transistor — remains to be elucidated.

But how low a contact resistance can one obtain? This problem in various forms has been studied for more than a century. James Clerk Maxwell calculated[4] the classical 'contact' resistance between two regions of conductivity σ separated by an insulator and connected by a conducting circular constriction of diameter D to be $R_c \sim 1/(\sigma D)$. In the 1950s and 1960s, Landauer[5] and Sharvin[6] gave the problem a quantum facelift. Their work predicted a minimum contact resistance value for $R_c \sim h/(2e^2M)$, where h is Planck's constant, e is the electron charge and M is the number of electron modes whose wavelength fit the narrow conductor. In other words, even for a perfect conducting channel with no scattering, only those electron modes that fit are allowed access into the channel, the rest are reflected. As the sheet density of electrons $n_{2D} = k_F^2/2\pi$ in a two-dimensional (2D) channel increases, the wavelength $\lambda = 2\pi/k_F$ of the energetic electrons riding the Fermi surface shortens, and more modes $M \sim k_F W$ fit, where W is the width of the channel and k_F is the Fermi wavevector. The minimum contact resistance is then $R_cW \sim h/2e^2k_F \sim 0.026/\sqrt{n_{2D}}$ kΩ μm, which depends strongly on the electron sheet density (in units of 10^{13} cm^{-2}) in the semiconductor channel, and weakly on some aspects of the bandstructure[7]. This is the quantum limit of the contact resistance for crystalline semiconductors, shown by the dashed line in Fig. 1.

This limit has been experimentally verified in atomic break-junctions and in split-gate quantum point contacts, in which a quantized conductance was observed[8]. The highest-performance semiconductor transistors are also grazing this lower limit[9], as shown in Fig. 1. The latest achievements for TMDs represent a major leap, yet there is still room for improvement. Recently, a joint academic and industry research team has reported a method to chemically dope MoS_2 and have achieved low-resistance contacts and high-performance transistors[10]. Their technique is similar to the traditional method used for semiconductors, and the contact resistance values are similar to the 1T contacts discussed here. Both these old and new approaches mark important steps towards harnessing the innate potential of 2D crystal semiconductors. More importantly, metal–semiconductor junctions can enable a host of unanticipated physical phenomena exploiting the *d*-orbital pedigree of conduction electrons in TMDs. ❐

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References
1. Radisavlejevic, B., Radenovic, A., Brivio, J., Giacometti, V. & Kis, A. *Nature Nanotech.* **6,** 147–150 (2011).
2. Kappera, R. *et al. Nature Mater.* **13,** 1128–1134 (2014).
3. Lin, Y.-C., Dumnenco, D. O., Huang, Y.-S. & Suenaga, K. *Nature Nanotech.* **9,** 391–396 (2014).
4. Maxwell, J. C. *A Treatise on Electricity and Magnetism* (Clarendon, 1904).
5. Landauer, R. *IBM J. Res. Dev.* **1,** 223–231 (1957).
6. Sharvin, Y. V. *Sov. Phys. JETP* **21,** 655–656 (1965).
7. Datta, S., Assad, F. & Lundstrom, M. S. *Superlattices Microstructures* **23,** 771–780 (1998).
8. Van Wees, B. *et al. Phys. Rev. Lett.* **60,** 848–850 (1988).
9. Maassen, J., Jeong, C., Baraskar, A., Rodwell, M. & Lundstrom, M. *Appl. Phys. Lett.* **102,** 111605 (2013).
10. Yang, L. *et al. VLSI Technol. Digest of Tech. Papers, 2014 Symposium on*, 238–239 (2014); http:dx.doi.org/10.1109/VLSIT.2014.6894432

BIOMINERALIZATION

Crystals competing for space

Analysis of the growth patterns of calcitic prisms within the shell of the fan mollusc *Pinna nobilis* shows that growth can be predicted using grain theory and that the organic casings of the prisms set the thermodynamic boundaries.

Nico A. J. M. Sommerdijk and Maggie Cusack

Biominerals, such as bone, teeth and shells, are organic–inorganic composite materials with often amazingly complex shapes and structures. Biology uses a variety of minerals to form these structures — most commonly, calcium carbonate ($CaCO_3$) and calcium phosphate, which are used by marine invertebrates and vertebrates, respectively, as well as iron oxides and silica[1]. Growth of biominerals is thought to be controlled by their interaction with a complex organic macromolecular matrix that consists of a specialized dynamic assembly of (glyco)proteins and carbohydrate polymers. As a consequence of these interactions, a high level of control is achieved over the composition, structure, size and morphology of the resulting material[2]. Moreover, through these interactions the structure and properties of the biological hybrids are precisely tuned towards their specific functions: for example, navigation, mechanical support, photonics and protection against predation, often producing physical structures that surpass those of synthetic analogues. However, the extent to which the growth of biominerals is controlled by their interaction with these organic matrices, and whether there is also control through classical thermodynamic parameters, remains unclear.

Writing in *Nature Materials*, Zlotnikov and colleagues now shed light on the shape evolution of calcite prisms in a mollusc, and show that the prismatic structure and morphology can be predicted by classical thermodynamic theories[3]. Using synchrotron-based microtomography, they analyse the mesostructure of the prisms forming the calcitic outer layer of the giant Mediterranean fan mollusc *Pinna nobilis* and conclude that only a minimal amount of biological control is used to create the well-organized prismatic crystals. Indeed, other than setting the boundary conditions of the thermodynamics involved in the process, the findings of Zlotnikov and colleagues suggest that the biological organism has little involvement in the formation of the finer structural detail of the outer layer of its shell.

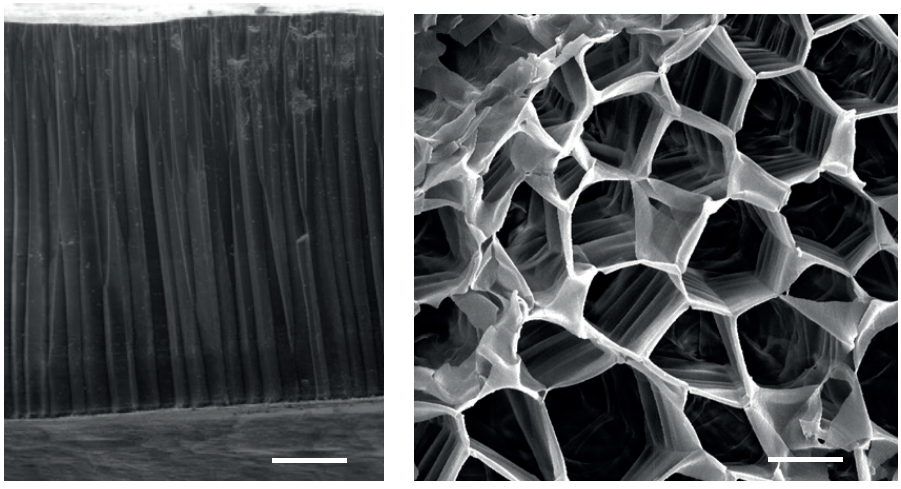

Figure 1 | Secondary electron images of the calcite prisms and organic casings of the shell of the fan mollusc, *Atrina vexillum*. **a**, Fracture section of the shell of *A. vexillum* showing the oriented calcite crystals in the prismatic layer of the shell. Scale bar, 250 μm. **b**, The organic casings in which the prisms grow. The prisms were dissolved by incubation in acetic acid (1 M) for 24 h. Scale bar, 50 μm. Images courtesy of Peter Chung (**a**,**b**) and Maggie Cusack (**b**), University of Glasgow.

Biomineralization has intrigued scientists for many decades and serves as a constant source of inspiration for the development of new materials with highly controllable and specialized properties[4]. Also, because biological materials are normally synthesized in aqueous media and at ambient temperatures — conditions that are prerequisites for the synthesis of green materials — a richer understanding of the biomineralization process may open new sustainable pathways to materials with advanced functional and structural properties. Moreover, the findings reported by Zlotnikov and colleagues point towards the simpler nature of the factors that control this particular biomineralization process, and if similar strategies could be exploited by synthetic chemists the accessibility of green synthesis routes could be greatly improved.

As a result of their abundance in nature, biological materials composed of $CaCO_3$, for example mollusc shells, are the

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Reporting Period Start Date

09/28/2012

Reporting Period End Date

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Abstract

This award allowed us to do the following for the first time:

1) Propose alternative devices for GHz-THz electronics based on 2D Xtals, such as the tunneling THIN-TFET.

2) Tunneling transistors using 2D Xtal semiconductors are most promising for GHz-THz electronics.

3) Identify the major scattering mechanisms limiting mobility in 2D crystals towards high-frequency operation.

4) Identify methods to improve carrier transport in 2D Crystal semiconductors.

5) Compare FETs made from naturally occuring and chemically synthesized 2D Crystal semic'ductors.

6) Elucidate the effect of contact resistance, and gauge the challenges for GHz-THz electronics by comparing to Si and high-speed III-V semiconductor materials.

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Research Objectives

Technical Summary

Funding Summary by Cost Category (by FY, $K)

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