CHARACTERIZATION AND ANALYSIS OF INTEGRATED SILICON PHOTONIC DETECTORS FOR HIGH-SPEED COMMUNICATIONS

THESIS

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Abstract

As the digital age of rapidly expanding information systems and technology continue to grow and develop at an ever increasing rate, new fabrication media must be investigated in order to keep up with these trends. The modern age has been defined by the innovation and advancement of the semiconductor transistor specifically Silicon, however these days of exponential performance gain through gate minimization are coming to a close. One such field which shows great promise for meeting the challenges of the future is the integration of photonic and complementary metal oxide semiconductor components; leveraging the long standing fabrication history of Silicon devices. This document describes the characterization and analysis of integrated photodiodes for digital and analog applications. The photodiode is one small but necessary component for the integration of system-level photonic devices.

A number of standard measurements were taken on the photodiodes to analyze their performance and potential application. Additionally, an anomalous detector behavior was investigated through both transient measurements to identify the driving mechanism of the abnormality. Through this testing the devices were found to perform with up to 30-GHz of bandwidth while maintaining dark currents below 5 nA. The non-linear behavior was observed under CW conditions and analyzed using the transient response of the photodiode. The transient response of the photodiode supported that the non-linear mechanism was photon-induced avalanche-like effect, however, further investigation is required. Additional work is described to further investigate this behavior, as well to identify potential effects on future application in system level communication designs.

Acknowledgements

The thesis endeavor is the collaborative construct of ideas and knowledge composed into a singular document by the author. This insufficient section gives credence to the great aide provided by all those who guided me towards the final goal of graduation as well as their thoughtful discussions on device theory.

I would first like to thank my advisor, Maj. Langley, for his support and guidance in the completion of this work. His direction was invaluable to drafting this document as well as keeping me on track to graduation.

I would like to especially thank Dr. Usechak for his guidance and patience throughout my time at AFIT. I am grateful to have had the opportunity to work in the state of the art laboratory environment he has assembled at AFRL, as well as pick his brain for a greater understanding of photonic device theory, even beyond the scope of photodetectors. His layman's description of difficult mathematical concepts has greatly expanded my understanding of photonics.

Additionally, I would like to thank Dr. Cain for direction and guidance in not only my research here at AFIT, but also for career development both in and out of the Air Force.

Finally, a special thanks is in order to Sandia National Laboratory, specifically Dr. DeRose, Dr. Zortman, and Dr. Lentine for providing me with test samples of integrated Ge on Si photodectors for this work. Their willingness to share their design and fabrication efforts with me was integral to my research.

Joseph W. Haefner

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CMP	chemical mechanical polish	14
P	Phosphorous	15
Ti	Titanium	15
TiN	Titanium Nitride	15
W	Tungsten	15
AlCu	Aluminum Copper	15
PECVD	plasma-enhanced chemical vapor deposition	15
SiO_2	Silicon Dioxide	15
RPCVD	reduced pressure chemical vapor deposition	15
SRH	Shockley–Read–Hall	26
ODE	ordinary differential equation	27
OE	optical-to-electrical	38
TEC	thermo-electric cooler	43
HVAC	heating, ventilating, and air conditioning	45
GSG	ground signal ground	46
NA	numerical aperature	47
DMM	digital multi meter	49
SMU	system source meter	49
BNC	Bayonet Neill–Concelman	50
EMI	electro-magnetic interference	50
DUT	device under test	50
LCR	inductance, capacitance, and resistance	52
TE	transverse electric	59
PMF	Polarization maintaining optical fiber	59

Abbreviation		Page
DFB	distributed feedback	60
PNA	precision network analyzer	61
VNA	vector network analyzer	61
SNR	signal-to-noise ratio	61
OVNA	optical vector network analyzer	62
LCA	lightwave component analyzer	63
EO	electrical-to-optical	63
ESA	electrical spectrum analyzer	67
GPIB	general purpose interface bus	69
DOE	design of experiments	76
AFRL	Air Force Research Laboratory	93

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CHARACTERIZATION AND ANALYSIS OF INTEGRATED SILICON PHOTONIC DETECTORS FOR HIGH-SPEED COMMUNICATIONS

I. Introduction

The prevalence of Silicon (Si) devices in the modern world can not be understated. From computers and cell phones to modern kitchen appliances nearly every commercial electronic device contains Si integrated circuits (IC)'s. This can be seen through the exponential growth of global information dissemination by means of the Internet. Si's impact can also be seen through the rapidly expanding fields of scientific advancements. These advancements are not only limited to solid state physics and engineering, but have spilled over into other scientific fields as greater processing power and memory continue to aid advancements in mathematics, physics, biology, etc. The human genome sequencing project is one such beneficiary of advanced computational power as "it is becoming faster and cheaper to sequence the entire genome of an organism" [1].

During the past half century computer chips have benefited from steady exponential increases in computational power, performance, and memory. This trend has been facilitated by increasing fabricated on-chip transistor density, and is commonly referred to as Moore's Law. Moore's Law states that the number of transistors fabricated on a single chip doubles over a prescribed time period [2]. Typically the trend is framed as doubling every 1.5 years. Figure 1 demonstrates one performance metric of processing efficiency related to Moore's law. It defines the historical computational

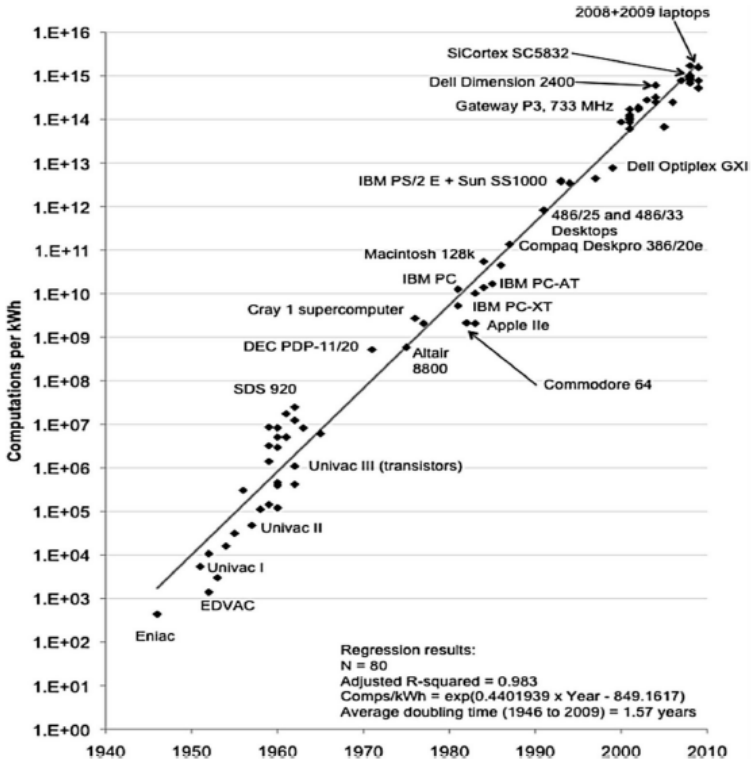


Figure 1. Computational cost per KWh vs. time. [4]

cost per kWh through the year 2010. Recently the exponential growth has waned as the fundamental limits of transistor gate size are being approached. Although progress has been made to enhance device speed by utilizing binary semiconductors with greater electron and hole mobilities, the cost and relatively small-scale advancements, 20–50% improvement, are overshadowed by present-day economics [3]. These devices are currently relegated to smaller niche markets or university research environments where the increased performance is paramount, even if it comes at a greater monetary expense. As a consequence of the cost, size, weight, and power ($CSWAP$) constraints associated with systems designed for use on aircraft and unmaned aerial vehicles (UAV)'s, the Air Force has great interest in inexpensive light communication systems for use on aircraft.

1.1 General Motivation

Photonics has long served the long-haul communication market (telecommunication companies and Internet providers), being used to rapidly transmit large amounts of data over fiber at rates not realizable using traditional electronic solutions. These data rates, typically 10 gigabits per second ($GBPS$) per channel, have been achieved based on the fact that light only minimally interacts with itself while traveling through optical fibers (due to non-linearities), as well as the fact that it experiences far less dispersion than other transmission media. [5]. In long-haul communication systems, dense wavelength division multiplexing ($DWDM$) allows many channels to be transmitted over a single fiber each at a data rate defined by the transceiver's bandwidth. This means that increasing data rates can be achieved through an up-and-out architecture where increases in bandwidth have a multiplicative effect based on the number of channels implemented.

Si photonics has recently become an area of intense interest due to the future data rates achievable using this technology as well as its scalability and potentially low-cost fabrication. Research advances in photonics promise to overcome the challenges associated with the electronic chip limitations of bandwidth, device scale, power, and heat dissipation. The general platform of photonics provides significant advantages over purely electronic circuitry systems. The commonly touted improvements are higher bandwidth with low-loss transmission over long distances, as well as the potential to "dramatically reduce power consumption for the global circuit" [6]. The integration of complementary metal oxide semiconductor ($CMOS$) electronics with photonics leverages advantages in both fields in order to design synergistic programmable devices based on the principles of both the photonic and electronic components. Additionally, it is highly desirable to integrate many optical components into $CMOS$-controlled photonic circuits as it will allow for the production of robust optical systems.

The interferometric properties utilized by many photonic systems mean that their performance greatly suffers from vibrational and thermal effects. These effects are difficult to compensate and cause issues in both fiber based and free-space based optical systems as well as make the system more fragile. However, with the reduction in physical size, a photonic integrated circuit (PIC) may be able to mitigate some of these deleterious effects of the surrounding environment without reliance on feedback controls, as well as make the system more robust [7]. These problems are extremely relevant to Department of Defense (DoD) applications especially in the Air Force as wild thermal differences (-50–250 °C) and adverse vibrational environments are extremely common in airframes.

The use of optical interconnects (OIC)'s is another area holding great promise since it will allow for higher bandwidth, lower loss communications over short distances. This application varies from the long-haul transmission application as it is designed to cover a short distance between many chips, or within a chip. As such, OIC's address applications that are particularly attractive for industrial communication implemented in data centers or supercomputers [8]. This will allow for significant improvement over purely electronic transmission which suffers high losses due to parasitic capacitance in the cabling, (up to 3 dB/m at high frequencies). In addition, microwave cables cost far more than silica fiber. The advantages of silica fiber or optical waveguide structures is readily apparent as losses can be as low as 0.2 dB/km and are virtually flat across the radio frequency (RF) transmission spectrum up to $\sim$1 THz. This flat frequency response is due to the wavelength-dependent losses in optical waveguides; in which the modulation of a GHz signal onto a THz carrier does not shift the spectrum enough to vary the loss attributed to the optical media. In addition, by creating greater separation between processing cores using PIC's, thermal management concerns for heat dissipation in compact processing environments

may be diminished.

Contemporary techniques for fabricating *OIC*'s require flip-chip bonding, as many photonic components are derived from legacy long-haul technologies fabricated using binary *III-V* semiconductors. Within *Si* foundries, *III-V* binary compounds contaminate the process of fabricating *Si CMOS* components. The risk of contamination precludes the monolithic fabrication of such devices [9]. In order to construct such systems, the electronic and photonic components are manufactured separately to ensure the integrity of both structures. Then the two must be flip-chip bonded during the packaging process to complete the integration of the device; one such example is the 1550-nm transceivers fabricated by Roth et al. [10]. While these devices exemplify the integration advantages of *PIC*'s, a better solution is the seamless monolithic fabrication of group *IV* photonic devices amalgamated into the reliable and greatly developed market of *Si* electronics.

Due to the long fabrication history of *Si IC*'s and the prevalence of elemental *Si* (which can be refined into very pure ingots), as well as the large monetary investment in *Si* foundries, *Si* has been identified as a favorable candidate for hosting *PIC*'s. Moreover, it has a higher index of refraction than Indium Phosphide (*InP*) binary components allowing for greater filtering in the application of wavelength division multiplexing (*WDM*) [11]. The larger index of refraction also enables smaller feature sizes due to stronger optical confinement when compared to *InP*. This in turn allows for tighter bends with less loss while routing the optical signal around the chip. Tighter bends also enable waveguides to be smaller without suffering additional penalties, which saves valuable space for the fabrication of *CMOS* electronics or other photonic components on the wafer enabling greater system complexity at lower cost per area.

1.2 DoD Motivation

While industry has looked to the previously stated high-bandwidth and *WDM* properties of photonics to address their big data storage, processing, and transmission concerns, the *DoD* has seen an abundance of relevant applications for such stable photonic systems. The first primary application of the *DoD* is simply an extension of the above stated industrial application. As greater numbers of sensors and systems are placed on combat equipment, a high-bandwidth data transmission system with the ability to transmit, connect, and process the information from all of these sources provides a platform for enhancing the warfighter's battlefield awareness.

An additional application for the high-bandwidth capability of integrated photonic systems, could be used for analog antenna remoting. By up-converting to a high-bandwidth optical carrier the entire received *RF* spectrum can be transmitted and centrally processed using photonics [12, 13]. This approach would facilitate a greater consciousness for the *RF* spectrum from MHz to $\sim$1 THz demonstrating an advantage over any purely electronic approach. Electronic approaches suffer an intrinsic bottleneck due to narrow-band down conversion, as a small region of the incident *RF* signal must first be down converted before being transmitted. This requires expensive narrow-bandwidth mixers as well as heavy *RF* equipment and cables, a detrimental attribute when loaded onto weight-conscious airframes.

Beyond the high-bandwidth capabilities of integrated photonic systems is the application of beam steering. Integrated photonics provides a fabrication media in which greater directionality can be achieved in the *RF* spectrum. While traditional electronics rely on phase shifters to perform beamforming for directionality and tracking in radar applications, the use of true time delay photonics has the potential to significantly improve performance over a wide frequency range [14].

Another integrated photonics application worth noting lies outside the focus of

communication and signal identification. It relates to the battlefield application of the recognition of various chemicals or organic compounds using integrated photonic platforms. By using various ring resonators with binding agents the shift in the operating frequency of the ring, and therefore the detected optical signal, by foreign matter bound to ring material can be used to identify both the compound and the quantity [15]. This has potential application for the identification of biological agents used against personnel in deployed environments.

1.3 Focus

With *Si* firmly established as an attractive platform for monolithic photonic integration today, a significant struggle must be identified and addressed: Group *IV* semiconductors, [e.g. *Si* and Germanium (*Ge*)], are indirect band-gap materials. As a consequence, fabrication challenges arise for some of the requisite components used in the implementation of optical communication systems. The three essential components for building any optical communication system are an emitter, a channel and a receiver. Additionally, either the direct modulation of the source or an external modulator as depicted in Figure 2 is required to encode the electrical signal onto the optical carrier. Figure 2 shows a pictorial representation of these necessary components used in an optical communication system. With the exception of an efficient electrically pumped optical source, which had been theorized and very recently demonstrated using heavily strained and doped *SiGe* heterostructures [16, 17, 18], all of the remaining constituent optical components have been successfully fabricated and tested with sufficient yields using *CMOS* suitable techniques.

The 1550-nm window has long been identified as the optimal operating wavelength for communication as it is the wavelength with the minimal loss for single-mode fiber (*SMF*) based on silica. Another approach to incorporate a source on-chip is the

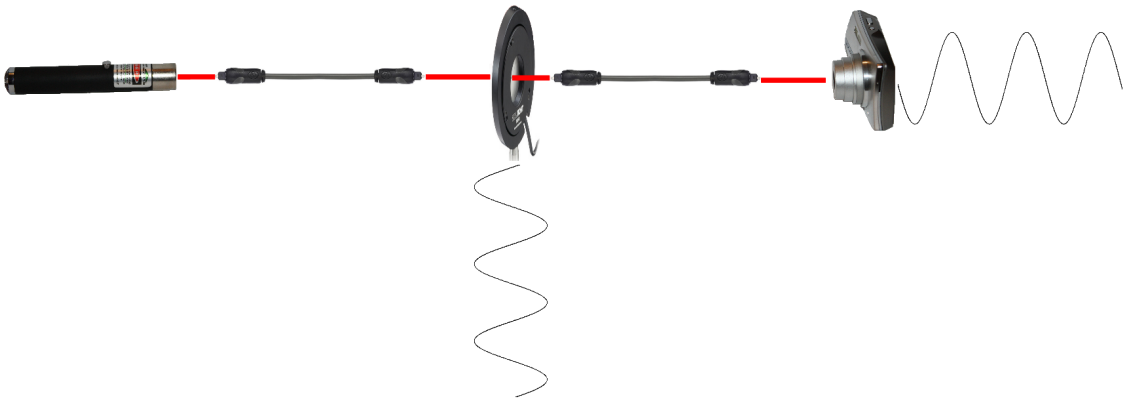


Figure 2. A pictorial representation of the requisite components in an externally modulated photonic communication system showing: an optical source (to act as a carrier for the signal), a transmission channel (a media which confines the optical field for minimal loss), a modulator (to encode data onto the carrier), and an optical receiver(to detect the encoded information).

molecular bonding of InP onto Si waveguides. Here evanescent coupling of an InP laser is used to stimulate emission in the Si waveguide at 1310 nm. The 1310-nm wavelength is the other common communication window as it is the minimum dispersion wavelength of silica fiber [19, 20].

The second component is the channel, which has been fabricated using on-chip Si wire waveguides. Si wire waveguides have been demonstrated as a sufficient channel at 1550 nm since they have been measured to have bend losses of 0.0086 dB/turn fabricated with a turn radius of 1 μm [21, 22, 23]. Also, the absorption coefficient of Si rapidly falls for wavelengths longer than 1 μm leading to low-loss optical transmission on the chip.

The third optical component is the modulator. While Lithium Niobate ($LiNbO_3$) modulators dominate the commercial market they are not easily realizable on a monolithically integrated platform [24]. Intensity modulators are the are the easiest to understand for the transmission of information; the most simplistic of these modulators is the electro-absorption modulator. Electro-absorption modulators work by changing the absorption coefficient of the channel thereby modulating the intensity of

the optical signal. Unfortunately, electro-absorption modulators fail to approach the bandwidth and extinction ratio of the Mach–Zehnder Modulator (*MZM*). A *MZM* is simply an interferometer which uses an applied voltage to change the optical path length in one or both arms. A Y-junction is used to split the light between the two arms of the modulator, the delay between the arms then causes the modes to be "out of phase." When they recombine using another Y-junction a majority of the power leaks out through the evanescent mode due to the phase shift. *Si MZM*'s have been demonstrated with bandwidths of over 40 GHz and tested well beyond 10-*GBPS* non-return to zero (*NRZ*) patterns [25, 26, 27, 28, 29].

While modulator development has received the majority of attention for system-level improvement; the design of a high-bandwidth optical detector still requires characterization and improvement for overall system-level functionality [6]. Based on the previous requirements and motivation, high-speed *SiGe* photodiodes are a natural candidate to fill this component need. They are sufficiently small, and can be fabricated using *CMOS*-compliant techniques. *SiGe* detectors also have a narrow bandgap which can absorb incident optical power beyond the wavelength of *Si* detectors. This allows them to operate in both of the tele-communication windows: 1310 nm and 1550 nm. The effective monolithic fabrication of *PIC* structures simultaneously with electronic integrated circuits represents the initial system-level goal of *OIC*'s as demonstrated in [30]. Pinguet *et al.* successfully fabricated a four-channel bi-directional 40-*GBPS* transceiver by integrating all these necessary components (with the exception of an integrated optical source).

1.4 Organization

This thesis focuses solely on *SiGe* photodiode characterization, application, and modeling for optical link recievers. It is broken into five chapters including this intro-

duction as well as an appendix . The second thesis chapter describes the structures and fabrication of $SiGe$ photodiodes. This chapter also includes an introduction to the basic operating principles for pin junctions based on a traditional model. Through the derivation of this model, some non-idealities will be described.

Chapter three describes the principles of testing and analysis of fabricated $SiGe$ photodetectors as well as the purpose of each measurement. A description of the test-measurement fixtures designed to facilitate this work is also included. This highlights the new improvements over traditional test fixture design. Verification of the test and measurement collection using a commercial off the shelf ($COTS$) photodetector is used to validate and calibrate the results shown in the fourth chapter.

Chapter four contains the results of the data obtained from the devices as well as conclusions which can be drawn for future design and manufacture of $SiGe$ devices. In addition, the chapter contains new findings on uncharacteristic behavior of photodetectors and hypothesis to explain the physical mechanism leading to these results.

Finally, chapter five contains a synopsis of the results and findings of chapter four. It also gives suggestions for future related work in advancement of the monolithic integration of photodiodes in group IV semiconductors for both commercial and DoD applications. Access to a greater number of die to test would have facilitated a numerical analysis on variation and yield within the fabrication process. For this research, foundry constraints limited the number of samples obtained.

II. Theory and Literature Search

2.1 Fabrication

PHOTODETECTORS for monolithic *OIC*'s are typically designed either using a metal-semiconductor-metal (*MSM*) Schottky photodiode [31, 32, 33], or a *pin SiGe* photodiode structure [6, 34, 35, 36]. Nevertheless, due to the significantly larger dark currents in Schottky photodiodes, *pin SiGe* structures are preferred. Such *pin SiGe* photodiodes can be fabricated either using a vertical structure or a horizontal configuration depending on the foundry capabilities and mask design. Vertical photodiodes are stacked devices in which the electric field runs perpendicular to the face of the wafer, where as the horizontal structure generates an electric field that runs parallel to the surface of the wafer. For both schemes, the optical field propagation is perpendicular to the electric field. These designs are different from commercial detectors which use surface coupling of the light to impinge upon a vertical structure. Therefore, in the *COTS* devices the electric field and the propagation of the optical field are parallel to one another.

The final characteristic associated with the photodiode structure is the coupling method. Integrated detectors can be: 1) butt or end-fire coupled (the waveguide terminates directly into the photodiode), 2) adiabatically taper coupled (the waveguide tapers as it approaches the detector drawing the mode out of the waveguide and into the higher index material of the *Ge* detector), or 3) evanescently coupled (the evanescent field of the spatial mode is detected as the waveguide passes close to the detector). Evanescent detectors have the lowest responsivity as they only detect a small portion of the guided mode. This often means they must be larger in size and take up more space on the chip in order to have responsivities near that of the butt-coupled devices [6]. Therefore, butt-coupled devices are frequently used in order

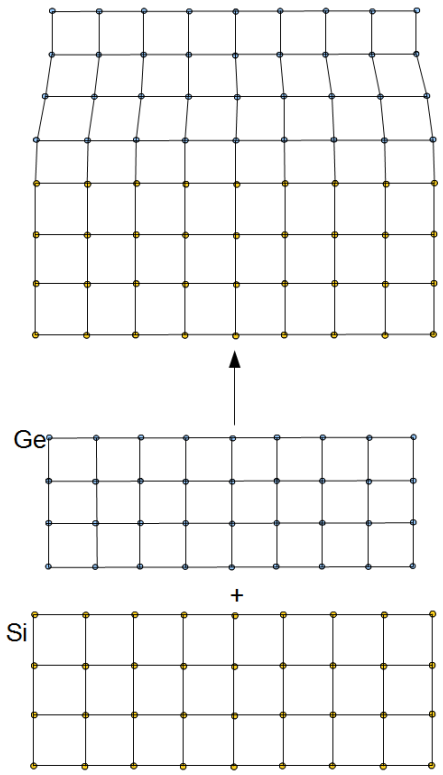
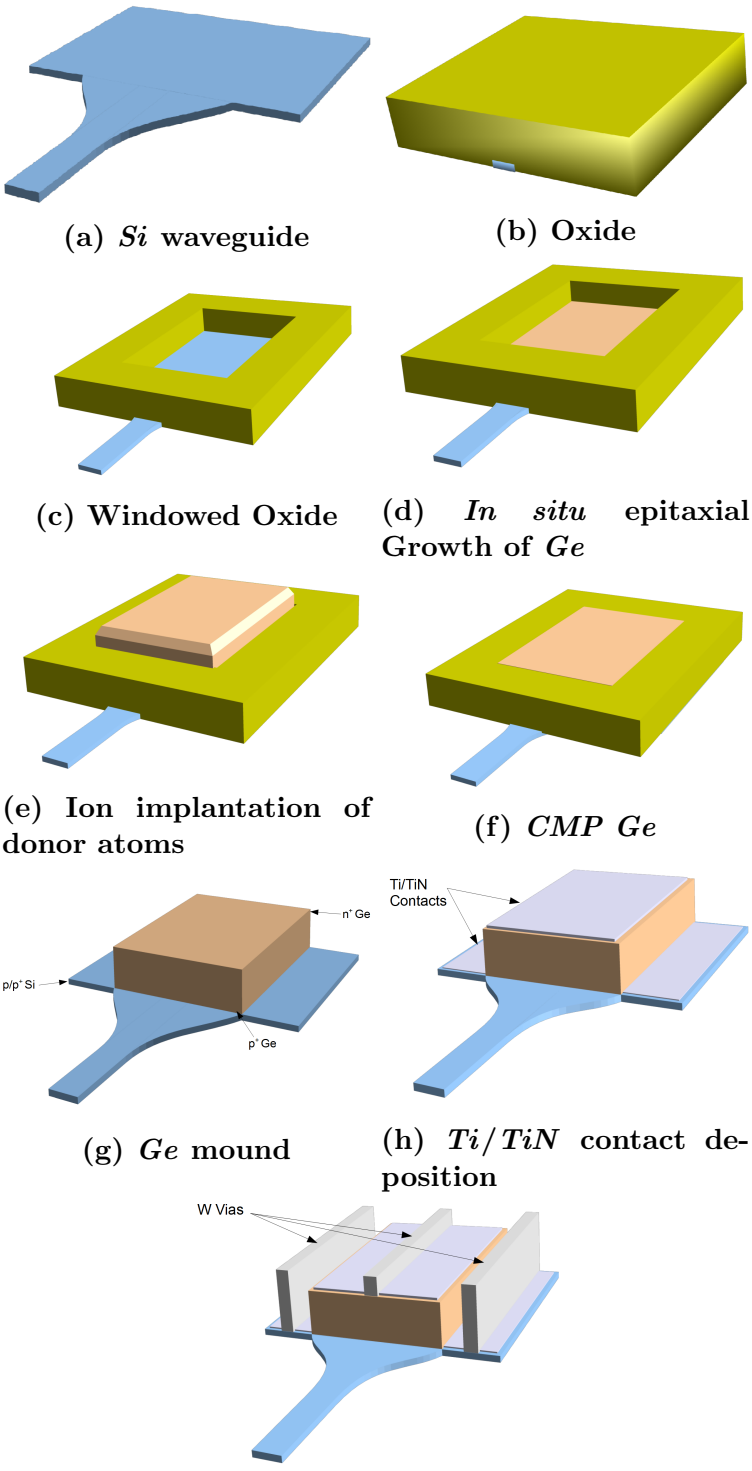


Figure 3. Lattice strain between *Si* and epitaxially grown *Ge* adapted from [37].

to maintain a minimum footprint, thus maximizing the area over which transistors or other devices can be fabricated.

The manufacturing challenge associated with the *Ge* detectors fabricated on *Si* substrates stems from the large lattice mismatch of 4.2% between the *Si* lattice and the *Ge* lattice. Such a mismatch can be seen in Figure 3. This lattice mismatch induces a strain in the composite device that leads to threading dislocations which directly contribute to the dark current noise value for the detector by creating recombination sites. Increased dark current decreases the dynamic range of the photodetector as it limits the noise floor for low-threshold signal detection and is problematic particularly for analog applications. As a result the characterization of a photodiode's dark current is one of the key measurements to determine the quality and functionality of the detector.



(a) *Si* waveguide

(b) Oxide

(c) Windowed Oxide

(d) *In situ* epitaxial Growth of *Ge*

(e) Ion implantation of donor atoms

(f) *CMP Ge*

(g) *Ge* mound

(h) *Ti/TiN* contact deposition

(i) Vertical *Ge pin* diode

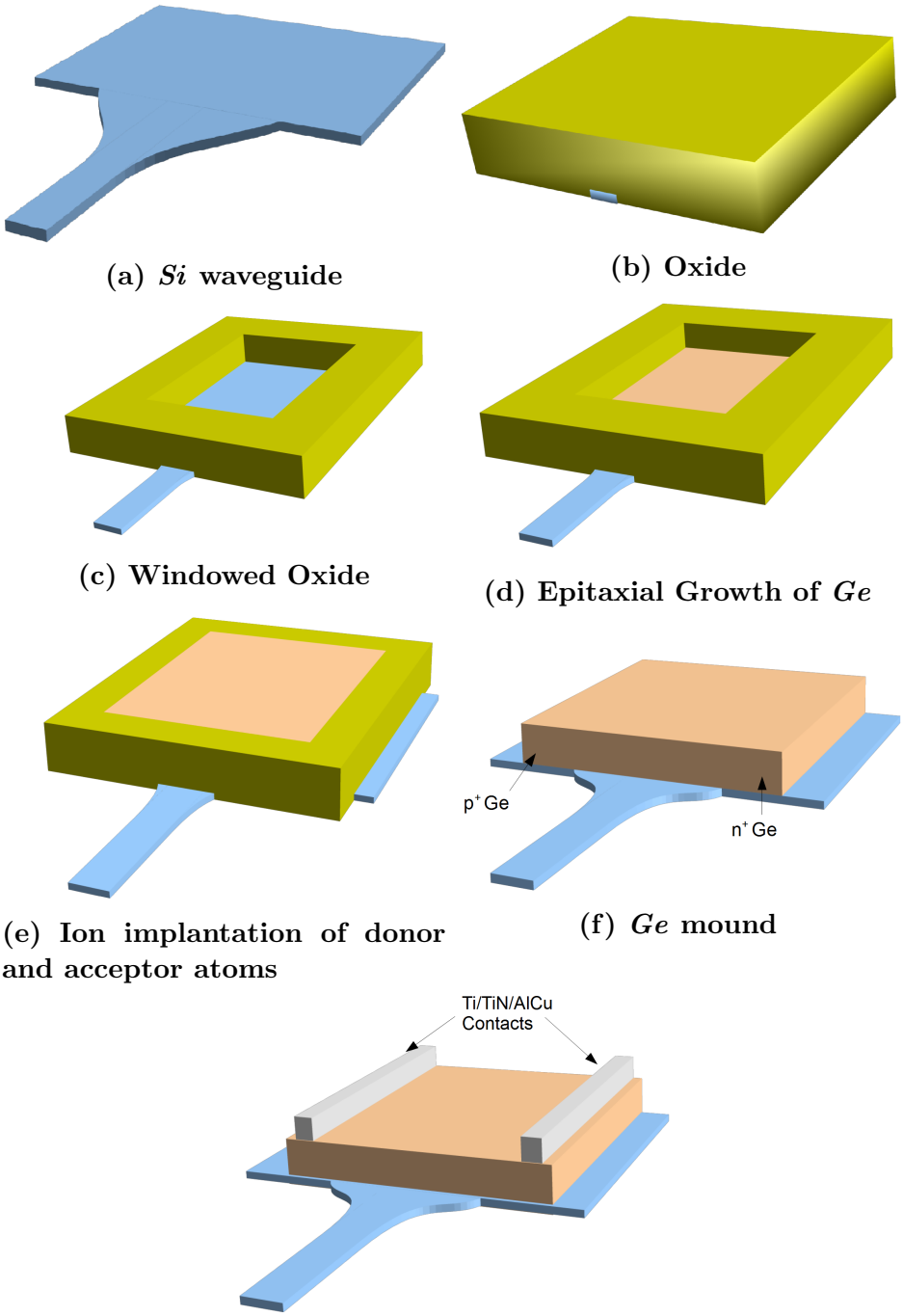
Figure 4. Fabrication steps for realizing a vertical *Ge pin* photodiode from [36].

The *pin* photodiode consists of an epitaxially grown layer of *Ge* which is annealed and heavily doped on either the sides or top and bottom depending on the geometry. This process creates the resulting *p*-doped intrinsic *n*-doped composition of the *pin* device. The vertical *pin* diodes traditionally implemented a top-down approach to the growth of *Ge* on *Si*, epitaxially growing a field of *Ge* which was etched back to leave *Ge* mesas on which the detector would be fabricated [36]. However, windowing the insulating layer grown on a Silicon-on-Insulator (*SOI*) wafer, and selectively growing Ge epilayers reduces the number of threading dislocations as the limited growth area allows for dislocations to rapidly terminate at the *Ge*-oxide boundary [36, 38]. The decrease in dislocation density diminishes the dark current of the detector resulting in better performing devices. Dislocations as low as 2.3x10^6 cm^{-3} have been reported in such structures using a periodic annealing process [38].

The account of the following fabrication process flow for a vertical *pin* structure is derived from Ref. [36] and can be visualized in Figure 4. The initial buffer layer is grown on heavily doped ion-implanted *p*-type or p^+-type *Si*, in an etched window at the termination of a fabricated waveguide. Here the heavily doped *Si* acts as an ohmic contact for the *p*-type Germanium. The initial *Ge* was slowly grown at low temperatures (400 °C). As this initial layer is grown it is *in-situ* doped with Boron (*B*) acceptor atoms to create the *Ge* *p*-type region of the *pin* diode. Upon completion of the *p*-type *Ge* growth, the remaining growth of intrinsic *Ge* is completed at 600 °C, where it occurs more rapidly, until the *Ge* reaches a thickness of 0.6–0.8 μm, just beyond the height of the oxide. A chemical mechanical polish (*CMP*) planarization process is used to return the over grown *Ge* mound to the height of the oxide. The overgrowth is required to fill voids at the upper boundary of the oxide therefore reducing dislocations. The *CMP* is simply required to return the mound to the proper height of 0.5–0.7 μm. Following the completed mound growth ion implantation

is used to dope the top region of the Ge with Phosphorous (P) atoms creating the capping n-type layer of the *pin*-junction which is thermally annealed at 630 °C in order to activate the doping atoms and complete the diode. Ti/TiN is sputtered over the surfaces in order to make ohmic contacts for the Tungsten (W) vias. The vias lead to metal interconnects using a $Ti/TiN/AlCu/TiN$ stack to complete the electrical connection. The final step is the plasma-enhanced chemical vapor deposition ($PECVD$) of the 2.5-μm SiO_2 optical cladding. This creates the low index of refraction ensuring optical confinement within the Si waveguide. In the case of the devices tested in this work, the lengths and widths were varied from 5–50 μm and 1–4 μm in order to identify ideal geometry for bandwidth, dark current, responsivity and junction capacitance. Such devices have been characterized with bandwidths greater than 45 GHz [36]. It should be noted that the devices characterized in this thesis document were designed in this manner using an end-fired coupling structure.

The alternate lateral *pin* structure has a very similar design flow for the fabrication of the Ge mound around which the vertical *pin* structure was fabricated. The Ge initially deposited is not *in-situ* doped during the growth process. Vivien, *et al.* describes the design flow for these lateral structures [6] as seen in Figure 5. One advantage of lateral *pin* structures is the smaller degree of surface topology. This simplifies the future process of integrating $CMOS$ structures with photonic devices. Following the fabrication of the waveguide structures on the SOI and deposition of a 0.8-μm Silicon Dioxide (SiO_2) layer, a 10x10x2-μm window is etched in the field oxide at the termination of the waveguide to expose the Si substrate. The Ge mound will be grown on this substrate using reduced pressure chemical vapor deposition $RPCVD$. The final Ge mound is grown beyond the oxide thickness and then CMPed to the proper height. Again this overgrowth and polish process reduces deleterious dislocations. Following the growth of the Ge mound it is masked and ion implanted



(a) *Si* waveguide

(b) Oxide

(c) Windowed Oxide

(d) Epitaxial Growth of *Ge*

(e) Ion implantation of donor and acceptor atoms

(f) *Ge* mound

(g) Horizontal *Ge pin* diode

Figure 5. Fabrication steps for realizing a horizontal *Ge pin* photodiode adapted from [6].

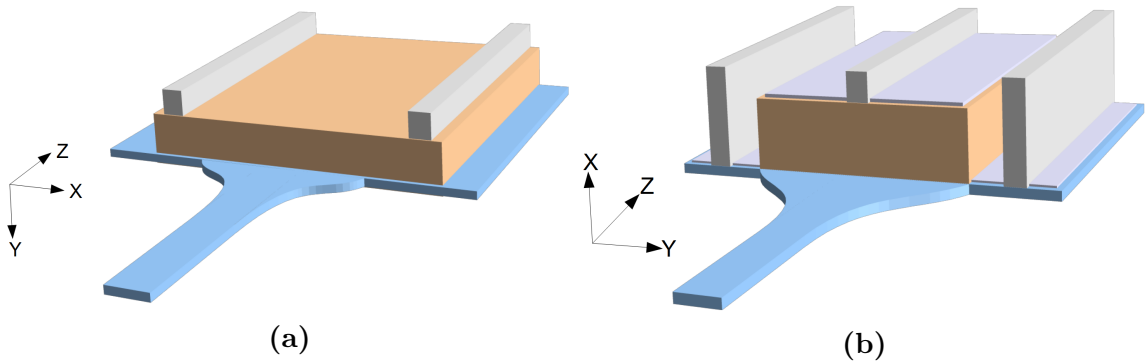


Figure 6. Assigned axes for *pin* (a) horizontal structure and (b) vetical structure. Optical field propagation is in the positive Z direction while the electric field of the reverse biased diode is in the negative X direction.

with B and P to generate the p-type and n-type regions respectively. Windows are etched and filled with TiN/W vias and connected the $Ti/TiN/AlCu$ metal interconnect to complete the device. Figure 6 shows a comparison of the two detector geometries with the associated coordinate system which will be used throughout this document.

2.2 Theory

A background in semiconductor physics and theory is discussed in order to understand the operation of photodiodes. This section will focus on the theory and operation of photodetectors and in so doing will lead to the derivation of commonly referenced figures of merit for such devices.

2.2.1 Steady State and CW Theory.

The basic theory behind photodetectors is relatively straight forward. Photodiodes are based on a reverse biased *pn* or *pin* junction. The reverse bias ensures carriers generated in the depletion region will rapidly be swept out thereby becoming

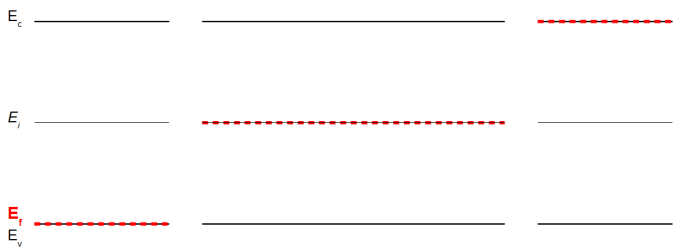


Figure 7. Fermi levels across the junction of *pin* diode before contact showing degenerate doping in the *n* and *p*-regions.

majority carriers contributing to the optically generated current. A simple analysis and derivation of the ideal photodiode operation will follow. Greater detail can be found in a more in-depth derivation of the ideal diode using e.g. Ref [39]. This section will begin with the derivation of the IV characteristics of a simple *pin* junction using Poisson's equation for electro-statics Eq. 1 as well as the continuity equations for electrons and holes (Eqs. 2 and 3) to ground the device's behavior.

$$\nabla^2\phi = \nabla\ E = \frac{\rho}{\epsilon_s} \tag{1}$$

$$\frac{\delta n}{\delta t}Adx = \frac{1}{q}\left(J_n\left(x+dx\right) - J_n\left(x\right)\right)A + \left(G_n - R_n\right)A \tag{2}$$

$$\frac{\delta p}{\delta t}Adx = \frac{1}{-q}\left(J_p\left(x+dx\right) - J_p\left(x\right)\right)A + \left(G_p - R_p\right)A \tag{3}$$

2.2.1.1 Depletion Region and Dark Current.

The derivation of the dark current is the simplest of the performance metrics of a photodiode to calculate as it is a purely electronic property of the device. It is assumed that all carriers are thermally generated and therefore the device can be treated exclusively as an electronic component. Typically *pin* diodes are degenerately doped with donors and acceptors such that the dopant densities approach the density of states in the conduction and valance bands ($N_d \rightarrow N_c$ and $N_a \rightarrow N_v$). This in turn

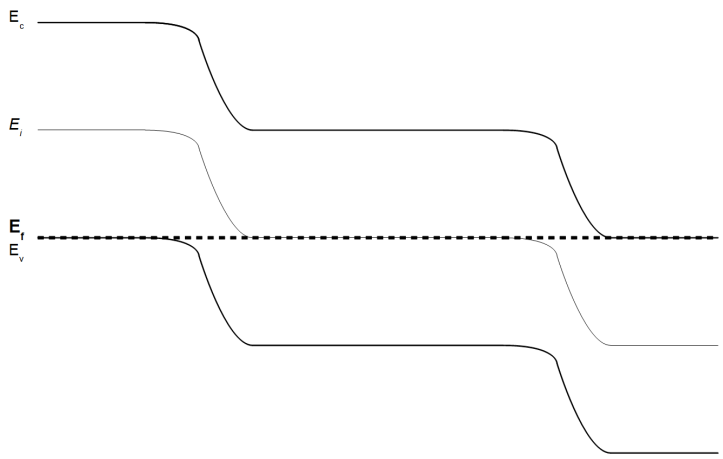


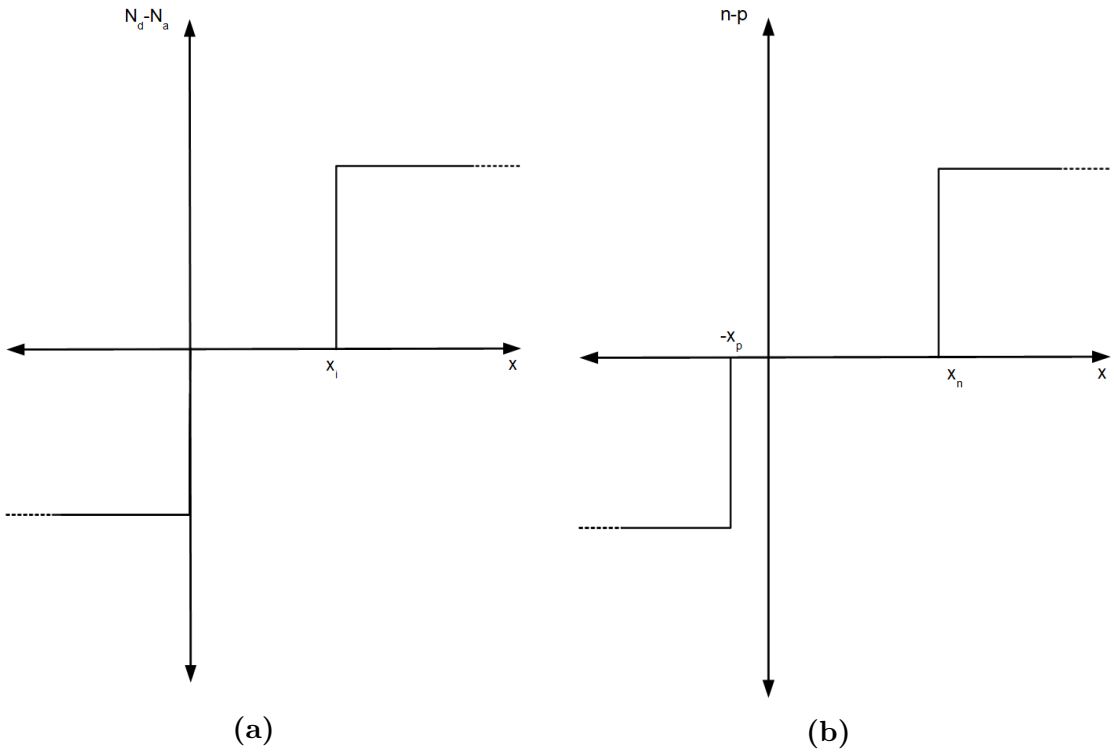
Figure 8. Band diagram of *pin* diode in equilibrium.

drives the Fermi level into the conduction and valence bands respectively as shown in Figure 7. Aligning the Fermi levels of the junction generates the band diagram of the *pin* junction shown in Figure 8. This band diagram will be the model for the derivation of the carrier dynamics of the current in the device.

Under the assumption that doping levels follow a step function, the width of the depletion region, as well as the potential (ϕ) and electric field (E) across the junction, can be solved using the one-dimensional Poisson's equation given by Eq. 4. Where p and n are the charge carrier concentrations, ρ is the space-charge density, q is the charge of an electron, and ϵ_s is the permitivity of Ge. It should be recognized that the coordinate system used is based upon the coordinate systems shown in Figure 6.

$$\frac{d^2\phi}{dx^2} = -\frac{dE}{dx} = -\frac{\rho}{\epsilon_s} = -\frac{q}{\epsilon_s}\left(p - n + N_d - N_a\right) \tag{4}$$

Using the energy band it is assumed that all activated donor and acceptor atoms ionize in order to contribute to the carrier concentration in a semiconductor near room temperature. Therefore the total carrier concentrations in the n-doped and p-doped



(a) **(b)**

Figure 9. (a) Dopant densities and (b) carrier densities in a *pin* junction.

regions can be estimated as $n = N_d$ and $p = N_a$. It was previously stated that dopant concentrations are significantly greater than the intrinsic carrier concentrations such that $N_a \gg n_i$ and $N_d \gg n_i$. This step function for the resultant dopant concentrations is shown in Figure 9a. Figure 9b shows the resultant carrier concentrations of the junction after it has reached equilibrium. It is important to note in Figure 9b that the carrier concentration in the depletion region is negligible, which allows for the simplification of Eq. 4 into Eq. 5.

$$\frac{d^2\phi}{dx^2} = -\frac{dE}{dx} = -\frac{\rho}{\epsilon_s} = -\frac{q}{\epsilon_s}\left(N_d - N_a\right) \tag{5}$$

With only the electrically charged dopant atoms remaining in the space charge region, the electric field can be solved for by rewriting the second half of Eq. 5 into its integral form:

$$E = \int \frac{\rho}{\epsilon_s}\,\mathrm{d}x = \int \frac{q}{\epsilon_s}\left(N_d - N_a\right)\,\mathrm{d}x \tag{6}$$

It is then easiest to separate the depletion region into three sections solving: $-x_p \leq x \leq 0$, $0 \leq x \leq x_i$, and finally $x_i \leq x \leq x_n$. The boundary conditions for the electric-field solution must also satisfy these criterion: the electric field must be continuous and the electric field is zero outside of the depletion region. This leads to the electric-field distribution shown in Eq. 7, which is represented in Figure 10. Substituting the solution from Eq. 7 into Eq. 5 generates the solution for the change in potential across the depletion region.

$$E(x) = \begin{cases} 0 & : \quad x \leq -x_p \\ \frac{-q}{\epsilon_s} N_a \left(x + x_p\right) & : \quad -x_p \leq x \leq 0 \\ \frac{-q}{\epsilon_s} N_a \cdot x_p & : \quad 0 \leq x \leq x_i \\ \frac{q}{\epsilon_s} N_d \ \left(x - x_i\right) - \frac{q}{\epsilon_s} N_a \cdot x_p & : \quad x_i \leq x \leq x_n \\ 0 & : \quad x \geq \ x_n \end{cases} \tag{7}$$

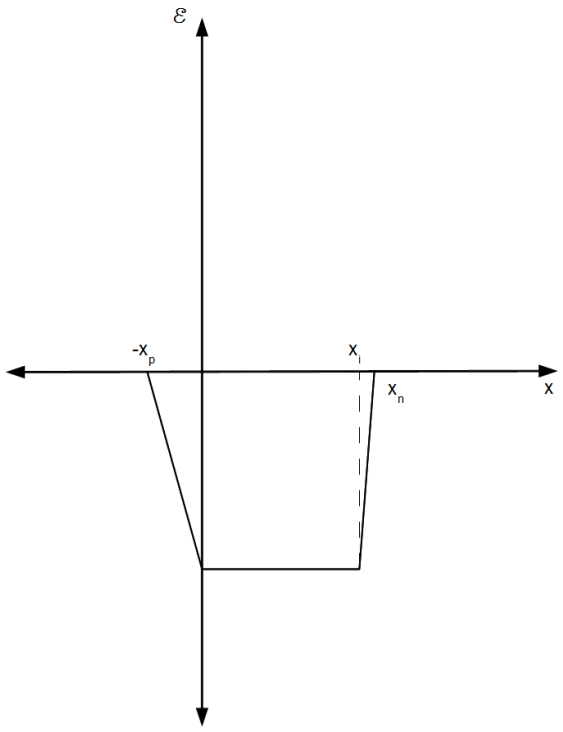


Figure 10. Electric-field strength across the *pin* diode.

Again rewriting the one-dimensional Poisson's equation into the integral form of Eq. 8 allows for the calculation the potential across the device using the electrical field solution from Eq. 7.

$$\phi(x) = -\int E(x)\,\mathrm{d}x \tag{8}$$

This is accomplished by integrating the electric field in the five regions while ensuring the result is continuous and the potential outside the depletion region on the n-doped side and p-doped side is equal to ϕ_n and ϕ_p respectively. Due to the earlier assumption that the Fermi levels are in the valence and conduction bands this simplifies the problem to $\phi_n = -\phi_p = \frac{E_g}{2}$. With these criterion satisfied the solution for the potential across the junction is shown in Eq. 9 where Figure 11 graphically represents

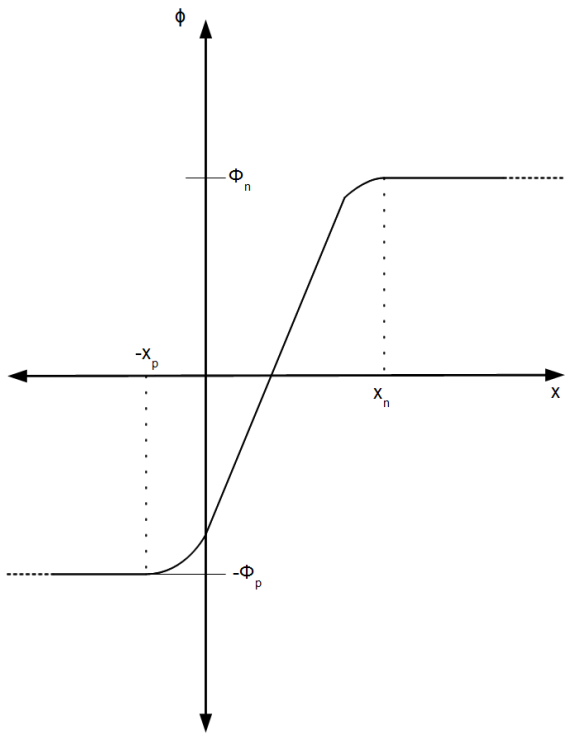


Figure 11. Potential within the *pin*-junction.

this result.

$$\phi(x) = \begin{cases} -\phi_p & : \quad x \leq -x_p \\ \frac{q}{2\epsilon_s} N_a \left(x^2 + 2x_p x + {x_p}^2\right) - \phi_p & : \quad -x_p \leq x \leq 0 \\ \frac{q}{2\epsilon_s} N_a \left(2x_p x + {x_p}^2\right) - \phi_p & : \quad 0 \leq x \leq x_i \\ \frac{-q}{2\epsilon_s} N_d \ \left(x^2 - 2x_i x + {x_i}^2\right) + \frac{q}{2\epsilon_s} N_a \left(2x_p x + {x_p}^2\right) - \phi_p & : \quad x_i \leq x \leq x_n \\ \phi_n & : \quad x \geq \ x_n \end{cases} \tag{9}$$

Finally, using the values for the potential across the junction it is possible to calculate the depletion region width of the diode. This value will be important to both the CW and RF response of the photodiode. Remembering that the junction must maintain a neutral charge, the number of dopant B and P atoms in the depletion

region of the junction must be equal. Under the previous assumption regarding the doping concentrations as a step function, the previous statement simplifies to $N_a\left(0+x_p\right) = N_d\left(x_n - x_i\right)$ which means x_p can be defined as $x_p = \frac{N_d}{N_a}\left(x_n - x_i\right)$. This value can be substituted into Eq. 9 for the region $x_i \leq x \leq x_n$. Additionally, recalling that the Fermi levels are in the conduction and valance bands respectively $\phi_n + \phi_p = \phi_i \approx E_g/q$. Therefore, the remaining single equation can be solved to determine the depletion region edge location x_n in Eq. 10.

$$\phi_i = \frac{-q}{2\epsilon_s} N_d \left({x_n}^2 - 2x_i x_n + {x_i}^2\right) + \frac{q}{2\epsilon_s} N_a \left(2\left[\frac{N_d}{N_a}\left(x_n - x_i\right)x_n\right] + \left[\frac{N_d}{N_a}\left(x_n - x_i\right)\right]^2\right) \tag{10}$$

By re-arranging the terms of Eq. 10 into the polynomial shown in Eq. 11 the solution becomes apparent as an application of the quadratic formula. The solution for the location x_n is then reduced to Eq. 12.

$$0 = {x_n}^2\left(\frac{N_d}{N_a} + 1\right) - x_n\left(2\frac{N_d}{N_a}x_i\right) + \left(\frac{N_d}{N_a} - 1\right){x_i}^2 - \frac{2\phi_i\epsilon_s}{qN_d} \tag{11}$$

$$\begin{aligned} x_n &= \frac{\frac{N_d}{N_a}2x_i \pm \sqrt{\left(2\frac{N_d}{N_a}x_i\right)^2 - 4\left(\frac{N_d}{N_a}+1\right)\left[{x_i}^2\left(\frac{N_d}{N_a}-1\right) - \frac{2\phi_i\epsilon_s}{qN_d}\right]}}{2\left(\frac{N_d}{N_a}+1\right)} \\ &= \frac{\frac{N_d}{N_a}x_i + \sqrt{{x_i}^2 + 2\left(\frac{\phi_i\epsilon_s\left(N_a+N_d\right)}{qN_aN_d}\right)}}{\frac{N_d}{N_a}+1} \end{aligned} \tag{12}$$

Using this result of the location of the depletion region boundary and its charge neutrality relation to the opposite boundary ($-x_p$), the total depletion width is given by Eq. 13. This value of depletion-region width is vitally important as it will define the absorption cross section and the junction capacitance for the RC equivalent circuit in the next sections. In addition, the depletion-region width changes with applied bias V_a, while V_{bi} has been substituted to represent the built-in potential which was previously shown to be $V_{bi} = \phi_i = E_g$. It should be obvious that the depletion region

width grows with increases in reverse bias, however the change in depletion width is very small. There are two factors which control why V_a has such a small effect. The first is the fact that the intrinsic-region width (x_i) dominates the width of the junction, while the second is related to the dopant concentrations. Because very high dopant densities are used in the fabrication of *pin* structures, the denominator of the second term under the radical becomes very large minimizing effects on depletion region width through the applied reverse bias.

$$w' = x_n + x_p = \sqrt{{x_i}^2 + 2\left(\frac{(V_{bi} - V_a)\,\epsilon_s\,(N_a + N_d)}{qN_aN_d}\right)} \tag{13}$$

With the solution for the depletion region completed, it is now possible to derive the ideal current through the device. Using the same solution approach as a *pn*-junction, the derivation begins with the one-dimensional continuity Eqs. 2 and 3 for electrons and holes from [39]. The Taylor-Series expansion seen in Eq. 14 is then used to expand the current density value at the edge of the infinitesimally thin slice through which the current flows. The first two terms of the series are substituted into Eq. 2 in order to simplify the expressions. Finally, substituting the current density Eqs. 15 and 16 into the simplified expression, the ambipolar transport Eqs. 17 and 18 are obtained. Where μ_n, μ_p, D_n, and D_p are the mobility and diffusion coefficients for the electrons and holes respectively. The diffusion coefficient for electrons is defined by Einstein's relation $\left(D_n = \left(\frac{kT}{q}\right)\mu_n\right)$, where T is the temperature and k is Boltzman's constant. The diffusion coefficient for holes is similarly defined by substituting μ_p for μ_n.

$$J_n\,(x + dx) = J_n\,(x) + \frac{\delta J_n}{\delta x}dx + \frac{\frac{\delta^2 J_n}{\delta x^2}dx^2}{2!} + ... \tag{14}$$

$$J_n = q\mu_n n E_x + qD_n\frac{dn}{dx} \tag{15}$$

$$J_p = q\mu_p pE_x - qD_p\frac{dp}{dx} \tag{16}$$

$$\begin{aligned} \tfrac{\delta n}{\delta t} &= \tfrac{1}{q}\tfrac{\delta J_n}{\delta x} + (G_n - R_n) \\ &= \mu_n n\,(x)\,\tfrac{\delta E(x)}{\delta x} + \mu_n E\,(x)\,\tfrac{\delta n(x)}{\delta x} + D_n\tfrac{\delta^2 n(x)}{\delta x^2} + (G_n - R_n) \end{aligned} \tag{17}$$

$$\begin{aligned} \tfrac{\delta p}{\delta t} &= -\tfrac{1}{q}\tfrac{\delta J_p}{\delta x} + (G_p - R_p) \\ &= -\mu_p p\,(x)\,\tfrac{\delta E(x)}{\delta x} - \mu_p E\,(x)\,\tfrac{\delta p(x)}{\delta x} + D_p\tfrac{\delta^2 p(x)}{\delta x^2} + (G_p - R_p) \end{aligned} \tag{18}$$

In order to generate a usable analytic expression for the generation and recombination rates for implementation in the ambipolar transport equations, several assumptions must be made. The first assumption considers low-level injection across the diode, such that minority carrier concentrations are much smaller than the majority carrier concentrations. Therefore, the majority carrier concentrations do not deviate significantly from their thermal equilibrium value. This leads to the presumption that Shockley–Read–Hall (SRH) recombination is the dominant recombination mechanism. The next assumption is that the capture cross sections for electrons and holes are equivalent, such that $\sigma_n = \sigma_p = \sigma_0$. This allows the expression for the net thermal recombination rate in Eq. 19 to be written as $\tau_0 = (N_t v_{th}\sigma_0)^{-1}$ where N_t and v_{th} are the density of trap states and electron thermal velocity respectively. The final simplifying assumption is that the trap states occur very near the intrinsic Fermi level ($E_t{\approx}E_i$). By assuming the traps occur approximately in the middle of the bandgap, the cosh() term goes to 1 which means the denominator $2n_i$ is insignificant. Rewriting the expressions for the carrier concentrations $n = n_0 + n'$ and $p = p_0 + p'$ where n_0 and p_0 are the equilibrium carrier concentrations and n' and p' are the generated electron pairs, it is possible to simplify Eq. 19 into Eq. 20.

$$U = R_{th} - G_{th} = \frac{pn - {n_i}^2}{\left[p + n + 2n_i\cosh\left(\frac{E_t - E_i}{kT}\right)\right]\tau_0} \tag{19}$$

$$U = \frac{n'}{\tau_0} \tag{20}$$

This result for the recombination rate can be substituted into the ambipolar transport equations resulting in Eqs. 21 and 22. Considering the results of these equations in the quasi-neutral regions under steady state, most of the terms go to zero as the quasi-neutral region is assumed to have no drop in potential. Additionally, in steady state there is no change in the number of carriers with respect to time therefore the derivative is zero. This result leaves only two terms in the equation, producing a simple ordinary differential equation (ODE).

$$\cancelto{0}{\frac{\delta n}{\delta t}} = \cancel{\mu_n n(x) \frac{\delta E(x)}{\delta x}}^{0} + \cancel{\mu_n E(x) \frac{\delta n(x)}{\delta x}}^{0} + D_n \frac{\delta^2 n(x)}{\delta x^2} - \frac{n'}{\tau_0} \tag{21}$$

$$\cancelto{0}{\frac{\delta p}{\delta t}} = \cancel{-\mu_p p(x) \frac{\delta E(x)}{\delta x}}^{0} - \cancel{\mu_p E(x) \frac{\delta p(x)}{\delta x}}^{0} + D_p \frac{\delta^2 p(x)}{\delta x^2} - \frac{p'}{\tau_0} \tag{22}$$

The general solution for an ODE of the form: $f''(x) = \frac{f(x)}{C}$ is an exponential of the form $f(x) = Ae^{\frac{x}{\sqrt{C}}} + Be^{-\frac{x}{\sqrt{C}}}$. This result is seen in Eq. 23. There are two common cases used to find a particular solution. The two extremum cases of short-base and long-base diodes impinge different boundary conditions upon the problem. The first case assumes that the quasi-neutral region is longer than the diffusion length of the diode. For this case under forward bias, p' and n' have gone to zero due to recombination well before the ohmic contacts (x_{cn}) and ($-x_{cp}$) as seen in Figure 12.

$$\begin{aligned} p'_n &= Ae^{\frac{x-x_n}{\sqrt{D_p \tau_0}}} + Be^{-\frac{x-x_n}{\sqrt{D_p \tau_0}}} \\ n'_p &= Ae^{\frac{x-x_p}{\sqrt{D_n \tau_0}}} + Be^{-\frac{x-x_p}{\sqrt{D_n \tau_0}}} \end{aligned} \tag{23}$$

The minority carrier concentrations at the depletion region edges under equilibrium and bias conditions are given by the Eqs. 24 and 25 from Ref [39], where ϕ_i

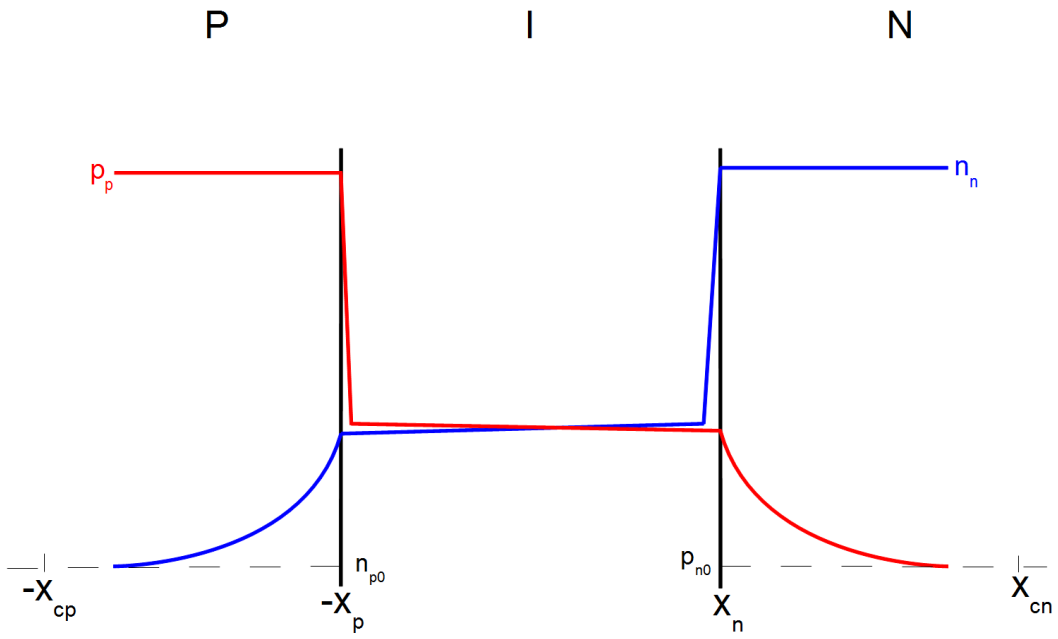


Figure 12. The electron hole concentrations across diode while forward biased.

is the equilibrium internal potential of the diode such that $\phi_i = \phi_n - \phi_p$ and V_a is the externally applied bias as previously described. These can then be used to solve for the excess carrier densities at the boundary edges in Eq. 26. These results will be used to enforce the boundary condition of the excess carrier concentrations at the depletion region edges in order to find the particular solution to the diode current.

$$\begin{aligned} n_{p0}\left(-x_p\right) &= N_d e^{\frac{-q\phi_i}{kT}} \\ p_{n0}\left(x_n\right) &= N_a e^{\frac{-q\phi_i}{kT}} \end{aligned} \tag{24}$$

$$\begin{aligned} n_{p0}\left(-x_p\right) &= N_d e^{\frac{-q(\phi_i - V_a)}{kT}} \\ p_{n0}\left(x_n\right) &= N_a e^{\frac{-q(\phi_i - V_a)}{kT}} \end{aligned} \tag{25}$$

$$\begin{aligned} n'_{p0}\left(-x_p\right) &= N_d \left[e^{\frac{qV_a}{kT}} - 1\right] \\ p'_{n0}\left(x_n\right) &= N_a \left[e^{\frac{qV_a}{kT}} - 1\right] \end{aligned} \tag{26}$$

With both boundary conditions known, the exact solution for the excess carrier con-

centrations in the quasi-neutral regions of the diode is given in Eq. 27.

$$\begin{aligned} n_p'(x) &= n_{p0}\left[e^{\frac{qV_a}{kT}}-1\right]e^{\left(\frac{x+x_p}{\sqrt{D_n\tau_0}}\right)} \\ p_n'(x) &= p_{n0}\left[e^{\frac{qV_a}{kT}}-1\right]e^{\left(-\frac{x-x_n}{\sqrt{D_p\tau_0}}\right)} \end{aligned} \tag{27}$$

Using this solution performed in the quasi-neutral region, the final dark current can be calculated from the area and current density equations seen in Eq. 28 which is also the commonly referenced solution for the dark current of an ideal diode [40].

$$\begin{aligned} I_d &= A\left(J_p+J_n\right) \\ &= A\left(-qD_p\tfrac{dp_n}{dx}+qD_n\tfrac{dn_p}{dx}\right) \\ &= A\left[qD_p\tfrac{p_{no}}{\sqrt{D_p\tau_0}}\left(e^{\frac{qV_a}{kT}}-1\right)e^{\frac{-x-x_n}{\sqrt{D_p\tau_0}}}+qD_n\tfrac{n_{po}}{\sqrt{D_n\tau_0}}\left(e^{\frac{qV_a}{kT}}-1\right)e^{\frac{x+x_p}{\sqrt{D_n\tau_0}}}\right] \\ &= Aq{n_i}^2\left(\tfrac{D_p}{N_d\sqrt{D_p\tau_0}}+\tfrac{D_n}{N_a\sqrt{D_n\tau_0}}\right)\left(e^{\frac{qV_a}{kT}}-1\right) \\ &= I_s\left(e^{\frac{qV_a}{kT}}-1\right) \end{aligned} \tag{28}$$

The second boundary value solution is solved under the short-base assumption that the ohmic contact is significantly closer to the depletion region edge than the diffusion length of the excess carriers as seen in Figure 13. This allows the general solution to the *ODE* in Eq. 23 to be estimated by the Taylor-Series expansion of an exponential. Using the first two terms of the expansion produces a linear solution in the form of Eq. 29. The boundary value at the depletion region edge is the same as in the long case, while the other boundary value is zero at the ohmic contact locations x_{cn} and $-x_{cp}$, recalling that $x_{cp}-x_p \ll \sqrt{D_n\tau_0}$ and $x_cn-x_n \ll \sqrt{D_p\tau_0}$. This results in the particular solution for the excess carrier concentration shown in Eq. 29. This solution is again used to calculate the current in the junction resulting in Eq. 30.

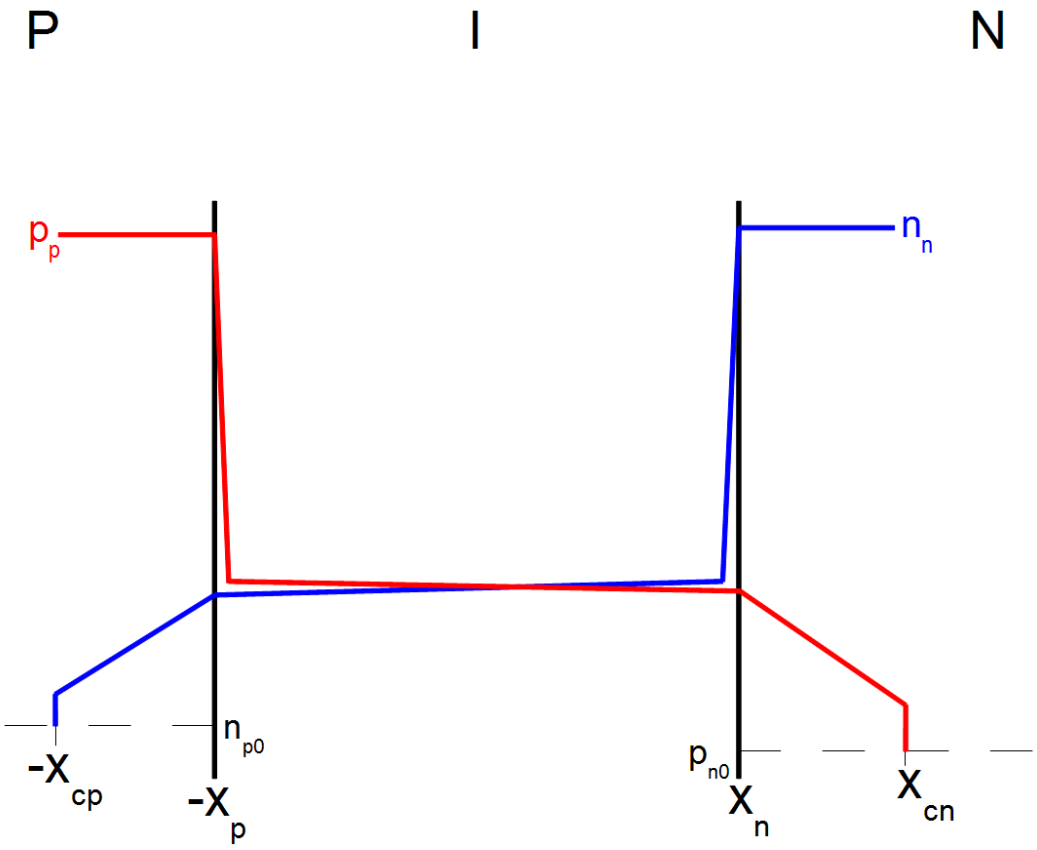


Figure 13. The electron and hole concentration across the diode while forward biased.

$$\begin{aligned} p_n' &= A_1 + B_1 \tfrac{x-x_n}{\sqrt{D_p \tau_0}} \\ n_p' &= A_1 + B_1 \tfrac{x+x_p}{\sqrt{D_n \tau_0}} \end{aligned} \tag{29}$$

$$\begin{aligned} I_d &= A\left(J_p + J_n\right) \\ &= A\left(-qD_p \tfrac{dp_n}{dx} + qD_n \tfrac{dn_p}{dx}\right) \\ &= A\left[qD_p \tfrac{p_{no}}{x_{cn}-x_n}\left(e^{\frac{qV_a}{kT}} - 1\right) + qD_n \tfrac{n_{po}}{x_{cp}-x_p}\left(e^{\frac{qV_a}{kT}} - 1\right)\right] \\ &= Aq{n_i}^2\left(\tfrac{D_p}{N_d(x_{cn}-x_n)} + \tfrac{D_n}{N_a(x_{cp}-x_p)}\right)\left(e^{\frac{qV_a}{kT}} - 1\right) \\ &= I_s\left(e^{\frac{qV_a}{kT}} - 1\right) \end{aligned} \tag{30}$$

While these solutions for the ideal diode do approximate the dark steady state behavior, they fail to address recombination which occurs in the depletion region. The approximations have assumed all injected carriers successfully traverse the depletion region. Due to the strain generated from the epitaxial growth of Ge on Si, there will be defects in the device which generate recombination centers in depletion region. The recombination in the depletion region is shown in Eq. 31 by replacing $pn = {n_i}^2 e^{\frac{qV_a}{kT}}$ in Eq. 19 [39].

$$U = \frac{{n_i}^2\left(e^{\frac{qV_a}{kT}} - 1\right)}{\left[p + n + 2n_i \cosh\left(\frac{E_t - E_i}{kT}\right)\right]\tau_0} \tag{31}$$

This equation is used to generate an upper limit on the ideality factor (n_e), which is sometimes known as the emissivity factor. It is obvious that the maximum recombination occurs where the denominator is at a minimum. The first derivative of the denominator with respect to p gives a critical point where $p = e^{\frac{qV_a}{2kT}}$ with a positive second derivative. By the concavity theorem this critical point is a minimum. Substituting the minimum value for the carrier concentration p, it is found that the maximum recombination occurs where $p = n = e^{\frac{qV_a}{2kT}}$. This modifies the boundary condition originally used to solve for the current across the diode, producing Eq. 32 for a non-ideal diode where n_e is a value between 1 for an ideal diode and 2 for a

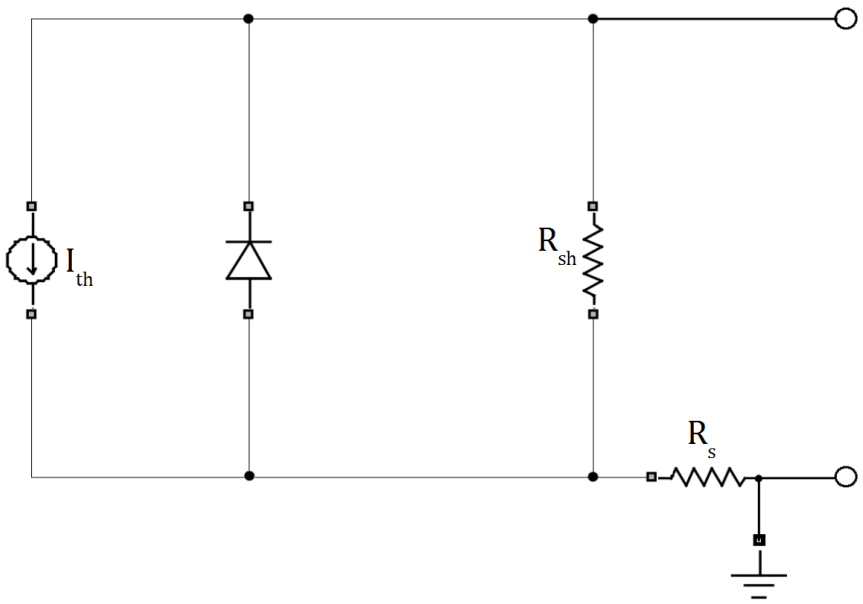


Figure 14. The device equivalent circuit under dark conditions.

generation recombination limited junction.

$$I = I_s \left(e^{\frac{qV_a}{nekT}} - 1 \right) \tag{32}$$

Although the behavior of the *pin*-junction has been solved, the device itself is often modeled as an equivalent circuit due to the necessary contacts and vias. These electrical connections are inevitable components of the device, and their behavior can not be decoupled from the *pin* junction. Figure 14 shows the equivalent circuit model using the non-ideal diode previously derived. For this circuit R_{sh} is the shunt resistance which is ideally infinite, however using finite values it is used to capture the leakage current of the diode. Leakage current is current which is permitted to flow around the device through the dielectric cladding. The series resistance R_s is the sum of the contact resistance and internal resistance of the diode. This value is ideally very small to reduce Joule heating in the device. Equation 33 describes

the equivalent circuit dark current model. The temperature dependence is often included after measurement of the I_s parameter at a static temperature defined as T_{nom} to produce Eq. 34 from [41]. The final thermal parameter is the saturation current temperature exponent (p_t). It is a fitting parameter used when modeling the temperature dependence of devices, for diodes it is typically modeled with a value near three. The results of this model and the effects of each of the parameters on device performance can be seen in Figure 15. While temperature and shunt resistance are shown to have the greatest effect on dark current for this model, series resistance will have a significant impact on the CW performance of the device as it contributes to the optical power damage threshold for the detector. If to much current is generated within the diode, Joule heating due to the series resistance can thermally damage the device.

$$I_d = I_s \left(e^{\frac{R_s(V_a - I_d R_s)}{n_e k T}} - 1 \right) + \frac{V_a - I_s \left(e^{\frac{R_s(V_a - I_d R_s)}{n_e k T}} - 1 \right) R_s}{R_{sh}} \tag{33}$$

$$I_s(T) = I_s(T_{nom}) \left(\frac{T}{T_{nom}} \right)^{\frac{p_t}{n_e}} e^{\frac{-qE_g}{kT}\left(1 - \frac{T}{T_{nom}}\right)} \tag{34}$$

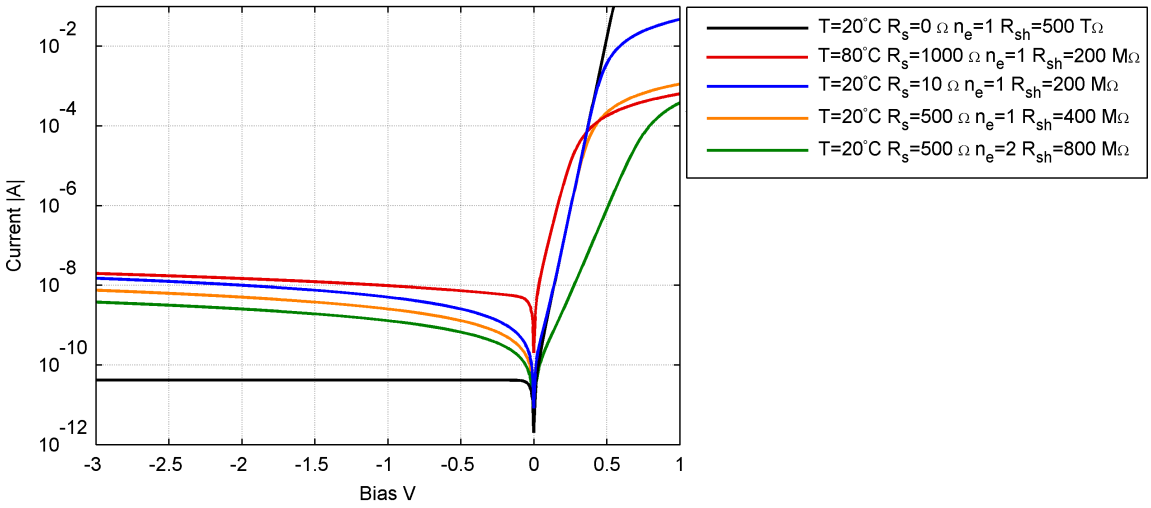


Figure 15. Effects of equivalent circuit parameters on device performance.

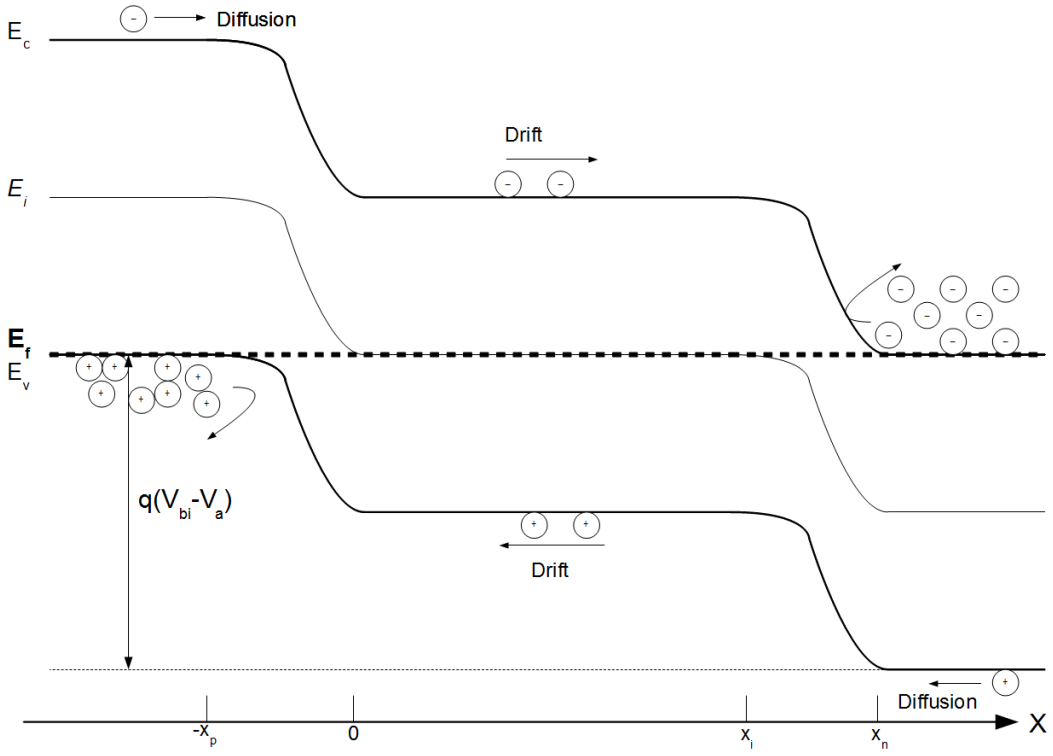


Figure 16. Carrier transport of *pin* diode in under illumination.

2.2.1.2 Photocurrent, Quantum Efficiency and Responsivity.

Extrapolating the established model from the dark current section provides the photodiode's response when light is impingent upon the device. The photo-generated current is derived by adding an optical generation term to the ambipolar transport Eqs. 17 and 18. The new generation term G_{rad} is based on the Beer–Lambert Law and is approximated in Eq. 35 where r is the reflectivity between the Si waveguide and Ge detector, Φ_0 is the incident photon flux, and α is the wavelength-dependent absorption coefficient of the Ge Ref [42].

$$G_{rad} = (1 - r)\,\Phi_0 \alpha\,(\lambda)\, e^{-\alpha(\lambda) z} \tag{35}$$

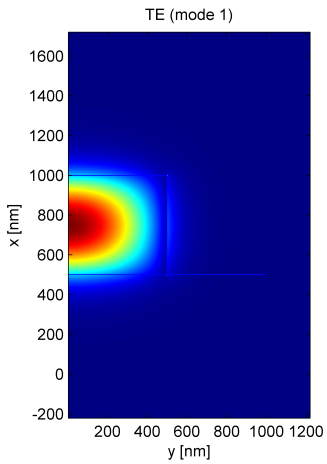


Figure 17. Simulation of the optical field inside the detector [43].

The simplest method sums the photocurrents generated in the three sections of the photodiode as shown in Figure 16. The first two are the diffusion currents of the minority carriers toward the depletion region on the n- and p-doped sides of the diode. The third region is defined by the drift current across the depletion region. The two diffusion currents in the quasi-neutral region can be nearly discounted due to the waveguide nature of the detector. The optical mode of the detector in the x-direction is primarily confined to depletion region. Additionally, the quasi-neutral regions are frequently kept as small as possible to avoid diffusion limiting the detector's bandwidth.

The depletion region current then is simple to solve as it assumes all carriers generated are rapidly swept out of the depletion region by the large reverse-biased electric field. Once they are swept out they become majority carriers where they contribute to the photo-generated current. This means integrating the generated carriers over the depletion region as shown in Eq. 36. Where W and L are the respective y and z dimensions of the fabricated device while w' is the depletion region width previously defined as x_n+x_p. Due to the waveguide structure of the photodiode,

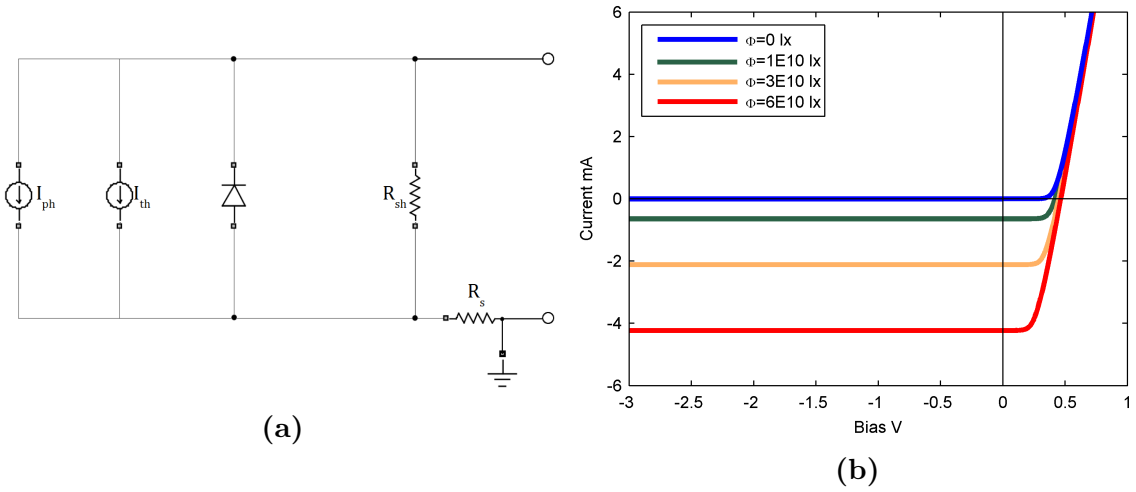


Figure 18. (a) Model equivalent circuit under illumination conditions. (b) Simulated results based on equivalent circuit model.

the incident number of photons Φ is the integral over the cross sectional area of the diode exposed to this optical field. A simulation of the field for Φ_0 inside the detector can be seen in Figure 17 This means that $\Phi = \int_{-W/2}^{W/2} \int_{-x_p}^{x_n} \Phi_0 (x, y)\, \mathrm{d}x\mathrm{d}y$ This resultant photocurrent of Eq. 36 is added to the dark current equivalent circuit $I = I_d + I_{ph}$ to produce the final CW model and response of a photodetector in Figure 18. The drop in potential across the series resistance is what pulls back the knee of the diode turn-on voltage when operating under short-circuit mode. It is clear when operating under a sufficient reverse bias, linear changes in the input optical power (photon flux) will result in a linear shift of the diode's output current. This is the basic premise behind optical photo detection.

$$\begin{aligned} I_{ph} &= -q \int_0^L \int_{-W/2}^{W/2} \int_{-x_p}^{x_n} G_{rad}\, \mathrm{d}x\, \mathrm{d}y\, \mathrm{d}z \\ &= -q\,(1-r) \int_{-W/2}^{W/2} \int_{-x_p}^{x_n} \Phi_0\, \mathrm{d}x\, \mathrm{d}y \left(1 - e^{-\alpha(\lambda)L}\right) \\ &= -q\,(1-r)\,\Phi \left(1 - e^{-\alpha(\lambda)L}\right) \end{aligned} \tag{36}$$

From the identification of the photocurrent, the efficiency of this optical-to-electrical

(OE) conversion becomes important. The quantum efficiency η of the photodiode describes how efficiently the absorbed photons contribute to the photocurrent. This means that quantum efficiency of the photodiode is described by Eq. 37. Quite often for commercial detectors the quantum efficiency of the photodiode is assumed to be unity. In this case every absorbed photon contributes to the photocurrent.

$$\eta = \frac{I_{ph}}{q\Phi\left(1-r\right)} \tag{37}$$

The quantum efficiency is not a quantity which can be directly measured, however the commonly cited figure of merit, responsivity, is directly related to the quantum efficiency of the diode. The responsivity is simply the photocurrent divided by the input optical power. Therefore, the responsivity can be written as Eq. 38. It should be noted that both the responsivity and the quantum efficiency are wavelength-dependent. The absorption coefficient in the $e^{-\alpha \cdot L}$ term is a wavelength dependent property of the material in which the detector was fabricated. This absorption dependence on wavelength can be seen in Figure 19 for several materials. It should be readily apparent why Ge was selected as the epitaxial detector material for integration with Si. Its absorption coefficient extends to the telecommunication wavelengths of 1550 nm, beyond where Si detectors are responsive. The responsivity has a second wavelength-dependent parameter as it is divided by the frequency, ν, of the incident optical power. Therefore the responsivity is dependent upon two competing terms each associated with the wavelength. This developed model provides an estimate for the behavior of the device under steady state operating conditions.

$$R = \left|\frac{I - I_d}{P_{in}}\right| = \left|\frac{I_{ph}}{P_{in}}\right| = \frac{q\eta}{h\nu} \tag{38}$$

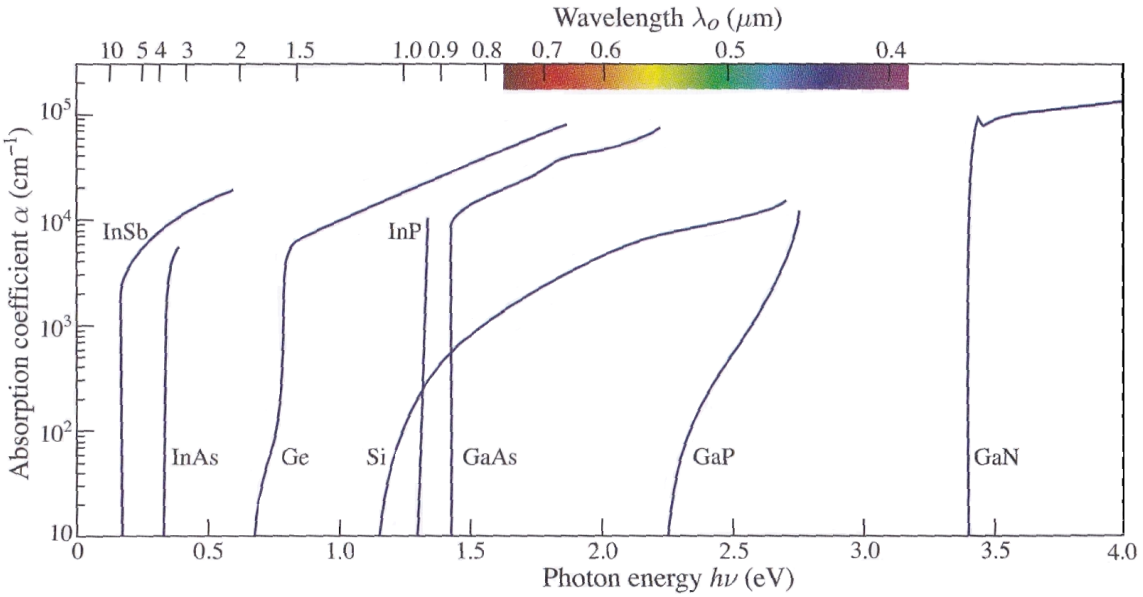


Figure 19. Wavelength dependent absorption coefficient values for various semiconductor materials. [44]

2.2.2 RF Photodiode response.

With an understanding of how the photodiode is able to detect changes in optical intensity and its importance as an optical receiver, it becomes critical to realize the limitations on the device's operating performance over various data rates or bandwidths. The *RF* response is a measurement associated with the bandwidth of the detector. It is a measure of the power transmitted by the device at each frequency.

The first limitation on the bandwidth of such devices comes from the so-called RC time constant. This term is the sum of the load and series resistance multiplied by the sum of the junction and parasitic capacitance. The parasitic capacitance C_p arises from the electrical connections necessary to connect to the device. As a result, C_p is determined by both the design and fabrication considerations at the foundry. Great care is taken to reduce this value as much as possible. The junction capacitance as the name implies arises from the nature of a *pin* junction. Under reverse bias, charge carriers build up on both sides of the depletion region. The junction capacitance can

then be obtained by taking the derivative of the change in charge with respect to bias as seen in Eq. 39, where x_n is the value obtained from Eq. 12.

$$\begin{aligned} C_j &= A\frac{\mathrm{d}Q}{\mathrm{d}V_a} \\ &= AqN_a\frac{\mathrm{d}x_n}{\mathrm{d}V_a} \\ &= \frac{A\epsilon_s}{\sqrt{{x_i}^2+\frac{2\epsilon_s(N_a+N_d)}{qN_dN_a}(V_{bi}-V_a)}} \end{aligned} \tag{39}$$

The results of this capacitance demonstrate that the junction capacitance can then be calculated using the standard equation for a parallel plate capacitor Eq. 40. This is because the denominator is equal to the depletion region width from Eq. 13. With the junction capacitance known, the RC time constant is defined by $\tau_{RC} = RC$ where $C = C_p + C_j$ and $R = R_s + R_l$. The model for this complete equivalent circuit RF device can be seen in Figure 20. Under CW conditions the model returns to Figure 18a as the capacitive terms act as "opens" and can be ignored.

$$C_j = \frac{A\epsilon_s}{w'} \tag{40}$$

The second factor influencing the bandwidth of the detector is carrier transport time. This time τ_{tr} is the time it takes for carriers to be collected from the absorption region of the photodiode. As light impinges on the diode it takes time for the generated carriers to drift across the depletion region thus adding another limiting term to the bandwidth. Although neither carrier type is instantaneously fast, holes are the significantly slower carrier having about half the mobility of electrons in Ge. This means holes will be the limiting factor for carrier travel time in the device. The

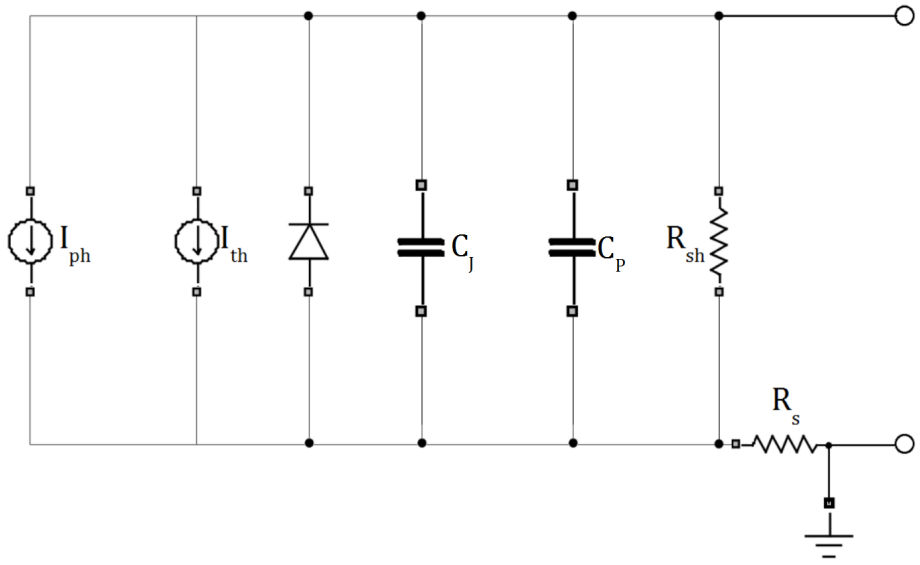


Figure 20. Equivalent circuit model for *RF* performance of an integrated photodiode.

travel time of the holes is based upon the drift current and is shown in Eq. 41.

$$\tau_{tr} = \left(\frac{E\left(x\right)\mu_p}{w'} \right)^{-1} \tag{41}$$

These two factors limit the carrier transport time thus reducing the bandwidth. The 3-dB bandwidth, or the frequency at which half of the low-frequency power is transmitted, is commonly referenced as Eq. 42 Ref. [40]. The total effect of these time constants can be seen in the Bode plot of Figure 21. In order to operate well into GHz frequencies, typically both the time constants must be less than 1 ps.

$$\Delta f = \left[2\pi\left(\tau_{tr} + \tau_{RC}\right)\right]^{-1} \tag{42}$$

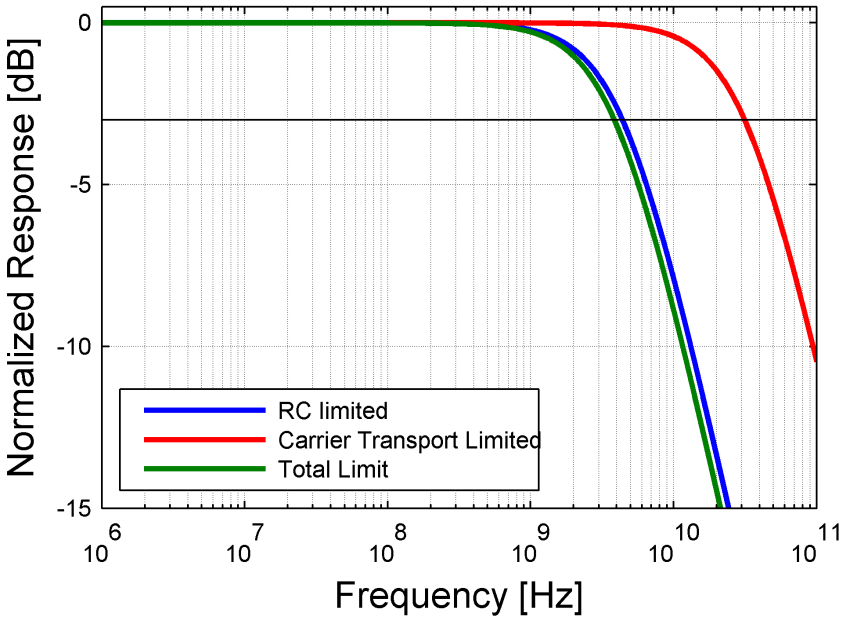


Figure 21. The overall bandwidth performance based on the *RF* equivalent circuit model.

2.3 Application

This basic model provides an understanding of the device operation. This will permit the analysis of the photodiode's performance metrics with an understanding of the underlying principles behind its operation. By using this model understanding of the reasoning behind device's performance can be gleaned from the characterization and results chapters of this thesis.

III. Characterization

With an understanding of the foundational performance metrics of photodiodes and their physical origins, it becomes important to characterize actual devices in an effort to maximize their performance. This allows one to assess both the potential efficacy of the device in a system, as well as analyze possible advancements or issues which must be addressed to improve the design or manufacture. This chapter will cover the testing procedures and equipment used for the characterization of vertical stack epitaxially grown Ge on Si integrated waveguide photodetectors.

3.1 Test Fixtures and Equipment

The difficulty associated with making repeatable measurements can only truly be understood after one works in a laboratory environment, and encounters all of the variability associated with even the most basic of measurements. Measurement reliability is achieved through the use of proper equipment suited to each measurement. Additionally, a stable testing platform should provide repeatable results by holding as many environmental parameters as possible constant from test to test. However, a very rigid structure trades some flexibility in measurement. The device testing platform described in this section attempts to strike an optimal balance between these trade-offs.

While the original test infrastructure was used for the initial testing of devices during this thesis work, there were some non-ideal limitations associated with its design. These issues were addressed in the design of a new generation of test fixtures to aid in data collection. The original first-generation design can be seen in Figure 22. While it provided an excellent starting point it suffered thermal runaway when the thermo-electric cooler (TEC) was set to either temperature extreme. The fixture was

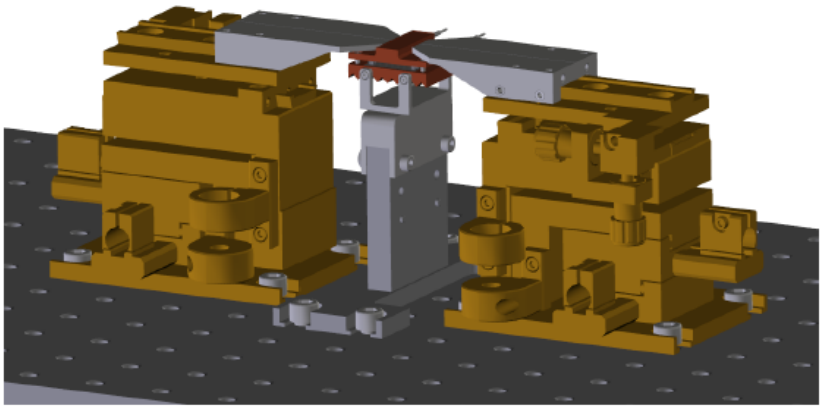


Figure 22. First generation legacy fixturing for integrated device testing [45].

also prone to shift the position of the sample under test by several μm per 5 °C, an unacceptable mechanical movement for optical waveguides which are approximately 200 nm by 400 nm. Finally, the ability to align the input and output fibers to the full dimension of the chiplet was limited by the translation range of the fiber positioners.

The first issue addressed was the limited motion of the fiber positioners. They did not have sufficient range of motion to scan the entire lateral dimension of the chiplet, which meant they had to be physically moved along the table and completely realigned before measurements could be taken again. This was addressed through the acquisition of newer model 562 positioners, which have replaced the older 561-model positioners. Additionally, the 562 positioners are designed with greater thermal invariance to environmental changes therefore they maintain superior alignment. The second-generation system without the fiber holding mounts can be seen in Figure 24. They were not redesigned as they seemed to maintain good performance in stably holding the fibers.

Nevertheless, thermal management concerns were the main reason the custom mounts were designed. *Ge* photodiodes have a strong temperature dependence due to their narrow bandgap and therefore need be characterized without variation in lat-

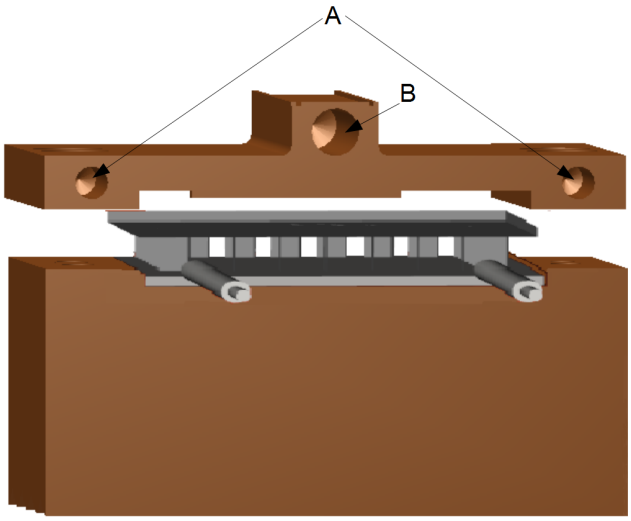


Figure 23. Second generation mounting designed to reduce thermal movement of the device and avoid thermal runaway of the heat sink. (A) shows the tapped holes used to attach the plate to the mounting bracket. A thermister was placed within (B) in order to approximate the lattice temperature of the device under test.

tice temperature. While the ambient temperature typically remains fairly consistent in the lab, during seasonal changes the temperature in the laboratory varies by +/- 5°C due to the building's poorly controlled heating, ventilating, and air conditioning (*HVAC*) system. This means it would be ideal to hold the temperature of the chip constant between testing. This can be done by utilizing the temperature feedback-control loops in laser diode controllers. In the mount design a hole was milled laterally into the chip mount plate to accommodate a thermistor. This design with the thermistor hole, (labeled B), as well as the *TEC* can be seen in Figure 23. The use of a thermistor allows the temperature at the boundary of the chip and copper plate to be reasonably estimated. This information is then used to drive a feedback-control loop to apply or reduce current to the *TEC*. This current feedback control maintains the set temperature for the top mounting plate. The temperature control of the *TEC* arises from its ability to sink heat from the chiplet mount into a heat sink where it can be radiatively and conductively released back into the environment. This heat

sinking lead to several problems associated with the first-generation design of the original test system.

The first problem was the size of the heat sink in comparison to the amount of heat that needed to be dissipated. Figure 22 shows that the heat sink was about the same size as the top plate; far too small to meet the heat dissipation requirement. A second issue was exacerbated by the first. Conducting metal screws were used to hold the mounting plate and heat sink together, sandwiching the *TEC* between the two. As the heat sink became hot, as it did not have enough thermal mass to remain near room temperature, heat would begin to flow through conducting screws back into the chiplet mounting plate. This generated a thermal runaway condition which would trip the current limit on the *TEC* feedback loop. The use of a heat sink with a much larger thermal mass and ceramic screws to reduce thermal conduction through the plates alleviated the majority of these issues.

The final issue related to the assembly of the original mounts. While the temperature of the top plate remained the same, the bottom plate was constantly changing due to the aforementioned reasons. This meant that the heat sink was expanding and contracting. Unfortunately it was pinned to the mounting bracket therefore it would remain stationary, however, The mounting plate was left to float and thus would move with changes in the temperature due to the linear expansion or contraction of the heat sink. The second-generation mount bracket was pinned to the top plate by the threaded holes labeled A in Figure 23, rather than the heat sink, and thus chip remained stationary if the temperature was held constant. The design for all of these modifications can be seen in Figure 24, along with the realization of this final design in Figure 25.

In Figure 25 the probing set up can be seen along with fiber launch platforms. The devices tested were fabricated with ground signal ground (*GSG*) *RF* probe pads

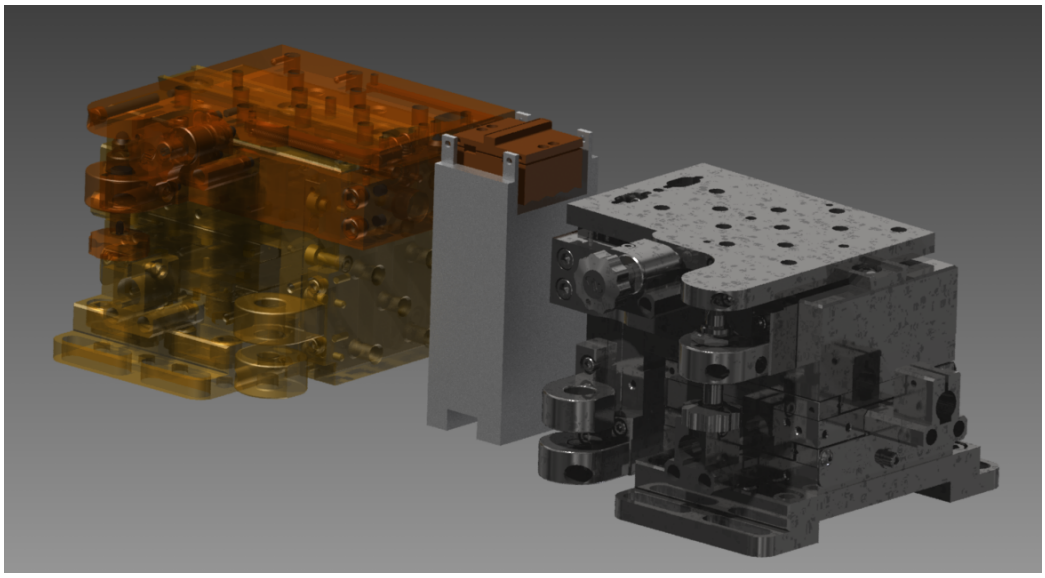


Figure 24. Second generation fixturing designed for greater flexibility and stability.

utilizing a 100-μm pitch, therefore the appropriate *RF* 50-GHz probes were used for testing whenever possible. Additionally, 2.4-mm cabling was used to carry the signal from the probe tip to the external measurement equipment. *DC* probes were substituted for the *RF* probes during the CV measurement. A break-out box was assembled for the use of the *RF* probes during testing, but the inside of the box was unshielded and did not allow for the measurement of device capacitance below 90 nF during the CV measurements. The final system set-up also includes lensed fibers for coupling into the optical guiding structures of the chip. Lensed fibers focus the fiber's optical mode into the waveguide in order to better match the mode of the on-chip waveguide, thus reduce the insertion loss. Although high numerical aperature (*NA*) fiber has the potential to reduce insertion loss further, it was unavailable at the time of this work.

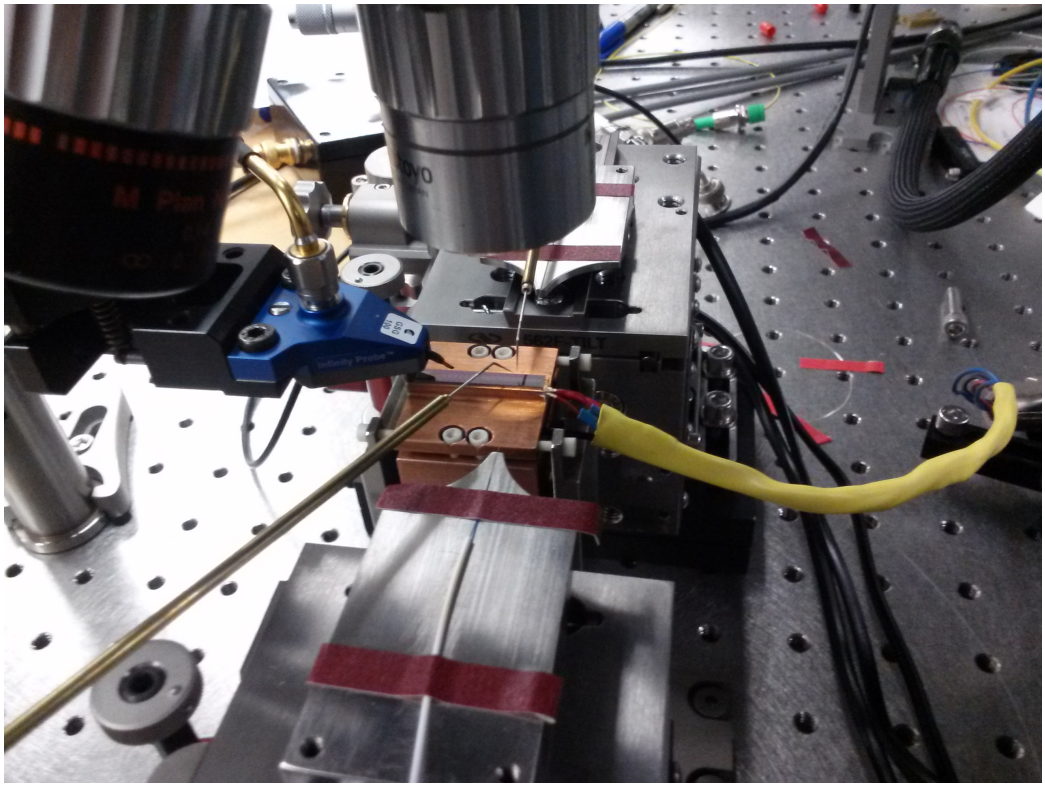


Figure 25. Physical realization of the design for a thermally stable mount platform designed for use with integrated photonics.

3.2 Electronic Characterization

The electronic characterization of the integrated photodetectors was accomplished through the measurement of dark current and parasitic capacitance while using the stable testing platform previously described. Great care went into the identification and selection of proper lab equipment for the measurement of the performance metrics in such small-scale integrated devices, where the opportunity for error is always present.

3.2.1 Dark Current.

With the small size of the devices tested, a very precise piece of equipment is required in order to measure dark current values of a single nA while providing a fixed DC voltage across the junction. This can be done using a voltage source and a digital multi meter (DMM) to apply a bias and measure the drop in voltage across a known load. However, with very low currents, a large resistor is required in order to have the resolution to measure the very small changes in current flowing through the resistor. This is not ideal as this large resistor would be in series with the device and would cause problems with the test measurement of photocurrent. The main problem is the large drop in potential across this series resistance. This will in turn move the set bias voltage on the detector changing where on the IV and LIV curves each measurement point is taken. In order to work around these issues a system source meter (SMU) was used for dark current testing. The use of a SMU allows for the short-circuit measurement of the diode's IV characteristics. This provides the electronic performance of the junction which can be used to back out the equivalent circuit parameters of the device.

The accuracy of the measurement, especially for low dark currents, is generated by suppressing noise currents from the many potential sources such as various other

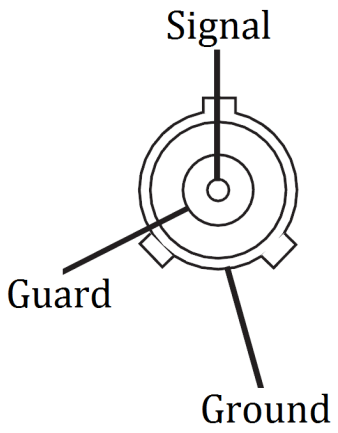


Figure 26. The components of a triaxial cable allowing for low noise current measurements.

lab equipment on the optical table. To achieve this accuracy, the *SMU* requires both a high and low potential port for inputs using triaxial cables rather than a single Bayonet Neill–Concelman (*BNC*) cable in order to suppress these noise currents. This provides electro-magnetic interference (*EMI*) protection for both paths of the signal. While two *BNC* cables could be used to transmit the low and high signals to the measurement equipment they add potential eddy noise currents to the measurement as potential is dropped between the signal pin and the ground sheath of the cable. Triaxial cabling avoids this drop in potential by including a guard as shown in Figure 26 which is at the same potential as the signal pin. This means that no current will flow from the signal pin to the guard avoiding measurement noise generated within the cabling.

As stated earlier the measurement setup used *GSG RF* probes to contact the device under test (*DUT*). The *RF* cabling used for the connection of *RF* probes precluded directly connecting the *DUT* using the triaxial cables required for the *SMU*. For this reason a break-out box was assembled in order to interface between

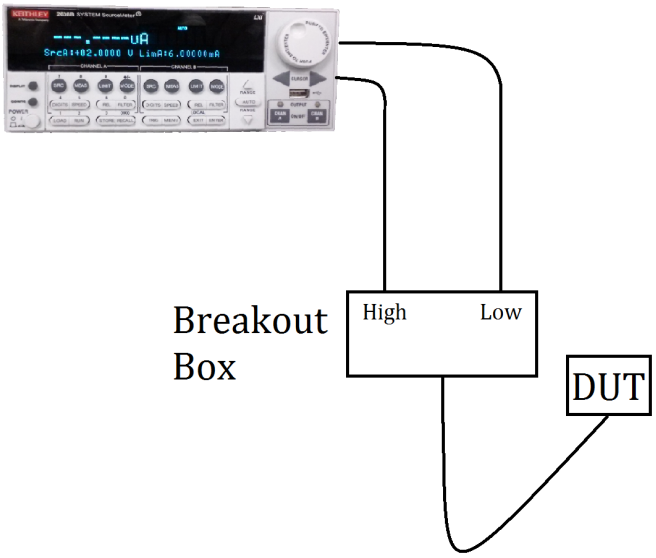


Figure 27. Dark current was measured using an *SMU* with an additional break out box to facilitate connection to an RF probe.

the output of a single *RF* cable and the requisite low- and high-port triaxial cables which connect to the SMU. The measurement set up for dark current can be seen in Figure 27. It should be pointed that electrical signals will be depicted using black lines while optical signals will be shown using blue lines in the remainder of this thesis.

In order to use the results of the dark current measurements to back out system parameters of the junction, code was written to fit the dark current equivalent circuit model parameters to the measured IV relationship. This fit gives a good estimate of the ideality factor n_e, the series and shunt resistance R_s and R_{sh}, and the saturation current I_s for the device. These parameters were used to evaluate the electronic properties of the photodiode.

3.2.2 Capacitance.

The measurement of the bandwidth robbing capacitance of the device, just like the dark current measurement, is not trivial. While laboratory approaches have been developed to determine the sum of the junction and parasitic capacitances, the very small capacitances encountered in high-bandwidth integrated optical detectors makes them exceedingly difficult to measure. Some have used the detection of a small signal sinusoidal phase shift across the junction and series resistor in order to back out the capacitance at several biases using Eq. 43, where ϕ is the observed phase difference between the signal on the resistor and the signal across the junction, f is the frequency of the applied signal, $\tilde{v}_r$ is the magnitude of the voltage across the series resistance (R_m), and finally $\tilde{v}_{junction}$ is the magnitude of the voltage across the junction [46]. While this measurement technique is sufficient for higher capacitance junctions having nF of capacitance, it is not feasible for integrated high-bandwidth *pin* devices which strive for sub 10-fF capacitances. These low capacitance structures allow devices to maintain GHz operating bandwidths. This measurement therefore precludes simple laboratory testing of the capacitance of the devices using oscilloscopes.

$$C = \frac{\sin(\Delta\phi)}{2\pi f} \frac{\tilde{v}_r}{R_m \tilde{v}_{junction}} \tag{43}$$

Another specialized piece of equipment known as an inductance, capacitance, and resistance (LCR) meter, must be used to identify the capacitance of such junctions. While the general method is similar, this piece of equipment permits measurements of aF of capacitance by assuming one of several impedance calculation models for the DUT. Additionally, it has internal feedback controls which permit the piece of equipment's superb measurement fidelity.

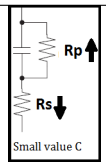
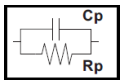
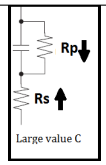
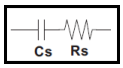
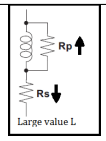
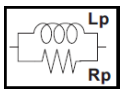
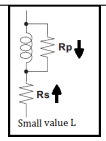
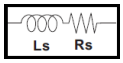
The first measurement taken on the device is the impedance which is given by

Eq. 44. The impedance is broken into a real and an imaginary part given by the resistance R and the reactance X respectively. The LCR meter actually measures the magnitude of the impedance and phase change through the DUT; this relates to the phaser model seen in the second half of Eq. 44. This allows the selection of the correct equivalent circuit from Table 1. There are two equivalent circuit models to choose from which will represent parasitics of a modeled device. Using the value from the impedance measurement the second column identifies what equivalent circuit and measurement mode the LCR meter should be placed in. These measurement modes and their associated reduced equivalent circuit are shown in columns three and four. The capacitance is the parameter that limits the bandwidth of a junction, therefore while testing photodiodes it is typically assumed measurements will be from the top half of the table. Finally, the measurement selection of C_p is reassured by a typical measure of GΩ for the impedance of these integrated devices. This means that the testing of integrated photodiodes should be confined to the top row of Table 1.

$$Z = R + jX = |Z|\angle\theta \tag{44}$$

Once the measurement parameters are defined, the system must be calibrated. The LCR meter has its own built in correction system. This correction is designed to compensate for phase shift due to cabling as well as calibrate low- and high-impedance measurements with pre-measured corrections. As was already discussed, very low-capacitance structures such as integrated Ge photodiodes have very high impedance, this means that only the cable length and open circuit corrections are necessary for an accurate measurement of the capacitance. Short-circuit corrections are very important for accurate low-impedance measurements. The application of these correction factors can be seen in Eq. 45 where Z_o and Z_s are the open- and

Table 1. Selection of equivalent circuit type and measurement for *LCR* meter

Circuit Model	Functions	Impedance	Model Selection
	$Z \geq 10k\Omega$	C_p-D C_p−Q C_p-G C_p-R_p	
	$Z \leq 10\Omega$	C_s-D C_s-Q C_s-R_s	
	$Z \leq 10\Omega$	L_p-D L_p-Q L_p-G L_p-R_p	
	$Z \geq 10k\Omega$	L_s−D C_s−Q L_s−R_s	

closed-circuit correction factors respectively [47]. Using this equation it becomes apparent why the short-circuit impedance correction is not required for high-impedance measurements on photodiodes.

$$Z_{final} = \frac{1}{\frac{1}{Z_m - Z_s} - \frac{1}{Z_0}} \tag{45}$$

The now-calibrated LCR meter is then ready to begin taking data. To get an idea of the depletion region typically CV measurements are taken to identify how the depletion region changes with bias. The frequency of the sinusoidal signal is set as close as possible to the operating frequency of the device. The goal is to match the environment seen under operation. The high bandwidth nature of the photodiodes means that the ideal frequency for such measurements is ∼20 GHz, so the LCR meter is set to 2 MHz; the highest frequency at which the LCR meter can can operate due to the internal feedback control. The next measurement parameter to identify in the process is the signal voltage. The goal is to avoid disturbing the diode's depletion region width with the testing signal. If the changes in the applied signal are too large they will modulate the depletion region width. Therefore, the signal voltage should be kept as small as possible while still obtaining accurate measurements. This can be achieved by starting at a higher signal level and backing it down to the minimum value which produces stable results. This was found to be near 25 mV for the devices tested in this work. The testing set up is shown in Figure 28. Originally RF probes were used to make measurements, however the signal noise floor for the break-out box used with the LCR meter was above 90 nF. This required switching to the use of two DC probes to ensure accurate measurements below 10 fF. After changing to DC probes the lower measurement limit dropped to hundreds of aF. This permitted the accurate measurement of the photodiode's capacitance.

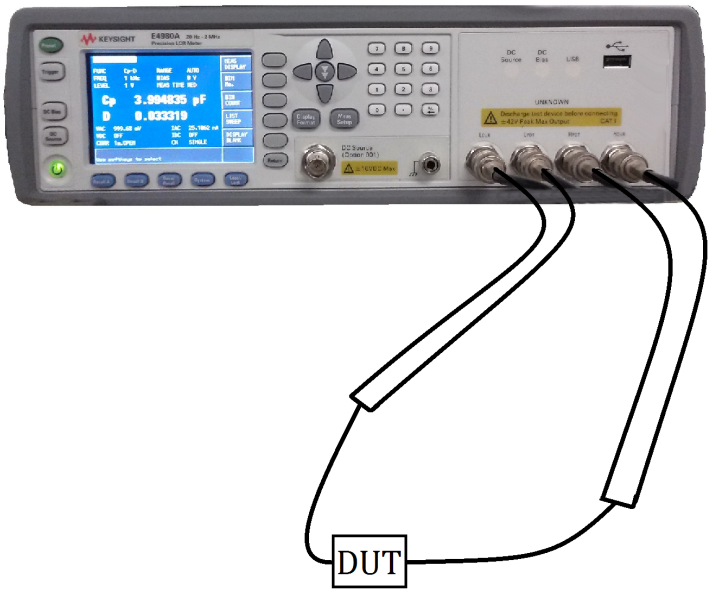


Figure 28. The experimental set up for measuring the parasitic capacitance of the *pin* photodiodes.

Figure 29. A microscope image of the alignment of the lensed fiber to the *Si* wire waveguide.

3.3 Optical CW Characterization

After the setup for the electronic characterization of a photodiode has been assembled, the *CW* optical characterization is quite simple. It involves an identical measurement technique with the exception that additional photo-generated carriers increase the current to the measurement equipment. The primary difficulty in these measurements is the fiber alignment which can be seen in Figure 29. There are many things which contribute to the losses associated with coupling into an integrated optical waveguide, including misalignment, surface reflections and modal mismatch between a circularly symmetric fiber and a rectangular waveguide. These losses do not affect the performance of the device and will be grouped into a single loss term known as the insertion loss.

While the insertion loss does affect the measurement of these devices, it can be decoupled from the detector response and used as a calibration term in the measurement of the devices. Using a waveguide which passes across the chip, the loss through the waveguide can be calculated by coupling into and out of the structure. With various waveguide lengths it also becomes possible to decouple the propagation loss from the insertion loss. For this chiplet fabrication run only one length of waveguide was

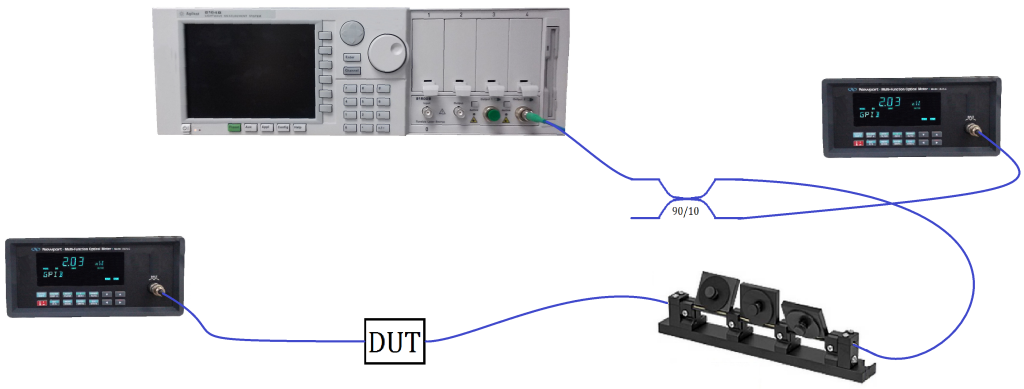


Figure 30. A representation of the insertion loss measurement setup using a tunable laser source to measure the wavelength dependent insertion loss of the *Si* waveguides.

fabricated, precluding the ability to separate these losses. Reversing the measurement is a check to ensure the input coupling and output coupling are approximately equal. As stated before, because the propagation loss could not be measured, this method assumes the waveguide losses to be zero and gathers all of the loss into input and output coupling. It is not possible to identify losses due to propagation through the waveguide without various length waveguides. However, with such short linear propagation distances on chip these losses will be greatly overshadowed by the coupling losses and are satisfactorily ignored. The insertion loss I_L can then be calculated using Eq. 46 where P_{launch} is the power launched from the lensed fiber and P_{tr} is the power received at the output fiber. The power incident on the optical detector P_{in} is then defined by Eq. 47. The experimental setup for determining the insertion loss can be seen in Figure 30

$$-I_L = \frac{1}{2} 10 \log_{10} \left(\frac{P_{tr}}{P_{Launch}} \right) \tag{46}$$

$$\begin{aligned} P_{in} &= P_{Launch} \cdot 10^{\frac{-I_L}{10}} \\ P_{in_{dB}} &= P_{Launch_{dB}} - I_L \end{aligned} \tag{47}$$

Additionally, the polarization must be aligned to the transverse electric (TE)-mode of the waveguide for optimal confinement in the wire waveguide structure. The circular symmetry of traditional fiber does not create a preferential polarized mode as rectangular waveguides do. Polarization maintaining optical fiber (PMF) is manufactured to achieve just such a result by building stress rods into the fiber. These induce birefringence within the fiber and generate a preferential polarization. The polarization dependence of the confinement of the optical field in an integrated Si wire waveguide can be seen in Figure 31. It should be noted that the modes are symmetric about the y-axis of the plot, however the units match the coordinate system of Figure 6. Unfortunately, it is extremely difficult to align a PMF to an on-chip waveguide while ensuring the proper polarization state is coupled to the on-chip waveguide. Therefore, an external polarization controller is used to stress the SMF fiber which causes birefringence in the Silica, rotating the polarization state of the confined mode. This effect is then used to rotate the polarization so that it is properly aligned when it is launched from the lensed fiber. However, this stress-induced polarization rotation is wavelength dependent. Nevertheless, this improper launch polarization-based loss can be calibrated out within the insertion loss measurement of the waveguides. P_{Launch} is calibrated by removing the DUT in Figure 30 and measuring the power which is launched from the polarization controller.

With a known launch power there are two responsivities to measure for the device, the wavelength-dependent responsivity and the power-dependent responsivity. This power dependence is referred to as the linearity of the device. The wavelength-dependent responsivity is the responsivity at each wavelength of incident light. This measurement has greater fluctuations in the collected current due to polarization state changes, however the wavelength-dependent losses due to the polarization state should be accounted for in the wavelength dependence of the insertion loss. The

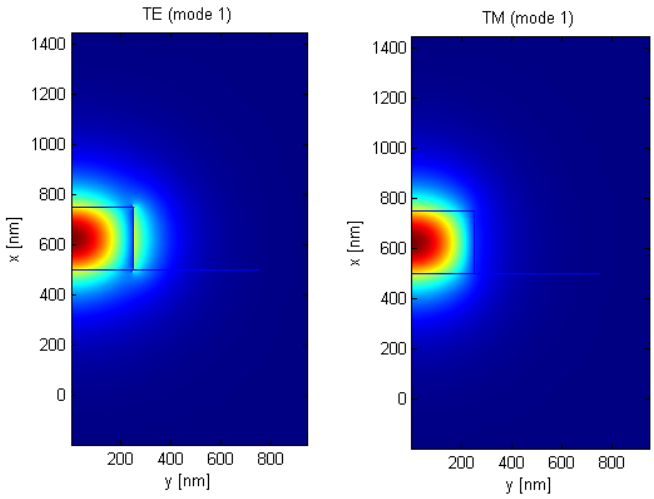


Figure 31. A simulation of the optical power distribution within the *Si* waveguide using [43].

experimental setup can be seen in Figure 32. The *DUT* is reverse biased using the *SMU* which is also used as the ammeter to record the sum of the dark current and generated photocurrent. The tunable source is swept across a range of wavelengths to identify the responsivity of the detector at each wavelength.

Most often the responsivity is not measured as a power dependent term as it is assumed to be constant for all incident optical power. This is not entirely true as detectors have saturation points were the absorbing material can become bleached and can no longer absorb incident photons. The power of the tunable laser source is far too low to reach the saturation point of the on-chip detectors, therefore a high-power distributed feedback (*DFB*) laser was used to characterize the power dependence of the devices. This measurement is performed at the fixed wavelength of the *DFB* while the photodiode is biased using the *SMU* just as in Figure 32. Additionally, the *SMU* bias is swept in order to generate the LIV curves of the device under incident optical power. These curves provide insight into the optimal bias to maximize responsivity and linearity.

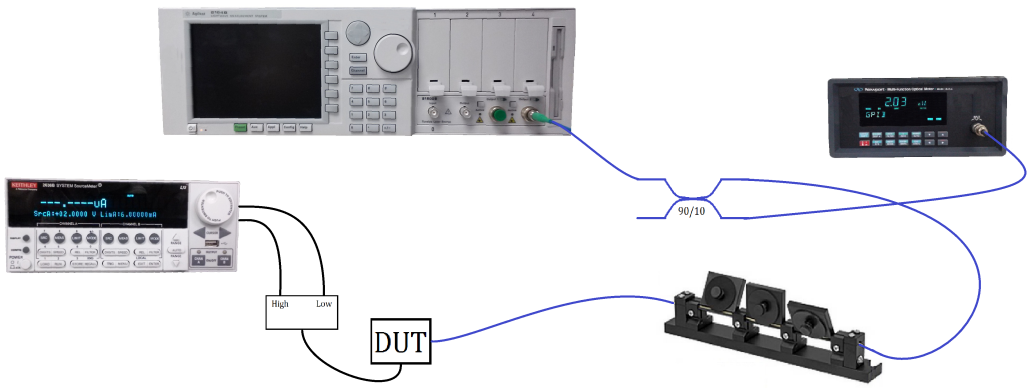


Figure 32. A representation of the responsivity measurement setup using a tunable laser source to measure the wavelength dependent response of the photodiode.

3.4 RF Response

The *RF* response of the photodiode characterizes the device's system level performance. The bandwidth of the slowest component defines the bandwidth limit of the entire system, and as stated in the introduction, increases in bandwidth can have a multiplicative effect on the system. The bandwidth for these photodiodes can be measured in two ways. The first method involves the use of a precision network analyzer (*PNA*), more commonly referred to as a vector network analyzer (*VNA*), to measure the S_{21} parameter of the device. While this method is very accurate and provides a large number of data points it suffers a large power loss to an already small signal when coupling onto the chip. The second method relies on down conversion of two optical sources by heterodyning them on the detector. This method provides much greater signal-to-noise ratio (*SNR*) when coupling into the waveguide, however the point spacing of the measurement is much larger as the step size is controlled by the operating wavelength of the laser.

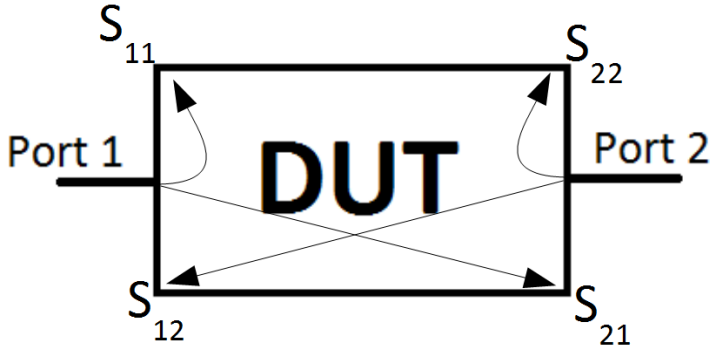


Figure 33. Representation of S-parameter measurements.

3.4.1 Small-Signal Modulation Bandwidth Characterization.

The first method described to measure bandwidth uses an optical vector network analyzer (*OVNA*), a piece of equipment specifically designed to measure the electrical frequency response of all *RF* devices and systems, both electronic and optical. It measures four S-parameters to determine how much power is transmitted and how much power is reflected at each port of the *DUT*. The measurement of each of the four parameters are defined by their subscripts. The first subscript always refers to the power out of the port specified by the subscript value, while the second subscript similarly refers to the power into the port specified. This means that an S_{11} measurement would identify power reflected at port one of the *DUT*. For the characterization of photodiodes, the S_{21} is the only parameter which is logical to measure. This is defined as the power transmitted by the device which can be written as Eq. 48. Figure 33 depicts what each of the S-paramters represents when taking an *RF* measurement.

$$S_{21} = 10\log_{10}\left(\frac{P_{out2}}{P_{in1}}\right) \tag{48}$$

The measurement of the S_{21} begins with calibrating the electrical response of the

PNA. This is accomplished by performing an E-cal measurement using an electronic calibration module. This ensures that any frequency dependent losses internal to the piece of equipment are calibrated before the measurement is taken, therefore the *PNA* starts with a flat frequency response. Additionally, the cabling and bias tee's *RF* responses must be measured to deembed their frequency dependent loss from that of the *DUT*. This response is post processed out after the measurement is taken. The final step is the manual entry of the S-parameters of the probes used.

When shipped the probes arrive with their measured calibration from the manufacturer, this calibration file is entered and appends the internal calibration of the *PNA* to include the probe's frequency response. Still, this appended file is not ideal, over time repeated contact with test substrates and device probe pads deteriorates the response of the probe invalidating the initial calibration. As this occurs the accuracy of the original calibration file is degraded, however, because only one probe is used in the measurement there is no way to directly measure the S_{21} parameter. By completing these steps the calibration of the electronic components of the measurement design are completed.

The next step is to modulate the *RF* tones produced by the *PNA* onto the optical carrier for measurement by the photodiode. This modulation process must also be calibrated. There is a second piece of equipment designed specifically to work with the *PNA* used for the measurement of optical devices known as a lightwave component analyzer (*LCA*). This piece of equipment directly interfaces with the *PNA* to complete either electrical-to-optical (*EO*) or *OE* measurements. These conversions are performed using an internal modulator and high-speed photodetector whose *RF* signals are fed directly into or out of the *PNA*. Together these two peices of equipment comprise the *OVNA*.

Another step of calibration is required for this *EO* process before it can be used to

measure the integrated photodiode. The output of the modulator is fed directly back to the *LCA*'s detector in order to produce the frequency response of the modulator. This calibration process does need to make one assumption, the detector, internal to the *LCA*, has a completely flat frequency response over the tested frequencies. This *LCA* assumption creates a problem with the measurement of photonic devices, as the measurement becomes a proverbial catch-22. In order to calibrate the modulator, a calibrated detector must be used, however to calibrate the detector a calibrated modulator must be used. Using one to calibrate the other means there is no absolute calibration, however for the 67-GHz *OVNA* the flat frequency response of the detector appears to be a resonable assumption as shown latter using the heterodyne approach.

Once all of the calibration is completed it is possible to test the integrated photodiode response. A voltage source and a bias tee are used to bias the photodiode for the measurement. A bias tee is a three port device with a *DC* port to apply a *DC* bias to the *DUT*, a *RF* port which acts as a high-pass filter only transmitting the *RF* tone received by the photodetector, and a third port which goes to the device acting as an all-pass filter. This port biases the device while transmitting the received signal from the photodiode to the *RF* port. The measurement setup can be seen in Figure 34.

The one drawback of using the *LCA* is the low output power. The max *RF* power is -6 dBm while the maximum optical power is 6 dBm. Although this would be more than sufficient power when testing a traditional (normally incident) photodetector, the large insertion loss while coupling onto the chip significantly diminishes the received power. This loss is magnified by a power of two due to the *OE* conversion in the photodiode. The photo-generated current is directly proportional to the input optical power on the photodiode. However, if an insertion loss, (I_L) is seen by the waveguide the received power of the photodiode is diminished by the value seen in Eq. 47.

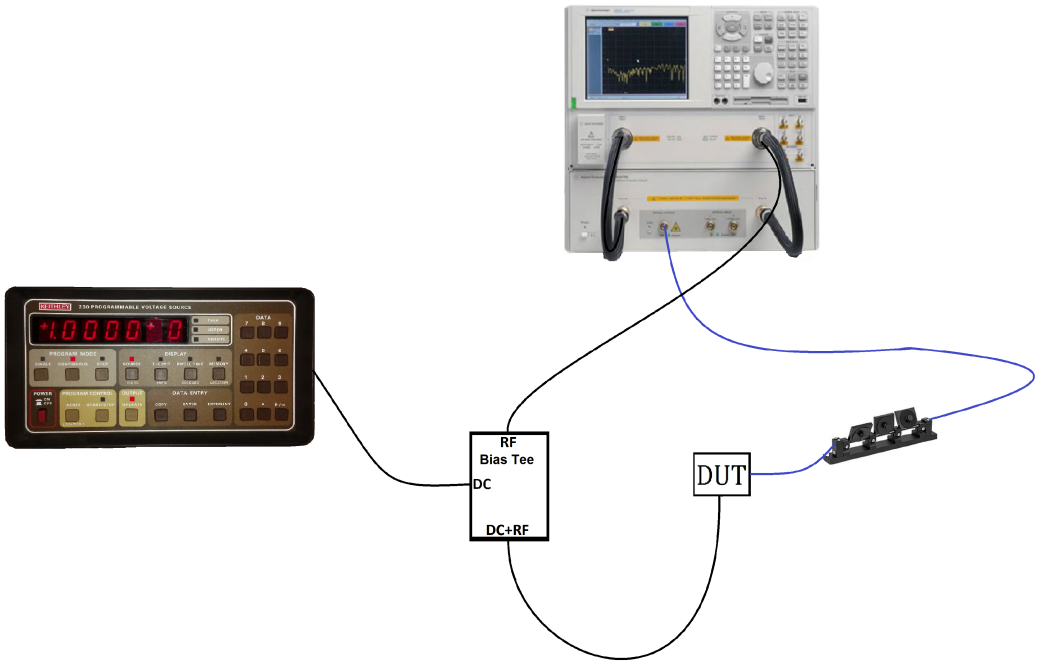


Figure 34. The measurement setup of the the detector bandwidth using a *PNA LCA* system.

Photocurrent is directly proportional to the optical power, (P_{in}) seen by the detector, however the output power (P_{out}) of the detector is shown in Eq. 49, where I generated photocurrent and R is the load resistance of the PNA. Therefore, the optical power loss due to coupling into the waveguide structure is squared due to the squared current term. This means that a 3-dB insertion loss translates to a 6-dB loss in signal strength measured by the PNA.

$$P_{out} = I^2 R \tag{49}$$

3.4.2 Large-Signal Modulation Bandwidth Characterization.

By heterodyning two lasers together on the diode, a more powerful optical signal can be launched into the photodiode. This larger optical signal in turn produces a larger RF tone at the output of the diode. The method by which these two lasers produce a microwave tone on the photodiode is described in the following section.

Once the method is understood the application of this test measurement will be detailed.

$$Int = |U|^2 = \left[Ae^{j(2\pi\nu t+\phi)} \cdot \ A^* e^{-j(2\pi\nu t+\phi)}\right] = 2A^2 \tag{50}$$

A photodetector cannot respond quickly enough to detect electric fields. Indeed, it acts as a low-pass filter, stripping the optical carrier off any signal below its bandwidth by detecting intensity. Therefore, when a laser with frequency $\nu = \frac{\lambda}{c}$ and amplitude (A) is detected on the photodiode, it is really detecting the magnitude squared of the field (intensity) Int as shown in Eq. 50. The equation shows that the detector has stripped off the high frequency carrier leaving only the DC signal riding on that carrier.

Expanding now to two lasers of similar wavelength impingent on the photodiode the equation may be rewritten by substituting the new sum of the fields into the solitary field of Eq. 50. To simplify the problem, each laser can be thought of as a perfect mono-chromatic source, however the finite linewidth of a real laser will be addressed later. The frequencies of the two lasers can then be written as ν and $\nu+\nu_{RF}$ to show the RF separation between the two signals. The resultant detected intensity is shown in Eq. 51. There is no coherence between the two sources, which means the phase difference between the lasers is irrelevant over the integration time of the detector. The final result is the sum of half of the intensity of each of the two fields and an RF sinusoid of frequency ν_{RF}. This derivation ignores the physical linewidth of the laser in favor of assuming two Dirac–delta functions in the frequency domain. When heterodyning the two lasers, the width of the microwave tone will then be approximately the sum of the linewidths of the two lasers. This was ignored due to

the selected resolution of the measurement equipment.

$$\begin{aligned} Int &= |U_1 + U_2|^2 \\ &= \left|A_1 e^{j(2\pi\nu t)} + A_2 e^{j[2\pi(\nu+\nu_{RF})t]}\right|^2 \\ &= {A_1}^2 + {A_2}^2 + A_1 A_2 e^{-j(2\pi\nu_{RF})} + A_1 A_2 e^{j(2\pi\nu_{RF})} \\ &= {A_1}^2 + {A_2}^2 + A_1 A_2 \cos(2\pi\nu_{RF}t) + jA_1 A_2 \sin(2\pi\nu_{RF}t) + ... \\ &\quad A_1 A_2 \cos(2\pi\nu_{RF}t) - jA_1 A_2 \sin(2\pi\nu_{RF}t) \\ &= {A_1}^2 + {A_2}^2 + 2A_1 A_2 \cos(2\pi\nu_{RF}t) \end{aligned} \tag{51}$$

The measurement of the heterodyne bandwidth should give the same results as the *PNA LCA* bandwidth, but it will have a much higher signal to noise ratio due to the higher power input. Again, the device was biased using a voltage source and a 67-GHz bias tee just as in the *PNA* measurement. However, rather than using a modulator, the measurement was performed using two narrow-linewidth *DFB* lasers. One laser was fixed while the other was temperature tunned to modify the gain cavity length, thus shifting the laser wavelength. As shown previously, the frequency detuning of the second laser is equivalent to shifting the frequency of the *RF* tone seen by the detector. The *DC* component of the heterodyne measurement is then stripped off the signal at the bias tee, while the *RF* port of the bias tee is sent to an electrical spectrum analyzer (*ESA*) which records the peak frequency on the spectrum from 50 MHz to 50 GHz.

Originally a *DC* block was used in line with the bias tee for fear that the large *DC* power from the device could damage the *ESA*. It was later determined that the use of a *DC* block is unnecessary for the measurement. The final measurement design can be seen in Figure 35. As stated earlier in the heterodyne derivation, the linewidths of the lasers will cause spectral broadening of the *RF* signal. This would cause a problem if the *ESA* sweep resolution were smaller, however with sufficiently wide resolution

steps this problem can be avoided. This problem can be avoided because the *ESA* places all of the *RF* power detected during its frequency sweep into a bin with the width of the resolution frequency of the *ESA*. For a 50-MHz to 50-GHz measurement, the bin sizes are over 300-MHz wide. This means that the 500-KHz broadening of the *RF* signal will be imperceptible to the equipment's measurement capabilities. It is also worth noting that the data obtained at frequencies below 200 MHz is limited by noise issues. When the two lasers' frequencies were close together small reflections from the couplers began feeding back into the cavities causing frequency pulling as the lasers were unstably injection locked. The addition of isolators would prevent the potential for back reflections from reaching the cavities which would clean up the signal at low frequencies. However, this was not necessary as the frequency response of interest lies primarily beyond 1-GHz. Finally, the complete measurement must be post processed to remove the frequency response of the cables and bias tee which were measured as part of the calibration for the *PNA* measurement.

A second method was used to verify the results obtained from the *ESA*. The measurement was repeated a second time with identical sweeping parameters using an *RF* power meter to replace the *ESA* in Figure 35. This replacement was performed to ensure the results of the *ESA* measurement were accurate. When measuring using the *ESA* there is potential for the *RF* tone to jump into and out of the window of the oscillator as the frequency is swept over the *ESA*'s range. This movement around the oscillator would cause the output *RF* power to fluctuate. However, an *RF* power meter sums the power over its entire bandwidth. If the *RF* tone was unstable, the total power over the spectrum would be integrated by the power meter, therefore the reading would remain unchanged. However, because it integrates over the whole *RF* bandwidth it can not tell what frequency signal it is receiving. Therefore, the *RF* power data has to be appended to the *ESA* sweep to know what *RF* frequency each

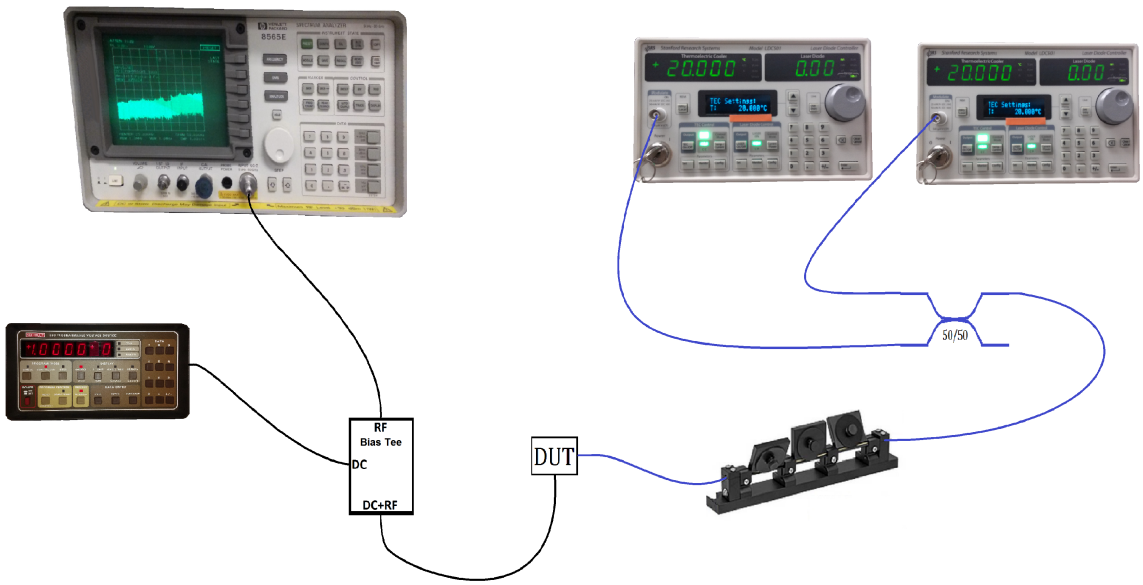


Figure 35. The measurement setup of the detector bandwidth by heterodyning two *DFB* lasers.

detuning temperature produces.

3.5 Automation

The effort of completing all these measurements was greatly aided by the application of computer programs to interface with the lab equipment over general purpose interface bus (*GPIB*) cabling. These programs were provided by the lab manager, Dr. Usechak, who has written code to interface with a majority of the equipment present in the lab. The use of these programs to interface with equipment provides higher resolution data as well as saves invaluable time spent on collection. Automating the data collection process and assigning it to readable files allows more time for the aggregation of data and analysis of the results. It also provides the infrastructure to rapidly test and compile data on future devices, reducing the turn-around time between fabrication and modification.

The results of these types of measurements give insight into the capabilities of the integrated devices and their potential for practical applications. Although these measurements are simple in theory, it takes time to develop a measurement test suite which accurately provides data for the devices.

IV. Results

The use of a well-developed test suite allows for the rapid testing and analysis of devices, expediting test and measurement throughput, uniformity, and reliability. Results obtained by testing detectors using the measurement techniques described in the previous chapter will be discussed in order to gain an understanding of the performance limitations of the detectors under test, based on the previously derived models in chapter II. A *COTS* device was initially tested to ensure the validity of the test and measurement procedures as well as to establish a baseline by which to ground the results obtained from the test structures.

4.1 Measurement Validation

The initial device tested was a packaged 22-GHz high-power *COTS* InP photodiode. The device was fully packaged and required no probe pads or waveguides, to extract the electrical signal which typically must be calibrated out of integrated device measurements. This packaging made this device an ideal candidate to ensure the measurements made using the test suite worked as intended. It also was accompanied by specifications and measurements published by the manufacturer which could be confirmed through the charactrization process. Beginning with the dark current, the devices electrical properties were measured. An iterative search program was written to scan through the four fitting parameters of the non-ideal diode equation from (Eq. 33) minimizing a normalized percent-error function. The minimization of the percent-error function describes the best-fit model for the measured device. The results of this fit can be seen in Figure 36. The data shows good agreement between the equivalent circuit model and the device's electronic performance. The high-power handling capabilities of the device are achieved through the reduction

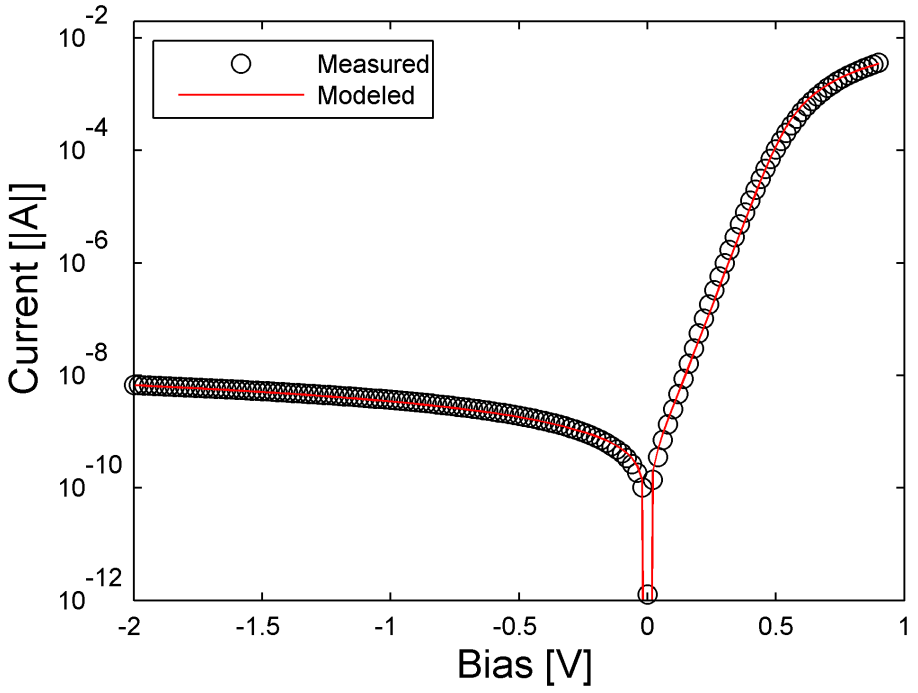
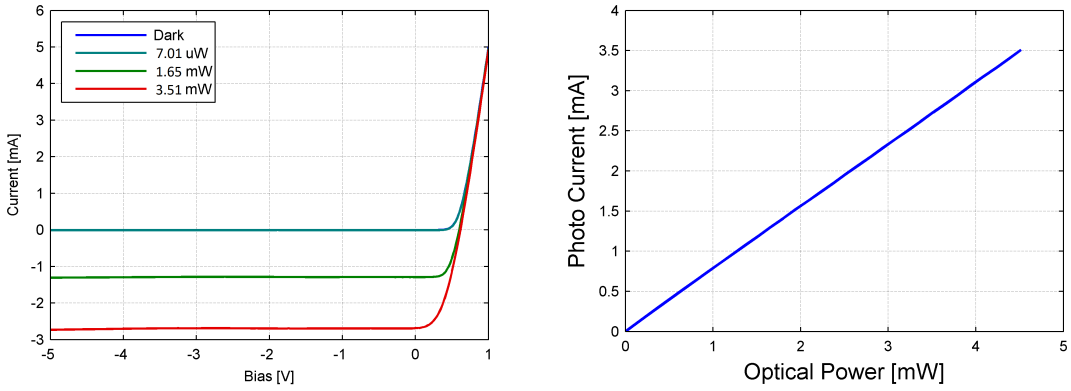


Figure 36. Results of the code used to fit the equivalent circuit parameters to the measured dark current results.

in series resistance to 97 Ω. This means that less of the photocurrent generated contributes to the Joule heating of the device. The device did show recombination in the depletion region as n_e was 1.4, however, this value was not included in the manufacturer's published specifications. It maintained a 15-nA dark current at the operating reverse bias of −5 V. The power dependent responsivity is easily identified by simply dividing the photocurrent by the launched optical power. This result can be seen in Figure 37 which demonstrates both the LIV characteristics and the power dependent responsivity. The measured value of 0.78 A/W was very close to the specified 0.8 A/W responsivity published by the manufacturer. Unfortunately, the *DC* bias port of the detector had soldered connections with long leads. While these long unshielded connections do not affect the performance of the device, as they only carry a *DC* voltage, they do make it impossible to make an accurate CV measurement on the device. Therefore, the detector's capacitance was estimated assuming the device



(a) **(b)**

Figure 37. (a) LIV curves for a packaged *COTS* photodetector. (b) Photocurrent generated based on input optical power. Demonstrate a resultant responsivity of the *COTS* detector to be .78 A/W.

was RC limited.

The bandwidth was tested with both the *OVNA* method as well as the heterodyne detection method. The *OVNA* method is better suited for this type of measurement as there is no large optical coupling losses in the experimental setup. This means the *SNR* is more than sufficient to identify the bandwidth of the device. This may be contrasted with the heterodyne measurement where the high power of the two *DFB* lasers is not necessary to overcome the insertion loss of the on-chip waveguides. However, both techniques were used in order to ensure the validity of both measurement setups. The comparison of the results of the measurements can be seen in Figure 38. While there are some small deviations between the measurements, they both predict a 23.1-GHz bandwidth. Using the fitted series resistance R_s the capacitance was calculated to be approximately 24 nF. With the exception of the capacitance measurement, the test suite was successful in identifying all of the specified performance metrics of the device validating the designed measurement process. This verification action gives the assurance that the characterization of the integrated devices is accurate.

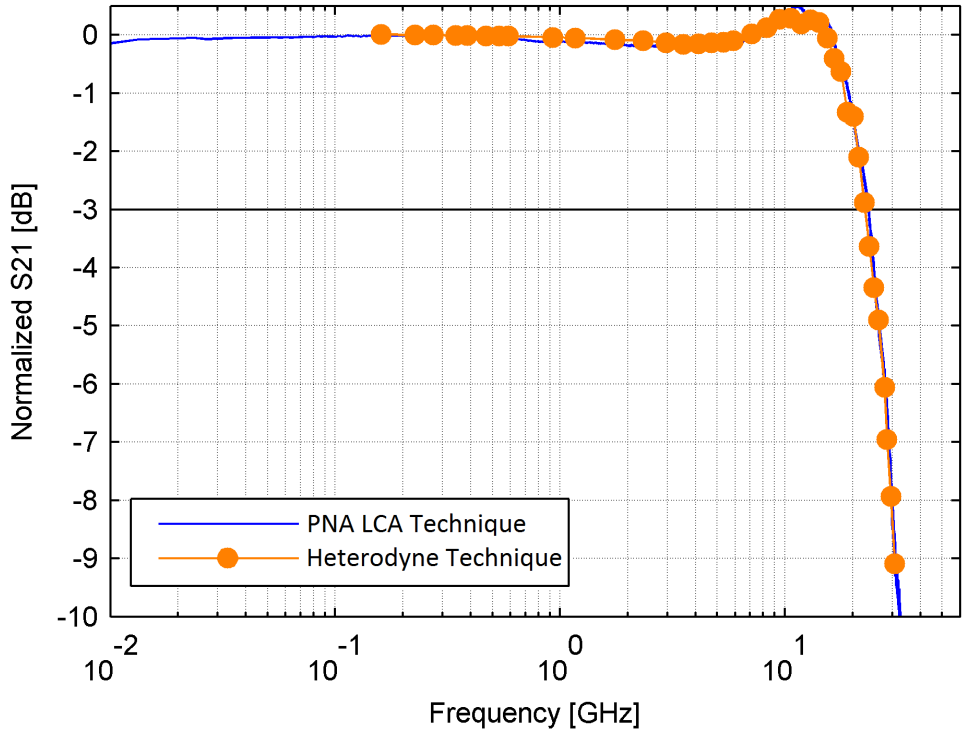


Figure 38. Comparison between the optical heterodyne and *PNA* bandwidth measurements shows good agreement between the techniques.

4.2 Waveguide Structure Characterization For Detector Correction

The characterization of the waveguide as described in the previous chapter is fairly straightforward. The difficulty stems from optimizing the alignment of both the input-coupled and output-coupled fibers. Indeed, it is difficult to identify whether one or both of the fibers are out of alignment. Additionally, slab modes of the SiO_2 are easily excited if the input fiber is out of alignment. This can be deceiving during the optimization of the fiber alignment, leading to wasted time aligning to the incorrect structure. Leveraging the fact that the devices analyzed are photodetectors, the optimization of the fiber alignment could be performed one at a time on a detector structure then moved laterally to align to the waveguide where only small corrections must be made to each fiber for optimal alignment.

Using two power meters as shown in Figure 30, while bypassing the DUT, a small percentage (10%) of the power was sent to a monitor optical power meter where it acts as a known reference for the launch power measured at the output of the lensed fiber. Unfortunately, the output power of the lensed fiber was difficult to accurately measure and would vary depending on the location of the lensed fiber's tip when using an integrating sphere. Instead, the output of the polarization controller was directly fed to the second optical power meter in order to identify how much optical power was launched into the chiplet. This relied on the assumption that the losses generated by the 0.5-m lensed fiber and the additional connector are minimal. With the proportionality constant between the monitor optical power meter and launched optical power known, the waveguide's insertion loss can be characterized.

With both fibers aligned to either end of the waveguide, the power transmitted through the structure was measured. The monitor optical power meter acts as a reference for the launched optical power to avoid variation from test to test. Therefore, the final insertion loss can be calculated using Eq. 46. The results of the insertion loss

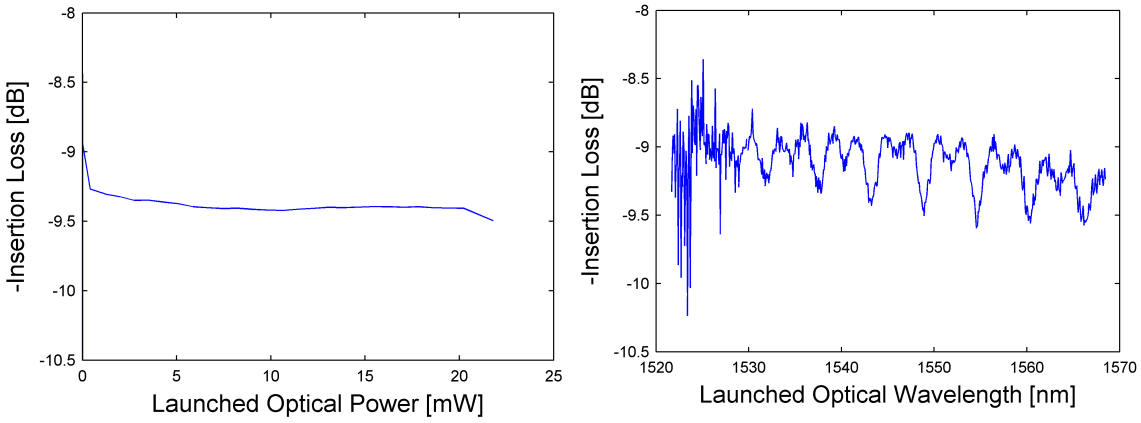


Figure 39. The power (a) and wavelength (b) dependent transmission of an integrated waveguide structure. aligned to the *TE* polarization at 1548 nm.

for the wavelength- and power-dependent sweeps of the waveguide structure can be seen in Figure 39. For a fixed wavelength the power-dependent insertion loss of 9.4 dB can be seen in Figure 39a. The 1-dB fluctuations in wavelength-dependent insertion loss are due to improper alignment of the polarization state as the laser's wavelength is swept. This will cause noise in the calculation of the wavelength-dependent responsivity of the diode, but unfortunately cannot be avoided without measurement and feedback control of the polarization state when using non-polarization maintaining fiber. While such a feedback control system could be used, it adds another level of complexity to the measurement suite and was intentionally avoided for this work.

4.3 Device Experimental Test Parameters

For this work new devices were fabricated in an effort to further improve the performance of previously fabricated and published devices. A design of experiments (*DOE*) chiplet was received from Sandia National Laboratories for testing and characterization in an effort to refine the fabrication processes in the future. Therefore, the results of this work will aid in the development of superior devices in the future.

For this chip layout, a full factorial *DOE* design (i.e. every possible combination of design factor was fabricated) was used with five parameters (factors) each with levels ranging from two to four. The first parameter was width. Three levels of device width were selected: 1, 2, and 4 μm. The next parameter was device length which also had three parameters of: 5, 15, and 50 μm. These physical size parameters allow for the identification of area-dependent effects on the device's performance (e.g. whether dislocation densities, and therefore dark current, scale with area). The third parameter was substrate doping which had two levels: one doped with *B*, the other degenerately doped with *B*. The substrate is doped in order to create an ohmic contact for the vertical *pin* structure. The dopant densities were varied to test the variation in contact resistance at the *Ge–Si* interface. In addition to substrate doping, two substrate etching levels were selected. *Ge* stacks were grown on full-thickness *Si* and partially-etched *Si*. The final factor of the *DOE* chiplet was the *Ge* fill which was tested with four different levels. For this parameter, the surrounding oxide was etched and filled with varying percentages of *Ge*: 0%, 1%, 5%, and 10%. These fill fractions are designed to reduce dislocations by reducing the lattice strain mismatch. This *DOE* mask set resulted in the fabrication of 144 devices. A table of all of these factors and their levels can be seen in Table 2. The colors for the location of the substrate factors refer to the chip map image of Figure 40.

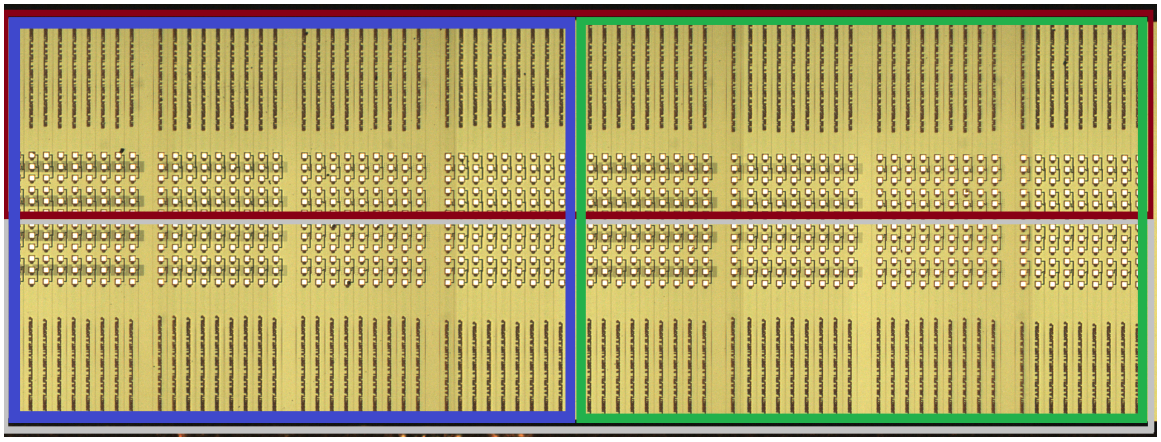
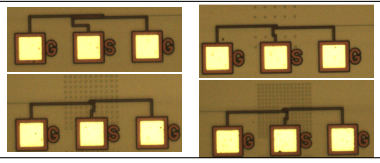


Figure 40. Microscope image of the chiplet used for testing. The areas encompassed by the blue, green, red, and gray rectangles are the etched *Si*, full-height *Si*, p^+-, and p-doped substrates respectively.

Table 2. Factors and levels for the *DOE* chiplet characterization.

Factors	Levels	Description
Width	1 μm 2 μm 4 μm	
Length	5 μm 15 μm 50 μm	
Substrate Doping	P P^+	
Substrate Etch	Full Height *Si* Etched *Si*	
***Ge* Fill**	0% 1% 5% 10%	

With the knowledge of what devices were fabricated at the foundry, testing could begin in order to identify the effect of each factor on the device performance. The p-doped devices were tested first as they had not been characterized in the previous published paper where heavily doped p^+ Si was used for the device fabrication [36].

4.4 Characterization Results

The p-doped devices were the first to be characterized, however, only a small number of devices were tested as they suffered from an issue associated with the doping of the structures. The electronic performance was again analyzed first, however the devices were extremely difficult to fit to the equivalent circuit model as they did not behave as anticipated for an ideal diode. Due to the exponential value in the ideal-diode equivalent circuit model, there should be a linear region, on a logarithmic scale, from the point where the device begins to "turn on" until the series resistance starts to dominate. The slope of this linear region is defined by the ideality factor as previously shown in Figure 15. This region was not seen for the p-doped substrate structures leading to the presumption that there is an issue in the doping of these devices. Due to the odd behavior of the devices, the equivalent circuit parameters could not be accurately fit and could only be loosely estimated using the iterative best fit approach. This uncharacteristic diode behavior can be seen in Figure 41 along with the result of the best fit for the designed model. The results of the equivalent circuit parameters can be seen in Table 3, however due to the poor fit the accuracy of the results is questionable.

Upon testing the photocurrent of the devices the suspected fabrication problems seen in the dark-current testing were confirmed. As a result, it was assumed that there was an issue in the production of the devices either generated from doping of the *pin* structures themselves or a failure to produce a proper ohmic contact at the

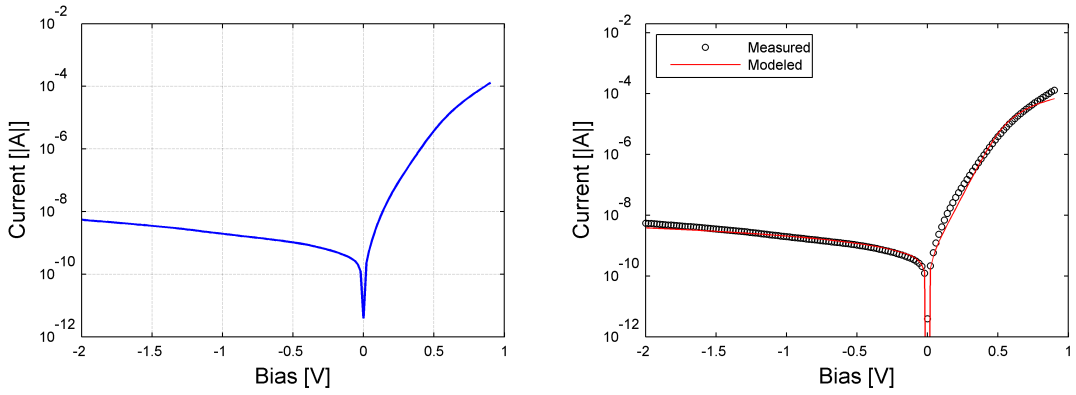


Figure 41. (a) The electronic characterization of p-doped substrate device. (b) Best fit approximation used to identify the equivalent circuit parameters

Ge junction's interface with the *Si* substrate. Rather than exhibiting the typical behavior of a photodiode where, $I = I_d + I_{ph}$, the devices had a large bias region where the current was negligible, regardless of the input optical power. This meant that within this bias region all the carriers were trapped and the device's responsivity was zero. This behavior can be seen in Figure 42a between -0.3 V and 0.4 V. After the realization that all of the p-doped substrate devices exhibited this behavior, their characterization was abandoned in order to focus on the characterization of the p^+-doped substrate devices. Figure 42 compares the results of the LIV curves for the p^+-doped substrate and p-doped substrate devices. Although the increased B doping of the substrate diminished the region over which charge was trapped in the device, there still remains a small portion from 0.1 to 0.25 V where the device does not behave as anticipated.

The devices fabricated on the p^+-doped substrate had been previously demonstrated in [36], therefore the expectation was that similar performance would be reproduced. Good results for the devices fabricated on the p^+-doped *Si* substrate allowed for the analysis of device parameters after eliminating the substrate-doping factor from the *DOE* measurement. Additionally, it allowed for the conclusion that

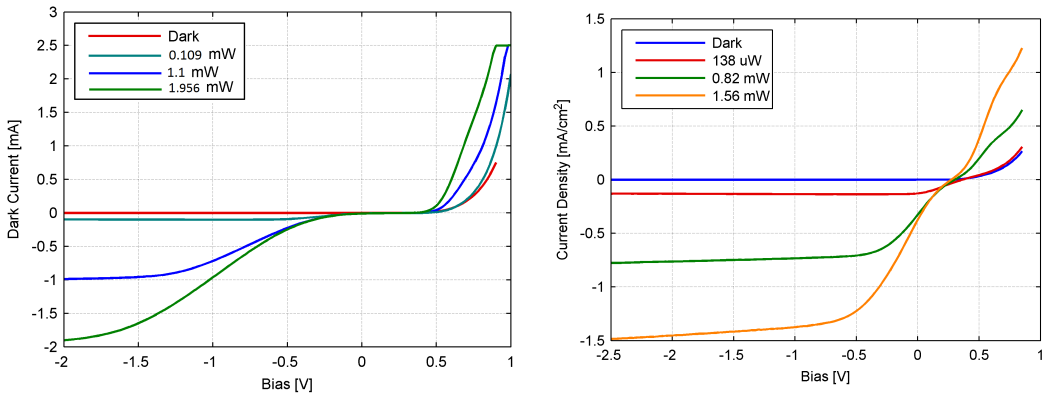


Figure 42. Comparison of substrate doping, (a) p-doped substrate (b) p^+-doped substrate, on device's photocurrent over operating biases.

the doping of the *Si* at *Si-Ge* interface was responsible for the non-ideal charge trapping behavior of the photodiodes fabricated on the p-dopoed *Si* substrate. The dark current exhibited by the devices fabricated on the p^+-doped substrate followed the anticipated behavior described by the ideal diode equivalent circuit, therefore they could be accurately fit by the model. Figure 43 shows the accuracy of the fit for the diode behavior. Fitting the measurement of the device to the equivalent-circuit modeling parameters provided the results which can be seen in Table 4.

The primary factor affecting the dark current of the devices was found to be the size of the structure. While there is some variation between the different *Ge* fill percentages and substrate etching profiles, it is within the fabrication variability between devices for the limited number of devices tested. This result can be seen in Figure 44, which demonstrates the dark current for various size detectors all with different *Ge* fill fractions. The primary factor affecting the dark current for these devices was their the size. Additionally, the series resistances from the fits of the diodes are dependent on device size, but not on area. A tripling of device length leads to a respective drop in the series resistance of the device, therefore the series

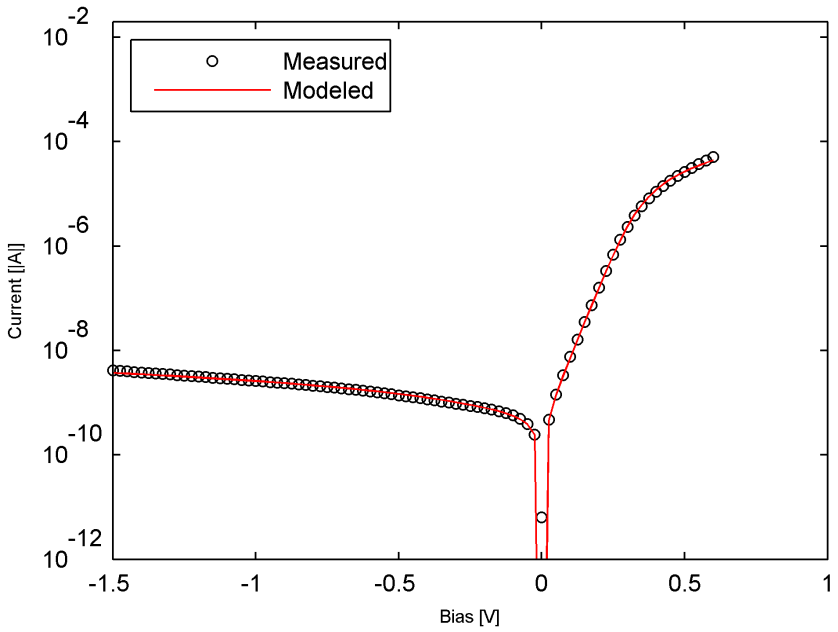


Figure 43. The results of the equivalent circuit model fit to the collected data of a 1x5-μm device fabricated on a p$^+$-doped substrate.

resistance of the 1x15-μm diode has 1/3 the series resistance of the 1x5-μm detector. This result was not true for the width. As the width is doubled the resultant series resistance is not halved, but reduced by a factor of 2/3. This result is significant as the capacitance of the detector scales with the area, therefore this relationship has a significant impact on the bandwidth of the devices.

Capacitance voltage measurements were taken on the diodes to determine their RC bandwidth limits and identify the ideal bias point for the device operation. These were taken using the *LCR* meter as described previously. The capacitance was unaffected by the etch and *Ge* fill parameters of the devices and only scaled with area. Just beyond -1 V of reverse bias the capacitance becomes nearly flat, which means any increase in reverse bias will only generate a small decrease in the capacitance of the device. However, the dark current will increase, decreasing the dynamic range of the device. This is one of the reasons -1.5 V was selected as the optimum bias for the

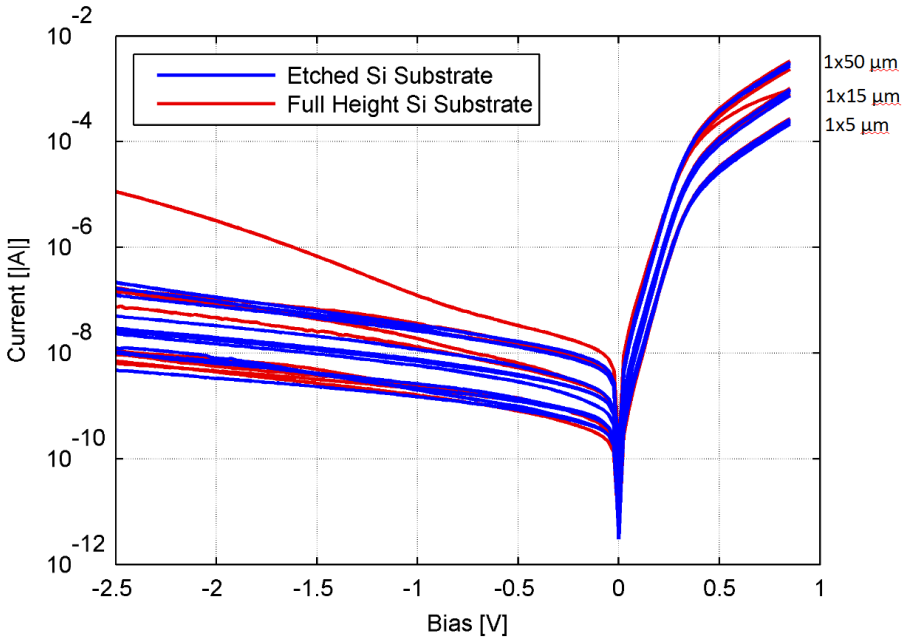
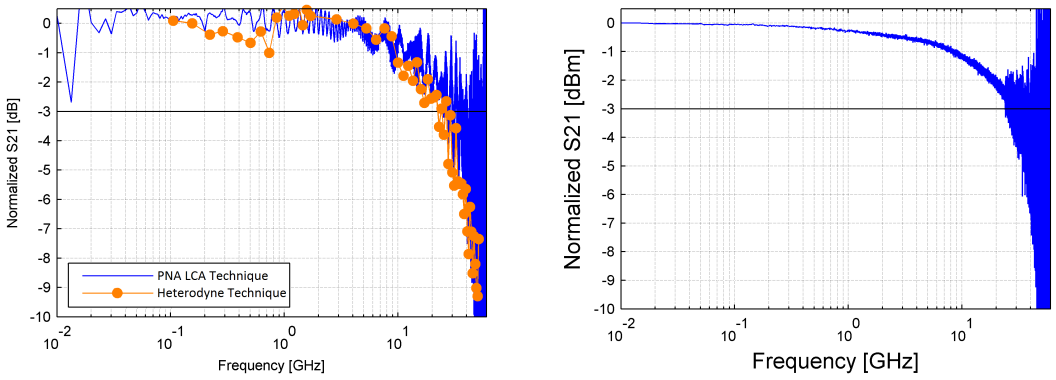


Figure 44. Comparison of detector size and substrate etching on dark current.

photodiodes, the other reason will be discussed in the next section.

The 3-dB bandwidths of the devices were initially obtained through the use of the *OVNA*. Although the system can be calibrated, issues arise at the probe tips especially if the correction file provided by the manufacturer is incorrect. If the S_{21} calibration of the probe is incorrect it will directly lead to significant errors in the measurement of the device. The devices were tested to obtain the 3-dB bandwidth of the detectors. However, they all showed similar impedance matching issues just as in Figure 45a. Similar frequency dependent noise levels in the impedance matching for the *RF* response of all of the measured detectors, (regardless of size, series resistance, or capacitance) led to the realization that the probe calibration file (provided by the manufacturer) was incorrect. Post processing was used to generate a probe calibration file which subtracted the variation around the mean at each point of a single measurement. This calibration file could then be used to remove the noise generated by the probe's impedance matching issues for any other detector measured.



(a) (b)

Figure 45. The electronic characterization of p^+-doped substrate device. (a) Direct measurement of 3-dB bandwidth. (b) 3-dB bandwidth measurement post processed using estimated probe calibration.

By generating a calibration file on the adjacent device, the impedance matched result of the frequency response of the detector can be seen in Figure 45b. This result gives an approximate bandwidth very close to the estimated bandwidth based on the RC limit of the device. The device's bandwidth at -1.5 V with a capacitance and series resitance of 7.8 fF and 4.4 kΩ respectively generates a RC bandwidth of 28 GHz. Although the measured bandwidth was 25 GHz, the increased noise at the higher frequencies makes it difficult to estimate the exact 3-dB bandwidth of the detector.

Finally, the responsivity was measured using the calibration file previously generated from the waveguide measurements. The responsivities of all the devices were nearly identical regardless of the length, substrate etch, or *Ge* fill fraction. The responsivity did however change with the width as the cross-sectional area of the detector exposed to the incident optical field was increased. Under normal operating optical input powers the value ranged between 0.89 and 0.96 A/W. This variation was due to imperfect and inconsistent alignment of the fibers. This result makes sense when analyzing the absorption coefficient of *Ge* as all of the carriers are typically absorbed in the first 5 μm of the device. The power-dependent responsivity over the

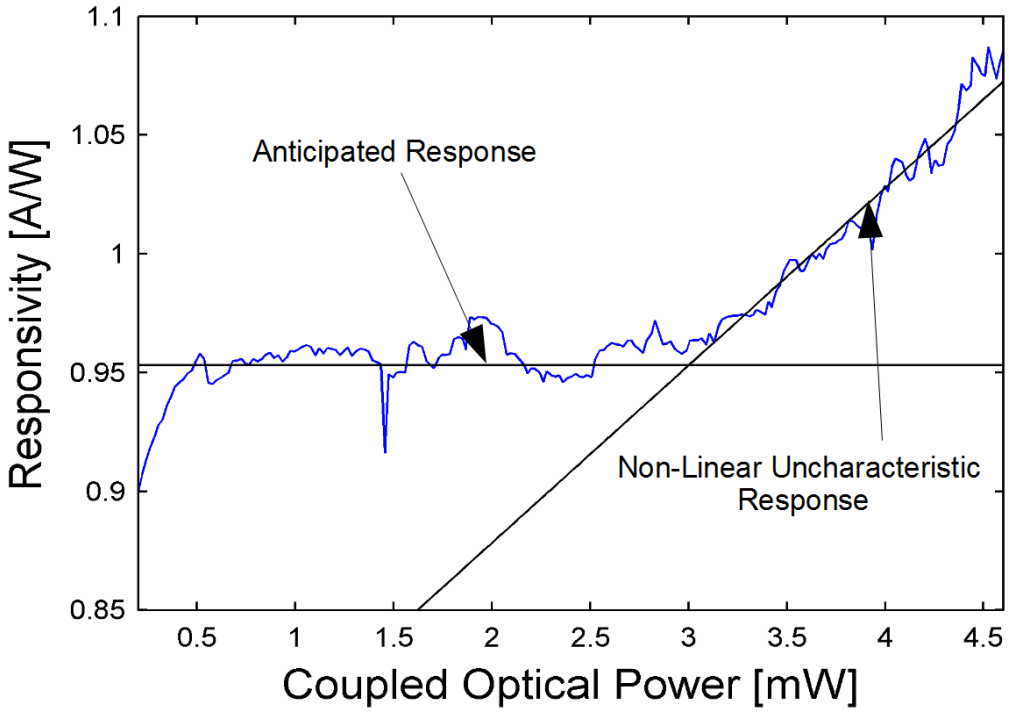


Figure 46. Measured responsivity of the detector over a wide range of optical power.

full power of the laser diode is shown in Figure 46. While the responsivity results at low optical power can be explained by the laser's operation just above threshold, the results under high optical intensity show that the device begins to have a responsivity greater than one. This perplexing result was heavily investigated in order to identify the mechanism driving the increase in photocurrent.

4.5 Measurement and Analysis of The Non-Linear Avalanche-Like Effect

As shown in Figure 46, while testing the power-dependent responsivity of the devices, a high-power laser source was used in an attempt to saturate the photodiode. Surprisingly saturation was not observed under high powers, but rather an increase in responsivity was observed. This abnormal behavior can be seen in Figure 46 and 47. This unexpected result was verified by generating LIV curves with high optical input powers and large reverse biases as seen in Figure 47. The behavior was seen in all of the p^{+}-doped devices. This behavior implies that additional carriers were being generated under high-power and high-reverse bias conditions. Additionally, these supplemental carriers produce damaging current densities which caused devices to break down over time or catastrophically fail.

This response was theorized to either be generated from an optically induced avalanche breakdown of the junction or a thermal runaway due to the narrow bandgap of *Ge*. An experiment was devised in order to identify the underlying physics responsible for this non-linear behavior. It was decided that looking at the transient response of the photodiode would provide a method to separate the thermal and avalanche processes. For the experiment it was assumed that avalanche breakdown of the depletion region could be triggered with a sufficient carrier population. This would drive the diode out of equilibrium generating a large enough electric field to create a gain region across the junction. With such a large electric field, carriers would gain sufficient energy to cause impact ionizations during transit across the depletion region leading to an avalanche effect. This avalanching effect would be orders of magnitude faster than the thermal heating of the device and surrounding material. In order to test this the optical power would have to be rapidly turned on and off while operating in the non-linear region.

Selecting a hard optical pulse or step function from completely "off" (in order to

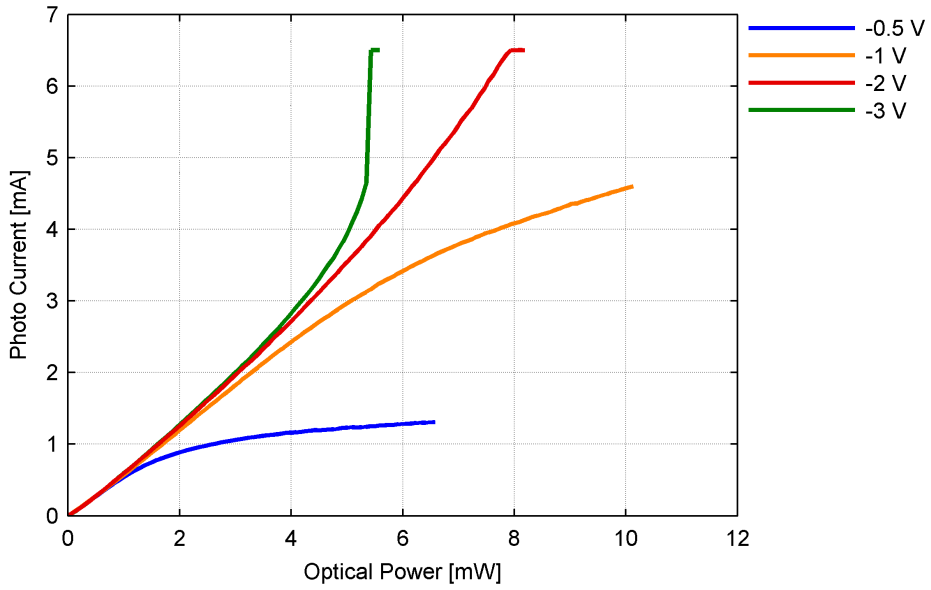


Figure 47. Observed increase in generated photocurrent based upon reverse bias voltage.

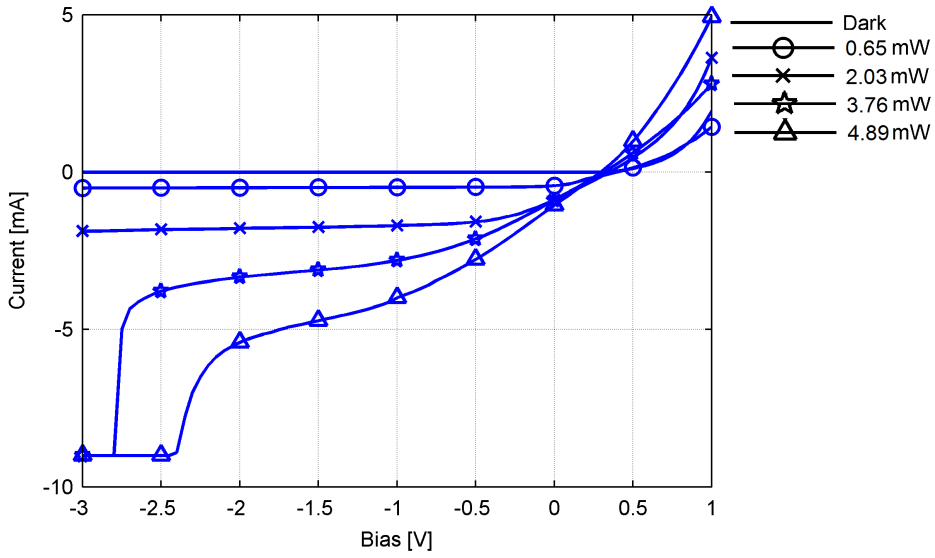


Figure 48. Observed increase in photodiode response based upon reverse bias voltage and input optical power.

measure the dark current) to "on" and then back "off" again, would ideally be able to identify which of the two mechanisms were driving the behavior. Such "hard pulsing" is necessary to decouple optical carriers from thermally generated carriers. When measuring the thermally generated carriers in the optical "off" state, any optically produced carriers become noise. Originally a $LiNbO_3$ *MZM* was used to pulse the optical signal applied to the device as these devices can be rapidly modulated and handle large optical powers, however they lack the ability to fully block light while in the "off" state. As a consequence, an optical chopper was selected as it can provide near perfect extinction. The only drawbacks to a chopper are its fixed duty cycle, (it only produces a square wave), and the slow modulation speed, ($\sim$100 Hz square wave signal). In order to accommodate the chopper, a more complicated setup was required which included a free-space optical component. This collimating "U-bench" adds an additional 1.5 dB of loss to the measurement platform, however the *DFB* lasers used in the experiment had sufficient power to overcome the loss induced by the U-bench.

With this experimental design in mind, several pieces of equipment were tested in order to identify which one would have sufficient bandwidth for the measurement of the transient response of the device. While the *SMU* provides accurate low-level current measurements and would be an excellent piece of equipment to use in order to identify the operating temperature of the junction, it comes at the price of long response times. The buffered memory of the equipment can only sample at intervals $\sim$1 ms. Even worse, the acquisition circuitry of the equipment cannot handle large changes in the measurement value on that time scale, (even with a fixed measurement range). Therefore, the *SMU* could not be used as a monitor for the transient response of the device. A bias tee was also investigated as its high-frequency output could be analyzed using an oscilloscope, however all the low-frequency information was

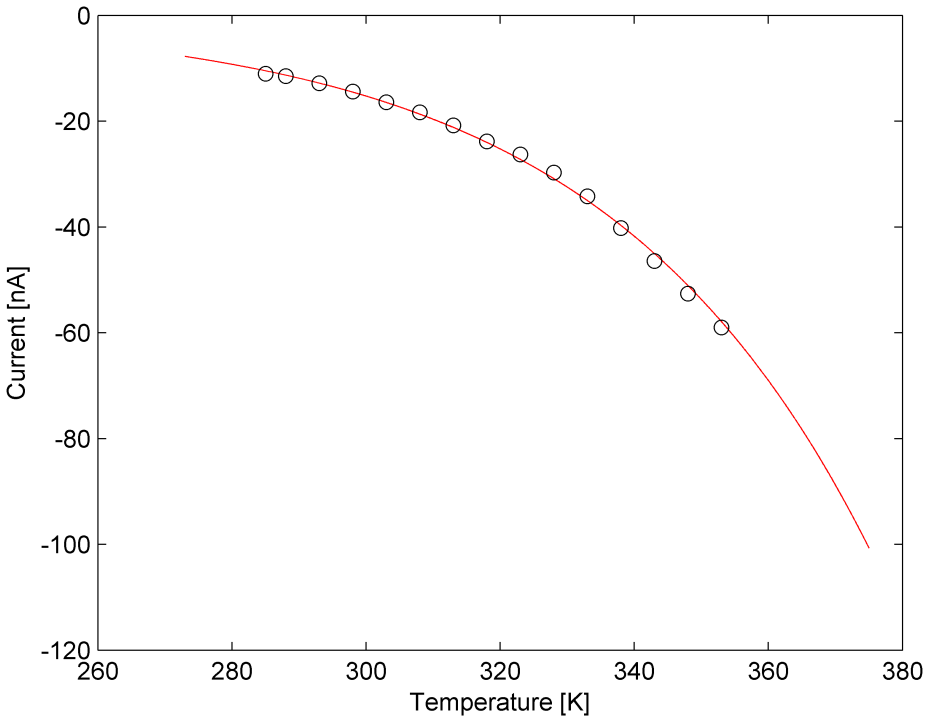


Figure 49. Measured thermal dependence of the dark current at -2-V reverse bias.

stripped off by the high-pass filter of the bias tee. The ideal solution for making this measurement requires a high-bandwidth transimpedance amplifier. This was the final approach used to identify the timescale of the device's breakdown effect.

The final experimental set up for the analysis of the additional carrier generation was performed by connecting the output of two integrated photodetectors to transimpedance amplifiers and visualizing the output using an oscilloscope in order to measure the transient response of the hard-pulsed optical signal. In this setup the first photodiode would be the device under test, receiving the full power of the optical pulse. A second photodiode adjacent to the *DUT* acts as a "witness" for the temperature of the lattice. At a fixed bias the temperature of the device was fit with an exponential as seen in Figure 49. This result provides the variation of the dark current as a function of temperature; the transient measurement seeks to exploit this

variation by measuring the current of the witness detector and use its dark current to infer the lattice temperature surrounding the DUT [48]. A third off-chip photodiode was used as a monitor for the optical pulse and to trigger the oscilloscope. By using a chopper with a relatively fast rise time, the mechanism can be determined by the output of the electrical signal.

Due to the inherently slow nature of thermal propagation of heat through the lattice of the chip ($\sim\mu$s), the output of the electrical response would have two parts. The first response would be the optical turn on of the generated square wave, while the second would be a more gradual turn on beyond the optical signal as thermally generated carriers began to cause a thermal runaway in the device. Additionally, some time later an increase in the witness photodiode current would be observed as the lattice heated the adjacent junction. By measuring devices closer and further away from the DUT, a fit could be generated to the temperature gradient of the chiplet permitting the estimation of the junction temperature. The second hypothesis was that the device's additionally generated carriers are driven by an avalanche process in the depletion region where hot electrons would trigger impact ionization events. This hypothesis would be substantiated if the electrical response of the DUT matched the input optical signal since this process is expected to be fast ($\sim$ns). Additionally, the witness detector would show no substantial change in the dark current as there would not be a significant amount of heat generated across the chiplet. Unfortunately, the "witness's" current will change a small amount as some power will inevitably couple into the slab mode of the waveguide and leak into the "witness" detector. Still, it was verified that the small change in dark current due to the small number of optically generated carriers will not mask the thermally generated carriers due to lattice heating from the DUT. This experimental design can be seen in Figure 50.

General-purpose transimpedence amplifiers were used for this work but were lim-

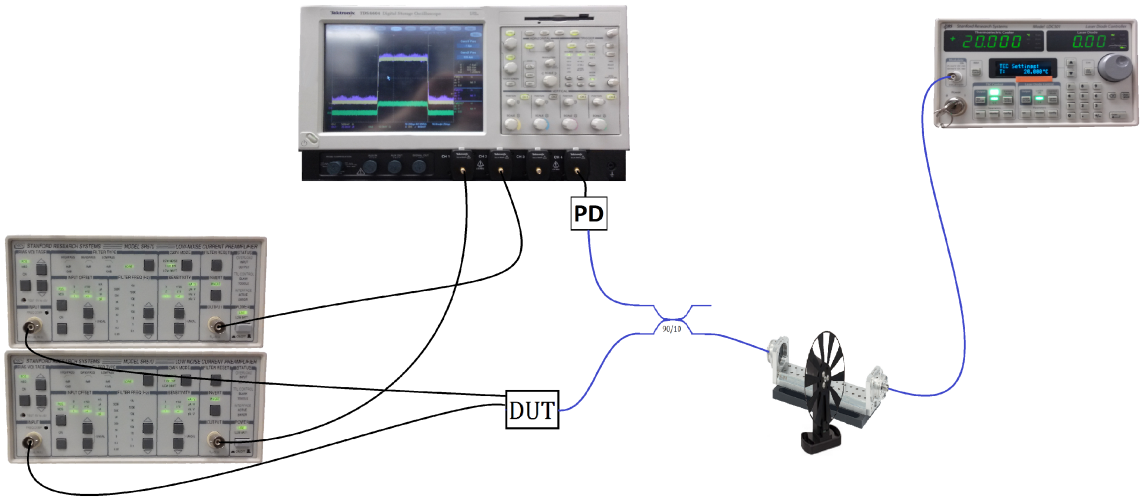


Figure 50. Experimental design for testing the transient response of the photodetectors to determine the carrier generation mechanism.

ited to 5 mA of input current therefore the bias selected for the DUT could not exceed ∼-2.5 V. This bias is on the edge of the knee in Figure 48 where the excess carriers should begin to be generated. This would provide a good result without damaging the device due to too much excess current. The results of this measurement with a 600-Hz chopper frequency can be seen in Figure 51. It should be noted that the witness detector response is not to scale, it has been multiplied in order to make the rise time of both devices viewable. Both devices essentially exhibit the same response; both reproduce the input optical square wave. This response appears to support the hypothesis that the avalanche breakdown is induced by the large number of photo-generated carriers. Unfortunately, due to time constraints, and the limitation of the transimpediance amplifiers I was unable to repeat this measurement further into the non-linear region where more conclusive results could have been obtained. Future testing and characterization should yield greater understanding as well as aid in the development of a model for this behavior.

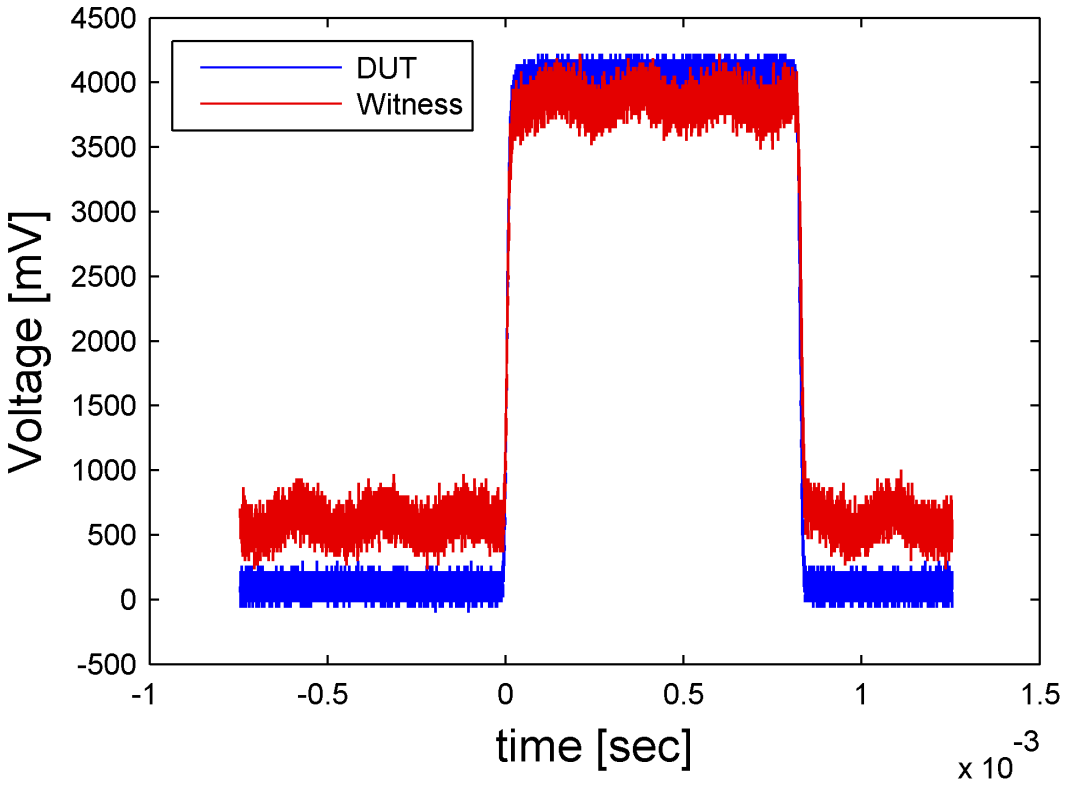


Figure 51. Transient response of the device on the edge of the non-linear region.

V. Conclusions and Recommendations

This final chapter summarizes the results and findings of the document to give clear direction and recommendations for the future fabrication of *Ge pin* diodes for integration with *CMOS* electronics. Additionally, it points to future investigation into device behavior based high-optical-power testing.

5.1 Conclusions of Research

fThe primary objective of this research was the further refinement of the fabrication processes associated with manufacture of integrated *Ge* photodiodes. An abundance of data was taken across many devices in order to provide the standard characterization of the device properties. Additionally, an unknown non-linear effect was observed and explored through a set of initial transient measurements of the device behavior in the non-linear region. Finally, new test mounting structures were designed and implemented in order to provide greater stability and flexibility to the test-and-measurement suite built at Air Force Research Laboratory (*AFRL*).

Both *RF* and *CW* metrics of a number of detectors were characterized and analyzed in order to identify potential modifications to the substrate doping of the device's *Si* contact layer. The non-optimal doping caused charge trapping, inhibiting the device's operation over a large bias region. It was observed that this region was significantly reduced through higher dopant densities in the substrate. Although only two points were observed for the dopant densities, a modification of the doping on the p-doped side of the diode as well as the substrate doping may lead to a reduction in resistance as well as superior ohmic contacts for the p-side of *Ge* photodiode stack. Moreover, the series resistances due to the contacts of the devices are very high and lead to reduction in the *RF* bandwidth. Modification of the via connections or con-

tact layers may lead to improved RF performance for the photodetectors by reducing the RC time delay of the circuit.

Finally, a majority of the time consumed by this work was focused on identifying the mechanism which induced greater carrier concentrations in the device leading to an eventual breakdown of the depletion region. While potential methods presented themselves initially for characterizing the non-linearity, the analysis of the transient response on a DC coupled oscilloscope appears to be an effective approach to identify the dominant carrier generation mechanism, however it was limited by the equipment output. Future testing should provide greater insight.

5.2 Research Contributions

Significant research advancements have been made in the last decade toward the monolithic fabrication of photodiodes, this research provides yet one small advancement toward the development of these critical photonic components. Indeed in this work I:

- Designed and assembled a second-generation mounting platform to facilitate the testing of integrated photonic structures.
- Designed and set up a test suite to facilitate the rapid testing of integrated photonic devices, specifically photodidoes.
- Performed standard characterization and performance measurements on an array of detectors in order to determine how various fabrication parameters affect the device's performance metrics generating useful data for future fabrication runs.
- Observed a non-linear response in the photodiode and began to investigate the physics behind this behavior using a novel time-resolved approach. This result

has a significant impact on the future applications of integrated detectors in analog photonics.

5.3 Future Recommendations

This research has shown the effective performance of monolithically fabricated integrated photodiodes through testing and characterization, while highlighting some current limitations and potential avenues for advancement. The design of a second run in which several of the same devices are produced will provide a better understanding of the variability and yield of the fabrication processes. Additionally, a *DOE* wafer which identifies the optimized contact and substrate doping levels would provide significant advancement of the device bandwidths, which appear to be limited by the very large series resistance. The devices' capacitance were well designed, remaining below 10 fF for a majority of the devices tested.

Additional measurement suite advancements could potentially be made through the design and implementation of a polarization-maintaining-fiber-alignment system to ensure the proper polarization is consistently aligned to the optical structure. This would eliminate the test issues associated with polarization rotation which were observed when testing the wavelength dependence of the structures. This problem is not isolated to detector characterization, but the characterization of all integrated photonic systems and devices.

The largest area of future interest, especially to push *DoD* concerns, lies in the modeling of the high-optical-power non-linear behavior of the photodiodes. With a greater understanding of the non-linear behavior observed in this work, steps may be taken to mitigate this induced avalanche-like-breakdown effect for high-power linear devices in the future. In microwave photonic systems, which are being pursued for use in aircraft, the linear performance of devices is paramount due to the analog signals

transmitted by such systems. Any non-linearity will directly impact the output of the system negatively as it will modify the original received signal. While the integration of optical platforms will bolster the potential of such visions, it is not realizable while imposing strict power restrictions on the system-level design of these applications.

Appendix A.

Results of the electronic equivalent circuit parameter fits for characterized integrated Ge photodiodes.

Table 3. Selection of the equivalent circuit parameter results from device testing.

Size [μm]	Substrate	Ge %	Doping	I_d [nA]	I_s [nA]	R_s [Ω]	R_{sh} [MΩ]	n_e
1x5	full Si	0	p	6.06	0.918	1221	347	1.98
1x15	full Si	0	p	11.2	1.25	1710	171	1.97
1x50	full Si	0	p	100.5	2.07	693	205	1.69
2x15	full Si	0	p	59.2	3.9	1000	347	1.98
2x50	full Si	0	p	131.3	7.5	261	199	1.92
1x5	full Si	1	p	3.52	0.097	997	402	1.65
4x50	full Si	1	p	283.1	15	200	94.4	1.97

Table 4. Selection of the equivalent circuit parameter results from device testing.

Size [μm]	Substrate	Ge %	Doping	I_d [nA]	I_s [nA]	R_s [Ω]	R_{sh} [MΩ]	n_e
1x5	full Si	0	p^+	4.90	0.324	3668	454	1.29
1x5	full Si	1	p^+	2.67	0.166	4082	716	1.18
1x5	full Si	5	p^+	3.74	0.260	4247	457	1.25
1x5	full Si	10	p^+	3.17	0.370	4014	571	1.29
1x5	etch Si	0	p^+	3.98	0.216	4378	575	1.22
1x5	etch Si	1	p^+	2.31	0.261	3874	816	1.25
1x5	etch Si	5	p^+	4.06	0.347	4653	530	1.29
1x5	etch Si	10	p^+	4.10	0.347	4950	443	1.28
1x15	full Si	5	p^+	43.7	0.733	1442	71.9	1.22
1x15	full Si	10	p^+	25.1	0.861	1092	93.1	1.23
1x15	etch Si	0	p^+	20.7	1.04	1201	96.8	1.25
1x15	etch Si	1	p^+	12.6	0.920	1152	153	1.25
1x15	etch Si	5	p^+	9.59	0.518	1600	197	1.18
1x15	etch Si	10	p^+	11.3	0.938	1125	168	1.27
1x50	full Si	0	p^+	677	4.514	478	13.5	1.28
1x50	full Si	1	p^+	68.3	2.749	667	32.6	1.21
1x50	full Si	10	p^+	48.7	3.229	294	41.9	1.26
1x50	etch Si	1	p^+	62.5	3.617	356	34.0	1.26
1x50	etch Si	5	p^+	53.5	2.728	335	40.5	1.24
1x50	etch Si	10	p^+	46.2	2.847	350	43.6	1.24
2x5	full Si	0	p^+	10.5	0.370	2919	198	1.24
2x5	full Si	1	p^+	9.22	0.190	2779	248	1.17
2x5	full Si	5	p^+	7.41	0.358	3029	266	1.25
2x5	full Si	10	p^+	7.29	0.401	3090	262	1.26
2x5	etch Si	0	p^+	7.06	0.292	3046	321	1.23
2x5	etch Si	1	p^+	8.31	0.261	3000	244	1.20
2x5	etch Si	5	p^+	8.67	0.297	2879	257	1.22
2x5	etch Si	10	p^+	5.13	0.466	2833	365	1.29
4x5	full Si	0	p^+	37.9	0.494	1834	60.9	1.23
4x5	full Si	1	p^+	15.6	0.311	1475	160	1.21
4x5	full Si	5	p^+	23.7	0.239	3297	117	1.14
4x5	full Si	10	p^+	25.3	0.300	1969	140	1.18
4x5	etch Si	1	p^+	18.4	0.309	2043	118	1.19
4x5	etch Si	5	p^+	19.2	0.329	2009	159	1.21
4x5	etch Si	10	p^+	18.3	0.328	1991	146	1.20

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14. ABSTRACT

As the digital age of rapidly expanding information systems and technology continue to grow and develop at an ever increasing rate, new fabrication media must be investigated in order to keep up with these trends. The modern age has been defined by the innovation and advancement of the semiconductor transistor specifically Silicon, however these days of exponential performance gain through gate minimization are coming to a close. One such field which shows great promise for meeting the challenges of the future is the integration of photonic and complementary metal oxide semiconductor components; leveraging the long standing fabrication history of Silicon devices. This document describes the characterization and analysis of integrated photodiodes for digital and analog applications. The photodiode is one small but necessary component for the integration of system-level photonic devices.
A number of standard measurements were taken on the photodiodes to analyze their performance and potential application. Additionally, an anomalous detector behavior was investigated through both transient measurements to identify the driving mechanism of the abnormality. Through this testing the devices were found to perform with up to 30-GHz of bandwidth while maintaining dark currents below 5 nA. The non-linear behavior was observed under CW conditions and analyzed using the transient response of the photodiode. The transient response of the photodiode supported that the non-linear mechanism was photon-induced avalanche-like effect, however, further investigation is required. Additional work is described to further investigate this behavior, as well to identify potential effects on future application in system level communication designs.

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