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OPERATIONAL CHARACTERISTICS OF AN SCR-BASED PULSE GENERATING CIRCUIT

by

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OPERATIONAL CHARACTERISTICS OF AN SCR-BASED PULSE GENERATING CIRCUIT

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ABSTRACT

A commercial off-the-shelf silicon controlled rectifier (SCR) was connected in series with a parallel *RC* load under DC bias to produce self-terminating voltage pulses. The physics underlying the switching mechanism of the SCR in such a circuit was investigated and the values of load resistance and capacitance varied to ascertain their role on the pulse-generating capability of the circuit. When pulsing was successfully achieved, a reverse recovery current was always present to return the SCR from its "on" state to its "off" state. In addition, the regenerative process responsible for turning the SCR is through the avalanche multiplication of charge carriers within the device. This appeared to be independent of the mode of triggering, either by increasing the DC bias or using a current at the gate. Significantly, pulsing was discovered to be sustainable for a specific range of RC values that depends on the SCR's intrinsic turn-off time. Specifically, it was found that without making modifications to the SCR itself, the minimum dead time achievable between pulses was essentially the turn-off time of the SCR. The findings of the research will help to design optimum SCR-based circuits for pulse mode detection of light and ionizing radiation without external amplification circuitry.

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LIST OF ACRONYMS AND ABBREVIATIONS

C_{BANK}	capacitor bank
C_{OUT}	output capacitor
I_A	anode current of thyristor
I_C	current through output capacitor
I_H	holding current of silicon controlled rectifier
I_R	current through resistor
I_S	switching current of silicon controlled rectifier
I_{SCR}	current through silicon controlled rectifier
SCR	silicon controlled rectifier
SCS	silicon controlled switch
t_{OFF}	turn-off time of silicon controlled rectifier
V_{AK}	anode voltage of thyristor with respect to cathode
V_{DC}	DC bias
V_H	holding voltage of silicon controlled rectifier
V_{RC}	voltage across resistor and output capacitor
V_S	switching voltage of silicon controlled rectifier

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I. INTRODUCTION

A. BACKGROUND

The thyristor, as defined by the International Electrotechnical Commission, is "any semiconductor whose bistable action depends upon p-n-p-n regenerative action" [1]. Of the many semiconductor devices that fall under the thyristor family, the silicon controlled rectifier (SCR) and the silicon controlled switch (SCS) are perhaps the most important and widely used. Notably, both devices are able to switch from a high impedance state (forward blocking mode) to a low impedance (conduction mode) state, depending on the external bias and the gate current applied [2]. This has resulted in their traditional application in the fields of electrical power and industrial electronics, particularly for power regulation and control, and the provision of excess and low voltage protection and short circuit current protection [1].

B. THYRISTOR THEORY OF OPERATION

The thyristor is essentially a p-n-p-n semiconductor structure with the top p-layer, device anode (*A*), acting as the hole emitter and the bottom n- layer, device cathode (*K*), as the electron emitter. The behavior of the thyristor in a circuit containing a series load resistor and DC bias will first be discussed before the physics of its operation is described qualitatively.

The I_A-V_{AK} characteristics of a typical thyristor along with a set of load lines corresponding to varying DC bias are shown in Figure 1, where I_A is the anode current and V_{AK} is the anode voltage with respect to the cathode. As V_{AK} is gradually increased from zero, the current through the thyristor increases at a much slower rate and remains low, as indicated by the operating points on the lower branch of the I_A-V_{AK} characteristic. The thyristor remains in the "off" state during this period. When DC bias (V_{DC}) is increased to V_{DC3}, the load line intersects the I_A-V_{AK} at an unstable point. The corresponding V_{AK} is known as the switching voltage of the thyristor, V_S, and increasing

V_{DC} beyond V_{DC3} switches the thyristor from a high-voltage, low-current ("off") state to a low-voltage, high-current ("on") state. In the "on" state, the thyristor is now operating on the upper branch of the I_A-V_{AK} characteristic as illustrated in Figure 1(a). When the device is in the "on" state, reducing V_{AK} will cause the thyristor to continue operating along the upper branch of the curve until I_A falls below the holding current, I_H as indicated in Figure 1(b). The thyristor is now in the "off" state and will continue operating on the lower branch of the I_A-V_{AK} characteristic until it is switched on again when V_{DC} is increased beyond V_S [3]–[5].

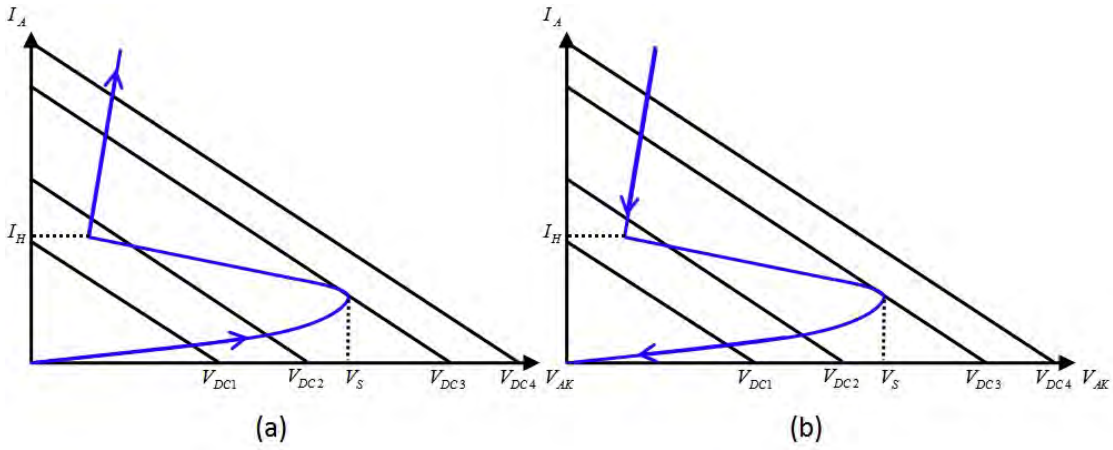

Figure 1. The p-n-p-n four layer diode in operation (after [3]). (a) Device is switching to its "on" state. (b) Device is switching to its "off" state.

The thyristor's switching phenomenon can be explained qualitatively through the use of energy band diagrams [3]. For a positive bias applied across the device, there exist two forward-biased p-n junctions and one reversed-biased junction, as seen in Figure 2a. The positive bias causes holes injected from the p_1 region to accumulate in the p_2 region because of the relatively narrower width of the n_1 region. This accumulation of holes in the p_2 region results in an overall decrease in the potential energy which causes the p_2 region to move down on the energy band diagram as seen in Figure 2(b). Consequently, this lowers the barrier at the reversed-biased n_1-p_2 junction which in turn

enables more electrons to be injected from the n_2 region into the p_2 region. These electrons subsequently accumulate in the n_1 region, due to the narrow p_2 layer, which eventually increases the potential energy in the n_1 region and moves it up on the energy band diagram. This regenerative process is limited by the recombination current at the forward-biased junctions, and for positive bias below V_S, the overall current is limited to a small value. However, as the bias is increased beyond V_S, all the junctions in the device are forward-biased, and large currents (limited to the loads in the circuit) are conducted across the device. This is illustrated in Figure 2b.

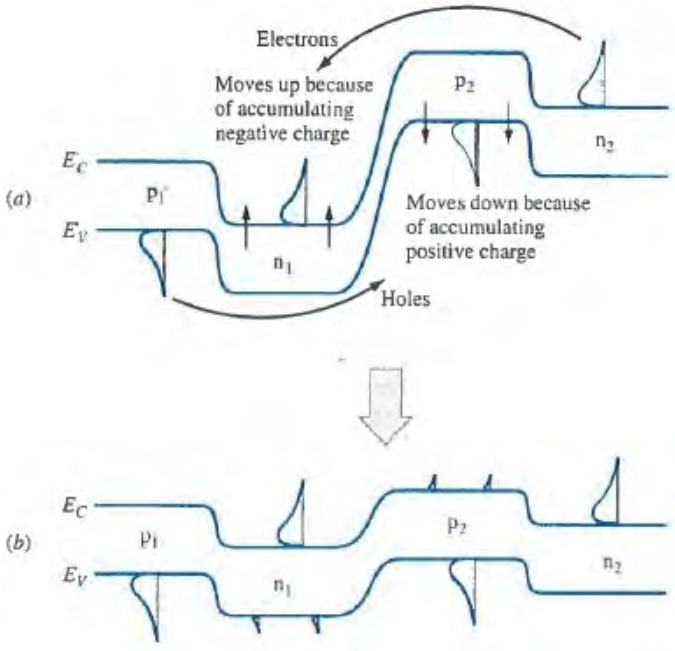

Figure 2. The energy band of the p-n-p-n device (from [3]). (a) Under positive DC bias, injected electrons accumulate in the n_1 region and injected holes accumulate in the p_2 region, thereby lowering the barrier at the reverse-biased junction. (b) Reverse-biased center junction has been triggered into a forward-biased junction.

In the case of an SCR, an additional gate is connected at the p_2 region as shown in Figure 3. This enables one to apply suitable current pulses at the gate and achieve the switching phenomena at significantly lower values of V_S. For example, a positive

current pulse applied at the gate injects holes to the p_2 region, thus making it more positive and therefore lowers it on the energy band diagram. This in turn reduces the barrier at the reversed-biased n_1 - p_2 junction and kick-starts the regenerative process previously described (see Figure 4). Intuitively, the application of a positive current at the gate would mean that less injection current is required at the device's anode, and therefore lower values of V_S can be achieved.

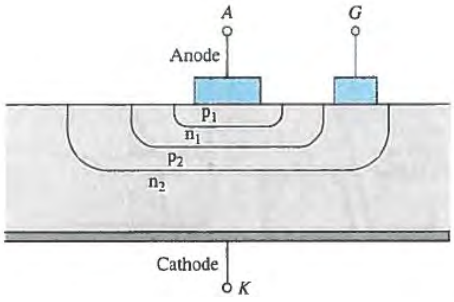

Figure 3. Schematic diagram of the SCR (from [3]).

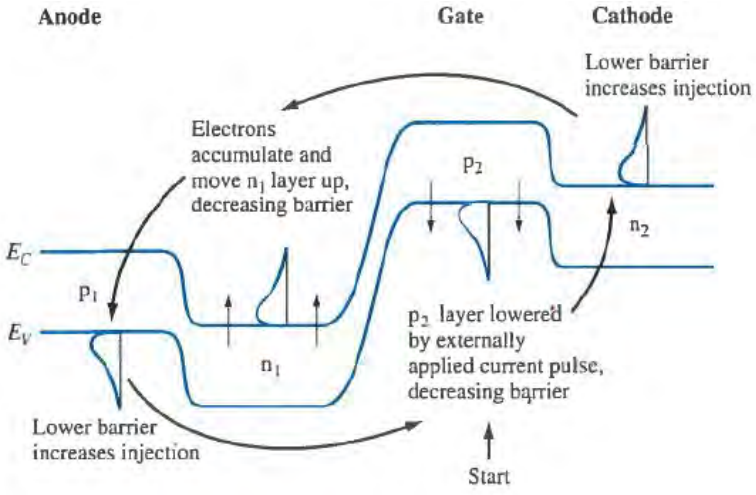

Figure 4. The energy band diagram of the SCR (from [3]). In this case, switching of the SCR to its "on" state is via the application of a gate current.

C. RECENT DEVELOPMENTS

More recently, the possible exploitation of the SCR/SCS in other more novel applications has been explored. It has been demonstrated that an SCR connected in series with a parallel *RC* circuit under DC bias, as shown in Figure 5, was able to generate self-terminating voltage pulses spontaneously, with the pulse rate increasing as the DC bias was increased and saturating as the pulse period approached the *RC* time constant of the circuit (see Figure 6). When a photodiode was connected to the gate terminal of the SCR, the pulse rate was observed to increase with light intensity, as shown in Figure 7. This lends credence to the possibility of adapting the SCR-based circuit as a pulse mode light detector [6]. The use of such a simple circuit could potentially be extended to applications that require the generation of voltage or current pulses in response to DC stimulations, for example, in pulse mode optical sensing for the detection of light sources [7] and in neural stimulators for retinal implants [8].

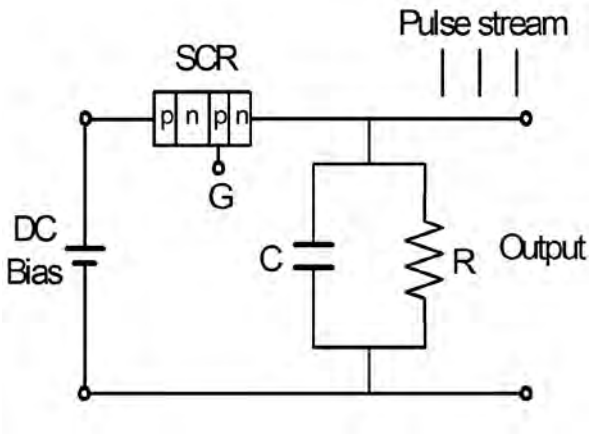

Figure 5. Schematic diagram of a pulse-generating circuit using an SCR connected in series with a parallel *RC* ($R = 33$ kΩ and $C = 22$ nF) load under DC bias (from [6]).

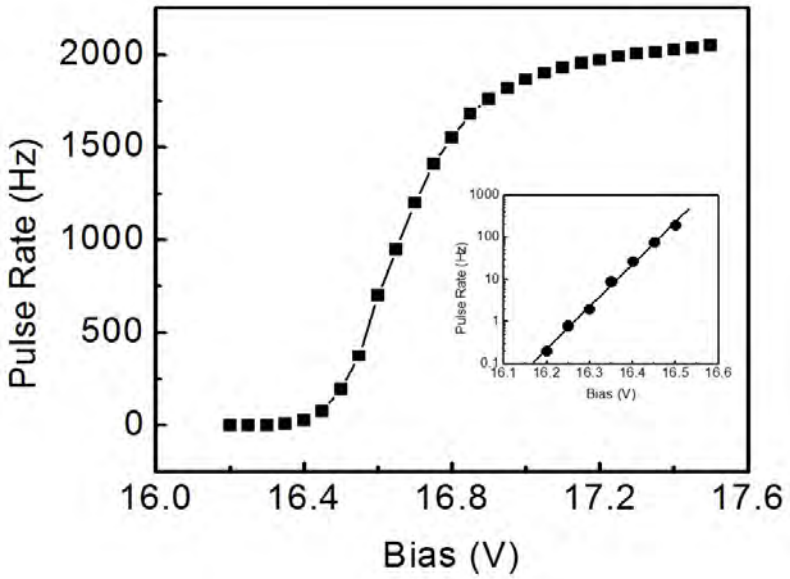

Figure 6. Measured pulse rate as a function of DC bias across the circuit (from [6]). Saturation of the pulse rate at high bias is due to the *RC* time constant of the output circuit. For the parameters used (*RC* = 0.71 ms) saturation occurs around 1.4 kHz.

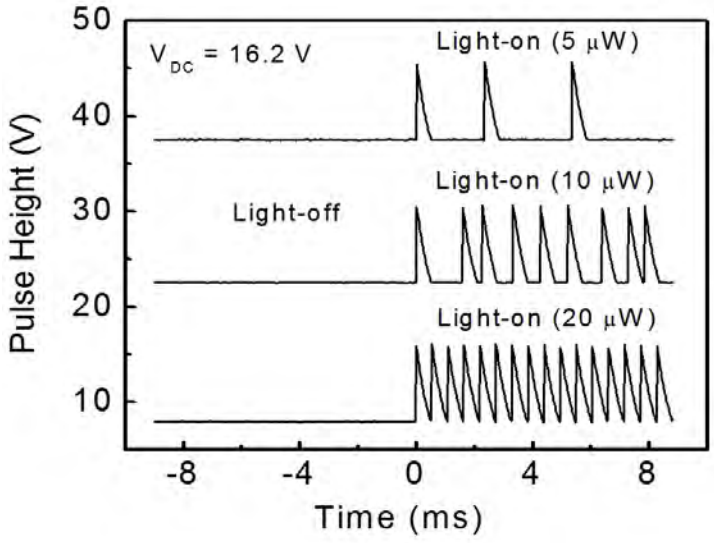

Figure 7. Measured pulse sequences under light illumination at three different intensities (from [6]). The DC bias across the circuit was kept at about 16.2 V and no pulses were observed in the absence of light.

The work performed on the use of the SCR-based circuit as a pulse mode light detector was also extended to the field of radiation detection. Notably, a SCS-based detector circuit was demonstrated to be able to detect ionizing radiation successfully [2]. As per the pulse mode light detector configuration, an SCS connected in parallel to an *RC* load was able to generate large voltage pulses in response to the ionization events when exposed to alpha particle radiation from an Am-241 source and beta particle radiation from a Cs-137 source impinging on the reverse-biased middle p-n junction of the SCS, as shown in Figure 8.

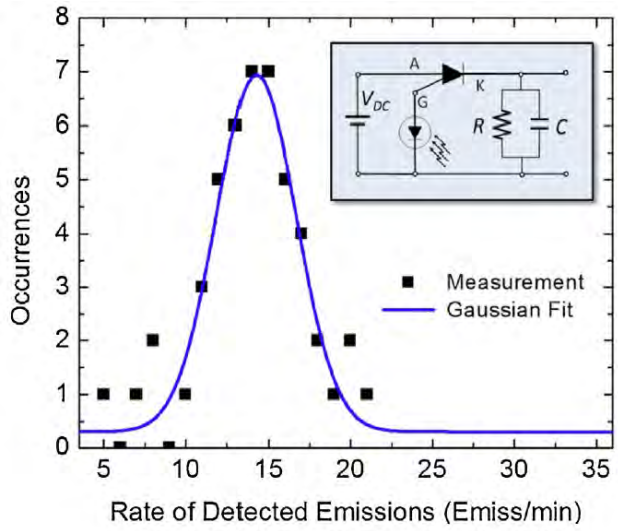

Figure 8. Compilation of the rate of detected emissions per minute (solid squares) of a source of Cs-137, measured using a silicon p-i-n photodetector connected to the gate of the SCS as shown in the inset (from [2]). The solid line is a Gaussian fit with the average detection rate of 15 per minute.

The advantages of using solid state radiation detectors [9], [10] are three-fold. Firstly, the use of solids as a detecting medium, which are about 1000 times denser than the gases used in gas ionization chambers, ensures that the resultant size of the semiconductor detector is significantly less bulky since much smaller volumes are required for capturing and detecting the radiation. Secondly, the ionization energy required to generate a detection signal in semiconductor detectors is about an order of magnitude lower than that of gas detectors, and this consequently improves the energy

resolution in the former significantly. In the case of a scintillator, while the fundamental ionization energy required is comparable to that of a semiconductor detector, the inefficient processes involved in the conversion of the ionization events into light pulses and the subsequent conversion of photons into photoelectrons in the photomultiplier, adversely impact the energy resolution available [11]. Thirdly, the SCS-based detector is modeled as an electronic equivalent to a spark chamber [12], [13]. By biasing it near to a trigger point, the SCS-based detector is able to return a large signal pulse with little or no additional amplification circuitry. This is in stark contrast to a typical semiconductor radiation detector, where additional circuitry, such as low-noise/high-gain amplifiers, is essential to recover the relatively small current typically generated by the ionizing radiation.

D. IMPETUS FOR THESIS

It was proposed that the SCS-based radiation detector is potentially able to combine the advantages of the small size and low power consumption of semiconductor detectors with the high gain and sensitivity of the gas detectors [2]. Notwithstanding, work on the SCS-based detector is still in its nascent stages. One key concern is the dead time between the voltage pulses returned, during which any radiation incident on the detector will not be picked up. This is limited by the *RC* time constant of the circuit used [2], and cannot be resolved by arbitrarily reducing the sizes of the resistive loads and capacitance used in the circuit.

The inability to arbitrarily reduce the sizes of the resistive loads and capacitance used is inherently due to the nature of the thyristor's I-V characteristic. Notably, it was proposed that for pulses to be sustained [6], the load line of the circuit has to intersect the thyristor's I-V characteristic at only one point between the device's holding current, I_H, and switching current, I_S, or during the unstable transition regime of the device between its "on" and "off" states, as shown in Figure 9. The equation of the load line is given in (1).

$$V_{DC} = V_T + I_R R \tag{1}$$

where V_{DC} is the DC bias, V_T is the voltage across the SCR, I_R is the current in the circuit and R is the series load resistor.

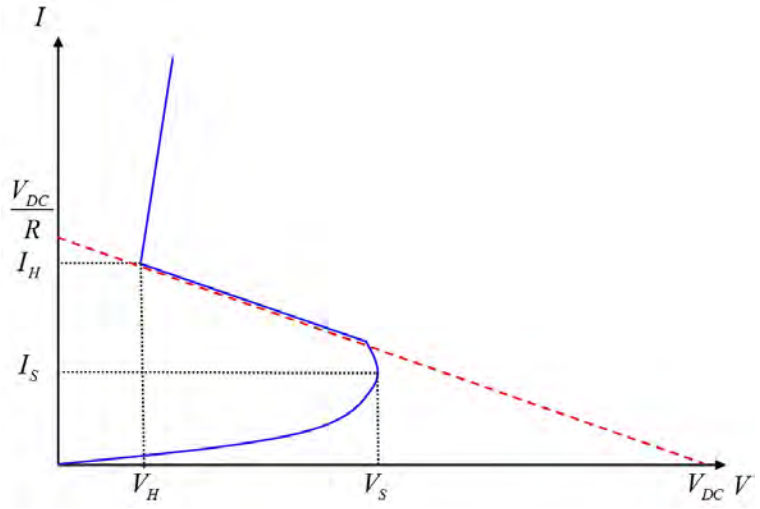

Figure 9. Static load-line switching criteria for thyristor. Load-line lies in unstable transition regime of device between "on" and "off" states.

Intersection of the load line anywhere else on the I-V characteristic results in the device remaining in either the "on" or "off" state and no pulsing is achieved. This constraint on the placement of the load line means that the size of the resistor, R, must be small enough to maintain the steady current above I_S for turning the device on, and yet large enough to keep the current below I_H for switching the device off (i.e. the operating point should be an unstable point along the unstable regime of the device's I-V characteristic). In addition, if the transition regime in the I-V characteristic of the device is flatter or less inclined, larger resistor values, and consequently larger DC biases, would be required for pulsing. Conversely, a more inclined transition regime in the I-V characteristic would allow smaller resistor values to be chosen.

The objective of this thesis is therefore to re-examine the SCR-based pulse generating circuit developed in [6], and determine how changes to the *RC* parameters of the circuit impact its pulse generating capabilities, with the aim of improving the sensitivity and speed of operation of the SCS-based radiation detector.

E. THESIS ORGANIZATION

This thesis is organized in the following manner:

Chapter II describes in detail how the SCS-based circuit was used to study the intrinsic switching characteristic of the thyristor. Emphasis is placed on how the DC bias was regulated, how the IV characteristics of the thyristor were determined, and how the values of the resistance and the capacitance in the load circuit were varied to observe their impact on the voltage and current pulses generated.

Chapter III presents and analyzes the observations made on the pulse-generating capability of the circuit when resistance and capacitance were varied. Significantly, key observations underpinning the switching mechanism of the device are discussed here, along with the development of the dynamic I-V characteristics of the thyristor.

Chapter IV concludes the thesis and provides recommendations for future research work.

II. EXPERIMENTAL SETUP

A. PULSE GENERATING CIRCUIT

The MBS 4993 silicon bidirectional switch was the SCR of choice due to its low voltage switching characteristics (low V_S of 8 V typically). The I-V characteristic of this device was determined using the circuit shown in Figure 10. The DC bias was steadily increased from 0 V and values of V_{DC} and V_R recorded. The potential difference across the device $\left(V_T = V_{DC} - V_R\right)$ was plotted against the current through it $\left(I_R = V_R / R\right)$ to give the I-V characteristic in Figure 11.

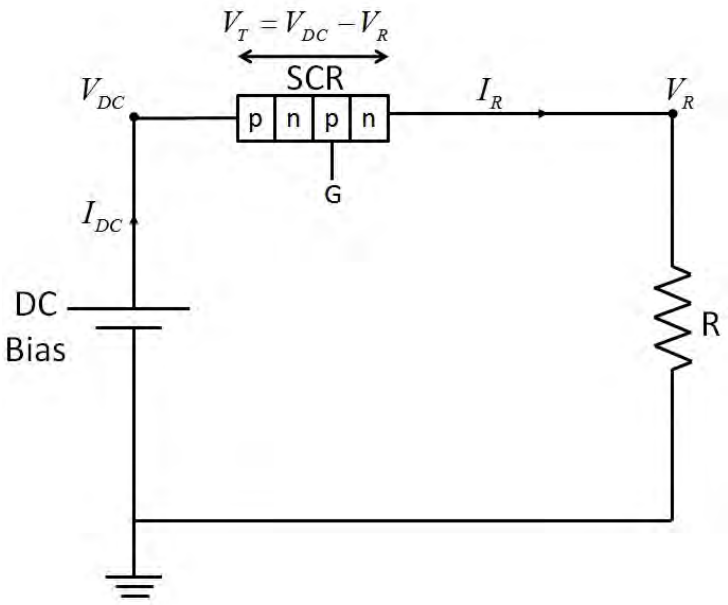

Figure 10. Schematic of circuit used to determine I-V characteristic of MBS 4993 SCR.

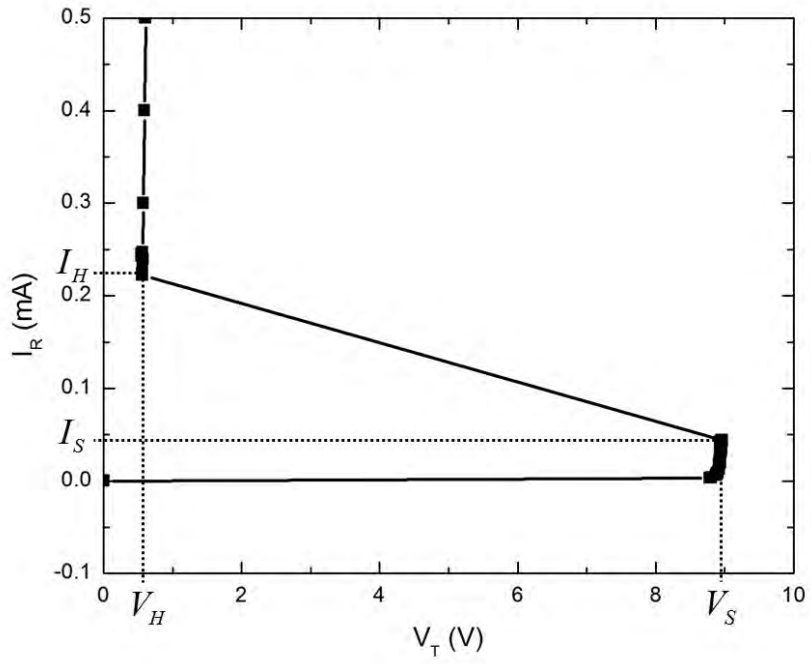

Figure 11. Measured I-V characteristic of MBS 4993 SCR. I_S and V_S are 0.044 mA and 8.96 V, respectively, while I_H and V_H are 0.223 mA and 0.562 V, respectively.

The device was then placed in a circuit board adapted after the SCR-based pulse generation circuit previously developed [6], and as depicted in Figure 12 (schematic of the circuit) and Figure 13 (assembled circuit). Connections were made from an oscilloscope to key nodes of the circuit to enable the transient analysis of the voltage just before the SCR (V_{DC}), current through the SCR (I_{SCR}), the voltage just after the SCR (V_{RC}), and the currents through the resistor (I_R) and the capacitor (I_C). These are the notations that will continue to be used to reference the voltages and currents being discussed in the subsequent chapters.

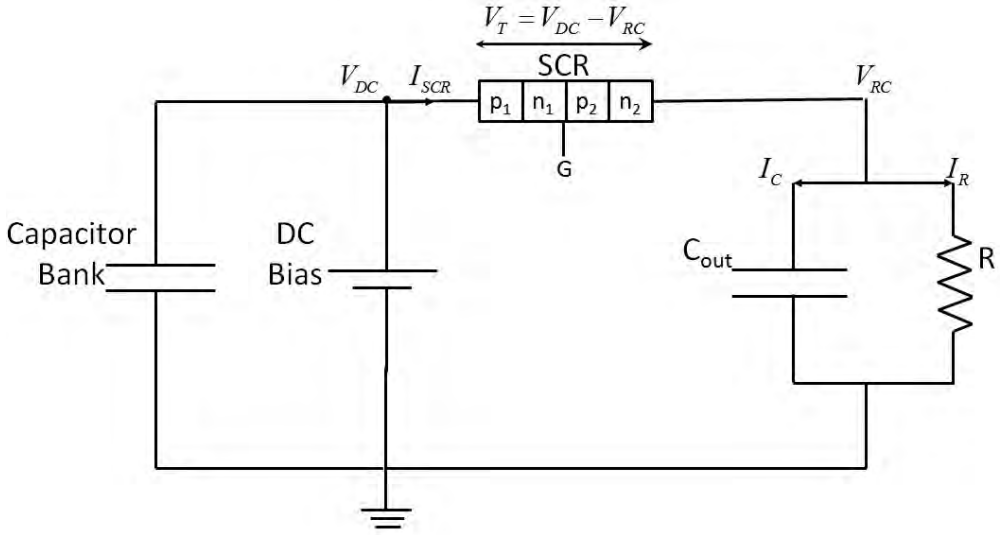

Figure 12. Schematic of pulse generating circuit showing the DC power supply along with a capacitor bank to keep the V_{DC} constant during the SCR switching.

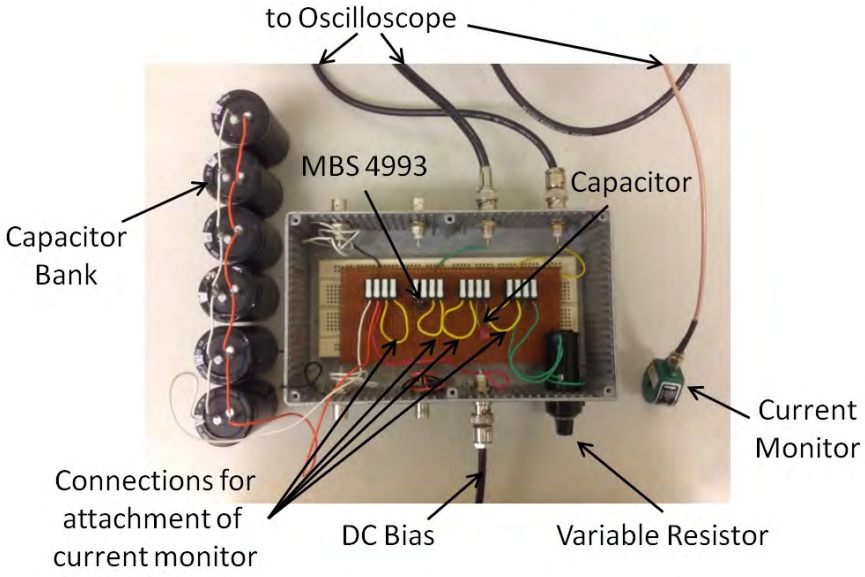

Figure 13. Picture of pulse generating circuit with MBS 4993 (SCR) connected in series with a parallel *RC* load.

B. SELECTION OF RESISTORS

As previously discussed, the size of the resistor to be used has to be small enough to maintain the steady current above I_S for turning the device on, and yet large enough to keep the current below I_H for switching the device off. This is summarized by the following relations:

For the SCR to switch on,

$$I_R \geq I_S \Rightarrow \frac{V_{DC} - V_S}{R} \geq I_S \tag{2}$$

For the SCR to switch off,

$$I_R \leq I_H \Rightarrow \frac{V_{DC} - V_H}{R} \leq I_H \tag{3}$$

For a desired DC bias of approximately 11 V, an initial resistor value of 47 kΩ was chosen to initialize the pulsing.

C. INCORPORATION OF CAPACITOR BANK

In the early stages of the experiment, oscillations or ringing were observed at the V_{DC} node of the circuit during the switching process although the value should remain constant (see Figure 14). As the potential difference across the SCR, V_T, was increased beyond V_S, the SCR switched from a high impedance state to a low impedance state, resulting in a sudden surge in the current through the circuit. It was hypothesized that the oscillations observed in the transient response of V_{DC} was due to the inability of the power supply to meet the surge in current during the switching process. Note that nearly all the transient current during switching passes through the output capacitor due to its smaller impedance as compared to the load resistor.

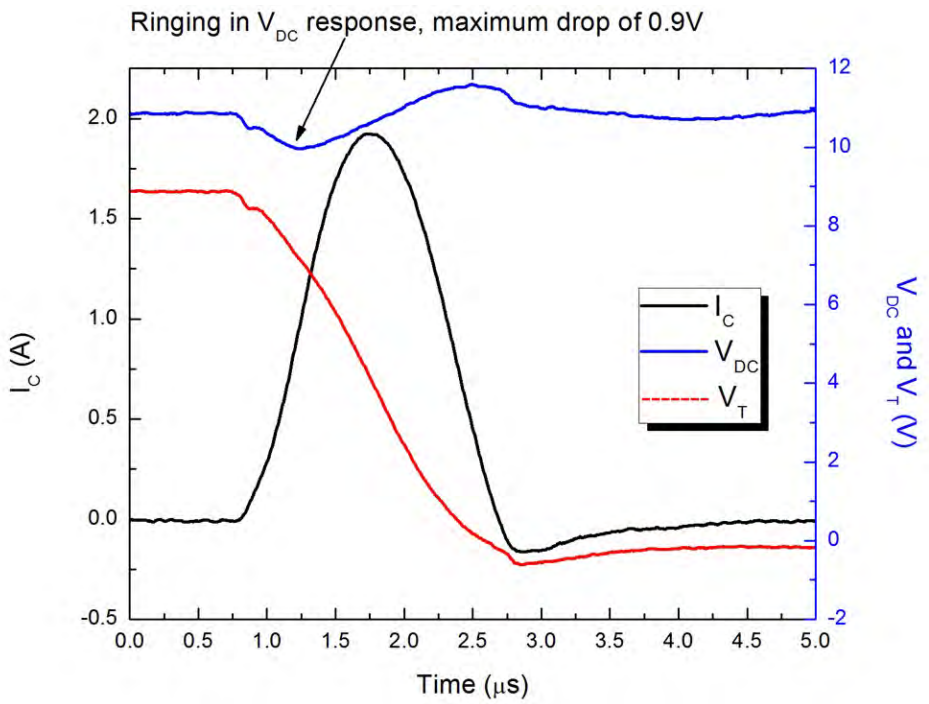

Figure 14. Measured V_{DC}, I_C and V_T during switching of SCR. A ringing was observed in the V_{DC} transient response. This data is for a circuit with $R = 47$ kΩ and $C_{OUT} = 217$ nF.

To test this hypothesis, a capacitor bank was connected in parallel to the voltage source as previously depicted in Figure 12, while a 47 kΩ resistor and a 217 nF capacitor were connected in parallel to the SCR to initiate pulsing. It was proposed that an adequately sized capacitor bank would possess the necessary amount of stored charges required by the surge in current during the SCR's switching process, thus curtailing the emergence of oscillations in the V_{DC} response. To determine the size of the capacitor bank required, capacitors were added to the bank in increments of 22 μF or 33 μF, and the rise time of the V_{RC} pulses measured for each incremental step. The rise time of the V_{RC} pulses, as a function of the size of the capacitor bank, was found to saturate for values of capacitance beyond 121000 μF, as shown in Figure 15, which suggested that capacitor banks larger than this would possess sufficient stored charge to meet the demands of the SCR's switching process. A 165000 μF capacitor bank was then included in the circuit.

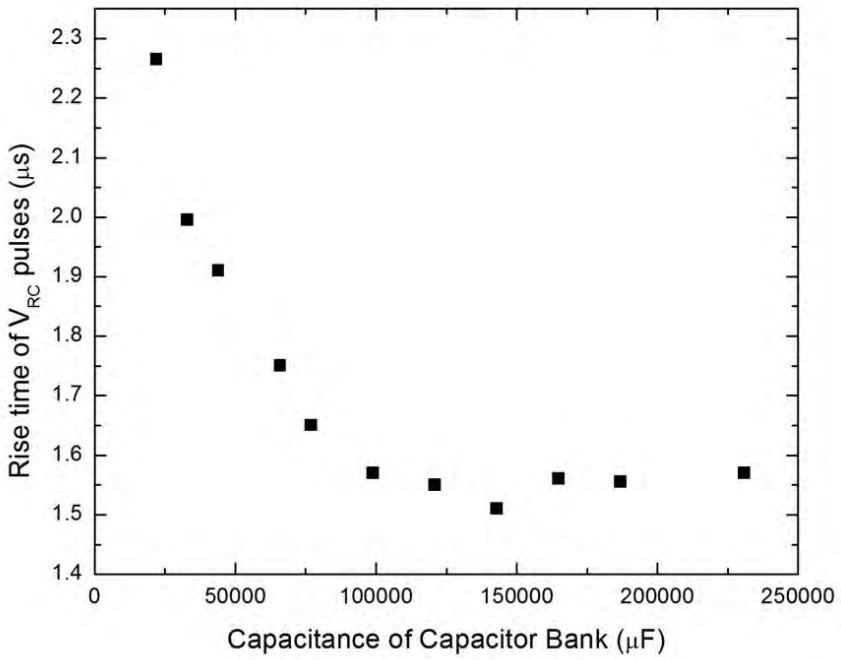

Figure 15. Rise time of V_{RC} pulses saturates beyond capacitor banks larger than 121000 μF.

Notwithstanding, ringing continued to be observed even after the inclusion of the 165000 μF capacitor bank, with a significant pull-down of 0.9 V in the V_{DC} transient response during the switching process. An analysis of the charge transfer from the capacitor bank to the output capacitor during the switching process was then performed in an attempt to understand this behavior.

The reduction of charge in the capacitor bank due to the pull-down in the DC level, ΔV_{DC}, can be estimated using

$$\Delta Q = \Delta V_{DC} C_{BANK} \tag{4}$$

The amount of charge stored by capacitor, C_{OUT}, during switching can be estimated using the measured current I_C:

$$I_C = \frac{\Delta Q}{\Delta t} = \frac{C_{OUT} V_{RC}}{\Delta t} \tag{5}$$

If the reduction of charge on the capacitor bank is used for charging the output capacitor, the pull down in DC level is given by:

$$C_{OUT}V_{RC} = \Delta V_{DC}C_{BANK} \tag{6}$$

$$\Delta V_{DC} = \frac{C_{OUT}V_{RC}}{C_{BANK}} \tag{7}$$

Using (7), the pull-down in the V_{DC} voltage was found to be approximately 14 μV, for a capacitor bank, C_{BANK}, of 165000 μF and C_{OUT} of 217 nF. This was significantly smaller and contrary to the actual pull-down observed, which suggests that the ringing observed on the oscilloscope was not due to the sudden demand of charges during pulsing since the capacitor bank was theoretically able to stabilize the V_{DC} transient response. It was concluded that the ringing was therefore caused by the inductive loading of the probe connected to the oscilloscope during pulsing. The fast rise time (□ < 1 μs), coupled with the surge in current accompanying each pulse indicate that the rate of change of current with time, $\frac{dI}{dt}$, was large (□ 1A/ μs). This was likely to have induced a back emf, which presented itself as the large pull-down in the V_{DC} transient response observed during pulsing. For the thesis work that followed, the 165000 μF capacitor bank was included in the circuit, with the ringing in the V_{DC} transient response ignored.

Measurements of the transient responses of voltages and currents at the key nodes of the circuit were measured as C_{OUT} was varied from 1 nF to 1024 nF for a fixed load resistor of 47 kΩ, and again as R was varied from 800 Ω to 50 kΩ for a selected value of C_{OUT}. These were analyzed to determine the effect both C_{OUT} and R had on the pulse generating capability of the circuit.

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III. RESULTS AND ANALYSIS

A. REVERSE CURRENT OBSERVATIONS DURING SWITCHING

The transient analysis of I_C with variations in C_{OUT} (between 1 nF to 1024 nF) provided useful insights into the switching characteristic of the circuit. Figure 16 shows a typical switching characteristic of the SCR. When the SCR begins to switch from its "off" state to its "on" state, I_C increases from I_S to a maximum value before falling back to very a small value again. In addition, the increase in C_{OUT} increases the maximum value of I_C, and also lengthens the duration of the positive current surge as shown in Figure 17. This is expected because the larger C_{OUT} will undoubtedly draw more charges across the SCR when the latter is turned on, while the longer period of positive current surge is determined by the $R_{SCR}C_{OUT}$ time constant of the circuit, where R_{SCR} is the resistance of the SCR. The amount of charge in C_{OUT} is estimated by integrating the positive I_C and the result is observed to agree closely to that obtained using (5). This substantiates the assumption that the duration of the positive current surge corresponds to the period when the SCR is in the "on" state and that all the current passed through the device goes towards charging C_{OUT}.

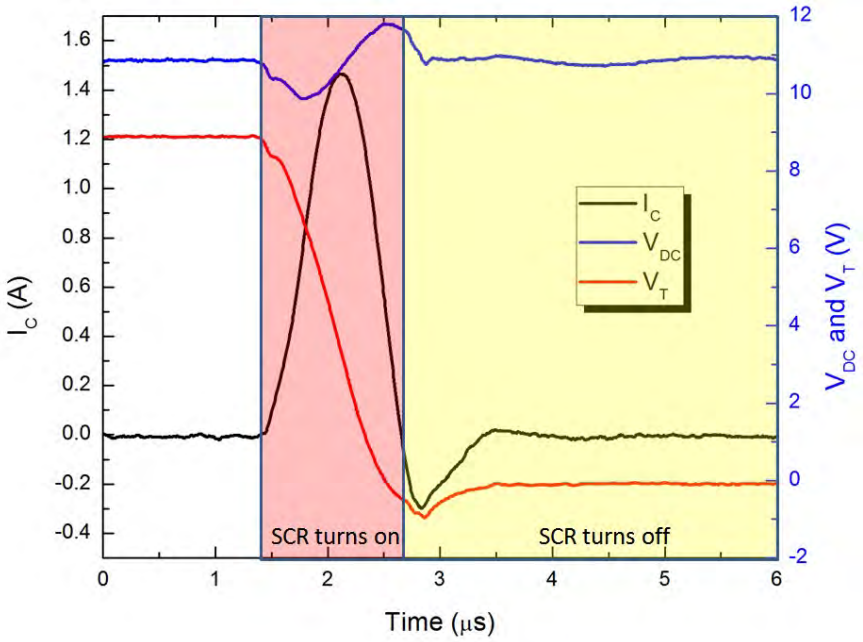

Figure 16. Breakdown of switching process of the SCR. I_C begins to increase while V_T drops as the device turns on. This data is for a circuit with R = 47 kΩ and C_{OUT} = 100 nF.

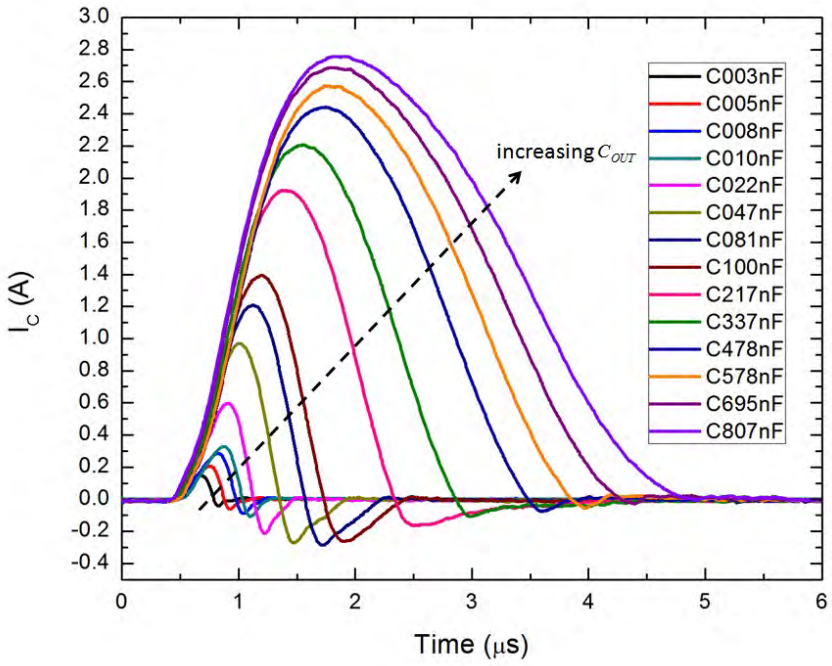

Figure 17. Measured variation of I_C with C_{OUT}. Magnitude of reverse current decreases as C_{OUT} approaches the limits of pulsing.

More significantly, it was found that I_C goes to zero just as the voltage drop across the device, V_T, decreases to zero. Thereafter, a negative I_C phase, accompanied by a negative V_T across the SCR exists. This indicates that the regenerative process due to the avalanche multiplication of charges within the middle p-n junction of the SCR generates additional current which charges the output capacitor above the DC bias. Note that the negative I_C is almost negligible for values of C_{OUT} for which no pulsing occurs (i.e. when C_{OUT} 1 nF or C_{OUT} 1024 nF). Between these values of C_{OUT} where pulsing is observed, the I_C decreases to a minimum of -0.287 A at C_{OUT} = 81 nF, before increasing back towards zero as C_{OUT} is increased (see Figure 18).

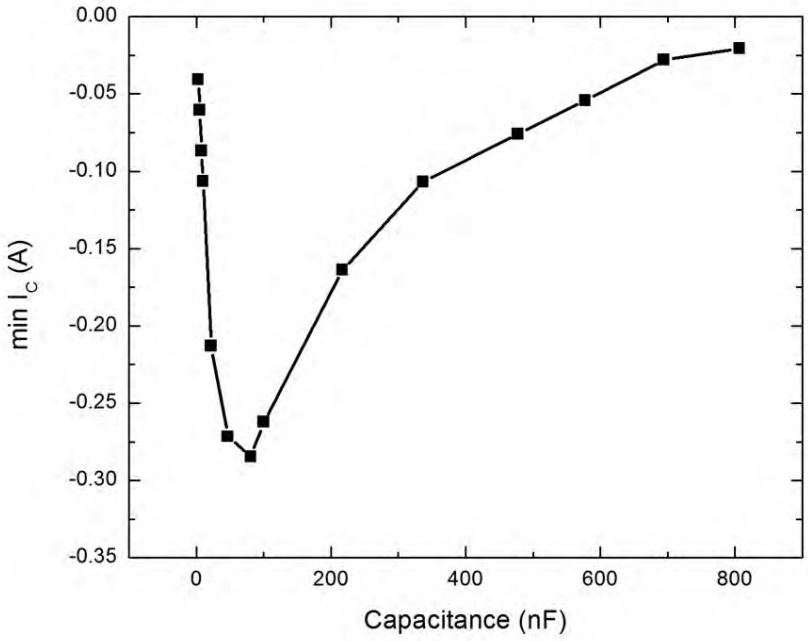

Figure 18. Variation of minimum I_C with C_{OUT}.

The existence of a negative I_C phase when pulsing occurs, and the lack thereof when pulsing cannot be achieved, suggests that the reverse current through the SCR is the trigger for switching the device from its "on" state to the "off" state. The process whereby the SCR is switched from the "on" state to the reverse blocking "off" state via a

reverse current is referred as the reverse recovery [14]. In its low-impedance, high-current "on" state, all of the SCR's junctions ($p_1 - n_1$, $n_1 - p_2$ and $p_2 - n_2$) are forward biased and a large concentration of free carriers exist in the drift region, thus accounting for the low V_T. To return the SCR to its "off" state, the central $n_1 - p_2$ junction has to return to its reverse-biased state, and the free carriers removed to enable the formation of a depletion region that can support a high electric field [14]. This is done via a reverse current, which occurs when V_T is negative, and persists till sufficient free carriers are removed from the middle junction. During this period of negative bias across the device, holes injected from the n_2 region accumulate in the n_1 region due to the relatively narrower width of the p_2 region. The accumulation of holes in the n_1 region results in an overall decrease in potential energy which causes the n_1 region to move down the energy band diagram. Likewise, electrons injected from the p_1 region accumulate in the p_2 region which result in an overall increase in potential energy and cause the p_2 region to move up the energy band diagram. Consequently, this raises the barrier at the forward-biased $n_1 - p_2$ junction, which eventually returns to its original reverse-biased state.

B. EFFECT OF CAPACITANCE ON PULSING

The effect of capacitance on the pulse generating capability of the circuit was examined by varying the capacitance from 1 nF to 1024 nF, with the resistor value maintained constant at 47 kΩ. Pulsing was achieved for values of C_{OUT} between 1 nF and 1024 nF. When C_{OUT} was set at 1 nF and 1024 nF, respectively, no pulsing was observed. The SCR switched to its "on" state and was unable to revert to its "off" state. The measured voltage across the thyristor, V_T, and current through the load resistor, I_R, for each value of C_{OUT} used are summarized in Figures 19 to 22.

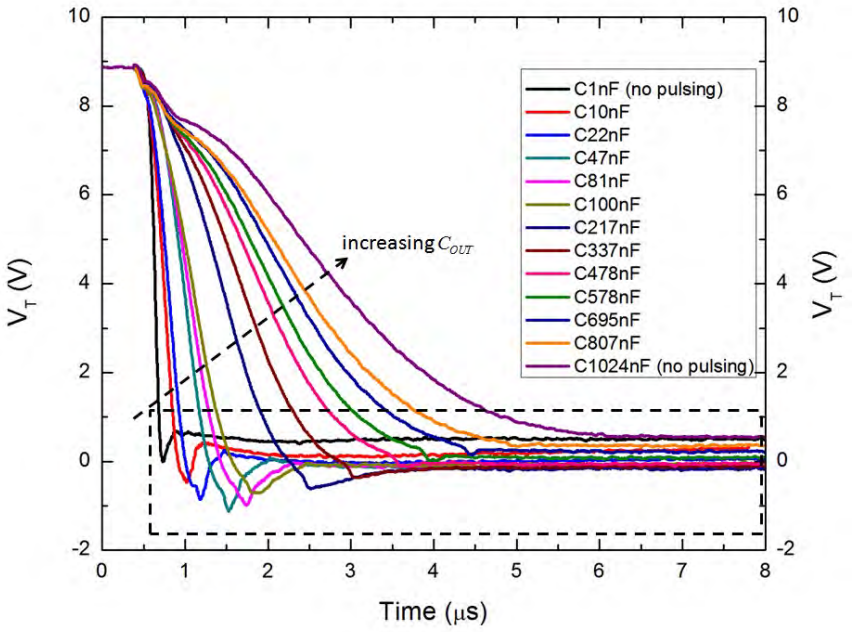

Figure 19. Dependence of V_T with time during switching for a set of C_{OUT} values. Magnified view of dependence of V_T with C_{OUT} is illustrated in Figure 20.

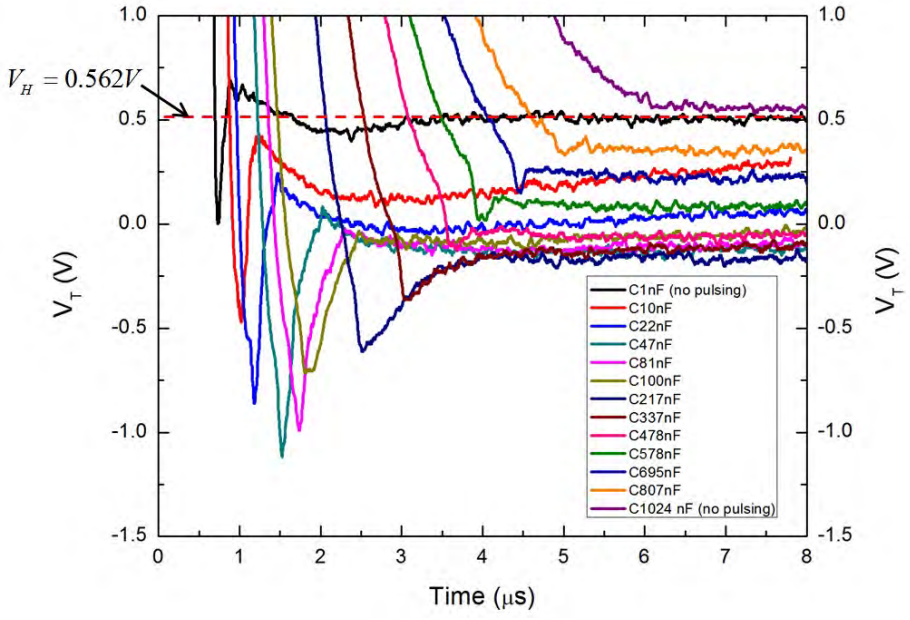

Figure 20. Magnified view of dependence of V_T with C_{OUT}. It can be seen that for output capacitors of 1 nF and 1024 nF where pulsing is not achieved, V_T does not fall below V_H during most of reverse recovery period.

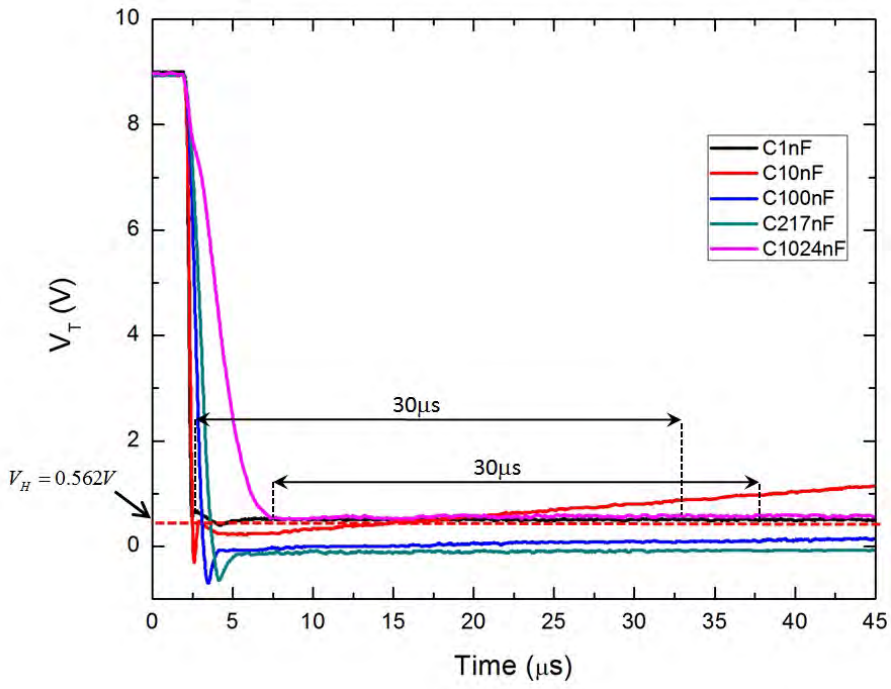

Figure 21. Dependence of V_T with time for a selected set of C_{OUT}. For output capacitors of 1 nF and 1024 nF where pulsing is not achieved, V_T does not fall below V_H even after the SCR's turn-off time of 30 µs.

Two stark observations are immediately apparent from Figures 19 and 20. Firstly, it can be seen that for all values of C_{OUT}, V_T first decreases rapidly from 8.9 V to a minimum value when switching occurs, then increases fairly rapidly to a transient peak before flattening out and thereafter returning to its pre-pulsed value of 8.9V at the end of each pulse (not shown due to long duration of time). Secondly, for C_{OUT} of 1 nF and 1024 nF where pulsing is not achieved, the values at which V_T plateaus are above the SCR's holding voltage (V_H = 0.562V). This observation holds true even after the SCR's specified turn-off time, t_{OFF}, of 30 µs, as shown in Figure 21. As C_{OUT} is increased from 1 nF, the value at which V_T plateaus is observed to decrease to a minimum of -0.18V at 217 nF before increasing steadily again. In addition, at the initial stage of discharging of C_{OUT}, I_R does not increase beyond the SCR's holding current (I_H =2.23 mA) for C_{OUT} of 1 nF and 1024 nF (where no pulsing was observed) as shown in Figure 22.

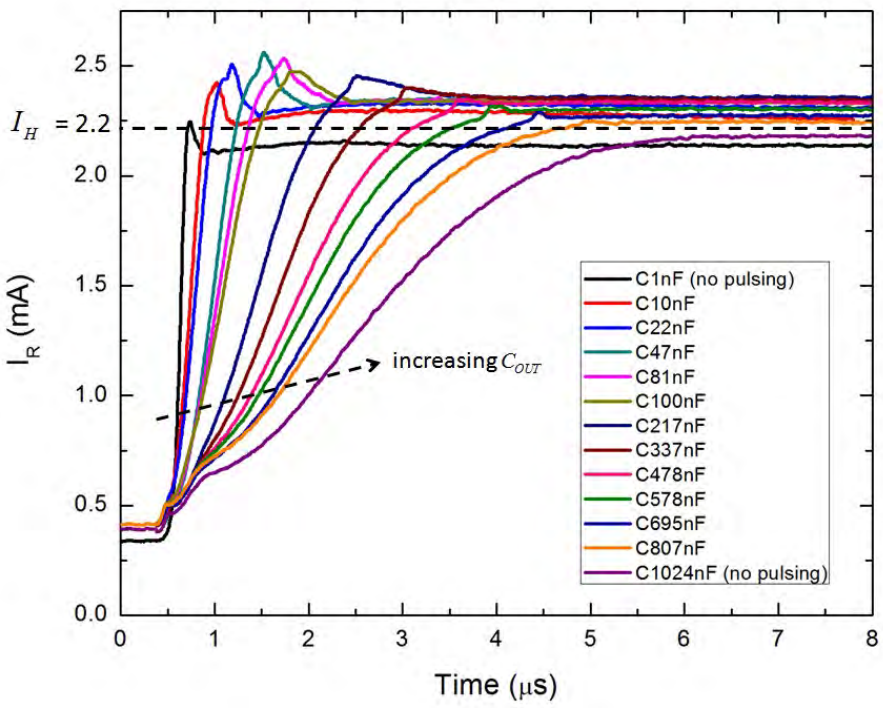

Figure 22. Variation of I_R .with C_{OUT} . I_R does not increase beyond I_H for C_{OUT} = 1 nF or 1024 nF.

The SCR's ability to switch from its "on" state to its "off" state is dependent on V_T falling below V_H, and I_R increasing beyond I_H. The lack of pulsing observed for C_{OUT} of 1 nF and 1024 nF is therefore due to V_T and I_R failing to meet these criteria. In addition, the manner in which V_T varies with C_{OUT}, as shown in Figure 23, suggests that there exists a range of values of C_{OUT} for which pulsing is most favorable (i.e where V_T is much smaller than V_H).

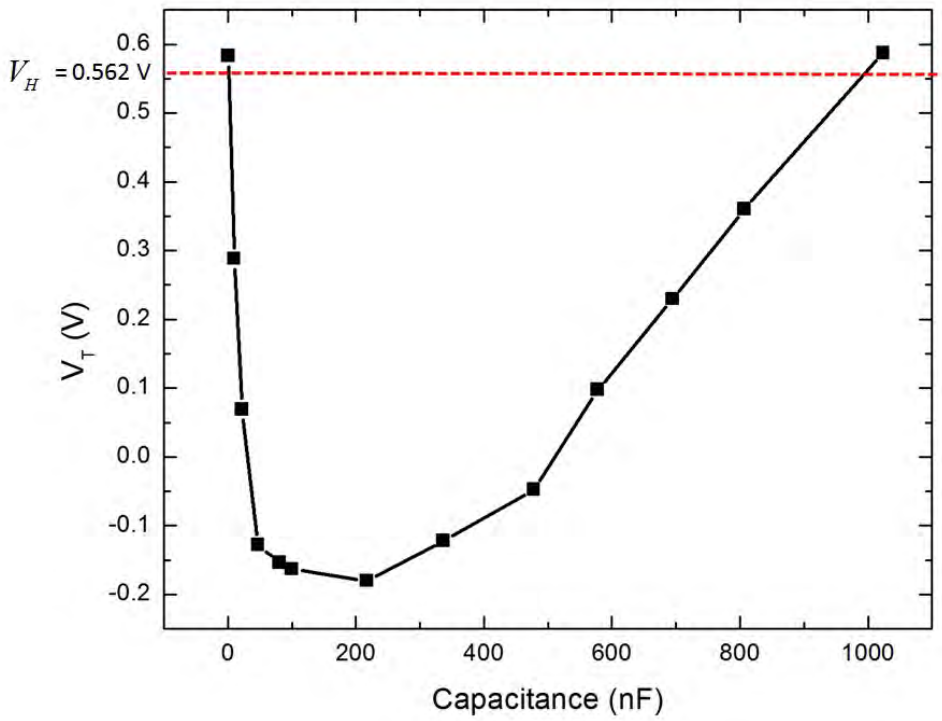

Figure 23. Variation of V_T with C_{OUT}, just after SCR is switched on. The pulsing of the circuit requires V_T to be below V_H.

The lack of pulsing achieved at the extreme ends of C_{OUT} can further be explained by the RC time constants involved in the charging and discharging of C_{OUT} during each pulse. When the SCR is switched to its "on" state, C_{out} is being charged and its rate of charging is governed by the $R_{SCR}C_{OUT}$ time constant, where R_{SCR} is the dynamic resistance of the SCR when it is conducting, which is typically a few ohms. When C_{OUT} is fully charged, V_T across the SCR is at its minimum and the SCR commences switching back to its "off" state. During this period, C_{OUT} discharges through R and this discharge rate is governed by the RC_{OUT} time constant. For a high C_{OUT} of 1024 nF, pulsing does not occur because the time it takes for the large capacitor to fully charge is substantially longer than the turn-off time of the SCR, t_{OFF}, as summarized in (8).

$$R_{SCR}C_{OUT} > t_{OFF} \tag{8}$$

Thus, the voltage across the SCR, V_T, does not fall below the device's holding voltage, V_H, within the device's turn-off time. The device remains in the "on" state without being able to revert to its "off" state, and no pulsing occurs. In order to determine the upper limit of C_{OUT}, R_{SCR} was estimated using the data in Figure 19. The plots of $\log_e(V_T)$ with time, for a set of output capacitor values, show linear dependence as illustrated in Figure 24 due to the charging of C_{OUT} via the "on" state resistance of the SCR. The dynamic resistance of the SCR varies from 36.7 Ω to 1.4 Ω as the size of the output capacitor is varied from 1 nF to 1024 nF (see Figure 25). In addition, the turn-off time of the SCR used (MBS4993) as specified in the data sheet is about 30 μs [15]. This gives the upper limit of the output capacitor needed as 20 μF, which agrees fairly well with the experimental observations.

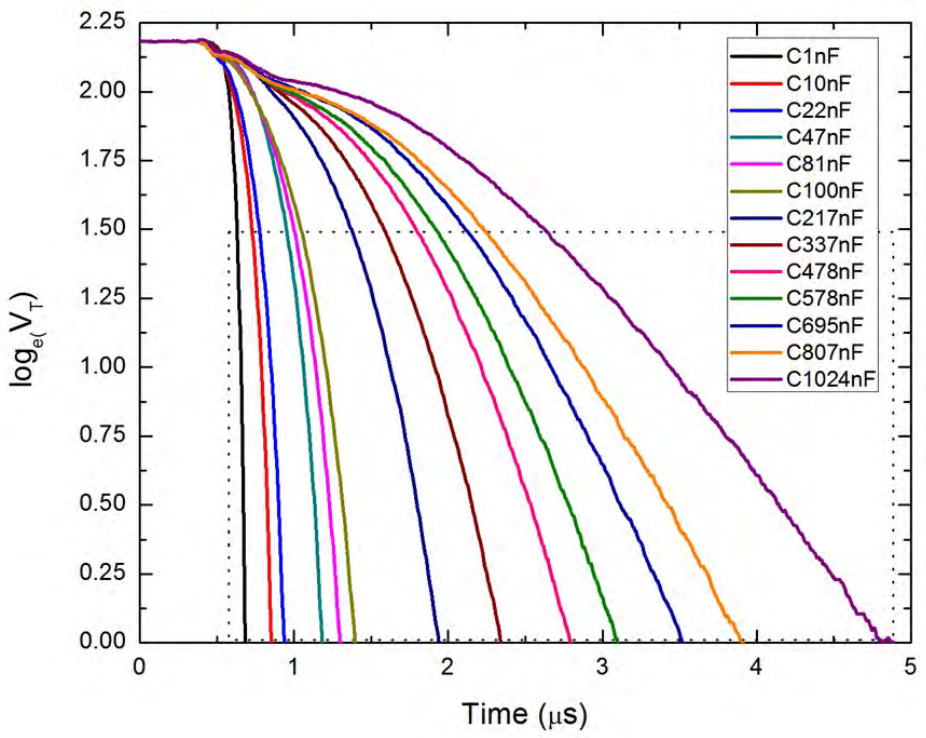

Figure 24. Variation of $\log_e(V_T)$ with time for a set of output capacitor values. Linear dependence observed for values of $\log_e(V_T)$ between 0 and 1.5.

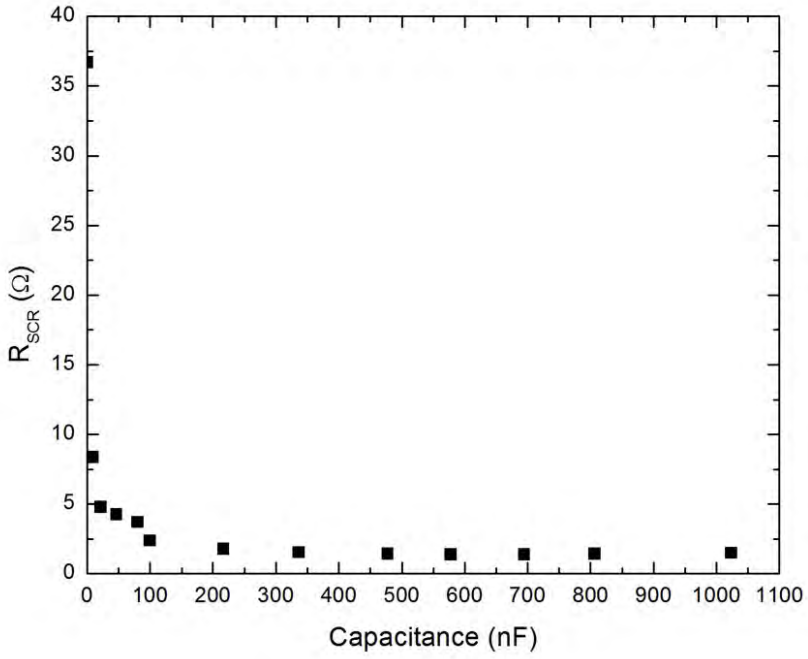

Figure 25. Variation of R_{SCR} with output capacitance, C_{OUT}.

On the other hand, pulsing does not occur for small values of C_{OUT} because the time taken for the capacitor to begin discharging is much shorter than the turn-off time of the SCR. Thus, the voltage across the output capacitor starts decreasing relatively fast, thereby pushing the voltage across the SCR above the holding voltage within the turn-off time of the device. This is summarized in (9).

$$RC_{out} < t_{OFF} \tag{9}$$

Based on the 30 μs turn-off time of the SCR and a load resistance of 47 kΩ, the minimum output capacitance needed is about 0.6 nF, which is in good agreement with the experimental value of above 1 nF required for pulsing. Leveraging the reverse current analysis previously discussed, the short discharge time of the smaller-sized C_{OUT} suggests that the reverse current from C_{OUT} may not only be insufficient to remove the free carriers in the device, and return the $n_1 - p_2$ junction to its reverse-biased state, but also lacking in the time available for the process to be reversed. This explains why the SCR could only be switched on but not turned off for small values of the output capacitor.

C. EFFECT OF RESISTANCE ON PULSING

The effect of the load resistance on the pulse generating capability of the circuit was also examined by varying the resistor values from 800 Ω to 50 kΩ, with C_{OUT} maintained constant at 100 nF. The transient measurements of voltage across the SCR, V_T, and current through it, I_{SCR}, for the set of resistor values used are summarized in Figure 26 and Figure 27, respectively.

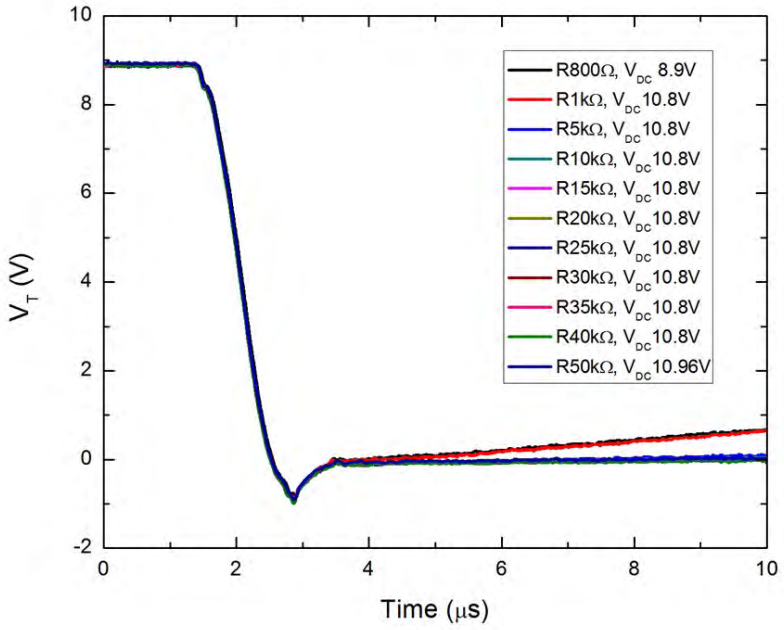

Figure 26. Measured V_T during the switching of SCR for a set of values of R, C_{OUT} maintained at 100 nF.

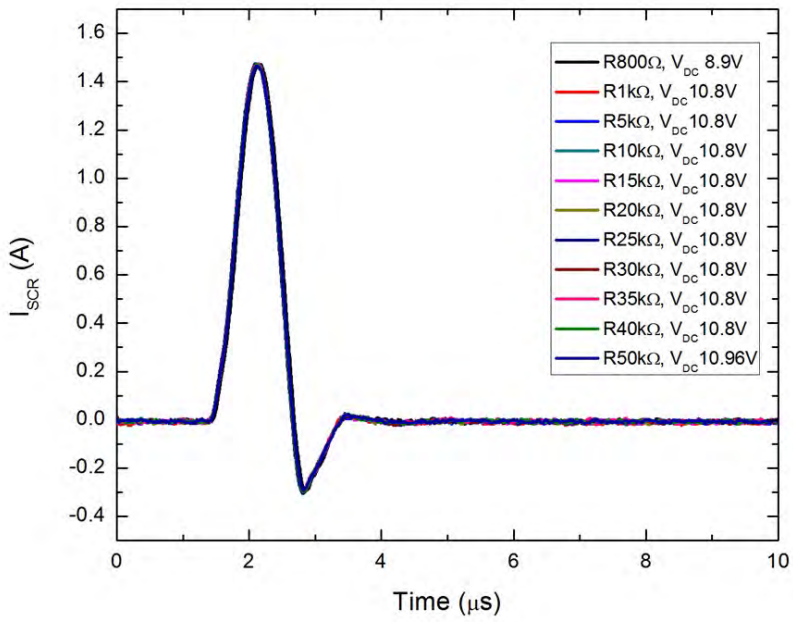

Figure 27. Variation of I_{SCR} with R, C_{OUT} .maintained at 100nF.

It can be seen in Figure 27 that changing the resistor values had no impact on I_{SCR}. This is to be expected since C_{OUT}, which is responsible for the transient current through the SCR when the device switches to its "on" state, is fixed in this case. The effect of varying the load resistance is apparent only when the SCR is reverting to its "off" state, as seen in Figure 26, where the rate of increase of V_T increases with decreasing R. This lends further credence to the previous discussion which indicated that the ability of the device to switch off should satisfy $RC_{out} > t_{OFF}$. Thus, a smaller load resistor requires a larger output capacitor to sustain pulsing and this agrees well with the measured range of C_{OUT} for which pulsing occurred when different load resistors were used (see Figure 28). Specifically, pulsing was achieved only for C_{OUT} values between 81 nF and 1024 nF when the 800 Ω load resistor was used. This lower limit of C_{OUT} was significantly higher as compared to a 47 kΩ resistor circuit. From (9), using a lower R of 800 Ω means that a larger C_{OUT} is required for $RC_{OUT} > t_{OFF}$ to be satisfied for pulsing to ensue. This ensures that the time required by the SCR to revert to its "off" state is not restricted by the discharge time of C_{OUT}. In addition, the upper limit of the output

capacitance required to sustain pulsing is not affected by the value of the load resistor used since it only depends on the on-resistance of SCR.

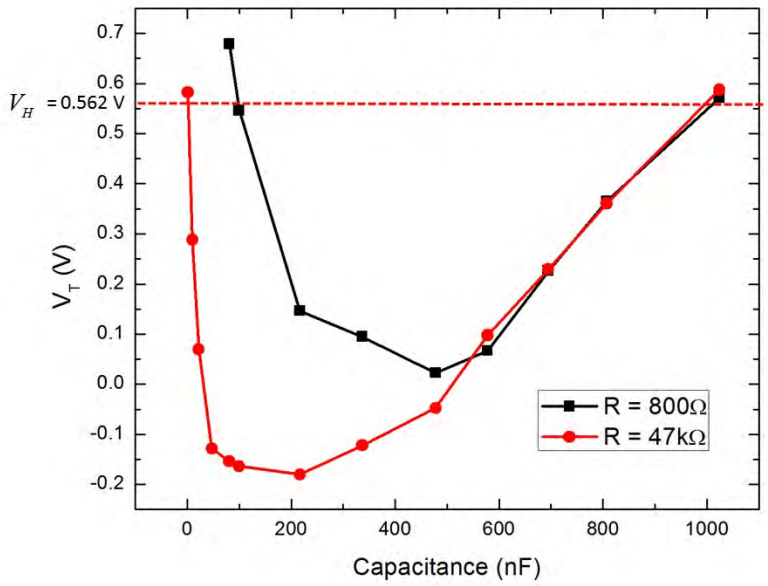

Figure 28. Comparison of variation of V_T with C_{OUT}, just after SCR is switched on, and when different load resistors are used. For pulsing to be sustained, the upper limit of output capacitors is not dependent on the value of the load resistor.

To note, pulsing was achieved for resistor values as low as 800 Ω although these values do not satisfy the static load-line criteria set forth previously and as illustrated in Figure 29. This is because the static load-line analysis previously described was applicable for a circuit with only a resistive load. With the *RC* load in our case, the current generated during the switching primarily passes through the output capacitor due to its low impedance and at fast switching speeds. When pulsing occurs, the dynamics of the circuit become more convoluted, and (1) should be modified to account for the impedance of C_{OUT} as given in (10). However, analyzing the dynamic circuit equation to explain this phenomenon is complex since the angular frequency, ω, is not a constant.

$$V_{DC} = V_T + I_R\left(R + \frac{1}{j\omega C_{OUT}}\right) \tag{10}$$

Figure 29 shows a set of load lines with varying load resistances. It can be seen that only $R = 50\ \text{k}\Omega$ has a single unstable operating point that lies between I_S and I_H of the SCR's I-V characteristics. This instability would enable the SCR to be triggered between its "on" and "off" states, as previously explained. On the other hand, the other resistors each possess two stable operating points on the I-V characteristics: one below I_S and the other above I_H. In theory, no pulsing should occur for these resistors and the SCR should simply switch from its "off" state to its "on" state and remain there. The fact that pulsing occurs can be attributed to the role that the output capacitor, C_{OUT}, plays during the switching process. It can be seen from Figure 26 that switching occurs within about 1 μs, which is close to the SCR's turn-on time of 1 μs. This suggests the possibility that C_{OUT} was able to charge up and establish a negative bias across the SCR before the device could turn on fully and reach its stable operating point above I_H. The negative bias, V_T, then drove a reverse current, I_{SCR}, through the SCR and returned the device to its "off" state, thus allowing pulsation.

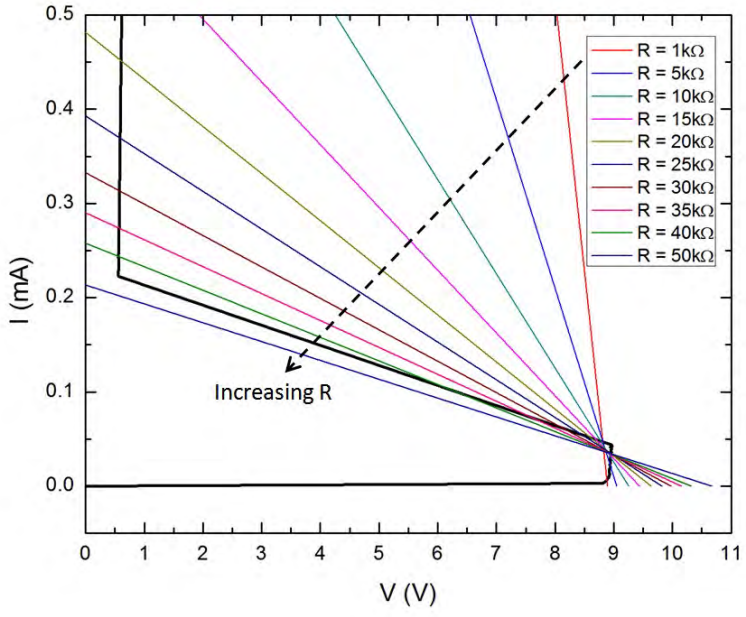

Figure 29. Change in load-line as resistor changes. Pulsing is still achieved for resistor values whose load-lines do not satisfy the static load-line criteria for pulsing.

D. EFFECT OF GATE CURRENT ON PULSING

In order for the circuit to be incorporated into light detection or ionizing radiation detection applications, it is important to understand the effect of triggering the SCR externally for pulse generation. The SCR can be triggered either by sending a current through the gate terminal or by shining light or radiation on the middle p-n junction. For the purposes of this thesis, the provision of a gate current was conveniently achieved by connecting a photodiode to the gate of the SCR in the reverse-biased configuration. DC bias was increased till the onset of pulsing and V_T and I_{SCR} were measured for C_{OUT} = 3 nF and R = 47 kΩ. These were compared against the V_T and I_{SCR} transient responses for an un-gated, DC bias-triggered pulsing of the SCR, as shown in Figure 30 and Figure 31, respectively. The I-V characteristics of the photodiode with and without illumination were also measured using a parameter analyzer and illustrated in Figure 32. A 5 μA photocurrent was generated when the photodiode was illuminated based on the data in Figure 32.

As expected, the injection of a gate current enabled pulsing to be sustained at a lower DC bias. In addition, the gated and un-gated transient I_{SCR} responses were comparable in profile with slight differences in their magnitude. This suggests that the switching mechanism of the SCR is not sensitive to the means by which it is triggered, be it an un-gated, DC bias or via a gate current. The higher I_{SCR} with gated triggering is possibly due to an increase of avalanche generation with additional holes injected into the p_2 layer via the gate terminal.

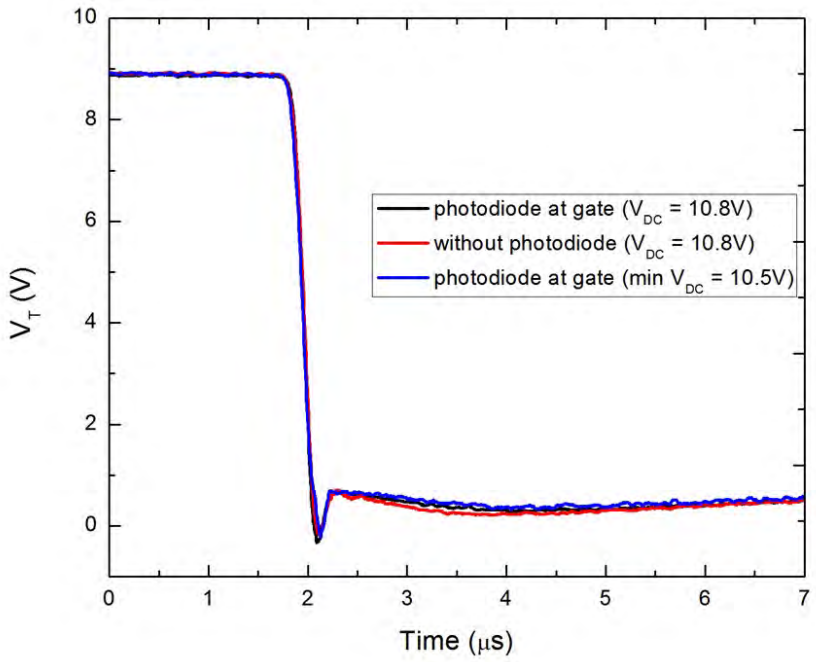

Figure 30. Comparison of V_T transient response for gated (via photodiode) and un-gated pulsing.

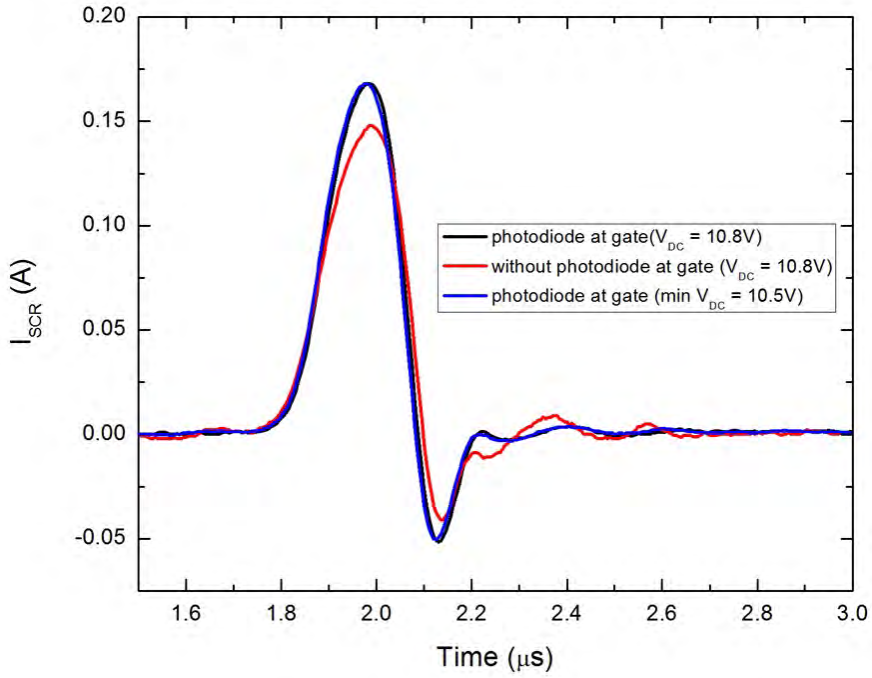

Figure 31. Comparison of I_{SCR} transient response for gated (via photodiode) and un-gated pulsing.

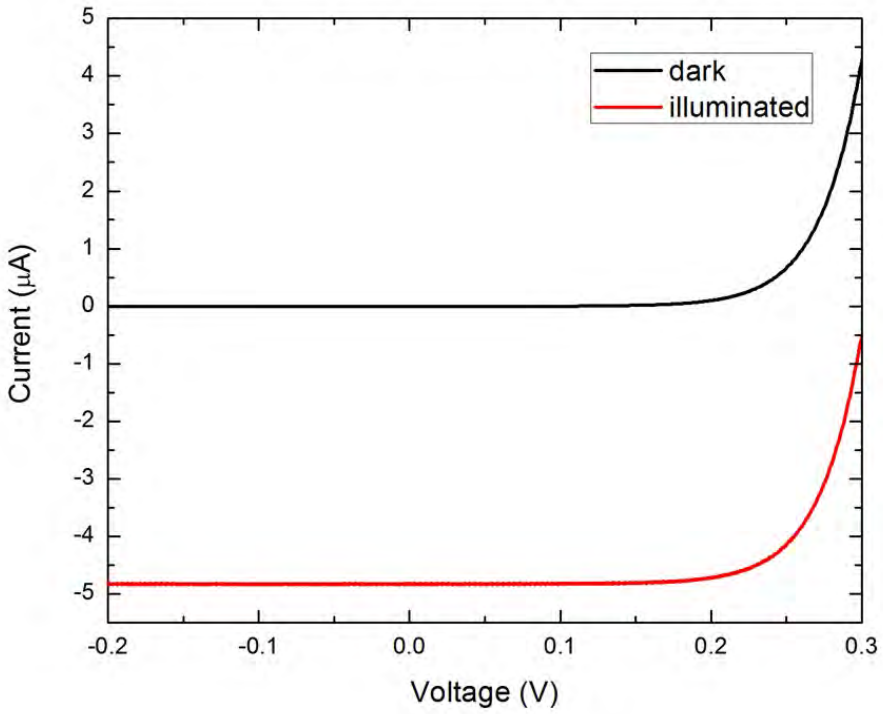

Figure 32. I-V characteristics of photodiode in dark and illuminated conditions; the amount of gate current injected is about 5 μA.

E. DYNAMIC I-V CHARACTERISTICS OF MBS 4993

As previously mentioned, a static load-line analysis of the circuit is not applicable when pulsing occurs with a *RC* load. The I-V characteristic of the SCR during pulsing is needed for describing the dynamics of the circuit. This is done by using the transient data I_{SCR} and V_T for a given C_{OUT}, and plotting I_{SCR} vs V_T as shown in Figure 33.

At a first glance, the dynamic I-V characteristic of the SCR differs significantly from its static I-V profile. Notably, the amplitudes of the currents involved during pulsing (-0.26 A – 2.86 A) are approximately three orders of magnitude larger than in the static case (0 mA – 0.25mA). Secondly, the large differences in the I-V characteristic when C_{OUT} is varied clearly emphasize the significant role C_{OUT} plays in the generation of pulses. Thirdly, the impedance of the device is obviously not a constant as evidenced by the non-linear behavior of V_T with I_{SCR}.

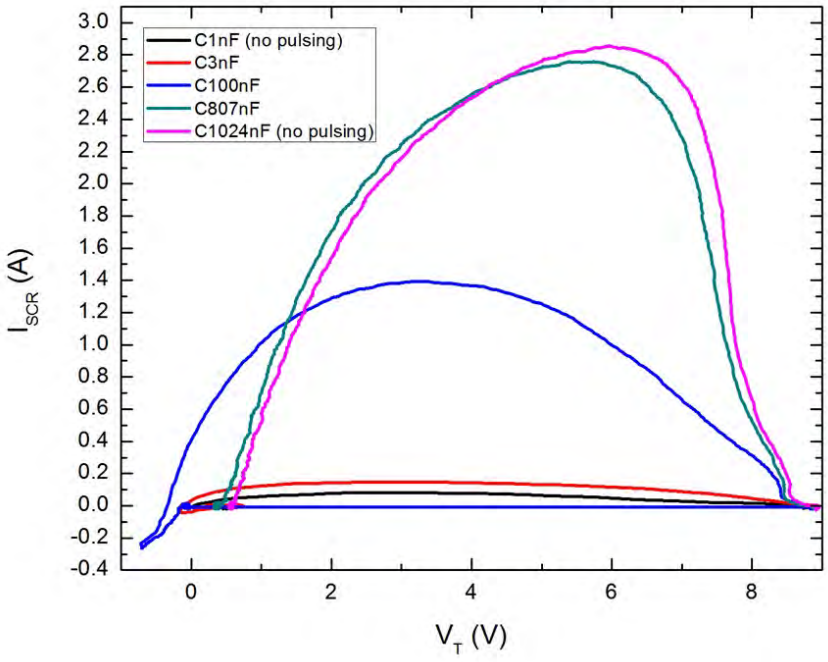

Figure 33. Dynamic I-V characteristic of the MBS 4993 for a set of C_{OUT} with load resistance of 47 kΩ.

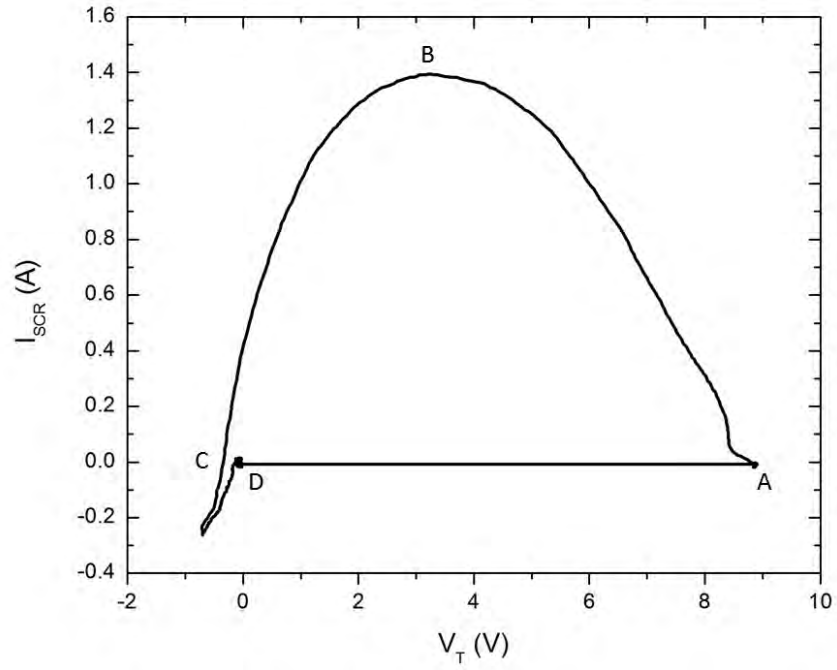

Figure 34. Dynamic I-V characteristic of the MBS 4993 for C_{OUT} = 100 nF and R = 47 kΩ.

The dynamic I-V characteristic of the SCR is examined in closer detail using the data for C_{OUT} = 100 nF (see Figure 34). As the plot is created using the time-dependent response of both V_T with I_{SCR}, the I-V characteristic is intrinsically a function of time as well. When pulsing first occurs at point A, V_T across the SCR drops from V_S as the device switches to its "on" state. The forward-biasing of all of the SCR's three junctions (p_1 - n_1, n_1 - p_2 and p_2 - n_2) due to avalanche multiplication of injected charges from the outer two p-n junctions (p_1 - n_1 and p_2 - n_2) into the middle n_1 - p_2 junction gives rise to a surge in the current through the circuit. The upper branch of the I-V characteristic from point A to point B illustrates this. During this period, C_{OUT} is charged and from point B to point C, V_T decreases with I_{SCR} as the charging of C_{OUT} nears completion. At point C, the charge on C_{OUT} is at its maximum while V_T across the SCR is close to zero. Between points C and D, a reverse current exists to return the SCR to its "off" state. The switching of the SCR to its "off" state is depicted by the lower branch of the I-V characteristic from points D to A. When V_T across the device increases beyond V_S, the switching process is repeated and a new pulse occurs.

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IV. CONCLUSION AND RECOMMENDATIONS

In this thesis, we have shown definitively that the SCR switches from its "on" state to its "off" state via a reverse recovery current (negative I_{SCR}) that is accompanied by a negative voltage drop across the device. This reverse recovery current is needed to remove the free carriers in the drift region and return the central $n_1 - p_2$ junction to its reverse-biased "off" state. In addition, the regenerative process by which charges are avalanched into the circuit when the SCR is turned on appears to be independent of the mode of triggering (i.e. via direct un-gated DC bias or using a current at the gate). However, the magnitude of current generated during the switching depends on the gating mechanism employed.

Significantly, in wanting to improve the sensitivity of the pulse generating circuit for radiation detection, we also established that the extent to which the dead time between the pulses (i.e. the RC_{OUT} time constant of each pulse) can be reduced is in fact constrained by the SCR's intrinsic turn-off time, t_{OFF}. This means that without making modifications to the SCR itself, the minimum dead time achievable for pulsing to be sustained is essentially the turn-off time of the SCR. Reducing R and/or C_{OUT} such that $RC_{OUT} < t_{OFF}$ will not enable pulsing, as previously demonstrated and discussed.

To further increase the sensitivity of the circuit, future work may require modifications to be made to the SCR itself. Typically, the SCR's turn-off time can possibly be lowered by doping the device with minority carrier lifetime killing impurities such as gold. In addition, it was further proposed that confining the doping of the minority carrier lifetime killing impurities to a thin region of the device in a plane perpendicular to the on-state current flow would make for better reduction in turn-off times [16]. Alternatively, the introduction of additional anode gates at the n_1 layer could be explored to reduce t_{OFF} since positive turn-off time improvements of up to 55% could apparently be achieved [17].

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