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# Design and Performance of a 560-Microsecond Ku-Band Binary Fiber-Optic Delay Line

JOSEPH M. SINGLEY

JOHN F. DIEHL

CHRISTOPHER S. McDERMITT

CHRISTOPHER E. SUNDERMAN

VINCENT J. URICK

*Photonics Technology Branch  
Optical Sciences Division*

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# DESIGN AND PERFORMANCE OF A 560-MICROSECOND Ku-BAND BINARY FIBER-OPTIC DELAY LINE

## EXECUTIVE SUMMARY

- Fiber-optic delay line usefulness is described.
- The Bi-FODL architecture is shown and discussed.
- The measured gain of the Bi-FODL is shown over all possible delays.
- The measured noise figure of the Bi-FODL is shown over all possible delays.
- The measured  $P_{1dB}$  is shown for the Bi-FODL.
- The measured SFDR is shown for the Bi-FODL.
- The measured OIP3 is shown for the Bi-FODL.
- The measured phase noise is shown for the Bi-FODL.
- An operating procedure for the Bi-FODL is described.





# DESIGN AND PERFORMANCE OF A 560-MICROSECOND Ku-BAND BINARY FIBER-OPTIC DELAY LINE

## 1 INTRODUCTION

An extremely powerful tool afforded by microwave photonics is a fiber-optic delay line (FODL). The concept of a FODL is simple: light is modulated by an RF waveform(s) and a length of fiber is utilized to store the information. The delay or storage time in the fiber is about  $5 \mu\text{s}/\text{km}$  for typical fiber. The low optical loss in fiber over a very wide bandwidth, typically  $0.2 \text{ dB}/\text{km}$  or  $0.04 \text{ dB}/\mu\text{s}$ , makes a photonic delay line much more feasible than an RF coaxial cable for any appreciable delay length. Electrical power consumption and instantaneous bandwidth are also metrics in favor of an analog FODL as opposed to digital RF memory (DRFM) when the bandwidth is greater than 1 GHz or so. One downside of an analog FODL as compared to a DRFM is that the former does not provide a continuously-accessible memory module. However, there are a number of applications where this is not a concern.

As opposed to a point-to-point link, a FODL serves as a “black box” that delays an RF signal in time. The physical size of a FODL is driven largely by the amount of fiber employed but there are numerous applications where rack-mount units are feasible. Shown in Figures 1 and 2 are two applications of a FODL in electromagnetic warfare (EW) scenarios. A FODL is used as a buffer for a cued receiver in the architecture in Figure 1. In this type of system, an incoming RF spectrum is channelized into some number of channels for coarse, high-speed signal detection. The output of the channelizer cues a high-performance analog-to-digital converter (ADC) that is tuned to the frequency of interest. The cueing process can take a considerable amount of time, thus the utility of the FODL is to preserve a time-delayed copy of the received spectrum. The requirements on the FODL in this implementation can be quite stringent, driven by the sensitivity and dynamic range of the ADC as well as the time needed for the cueing process. A FODL can also be utilized to emulate range in radar testing such as depicted in Figure 2. In this scenario, a transmitted radar signal impinges on a target at a fixed range and the returned signal is passed through a FODL before processing. A fixed-length FODL can allow for testing situations beyond what is feasible in a chamber or limited test range. A more-versatile option is to employ a FODL with variable delay and amplitude to provide a multitude of range scenarios.

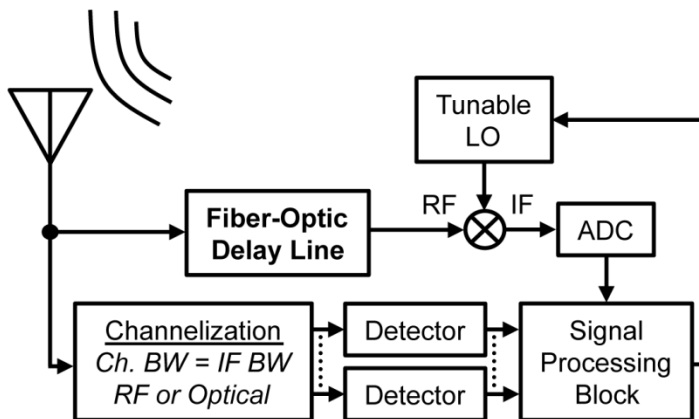


Figure 1: Block diagram of a FODL used as a buffer for a cued receiver.



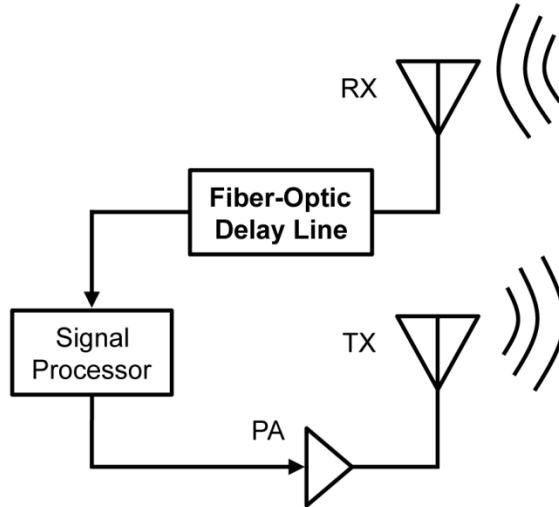


Figure 2: Block diagram of a FODL used to emulate range in a range testing application.

As compared to a fixed-length FODL, units with adjustable delay offer more versatility with the tradeoffs of added complexity and cost. A series of delays and switches in a binary arrangement provides a large number of possible paths in a hardware-efficient manner. The focus of this report is the design and performance of such a binary fiber-optic delay line (BiFODL) as shown in Figure 3. The BiFODL depicted there consists of nine delays, each twice the preceding delay. Fiber-optic switches are employed to insert or remove each delay. As a result, there are 512 possible paths through the BiFODL ranging between  $1.1 \mu\text{s}$  and  $560 \mu\text{s}$  in  $1.1 \mu\text{s}$  steps. In general, a BiFODL architecture with a base delay of  $x$  and  $N$  total delay lines will result in  $2^N$  possible paths ranging from  $x$  to  $x \cdot 2^N$  in steps of  $x$ . The EDFAs in the BiFODL shown in Figure 3 were specially designed to equalize, as much as practical, the RF performance for each delay setting. That is, the EDFAs were arranged to be in saturation for all configurations with nominally the same optical gain and output noise power. Further discussion of the BiFODL design is provided in Section 2. The measured RF performance of the unit is then documented in Section 3. The report concludes with a short summary on the operation of the BiFODL rack mount unit.

## 2 ARCHITECTURE

A schematic of the BiFODL is shown below. The unit is comprised of nine separate fiber delays that can be inserted in various combinations by way of “add/drop” optical switches. This optical configuration allows for 512 possible delays with a “static” minimum delay of 332 ns if all of the optical switches are set to their bypass state. Eight EDFAs are strategically located throughout the delay paths to provide optical gain which offsets the loss experienced from light travelling through the long lengths of fiber. The individual fiber lengths and types were designed specifically to combat chromatic dispersion so that the net dispersive effect is close to zero.

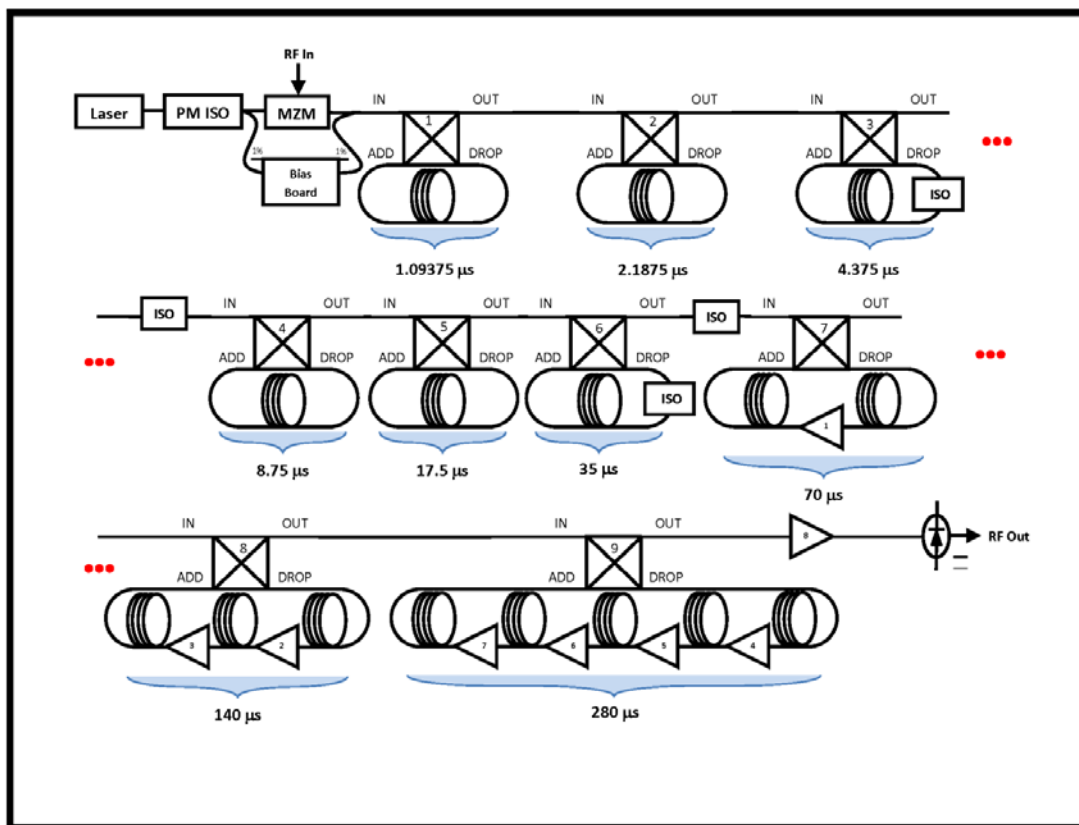


Figure 3: The experimental setup used to measure the RIN of each laser [7]. The (VOA) is used to reduce the laser’s output to a level that produces 10 mA of photocurrent ( $I_{dc}$ ) at the photodiode. The signal from the photodiode is then amplified and displayed on the ESA. The gain ( $G_{amp}$ ) and noise figure ( $NF_{amp}$ ) of the amplifier must be measured independently of the laser’s RIN and manually subtracted later in order to realize the true laser intensity noise spectrum.

### 3 PERFORMANCE

An S21 measurement was performed for all 512 possible delays. Below is a plot that shows the RF gain of the system from 500 MHz to 18 GHz. The red line indicates the average gain of all possible delays while the lighter red area shows the total excursion of the gain over all possible delays.

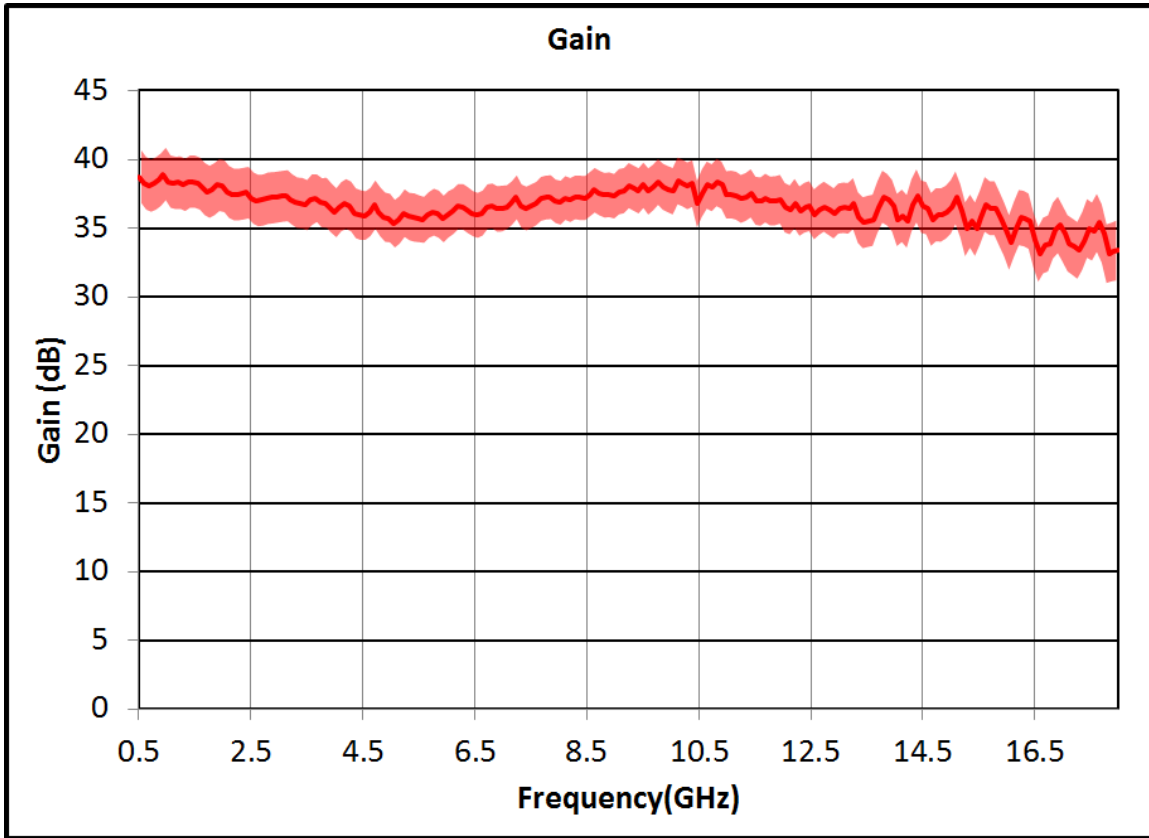


Figure 4: Bi-FODL gain data from 500 MHz – 18 GHz. The dark red curve is the average gain of all 512 possible delays while the shaded light red area shows the spread of the gain data over all possible delays.

A Noise Figure measurement was performed for all 512 possible delays. Below is a plot that shows the Noise Figure of the system from 500 MHz to 18 GHz. The red line indicates the average Noise Figure of all possible delays while the lighter red area shows the total excursion of the Noise Figure over all possible delays.

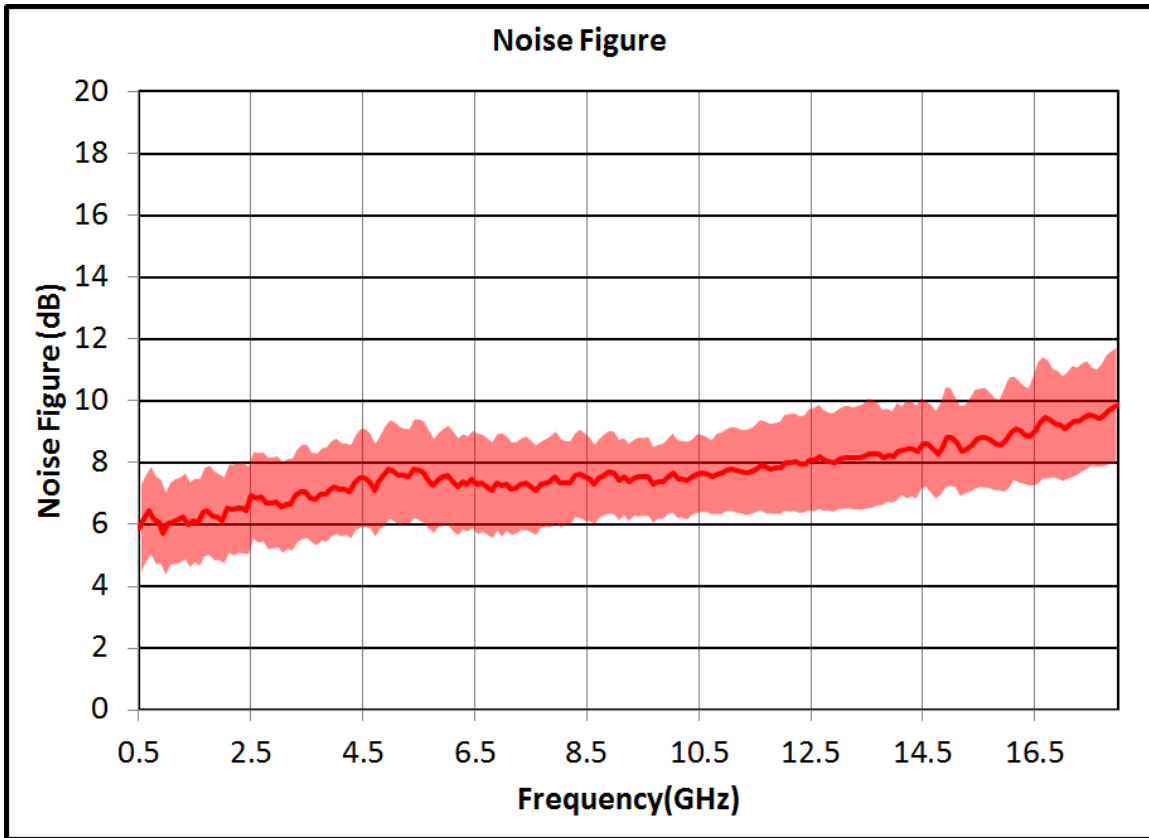


Figure 5: Bi-FODL noise figure data from 500 MHz – 18 GHz. The dark red curve is the average noise figure of all 512 possible delays while the shaded light red area shows the spread of the noise figure data over all possible delays.

The 1 dB compression point was measured using a single tone with a frequency of 10.24 GHz. It was determined that 1dB of compression in the gain is experienced with an input power level of -49.8 dBm as can be seen in the plot below.

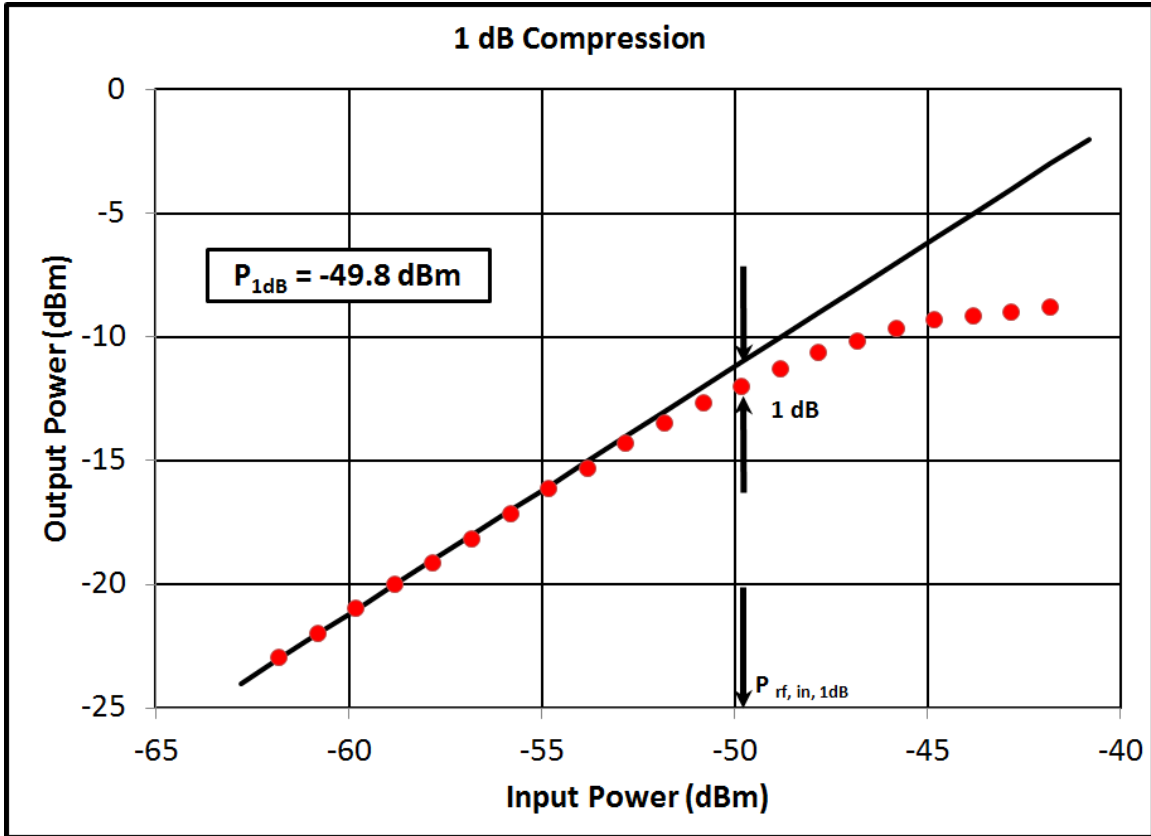


Figure 6: Chart displaying the 1 dB compression point of the Bi-FODL at 10.24 GHz.

The spur-free dynamic range (SFDR) was determined using a two-tone test with frequencies of 10.235 GHz and 10.245 GHz. The measurement noise floor was approximately -128 dBm in a 1 Hz bandwidth. This results in an OIP3 of -1.7 dBm and a SFDR of -88 dB in a 1 Hz bandwidth.

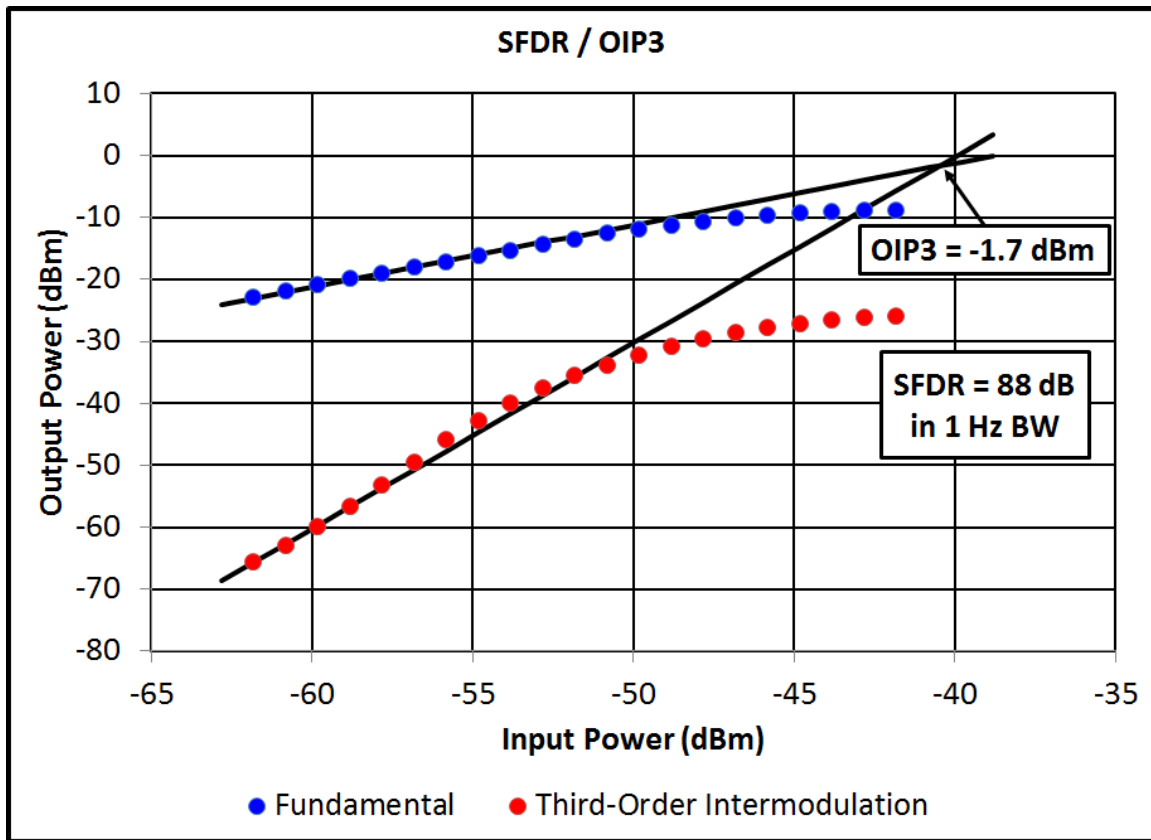


Figure 7: Chart displaying the SFDR and OIP3 of the Bi-FODL at 10.24 GHz. The plot shows the output power of the fundamental (blue dots) as well as the odd-order distortion (red dots).

The phase noise of the system was measured for both the minimum and maximum possible delay over an offset frequency range of 10 Hz to 10 MHz. The plot below also displays the phase noise of the reference oscillator in addition to the phase noise of the low phase noise amplifier used in the measurement setup.

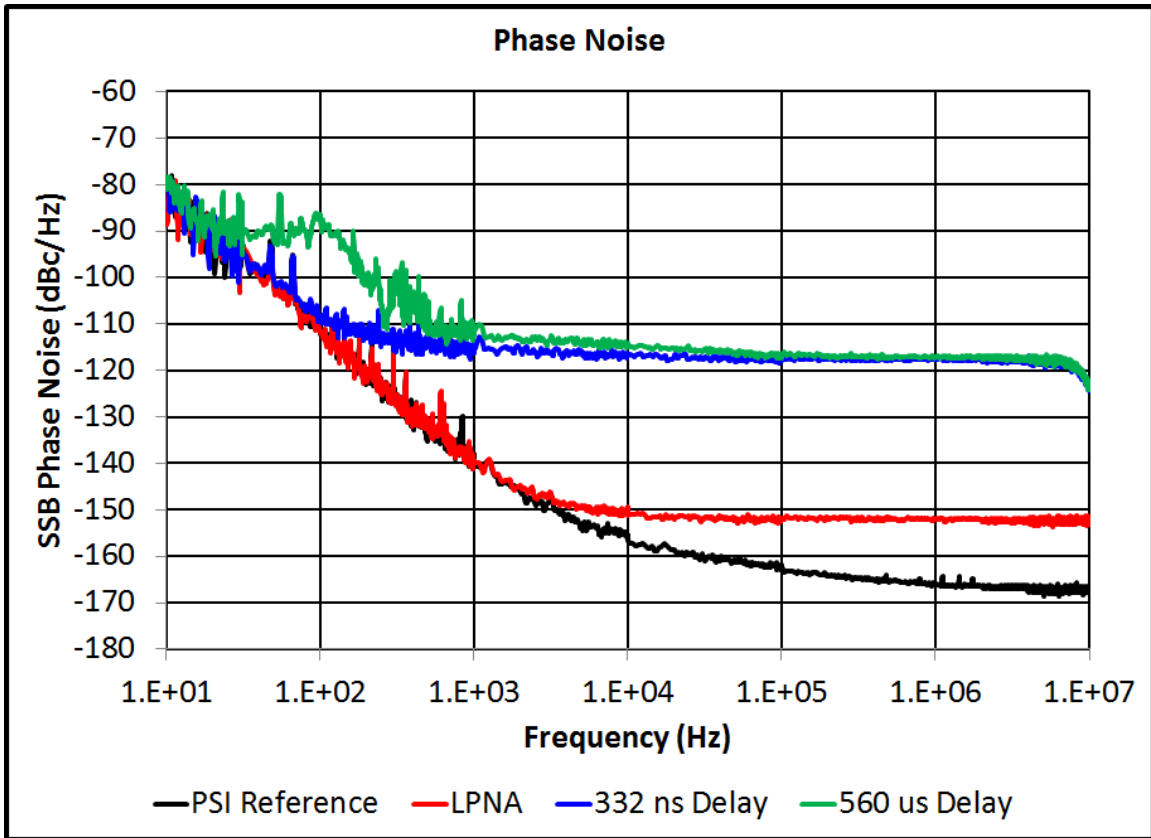


Figure 8: Plot showing the phase noise of the Bi-FODL from 10 Hz – 10 MHz. The blue curve displays the phase noise of the Bi-FODL through the shortest possible delay path. The green curve displays the phase noise of the Bi-FODL through the longest possible delay path. The red curve represents the phase noise added to the measurement system by the low phase noise RF amplifier required to measure the phase noise of the Bi-FODL. The black curve shows the phase noise of the reference oscillator which represents the noise floor of the measurement apparatus.

The table below was created to compare the desired performance level that was requested by section 5726 with the measured data collected by section 5651 at the completion of the system build. All desired metrics were met with the exception of RF noise figure due to the addition of an RF attenuator at the request of section 5726. The noise figure can be improved approximately 4-5 dB by removing the RF attenuator which is located right before the low noise RF amplifier.

Specification	Symbol	Desired Value	Measured Value
Operational Bandwidth	BW	0.5 – 18 GHz	0.5 – 18 GHz
RF Noise Figure	NF	≤ 3 dB	≤ 10 dB *
Input 1dB Compression Point	P <sub>1dB</sub>	≥ -50 dBm	-49.8 dBm
Spur Free Dynamic Range	SFDR	≥ 50 dB	88 dB
Dimensions	LxWxH	25.5 x 17 x 8.75 inches	

\*The NF can be improved ~4 - 5 dB by removing the RF attenuator located before the LNA.

Table 1: A comparison of the desired system performance versus the actual measured results.



## APPENDIX (OPERATING PROCEDURE)

1. Check to see that there is a fuse (250V, 3A) inserted into the fuse tray on the AC power entry module.
2. After checking that the switch is in the open position, as indicated by the “O” symbol on the rocker, connect the 120 AC power cord from a wall plug to the FODL unit.
3. Connect the RF input and output cables to the front panel, without any power on the RF input. **\*Please note that the maximum input power is -50 dBm.**
4. Close the switch and the AC power indicator light will come on. At this point the AC line is powering the internal power supply which in turn powers the modulator bias control board, laser, low-noise RF amplifier, RF attenuator, and applies a bias voltage to the photodiode.
5. Press the laser power button on the front panel. The ring illuminator on the button will light. This button activates the current drivers for all eight EDFAs.
6. Wait 5 minutes. During this time the laser and modulator will warm up and the modulator bias control board will lock the modulator at the appropriate bias point (quadrature).
7. Turn on the RF input power.
8. Currently, the delay time and RF attenuation are set using the Ethernet port on the back of the unit. The software that allows for communication to take place resides on a laptop computer that is in Tracy Hill’s possession (Code 8143). Please see Tracy for a tutorial of that software. Future plans may include controlling the FODL through the touchscreen on the front panel.