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This projec	t developed m	,	•	and d	evice desig	gns	for radio enabled electronics that are		
capable of complete dissolution in water.									
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Report Title

Final Report for Program on Resorbable Radio Devices

ABSTRACT

This project developed materials, manufacturing schemes and device designs for radio enabled electronics that are capable of complete dissolution in water.

Enter List of papers submitted or published that acknowledge ARO support from the start of the project to the date of this printing. List the papers, including journal references, in the following categories:

(a) Papers published in peer-reviewed journals (N/A for none)

Received	Paper
05/05/2014	2.00 Suk-Won Hwang, Xian Huang, Jung-Hun Seo, Jun-Kyul Song, Stanley Kim, Sami Hage-Ali, Hyun-Joong Chung, Hu Tao, Fiorenzo G. Omenetto, Zhenqiang Ma, John A. Rogers. Materials for Bioresorbable Radio Frequency Electronics, Advanced Materials, (07 2013): 0. doi: 10.1002/adma.201300920
10/11/2012	1.00 SW. Hwang, H. Tao, DH. Kim, H. Cheng, JK. Song, E. Rill, M. A. Brenckle, B. Panilaitis, S. M. Won, YS. Kim, Y. M. Song, K. J. Yu, A. Ameen, R. Li, Y. Su, M. Yang, D. L. Kaplan, M. R. Zakin, M. J. Slepian, Y. Huang, F. G. Omenetto, J. A. Rogers. A Physically Transient Form of Silicon Electronics, Science, (09 2012): 0. doi: 10.1126/science.1226325
TOTAL:	2

Number of Papers published in peer-reviewed journals:

(b) Papers published in non-peer-reviewed journals (N/A for none)

Received Paper

TOTAL:

Number of Papers published in non peer-reviewed journals:

(c) Presentations

"Stretchy Electronics That Can Dissolve in Your Body," presented as a Keynote talk at the Annual Qualcomm Technology Meeting, in San Diego, CA on June 7, 2013.

"Stretchy Electronics and Can Dissolve in Your Body," Distinguished Seminar, Department of Electrical Engineering at Stanford University, in Palo Alto, CA on April 23, 2013.

	Non Peer-Reviewed Conference Proceeding publications (other than abstracts):
Received	Paper
TOTAL:	
Number of Nor	n Peer-Reviewed Conference Proceeding publications (other than abstracts):
	Peer-Reviewed Conference Proceeding publications (other than abstracts):
Received	Paper
TOTAL:	
Number of Pee	er-Reviewed Conference Proceeding publications (other than abstracts):
	(d) Manuscripts
Received	Paper
TOTAL:	
Number of Ma	nuscripts:
	Books
Received	Paper

TOTAL:

Patents Awarded

Awards

Smithsonian Ingenuity Award for Physical Science, Smithsonian Institution Robert Henry Thurston Award, American Society of Mechanical Engineers

Graduate Students					
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Student Metrics This section only applies to graduating undergraduates supported by this agreement in this reporting period
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The number of undergraduates funded by your agreement who graduated during this period and will continue to pursue a graduate or Ph.D. degree in science, mathematics, engineering, or technology fields: 0.00
Number of graduating undergraduates who achieved a 3.5 GPA to 4.0 (4.0 max scale): 0.00 Number of graduating undergraduates funded by a DoD funded Center of Excellence grant for Education, Research and Engineering: 0.00
The number of undergraduates funded by your agreement who graduated during this period and intend to work for the Department of Defense 0.00
The number of undergraduates funded by your agreement who graduated during this period and will receive scholarships or fellowships for further studies in science, mathematics, engineering or technology fields: 0.00

Names of Personnel receiving masters degrees

<u>NAME</u>

Total Number:

Names of personnel receiving PHDs

<u>NAME</u> Sukwon Hwang **Total Number:**

1

Names of other research staff

NAME

PERCENT_SUPPORTED

FTE Equivalent: Total Number:

Sub Contractors (DD882)

Inventions (DD882)

Scientific Progress

See attachment.

Technology Transfer

Transient Electronics Resorbable Radios and RF Energy Scavenging Systems

Grant Number: Army W911NF-11-1-0254; A1074/486349

Principal Investigator : John A. Rogers (UIUC)

Team members: Seung-Kyun Kang (UIUC), Suk-Won Hwang (UIUC)

Summary of Effort: Demonstrate radio frequency devices, schemes for triggered transience and power systems

Research Goals: Outlined in the first page of the attached slide set.

Challenges: 1) Identifying suitable materials and device designs, and 2) establishing processing techniques for integrated systems.

Technical Approach and Progress

1) Transfer print fully formed silicon devices and RF components to build radios and scavengers.

2) Exploit new concepts in triggered transience, mechanical energy harvesting and others.

Key Technical Results

The technical results are summarized, with all associated details, in the attached slide set and the published papers.



Summary

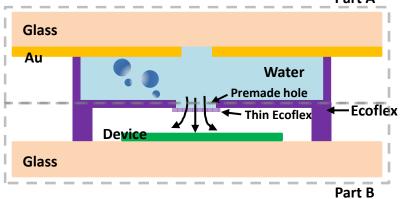
Illinois Deliverables	Status	
Fabricate transient transistors and mechanical energy harvesters based on ZnO, and compare behaviors to theoretical models	Done	Fully completed
Demonstrate electrically triggered transience, with examples at the device and system levels	Done	RF scheme demonstrated; advanced implementations underway
Demonstrate CMOS microdie, with transfer printing	Done	CMOS microdie printed and interconnected with Mg
Develop Si CMOS foundry routes to transient devices	Done	Collaborate with LL
Develop schemes for mechanically triggered transience	Done	Demonstrated disintegration
Demonstrate transient RF beacon devices, with solar power	Done	PCB + a-Si flexible solar panes
Demonstrate non-aqueous transient substrate materials	Done	Demonstrated materials that sublime at room temperature

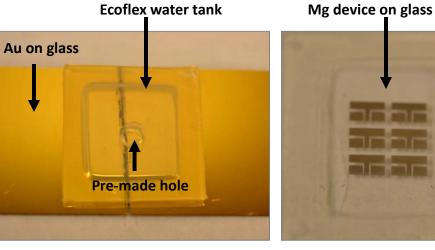


Trigger transience of full circuits

-. Trigger water electrolysis to give out gas

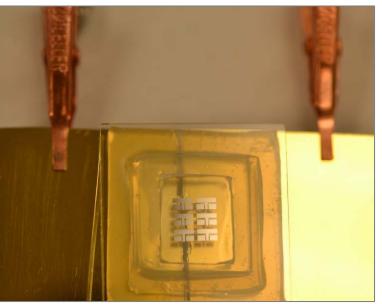
-. Gas pushes water out of the weak point of the water tank, e.g., a pre-made hole with/without covering with a thin Ecoflex layer Part A



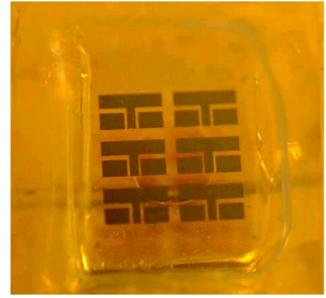




Part B



Stacking of part A & B

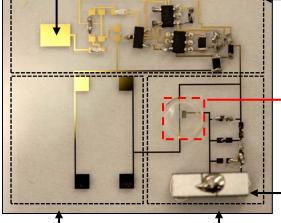




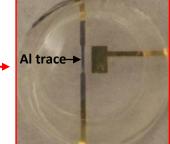


Beacon trigger transience

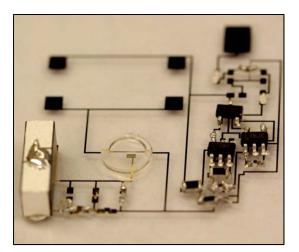
Transmitting antenna



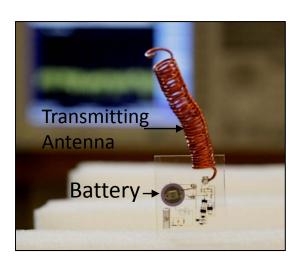
Beacon circuit Ecoflex[®] encapsulating electrolyte

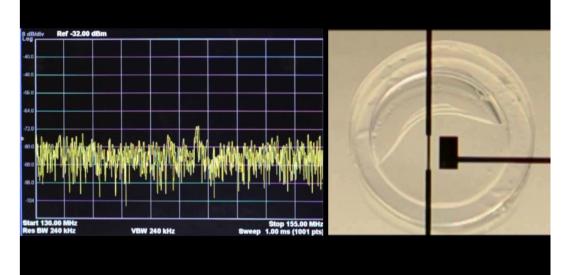


Receiving antenna



Power supply Trigger circuit

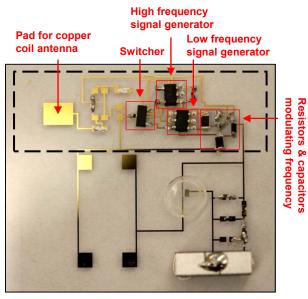


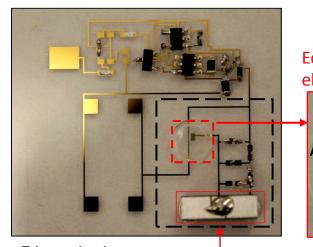




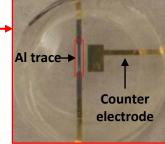
Beacon trigger transience

- Beacon circuit
 - Powered by a 3V lithium battery
 - Containing copper coil antenna for signal transmitting
 - Generating high frequency signal (~145 MHz) which is modulated by low frequency signal (1 Hz)
 - Beacon signal is received by a signal analyzer with high gain antenna
- Trigger circuit
 - A small segment of the beacon power supply line is made of Al trace
 - Small amount of PBS electrolyte is encapsulated by a thin layer of Ecoflex[®]
 - A ceramic antenna is used to receive the RF signal at 915 MHz
 - Upon RF signal, a voltage ~4V is sensed between the AI trace and the counter electrode triggering the electrochemical dissolution of AI, as a result ceasing the beacon transmitter





Ecoflex[®] encapsulating electrolyte



Beacon circuit

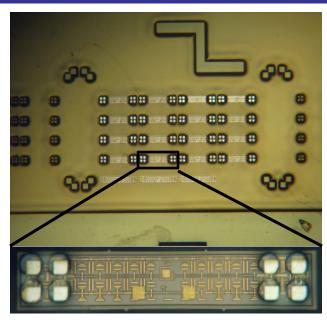
Trigger circuit

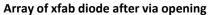
Ceramic antenna

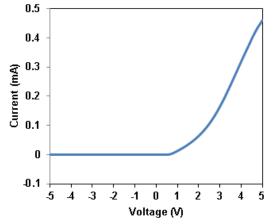
Transient Al trace



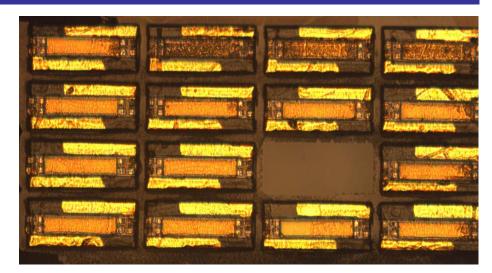
Modularization of Xfab Devices



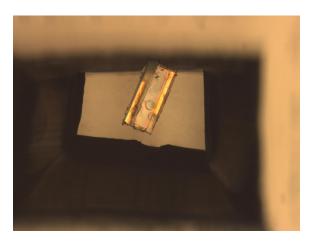




I/V characteristic of a modularized xfab diode



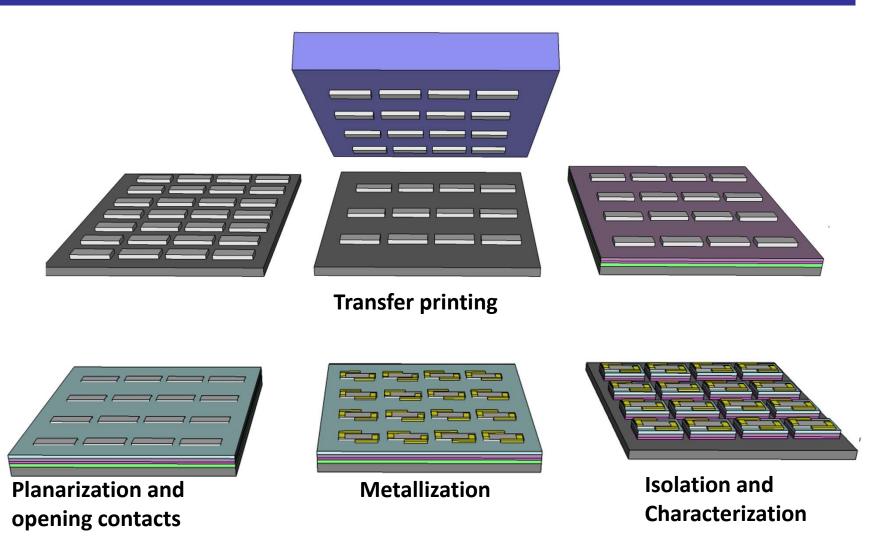
Xfab device matrix after isolation and characterization



Single xfab device picked up on PDMS stamp



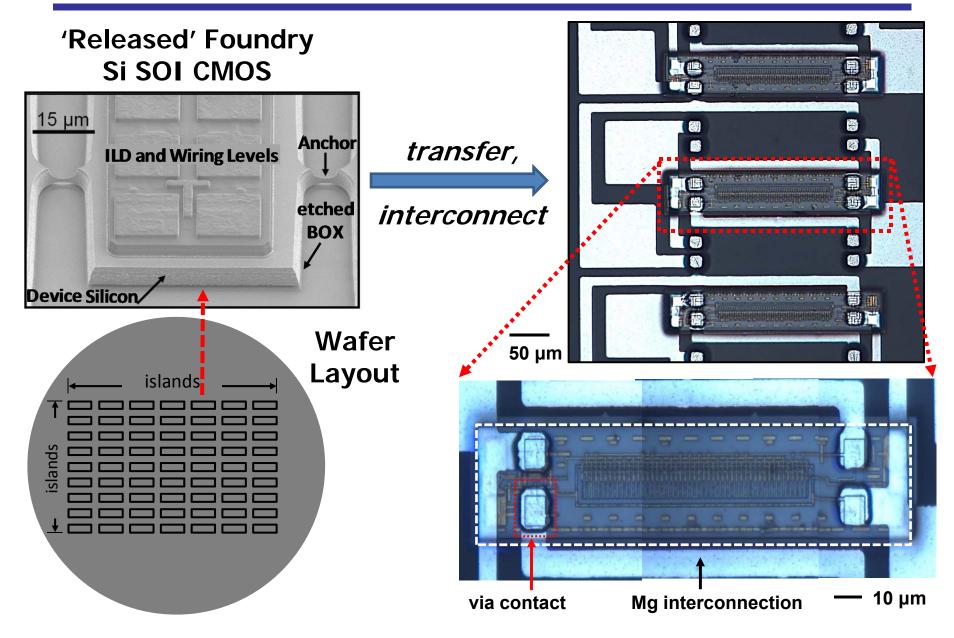
Modularization of Xfab Devices



Modularization process of xfab device involve transfer printing, planarization, vias opening, metallization, isolation, and characterization.

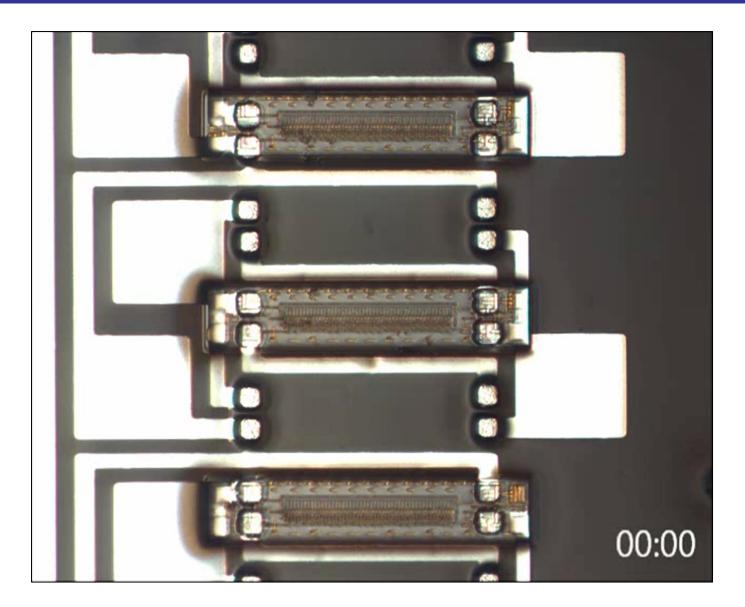


Transient Interconnects for Si Micro-Die





Transient Interconnects for Si Micro-Die



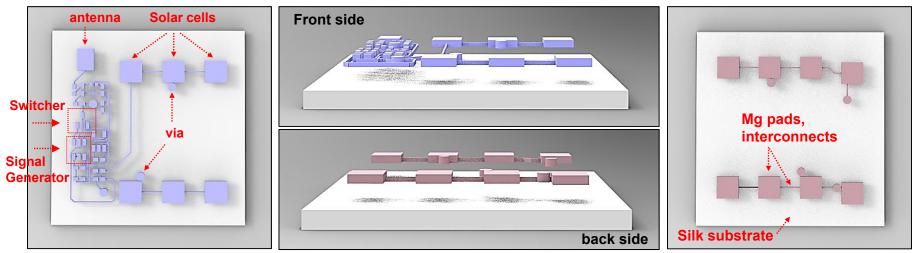


Transient Dual-Sided PCB – Design & Fabrication

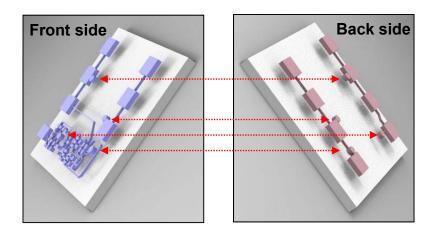
1. Mg deposition through shadow mask on silk substrate

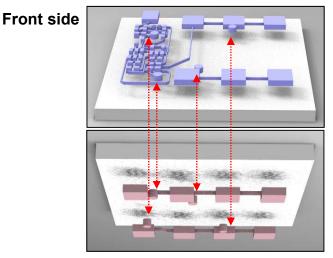
Front side

back side



2. Punch holes through via pads, and Connect both front and back with silver paste





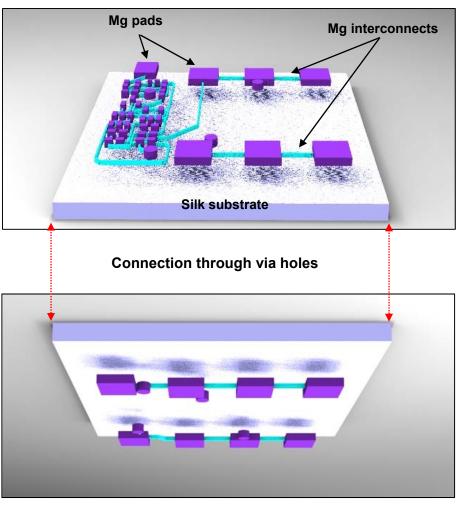
Back side

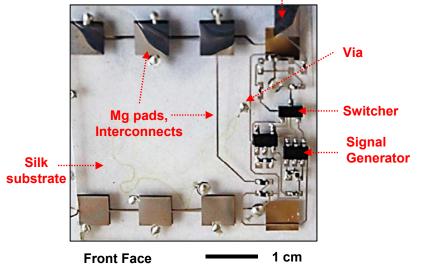


Solar Powered RF Beacon

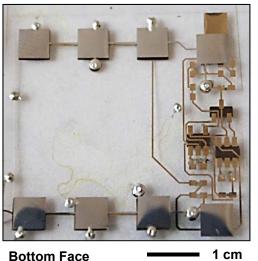
Front

Back





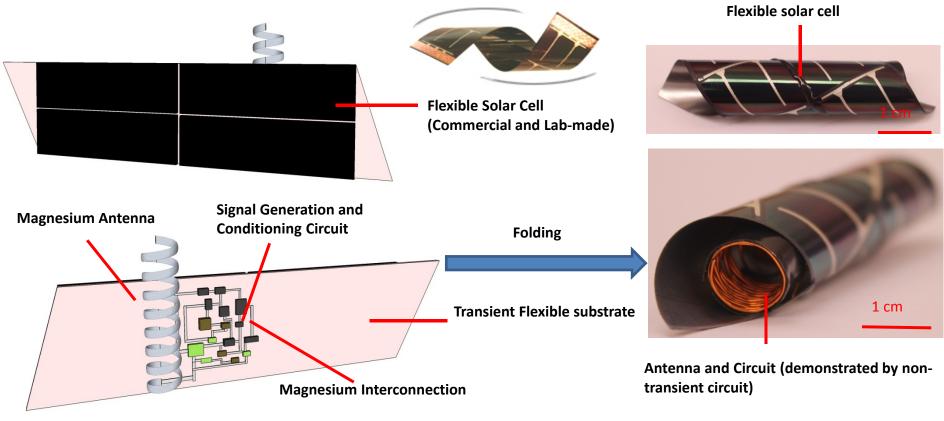
Antenna.



Bottom Face



Transient RF Beacon (3D arbitrary shape)

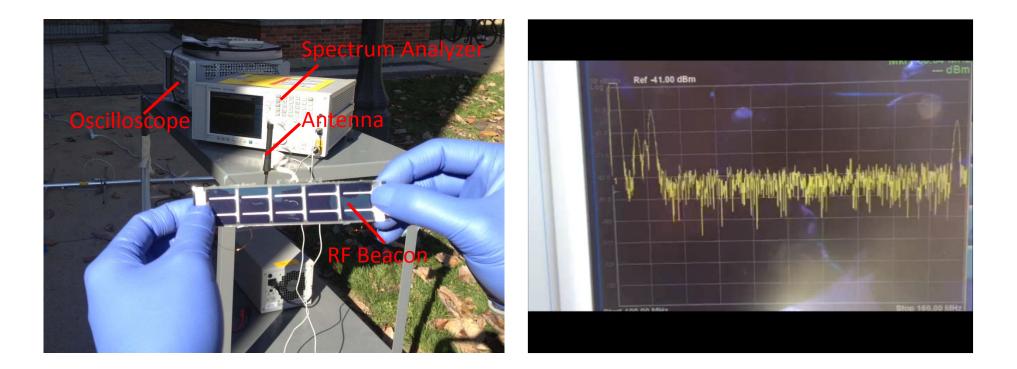


Flexible circuit sheet

- Major circuit components: High and low frequency signal generators, flexible solar cell, magnesium antenna and interconnections, super capacitor (provides extra power to the circuit).
- Circuit is on flexible sheet and can be folded into arbitrary shape to maximize the exposure of sun light (cylinder, cube and pyramid as demonstration).
- Transient circuit is under fabrication.



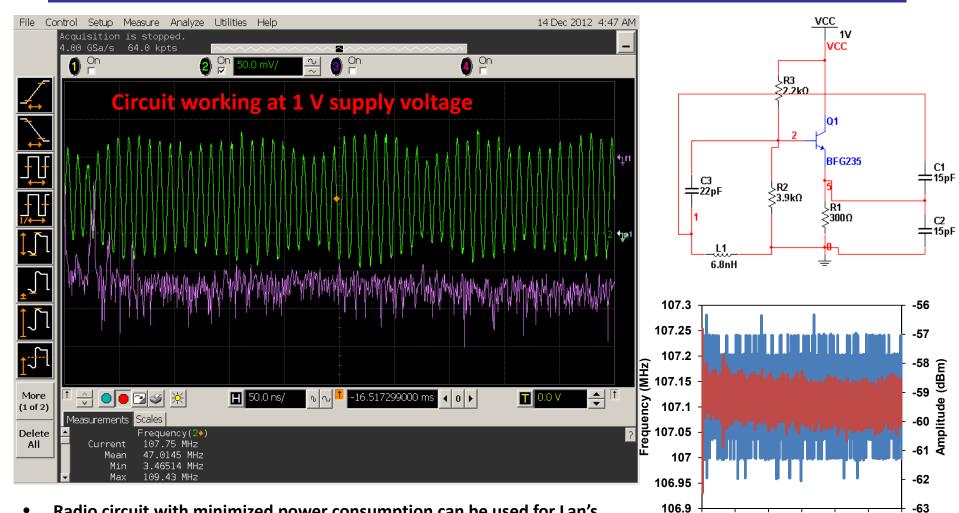
Transient RF Beacon-Outdoor Experiment



- Experiment was done in the morning in fall, when the sun light intensity is not very strong.
- The beacon was powered purely by a flexible solar cell.
- A minimized 160 MHz antenna was able to received a signal from the RF beacon 1 meter away.
- Spectrum analyzer and oscilloscope were used to analyse the signal generated by the beacon.



Radio Circuit with Minimized Power Consumption



- Radio circuit with minimized power consumption can be used for Lan's ٠ battery and kijun solar cell.
- This circuit are using in epidermal active hydration sensor. Will be used in ٠ transient PCB project with kijun's solar cell.



0.6

Time (h)

0.8

0.4

0

0.2

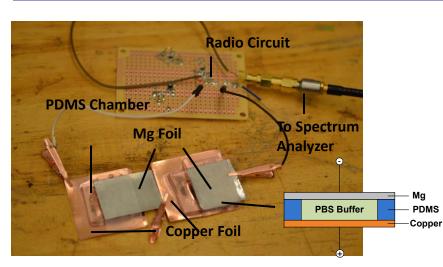
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1.2

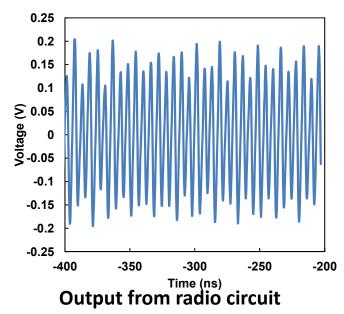
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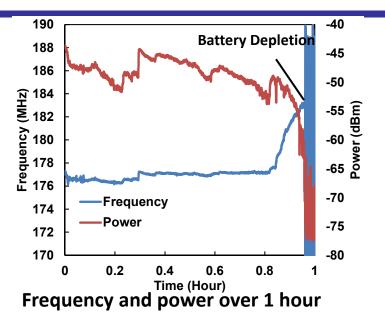


Radio Circuit Powered by Mg Cells



Radio Circuit powered by Mg cells







Transient, Biocompatible Electronics and Energy Harvesters Based on ZnO

Canan Dagdeviren, Suk-Won Hwang, Yewang Su, Stanley Kim, Huanyu Cheng, Onur Gur, Ryan Haney, Fiorenzo G. Omenetto, Yonggang Huang, and John A. Rogers*

Semiconducting oxides are of growing interest as replacements for silicon in thin film transistors for active matrix display backplanes; they are also of potential use in transparent, flexible electronics and energy harvesters. Zinc oxide (ZnO), in particular, has a favorable combination properties. including excellent transparency in the visible wavelength range,^[1] high electron mobility,^[2] and strong piezoelectric response.^[3] As a result, ZnO, in forms ranging from films to wires and rods, has been explored in sensing,^[4–6] catalysis,^[7,8] optical emission,^[9,10] piezoelectric transduction,^[11] and actuation.^[12] Previous work also suggests that ZnO is biocompatible,^[13–15] and therefore suitable for devices that integrate on or in the human body. Here we introduce classes of ZnO based electronic devices that have, as their key attribute, the ability to dissolve completely in water or biofluids. In this way, ZnO provides an alternative to silicon^[16] or organic semiconductors^[17–20] for physically transient forms of electronics

and sensors, with expanded capabilities in energy harvesting,
light emission and others. The other constituent materials
of the devices presented here include magnesium (Mg) for
electrodes and interconnects, magnesium oxide (MgO) for
the dielectrics, and films of silk fibroin for the substrate and
package. Each material used here is also biocompatible, as
discussed in previous reports. ^[21,22,23-26] We present specific
designs and fabrication schemes for ZnO thin film transis-
tors and mechanical energy harvesters (also for use as strain
gauges). Detailed studies reveal the kinetics of dissolution
and the ability to use materials and design choices to control
this kinetics. Combined experimental/theoretical work illus-
trates the key operational features of the devices.

Figure 1a and b provide a schematic diagram and an image of water-soluble ZnO thin film transistors (TFTs) and mechanical energy harvesters (MEHs)/ strain gauges. Sheets of silk fibroin provide substrates and, in certain cases,

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DOI: 10.1002/smll.201300146

communications

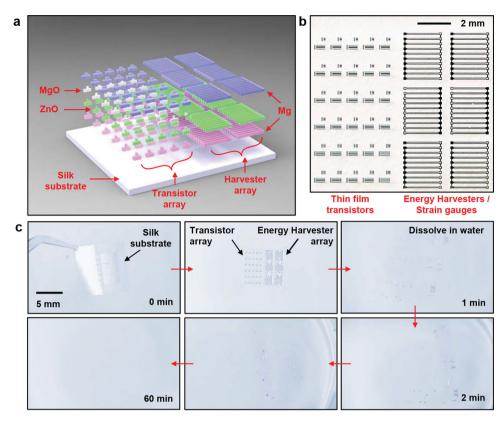


Figure 1. Materials and designs for transient thin film transistors (TFTs) and mechanical energy harvesters (MEHs)/strain gauges based on ZnO, Mg, MgO, and silk. a) Schematic illustration of transient ZnO TFTs and MEHs/strain gauges that consist entirely of water soluble materials: ZnO (semiconductor/piezoelectric), Mg (conductor), MgO (insulator), silk (substrate). b) Photograph of a collection of ZnO TFTs and MEHs on a silk substrate. All electronic materials were deposited through high-resolution shadow masks made of polyimide (PI) film (Kapton, 12.5 μm, Dupont, USA). c) A set of images of an array of ZnO TFTs and MEHs on silk, at various times after immersion in deionized water at room temperature.

encapsulating layers. Magnesium, deposited by electron beam evaporation through fine-line stencil masks made of polyimide (PI) films (Kapton, 12.5 µm, Dupont, USA), is used for the electrodes and interconnects (thicknesses between 200 and 500 nm). A first layer of Mg defines the source/drain electrodes for the TFTs (and, therefore the channel length, L_{ch}) and the bottom electrodes of the MEHs. Sputter deposition of thin films of ZnO (thicknesses between 350 and 500 nm) through PI masks forms semiconducting and piezoelectric components of the devices. The widths of the patterned ZnO films determine the channel widths (W) of the transistors. Layers of MgO (thicknesses between 100 and 150 nm) deposited by electron beam evaporation through PI masks serve as the gate dielectric layers for the TFTs. An additional patterned deposition of Mg (~400 nm) yields top electrodes for MEHs, and source, drain and gate contacts for the TFTs. A top encapsulating layer of silk can be applied by spin casting. All constituent materials, i.e. Mg (electrodes, contacts and interconnects), MgO (gate and interlayer dielectrics), ZnO (active material for the TFTs and energy harvesters/ strain gauges) and silk (substrate and encapsulant), dissolve in water. The products of this dissolution include Mg(OH)₂, Si(OH)₄ and Zn(OH)₂. Previous studies suggest that these compounds, and the device materials themselves, are biocompatible and environmentally benign.^[14,27,28] Figure 1c includes a set of images collected in a time sequence during dissolution in deionized water (DI) at room temperature. The silk substrate (~25 μ m), in the formulation used for this example, quickly disappears by simple dissolution. This process causes the device structures to physically disintegrate. Afterward, each remaining material disappears due to hydrolysis at different rates, as described in the following sections and previous reports.^[29–33] The time frames for dissolution can be programmed not only by encapsulation and packaging methods, but also by choices of dimensions, thicknesses and configurations in the materials for the device structures.

Dissolution of the constituent materials, other than the silk, involves hydrolysis to produce metal hydroxides. In the case of ZnO, the product is zinc hydroxide $(Zn(OH)_2)$, as a result of the reaction $ZnO + H_2O \leftrightarrow Zn(OH)_2$. Figure 2a shows a collection of images of a meander trace of ZnO (200 nm) at various times during hydrolysis. The trace completely disappears after 15 hours, in DI water at room temperature. The mechanisms of dissolution of ZnO can be analytically described by reactive diffusion models, in which water diffusion into the materials is the rate limiting process. Previous reports describe in detail the dissolution behaviors of ZnO and the dependence on pH, temperature, dimensions and surface structures.^[27,34–37] Additional experiments on dissolution, monitored by measurements of thickness as a function of time during immersion in several different types of solutions, such as phosphate buffer saline (PBS, pH 4.0, Sigma-

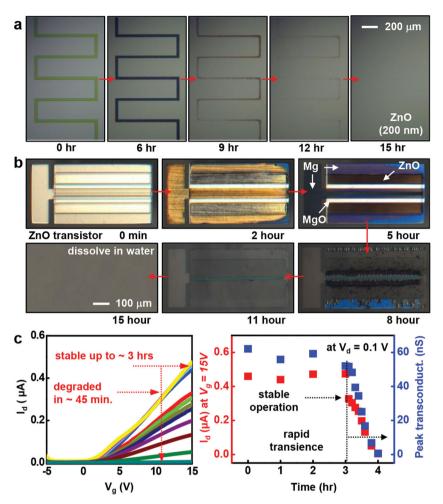


Figure 2. Dissolution kinetics of water soluble electronic materials, and devices. a) A series of optical microscope images collected at various times during dissolution of a meander trace of ZnO (200 nm) immersed in deionized water at room temperature. b) Images of a representative ZnO TFT at various times during dissolution. All components fully dissolve. c) Experimental results of degradation in electrical properties of a ZnO TFT encapsulated with MgO (500 nm) at various times after immersion in DI water. The linear scale transfer curves (left) and the drain current (I_d) at drain and gate voltages of $V_d = 0.1$ V and $V_g = 5$ V, respectively, and the peak transconductance (left) show that the operation of the device is stable for ~3 h, after which the properties quickly degrade in ~45 min.

Aldrich, USA) serum, and comparison of the results with theoretical models (see SI for details) appear in Figure S1a. The rate of dissolution ZnO increases with decreasing pH, consistent with a previous literature report.^[27] In acidic solution, the dissolution of ZnO is also attributed to the reaction, ZnO + 2H⁺ \rightarrow Zn₂ + H₂. A set of optical micrographs shows a fully formed ZnO TFT undergoing dissolution under similar conditions, as presented in Figure 2b. All electronic materials, i.e. Mg, MgO and ZnO, completely dissolve in 15 h after immersion in DI water at room temperature, in a controlled manner, without cracking, flaking or delamination. For the device dimensions studied here, the thicknesses of the layers determine, in large part, the timescales for dissolution.

Figure 2c summarizes the temporal variation in the electrical properties of a ZnO TFT, as it dissolves. (See Figure S1b for an image and diagram of the device.) In this case, a plate of glass serves as the substrate, and a layer of MgO (500 nm), deposited by electron beam evaporation, encapsulates

the entire system everywhere except at the contacts for source, drain, and gate electrodes which themsleves are not immersed. Measured transfer curves. drain currents (I_d) and peak transconductances show stable operation for ~3 h, followed by rapid degradation over the next ~45 min. (Additional electrical properties appear in Figure S1c.) The encapsulant and the device materials (mainly the Mg in this case) define the first and second timescales, respectively. The results of Figure 2c are only representative. The encapsulant material and thickness can be selected to achieve stable periods of device operation that match requirements for specific applications. For example, silk can be combined with MgO to enable the lifetime to extend from minutes to years, as demonstrated in a previous result.^[16] Complete electrical and mechanical characterization of ZnO TFTs and MEHs appear in Figure 3. All electrical measurements and bending studies were performed in a dry environment. Here, the TFTs use Mg (150 nm, source, drain and gate electrodes), ZnO (200 nm, active layer), MgO (100 nm, gate dielectric). Figure 3b illustrates additional details in optical micrographs of a typical TFT, collected after defining the channel configuration (top) and completing the fabrication (bottom). Analysis of current-voltage (I-V) characteristics (Figure 3c,d) of a typical device (channel length (L_{ch}) and width (W) are 20 µm and 500 µm, respectively) yields a mobility of ~0.95 cm²/V·s, an on/off ratio of >10³, a subthreshold swing of ~1 V/dec (at V_d = 0.1 V) and a threshold voltage of ~1 V. (See details on contact resistance of Mg

in Figure S1d). These properties are similar to those of nontransient counterparts.^[38-41] Previous literature studies suggest that deposition procedures and subsequent processing conditions for ZnO strongly affect the electrical properties.^[38,42-45] Careful parametric studies reveal conditions for sputter deposition that yield transistor characteristics (i.e. mobilities, on/off ratios, etc) in transient devices on silk that fall into a well established range set by more conventional sets of materials and substrates.^[40,46]

Figure 3e presents an image of an array of MEHs, each with a capacitor type geometry. A layer of ZnO (500 nm) lies between bottom (300 nm) and top electrodes (500 nm) of Mg that define an active area of 50 μ m × 2 mm. An MEH consists of six groups of devices; each group includes ten separate capacitor structures electrically connected in parallel. The six groups are connected in series. A IPC Flexural Endurance Tester (Model: CK-700FET) enables accurate evaluation of properties under bending. The test configuration involves the

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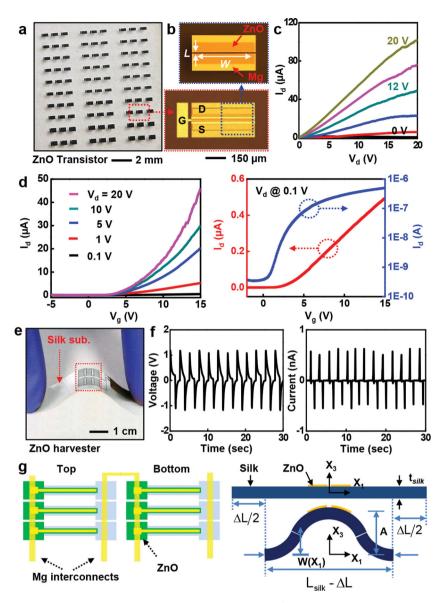


Figure 3. Electrical characterization of ZnO TFTs and MEHs. a) Image of an array of ZnO TFTs on a silk substrate. The devices use Mg (source, drain, and gate electrodes), ZnO (active layer) and MgO (gate dielectric). b) Optical micrographs of a TFT, after defining the channel configuration (top), and after completing the fabrication (bottom). c) Current-voltage characteristics of a typical device, at different gate biases. d) Linear scale transfer curves at various drain voltages (left), and linear (red) and log scale (blue) transfer curves at a drain voltage of 0.1 V (right). e) Optical micrograph of a transient, ZnO energy harvester on a thin film silk substrate, in a bent configuration. f) Output voltage vs time and output current vs time during cycles of bending. g) Schematic illustration of ZnO strips connected in series, and the theoretical shape for buckling of a device under compression.

two edges of the sample fixed within the two sliding fixtures of the instrument. During compression, the sample mechanically buckles upward to generate a well-defined, although non-uniform bending moment. Periodic variations in positive and negative voltage output peaks accompany the application and release of the buckling stresses (tensile at the location of the devices), respectively. The voltage and current outputs from an MEH are ~1.14 V and ~0.55 nA, as shown in Figure 3f. The peak output power density is ~10 nW/cm². The output averaged over the entire range of deformation, combined with a theoretical analysis of the mechanical input power required to bend the device, suggests a conversion efficiency of 0.28%, but in a way that is dependent on many parameters of the system, including the external electrical load. See Supporting Information. The structures are not fully optimized for efficiency. High absolute efficiencies might not be a relevant goal for many applications in bio-integrated devices. In such cases, the aim is to collect enough power to operate a device (e.g. a pacemaker), but to do so without inducing significant mechanical loading on natural motions of the relevant part of the body. High efficiency operation would, necessarily, impose constraints on motion, due to conversion of a significant fraction of mechanical work into electrical power. Such constraints can have adverse biological consequences, particularly in an organ like the heart which responds to mechanical loading by arrhythmic behavior. The efficiency can be improved through optimized choices of thicknesses, lengths, widths and Young's moduli for the substrate and piezoelectric layers.^[47] Furthermore, reduction in viscoelastic dissipation of the substrate can be beneficial.^[42] Figure 3g gives a schematic illustration of narrow strips of ZnO films connected in series, and the theoretically predicted shape of the buckled device.

Analytical models that couple the mechanical deformation and the piezoelectric effect provide additional insights into the behaviours. Compression of the silk substrate of length L_{silk} leads to its buckling with a representative out-of-plane displacement $w = A[1 + \cos(2\pi x_1/L_{silk})]/2$, where the origin of coordinate x_1 is at the center of silk substrate, and the amplitude A is related to the compression ΔL between two ends of the silk substrate by $A \approx (2/\pi) \sqrt{L_{silk} \cdot \Delta L}$ (see SI for details). The ZnO strips, together with the top and bottom electrodes, bend with the buckled silk substrate. The strain in the ZnO consists of membrane and

bending strains. The membrane strain is given analytically by $\varepsilon_m = 4\pi \sqrt{\Delta L/L_{silk}} (\overline{EI}_{silk}/\overline{EI}_{comp}) (h/L_{silk})$;^[48] (see SI for details), where \overline{EI}_{silk} and \overline{EI}_{comp} are the bending stiffnesses of the silk substrate and the composite structure of ZnO strips with electrodes and silk substrate, respectively; and *h* is the distance between the center of ZnO strips and the neutral mechanical plane of the composite structure (Figure S2). The bending strain is much smaller than the membrane strain since the ZnO strips are very thin. As a result, the total strain is essentially the same with the membrane strain. In addition, the bending strain has opposite signs above and below the center

of ZnO strips and does not contribute to the voltage and current output of the MEH (see SI for details).

The ZnO strips are transversely isotropic with elastic, piezoelectric, and dielectric constants c_{ij} , e_{ij} , and k_{ij} , respectively. The polarization direction x_3 is normal to the surface of the strip and the surface of the silk substrate. For plane-strain deformation ($\varepsilon_{22} = 0$) the strain ε_{33} and the electric field E_3 along the polarization direction x_3 satisfy the constitutive relations $0 = c_{13}\varepsilon_{11} + c_{33}\varepsilon_{33} - e_{31}E_3$ and $D_3 = e_{31}\varepsilon_{11} + e_{33}\varepsilon_{33} + k_{33}E_3$, where the electric displacement D_3 along the polarization direction is a constant to be determined. For measurements of current, the top and bottom electrodes are connected to an ammeter as shown in Figure S2b. The ammeter has negligible electrical resistance, and therefore negligible voltage drop. The current (through the electrodes and ammeter) results from the moving charge induced by the strain in the ZnO (i.e., piezoelectric effect) even without voltage between the top and bottom electrodes. The zero voltage between the top and bottom electrodes of each ZnO strip, together with the above equations, gives $D_3 = \bar{e}\varepsilon_m$ $\bar{e} = e_{31} - (c_{13}/c_{33})e_{33}$, where is the effective piezoelectric constant. For each group of device in series, the current is given by $I = -A_{ZnO}D_3$, where A_{ZnO} is total area of ZnO strips in each group. For a representative compression $\Delta L = \Delta L_{max} [1 - \cos(2\pi t/T)]^2/4$ with the maximum compression ΔL_{max} and period T, the maximum current is obtained as

$$I_{\max} = 4\pi^2 \frac{(-\bar{e}) A_{ZnO}}{T} \frac{\overline{E I}_{silk} h}{\overline{E I}_{comp} L_{silk}} \sqrt{\frac{\Delta L_{\max}}{L_{silk}}}$$
(1)

For $\Delta L_{\text{max}} = 1.5$ cm, T = 2.3 second and $L_{silk} = 3$ cm as in experiments, $\overline{EI}_{silk}/\overline{EI}_{comp} = 0.34$, $h = 5.5 \,\mu\text{m}$ and $A_{ZnO} =$ $1.08 \,\text{mm}^2$ from the specimen geometry (see SI for details), and $\bar{e} = -0.67 \,\text{C/m}^2$, which is on the same order of magnitude as the literature values.^[8,49] Equation (1) gives the maximum current $I_{\text{max}} = 0.55$ nA, which agrees well with the experimental result as shown in Figure 3f.

For measurements of voltage, if V denotes the total voltage for n groups of devices in series, then the voltage across each group is V/n. The electric displacement becomes $D_3 = \bar{\epsilon}\varepsilon_m + \bar{k}V/(nt_{ZnO})$, where $\bar{k} = k_{33} + (e_{33}^2/c_{33})$ is the effective dielectric constant and t_{ZnO} is the thickness of ZnO strips. The current $I = -A_{ZnO}D_3$ is also related to the voltage V and resistance R of the voltmeter by I = V/R, which gives $V/R = -A_{ZnO}\dot{D}_3$, or equivalently

$$\frac{dV}{dt} + \frac{nt_{ZnO}}{A_{ZnO}R\bar{k}}V = -\frac{n\bar{e}t_{ZnO}}{\bar{k}}\frac{d\varepsilon_m}{dt}$$
(2)

For $\Delta L = \Delta L_{\text{max}}[1 - \cos(2\pi t/T)]^2/4$ and the initial condition V(t = 0) = 0, the maximum voltage is given by

$$V_{\rm max} \approx 4\pi^2 R \frac{(-\bar{e}) A_{ZnO}}{T} \frac{\overline{E I}_{silk} h}{\overline{E I}_{comp} L_{silk}} \sqrt{\frac{\Delta L_{\rm max}}{L_{silk}}}$$
(3)

For $R = 2.3 \times 10^9 \Omega$ in the experiment, the theory gives the maximum voltage 1.1V, which agrees well with experiment result of 1.14V. In addition to electrical characterization of devices, the intrinsic piezoelectric and morphological properties of active layer ZnO thin film by sputtering system was studied by AFM, SEM, and XRD techniques in detail (Figure S3).

The results presented here indicate that ZnO can be used effectively as an active material for transient electronics, as well as for energy harvesting and strain sensing devices, for which all of the consituent elements dissolve completely in water. Compared to silicon, ZnO has features, such as wide, direct bandgap and piezoelectric responses, that could enable expanded capabilities in transient devices. The use of this material alone, or in heterogeneous configurations with silicon, opens up additional application possibilities for transient technologies, in areas ranging from biomedicine, to environmental monitoring and certain areas of consumer electronics.

Experimental Section

Fabrication of ZnO TFTs and MEHs: All electronic materials were directly deposited onto silk substrates through high resolution stencil masks made of polyimide (PI) films (Kapton, 12.5 μm, Dupont, USA). These materials consist of ZnO (semiconductor), Mg (conductors), MgO (insulators), and silk (substrate). A layer of Mg (150 nm) deposited by electron beam evaporation (Temescal) defined the source and drain electrodes for the TFTs. ZnO (200 nm) deposited by RF magnetron sputtering (AJA) through a PI mask served as the semiconductor. A high-purity of ZnO target was used (99.99%), with base pressures of 2×10^{-6} torr, and working pressures of 15 mTorr, maintained with a Ar (99.99%): $O_2 = 2:1$ (sccm) gas mixture. The sputtering was performed at room temperature (RT) with an RF power of 250 W, immediately after cleaning the target with Ar plasma for 5 min. The deposition rate was ~150 nm/h. Electron beam evaporation of MgO (100 nm), also through PI masks, defined the gate dielectrics. The gate electrode consisted of Mg (300 nm), deposited and patterned using schemes similar to those for the source and drain.

ZnO MEHs were designed in six groups, each of which contains ten separate devices (ZnO strips with Mg electrodes on top and bottom, in a capacitor type geometry). Devices within each group were connected in parallel; the six groups themselves were connected in series. The fabrication began with deposition of Mg (300 nm) by electron beam evaporation through a Pl shadow mask, to form bottom electrodes. A layer of ZnO (400~500 nm) was then formed by RF sputtering, through a shadow mask aligned to the Mg bottom electrodes. Top electrodes of Mg (~500 nm) were formed in a manner similar to that for the bottom electrodes. Individual ZnO strips defined active areas of 50 μ m × 2 mm. Square pads at their ends faciliated electrical top and bottom contacts. The ZnO layer was formed in a geometry slightly bigger than that of the bottom electrode to avoid shorting of top to bottom, as seen in Figure S2.

Investigation of ZnO Thin-Film Properties and Device Analysis: X-ray diffraction (XRD, Philips X'pert) revealed that the films consist of hexagonal ZnO, with prefered orientation of (002). Scanning electron microscope (SEM, Hitachi S4800) imaging determined the surface topography and provided cross sectional views of the films. Measurements of voltage induced displacements in thin films of ZnO were conducted by atomic force microscopy (AFM, Asylum Cypher, USA). A semiconductor parameter analyzer (4155C, Agilent) was used to measure the electrical characteristics of TFTs and MEHs.

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Bending Tests for Energy Harvesters/Strain Gauges: A commercial instrument (IPC Flexural Endurance Tester Model: CK-700FET) was used to perform bending experiments. The test involved compressing a sheet of devices bewteen two clamped edges; the result was a buckling structure whose curvature was defined by the extent of compression. Electrical measurements revealed positive and negative swings in voltage and current output, corresponding to the application and release of such buckling stresses. An analytical model of the mechanical deformations and the associated piezoelectric effects captured the experimental observations.

Dissolution Experiments: Dissolution tests were performed to study degradation behaviors of devices and kinetics of materials removal. To observe dissolution of ZnO, a meander trace of ZnO (200 nm) on a glass substrate was submerged in DI water at room temperature. Optically significant changes were observed after 9 hours, and complete disappearance occurred in 15 h. In a similar way, a ZnO transistor, consisting of Mg, MgO, and ZnO, on glass was used to illustrate the various stages of dissolution at the device level. Most components disappeared within 8 h; complete dissolution occurred within 15 h. In addition, measurements of changes in electrical properties defined timescales of device function. A transistor with a design similar to that described above was prepared and encapsulated with a layer of MgO (500 nm). Measured and calculated characteristics revealed two-stage kinetics. The first was determined by the encapsulation layer; the second, primarily by the Mg electrodes.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Materials for Bioresorbable Radio Frequency Electronics

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Devices constructed using bioresorbable materials have many roles in clinical medicine, ranging from drug delivery vehicles^[1,2] to stents^[3,4] and sutures.^[5,6] In such cases, the function is defined primarily by the mechanics and/or the structure of the component, with operation that is often passive. The ability to achieve similar bioresorbable characteristics in active semiconductor devices and sensors could significantly expand the possible modes of use. Past approaches include partially resorbable systems based on miniaturized silicon transistors bonded to biomaterial substrates and, in separate work, on organic active materials (e.g. semiconductors).^[7-11] Recent studies demonstrate a completely water soluble class of silicon-based technology,^[12] to enable devices and systems that build on foundational knowledge and engineering capabilities derived from the integrated circuit industry. Components of this type can be implanted into the human body where they gradually dissolve into biofluids after their useful functional life, thereby eliminating unnecessary device load without the need for surgical extraction. For many applications, radio frequency (RF) operation is a key feature, both for data transmission and for power supply. The results presented here represent progress in this direction. We report antennas, rectifying diodes, transistors,

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capacitors, inductors, resistors, ring oscillators and RF energy harvesting sub-systems, all of which involve water soluble and biocompatible constituent materials, i.e. silicon nanomembranes (Si NMs; semiconductors), magnesium (Mg; conductors), silicon dioxide or magnesium oxide (low temperature SiO₂ or MgO; interlayer dielectrics), and silk (substrates).

One of the most critical, but simplest, elements in RF systems for wireless reception/transmission is in the antenna. Transient antennas can be formed by evaporation of Mg (500 nm) through stencil masks made of polyimide (PI) films (Kapton, 12.5 µm, Dupont, USA) on thin films of silk. Two designs form the focus of studies reported here: simple linear dipoles consisting of two quarter wavelength arms and wideband quasi log-periodic dipoles, designed to operate at ~2.4 GHz and ~950 MHz, respectively. Figure 1a presents images of a transient Mg antenna at a sequence of times during immersion in deionized (DI) water at room temperature. The Mg and silk completely disappear after ~2 hours by hydrolysis and simple dissolution, respectively. An alternative route to similar antennas, but with thicknesses that can be much larger than the skin depth at relevant RF frequencies, exploits Mg foils (thickness from 5 µm to 50 µm, purity of 99.9%, Goodfellow, UK) cut into appropriate shapes. A layer of solvent-perfused silk serves as an adhesive to bond such antennas to silk substrates (Figure S1a). The measured S-parameters in Figure 1b show that both antennas are well matched to their designed operating frequencies. Images of the devices with coaxial connectors appear in Figure S2. Figure S1b shows a 950 MHz antenna integrated with a commercial RF power scavenging system on a printed circuit board to demonstrate functionality. Additional details can be found in Figure S1c.

Various transient devices with passive RF function, such as capacitors, inductors, and resistors, are also essential. Figure 1, c to g, provides images and electrical properties of several such components. As an example, a simple transient resistor consisting of a serpentine trace of Mg (Figure 1c) formed by evaporation onto silk through a stencil mask, indicates a resistance of 100 ohm, suitable for use in RF currentlimiters and voltage dividers. Capacitors and inductors can be formed on silk in which MgO (900 nm thick, formed by electron beam evaporation) serves as the dielectric, and Mg forms the electrodes and conducting traces. (Details appear in the experimental section.) The capacitors explored here exploit simple, parallel plate geometries with various lateral dimensions (Figure 1d; 150 μ m \times 150 um (black), 250 μ m \times 250 μ m (red), 400 μ m × 400 μ m (blue) and 550 μ m × 550 μ m (green)). Measured capacitances and Q factors of each capacitor appear in Figure 1e, along with simulation results. The operating frequencies extend up to ~6 GHz. Simple inductors (Figure 1f)

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а 4 cm dissolve in water @ RT Ma antenna Silk 0 min 1 min 5 min 60 min 120 min 30 min 200 10 b **P** 5 S11 (dB) 100 ^Ĝ rent 950 MHz -20 2.4 GHz 10 1 ō 2 0 1 Frequency (GHz) Mg resistor -- 200 µm Voltage (V) 100 20 е d s - 1 (PF) 80 15 - 2 Mg - 3 00 factor Capacitarice MgO 40 Mq 20 0 0Ľ 2 6 8 4 6 Frequency (GHz) Frequency (GHz) 3 mm Mg cap. g f s 40 Inductance (nH) - 2 30 3 factor 20 ō 10 야 0 0 10 10 6 8 2 4 6 8 Frequency (GHz) Frequency (GHz) Ma ind 1 mm

Figure 1. Images and electrical properties of various passive components for transient RF systems: (a) A set of images of an antenna built with Mg on a silk substrate illustrates the process of dissolution in DI water. The Mg disappears completely by hydrolysis within ~2 hours. (b) Measured reflection coefficient S11 of Mg antennas operating at 950 MHz and 2.4 GHz. (c) Optical microscope image of a Mg resistor (left), and its current-voltage characteristics (right). The resistance is ~100 ohm. (d) Image of capacitors of different sizes built using Mg electrodes and MgO dielectrics. (e) Measured capacitance (left) and Q factor (right) as a function of frequency. Experimental results and simulations appear as lines and dots, respectively. The region of overlap between the top and bottom Mg electrodes in these metal-insulator-metal (MIM) capacitors is 150 μ m imes 150 μ m imes 150 μ m (black), 250 μ m imes 250 μ m (red), 400 μ m imes 400 μ m (blue) and 550 μ m \times 550 μ m (green). The inset provides a schematic illustration of a device. (f) Image of a collection of inductors that use Mg electrodes and MgO for interlayer dielectrics. The number of turns (n), outer diameter (d) and metal width/space (w/s) are 3, 440 μ m, 20/20 μm (green), 2, 440 μm, 40/20 μm (blue), 2, 1 mm, 100/20 μm (red), 3, 1 mm, 50/20 μm (black). (g) Measured inductance (left) and Q factor (right) as a function of frequency up to ~8 GHz for four representative inductors. Experimental results and simulations appear as lines and dots, respectively.

can be built using planar spiral coils with 2 or 3 turns; connections to the inner terminals use MgO (900 nm) as an interlayer dielectric. These devices have different resonance and maximum operating frequencies (Figure 1g, from 2 GHz to



8 GHz). The Q factors are modest, but can be improved by increasing the thickness of the Mg. Additional measurements and simulations on capacitors and inductors appear in Figure S3 to S5. Electrical behaviors in capacitors and inductors can be captured quantitatively using equivalent circuit models and parameters. Here, the devices are represented by a combination of main and parasitic parameters, such as inductances, capacitances, and resistances, that yield a good match with the measured characteristics. The circuit simulations use these device models.

Most RF circuits demand semiconductor devices. Figure 2a presents a schematic illustration of structures for transient RF silicon PIN diodes that use Mg contacts to silicon nanomembranes (Si NMs, thickness ~300 nm, p-type) with heavily doped p-type and n-type regions separated by lightly doped, nearly intrinsic areas. The fabrication involves patterned boron and phosphorous doping (950 °C ~ 1050 °C) of Si NMs while they are supported on a silicon wafer. Transfer printing delivers the Si NMs onto a film of silk cast on a separate wafer. Electron beam evaporation of Mg (~400 nm thickness) through a fineline stencil mask aligned to the doped regions of the Si NMs defines the contacts and interconnects. (Details appear in the experimental section.) Electrical measurements of a representative device (length and width of the intrinsic region: 5 µm and 1 ~ 2 mm, respectively) in Figure 2b indicate expected diode behavior, with a turn-on voltage at ~0.7 V and a forward current of ~1.5 mA at 1 V (left). Operation as a rectifier extends to a few GHz (right). Output responses to alternating current inputs at various frequencies, and measurements and simulations of the S-parameters appear in Figure S6 and S7. Figure 2c illustrates the dissolution kinetics of similar diodes fabricated on a glass substrate, encapsulated by a uniform layer of MgO (~500 nm thickness), and partially immersed in deionized (DI) water at room temperature. The measured electrical properties indicate stable operation for ~4 hours, followed by rapid degradation in ~45 minutes. The first stage of this kinetics depends on dissolution of the MgO encapsulant and/or permeation through it; the second depends mainly on hydrolysis of the Mg electrodes. The thickness of the

MgO can be selected to define the first time scale, in a way that does not affect device performance. Other encapsulating materials can be considered for times that extend beyond those practically accessible with MgO.^[12]

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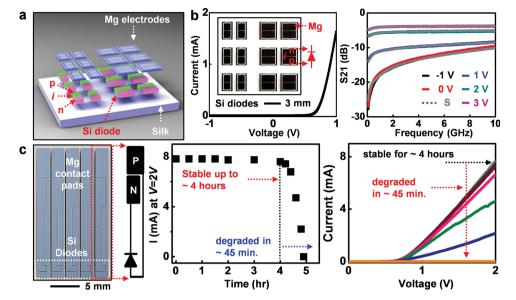


Figure 2. Electrical measurements of transient diodes, and dissolution kinetics of a representative diode and antenna: (a) Schematic illustration of Si NM PIN diodes (rectifiers) fabricated with Mg electrodes on a silk substrate. The near intrinsic "i" region has dimensions of $\sim 5 \ \mu m \times 1 \sim 2 \ mm$. (b) Current-voltage characteristics of a representative diode (left), including an image in the inset, and measured values (lines) and simulations (dots) of the S21 scattering parameter at frequencies up to 10 GHz with different DC biases (right). (c) Measurements of dissolution kinetics of a diode encapsulated with MgO (~500 nm). The results show stable current output for ~4 hours, followed by rapid degraded over the following ~45 min. due to dissolution of the Mg electrodes.

RF transistors enable active functionality. To demonstrate possibilities in transient RF, we constructed three-stage complementary metal-oxide-semiconductor (CMOS) ring oscillators using transient n-channel and p-channel metal-oxidesemiconductor field-effect transistors (MOSFETs) based on Si NMs, with Mg (~250 nm) for source, drain, gate contacts and interconnects, and MgO (~80 nm) for the gate dielectrics. Figure 3a provides an illustration and a schematic circuit diagram. To enable both n- and p-channel MOSFETs in a single Si NM, high temperature diffusion procedures create lightly doped p-wells (p⁻), and highly doped source and drain contacts for each MOSFET (n⁺, p⁺). Source and drain electrodes formed next to the p-wells define p-channel MOSFETs. Heavily doped regions for source and drain regions inside the p-wells enable contacts for n-channel MOSFETs. (See details in experimental section.) Figure 3b and 3c represent transfer curves and full current-voltage characteristics measured from p-channel and n-channel devices, respectively. Optical microscope images appear in the insets. In both types of MOSFETs, the on/off current ratios (I_{on}/I_{off}) are ~10⁵. The mobilities are ~70 cm²/V · s and \sim 350 cm²/V·s, for the p- and n-channel cases, respectively. Measurements on a typical CMOS inverter appear in Figure 3d; the gain and threshold voltage (V_{th}) are ~60 and -1 V, respectively. The negative threshold voltage of the inverters results mainly from the high negative threshold voltage (~5 V) of the p-channel MOSFETs. Figure 3e shows time-domain output voltage characteristics of a ring oscillator. The operating frequency can be adjusted, up to ~4.1 MHz, with applied bias, 10 V (black), 15 V (red), 20 V (blue). Theoretically, this frequency is inversely proportional to the number of stages (N) and linearly proportional to the applied voltage (V_{dd}). In the absence of other factors, the relative slope is expected to be approximately 1. Deviations from

this behavior suggest some non-idealities, likely due to propagation delays and parasitic capacitances. $^{\left[13,14\right] }$

The various transient RF electronic devices described previously can be integrated together for higher levels of functionality. A transient wireless RF power scavenger circuit provides a good example (Figure 4). The circuit contains an RF antenna, an inductor, six capacitors, a resistor and eight diodes, as shown in Figure 4a-b. A circuit diagram appears in Figure 4c. In this case, a thin layer of polyimide provides mechanical support to facilitate transfer of the entire, interconnected system (except for the antenna) to silk at improved yields. Connecting the input of the system to an RF function generator and the output to a commercial LED indicates effective rectification, over a frequency range from 10 kHz to 950 MHz (Figure 4d). Additional data appear in Figure S7e. By connecting the circuit to a Mg antenna designed for operation at 950 MHz, the system can wirelessly harvest energy from an RF transmitter, to turn on a LED at a distance of ~2 meters, as shown in Figure 4e. The power received by the antenna is approximately 17.3 dBm (54 mW) and the LED consumes a power of 8.5 mW. The resulting power conversion efficiency (PCE) is determined to be -8 dB (15.7%). This value is somewhat smaller than those of commercial bridge rectifiers, which range from 26.5% to 37%, due to their use of optimized fabrication processes and materials.^[15-17] Systems based on half-wave rectification circuits can also power LEDs, but with reduced efficiencies compared to the case of the full-wave rectifier (Figure S8). Circuits designed to enable integration with Si CMOS ring oscillators powered by scavenging circuits appear in Figure S9. In all examples, the electronic materials are water-soluble/biodegradable. Figure 4f shows a set of images collected at different times during dissolution. The entire power scavenger initially disintegrates in DI water at room temperature due to dissolution of the silk substrate; subsequently,



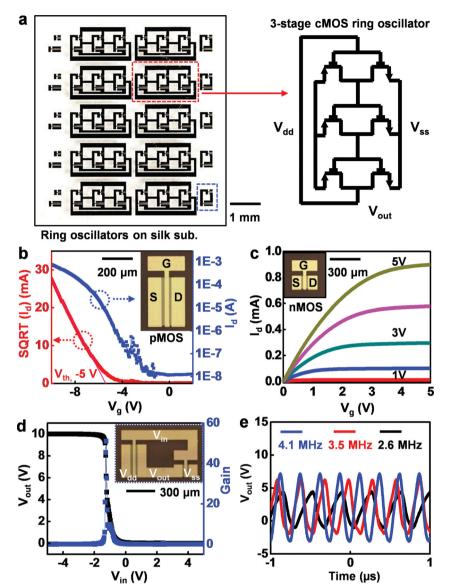


Figure 3. Images and measured properties of transient CMOS inverters and ring oscillators: (a) Image of CMOS three-stage ring oscillators (left), and circuit diagram (right). (b) SQRT (red) and log scale (blue) transfer curves of a typical transient p-channel MOSFET. The channel length (L) and width (W) are 5 μ m and 300 μ m, respectively. The mobility and on/off ratio are ~70 cm²/V·s and ~10⁵, respectively. The inset shows a microscope image of a representative device. (c) *I*–V characteristics of a typical n-channel MOSFET. The channel length (L) and width (W) are 15 μ m and 100 μ m, respectively. The mobility and on/off ratio are 350 cm²/V·s and ~10⁵, respectively. All MOSFETs use Mg for source, drain and gate electrodes, and MgO for the gate dielectric. (d) Output voltage characteristics of a representative CMOS inverter with V_{dd} = 10 V. The voltage gain is ~60. An optical microscope image appears in the inset. (e) Measured time domain responses of a ring oscillator at different frequencies.

the remaining materials reactively dissolve at their respective rates. A thick layer of Mg (~3 μ m) requires some days to dissolve. At these neutral pH levels, the Si and the low temperature SiO₂ formed by plasma-enhanced chemical-vapor deposition (PECVD) dissolve at rates that are much slower than those at physiological conditions.^[12] (Under such conditions, thermal SiO₂ dissolves at rates that are negligibly small)

In summary, the materials, device designs and manufacturing strategies described here provide a baseline of

components for RF transient electronics. The results demonstrate the versatility of the constituent materials and associated fabrication processes, and provide building blocks that are essential to many envisioned uses of transient technologies, particularly in wireless power delivery and communication approaches for implantable medical devices and environmental monitors.

Experimental Section

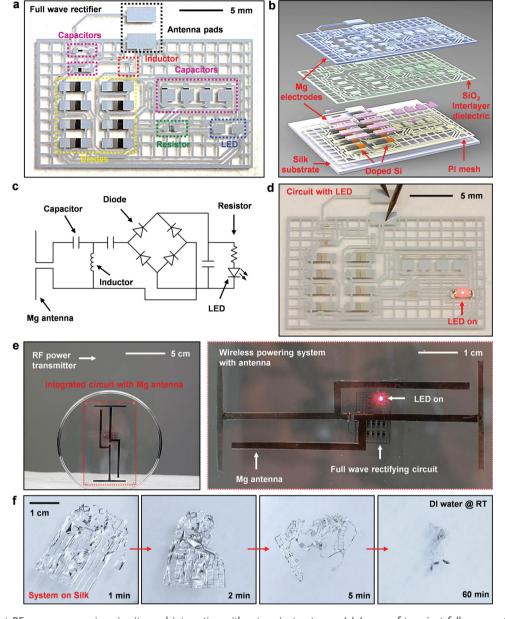
Fabrication of transient passive components (capacitors and inductors): Mg electrodes (~200 nm) for bottom contacts (capacitors) and crossovers (inductors) were formed by electron beam evaporation on a silk substrate. Deposition of MgO (~900 nm) defined interlayer dielectrics. Another layer of Mg served as top electrodes for capacitors (~1 μ m), and planar spiral coils for inductors (~3 μ m). In all cases, high resolution stencil masks made of polyimide (PI) films (Kapton, 12.5 μ m, Dupont, USA) were used to pattern the Mg and MgO.

Fabrication of transient Si CMOS ring oscillators: Three different doping procedures were performed on an n-type SOI wafer (SOITEC, France). Boron doping at 550 °C using spin-on dopant (SOD, Filmtronics, USA) defined lightly doped regions for the p-wells (p-). Heavily doped p-type regions for source and drain electrodes were formed at 1050 °C for p-type transistors. Phosphorous doping at 950 °C defined highly doped areas for source and drain contacts for n-type transistors. These doped silicon nanomembranes (Si NMs) were isolated by reactive ion etching (RIE; Plasmatherm) with sulfur hexafluoride (SF₆) gas. To release the Si NMs from the SOI, the buried oxide was partially removed by wet etching with hydrofluoric acid (HF, 49% electronic grade, ScienceLab, USA). Next, patterning a layer of photoresist (AZ 5214) formed structures that anchored the Si NMs to the underlying wafer during a second etching step to complete the removal of the buried oxide. Individual Si NMs formed by this procedure were transfer printed onto a temporary "carrier" substrate coated with a layer of silk. Gate dielectrics (MgO, ~80 nm), as well as electrodes and interconnects (Mg, ~300 nm) were deposited by electron-beam evaporation through fine-line stencil masks.

Fabrication of transient RF power scavenger systems: High temperature diffusion doping of boron at ~1050 °C and phosphorous at ~950 °C using spin-on dopant established desired patterns of doping in the top silicon layer of a silicon-on-insulator (SOI, SOITEC, France) substrate. Thermally grown oxide

(~1100 °C) served as the doping mask. Removal of the buried oxide layer (~1 μ m) with HF, released doped Si NMs (thickness ~300 nm, p-type), for transfer printing onto a carrier wafer coated with poly (methylmethacrylate) (PMMA, ~100 nm; sacrificial) and polyimide (PI, ~1.2 μ m; cured at 250 °C for 1 hour in a glove box). Active device regions were isolated by RIE with SF₆ gas. The first layer of electrodes/interconnects was defined by lift-off using LOR 20B (Microchem, USA) and AZ 5214 photoresists, with Mg (150 nm) deposited by leectron beam evaporation. A 900 nm thick layer of SiO₂ was deposited by low temperature plasma-enhanced chemical-vapor deposition (PECVD). Openings to the contacts were formed by





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Figure 4. Transient RF power scavenging circuits, and integration with a transient antenna: (a) Image of transient full-wave rectifying circuit that includes an array of diodes and capacitors, an inductor, a resistor and antenna pads, all fabricated with transient electronic materials: Si NMs (semiconductors), Mg (electrodes), SiO₂ (interlayer dielectrics), and silk (substrates). (b) Schematic exploded view illustration. (c) Circuit diagram. (d) Operational demonstration of a full wave rectifying circuit with a commercial LED. (e) Image of a full wave rectifying system powered wirelessly with an RF transmitter and a Mg receiving antenna (left), and magnified view (right). The working distance here is ~2 meters. (f) Images of a rectifying circuit immersed in deionized water after 1 min, 2 min, 5 min and 1 hour, respectively.

buffered oxide etching (BOE, 6:1, Transene company, USA) of the SiO₂. Photolithography (AZ nLOF 2070, Microchem, USA) and liftoff with a thick film of Mg (~3 μ m) defined the second layer of electrodes/interconnects. Next, an oxygen RIE (March) step created an open mesh pattern in the PI to allow removal of the PMMA by immersion in acetone. Entire devices released in this manner were then transfer printed onto a film of silk.

RF electrical characterizations: Each passive component was measured for scattering (S-) parameters using an Agilent E8364A performance network analyzer. An external DC power supply was applied to the diodes using a bias-tee during testing. The measurement setup was calibrated to the probe tips using a standard Short-Open-Load-Thru (SOLT) on-wafer probing kit for a frequency range of

45 MHz—20 GHz. Aglilent Advanced Design System (ADS) was used to extract device model parameters from the respective equvilent circuits. The antennas were connected to SubMiniature - A (SMA) connectors with silver epoxy. Their impedance characteristics were measured using an Agilent 5062A network analyzer with 1-port Open-Short-Load calibration.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.







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Materials and Fabrication Processes for Transient and Bioresorbable High-Performance Electronics

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Materials and fabrication procedures are described for bioresorbable transistors and simple integrated circuits, in which the key processing steps occur on silicon wafer substrates, in schemes compatible with methods used in conventional microelectronics. The approach relies on an unusual type of silicon on insulator wafer to yield devices that exploit ultrathin sheets of monocrystalline silicon for the semiconductor, thin films of magnesium for the electrodes and interconnects, silicon dioxide and magnesium oxide for the dielectrics, and silk for the substrates. A range of component examples with detailed measurements of their electrical characteristics and dissolution properties illustrate the capabilities. In vivo toxicity tests demonstrate biocompatibility in sub-dermal implants. The results have significance for broad classes of water-soluble, "transient" electronic devices.

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biomedical Implantable components serve critically important roles in modern clinical medicine. Such devices can be classified into two types: those that exist for long periods of time, typically designed to be permanent; and those that disappear, or resorb, in the body after they provide some useful function. The former includes both simple, passive devices such as artificial joints and pins,^[1] as well as sophisticated electronic components such as deep brain electrical stimulators,^[2] cardiac pacemakers^[3] and programmable drug delivery systems.^[4] The latter, by contrast, is currently available only in

the form of passive elements such as resorbable sutures^[5,6] or matrices for drug release,^[7,8] degradable intravascular stents^[9,10] and resorbable plate-screw systems.^[11] An unaddressed technology opportunity, then, exists in biodegradable devices that are capable of active electronic processing, sensing, communication and/or actuation within or on the surface of the body. Envisioned uses range from non-antibiotic appliques designed to reduce the incidence of surgical site infections, to electrical stimulators that can accelerate bone growth, to systems that can release drugs at programmed intervals. In each case, the devices operate only over some finite period of time, typically defined by a healing process; afterward, they resorb to eliminate unnecessary device load without surgical intervention.

Initial, early technical work toward this type of technology yielded two examples of partially resorbable devices, in the sense that certain, but not all, of the component materials resorb. One involves ultrathin electrodes and/or transistors built on films of silk fibroin, engineered to facilitate conformal contact with biological tissues, as demonstrated in electrocorticography,^[12] or to disperse thin, miniaturized electronic components in ways that minimize adverse body responses, as demonstrated in sub-dermal implants.^[13] The other uses organic or bio-organic semiconductors with polymer dielectrics/substrates to yield systems in which all components except for the electrodes and interconnects dissolve in bio-fluids, in a potentially biocompatible manner.^[14,15] Although the modest properties of known organic electronic materials limit the performance that can be achieved, this approach has some potential for devices that require only simple functions. A recent report describes



materials and schemes that bypass constraints associated with these two previous directions.^[16] The result is a fully resorbable, high performance class of electronics, where ultrathin sheets of semiconductorgrade monocrystalline silicon (i.e., silicon nanomembranes, or Si-NMs) serve as the active materials, inorganic dielectrics (e.g., MgO, SiO₂) and conventional metals (e.g., Mg) provide the other electronic functions, and silk forms the substrate and encapsulation layers. Enabled devices encompass nearly all of the key building blocks for integrated circuits, ranging from metal-oxide semiconductor field-effect transistors (MOS-FETs) to pn junction diodes, resistors, inductors and capacitors. Additional demonstrated components include solar cells, photodetectors, strain and temperature gauges, inductive power delivery systems and others. Although initially conceived for bioresorbable devices and demonstrated in programmable non-antibiotic bacteriocidal appliqués, this same technology can be more generally considered as a physically transient form of electronics, capable of disappearing via controlled physical or chemical change with welldefined rates. Non-biological applications include environmental sensors that avoid the need for recovery and collection after use, and consumer devices that minimize costly and hazardous disposal procedures.

A disadvantage of the original embodiment of this class of transient electronics is that many of the fabrication steps occured on a transient substrate (e.g., silk), thereby constraining significantly the temperatures, lithographic techniques, solvents and other aspects of the processing. These limitations prevent the use of manufacturing techniques that serve as the basis for high volume, low cost production of commercial silicon integrated circuits. The work described here establishes a silicon wafer-based strategy to fully formed transient circuit components and circuits, in configurations that allow their subsequent, and separate, integration with transient substrates and packaging mate-

rials. The results are important because they have the potential to enable realistic manufacturing strategies for transient electronics, in which only modest modifications to microelectronic fabrication facilities are needed. The concepts rely on the combined use of a specialized type of silicon on insulator (SOI) wafer and the techniques of transfer printing. The resulting devices involve constituent materials that all have some solubility in water: silicon, silicon dioxide, magnesium oxide, magnesium and silk. The following describes the concepts and demonstrates their use in fabrication of various electronic components and simple logic gates, with studies of their transient

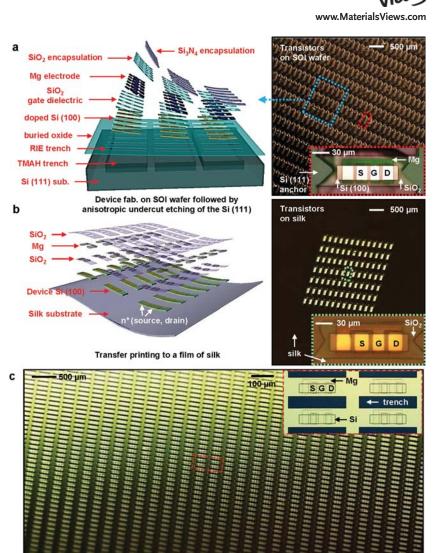


Figure 1. Wafer-scale fabrication of fully formed transient transistors on specialized SOI substrates and their subsequent transfer printing to films of silk. a) Schematic exploded view illustration and optical microscope images of devices after complete processing followed by anisotropic undercut etching of the surface region of the SOI wafer substrate with TMAH. The inset shows a magnified view of an individual transistor in the array. b) Schematic illustration and image of these same devices after transfer printing to a film of silk. The inset shows a magnified view of an individual transistor. The device uses magnesium (Mg; \approx 200 nm) for source, drain and gate electrodes, silicon dioxide (SiO₂) for the gate (\approx 100 nm) and interlayer (\approx 100 nm) dielectrics, silicon (Si) for the semiconductor (\approx 100 nm) and silk for the substrate (\approx 25 µm). c) An optical image of a large area of n-channel MOSFETs, with microscope image of a representative set of devices in the inset.

behaviors both through in vitro investigations of the kinetics and in vivo evaluations of biocompatibility and resorption.

2. Results and Discussion

The overall scheme involves complete fabrication of circuits and/or circuit components in transient materials on a silicon wafer, followed by their controlled release and subsequent integration onto a transient substrate via transfer printing. **Figure 1** presents exploded-view schematic illustrations and



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optical micrographs of a representative system composed of a large-scale array of transient n-channel monocrystalline silicon metal-oxide field-effect transistors (MOSFETs), undercut etched from a SOI (111) wafer on which they were formed (Figure 1a) and after their transfer to a thin sheet of silk as a substrate (Figure 1b). The SOI wafer consists of ultrathin top layer of Si (p-type, ≈100 nm) with (100) orientation for the active regions of the devices, a buried oxide layer ($\approx 1 \mu m$) and supporting wafer with (111) orientation. The orientation of the wafer plays a critical role in the release of devices from its surface, as described in the following. Fabrication begins with high temperature, patterned doping (phosphorous at ≈950 °C) of the top Si to define the channel regions and contacts for the MOS-FETs. Patterned etching of the silicon creates isolated regions for each of the devices. A coating of SiO₂ (≈100 nm) deposited by plasma-enhanced chemical-vapor deposition (PECVD) at 250 °C forms the gate dielectric. Etching in buffered oxide etchant (BOE, 6:1, Transene Company, USA) creates windows for source and drain contacts. Depositing Mg (≈200 nm) by electron beam evaporation yields source, drain and gate electrodes aligned to the contacts and channel areas (Supporting Information Figure S1a). Sequential PECVD steps define encapsulation layers of SiO₂ (\approx 100 nm thick; patterned to expose the source, drain, and gate contacts) and Si₃N₄ (≈400 nm thick; uniform across the entire area). Deep etching through a hard mask of Cr/Au (10/200 nm) establish trenches between the devices, down to a depth of $\approx 1.5 \ \mu m$ into the (111) silicon supporting wafer (Supporting Information Figure S1b). Anisotropic wet etching of the underlying (111) silicon with tetramethyl ammonium hydroxide (TMAH, 25 wt% in H₂O, Sigma-Aldrich, USA; 30 min at 100 °C) leaves free-standing MOSFETs tethered to the wafer at their ends by bridging films of the buried oxide (Supporting Information Figure S1c). Cross-sectional images in Supporting Information Figure S1d illustrate that the undercut proceeds in the (110) direction, along the surface of the wafer, to allow efficient release. Details appear in Supporting Information Figure S2. Free-standing MOSFETs created in this manner have total thicknesses of $<2 \mu m$, including the buried oxide layer (~1 µm). Because the SOI substrates and processing conditions are compatible with state-of-the-art commercial microelectronics fabrication facilities, dramatic reductions in the thicknesses and lateral dimensions are possible.

Figure 1b illustrates an array of such MOSFETs after release from the SOI substrate and integration onto a film of silk, using the techniques of transfer printing.^[17] A reactive ion etching (RIE; SF₆) step removes the Si₃N₄ after transfer. The buried SiO₂ and top coating of PECVD SiO₂ physically isolate the devices from their surroundings, thereby enabling performance that is nearly independent of substrate or subsequent encapsulating material. This versatility is important, particularly in an area such as transient electronics where choices of constituent materials can be highly unusual compared to those with proven utility in conventional electronics. Figure 1c demonstrates that these types of MOSFETs can be fabricated and transferred over large areas, with high yields.

Figure 2 provides a set of images collected during dissolution of a system like that illustrated in Figure 1c, at various times after immersion in deionized (DI) water at room temperature. Here, the silk rapidly dissolves within two minutes,

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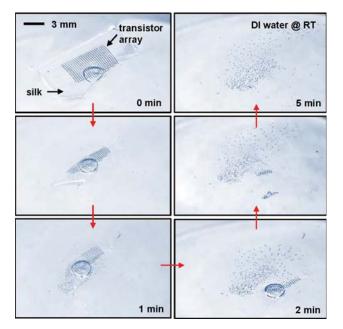


Figure 2. Optical images at various stages of disintegration and dissolution of an array of fully formed transient transistors on film of silk. These n-channel MOSFETs have total thicknesses of <2 μ m, including a base layer of thermal SiO₂ (~1 μ m), and use Mg for the electrodes, SiO₂ for the gate dielectric and Si for the semiconductor. This process of dissolution occurs in DI water at room temperature.

thereby leading to disintegration of the array into individual devices. The rate of dissolution of silk can be controlled over a wide range.^[18,19] Each component then gradually disappears in a manner defined by the dissolution rates of the various constituent materials.^[16] Hydrolysis consumes the Mg in several hours (Mg + 2H₂O \rightarrow Mg(OH)₂ + H₂). Dissolution of PECVD SiO₂ and Si in PBS solution (pH 7.4) at room temperature occurs on a timescale of weeks (SiO₂ + 2H₂O \rightarrow Si(OH)₄; Si + 4H₂O \rightarrow Si(OH)₄ + 2H₂); the thermal oxide takes considerably longer. In all of the materials, the rates for complete disappearance depend strongly on temperature, pH, layer thicknesses and morphology.

The overall fabrication process accommodates not only individual MOSFETs, but also logic gates and small-scale integrated circuits. Figure 3a shows an array of inverters, with a magnified optical micrograph and a circuit diagram. Each inverter consists of a load and an input transistor with channel lengths and widths of $\approx 20 \ \mu m$ and $\approx 10 \ \mu m$, and $\approx 10 \ \mu m$ and \approx 40 µm, respectively. The fabrication procedures (Figure 3b) are similar to those described previously, including device isolation (top left), metallization (Mg evaporation, top middle), trench etching (bottom left), anisotropic undercut release (bottom right). A scanning electron microscope (SEM) image and a top view optical microscopy image appear in the bottom middle and top right frames, respectively. Supporting Information Figure S3 summarizes additional details. Electrical measurements on typical n-channel MOSFETs (channel length and width, $L_{ch} = \approx 10 \ \mu m, W = \approx 40 \ \mu m$) indicate on/off ratios of > $\approx 10^5$, saturation and linear regime mobilities of $\approx 530 \text{ cm}^2/\text{V}$ s and $\approx 650 \text{ cm}^2/\text{V}$ s, respectively (Figure 3c). Current-voltage



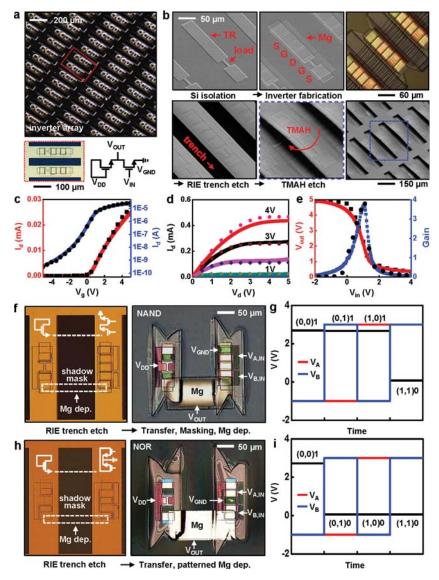


Figure 3. Fabrication of arrays of transient inverters and logic gates and their electrical properties. a) Image of an array of inverters, optical microscope image of a representative device (lower left) and circuit diagram (lower right). b) SEM and optical microscope images of key steps in the fabrication sequence. Device isolation (upper left), metallization (upper middle), RIE trench etch (lower left), anisotropic undercut etch with TMAH (upper right, lower right), and magnified image (lower middle). c) Linear (red) and log scale (blue) transfer curves of an n-channel MOSFET (channel length (L_{ch}) and width (W) are 10 μ m and 40 μ m, respectively). The mobility and on/off ratio are $650 \text{ cm}^2/\text{V}$ s, and $>10^5$, respectively. Experimental results (lines) and simulations (dots). d) I-V characteristics of an n-channel MOSFET. e) Output voltage characteristics and voltage gain of an inverter (L_{ch} and W are 20 μ m and 10 μ m for load transistor and 10 μ m and 40 μ m for input transistor, respectively). The peak gain is ≈4. f) Demonstration of a pair of n-channel MOSFETs in a logic gate (NAND) formed by interconnection with Mg. When one or both of the input transistors (at V_A or V_B) are in their off state, the associated resistance of the input exceeds that of the load transistor, thereby leading to an output voltage in the "1" state. When the input transistors are turned on, the output voltage reaches the "0" state. Images after RIE trench etch (left) and after transfer and interconnection on a silk substrate (right). Circuit diagrams appear in the top regions of the images on the left. g) Output voltage characteristics of logic gates (NAND) at V_{DD} = 3 V. V_A and V_B represent input voltages. h) Images of a NOR circuit after RIE trench etching (left) and interconnection with Mg via deposition through a shadow mask after transfer printing a pair of n-channel transistors onto a silk substrate (right). The configuration of a NOR gate is similar to a NAND gate except for the connection of the input transistors. Here, parallel connection of the input transistors leads to an output state of "0", when either input is turned on. The output voltage can reach the "1" state only when both input transistors are turned off. i) Output voltage characteristics of NOR circuits at a supply voltage of 3 V (V_{DD}), with input voltages of V_A and V_B .



characteristics evaluated at different gate biases are shown in Figure 3d. Voltage transfer characteristics (VTC) of the inverters (Figure 3e) are consistent with expected behaviors, and gains of up to ≈ 4 at supply voltages of ≈ 5 V when the input voltage is swept from -2 V to 4 V (measured values (lines) and simulations (dots)). Behaviors in the transistors and circuits were verified by SPICE (Simulation Program with Integrated Circuit Emphasis) simulation. Here, the devices were modeled using a combination of parameters, such as channel width and length, gate oxide capacitance, carrier mobility, and channel length modulation, that yielded a good match with the measurements. The circuits were simulated based on the resulting device models. The observed electrical properties are comparable to those of devices reported previously, fabricated in a similar manner with conventional, nontransient materials.^[20] Circuit components with increased sophistication are possible either through extended processing on the wafer, or through the use of interconnect structures formed after transfer printing. See Supporting Information Figure S4 for fabrication details. Examples of NAND and NOR gates appear in Figure 3f and 3h, respectively. Figure 3g,i show output voltage characteristics of NAND and NOR circuits. $V_{\rm A}$ and $V_{\rm B}$ are the input voltages. In case of the NAND gate, the output voltage assumes the "0" state when both input transistors are turned on. Output voltages for the "0" state and "1" state are ≈ 0.07 V and ≈ 2.67 V, respectively. For the NOR gate, output voltages reach the "1" state when both input voltages are low. Output voltages for the "0" state and the "1"state are ≈ 0.06 V and ≈ 2.7 V, respectively.

Inverters left in a released state on the SOI wafer allow for close examination of the dissolution processes. The image and schematic illustration in Figure 4 provide detailed information on the device structure and material components: Mg (≈200 nm) for the electrodes, Si (≈100 nm) for the active layer, and SiO_2 (≈ 100 nm) for the gate and interlayer dielectrics. Upon immersion in phosphate buffered saline (PBS, pH 7.4, Sigma-Aldrich, USA) solution at physiological temperature (37 °C), the various components of the device begin to dissolve, beginning with Mg, which undergoes reactive dissolution (i.e., hydrolysis) to Mg(OH)₂ during the first 10 h. Although PECVD SiO₂ (≈100 nm, interlayer dielectrics) encapsulates most of the Mg electrodes, after the exposed Mg at the contacts (source, drain, and gate) dissolves, the solution is able to undercut the Mg that lies



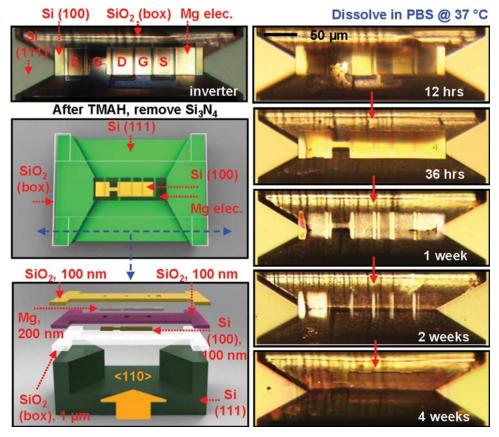


Figure 4. Schematic illustrations and time sequence of optical micrographs during dissolution of a transient inverter undercut etched but tethered at its ends to a Si wafer substrate, at various times of immersion in a phosphate buffered saline (PBS) solution at physiological temperature (37 °C) and pH (\approx 7.4). The frames in the middle and lower left provide schematic exploded view illustrations. The constituent materials include Si (100) with a thickness of \approx 100 nm for the semiconductor, Mg (\approx 200 nm) for the electrodes, and SiO₂ (\approx 100 nm) for the gate and interlayer dielectric.

beneath the SiO₂. This etching induces cracks in the SiO₂ that start from the edges and propagate to the center regions. This type of disintegration accelerates the overall rate of disappearance of the PECVD SiO2. After these top two layers mostly disappear, the SiO₂ gate dielectric (≈100 nm) begins to dissolve, reaching completion in two weeks or so. Over the next several weeks, the Si dissolves to form Si(OH)₄, with completion of this process in under 4 weeks. Consistent with previous reports of conventional acqueous etching approaches for silicon,^[21] the detailed rates can depend strongly on dopant type and concentration, on temperature, and on composition of the bath. The results shown here are for silicon derived directly from the SOI substrates, without additional doping. After disappearance of silicon, only the thermally grown buried oxide ($\approx 1 \, \mu m$) remains, with dissolution rates that are many times slower than any of the other materials. A similar time sequence of images of interconnected arrays of logic gates on silk substrate appears in Supporting Information Figure S5.

Control over the kinetics of this transience behavior, and in particular of the effects on electrical properties, is an important aspect of any practical design. The most straightforward strategies involve patterned or uniform encapsulation layers, with thicknesses and compositions selected to define desired timescales for penetration of solution into the active regions. **Figure 5** shows, as an example, changes in electrical characteristics of MOSFETs and inverters encapsulated by MgO (≈800 nm) as a function of time of immersion in DI water at room temperature. The measured transfer curves (at a drain voltage $V_d = 0.1$ V) and drain currents ($V_d = 0.1$ V, and at a gate voltage $V_g = 5$ V) in Figure 5a indicate that the device properties are stable (i.e., time invariant) for the first ≈ 8 h before they degrade quickly over the next ≈45 min. The calculated mobility appears in Supporting Information Figure S6. A typical inverter, with key characteristics summarized in Figure 5b, shows similar behavior: stable properties for the first ≈7 h followed by rapid degradation within ≈50 min. Both cases exhibit two different stages in the transient behavior: i) stable operation for a time defined by removal of the transient encapsulation layer and ii) functional degradation with a timescale set by dissolution of the transient active materials. Tuning and programming of transience behavior using this strategy and more complex variants of it provide many options in design.^[16]

Animal studies to examine biocompatibility were conducted by implanting a representative device in a Balb/c mouse in accordance with institutional IACUC-approved protocols as shown in **Figure 6**. In this example, the implant consisted of an array of resorbable transistors fabricated on a \approx 5 mm × 5 mm silk film, sterilized by ethylene oxide and then inserted subcutaneously through an incision on the back of the mouse (Figure 6a, left). Here, the silk was treated in a manner that FULL PAPER

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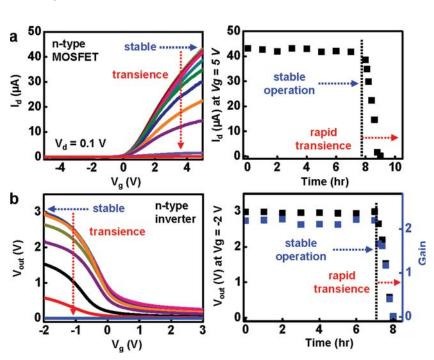


Figure 5. Study of the change in electrical properties of transient devices measured at various times during dissolution. a) Electrical properties of a representative n-type MOSFET encapsulated with MgO (\approx 800 nm) measured at various times during immersion in DI water at room temperature. The linear scale transfer curves (left), and the drain current (V_d = 0.1 V, V_g = 5 V) show that the properties are invariant for \approx 8 h. Afterward, the performance degrades completely within \approx 1 h. b) Measured characteristics of an n-channel inverter encapsulated with MgO (\approx 800 nm) at different times in DI water at room temperature. Voltage transfer characteristics (left), and output voltages at V_g = -2 V and gain (right) measured during dissolution. The device operation is stable for \approx 7 h, followed by rapid degradation in \approx 50 min.

leads to slow dissolution, thereby facilitating examination of the charcteristics of device resorption. The end of the functional life of the system is defined by disappearance of the encapsulation layer and/or substrate. After two weeks, the implanted sample (Figure 6a, right) was found to be nicely integrated into the surrounding tissues with no signs of magnesium or silicon. The device was retrieved and the surrounding tissue was extracted to determine the inflammatory response. Histological examination of the tissue surrounding the implant site revealed the absence of any severe inflammatory response, indicating that the implanted devices induced no significant adverse effects to the animal (Figure 6b).



Figure 6. In vivo evaluation of biocompatibility. a) Image of the subcutaneous implantation of a representative device, consisting of an array of transistors on a sheet of silk, in the dorsal region of a BALB/c mouse. b) Image of the implant site after 2 weeks, showing that the implant integrated into the surrounding tissues with no signs of the transistors. c) Histological examination of the tissue surrounding the implant site reveals no inflammatory response.



3. Conclusions

The concepts, materials and fabrication techniques reported here provide a wafer-based approach to transient electronics, in which a set of foundry-compatible processing steps creates arrays of transistors, logic gates and potentially other components made of transient materials on a host wafer. The resulting device configurations are well suited for transfer printing onto transient substrates. Various examples illustrate the feasibility of this approach, and the levels of performance that can be achieved. These ideas have the potential to accelerate the translation of biodegradable electronic implants and other classes of devices enabled by transient circuits, sensors and/or actuators, into realistic, practical technologies. Different applications demand different functional lifetimes. The wide range of relevant timescales creates many opportunities for future work on materials, devices and packaging designs.

4. Experimental Section

Wafer-Based Fabrication of Fully Formed Transient Electronic Devices: The fabrication began with custom silicon-on-insulator (SOI, Silicon Quest Inc., USA) wafers with a top silicon (100) layer ($\approx 2 \mu m$ thick, p-type 10–20 $\Omega \cdot cm$), a buried layer of silicon dioxide ($\approx 1 \mu m$ thick) and a Si (111)

supporting substrate. Repetitive cycles of dry oxidation at 1100 °C followed by wet chemical etching in hydrofluoric acid reduced the thickness of the top silicon layer to \approx 100 nm. Patterned doping with phosphorous at \approx 950 °C using a spin-on dopant (SOD, Filmtronics, USA) defined regions for source and drain contacts. Isolated areas of silicon were defined by patterned reactive ion etching (RIE; Plasmatherm, USA) with sulfur hexafluoride (SF₆) gas for \approx 1 min. A thin layer of SiO₂ (100 nm) deposited by plasma-enhanced chemical vapor deposition (PECVD) served as the gate dielectric. Patterned wet-etching of this layer with buffered oxide etchant (BOE, 6:1, Transcene company, USA) opened windows for source and drain contacts. Photolithography and liftoff formed Mg electrodes (\approx 200 nm) for source, drain and gate contacts. An additional layer of PECVD SiO₂ (100 nm) served as an encapsulant, with openings to the contacts formed by immersion in BOE. A 400 nm thick,

unpatterned layer of Si₃N₄ deposited by PECVD passivated the entire area of the devices. A bilayer of Cr/Au (10/150 nm) deposited by electron beam evaporation provided a hard mask for deep trench etching by RIE down to the underlying Si (111) wafer through the buried oxide. These processed substrates were then submerged in tetramethyl ammonium hydroxide (TMAH, 25 wt% in H_2O , Sigma-Aldrich, USA) for ≈30 min at 100 °C for anisotropic undercut etching of the wafer. Removal of the metal hard mask followed this etching. Next, the devices were transfer printed to a spin cast film of silk, and the passivation layer of Si₃N₄ was removed by RIE. In the case of logic gates, such as NAND and NOR gates, interconnection traces of Mg were deposited through fine-line stencil masks (Kapton, 12.5 μm, Dupont, USA).



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Dissolution Experiments: To observe dissolution of the constituent materials (Si, SiO₂ and Mg), a collection of undercut etched inverters on SOI were immersed in phosphate buffered saline (PBS, pH 7.4, Sigma-aldrich, USA) solution at 37 °C. Optical microscope images revealed the various stages of dissolution over the course of 4 weeks. Most of the Mg electrodes (≈200nm) react with water to form Mg(OH)₂ within 12 h; any residual remaining Mg dissappeared completely in 36 h. The exposed regions of Mg dissolved first, followed by undercut dissolution of those regions of Mg that lie beneath PECVD SiO₂. Simultaneously, the SiO₂ (\approx 100nm, interlayer dielectrics) also began to dissolve to form Si(OH)4. Due to the elimination of the underlying Mg, much of this SiO₂ disintegrated into tiny pieces (not visible directly), thereby accelerating the elimination of this layer. The SiO₂ (\approx 100 nm) that forms the gate dielectric disappeared in 2 weeks. Partial dissolution of the Si occurred at the same time. Dissapearance of all materials except for the buried oxide (SiO₂, 1 μ m) was complete within 4 weeks. Previous studies indicate that oxides grown at high temperatures have slow dissolution rates due to their morphology/ density.^[22]

Monitoring of electrical properties during dissolution was performed using transistors and inverters encapsulated by a uniform layer of MgO (800 nm). These devices were completely immersed in DI water, but configured with external probing pads to enable continuous mesurement. Experimental results illustrate two-stage dissolution kinetics: stable device operation, without changes in electrical characteristics, followed by comparatively fast degradation in key performance parameters. The duration of the first stage depends on the rate of dissolution of the encapsulation materials and/or penetration of water through them. The second stage is determined, primarily, by relatively fast dissolution of the Mg electrodes.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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