REPORT DOCUMENTATION PAGE

2

Form Approved OMB NO. 0704-0188

1. REPORT DATE (DD-MM-YYYY)	2. REPORT TYPE	3. DATES COVERED (From - To)
15-09-2014	Final Report	2-Aug-2010 - 1-Aug-2013

4. TITLE AND SUBTITLE
Final Report: Oxide Based Transistors for Flexible Displays

5a. CONTRACT NUMBER
W911NF-10-1-0316

5b. GRANT NUMBER

5c. PROGRAM ELEMENT NUMBER
611104

6. AUTHORS
Shanthi Iyer and Jay Lewis

5d. PROJECT NUMBER

5e. TASK NUMBER

5f. WORK UNIT NUMBER

7. PERFORMING ORGANIZATION NAMES AND ADDRESSES
North Carolina A&T State University
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Greensboro, NC 27411 -0001

8. PERFORMING ORGANIZATION REPORT NUMBER

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS (ES)
U.S. Army Research Office
P.O. Box 12211
Research Triangle Park, NC 27709-2211

10. SPONSOR/MONITOR'S ACRONYM(S)
ARO

11. SPONSOR/MONITOR'S REPORT NUMBER(S)
57900-EL-H.10

12. DISTRIBUTION AVAILIBILITY STATEMENT
Approved for Public Release; Distribution Unlimited

13. SUPPLEMENTARY NOTES
The views, opinions and/or findings contained in this report are those of the author(s) and should not contrued as an official Department of the Army position, policy or decision, unless so designated by other documentation.

14. ABSTRACT
The team of NC A&T and RTI, International investigated In free GaSnZnO (GSZO) material system, as the active channel in thin film transistors (TFTs) for next generation display technologies. A detailed and comprehensive study was carried out to ascertain the process-property relationships of radio frequency (RF) sputtered GSZO films as a function of number of deposition parameters, including deposition temperature, process pressure and annealing temperature, duration and ambient using variety of characterization techniques for chemical and microstructural properties, electrical and opto-electrical properties. The impact of process conditions on the device performance

15. SUBJECT TERMS
Thin film transistors, flexible electronics, RF sputtering, Transparent amorphous oxide semiconductors, GSZO, Rutherford backscattering, XRR, XPS, XRD, I-V, C-V, flexible electronics, plastic substrates

16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT	15. NUMBER OF PAGES	19a. NAME OF RESPONSIBLE PERSON
a. REPORT	b. ABSTRACT	c. THIS PAGE			Shanthi Iyer
UU	UU	UU	UU		19b. TELEPHONE NUMBER: 336-285-3710

Report Title

Final Report: Oxide Based Transistors for Flexible Displays

ABSTRACT

The team of NC A&T and RTI, International investigated In free GaSnZnO (GSZO) material system, as the active channel in thin film transistors (TFTs) for next generation display technologies. A detailed and comprehensive study was carried out to ascertain the process-property relationships of radio frequency (RF) sputtered GSZO films as a function of number of deposition parameters, including deposition temperature, process pressure and annealing temperature, duration and ambient using variety of characterization techniques for chemical and microstructural properties, electrical and opto-electrical properties. The impact of process conditions on the device performance was also subject of detailed study. Two sets of TFTs were examined in detail- one set corresponding to higher annealing temperature of 450 oC and the other processed at temperatures compatible with low temperature polymer substrates. Electrical and optical stability was also examined in detail. Bottom-gate GSZO TFTs have been demonstrated on PEN substrates which we believe to be the first reported on these films. Overall we have shown that GSZO is an excellent candidate for the replacement of IGZO films.

Enter List of papers submitted or published that acknowledge ARO support from the start of the project to the date of this printing. List the papers, including journal references, in the following categories:

(a) Papers published in peer-reviewed journals (N/A for none)

Received Paper

TOTAL:

Number of Papers published in peer-reviewed journals:

(b) Papers published in non-peer-reviewed journals (N/A for none)

Received Paper

TOTAL:

Number of Papers published in non peer-reviewed journals: 4

(c) Presentations

Robert Alston, Jay Lewis, Garry B. Cunningham and Shanthi Iyer," The Study of Low Temperature Nano-Scale Transistors Fabricated on Silicon and PEN substrates", MRS/ASM/AVS/AReMS Meeting 2013,Raleigh,NC

Briana McCall, Ngoc Nguyen, Robert Alston, Jia Li and Shanthi Iyer, " Improved characteristics & Bias Stress Stability of GSZO Thin Film Transistors on Annealing", MRS/ASM/AVS/AReMS Joint Symposium at NCSU. November 15 2013.

Briana McCall, Ngoc Nguyen, Robert Alston, Jia Li and Shanthi Iyer. Improved characteristics & Bias Stress Stability of GSZO Thin Film Transistors on Annealing. NanoManufacturing 2013 Conference, JSNN, September 25 2013

Robert Alston, Jay Lewis, Garry B. Cunningham, and Shanthi Iyer, "The Study of Low Temperature Nano-Scale Transistors Fabricated on Silicon and PEN substrates", NanoManufacturing 2013 Conference, JSNN, September 25 2013

Robert Alston and Shanthi Iyer," The Study of Low Temperature Nanoscale Transistors Fabricated on Silicon and PEN Substrates" NCA&TSU College of Engineering Poster Presentation, April 25, 2013.

Tewodros Tessema, Robert Alston, "The Study of RF Sputtered Gallium Tin Zinc Oxide Based Thin Film Transistors", Materials Research Society Conference North Carolina Section, November 16th 2012, Raleigh NC, Oral presentation.

Number of Presentations: 6.00

Non Peer-Reviewed Conference Proceeding publications (other than abstracts):

Received	Paper	
09/05/2014	9.00	Robert Alston, Shanthi Iyer , Tanina Bradley , Jay Lewis , Garry Cunningham, Eric Forsythe. Investigation of the effects of deposition parameters on indium-free transparent amorphous oxide semiconductor thin-film transistors fabricated at low temperatures for flexible electronic applications , SPIE conference. 25-FEB-14, . : ,
09/19/2013	6.00	Tanina Bradley, Shanthi Iyer, Robert Alston, Ward Collis, Jay Lewis, Garry Cunningham, Eric Forsythe. The effects of deposition conditions and annealing temperature onthe performance of gallium tin zinc oxide thin film transistors , The International Society for Optical Engineering (SPIE). 05-FEB-13, . : ,
TOTAL:	**2**	

Number of Non Peer-Reviewed Conference Proceeding publications (other than abstracts):

Peer-Reviewed Conference Proceeding publications (other than abstracts):

Received	Paper

TOTAL:

Number of Peer-Reviewed Conference Proceeding publications (other than abstracts):

(d) Manuscripts

Received		Paper
02/22/2013	4.00	Tanina Bradley, Shanthi Iyer, Robert Alston, Ward Collis, Jay Lewis, Garry Cunningham, Eric Forsythe. The effects of deposition conditions and annealing temperature on the performance of GSZO TFTs, SUBMITTED TO SPIE PHOTONICS WEST 2013 (02 2013)
09/27/2012	3.00	Tanina Bradley, Robert Alston, Jay Lewis, Garry Cunningham, Eric Forsythe, Shanthi Iyer. The Influence of Oxygen on Gallium Tin Zinc Oxide Thin Film Transistor Performance and Stability, ACS Applied Materials and Interfaces (09 2012)
TOTAL:		**2**

Number of Manuscripts:

Books

Received	Book

TOTAL:

Received	Book Chapter

TOTAL:

Patents Submitted

Patents Awarded

Awards

Graduate Students

NAME	PERCENT_SUPPORTED	Discipline
Robert Alston	0.00	
Briana McCall	0.30	
Ngoc Nguyen	1.00	
Olanrewaju Ogedengbe	0.30	
FTE Equivalent:	**1.60**	
Total Number:	**4**	

Names of Post Doctorates

NAME	PERCENT_SUPPORTED
Jia Li	0.00
FTE Equivalent:	**0.00**
Total Number:	**1**

Names of Faculty Supported

NAME	PERCENT_SUPPORTED	National Academy Member
Shanthi Iyer	0.40	
FTE Equivalent:	**0.40**	
Total Number:	**1**	

Names of Under Graduate students supported

NAME	PERCENT_SUPPORTED	Discipline
Ashkan Ghattan	0.20	Electrical and Computer Engineering
Matthew Hill	0.20	Electrical and Computer Engineering
Abid Bhatti	0.20	Electrical and Computer Engineering
Tewadros Tessema	0.30	Electrical and Computer Engineering
FTE Equivalent:	**0.90**	
Total Number:	**4**	

Student Metrics

This section only applies to graduating undergraduates supported by this agreement in this reporting period

The number of undergraduates funded by this agreement who graduated during this period:	2.00
The number of undergraduates funded by this agreement who graduated during this period with a degree in science, mathematics, engineering, or technology fields:.....	2.00
The number of undergraduates funded by your agreement who graduated during this period and will continue to pursue a graduate or Ph.D. degree in science, mathematics, engineering, or technology fields:.....	1.00
Number of graduating undergraduates who achieved a 3.5 GPA to 4.0 (4.0 max scale):.....	0.00
Number of graduating undergraduates funded by a DoD funded Center of Excellence grant for Education, Research and Engineering:.....	0.00
The number of undergraduates funded by your agreement who graduated during this period and intend to work for the Department of Defense	0.00
The number of undergraduates funded by your agreement who graduated during this period and will receive scholarships or fellowships for further studies in science, mathematics, engineering or technology fields:	1.00

Names of Personnel receiving masters degrees

NAME	
Briana McCall	
Olanrewaju Ogedengbe	
Total Number:	**2**

Names of personnel receiving PHDs

NAME	
Robert Alston	
Tanina Bradley	
Total Number:	**2**

Names of other research staff

NAME	PERCENT_SUPPORTED
FTE Equivalent:	
Total Number:	

Sub Contractors (DD882)

Inventions (DD882)

Scientific Progress

Technology Transfer

FINAL REPORT

to

ARMY RESEARCH OFFICE

Oxide Based Transistor for Flexible Displays

Grant No: W911NF-10-1-0316

Period: 08/02/10- 07/31/13

Program Manager: Michael Gerhold

Shanthi Iyer, Principal Investigator

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TABLE OF CONTENTS

Oxide Based Transistor for Flexible Displays

Grant No: W911NF-04-2-0051

This is the final technical report describing the research activities of the Battlefield Center of Excellence Center. The focus of the Center was to develop and demonstrate novel materials, both for device structures that advance the state-of-the-art in flexible electronics, as well as for environmentally stable, high-performance, hybrid organic/inorganic semiconductor, robust luminescent devices for flexible displays for the U.S. soldier.

There were two major research components to the Center. The first component constituted the detailed and comprehensive investigation of (a) Gallium tin zinc oxide (GSZO) based transparent amorphous oxide thin film transistors (TAO-TFTs) with processing temperatures below 150 ^{o}C compliant with flexible electronics applications, (c) GSZO TFTS annealed at 450 ^{o}C with performance close to that of IGZO based TFTs and (d) electrical and optical device stability. The primary goals of this effort were improved performance and stability, compared to conventional IGZO based TFTs. This work was carried out at NCA&TSU.

The second component of the research effort pertained to bottom gate configuration on the polyethylene naphthalate substrate. This component encompassed a highly collaborative effort of two institutions: NCA&TSU (**Iyer's group**) as lead and Research Triangle Institute International (RTI Int'l) investigators (**Jay Lewis, Garry Cunningham** and **Christopher Gregory**), and **Eric Forsythe** from Army Research Laboratory served on the most of the student's thesis/ dissertation. **Eric Forsythe's** valuable insight into the project allowed rapid progress in the project.

Student training, educational component, technology transition from RTI International to NCA&TSU and infrastructure development at NCA&TSU were the other major goal of this collaborative research. This funding was leveraged to get additional funding from the State funds allocated by the Departments for research activities as well as the Department of Education (DOE) through the Title III program for students support, student travel to conferences, equipment and characterization service fees.

A brief list of summary of accomplishments achieved every year is provided in the beginning of the report. The technical progress is also delineated into the yearly progress. Both of them have the student training, educational component imbedded.

I. Summary of Accomplishments

Year 1

- Transfer lengths measurements for different metal contacts on Gallium tin zinc oxide (GSZO) films. The ebeam evaporated metal contact films investigated were Al (100nm), Ti (20nm)/Al (30 nm)/Au (100nm), Al (30nm)/ Au (50nm) and Al (30nm)/ Pt (50nm). The effect of post deposition annealing duration on the electrical property of the contacts was also studied. Al (100 nm) provides the best resistivity in the shortest annealing period. Results show that Al has contact resistivity of 84 Ω-cm^2 for contact pad size of 500 x 500 μm^2 for consecutive post deposition annealing at 250^{o}C in N_2 ambient of 25 minutes.
- Effects of varying oxygen partial pressure on rf sputtered GSZO films of 30 nm deposited at both room temperature (RT) and at elevated temperatures (ET) and its impact on the TFT devices fabricated on Si was studied. X-ray photoelectron spectroscopy (XPS) analysis was performed to determine the surface composition of the channel layer and was correlated to the surface properties to the resulting TFT device performance.
- Depletion mode TFTs were produced with drain current (I_D) = 10^{-6} A, threshold voltage (V_T)= -3 V, sub threshold swing (SS)= 1.3 V/decade, and on/off current ratio ($I_{on/off}$)= 10^6 when operated in the dark without gate stress. TFTs with 9% oxygen incorporation during deposited and post-deposition annealing at 250 °C exhibits the best performance amongst enhancement mode devices with I_D of 10^{-7}A, V_T of 3V SS of 1.3 V / decade, and $I_{ON/OFF}$ of 10^6 In addition, a stable RT deposited TFT has been achieved with 2 % oxygen incorporation, and 250 °C post deposition annealing temperature, that exhibits a ΔV_T as low as ~0.5 V for a 3 hour stress period under a gate bias of 1.2 and 12 V.
- Different masks were designed by RTI for TFT production on polyethylene napthlate (PEN) substrates. Three different dielectric stacks of 250nm thick SiOx, 200nm SiOx+50nm SiNx and 200nm SiOx+50nm Parylene were deposited by low temperature plasma enhanced chemical vapor deposition (PECVD). Evaporated chromium served as gate contact. The first set of GSZO films deposited on this exhibited poor performance attributed to the roughness of the PEN substrate.
- Shereen Farhana: completed her Master thesis on transfer length measurements.

Year 2

- Capacitance-voltage (C-V) characterization was set up. Comparisons between GSZO TFT on Si for different contacts, deposition temperature, and post annealing temperature and duration were made and were compared to their output and input I-V device characteristics. Detailed analysis was made to get quantitative information on the interface state density and contact resistance. Demonstrated C-V to be a simple and powerful tool to get rapid insight into the performance of the TFT and to compliment the information provided by the I-V characteristics.
- The goal of the second iteration of the devices fabricated on PEN substrates was the deposition of two different planarization layers: spin-on polarization layer Su-8 and 1 um thick PECVD deposited oxide layer. PECVD layers of SiOx and SiNx were served as the dielectric was chosen as the CVD deposited planarization layer. Patterned Cr metal

contact served as the gate contact. This task was carried out by RTI International Inc. No TFTs were fabricated.

- Tanina Bradley (minority female student): Completed Ph.D. dissertation on GSZO TFT.

Year 3 and Beyond

- The trap density and its energetic distribution, and oxygen chemisorption were found to play a critical role in determining the operational characteristics of the TFT device, all of which can be controlled by the oxygen incorporation and substrate temperature during deposition, along with the post-deposition annealing. This work resulted in publication in **SPIE proc. 2013.**
- A comprehensive and detailed study on the performance of GSZO TFTs has been carried out by studying the effects of processing parameters such as deposition temperature and annealing temperature/duration, as well as the channel thickness **with all temperatures held below 150 °C**, with potential applications on flexible substrates. Variety of characterization techniques, namely Rutherford backscattering (RBS), x-ray photoelectron spectroscopy (XPS) and x-ray reflectivity (XRR) in addition to I-V and C-V measurements were employed to determine the effects of the above parameters on the composition and quality of the channel. Optimized TFT characteristics of I_D=3x10^{-7} A, ION/OFF =2x10^6, V_{ON} ~ -2 V, SS ~ 1 V/dec and µFE = 0.14 cm^2/V• s with a ΔV_{ON} of 3.3 V under 3 hours electrical stress were produced. This work resulted in publication in **SPIE Proc 2014**.
- Lower temperature processed (~150^{o}C) GSZO TFTs are strongly influenced by deposition parameters unlike the higher temperature annealed films. The oxygen deficient deposited films led to porous films, with high electron trap density, shallow oxygen vacancies and Zn interstitial states. The oxygen rich ambient deposition on the other hand led to smooth surface and interfaces with dense films with Sn in the desired Sn^{4+} state. However, these are dominated by deep filled states. The electrical and optical stability was also found to be sensitive to these deposition conditions.
- A systematic and detailed study on the electrical and optical stability of these TFTs as a function of annealing temperature, deposition pressure, film thickness and oxide thickness was carried out to gain better insight into the degradation mechanism of these transistors as well as to correlate to the initial performance of the device. Annealing does not alter the composition of the channel but anneals out the point defects such as oxygen vacancies leading to change in the Sn valence from Sn2+ to Sn4+. In addition the surface and interface roughness is also reduced. These manifest in significant reduction in the light induced sub-band states as well, in particular, the shallow and deep states with much better electrical and optical stability for higher temperature annealed devices at 450C. The low temperature annealed device at 140°C appears to be influenced by the deposition pressure. However, density of VB tail states are still large enough in both cases to significantly contribute to the degradation of these devices under 410nm and negative bias induced stress (NBIS).
- Bottom-gate **GSZO TFTs have been demonstrated on PEN substrates** which we believe **to be the first reported on these films**. Devices with planarization su-8 layer showed

improvement in device performance when compared to devices without the su-8 layer likely the result of smoother gate oxide surface roughness. An $I_{ON/OFF}$ ~10^5, SS~0.7 V/dec and μ_{FE}~0.7 $cm^2/V{\cdot}s$ was achieved with the indium-free TAOS GSZO TFT on PEN.

- Increased in the annealing temperature from 140 °C to 450 °C showed a drastic improvement in the overall electrical performance due to lower density defects in both shallow and deep type, resulting in higher quality film with better semiconductor/insulator interface along with a higher density of Sn^{4+}.
- Reduction in the active layer thickness from 15 to 8 nm resulted in significant improvement in performance with V_{ON} improving (-9 V – 1V), SS decreasing (0.91 V/dec – 0.3 V/dec) and I_{OFF} decreasing ($1.3x10^{-12}$ – $1.1x10^{-14}$ A). This is all indicative of a decrease in defect density with decreasing channel thickness borne out also by sharp transition from the depletion to accumulation region in the associated C-V data.
- Post oxygen annealing test have showed further improvement in the electrical characteristic with an increased in both ID and µFE and decreased in SS. However, V_{ON} shifts in the negative direction due to the increased charge resulting from reduction in the trap density.
- Deposition pressure, post deposition annealing, and metal contacts are the other parameters investigated and found to make marginal increase in the device performance. The best data that we have thus obtained is with V_{ON} is close to 0 V, $I_{ON/OFF} = 10^7$, with SS of 0.3 V/dec. corresponding to µFE 0f 0.9cm^2/Vsec. Higher $I_{ON/OFF}$ of 10^8 µFE 0f 5 cm^2/Vsec with almost one order of magnitude increase in I_D is achieved at the expense of V_{ON} shifting to large negative values.
- Robert Alston (minority student): Completed his Ph.D. dissertation on GSZO TFT on plastic substrates, Olanrewaju Ogedengbe completed Master thesis on C-V measurements of TFT, Briana McCall (minority female student) completed Master thesis on Stability of GSZO TFT.

Part II
Summary of Technical Progress

Year 1

1.1 Transfer Length Measurements for Different Metallization Options and Processing

Transfer length measurements for various metal contacts on GSZO films were performed to determine the specific contact resistivity. The investigated contacts were Al (100nm), Ti (20nm)/Al (30 nm)/Au (100nm) and Al (30nm)/ Au (50nm) and Al (30nm)/ Pt (50nm). These were deposited by electron beam evaporation. The contacts were annealed after metal deposition at 250^{o}C in N_2 ambient for different durations. The effects of post deposition annealing duration on the electrical property of the contacts have also been studied. This work has been detailed in **Shereen Farhana's** thesis[1].

Amongst the above contacts the best results were obtained on Al contact. In the following we present only the results of the best contact Al (100nm) for a specific contact pad size of 500 µm X 500 µm.

The total résistance vs. spacing between contact pads of the as-deposited sample is shown in Fig. 1.1.1. The total resistances values (10^7 Ω) are very high which leads to large transfer length of 1.4 x 10^4 µm. The contact, sheet and specific contact resistances are calculated as 5 x 10^6 Ω, 1.7 x 10^5 Ω/□ and 3.6 x10^5 Ω/ cm^2. After performing the post deposition annealing for 10 minutes in nitrogen ambient, the contact resistance value dropped down to

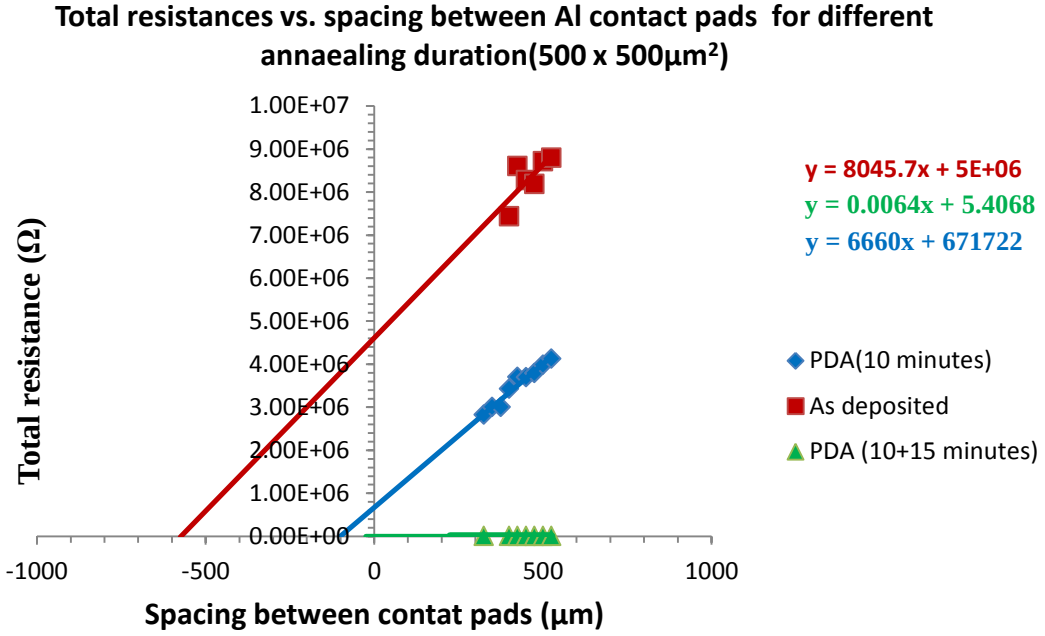

Figure 1.1.1: Comparisons of total resistances vs. spacing between contact pads (500 x 500 µm^2) of Al contact for different annealing duration.

2.5 x 10^6. The transfer length determined from the plot (Fig. 1.1.1) is 1.4 x 10^4 µm. The values of 3.2 x 10^6 Ω and 4.9 x 10^3 Ω-cm^2 are the sheet and contact resistivity, respectively. On further annealing the sample for 15 minutes in nitrogen ambient, led to the transfer length, contact resistance, sheet resistance and specific contact resistivity values of 50 µm, 3.4 x 10^5 Ω, 3.3 x 10^6 Ω/□, and 84 Ω-cm^2.The total resistances vs. spacing for different annealing duration are also summarized in Fig. 1.1.1. A comparison of specific contact resistances with respect to different annealing durations is shown in Fig 1.1.2. The specific contact resistivity is reduced with the increased annealing duration.

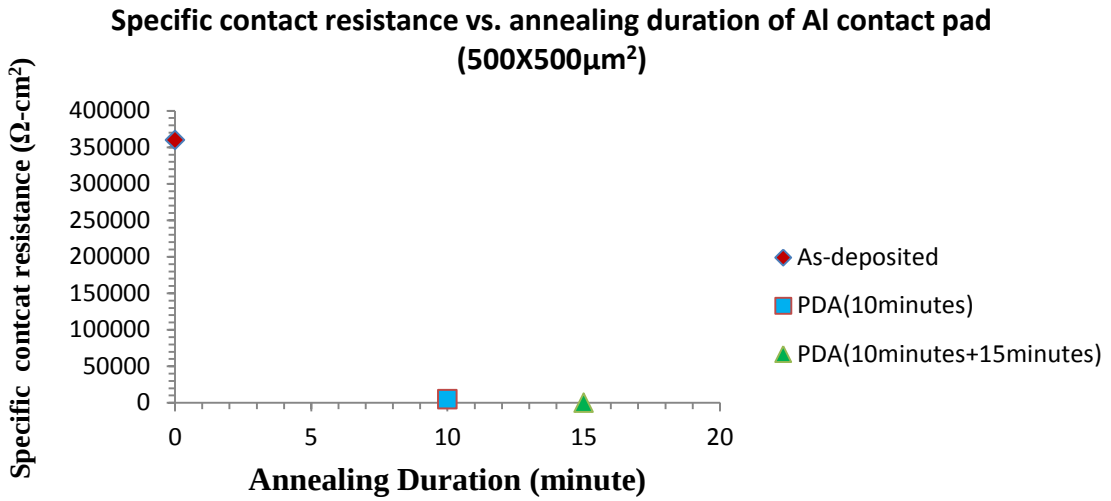

Figure 1.1.2: Specific contact resistance vs. annealing duration for Al (500 x 500µm^2) contact on GSZO film.

Although Ti/Al/Au contact also establishes improved specific contact resistivity of 68.6 Ω-cm^2 and resistivity is reduced with added post deposition annealing temperature, the trend was not consistent for other contact pad sizes (300 x 300 µm^2 and 1000 x 1000 µm^2). The Al (30 nm)/ Au(50nm) and Al (30nm)/Pt(50nm) contacts show very poor conductivity with high specific contact resistivity of 7.7 x 10^3 Ω-cm^2 and 1.6 x 10^3 Ω-cm^2 respectively. Thus Al appears to be the best contact for GSZO from the above studies not only from the electrical properties but also from simplicity as only a single element is involved for the contact.

1.2 The Effects of Deposition Conditions on the Performance of GSZO TFTs

GSZO films of 30 nm have been deposited by rf sputtering at both room temperature (RT) and at elevated temperature (ET) with varied oxygen partial pressures. Film properties were studied using x-ray diffraction (XRD) and transmission measurements to assess the structural and optical properties of the deposited films. X-ray photoelectron spectroscopy (XPS) analysis was performed to determine the surface composition of the channel layer, and correlate the surface properties to the resulting TFT device performance.

The films produced are amorphous within the temperature ranges of this investigation. Transparency typically above 80% in the visible region was observed for films with at least 2% oxygen in Ar ambient during deposition, with an optical band gap of approximately 3.1 eV. In this work the effects of deposition and post-deposition parameters on the film properties and interface traps were addressed. The film parameters' resultant effects on device performance and stability were also the subject of study with the use of various characterization techniques. All the data have been explained by delineating the O 1s XPS peak into two peaks, as shown in

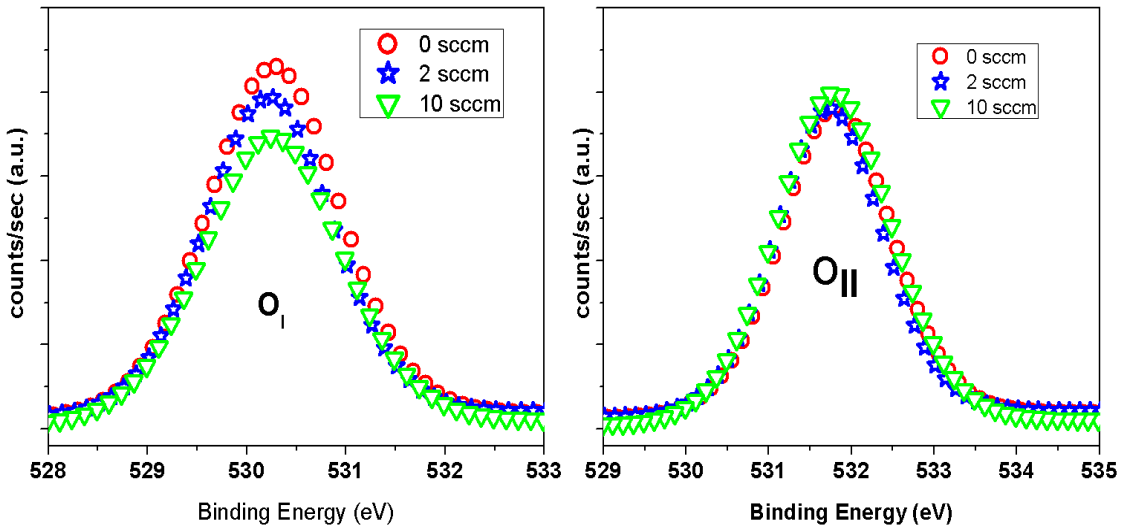

Figure 1.2.1: Gaussian fit of (a) OI and (b) OII contributors to the O_2 flow dependent O1s peak.

Figure 1.2.1, with the first one at lower binding energy attributed to the metal oxides and oxygen vacancies. The second peak at higher binding energy to chemisorbed species on the surface. The changes that were observed in O_2 flow as well as in the annealing temperature depend on the variation that occurs in the elemental atomic concentration of the films which is correlated to the variations in the oxygen vacancies through O_I peak. It is to be noted that zinc vacancies were also considered as a contributing factor in the variation of film composition, but was excluded after further investigation.

TFTs were fabricated with the transparent amorphous GSZO as the channel layer. These were fabricated on Si substrates to optimize performance prior to transferring device production on flexible substrates. The effects of oxygen incorporation on active layer properties and transistor performance were investigated. Both enhancement and depletion mode devices were fabricated. TFT performance was evaluated through the current-voltage (I-V) characteristics of the devices under normal, electrically stressed and photo-excited conditions operating conditions. Depletion mode TFTs were produced with drain current (I_D) = 10^{-6} A, threshold voltage (V_T)= -3 V, subthreshold swing (SS)= 1.3 V/decade, and on/off current ratio ($I_{on/off}$)= 10^6 when operated in the dark without gate stress. TFTs with 9% oxygen incorporation during deposited and post-deposition annealing at 250 °C exhibit the best performance amongst enhancement mode devices with I_D of 10^{-7}A, V_T of 3V SS of 1.3 V / decade, and $I_{on/off}$ of

10^6 (see Fig 1.2.2). In addition, a stable RT deposited TFT has been achieved with 2% oxygen incorporation, and 250°C post deposition annealing temperature, that exhibits a ΔV_T as low as ~0.5 V for a 3 hour stress period under a gate bias of 1.2 and 12 V.

The trap density, defect creation in the layer and oxygen chemisorption was found to play a critical role in determining the operational characteristics of the device, all which can be controlled by the oxygen incorporation and temperature during deposition, along with post-deposition annealing. We have shown[2,3] that in these devices by tailoring these parameters, the instabilities with respect to the electrical stress and optical illumination can be suitably

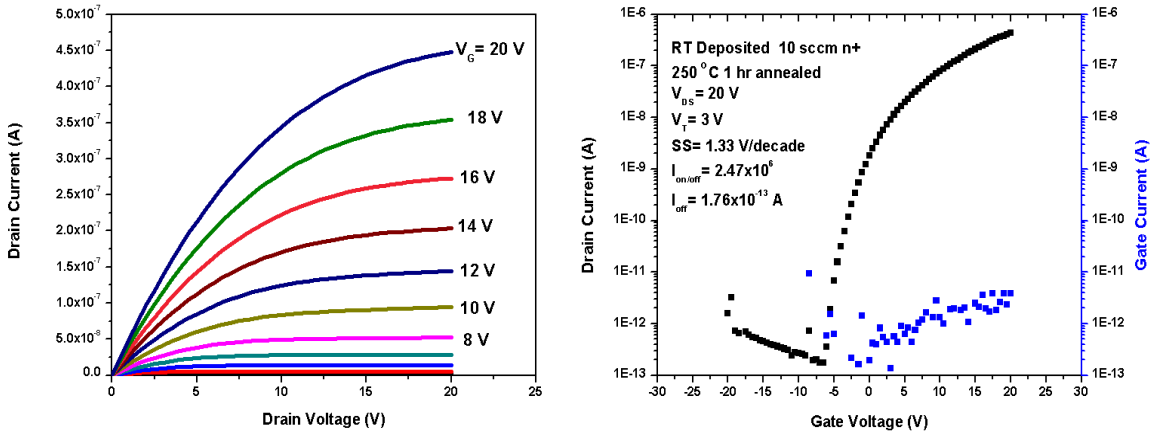

Figure 1.2.2: Input and output characteristics of GSZO TFTs on Si substrate for 10sccm oxygen flow.

suppressed. A stable RT deposited TFT has been achieved with 2% oxygen incorporation, and 250°C post deposition annealing temperature, that exhibits a ΔV_T as low as ~0.5 V for a 3hour stress period under a gate bias of 1.2 and 12 V. Mobility values are low ~0.1-0.7 cm^2/V-sec and are shown to increase with oxygen incorporation. All these have been detailed in Tanina Bradley's dissertation[2] and in the SPIE Proceedings 2013[3] published later.

It is to be noted all the above data are on the TFT which were air annealed. Different annealing ambient such as N_2+10%H_2 ambient were also used for two oxygen flows corresponding to 9% and 2% oxygen incorporation. The TFTs had a very low drain current of the order of 10^{-10} A (Fig. 1.2.3) and below, respectively.

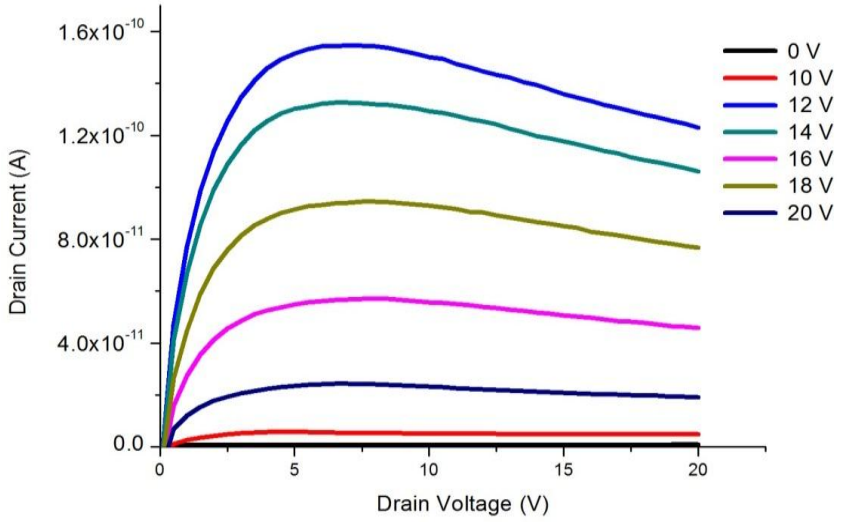

Figure 1.2.3: Output characteristics of SiO_2 oxide Si TFT deposited with O_2~2 SCCM and N_2+10%H_2 annealed.

The poor performance of the devices under this annealing N_2+10%H_2 is attributed to the H_2 atoms rapidly diffusing into the channel layer at the surface introducing high O vacancies, thereby making the channel highly conducting. This was further corroborated when the TFT operation ceased on annealing in H_2 ambient.

1.3 Thin Film Transistor Production on Plastic Substrates in collaboration with RTI Int'l

1.3a Device Layout at RTI Int'l

To fabricate a large number of TFTs on plastic using different process conditions while limiting the number of wafers required, a photomask was designed to enable chip-scale processing. The layout provides 12 full chips per wafer, as well as 4 additional chips that provide most of the functionality of a complete chip, as seen in Fig 1.3.1. At the chip scale, TFTs were designed using 8 different combinations of drain width/length, and each combination is repeated 5 times to provide statistical analysis, resulting in 40 devices per chip. The chip scale layout is shown in Fig 1.3.2. At the device scale, the first mask is designed for a lift-off patterned back gate. The second mask is designed to allow for patterning the active layer as well as the dielectric. The third mask is for lift-off deposition of the source drain electrodes. An example of a TFT layout with a 1000 µm channel width and 100 µm channel length is shown in Fig 1.3.3. All of the masks allow for either wafer-scale or chip-scale processing as needed.

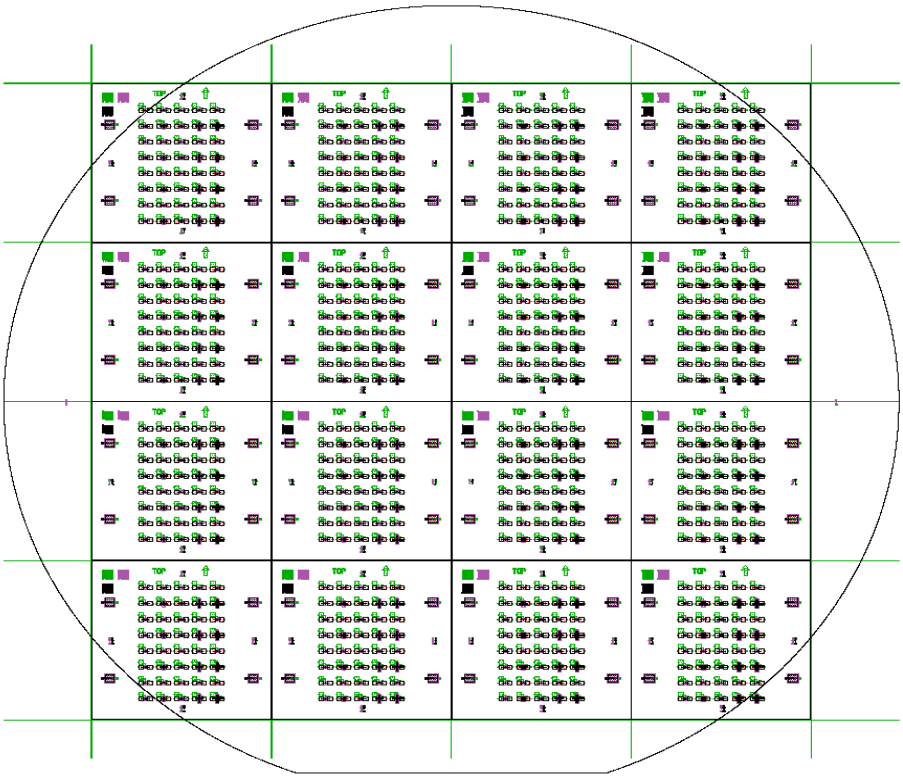

Figure 1.3.1: Wafer scale layout of devices.

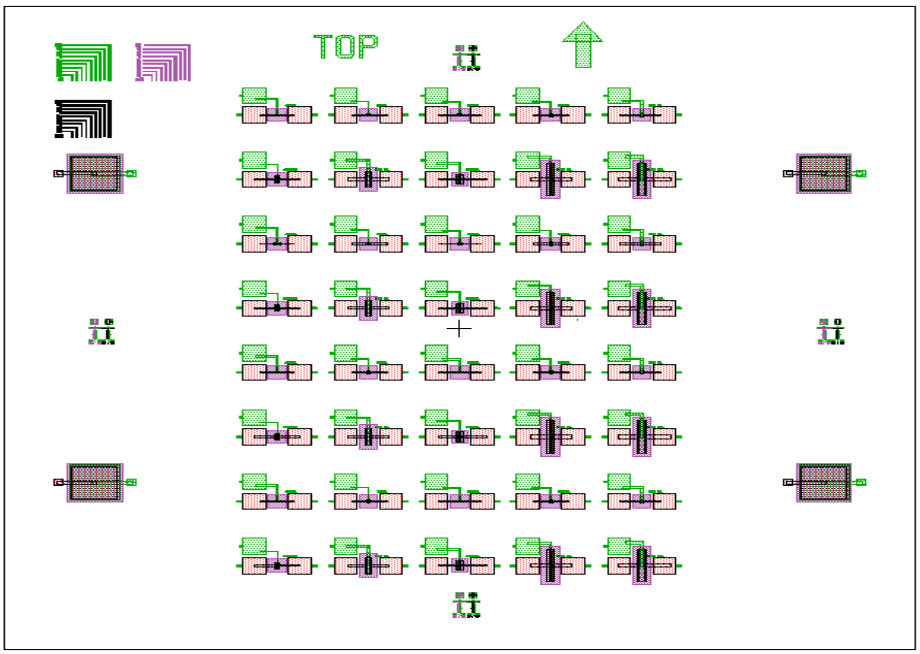

Figure 1.3.2: Chip scale layout. (Green = Gate, Purple =Dielectric / Active Layer, Pink = Source/ Drain Electrodes).

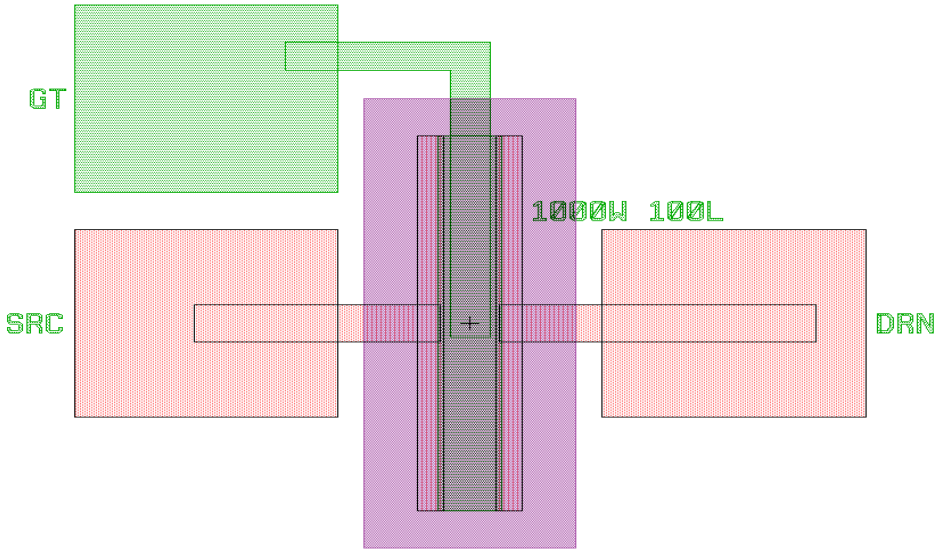

Figure 1.3.3: Representative example of individual node layout. (Green = Gate, Purple =Dielectric / Active Layer, Pink = Source/ Drain Electrodes).

1.3.b Device Fabrication in Collaboration with RTI International

The responsibilities for device fabrication are divided such that RTI International (Int'l) will initially perform all processing other than the active layer. NC A&T will then replicate the processes at RTI and perform more device processing over time. Preliminary devices have been processed using PEN (Poly (ethylene 2, 6-naphthalate) as the starting substrate due to its good barrier properties, relatively high processing temperature, and enhanced performance in flexible electronics. A chromium gate metal layer was deposited by e-beam deposition and photo-patterned using a lift-off process. A series of different dielectrics (discussed below) was deposited by PECVD at 150°C (limited by the PEN substrate) on top of the gate electrode. The substrates were then sent to NCA&T for active layer deposition. The active layers were deposited by RF sputtering and annealed in two different ambient which include air and N_2 +10%H_2 ambient for duration of 1hr.

Three different dielectrics / dielectric stacks were chosen (see Table 1.3.1). The first, SiO_2, is the most commonly used dielectric in the literature. Thermally grown SiO_2 on Si will be used as a control for a high quality dielectric. The low temperature PECVD layer was also deposited on a Si substrate to evaluate the effects of using a polymer substrate. The second dielectric replaces the top 500Å of the oxide layer with silicon nitride, SiN_x. The third dielectric iteration is similar to the second dielectric stack with a top layer of parylene. The different dielectric materials were chosen to provide very different chemical surfaces that should exhibit different characteristics for surface trap states, and therefore device stability. Only the top layer was replaced to keep the bulk capacitance of the gate dielectric relatively constant. Surface defects are a material dependent characteristic and play an important role in threshold

voltage, on- and off- currents, hysteresis, and to a lesser extent on / off ratio. Thus this study will allow us to evaluate the nature, role, and effects of dielectric/active layer surface defects.

Table 1.3.1 *List of substrates and dielectrics used in the TFT study.*

Substrate	Dielectric
1-3	2500Å Oxide
4-6	2000Å Oxide / 500Å Nitride
7-9	2000Å Oxide / 500Å Parylene
Si	2500Å Oxide

1.3.c Output Characteristics of GSZO TFTs on PEN carried out at NCA&TSU

The TFTs fabricated on PEN substrates exhibit noisy output characteristics along with high current. Except for the air-annealed PEN TFT deposited with O_2~10 sccm (9%), all the TFTs which include as-grown and annealed in N_2+10%H_2 ambient did not produce operating TFT. TFTs that were air-annealed appear to operate like TFTs with clear saturation. Drain current is also exceptionally high as compared to other TFTs with I_D between 10^{-6}-10^{-4} A (Fig. 1.3.4). The poor performance was attributed to the high surface roughness of the starting PEN substrate.

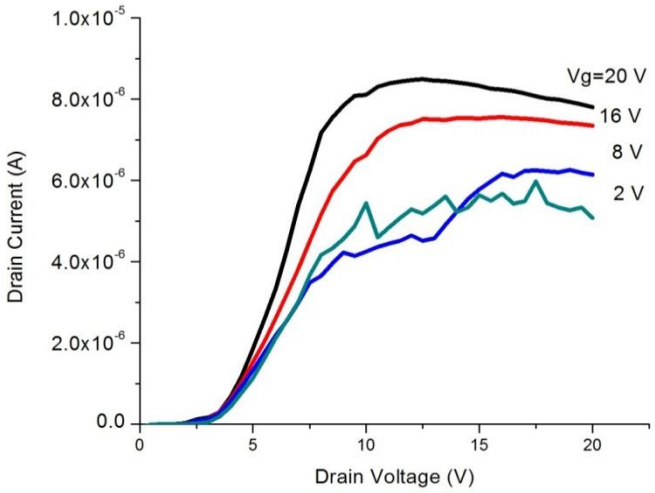

Figure 1.3.4: Output characteristics of TFT on PEN with Parylene as the dielectric. Deposited with O_2~10% and air annealed at 150 ^{o}C for 1hr.

1.4 Student Participation and Educational Component

One M.S.E.E. thesis entitled "Transfer Length Measurements for varied Metallization Options and Processing of Gallium Tin Zinc Oxide (GSZO) TFTs" by **Shereen Farhana** and Ph.D. preliminary oral exam entitled "The Effects of Deposition Parameters on the Performance of RF Sputtered GSZO Thin Film Transistors" by **Tanina Bradley** were completed during this period. **Eric Forsythe** from ARL, MD and **Jay Lewis** from RTI International served on **Tanina Bradley's** dissertation proposal committees.

There were three oral presentations [4-6] made by the graduate students. **Tanina Bradley** presented at MRS/AVS/ASM North Carolina symposium, **Adam Bowen** and **Robert Alston** presented at FlexTech Alliance 2011 Flexible Electronics and Displays Conference and Exhibition. Also two undergraduate students **Sinelk Behane** and **Jazmin Clark-Harris**, recipients of LSAMP Fellows-2011 worked on measuring the contact resistance of different metal source and drain contacts by transfer length measurement. An oral presentation9 of this work was made by Sinelk Behane at 2011 NC LSAMP/RISE Joint Research Symposium, at Fayettteville State University.

Year 2

2.1 The Effect of Deposition and Annealing Temperature on GSZO TFTs

Transistor performance was investigated as a function of both deposition and annealing temperature to determine an ideal combination for trap state reduction. Photo-excitation was used to evaluate qualitatively the variation in the density of traps present for the respective deposition and annealing temperatures. TFTs exhibiting a drain current (I_D) of 10^{-6} A, threshold voltage (VT) of -3 V, subthreshold swing (SS) of 1.3 V/decade, and on/off current ratio ($I_{on/off}$) of 10^6 was achieved for the channels deposited at 150 ^oC after annealing the channel at 250 ^oC for 1hr. The data suggest that the trap density and its energetic dependence are strongly influenced by the deposition and annealing temperatures. This work has been detailed in Tanina Bradley's dissertation[2].

2.2 C-V Characterization of TFT

Capacitance-voltage (C-V) characterization was set up as it is a simple and powerful tool to get rapid insight into the performance of the TFT and to compliment the information provided by the I-V characteristics. This measurement can be used in the TFT configuration and can be used to get quantitative information on the interface state density and contact resistance.

The C-V measurement of our GSZO TFTs was carried out at 250 Hz and 1 MHz frequencies. Comparisons between GSZO TFT samples of different contacts, deposition temperature, and post annealing temperature and duration contacts were made and were compared to their output and input I-V device characteristics. The details of this work are described in Olanrewaju Ogendengbe's Master's Thesis[7] and following is a brief summary.

Figures 2.2.1-2.2.3 are representative of three TFTs with Au/Ti (sample B) and Al (samples E and F) contacts. In all the cases the GSZO films were deposited at room temperature (RT). For samples B and F they were annealed at 250 ^oC in air for 1hr and post annealed for 5 minutes at 240 ^oC in air after the metal deposition. In the TFTE, the channel was annealed at 150 ^oC with no post contact annealing.

Listed below are the observations on the C-V characteristics of these 3 TFTs.

1. Three different operational regimes accumulation, depletion and inversion, as in the metal oxide semiconductor field effect transistor can be identified for the samples B and F, while sample E does not exhibit inversion regime.

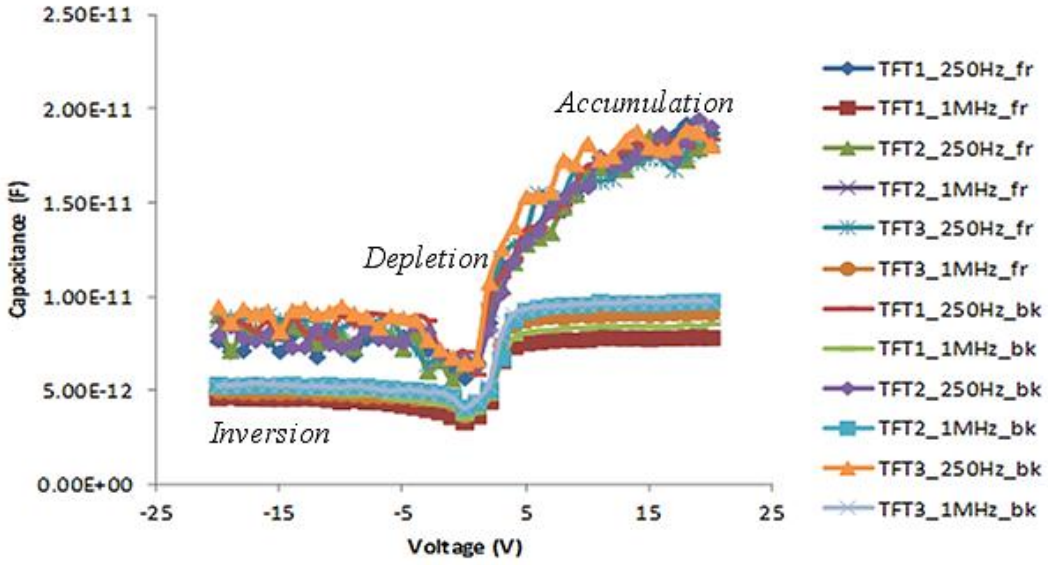

Figure 2.2.1: C-V Characteristics for GSZO TFT Sample B.

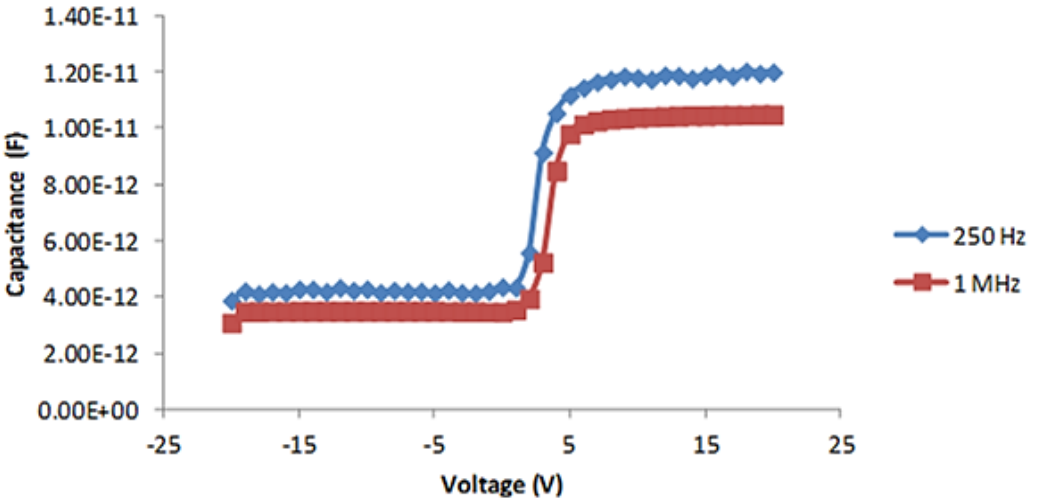

Figure 2.2.2: C-V Characteristics for GSZO TFT Sample E.

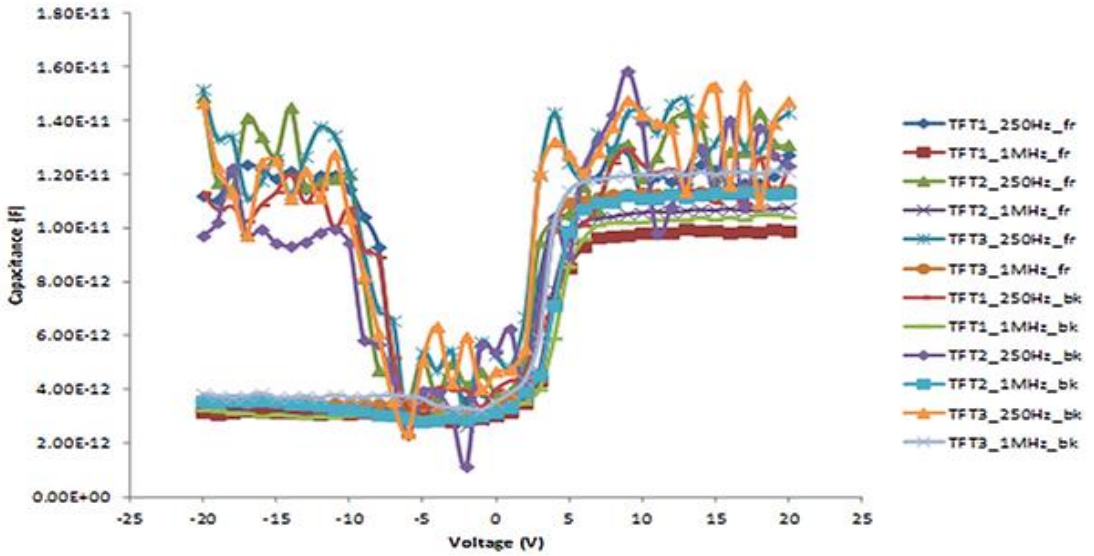

Figure 2.2.3: C-V Characteristics for GSZO TFT Sample F.

2. Comparing samples B to samples E and F, it was observed that the capacitance value in the accumulation regime varies with change in frequency for the GSZO TFTs with Au/Ti contact while the capacitance value in the accumulation regime was almost invariant with change in frequency for the GSZO TFTs which had Al contacts.

3. The common observation for all the TFT samples lies in the abrupt change in the capacitance (C) value with the onset of the depletion regime. The transition from the accumulation regime to the depletion regime is almost step-like in nature.

4. Strength of the inversion regime at low frequency varies with the TFT, with the TFT E exhibiting no inversion regime while F shows strong inversion and TFT B being moderate inversion.

Following is a brief discussion on each regime.

Accumulation Regime

The highest value of the capacitance is obtained in the accumulation regime at low frequencies. The capacitance in the accumulation regime (C_{acc}) in the low frequency regime is in the range of 1.6 to 3 x 10^{-4} Fm^{-2} and is close to the C_{ox} of 3.6 Fm^{-2} determined independently. We tried to correlate this capacitance to the oxide capacitance as in the conventional MOSFET. In the accumulation regime, the observation about the variation in capacitance values determined at different frequency can be largely attributed to contact resistance. Contact resistance (R_c) can be expressed as shown in the equation 1 below, where C_{ma} is the measured capacitance in accumulation, C_{ox} is the oxide capacitance and *w* the frequency of operation.

$$C_{ma} = \frac{C_{ox}}{(1 + w^2 R_c^2 C_{ox}^2)} \quad (1)$$

Therefore GSZO TFT sample with Au/Ti contacts exhibit higher R_c than the ones with Al contacts. R_c of Au/Ti is estimated to be almost twice the contact resistance of Al. This is consistent with the transfer length measurement carried out on Au/Ti and Al contacts by Shereen Farhana[5] of our research group and amongst the two contacts, Al contact exhibited much lower contact resistance in the order of $10^3\ \Omega cm^2$.

Interface trap is another major contributor to accumulation regime. These manifest as the impedance of the semiconductor-insulator interface which in turn decreases the capacitance of the semiconductor. Interface trap density (D_{it}) has been estimated from the combination of high and low frequency C-V data, the details of which are provided in Ogedengbe's M.S. Nanoengineering thesis[7]. It is to be noted that the interface trap density was found to be high close to the conduction band edge. Hence the overall capacitance of the device decreases. The presence of interface state density, we speculate to be responsible for the deviation of the C_{ma} of the GSZO device from the C_{ox} of the Si/SiO_2 structure measured independently. It is observed that the transistor performance deteriorates as the C_{ma} of the TFT device deviates from the C_{ox} of the Si/SiO_2 structure. The estimated values for the interface trap densities and the GSZO device are presented in Table 2.2.1.

Table 2.2.1: *Summary of deposition conditions, and comparison of C-V and I-V data for GSZO TFT samples.*

Sample	B	E	F
Contacts	Au/Ti	Al	Al
Annealing Temp (C)	250	150	250
Post Annealing (C)	240	-	240
Peak D_{it} ($x10^{11} cm^{-2} eV^{-1}$)	2.2	2.5	2.4
V_t after Post Annealing (V)	2.9	-	-0.9
C_{ma} ($x10^{-4} Fm^{-2}$)	2.7	-	1.8
I_{off} ($x10^{-11} A$)	20	-	3
$I_{on/off}$ (10^5)	4	-	1

Depletion regime

Comparing the C-V curves of our GSZO TFTs to ideal MOSFET ones, it was observed that capacitance change from accumulation to depletion is step-like in TFT as opposed to gradual change with gate voltage in a metal oxide semiconductor field effect transistor (MOSFET). The capacitance remains at the lowest value in the depletion regime and the value remains invariant with the change in the gate voltage, particularly at high frequencies. Such a plateau is also unique to the TFT case and is attributed to the small thickness of the semiconductor material, which is just a few nanometers in comparison to microns in the conventional MOSFET.

Inversion regime

Inversion regime is observed only in some samples when the TFT is annealed after the formation of contacts and also only at low frequencies. Annealing of contacts accelerates interfacial reactions, which will eventually lead to the out diffusion of oxygen from the GSZO films to the contacts (Au/Ti or Al). This out diffusion can create oxygen vacancies and increase the carrier concentration resulting in more conductive GSZO channel. The negative shift of the threshold voltage (V_t) observed in these samples attests to the above conjecture. We speculate that this also affects the depletion regions formed on the surface due to the electron induced increased adsorption of oxygen at the surface. Therefore, as negative voltage is applied to the gate, the electric field is in a direction to detrap the electrons from the GSZO films and drive away from the oxide interface and possibly driving the minority holes if there are any to the interface. This results in the oxide capacitance dominating in the inversion regime at the low frequency, similar to MOSFET.

The D_{it} values obtained by C-V method for all the GSZO TFT samples tested during this experiment are in the order of 10^{11} $cm^{-2}eV^{-1}$. The extracted D_{it} values obtained from this experiment compare well with the values of 10^{11} $cm^{-2}eV^{-1}$ in polysilicon TFTs[8,9] and the value obtained for IGZO TFT[10] reported in literature. The information provided by this analysis can be applied in our future TFT design on the polymer.

The values obtained for interface trap density are only estimates as few assumptions that apply to MOSFET has been extended to a TFT device. Because of the complexity of deriving a separate model for the TFT device, we applied the MOSFET model and we assumed that the contact resistance is negligible while estimating interface trap density. Thus, although the extracted D_{it} values are not too accurate, however they provide us a rough order of magnitude.

2.3 TFT Fabrication with Processing Temperatures below 150 °C

The transition of the fabrication of TFTs to polymer substrates requires the temperature to be lowered to 150 °C as polyethylene naphthalate has an upper working temperature of 155 °C. In this section, we present the optimization of the TFT performance by reducing the temperature involved to 150 °C for two metal contacts, Al and Au/Ti.

TFTs were fabricated on n^+ Si substrate with the inverted gate configuration as the other TFTs discussed earlier, with the difference that the deposition, channel annealing (in air) and post-contact annealing (in vacuum) temperatures were carried out at 150 °C. The GSZO annealing duration of 1-hour and 4 hours and the post-contact annealing duration of 1'and 5' were investigated. TFTs had 2:1 W/L ratio with a 50 µm channel length. It is to be noted that the drain current for the room temperature deposited TFT annealed at 150 °C with various post contact annealing duration did not exceed 10^{-8} A.

2.3.a I-V and C-V Characteristics for Al Contact

The best output and transfer characteristics of TFTs with Al metal contact obtained for 4 hr. annealing temperature with 5' post contact annealing durations are shown in Fig 2.3.1, respectively. The C-V characteristics for different annealing and post-contact annealing durations are illustrated in Fig 2.3.2. Table 2.3.1 summarizes the I-V and C-V performance of the TFTs for the different conditions. Mobility appears to improve with the annealing duration and overall improvement by 2 orders of magnitude is observed for the duration that we studied. Hence, the drain current also increases. However, the V_T and $I_{on/off}$ are influenced by post contact and channel annealing duration, respectively.

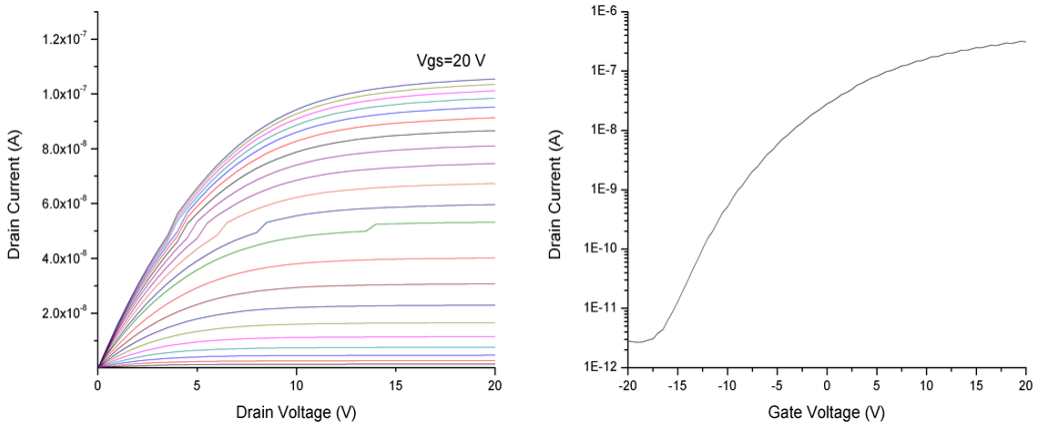

Figure 2.3.1: Output and transfer graphs of Al-TFT annealed at 150 °C for 4 hours and with PCA at 150 °C for 5 minutes.

With increasing annealing duration the C-V graph shifts towards negative bias voltage, while the post contact annealing is observed to enhance the capacitance value in the accumulation region. These seem to suggest that annealing duration reduces the interface states while the post contact annealing lowers the contact resistance.

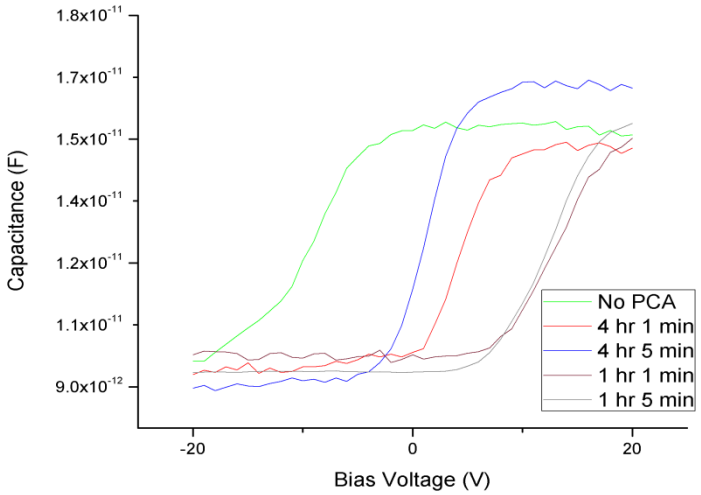

Figure 2.3.2: Low frequency C-V characteristics of TFTs with the Al metal contact. The channel annealed at 150 °C for 1 and 4 hours with various PCA.

Table 2.3.1: *Summary of TFT electrical characteristics with Al contacts*

Annealing Duration (Hr.)	PCA Duration (Min.)	μ_{FET} (10^{-3} cm-^{2}/V-s)	V_T (V)	$I_{on/off}$ (10^4)	I_G (10^{-11} A)	C_{ma} (10^{-11} F)	I_D (10^{-7} A@20 V V_{DS} and V_{GS})
1	1	0.3	8.0	0.12	3.3	1.5	0.15
	5	6.1	7.8	0.51	3.3	1.5	0.82
4	1	5.1	8.2	5.0	2.8	1.5	1.8
	5	14	-3.4	3.7	5.7	1.6	3.1

2.3.b I-V and C-V Characteristics for Au/Ti contact

The I-V characteristics (Fig. 2.3.3) and corresponding C-V characteristics (Fig. 2.3.4) with Au/Ti metal contacts show similar dependence on the annealing and post-contact annealing duration. Table 2.3.2 describes the effects of channel and post-contact annealing durations on the electrical characteristics of the Ti/Au TFTs. The major difference between the two sets of samples are the mobility values, being almost one more magnitude higher in the case of Ti/Au contact resulting in enhanced values of I_D and higher $I_{on/off}$. The capacitance in the accumulation region is higher which suggests that contact resistance is somewhat lower. This reduction in the contact resistance was also borne out independently from the transfer length measurements by Shereen Farhana[1] from our group.

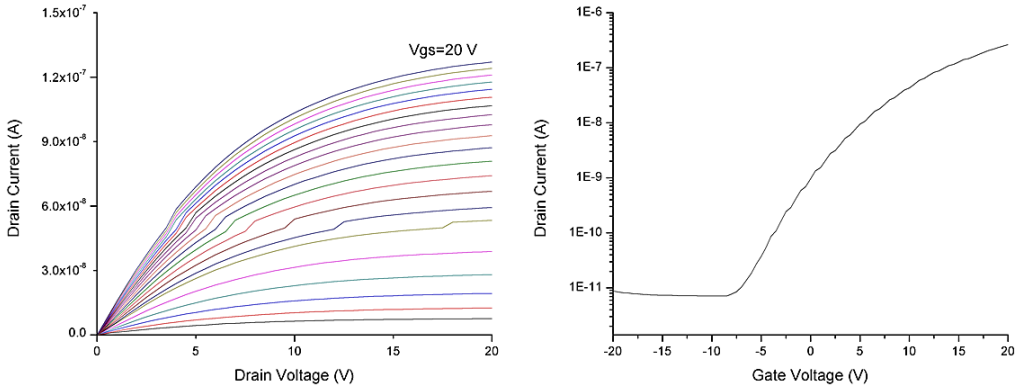

Figure 2.3.3: Output and transfer graphs of Au/Ti-TFT annealed at 150 °C for 4 hours and with PCA at 150 °C for 5 minutes.

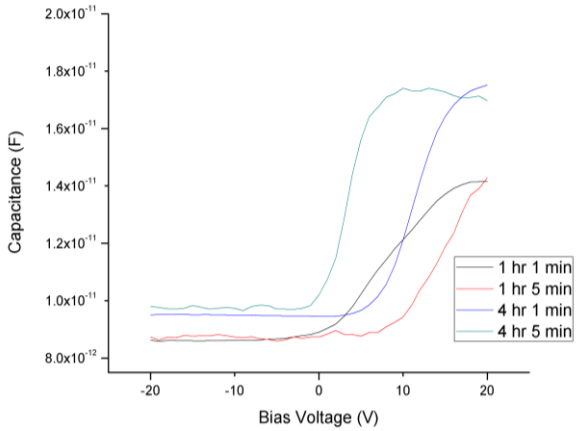

Figure 2.3.4: Low frequency C-V characteristics of Au/Ti-TFTs annealed at 150 °C for 1 and 4 hours with various PCA.

Table 2.3.2: *Summary of TFT electrical characteristics with Au/Ti contacts*

Annealing Duration (Hr.)	PCA Duration (Min.)	μ_{FET} (10^{-3} cm-^{2}/V-s)	V_T (V)	$I_{on/off}$ (10^4)	I_G (10^{-11} A)	C_{ma} (10^{-11} F)	I_D (10^{-7} A@20 V V_{DS} and V_{GS})
1	1	6.6	8.2	2.7	3.5	1.4	0.02
	5	15	7.3	4.9	2.9	1.4	0.3
4	1	26	7.0	12	2.5	1.8	0.8
	5	14	-4.2	12	3.0	1.7	2.6

It has been shown that post-deposition film annealing and post-contact annealing duration is an important process while preparing amorphous GSZO TFTs for plastic substrates. The best values for the TFTs obtained were I_D~ 10^{-7} A, V_T~ -4.2 V, μ_{FET}~ 1.4x10^{-2} cm^2/V-s, with $I_{on/off}$~ 10^5 for a low-temperature process (~ 150 °C) on Au/Ti contacts. Film annealing has found to have a strong effect on the threshold voltage and $I_{on/off}$ ratio of Au/Ti-TFTs while post-contact annealing has a strong effect on the mobility of Al-TFTs. It has also been shown through

capacitance measurements that both annealing processes affect the trap density within the semiconductor/oxide interface and contact resistance.

2.4 Thin Film Transistor Device Fabrication on Polymer Substrates in Collaboration with RTI Int'l

RTI International has continued its role of supporting TFT device fabrication on plastic substrates. During this grant period the latest iteration to the fabrication was introduction of planarization layers on the plastic substrates. The last set of devices indicated that the roughness of the flexible substrate caused issues in the overall device performance. The goal was to reduce the roughness with two different planarization techniques. The first was use a spin-on planarization layer, and the second was to use a CVD deposited layer. Su-8 was chosen as the spin-on polarization layer, and PECVD deposited oxide was chosen as the CVD deposited planarization layer.

A batch of ten substrates were started (2 Si, 1 Kovar (FeNi Alloy, CMP polished), and 7 on PEN). One Si wafer and 3 PEN substrates were coated with a 5μm layer of Su-8 and were subsequently exposed and cured. One Si wafer, 4 PEN substrates (one of the Su-8 coated substrates and 3 standard PEN substrates), and the Kovar foil were coated with 1μm of PECVD deposited oxide using a recipe known to give more conformal films. The last PEN substrate was used as received and will be used as a control. On top of the planarization layer, a gate metal (Cr) contact was patterned and deposited. The gate dielectric was then deposited. SiO_2 and Si_3N_4 were the dielectrics chosen for this experiment. This was accomplished by masking half of the substrate during each of the dielectric depositions, resulting in half of the substrate with oxide and half with nitride. The substrates were then shipped to NC A&T for further processing.

2.5 Student Participation and Educational Component

One **Ph.D. dissertation** entitled "The Effect of Deposition Parameters on the Performance of RF Sputtered GSZO Thin Film Transistors", by **Tanina Bradley (a minority female)** was completed during this grant period. **Eric Forsythe** from ARL, MD and **Garry Cunningham** from RTI International served on Tanina Bradley's dissertation committee.

Olanrewaju Ogedengbe, Master's thesis entitled "Capacitance-Voltage Characterization of Gallium Tin Zinc Oxide (GSZO) Thin Film Transistors" was completed. He is the **first Nanoengineering Master student from Joint School of Nanoscience and Nanoengineering.**

Two oral presentations[11,12] were made by the students which include one at MRS Fall Meeting, Boston 2011.

2.6 Infrastructure Development

During this period C-V measurement was set-up. Fig 2.6.1 shows the device test setup consisting of the device under testing (DUT) on a stainless steel platform with high-sensitivity probes placed on the contacts of the DUT connected to tri-axial cables, which are connected to the HP 4284 LCR device. In-house programmed software triggers the controls of the LCR meter which supplies the DC voltage and AC current to the DUT. The program then records and provides a graphical display of the measurement at the end of each experiment. The computer program also provides an interface that allows the user to input the measurement parameters such as frequency, DC and AC voltage values. A 2-D schematic of the DUT and connections are shown in Fig 2.6.2.

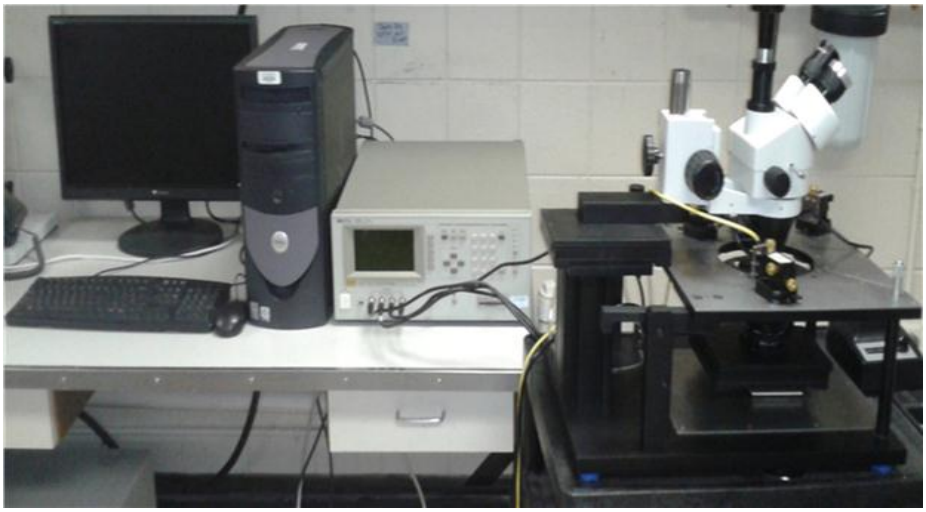

Figure 2.6.1: Experiment set up for C-V measurement on GSZO TFT.

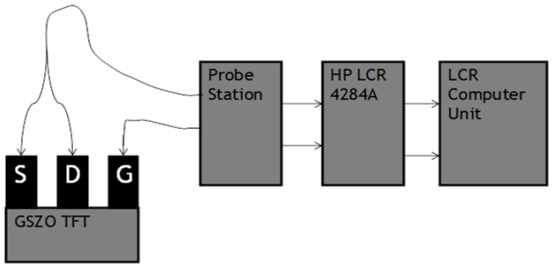

Figure 2.6.2: Experiment set up for C-V measurement on GSZO TFT.

Year 3

3.1: TFT with all the Processing Temperatures below 150°C

3.1.a. Effects of Annealing Temperature, Deposition Temperature and Channel Thickness on GSZO Films and on the TFT Devices

The bottom-gate GSZO TFTs fabricated on n^+ Si substrates were analyzed by varying procedure operations such as annealing and deposition temperatures, annealing duration, channel thicknesses and deposition pressures. GSZO films were investigated using material characterizations namely, RBS and XPS for elemental composition, XRR and AFM for surface morphology and absorption characterization for optical properties. Bottom-gate GSZO TFTs were fabricated onto PEN and its electrical characteristics were also analyzed.

i. Annealing

Annealing Temperature Reduction Previous work reported on amorphous GSZO TFTs from our group was with channels which were annealed at 250°C for 1 hour, while this work is focused on GSZO TFTs annealed at 140°C for 1 hour. Table 3.1.1 summarizes the electrical characteristics of the TFTs for two different annealing temperatures. With decreasing annealing temperature the threshold voltage slightly improved after shifting positively from -2 V to -1 V however SS degraded from 1.0 to 4 V/dec. Also I_{ON} decreased by an order of magnitude as the annealing temperature reduced, resulting in an $I_{ON/OFF}$ decrease by 1 order of magnitude.

Table 3.1.1: *Electrical characteristics of TFTs annealed at different temperatures*

Annealing Temperature	I_D (A)	$I_{ON/OFF}$	V_{ON} (V)	SS (V/dec)
250 °C	10^{-7}	10^5	-2	1
140 °C	10^{-8}	10^4	-1	4

Annealing Duration To improve the performance of the GSZO TFTs without exceeding an annealing temperature of 150°C, the annealing duration was varied. The TFTs were annealed for 1, 6 and 10 hours in air. Table 3.1.2 displays TFTs annealed at 140°C for different annealing durations and the transfer curves are shown in (Fig 3.1.1). The maximum drain current increased from 10^{-8} to 10^{-7} A and saturated even up to 10 hours of annealing study. The $I_{ON/OFF}$ ratio correspondingly increased from 10^3 to 10^5 with no apparent change in I_{OFF} with increase in annealing duration. The V_{ON} shifted negatively with increasing annealing duration, stopping at -9.5 V after 10 hours. The μ_{FE} improved with annealing duration by almost 2 orders of magnitude as SS decreased by half.

To reduce contact resistance and improve film adhesion, the GSZO TFTs were placed on a hotplate at 140 °C for 1 minute. This procedure we refer to as post-contact annealing (PCA) and the results are shown in Table 3.1.3. I_{ON} increased and order of magnitude for the 4 hour annealed device and remained constant for the 6 hour annealed device. For all devices, $I_{ON/OFF}$ improved by continuously increasing an order of magnitude for the 1, 4 and 6 hour annealed devices while V_{ON} shifted negatively. The SS remained the same and μ_{FE} increased for all devices.

Table 3.1.2: *Electrical characteristics of TFTs annealed at different temperatures*

Annealing Duration (Hr)	I_D (A)	$I_{ON/OFF}$	V_{ON} (V)	SS (V/dec)	μ_{FE} ($cm^2/V{\cdot}s$)
1	10^{-8}	10^4	-2.5	4	0.004
6	10^{-7}	10^5	-6.2	2.4	0.02
10	10^{-7}	10^5	-9.5	2.12	0.1

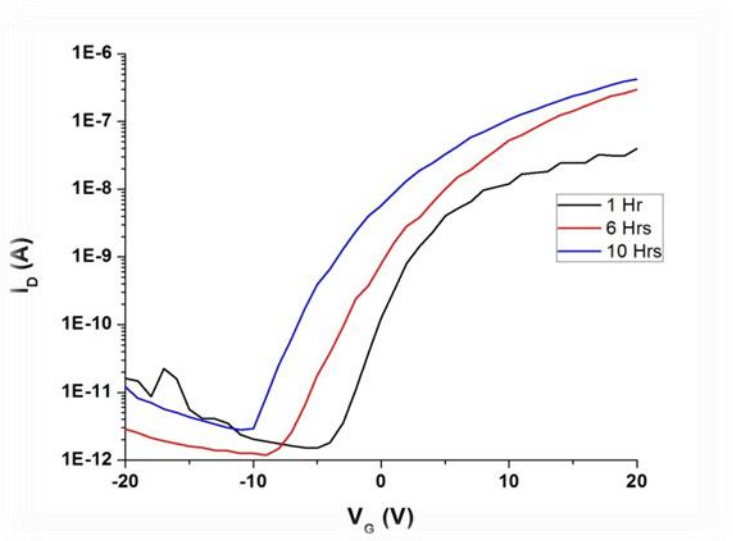

Figure 3.1.1: Transfer characteristics of TFTs annealed at 1, 6 and 10 hours in air

Table 3.1.3: *The electrical properties of TFTs annealed for different durations before and after PCA*

Annealing Duration (Hr)	I_{ON} (A)	$I_{ON/OFF}$	V_{ON} (V)	SS (V/Dec)	μ_{FE} ($x10^{-2}$ $cm^2/V{\cdot}s$)
1	$1x10^{-8}$	$1x10^{5}$	-2.5 → -3.5	4 → 2	0.4 → 1.7
4	$1x10^{-7}$ → $1x10^{-6}$	$1x10^{6}$	-6.2 → -8	2.4 → 2	0.6 → 2.0
6	$1x10^{-7}$	$1x10^{6}$	-9.5 → -11.5	2.1 → 2	1.6 → 4.6

XPS characterization was done on the surface and 5 nm below 15 nm GSZO films annealed at 140 °C for 3 and 10 hours to examine the effect of annealing duration on atomic composition. Table 3.1.4 provides the summary of the concentration of the constituent elements. Figs 3.1.2 and 3.1.3 show the O 1s spectra de-convoluted into the three OI, OII and OIII peaks of different binding energies for films annealed for 3 and 10 hours which are also tabulated in Table 3.1.5. Figures 3.1.4 and 3.1.5 show the Sn spectra as a function of annealing duration which is listed in Table 3.1.6. Annealing duration appears to have very little effect on the atomic composition of the film. The Sn^{2+} relative at.% on the surface of films increases (14.1 at.% to 39.6 at.%) with increasing annealing duration however decreases (74.6 at.% to 50.6 at.%) below the surface.

Table 3.1.4: *Atomic percentage of various constituent elements in 15 nm GSZO films annealed at 140 °C for 3 and 10 hours*

Annealing Duration	O-(Zn,Ga,Sn)	Cl	Zn	Ga	Sn
3 Hr Surface	53.6	1.0	41.1	2.2	2.2
3 Hr Sputtered	47.7	0.1	46.6	4.6	1.0
10 Hr Surface	53.6	0.8	41.7	1.9	2.0
10 Hr Sputtered	44.9	0.0	49.8	4.0	1.3

Table 3.1.5: *O-1s related relative percentage of 15 nm GSZO films annealed at 140 °C for 3 and 10 hours*

Annealing Duration	O Relative %			Binding Energy (eV)		
	OI	OII	OIII	OI	OII	OIII
3 Hr Surface	61	34	5	530.2	531.7	532.7
3 Hr Sputtered	76	24	0	530.3	531.7	532.7
10 Hr Surface	59	34	6	530.3	531.7	532.7
10 Hr Sputtered	82	18	0	530.1	531.5	532.7

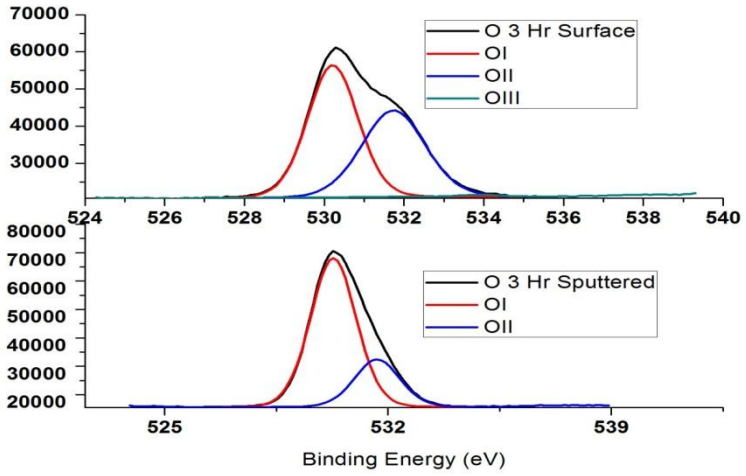

Figure 3.1.2: XPS spectra of O ions in GSZO films annealed at 140 °C for 3 hours

Table 3.1.6: *Sn related relative percentage of 15 nm GSZO films annealed at 140 °C for 3 and 10 hours*

Annealing Duration	Sn Relative %			Binding Energy (eV)		
	Sn^{2+}	Sn^{4+}	Sn^{0}	Sn^{2+}	Sn^{4+}	Sn^{0}
3 Hr Surface	14.1	85.9	0	486.2	486.8	0
3 Hr Sputtered	74.6	25.4	11.9	486.3	487.1	484.5
10 Hr Surface	39.6	60.4	0	486.3	486.8	0
10 Hr Sputtered	50.6	41.8	7.6	486	486.6	484.6

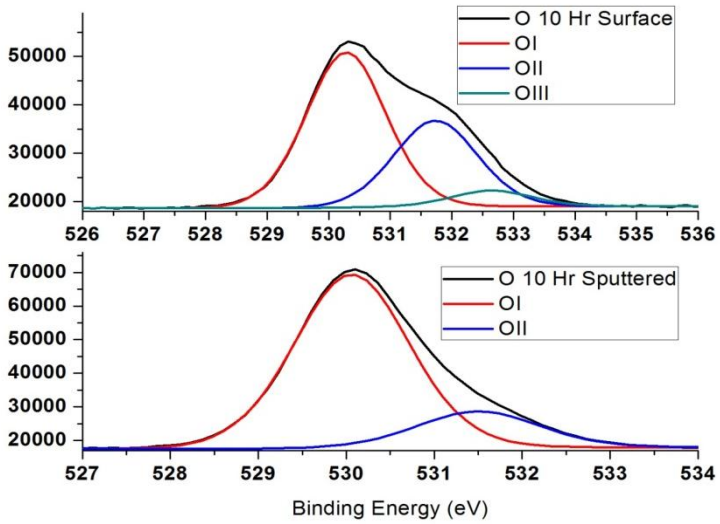

Figure 3.1.3: XPS spectra of O ions in GSZO films annealed at 140 °C for 10 hours

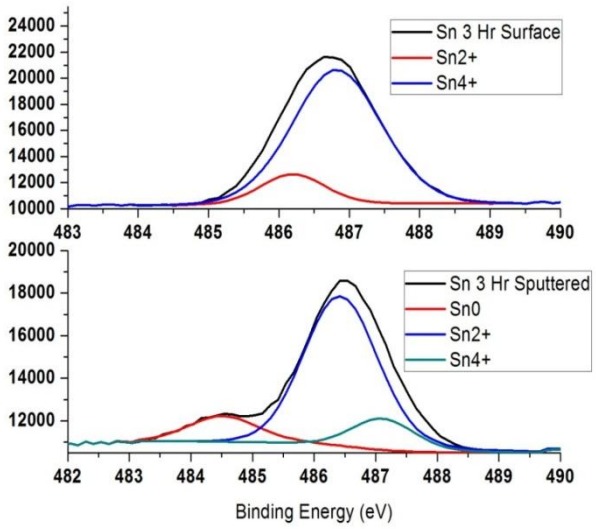

Figure 3.1.4: XPS spectra of Sn ions in GSZO films annealed at 140 °C 3 hours.

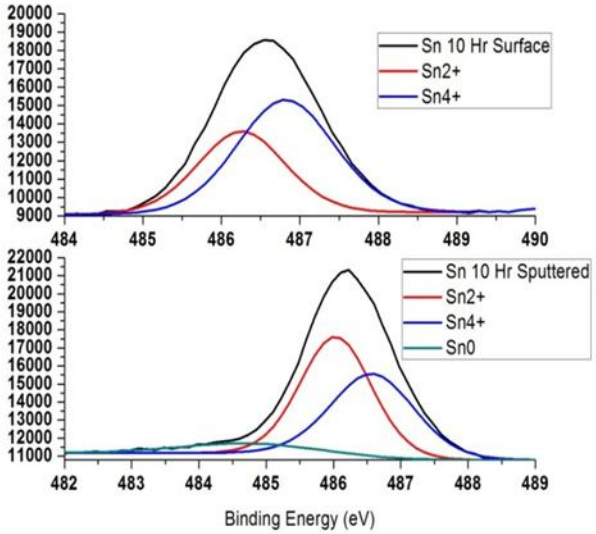

Figure 3.1.5: XPS spectra of Sn ions in GSZO films annealed at 140 °C for 10 hours

ii. Deposition Temperature

The deposition temperature was increased from 50 °C to 100 °C to examine its effects on the electrical performance of the TFTs which are shown in Table 3.1.7 and displayed in Fig 3.1.6. The maximum drain current I_D increased an order of magnitude and $I_{ON/OFF}$ improved by two orders of magnitude with increasing deposition temperature. V_{ON} shifted negatively from -3.2 V to -7 V while the SS slightly degraded by 0.7 V/dec.

Table 3.1.7: *Electrical characteristics of TFTs deposited at different temperatures*

Annealing Temperature	I_D (A)	$I_{ON/OFF}$	V_{ON} (V)	SS (V/dec)
50°C	10^{-8}	10^3	-3.2	2
100°C	10^{-7}	10^5	-7	2.7

XPS characterization was done on the surface and 5 nm below 15 nm GSZO films deposited at 50 °C and 100 °C to examine the effect of deposition temperature on atomic composition (Table 3.1.8). Table 3.1.9 and Fig 3.1.7 and Fig 3.1.8 show the O-1s spectra de-convoluted into the three OI, OII and OIII peaks of different binding energies for films deposited at 50 °C and 100 °C. Table 3.1.10 and Fig 3.1.9 and Fig 3.1.10 show the Sn relative at.% as a function of annealing duration. Increasing deposition temperature appear to decrease the O-1s and increase the Zn related atomic concentration on the surface however there appear to be little change below the surface. Deposition temperature appears to have little effect on the OI and OII species however traces of OIII related species can be found within the bulk of the 50 °C deposited film. The surface of both films contains a large concentration of Sn^{4+} while the bulk of the films are mostly Sn^{2+}. The 100 °C deposited film contains higher concentrations of Sn^{4+} in the bulk than the 50 °C deposited film and traces of Sn^0 can also be found.

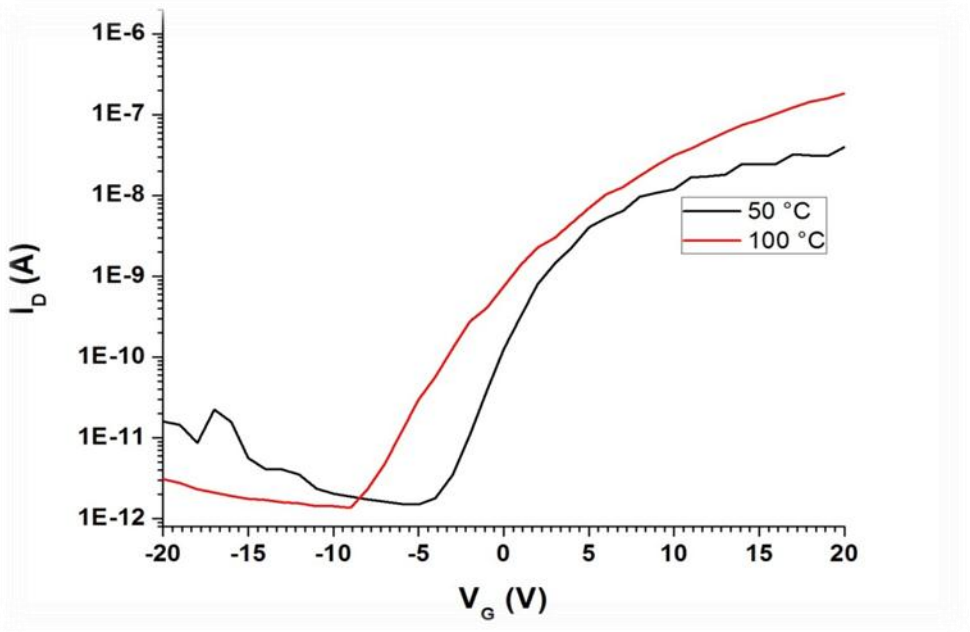

Figure 3.1.6: Transfer graphs of TFTs with varying deposition temperatures

Table 3.1.8: *Atomic percentage of 15 nm GSZO films deposited at 50 °C and 100 °C*

Deposition Temperature	O-(Zn,Ga,Sn)	Cl	Zn	Ga	Sn
50 °C Surface	59.2	0.4	36.6	1.6	2.1
50 °C Sputtered	46.4	0.0	48.5	3.8	1.3
100 °C Surface	53.6	1.0	41.1	2.2	2.2
100 °C Sputtered	47.7	0.1	46.6	4.6	1.0

Table 3.1.9: *O-1s related relative percentage of 15 nm GSZO films deposited at 50 °C and 100 °C*

Deposition Temperature	O Relative %			Binding Energy (eV)		
	OI	OII	OIII	OI	OII	OIII
50 °C Surface	54	39	7	530.4	531.8	532.7
50 °C Sputtered	78	21	1	530.2	531.6	532.7
100 °C Surface	61	34	5	530.2	531.7	532.7
100 °C Sputtered	76	24	0	530.3	531.7	532.7

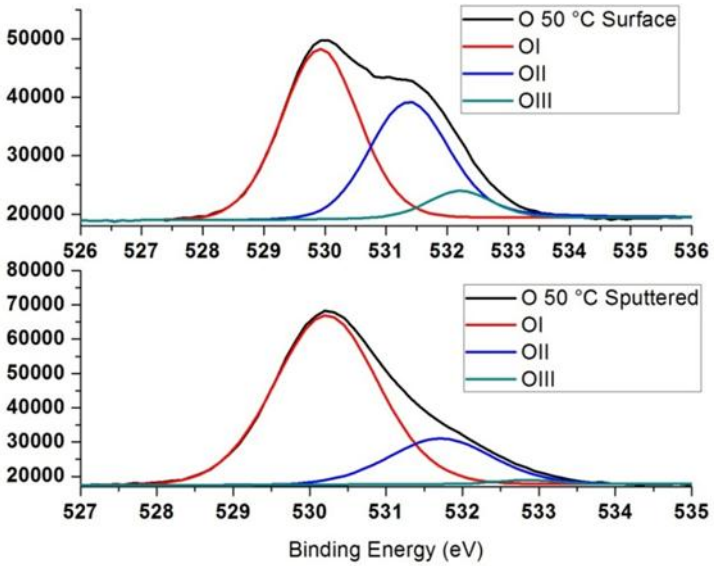

Figure 3.1.7: XPS spectra of O ions in GSZO films deposited at 50 °C

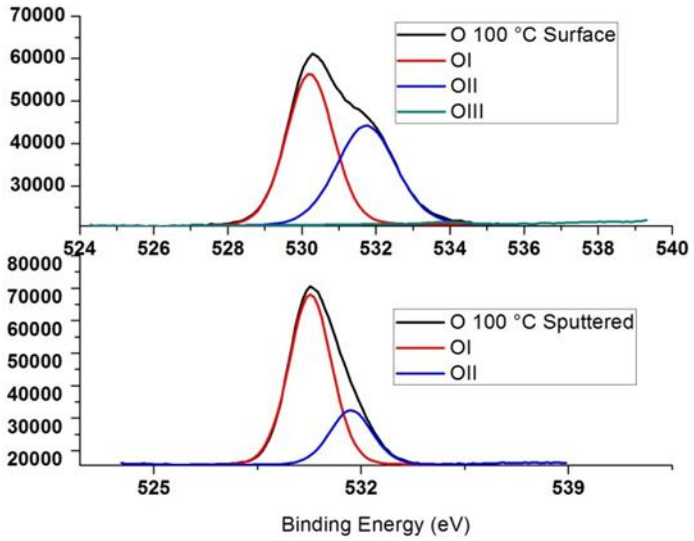

Figure 3.1.8: XPS spectra of O ions in GSZO films deposited at 100 °C

Table 3.1.10: *Sn related relative percentage of 15 nm GSZO films deposited at 50 °C and 100 °C*

Deposition Temperature	O Relative %			Binding Energy (eV)		
	Sn^{2+}	Sn^{4+}	Sn^{0}	Sn^{2+}	Sn^{4+}	Sn^{0}
50 °C Surface	25.2	74.8	0	486.2	486.8	0
50 °C Sputtered	84.4	15.6	0	486.2	486.8	485.7
100 °C Surface	14.1	85.9	0	486.2	486.8	0
100 °C Sputtered	74.6	25.4	11.9	486.3	487.1	484.5

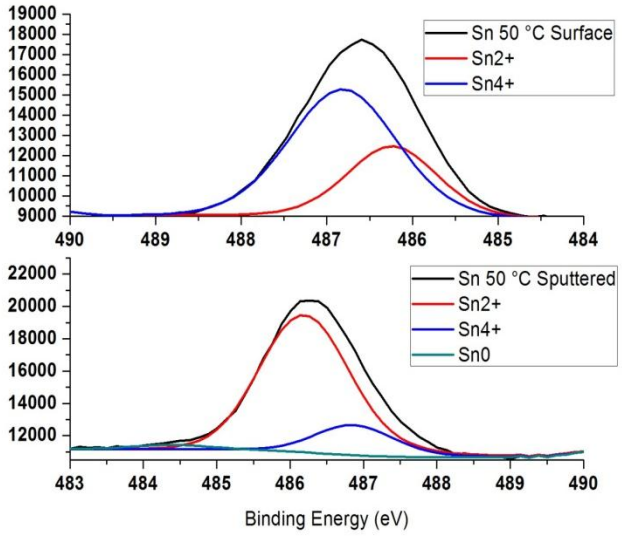

Figure 3.1.9: XPS spectra of Sn ions in GSZO films deposited at 50 °C

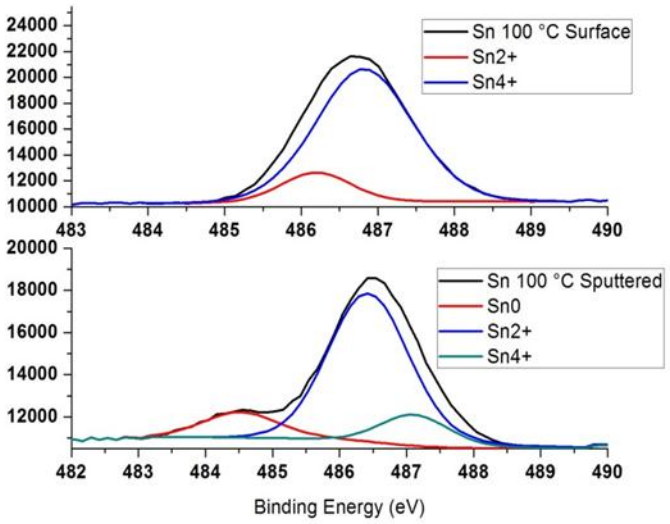

Figure 3.1.10: XPS spectra of Sn ions in GSZO films deposited at 100 °C

iii. Channel Thickness

Active layer thicknesses were varied to examine its effect on the electrical properties of the devices. I-V properties of 30, 20, 15 and 10 nm are listed in Table 3.1.11 and displayed in Figure 3.1.11 along with associated C-V characteristics in Figure 3.1.12. X-ray reflectance (XRR) characterizations were also taken on devices with decreasing channel thickness and are also shown in Table 3.1.11. Both I_{ON} and I_{OFF} decrease with decreasing channel thickness, with $I_{ON/OFF}$ remaining invariant in the 10^6 range from 30 nm to 10 nm. V_{ON} is largely negative at 30 nm however it shifts positively to -5 V at 15 and 10 nm. SS also improves from 2.1 to 1.06 V/dec with reduction in channel thickness with a corresponding increase in µFE to 0.14 cm2/V·s. The C-V graph shows no depletion region and small slope for the 30 nm device with a corresponding increase in slope with decreasing channel thickness. XRR measurements reveal an increase in film density (5.5, 5.9 and 6.5 g/cm^3) with decreasing channel thickness for 30, 15 and 10 nm, respectively. RBS characterization was carried out on 23 nm and 13 nm films and the results are shown in Table 3.1.12, Figure 3.1.13 and Figure 3.1.14. Both results show that film composition is invariant with increasing film thickness.

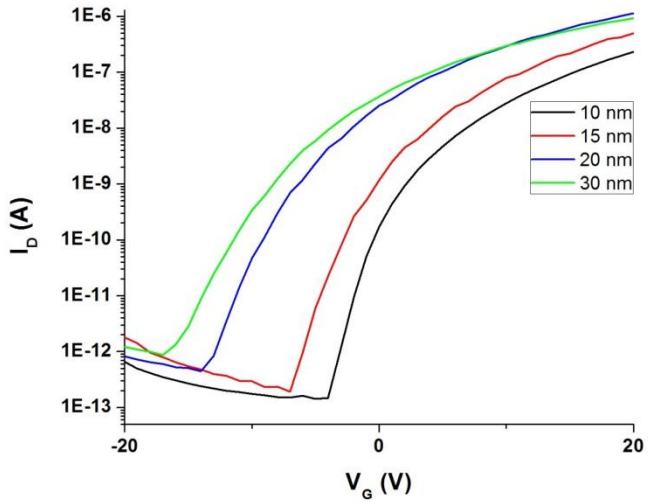

Figure 3.1.11 Transfer graph of TFTs with different thicknesses.

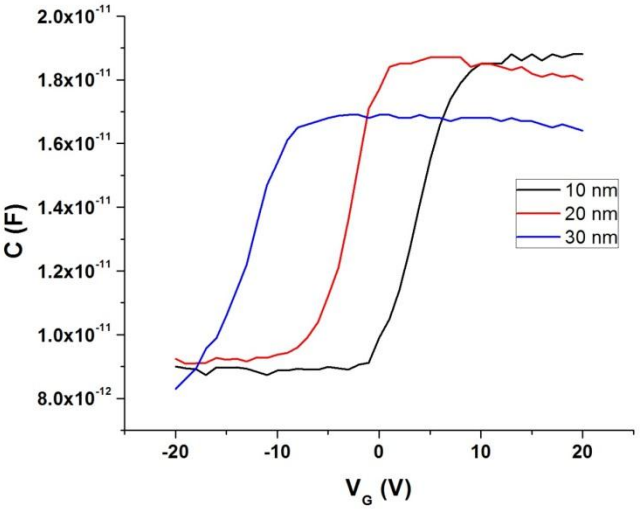

Figure 3.1.12 C-V graph of TFTs with different thicknesses.

Table 3.1.11 *Electrical characteristics of TFTs with different thicknesses*

Channel Thickness (nm)	I_D (A)	$I_{ON/OFF}$	V_{ON} (V)	SS (V/dec)	μ_{FE} ($cm^2/V \cdot s$)	Density (g/cm^3)
30	$9x10^{-7}$	$1x10^6$	-14.5	2.1	N/A	5.5
20	$1x10^{-6}$	$2x10^6$	-12	1.6	0.07	N/A
15	$5x10^{-7}$	$3x10^6$	-5	1.3	0.07	5.9
10	$3x10^{-7}$	$1x10^6$	-5	1.06	0.14	6.5

Table 3.1.12 *RBS characterization of films with different thicknesses.*

Thickness (nm)	Atomic Concentrations (at%)				Density (at/cc)
	Ga	Zn	O	Sn	
13	2.9	40.8	54.6	1.7	$6.77x10^{22}$
23	3.1	43.1	52	1.8	$6.75x10^{22}$

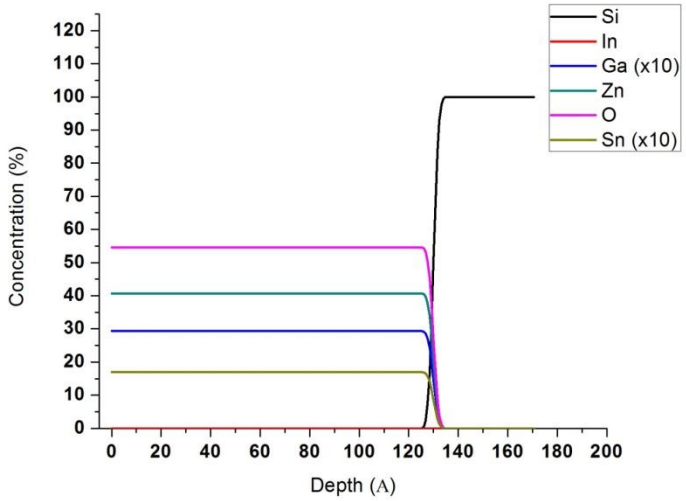

Figure 3.1.13 RBS plot of 13 nm GSZO film

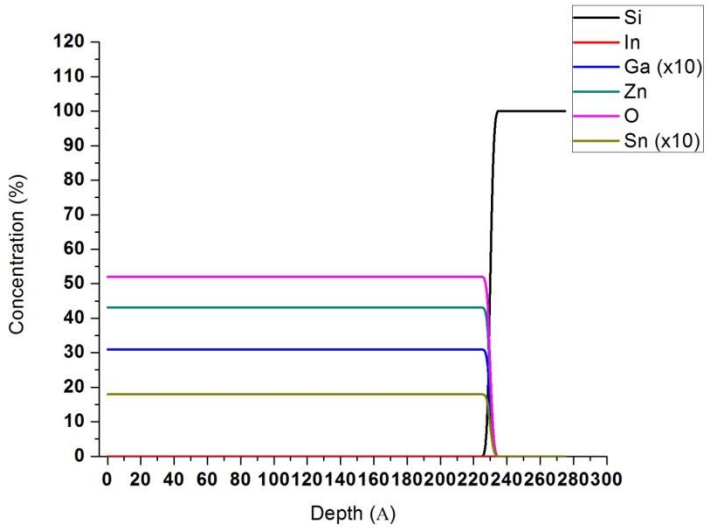

Figure 3.1.14 RBS plot of 23 nm GSZO film

The PCA procedure was used in attempt to further improve the performance of the devices with different channel thicknesses. The electrical performance is shown in Table 3.1.13 and Figure 3.1.15-Figure 3.1.17. The $I_{ON/OFF}$ decreased nearly by an order of magnitude due to

an increase in I_{OFF} while V_{ON} shifted negatively beyond -25 V for the 30 nm device. The 20 nm and 10 nm devices exhibited an increase in $I_{ON/OFF}$ and a positive shift in V_{ON}. The SS increased slightly for the 30 nm device, remained constant for the 20 nm device and decreased slightly for the 10 nm device. The μ_{FE} increased slightly for the 20 nm device and remained constant for the 10 nm device.

Table 3.1.13 *The electrical properties of TFTs with various channel thicknesses before and after PCA*

Film Thickness	I_{ON}	I_{OFF}	$I_{ON/OFF}$	V_{ON}	SS	μ_{FE}
30 nm	$6x10^{-7}$ ->$2x10^{-6}$	$9 x10^{-13}$ ->$1x10^{-11}$	$7 x10^{5}$ ->$1 x10^{5}$	-14.5 ->Beyond -25	3.0->3.2	-
20 nm	$6x10^{-7}$ ->$5x10^{-7}$	$4 x10^{-13}$ ->$2x10^{-13}$	$2 x10^{6}$ ->$3 x10^{6}$	-11.8 ->-8.8	1.8	.01 ->.08
10 nm	$3x10^{-7}$ ->$9x10^{-7}$	$1x10^{-13}$ ->$6x10^{-14}$	$3x10^{6}$ ->$2x10^{7}$	-5->-3.4	1.1->.96	0.14

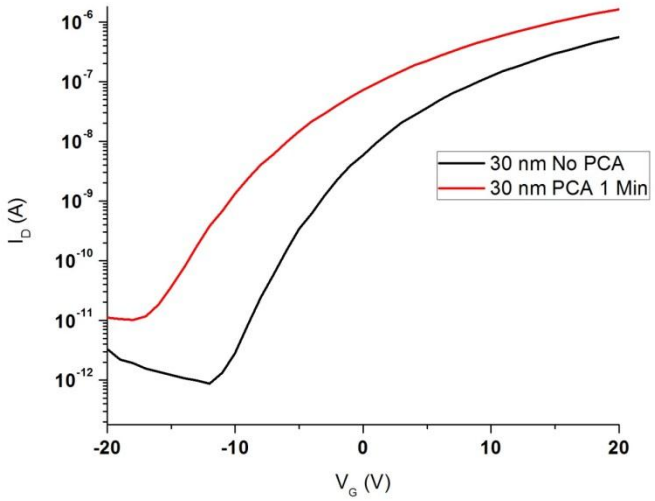

Figure 3.1.15 Effect of post-contact annealing on TFTs with 30 nm GSZO channel layer

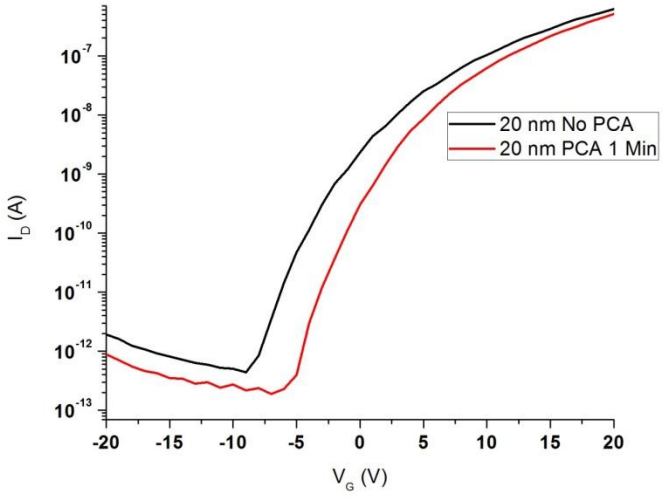

Figure 3.1.16 Effect of post-contact annealing on TFTs with 20 nm GSZO channel layer

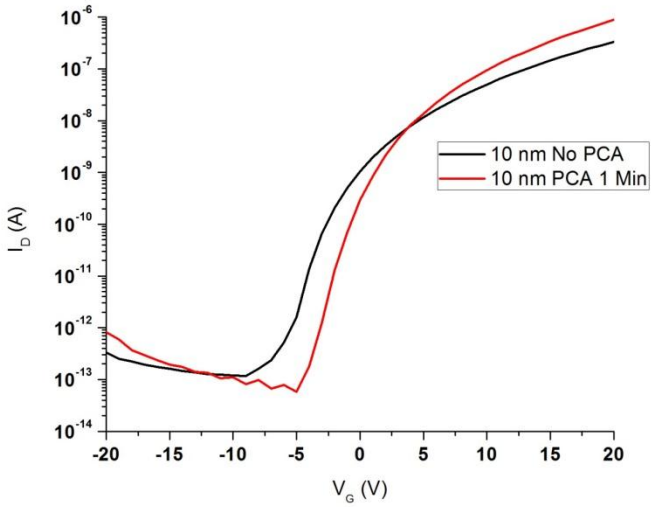

Figure 3.1.17 Effect of post-contact annealing on TFTs with 10 nm GSZO channel layer

iv. Comparison with Higher Annealing Temperature

Further examining on the effects of annealing temperature was taken to investigate the effect of high annealing temperatures. A GSZO TFT annealed at 140 °C for 3 hours and 450 °C for 1 hour were fabricated and the I-V plots are shown in Figure 3.1.18 and Table 3.1.14. It can be seen that overall device performance improves with increasing annealing temperature. SS 1.1 V/dec to 0.4 V/dec, I_{ON} increased 2 orders of magnitude and ION/OFF increased 3 orders of magnitude. XPS characterization was taken on the above films to examine the effect of annealing temperature on atomic composition (Table 3.1.15). Both films are more O-rich on the

surface however the 450 °C film contains is slightly more O-rich than the 140 °C annealed film. While the O at.% and Zn at.% is roughly the same in the bulk of the 140 °C annealed film the 450 °C annealed film shows a large increase in Zn at.%. An increase in Ga at.% and decrease in Sn at.% can be seen in the bulk of both samples however the difference between the samples remain invariant. Table 3.1.16 and Figure 3.1.19 and Figure 3.1.20 show the O-1s spectra de-convoluted into three peaks of different states, i.e., 530.2 eV (OI), 531.7 eV (OII) and 532.7 eV (OIII) for films annealed at 140 °C and 450 °C. On the surface, both films exhibit nearly the same at.% however a difference between the films can be seen 5 nm below the surface. The relative OI at.% increases and OII at.% decreases by 10 % with increasing annealing temperature while the presence of OIII related O-1s elements vanish within the bulk. Table 3.1.17 and Figure 3.1.21 and Figure 3.1.22 show the Sn relative at.% for films annealed at 140 °C and 450 °C. The surface of both films is majority Sn4+ however a difference can be seen within the bulk. The 140 °C annealed film showed a ~60 % decrease in Sn4+ below the surface while the 450 °C showed only a 14 % decrease. The 140 °C annealed film also showed traces of the metal Sn0 on the surface however these traces were not found within the bulk and the 450 °C annealed film showed no traces of Sn0 neither on the surface nor within the bulk.

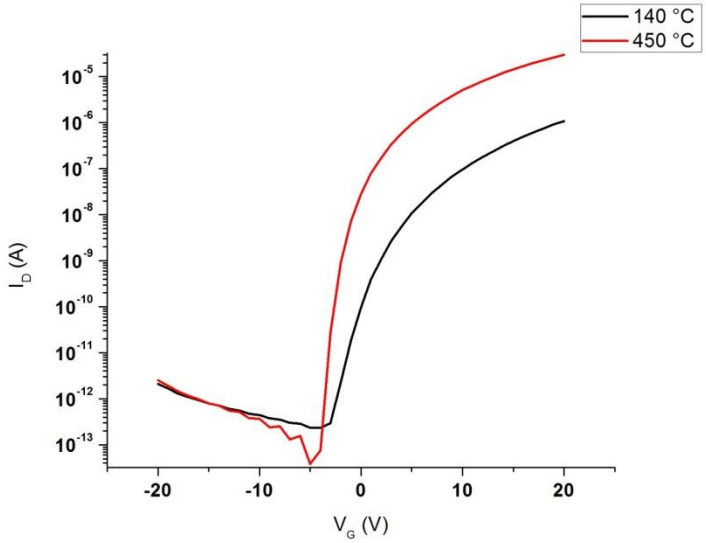

Figure 3.1.18 I-V transfer curves of GSZO TFTs annealed at 140 °C for 3 hours and 450 °C for 1 hour.

Table 3.1.14 *Electrical characteristics of TFTs annealed at 140 °C for 3 hours and 450 °C for 1 hour.*

Annealing Temperature	I_{ON} (A)	$I_{ON/OFF}$	V_{ON} (V)	SS (V/dec)
140 °C	10^{-7}	10^{6}	-2	1.1
450 °C	10^{-5}	10^{9}	-3.5	0.4

Table 3.1.15 *Atomic percentage of 15 nm GSZO films annealed at 140 °C for 3 hours and 450 °C for 1 hour.*

Annealing Temperature	O-(Zn,Ga,Sn)	Cl	Zn	Ga	Sn
140 °C Surface	53.6	1.0	41.1	2.2	2.2
140 °C Sputtered	47.7	0.1	46.6	4.6	1.0
450 °C Surface	58.7	0.3	37.0	1.6	2.3
450 °C Sputtered	43.6	0.0	50.8	4.3	1.3

Table 3.1.16 *O-1s related relative percentage of 15 nm GSZO films annealed at 140 °C for 3 hours and 450 °C for 1 hour.*

Annealing Temperature	O Relative %			Binding Energy (eV)		
	OI	OII	OIII	OI	OII	OIII
140 °C Surface	61	34	5	530.2	531.7	532.7
140 °C Sputtered	76	24	0	530.3	531.7	532.7
450 °C Surface	58	35	7	530.3	531.8	532.7
450 °C Sputtered	86	14	0	530.3	531.7	532.7

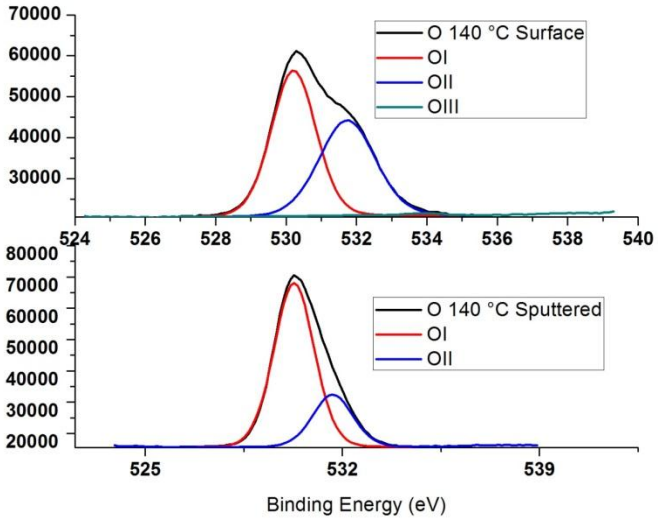

Figure 3.1.19 XPS spectra of O ions in GSZO films annealed at 140 °C for 3 hours.

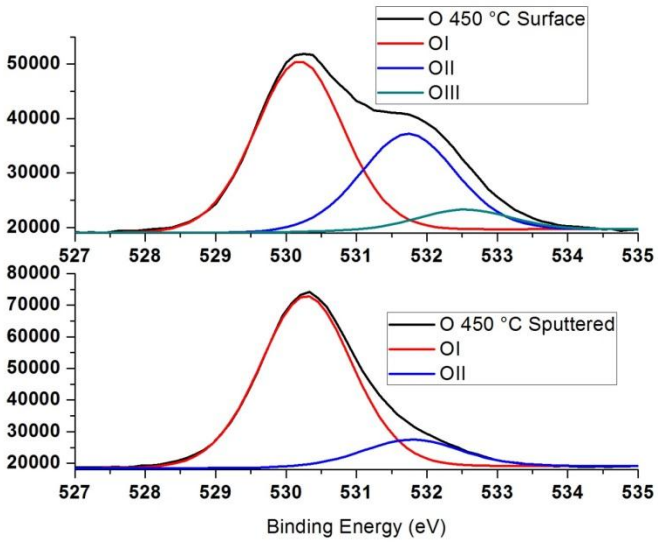

Figure 3.1.20 XPS spectra of O ions in GSZO films annealed at 450 °C for 1 hour.

Table 3.1.17 *Sn related relative percentage of 15 nm GSZO films annealed at 140 °C for 3 hours and 450 °C for 1 hour.*

Annealing Temperature	Sn Relative%			Binding Energy (eV)		
	Sn^{2+}	Sn^{4+}	Sn^{0}	Sn^{2+}	Sn^{4+}	Sn^{0}
140 °C Surface	14.1	85.9	0	486.2	486.8	0
140 °C Sputtered	74.6	25.4	11.9	486.3	487.1	484.5
450 °C Surface	28.1	71.9	0	486.2	486.8	0
450 °C Sputtered	42.6	57.4	0	486.2	486.8	0

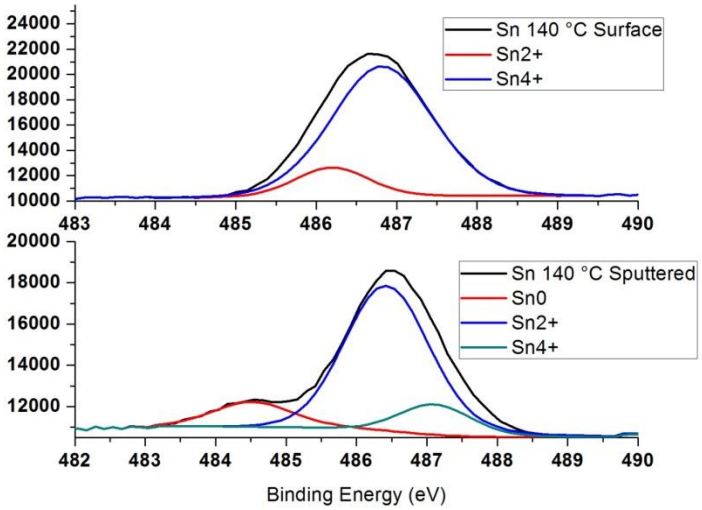

Figure 3.1.21 XPS spectra of Sn ions in GSZO films annealed at 140 °C 3 hours.

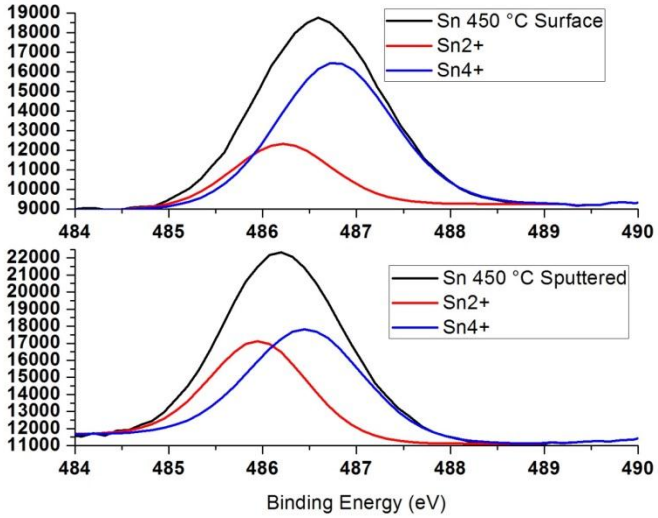

Figure 3.1.22 XPS spectra of Sn ions in GSZO films annealed at 450 °C for 1 hour.

v. Hysteresis

Hysteresis measurements were taken to observe the switching stability of the devices as a function of annealing duration. TFTs with 10 nm GSZO channels were annealed for either 3, 1, or 0 hours in air. For these devices, V_{ON} is the voltage at which ID= 10-10 A with the change in V_{ON} shown and electrical characteristics presented in Figure 3.1.23 and Table 3.1.18. It can be seen that the area between the forward and reverse I-V transfer curves reduces as annealing duration increases with ΔV_{ON} decreasing from 5-0.9 V. Along with a reduction in hysteresis is the absence of ridges in the I-V curves resulting in smoother curves as annealing duration increases.

Table 3.1.18 *Change in ΔV_{ON} as annealing duration increases.*

Annealing Duration (Hr)	ΔV_{ON}
0	5
1	1.1
3	0.9

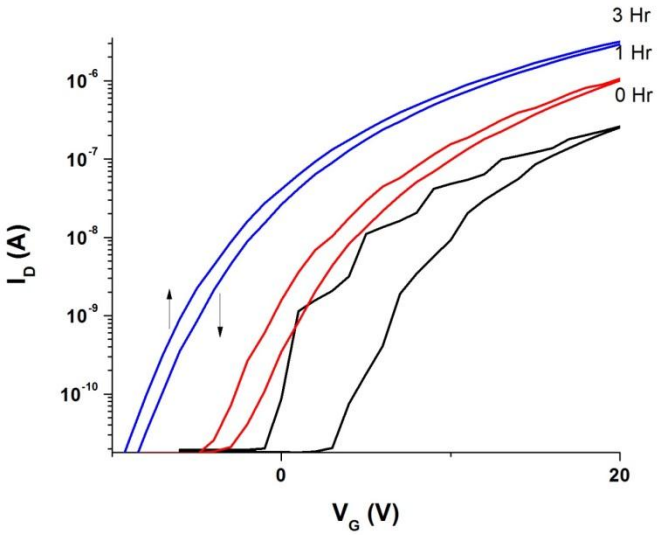

Figure 3.1.23 Transfer characteristics of TFTs annealed for different durations revealing hysteresis changes.

vi. Discussions for Sections (i) – (v)

50 °C Deposited Films

Continuing the research of work from our earlier group, subsequent 30 nm films were deposited at 50 °C in a 5 mTorr deposition pressure. Our previous reports on GSZO films were annealed at 250 °C which is too high a temperature to fabricate TFTs on PEN. Therefore the effect of reducing the annealing temperature was examined by annealing GSZO films at 140 °C for 1 hour and fabricating bottom-gate TFTs.

Lower Annealing Temperature

TFTs with GSZO films annealed at 250 °C have been compared to GSZO TFTs annealed at a lower temperature of 140 °C (Table 3.1.1) to examine the deleterious effects of lowering annealing temperatures. Overall device performance degraded with the lowering of the

annealing temperature, showing a reduction in $I_{ON/OFF}$ and I_{ON} by 1 order of magnitude and an increase in SS x4. Such a large increase in SS is either associated with either a dense increase in carrier concentration or D_{it}. Since the 140 °C device showed a decrease in I_D by an order of magnitude it is reasonable to assume that the lower annealed GSZO film has a higher concentration of D_{it} than the 250 °C. Low quality film adhesion and high density defects are believed to be the source of device degradation since it is well-known that increasing annealing temperature improves adhesion of the semiconductor/insulator interface along with local atomic rearrangement and metal bonding.

Annealing Duration

To sustain low annealing and processing temperatures suitable for flexible substrates, the effect of longer annealing duration was examined (Table 3.1.2 and Figure 3.1.1). The results clearly indicate improvement in the TFT performance with an improvement in I_D and $I_{ON/OFF}$ an order of magnitude with a minimal effect on I_{OFF}. SS improved by reducing by half and an increase in μ_{FE} by 2 orders of magnitude. Increased channel conductivity caused a negative shift in V_{ON} from -2.5 V to -9.5 V which is the result of an increase in carrier concentration. This, in turn, is the cause of the enhanced the field effect mobility by 2 orders of magnitude. This is consistent with the commonly known characteristic within AOS layers that an increase in carrier concentration results in corresponding increase in mobility. PCA devices showed an improvement in device performance with SS reducing to 2 V/dec and μ_{FE} increasing for each sample (Table 3.1.3). This improvement in device performance is likely due to an improvement in film adhesion at the GSZO/SiO_2 interface since the devices were placed directly on a hot plate. Significant reduction in the hysteresis of the transfer characteristics with annealing duration (Figure 3.1.23) reveals the decrease in trap density at the semiconductor/insulator interface.

XPS analysis shows annealing duration to have very little effect on the atomic composition of the film however an increase in Sn^{4+} at.% can be seen in devices with GSZO films annealed for 10 hours (Table 3.1.6 and Figure 3.1.4-Figure 3.1.5). This shows that along with increasing annealing temperature, longer annealing durations cause an increase in Sn^{4+} at.% due to local rearrangement of O atoms near Sn^{2+} atoms causing a change in oxidation state to Sn^{4+}. The binding energy 484.5 eV can be attributed to the metallic Sn^0 atoms which are known to increase the conductivity of ZnO based films. Though it can be seen from Table 3.1.17 that increasing annealing temperatures removes Sn^0, annealing duration of 10 hours still has traces of the Sn^0 metal indicating lack of energy needed by oxygen atoms to migrate to nearby metal cation. The above improvement in the TFT parameters in conjunction with invariant I_{OFF} strongly suggests that longer annealing is effective in annihilating only the shallow traps.

100 °C Deposited Films

All subsequent GSZO films were deposited at 100 °C in preparation for GSZO TFTs. A comparison of 50 °C and 100 °C was taken to examine the electrical and compositional effects by increasing the deposition temperature. TFTs with GSZO films of different thicknesses were fabricated to investigate the electrical and morphological properties as film thickness increases. Finally we investigated the effects of high-temperature annealing by comparing low-temperature TFTs annealed at 140 °C to high-temperature TFTs annealed at 450 °C since high-temperature annealed TFTs yielded better TFT performance.

Low-Temperature Deposition vs. High-Temperature Deposition

Increasing the deposition temperature from 50 °C to 100 °C provided an improvement in device performance due to the enhancement in I_D by an order of magnitude and $I_{ON/OFF}$ by 2 orders of magnitude however V_{ON} shifted negatively by ~4 V and SS slightly degraded to 0.7 V/dec (Table 3.1.7 and Figure 3.1.6). From these it is evident that an increase in deposition temperature caused an increase in carrier concentration which is the cause of the changes in device performance. This increase in carrier concentration is likely due to the concentration of Sn^0 in the bulk of the 100 °C deposited film since it is known to increase carrier concentration. The high concentration of Sn0 coupled with the Sn^{4+} at.% are likely causes of the improvement in μ_{FE} since Sn^{4+} has the $[Kr](4d)_{10}(5s)_0$ electronic configuration needed to improve electron mobility.

Increasing the deposition temperature from 50 °C to 100 °C had little effect on the bulk atomic composition (Table 3.1.8) however traces of hydroxyl (O-H) molecules can be found in the bulk of the 50 °C film. An increase in Sn^{4+} at.% can be found in both the surface and bulk of the 100 °C film, likely causing an improvement in device performance since Sn^{4+} $[Kr](4d)_{10}(5s)_0$ electronic configuration is known to improve electron mobility.

Comparison with Higher Annealed Temperature Device

Using this optimized deposition temperature of 100 °C we have attempted to compare the low annealed temperature device with the device fabricated with the channel annealed at higher temperature of 450 °C to ascertain if there is any valence change in the elements or coordination that is responsible for the observed large differences in these two sets of devices (Table 3.1.14-Table 3.1.17 and Figure 3.1.18-Figure 3.1.22). XPS characterization show a slightly less O-rich oxide surface layer with annealing temperature reduction however more O-rich in the bulk of the film. There appears to be very little change in Ga at.% and Sn at.% with annealing temperature reduction. OI (530.2 eV) is attributed to the oxygen bound with cations, OII (531.7 eV) is attributed to O^{2-} ions in oxygen-deficient regions and OIII (532 eV) is usually attributed to the presence of loosely bound oxygen on the surface of the GSZO film, belonging to a specific species, e.g., –CO, adsorbed H-O or adsorbed O within the amorphous film. The de-convoluted O 1s spectra peaks show a decrease in OI at.% and an increase in OII at.% with decreasing annealing temperature. The OIII at.% is a low percentage on the surface of the film however it vanishes within the bulk. As stated above, these are loosely bound O-related defects usually absorbed onto the surface of the film and are not seen within the bulk. The increase in OII at.% with decreasing annealing temperature shows an increase in oxygen vacancies (VO) which is expected since oxygen interstitials (OI) do not have sufficient thermal energy to migrate and fill such vacancies. Many of these VO's can be shallow defect locations (VO^{2+}) which are known to capture electrons from the conduction band (CBM) and degrade device performance(Table 3.1.14). XPS characterization show a high density of Sn^{4+} on the surface of both films however this concentration is significantly reduced in the bulk of the 140 °C film. Since the films were annealed in air and it is well known that Sn^{4+} is created by the migration of O atoms to nearby Sn^{2+} ions[13] it is understandable that a higher concentration of Sn^{4+} can be seen on the surface and reduces within the bulk. Since decreasing annealing temperature causes less atomic rearrangement in the film it is less likely that nearby O atoms will cause Sn^{2+} to become Sn^{4+}. It is not understood why traces of the metallic Sn^0 can be found on the surface of the film however they are quickly oxidized once annealed in air likely due to oxygen

absorption. Thus higher concentration of Sn^{4+} configuration is responsible for the superior characteristics exhibited by the TFTs annealed at higher temperatures.

Channel Thickness

TFT performance improved with the reduction in the channel thickness as shown in (Table 3.1.11-Table 3.1.12 and Figure 3.1.11-Figure 3.1.14), which is discussed below.

(a) Improvement in SS, μ_{FE} and I_{OFF}:

First, the active channel layer thickness extends only up to a couple of nm from the gate oxide/active channel interface; and secondly, the thinner channel layer is more dense and exhibit smoother interface as inferred from XRR data Table 3.1.11, leading to improved SS and carrier mobility. Hence the additional bulk channel layer in a thicker channel impacts the TFT performance only adversely by contributing to the background carrier concentration resulting in a large negative V_{ON} shift with enhanced I_{OFF}. This increase in I_{OFF} can also be inferred from Equation 2 where I_{OFF} is proportional to channel thickness, t_{CH}.

$$I_{OFF} = \frac{t_{CH} W \sigma V_{DS}}{L} \qquad (2)$$

where t_{CH} is the GSZO channel thickness, W is device width, σ is film conductivity, V_{DS} is the voltage between the drain and source electrodes and L is device length

(b) Positive shift in V_{ON} close to the origin and reduction in I_D:

Furthermore, the surface sensitivity to the oxygen adsorption from the ambient forming different strongly bonded negative ionic species such as O^{2-}, O^- etc aids in creating the depletion region at the surface. In a thinner channel this represents a significant portion of the channel layer, thereby restricting the channel conductivity. This explains the decrease in drain current observed for lower channel thickness. Hence fully depleted region is formed readily in the thinner channel for small gate voltages thus leading to positive shift in V_{ON}. This is also further attested by the C-V profile variation with channel thickness Figure 3.1.12, namely a positive shift in the C-V characteristics accompanied with a sharper transition between the different regions of operation and enhanced accumulation capacitance with thinner channel. RBS characterization show very little change in atomic composition with channel thickness.

Though most of the behavior of GSZO TFTs with annealing and deposition temperature is similar to those observed in IGZO TFT, the salient differences between the two systems seem to lie in the quality of the channel layer at lower thickness. Lower channel thickness in GSZO seems to result in denser layers and smoother interfaces, while IGZO reports seem to be unclear[14,15]. Thus the lower thickness seems to be potentially more advantageous in the case of GSZO TFT.

PCA tests provided improvements in V_{ON} for the 20 nm and 10 nm devices by exhibiting positive shifts. This is likely due to the dehydration of adsorbed water at the surface and within the film. The negative V_{ON} shift of the 30 nm device is due to the increased background carrier concentration which increases with channel thickness. This is evident in the increased I_{OFF} for the 30 nm device which degraded the $I_{ON/OFF}$ ratio. Since it is understood that SS is negatively affected by increased carrier concentration, as device thickness decreases, the SS improves thus suggesting carrier concentration to be dominantly effected by PCA.

Though the overall performance of GSZO transistor with processing temperature under 150 °C is still inferior to those obtained in the IGZO based TFT however an improvement has been

made and there is a potential for further improvement by fine tuning of the processing parameters as well as the target composition and possibly a passivation layer.

3.1(b) Effect of Deposition Pressure

Dependence of GSZO TFT performances as a function of Ar/O_2 pressures during the channel deposition was studied. GSZO TFTs were characterized using I-V and C-V measurements.

The optical properties of the GSZO thin films deposited under different pressures were studied by absorption measurements while surface and interface morphologies were examined using XRR and AFM measurements. Atomic composition analysis was also conducted by XPS characterizations.

(i) I-V Characterization

Table 3.1.19 and Figure 3.1.24 show the transfer I-V curves of devices with active layers deposited with increasing pressures from 1-10 mTorr. Subsequently all films were annealed at 140 °C for 3 hours in air. With an increase in deposition pressure it is observed that IOFF and I_{ON} decreases, V_{ON} shifts positively and $I_{ON/OFF}$ increases. However the SS (1.12 V/dec) and hysteresis (0.9 V) is lowest for the 5 mTorr device. Hysteresis values were found by calculating the change in V_{ON} (ΔV_{ON} at I_D=5x10^{-12} A) from the forward to reverse I_D sweep. Though the 10 mTorr film has the largest $I_{ON/OFF}$ of 5.2x10^{-6} A it also has the largest hysteresis (2 V). D_{It} is the density of interface traps calculated by the SS (Equation 3) where k-Boltzmann's constant, T-temperature (K), C'-capacitance per unit area of SiO_2 and q-electric charge constant.

$$D_{It} = \left[\left(\frac{Log(e)SS}{kT}\right) - 1\right]\frac{C\prime}{q} \qquad (3)$$

The D_{It} calculations show the 1 mTorr exhibiting higher interface traps compared to 5 and 10 mTorr devices. Though each device has similar μ_{FE} the 1 mTorr device has the largest with 0.43 $cm^2/V{\cdot}s$. The slope of the I-V output curves at V_{GS}=20 V and V_{DS}=15-20 V (Figure 3.1.25) was calculated to examine the saturation of the devices. It is shown that the saturation of the devices improves with increasing deposition pressure.

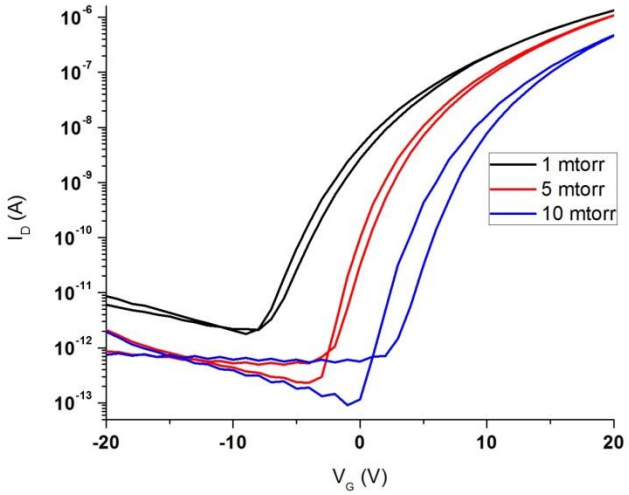

Figure 3.1.24 I-V transfer curves of devices with GSZO channel layers deposited at 1, 5 and 10 mTorr.

Table 3.1.19 *Electrical parameters of GSZO TFTs with channel layers deposited at 1, 5 and 10 mTorr.*

	1 mTorr	5 mTorr	10 mTorr
μ_{FE} ($cm^2/V.s$)	0.43	0.2	0.3
SS (V/dec)	1.8	1.1	1.2
V_{ON} (V)	-16	-1.8	2
I_{ON} (A)	$1.3x10^{-6}$	$1.1x10^{-6}$	$4.7x10^{-7}$
I_{OFF} (A)	$1.8x10^{-12}$	$2.3x10^{-13}$	$9.1x10^{-14}$
$I_{ON/OFF}$	$7.4x10^{5}$	$4.7x10^{6}$	$5.2x10^{6}$
ΔV_{ON} (V)	1.3	0.9	2
D_{it} ($cm^{-2}eV^{-1}$)	$5.4x10^{12}$	$3.2x10^{12}$	$3.5x10^{12}$

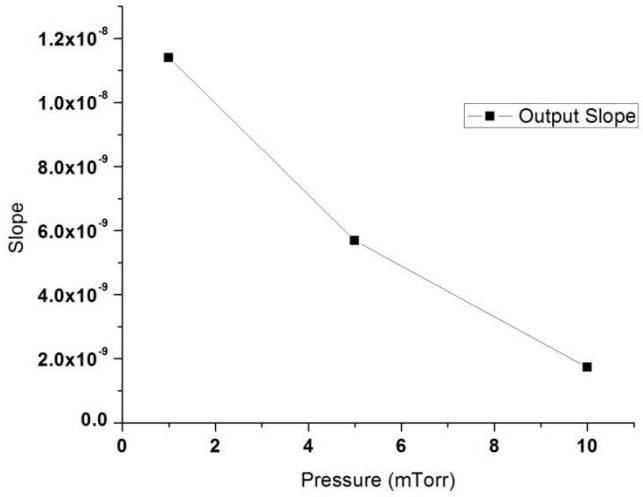

Figure 3.1.25 Slope of I-V output curves at V_{GS}= 20 V and V_{DS}=15-20 V.

After 2 months of exposure to air, device degradation for the 1, 5 and 10 mTorr TFTs was analyzed. The transfer graphs of the devices before and after 2 months are shown in Figure 3.1.26. It was observed that for all devices, the hysteresis vanished and V_{ON} shifted negatively. The I_{OFF} of the 1 and 10 mTorr devices increased after 2 months while the I_{ON} of the respective devices remained the same. In particular, the 1 mTorr device showed a large increase in I_{OFF}, reducing the $I_{ON/OFF}$ from ~10^6 to ~10^3. In contrast, the 5 mTorr device showed only a slight decrease in both I_{ON} and I_{OFF} resulting in no change in $I_{ON/OFF}$.

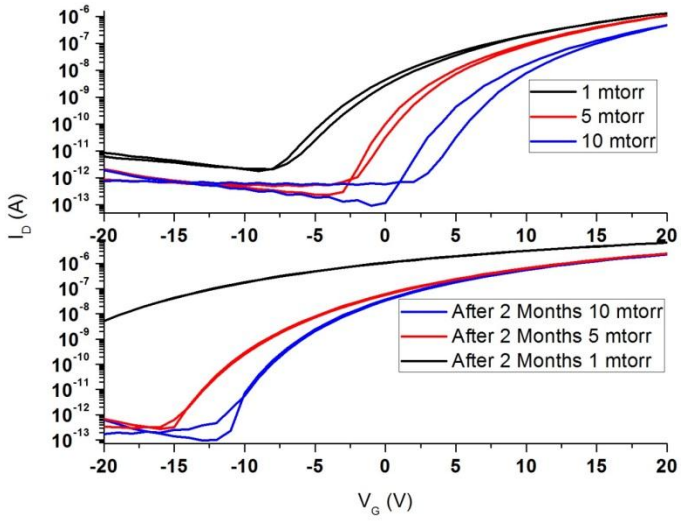

Figure 3.1.26 Transfer plots of the 1, 5 and 10 mTorr devices before and after 2 months of exposure to air.

(ii) C-V Characterization

C-V measurements with increasing deposition pressure taken at increasing frequencies (250-1M Hz) are shown in Figure 3.1.27-Figure 3.1.29. Figure 3.1.30 shows the C-V graphs at 250 Hz for all films superimposed. The flat-band voltage (V_{FB}) is the voltage at which the capacitance begins to increase. It can be seen that V_{FB} shifts positively with increasing deposition pressure (-5 V to 2.4 V). It can be seen that the onset of the accumulation region occurs at smaller V_{GS} voltages and the slope decreases with increasing frequencies. The 10 mTorr device exhibits the largest hysteresis, depletion and accumulation capacitances, The 5 mTorr device has the smallest hysteresis and the largest slope between the depletion and accumulation regions.

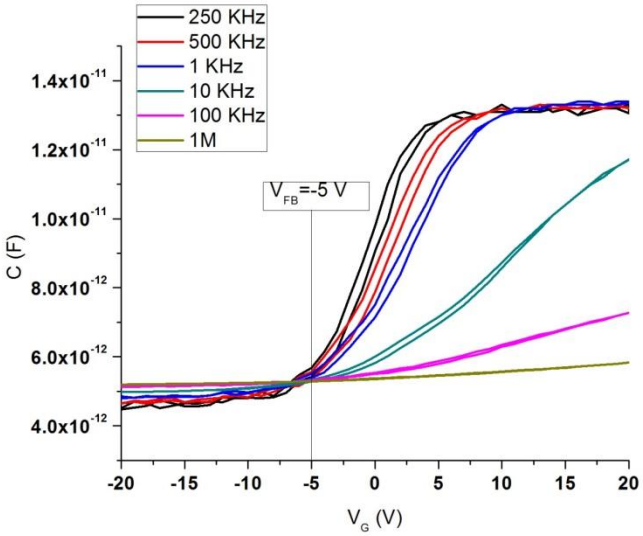

Figure 3.1.27 C-V curves of TFT with GSZO layer deposited at 1 mTorr.

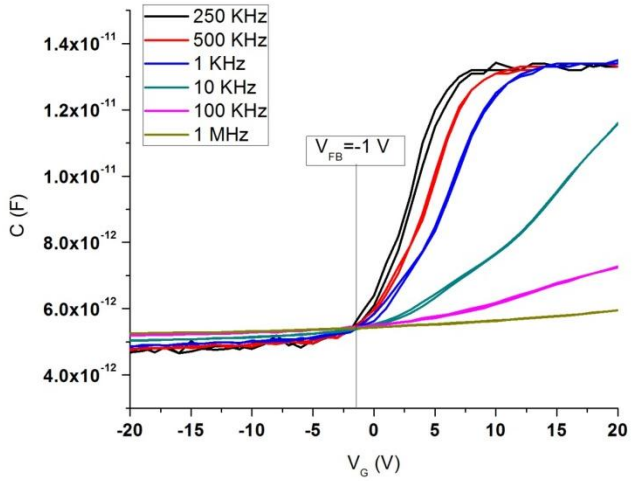

Figure 3.1.28 C-V curves of TFT with GSZO layer deposited at 5 mTorr.

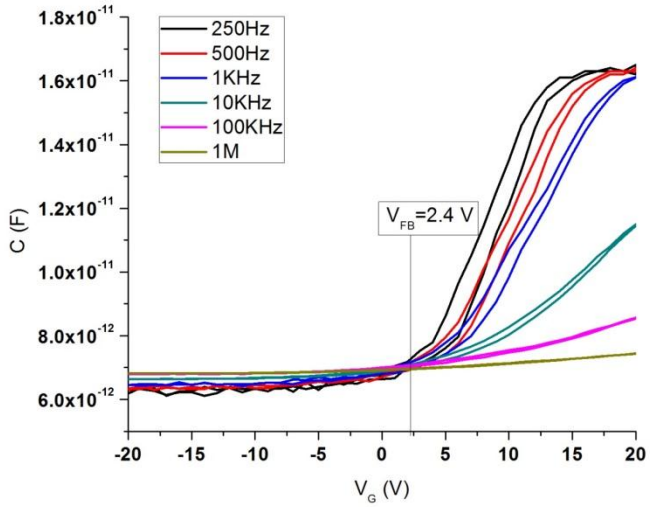

Figure 3.1.29 C-V curves of TFT with GSZO layer deposited at 10 mTorr.

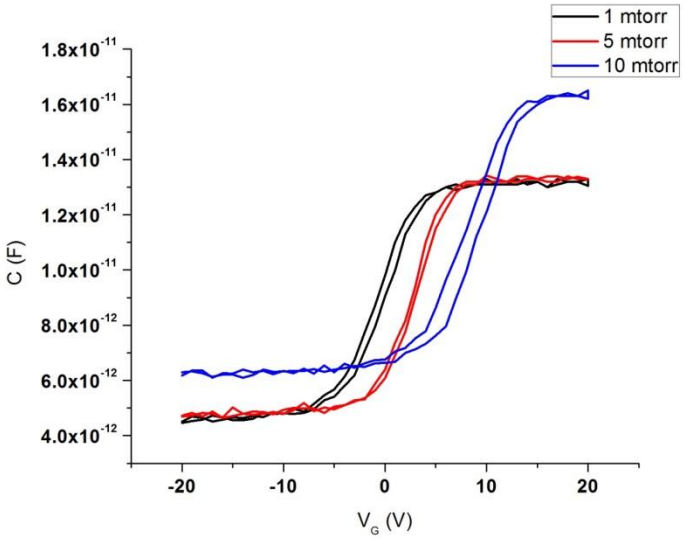

Figure3.1.30 Superposition of C-V curves deposited under different deposition pressures at 250Hz.

(iii) Morphological Characterization: XRR & AFM

To examine the effect of deposition pressure on the surface and interface morphologies of the films XRR and AFM measurements were taken to study the film density and roughness. Table 3.1.20 shows the values for the density, RMS, skew and kurtosis of the films. The skew is

a measure of the height distribution and profile symmetry about the mean line while kurtosis is a measure of the surface sharpness. Figure 3.1.31-Figure 3.1.33 depict AFM images (1 µm x1 µm) of the surface of the films deposited at different operating pressures. It is found that the density of the films increase and the surface root-mean-square roughness (R_{rms}) decreases with deposition pressure. The largest density (7 kg/cm^3) and smallest R_{rms} (19.7 pm) was found in the 10 mTorr film. The 1 mTorr film is the only film with both a positive skew and a negative kurtosis, while the other two films exhibited opposite.

Table 3.1.20 *Film density and surface roughness of films deposited at different pressures as determined from XRR and AFM characterizations.*

Deposition Pressure	Density (kg/cm^3)	R_{rms} (pm)	Skew	Kurtosis
1 mTorr	5.4	35.4	0.068	-0.0354
5 mTorr	6	27.9	-0.917	2.96
10 mTorr	7	19.7	-0.278	1.14

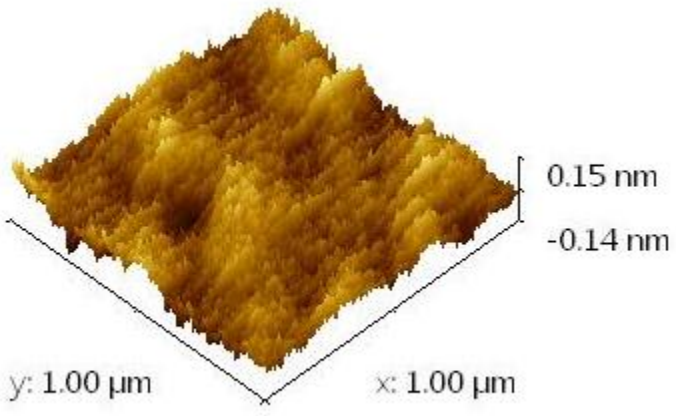

Figure 3.1.31 AFM images of a-GSZO films deposited at 1 mTorr deposition pressure

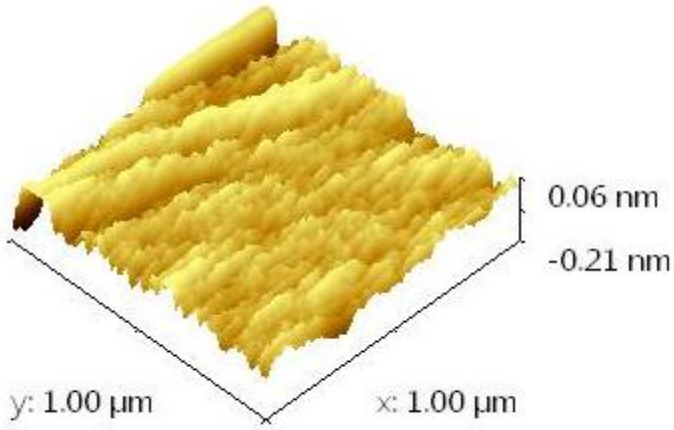

Figure 3.1.32 AFM images of a-GSZO films deposited at 5 mTorr deposition pressure

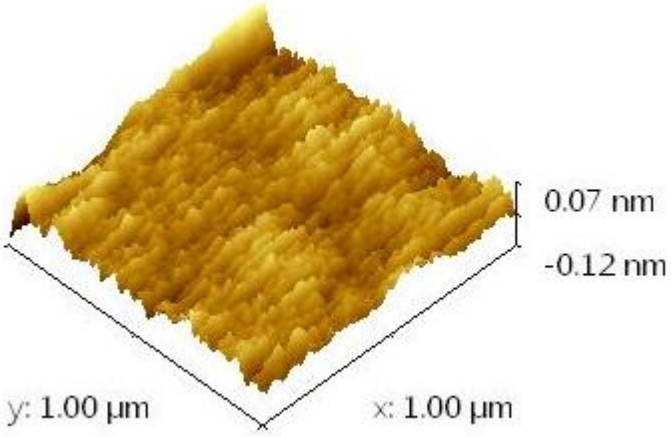

Figure 3.1.33 AFM images of a-GSZO films deposited at 10 mTorr deposition pressure

(iv) Atomic Composition Analysis: XPS

XPS characterization was done on the surface and 5 nm below 15 nm GSZO films deposited at 1, 5 and 10 mTorr pressures to examine the effect of annealing temperature on atomic composition (Table 3.1.21). It can be seen that deposition pressure has little effect on the atomic composition of the films at both the surface and the bulk. Table 3.1.22 and Figure Figure *3.1.34*-Figure 3.1.36 show the O 1s spectra de-convoluted into three peaks of different states, i.e., 530.2 eV (OI), 531.7 eV (OII) and 532.7 eV (OIII). Though the surface of all films have similar at.% ratios the 5 mTorr film shows an increase in OI and decrease in OII at.%. Table 3.1.23 and Figure 3.1.37-Figure 3.1.39 show the Sn relative at.% as a function of annealing temperature. The Sn^{2+} relative at.% within the bulk of the films decrease (84.4 to 23 at.%) causing a dramatic increase in Sn^{4+} relative at.% (15.6 to 77 at.%) with film deposition pressure increase from 1 to 10 mTorr.

To analyze the presence of Zn_I within the GSZO films the Auger $ZnL_3M_{4.5}M_{4.5}$ spectra were investigated with the two Auger peaks at 498 and 494.5 eV attributed to the Zn-O bonds and the Zn_I , respectively. Figure 3.1.40 shows the percentage of Zn_I to Zn-O bonds within the top 5 nm of the GSZO films as a function of pressure which clearly show a decrease in Zn_I with increasing deposition pressure.

Table 3.1.21 *Atomic percentage of 15 nm GSZO films deposited at 1, 5 and 10 mTorr pressures.*

Deposition Pressure	O-(Zn,Ga,Sn)	Cl	Zn	Ga	Sn
1 mTorr Surface	53.3	0.9	40.5	2.8	2.5
1 mTorr Sputtered	44.3	0.1	50.3	4.1	1.2
5 mTorr Surface	53.6	1.0	41.1	2.2	2.2
5 mTorr Sputtered	47.7	0.1	46.6	4.6	1.0
10 mTorr Surface	53.4	1.0	41.0	2.3	2.3
10 mTorr Sputtered	43.8	0.0	50.4	4.4	1.4

Table 3.1.22 *O-1s related relative percentage of 15 nm GSZO films deposited at 1, 5 and 10 mTorr pressures.*

Deposition Pressure	O Relative %			Binding Energy (eV)		
	OI	OII	OIII	OI	OII	OIII
1 mTorr Surface	60	35	6	530.3	531.8	532.8
1 mTorr Sputtered	83	17	1	530.3	531.7	532.7
5 mTorr Surface	61	34	5	530.2	531.7	532.7
5 mTorr Sputtered	76	24	0	530.3	531.7	532.7
10 mTorr Surface	59	34	6	530.3	531.7	532.6
10 mTorr Sputtered	83	17	0	530.2	531.7	532.7

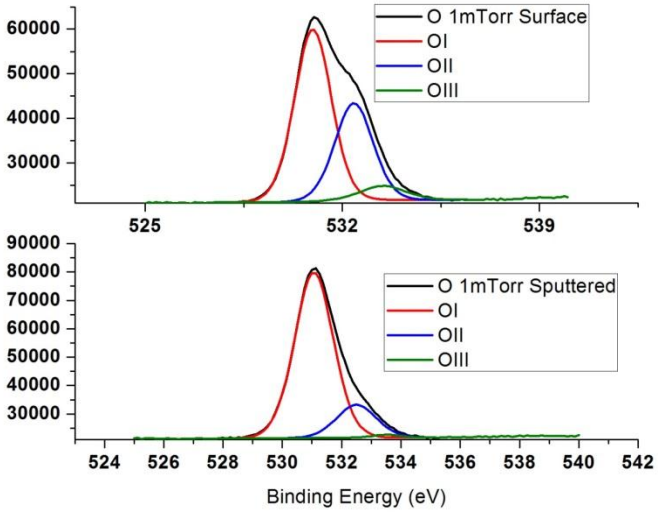

Figure 3.1.34 XPS spectra of O ions in GSZO films deposited at 1 mTorr.

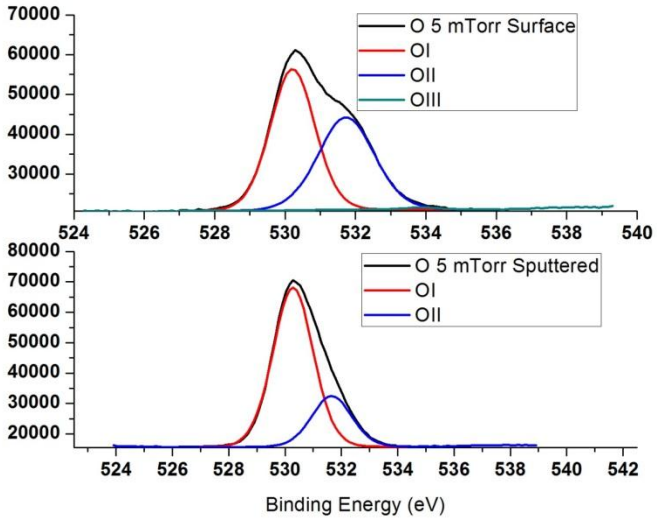

Figure 3.1.35 XPS spectra of O ions in GSZO films deposited at 5 mTorr.

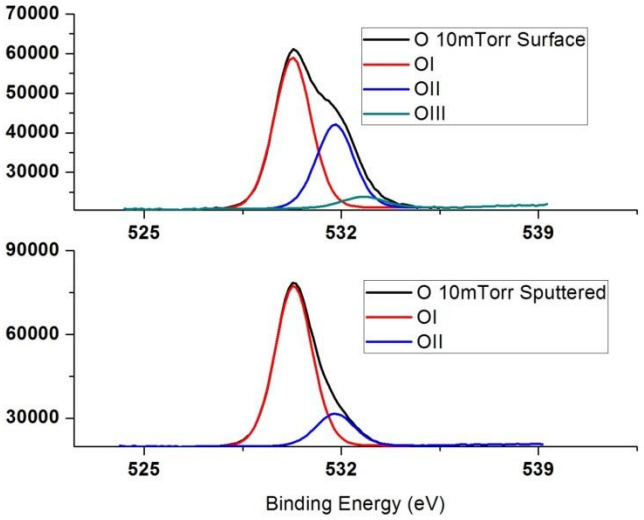

Figure 3.1.36 XPS spectra of O ions in GSZO films deposited at 10 mTorr.

Table 3.1.23 *Sn related relative percentage of 15 nm GSZO films deposited at 1, 5 and 10 mTorr.*

Deposition Pressure	Sn Relative%			Binding Energy (eV)		
	Sn^{2+}	Sn^{4+}	Sn^{0}	Sn^{2+}	Sn^{4+}	Sn0
1 mTorr Surface	25.2	74.8	0	486.2	486.8	0
1 mTorr Sputtered	84.4	15.6	0	486.3	487.1	0
5 mTorr Surface	14.1	85.9	0	486.2	486.8	0
5 mTorr Sputtered	74.6	25.4	11.9	486.3	487.1	484.5
\ 10 mTorr Surface	26.2	73.8	0	486.2	486.8	0
10 mTorr Sputtered	23	77	0	486.4	486.8	0

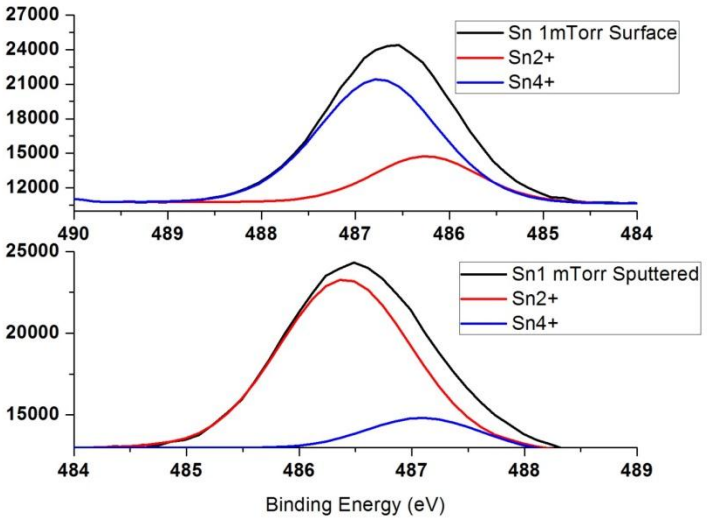

Figure 3.1.37 XPS spectra of Sn ions in GSZO films deposited at 1 mTorr.

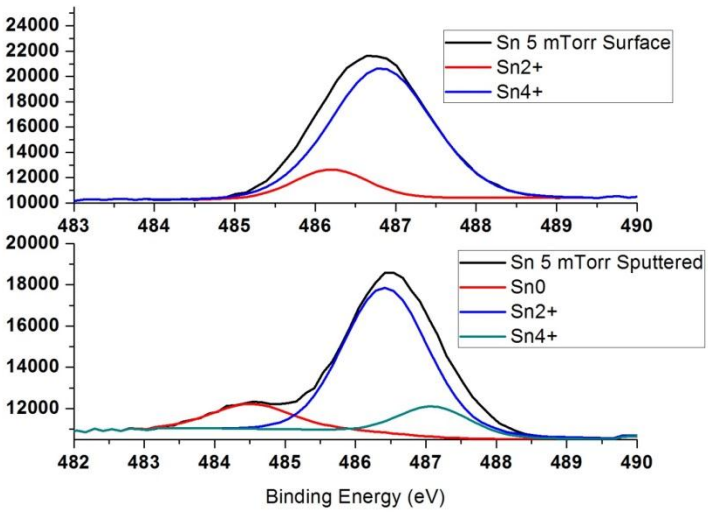

Figure 3.1.38 XPS spectra of Sn ions in GSZO films deposited at 5 mTorr.

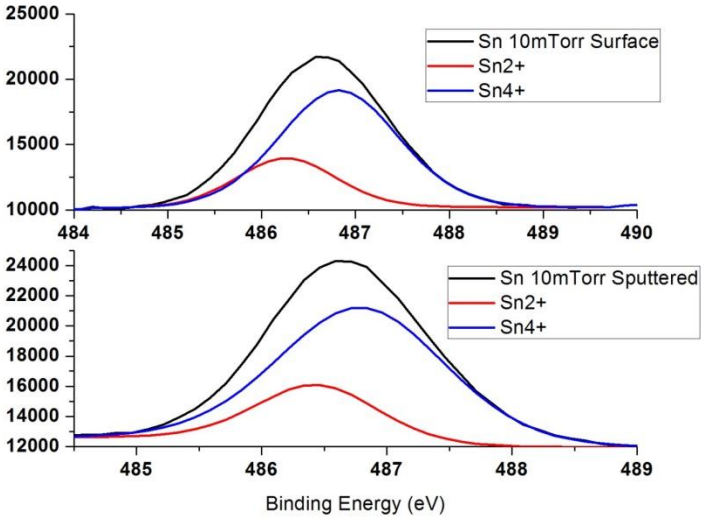

Figure 3.1.39 XPS spectra of Sn ions in GSZO films deposited at 10 mTorr.

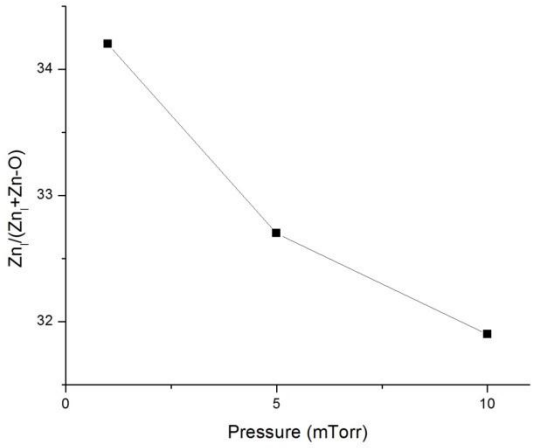

Figure 3.1.40 Percentage of Zn_i in first 5 nm of GSZO film as a function of pressure.

(v) Optical Characterization: Absorption Measurements

To study the optical properties of the a-GSZO films as a function of pressure, transmission measurements were taken to examine the transparency of the films as well as to find the absorption coefficient as a function of photon energy also known as the Tauc plot. The transmission plot is shown in Figure 3.1.41 between 200 nm and 800 nm. The optical gap of the a-GSZO films can be extrapolated by projected the x-intercept of the slope of the absorption coefficient curves. The Tauc plot in Figure 3.1.42 shows the optical gap of the a-GSZO films to be between 3.5-3.51 eV when deposited in pressures between 1 mTorr and 10 mTorr with the latter film exhibiting slightly higher absorption edge.

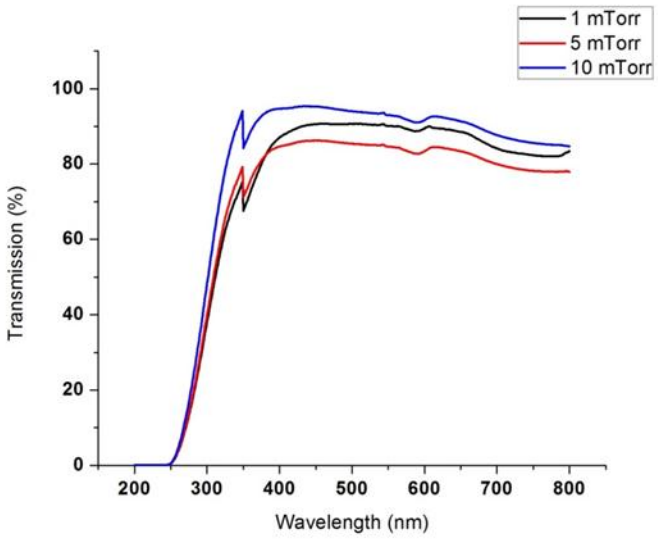

Figure 3.1.41 Transmission plot of films deposited at different operating pressures

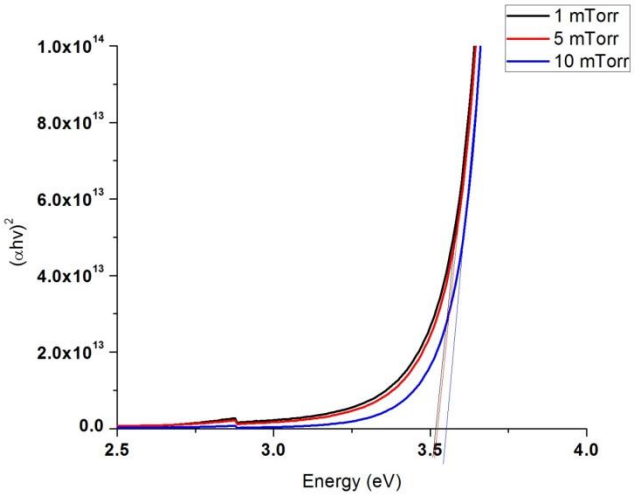

Figure 3.1.42 Optical absorption spectra of a-GSZO films deposited in chamber pressures of 1, 5 and 10 mTorr.

(vi) Discussion on (i)-(v)

TFTs with GSZO active layers deposited at different chamber pressures were compared to examine its effect on device performance. An in-depth systematic analysis was performed to study the electrical, morphological, compositional and optical properties of the GSZO films and devices. These films were 15 nm thick, deposited at 1, 5 and 10 mTorr deposition pressures and annealed at 140 °C for 3 hours.

(a) 1 mTorr device:

The 1 mTorr device showed the largest I_{OFF}, I_{ON} and most negative V_{ON} suggesting the film to be highly conductive. This can be verified by the devices large I_{OFF} from Equation 2. Due to the high conductivity of the film, the carrier mobility of the device was also the greatest at 0.43 $cm^2/V{\cdot}s$ with poor SS (1.8 V/dec) as it is well known that higher mobility is associated with higher carrier concentration and SS is poor for higher carrier concentration and trap density. XRR revealed a highly porous film for the 1 mTorr active layer as compared to the other films. Figure 3.1.31-Figure 3.1.33 show AFM images (1 µm x 1 µm) of the surfaces of GSZO films deposited at different deposition pressures. The R_{rms} values decrease from 35.4 pm to 19.7 pm with increasing deposition pressure. The surface of the film deposited at 10 mTorr was relatively smooth with small aggregates. The 1 mTorr film had the highest surface roughness which was probably due to the high bombardment energy of the ions during channel formation which gives rise to a higher concentration of defects and O-H contaminants. Both the 5 mTorr and 10 mTorr films have skew and positive kurtosis indicating that the surface is more planar with predominant valleys and smoother peaks. The 1 mTorr film has a positive skew with a negative kurtosis indicating a surface with more peaks than valleys. This AFM data agrees with the XRR surface density data in that the 1 mTorr film is more porous with large roughness and sharp peaks. The 1 mTorr TFT is also most sensitive to air showing largest ΔV_{ON} after 2 months.

(b) 5mTorr and 10mTorr devices:

V_{ON} shifted positively with increasing deposition pressures going from -16 V to -1.8 V from 1 to 5 mTorr. A decreased I_{OFF}, I_{ON} and μ_{FE} were also observed suggesting the film is less conductive than the 1 mTorr film. Device performance improved as SS reduced from 1.8 V/dec to 1.1 V/dec, $I_{ON/OFF}$ increased from $7.4x10^5$ to $4.7x10^6$ and ΔV_{ON} decreased from 1.3-0.9 V. This suggests a reduction in CB tail states and a further reduction in I_{OFF} than I_{ON} as the deposition pressure decreased. At 10 mTorr I_{OFF} and I_{ON} also decreased with $I_{ON/OFF}$ increasing even further to $5.2x10^6$ suggesting a less conductive film than the 5 mTorr and improvement in device controllability. The mobility of the 10 mTorr film improved however which is most likely due to the increase in film density which reduces V_o. However the 10 mTorr device showed the greatest hysteresis of 2 V suggesting a large density of traps in the active region of the GSZO layer. This large hysteresis was also observed in the C-V curves shown in Figure 3.1.29. The large density of traps is believed to be due to the high density of oxygen vacancies which are occupied which form deep states as will be inferred later from stability measurements.

Due to the increased channel density of the 10 mTorr film as well as smooth interfaces determined from XRR measurements in comparison to the 1 and 5 mTorr (Table 3.1.20), it is speculated that the electrical permittivity of the oxide is larger in this 10 mTorr device leading to the observed increase in capacitance in both the depletion and accumulation regions. This is found from Equation 4 where ε is the films electrical permittivity, A is the area of the GSZO film and t_{CH} is the thickness of the GSZO layer.

$$C = \frac{\varepsilon A}{t_{CH}} \qquad (4)$$

I_D saturation improved with increasing deposition pressure which is likely due to control of carriers within the film. The 5 mTorr film exhibits the sharpest slope in C-V curves along with the smallest hysteresis suggesting the film has overall less trap states.

Compositional Characterization

a) 1 mTorr and 10 mTorr:

XPS characterizations show the surfaces of both the 1 and 10 mTorr films to be relatively similar with Ga and Sn at. % are relatively low constituting less than 6 % of the film. Traces of the loosely-bound hydroxyl molecules exist both on the surface and within the bulk of the 1 mTorr device. Since hydroxyl molecules acts as donors and passivate defects it is believed that this is the cause for the high concentration of carriers within the 1 mTorr film. The 10 mTorr film had a large at. % of Sn^{4+} in the bulk which would then enhance the percolation conduction through distributed potential barriers around the conduction band edge and improve μ_{FE}[16]. This also explains why the 10 mTorr film has the larger optical gap from absorption measurement data (Figure 3.1.42). All devices showed transparency ≥80 % as shown in Figure 3.1.41.

b) 5 mTorr:

A relatively large atomic concentration of oxygen related defects was observed within the bulk of the 5 mTorr film suggesting the cause of the films 10^6 $I_{ON/OFF}$. However the 5 mTorr film also has the smallest SS and hysteresis which suggests low D_{It} at the semiconductor/insulator interface. Therefore it is believed that these oxygen-related defects are V_O defects constituting deep levels. Being below the Fermi level, they do not affect the mobility of the device. The 5 mTorr film shows higher concentration of Sn^{2+} in the bulk of the

film which has been reported to introduce CB tail states and hence suggesting this to be the cause of the low mobility.

After 2 months of exposure to air, a change in device performances was observed. The 1 mTorr device showed a large increase in I_{OFF} resulting in a decrease in $I_{ON/OFF}$. Since the 1 mTorr device is more porous than the other devices as shown from XRR characterization (Table 3.1.20), this device is more susceptible to absorption of H_2O from the atmosphere. It is well known that H acts as a donor to ZnO based films which would increase the conductivity of the film thus raising I_{OFF}. The 10 mTorr device also showed an increase in I_{OFF} however not as much as the 1 mTorr device. XRR analysis shows the 10 mTorr device to be much denser than the 1 mTorr device resulting in little effect on the devices I_{OFF}. The 5 mTorr device showed a decrease in both I_{ON} and I_{OFF} resulting in no change in $I_{ON/OFF}$. Since a decrease in film conductivity was observed, it is believed the 5 mTorr film absorbed more O_2 than the other devices since they suppress carriers in the active layer[17]. XPS analysis reveals the 5 mTorr device to have the most V_O's in the bulk thus making it more susceptible to oxygen absorption. All device showed a dramatic decrease in hysteresis which shows the suppression of CB tail states which has been shown to be the cause of absorbed H atoms[18]. Therefore it was observed that the 5 mTorr device showed least sensitive to air exposure.

(vii) Conclusion

In conclusion a comprehensive study of the effects of different deposition parameters under low-temperature (<150 °C) conditions on GSZO films and TFTs with bottom-gate configurations were examined which provided a greater insight and allowed manipulation of the film properties. At low temperature annealing the oxygen vacancies, Zn interstitials and adsorption and desorption of oxygen play a dominant role and determines the location, density and nature of the states present in the band gap and the Sn valency. This in turn determines the performance of the devices and the stability.

Bottom-gate GSZO TFTs have been demonstrated on PEN substrates which we believe to be the first reported on these films. Devices with planarization su-8 layer showed improvement in device performance when compared to devices without the su-8 layer likely the result of smoother gate oxide surface roughness. An $I_{ON/OFF}$ ~10^5, SS~0.7 V/dec and μ_{FE}~0.7 $cm^2/V\bullet s$ was achieved with the indium-free TAOS GSZO TFT on PEN. Poor thermal conductivity of the PEN was revealed in the abnormal output electrical characteristics for higher drain currents. These are preliminary data and there is considerable room for improvement in the fabrication of GSZO TFTs on PEN.

3.2. Bottom-Gate TFT on PEN Substrates in Collaboration with RTI Int'l

During this grant period and beyond, RTI Int'l continued to play its role of supporting TFT device fabrication on plastic substrates. Personnel from RTI Int'l still carried out the reactive ion etching for channel formation and the rest of the processing was transitioned to NCA&TSU.

Four different bottom-gate PEN TFTs were fabricated with GSZO active layers and tested for I-V performance: GSZO TFT with a SiO_2 gate insulator on PEN (TFT-A), TFT with a Si_3N_4 gate insulator (TFT-B), TFTs with Si/su-8/Si_3N_4 (TFT-C) and PEN/su-8/SiO_2 (TFT-D). The devices performance and electrical characteristics are shown in Table 3.2.1 and (Figure 3.2.1-Figure 3.2.8). Devices without su-8 yielded lower $I_{ON/OFF}$ ratios of 10^2 and 10^3 with I_D constantly above the current limit needed to establish V_{ON}. Thus for these devices V_{ON} was taken as the voltage at which the I_D begins to increase which is ~-7.5 V and ~-2.5 V for the A and B TFTs. Large SS's above 5 V/dec and smaller µFE below 0.5 $cm^2/V•s$ were also examined for devices without su-8. Improvement in electrical performance was seen for devices with an su-8 planarization layer (TFTs C and D) which showed $I_{ON/OFF}$ of 10^5, SS ~0.6 V/dec and ~0.7 V/dec and μ_{FE} ~0.5 $cm^2/V{\cdot}s$ and ~0.7 $cm^2/V{\cdot}s$. Strong saturation in the output plot of TFT-D can be seen in Figure 3.2.8 however I_D begins to decrease while V_D approaches 20 V. TFT-D was also tested with a decreased time delay (1 s-0.7 s) to examine its effect on the saturation of the output curves (Figure 3.2.9). It can be seen that saturation of output I_D current does not take place as it had when the same device was tested at a slower rate.

Table 3.2.1 *Electrical characteristics of plastic GSZO TFT*

TFT	TFT	I_{ON} (A)	I_{OFF} (A)	$I_{ON/OFF}$	I_G (A)	SS (V/dec)	V_{ON} (V)	μ_{FE} ($cm^2/V{\cdot}s$)
TFT-A	SiO_2/PEN	$3.4x10^{-7}$	$8.3x10^{-10}$	10^2	$4.4x10^{-11}$	8.0	-7.5	0.1
TFT-B	Si_3N_4/PEN	$1.8x10^{-8}$	$1.6x10^{-11}$	10^3	$2.9x10^{-12}$	5.4	-2.5	0.06
TFT-C	Su-8/ Si_3N_4/Si	$2.4x10^{-7}$	$1x10^{-12}$	10^5	$2x10^{-11}$	0.6	0.4	0.5
TFT-D	Su-8/ SiO_2/PEN	$3.1x10^{-7}$	$1x10^{-12}$	10^5	$2x10^{-11}$	0.7	0	0.7

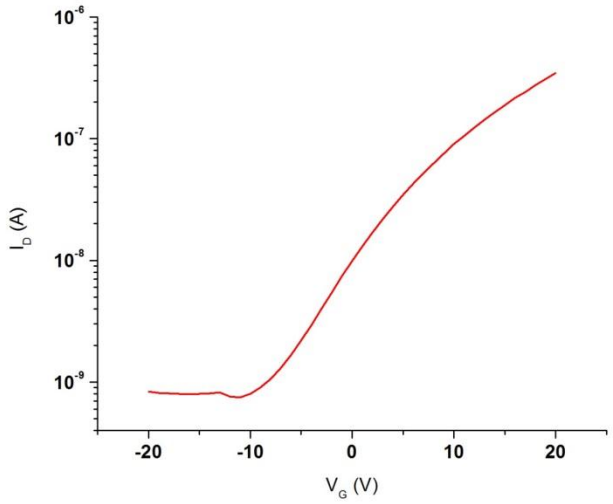

Figure 1 Transfer graph of 15 nm GSZO on PEN with SiO_2.

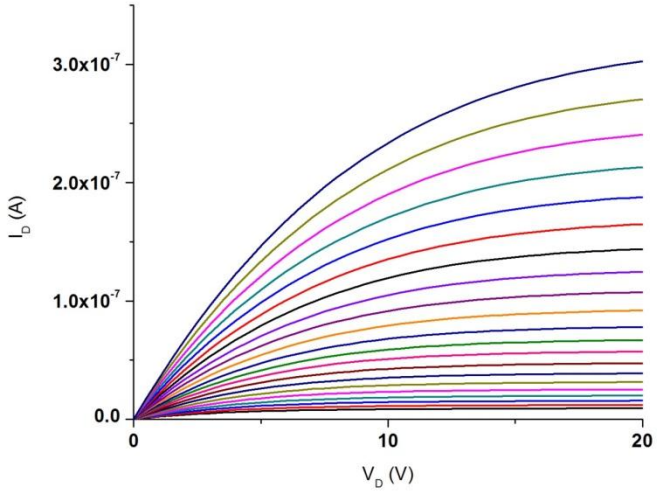

Figure 3.2.2 Output graph of GSZO TFT on plastic substrate with SiO_2 gate oxide.

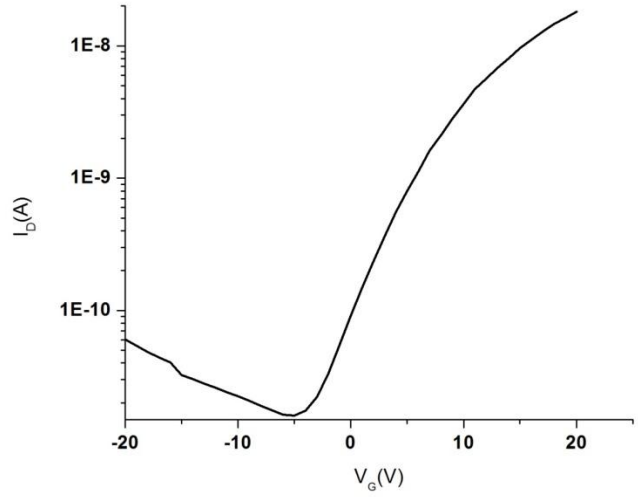

Figure 3.2.3 Transfer graph of 15 nm GSZO on PEN with Si_3N_4.

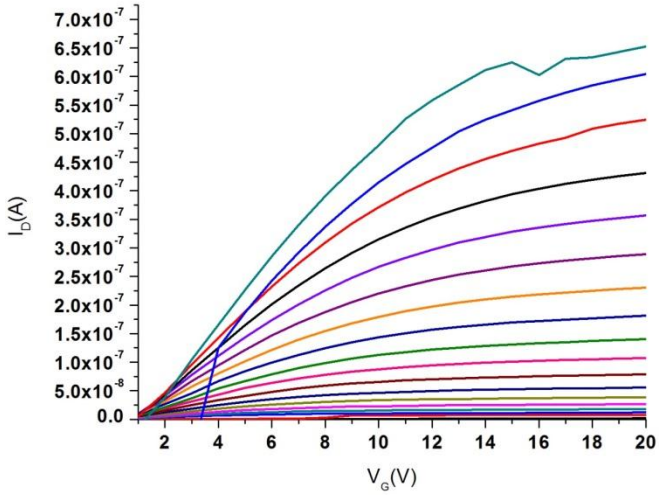

Figure 3.2.4 Transfer graph of 15 nm GSZO on PEN with Si_3N_4

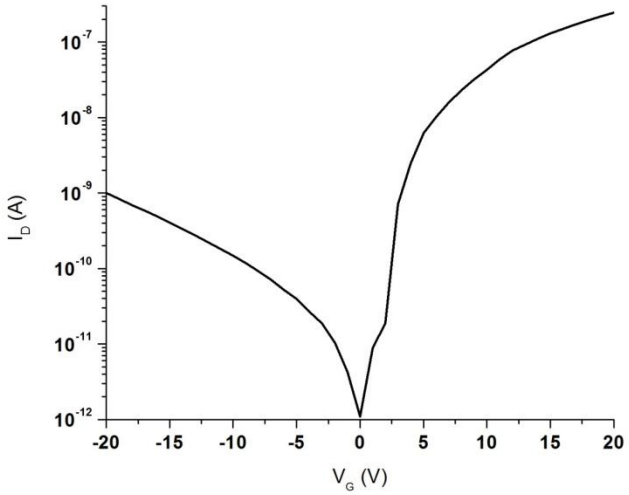

Figure 3.2.5 Transfer graph of 15 nm GSZO on Si with 5 mm of Su8.

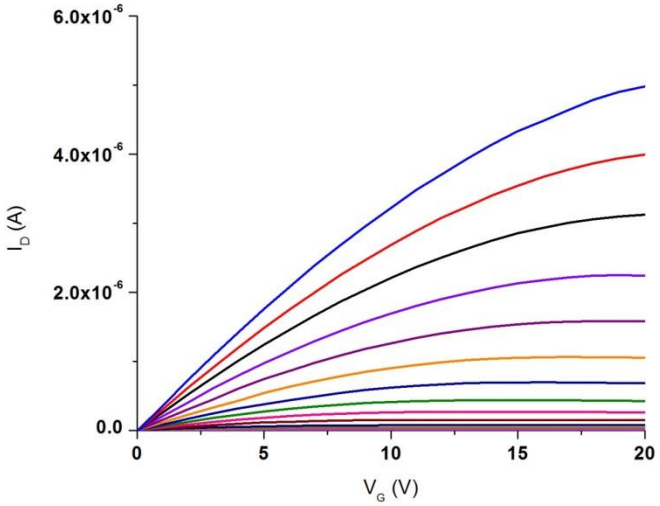

Figure 3.2.6 Output graph of 15 nm GSZO on Si with 5 mm of Su8.

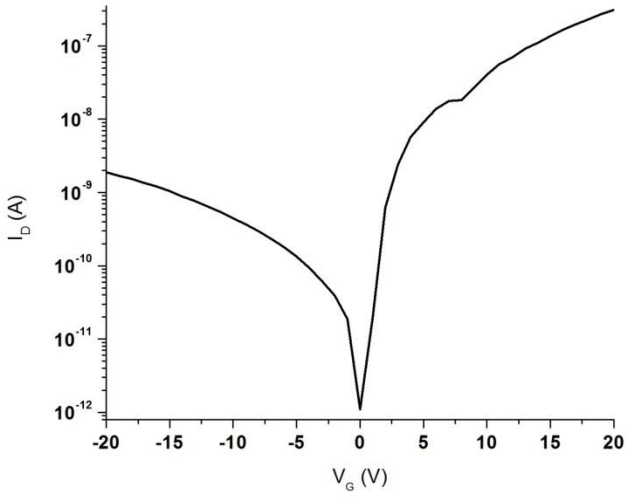

Figure 3.2.7 Transfer graph of Su8/SiO_2 GSZO TFT on PEN

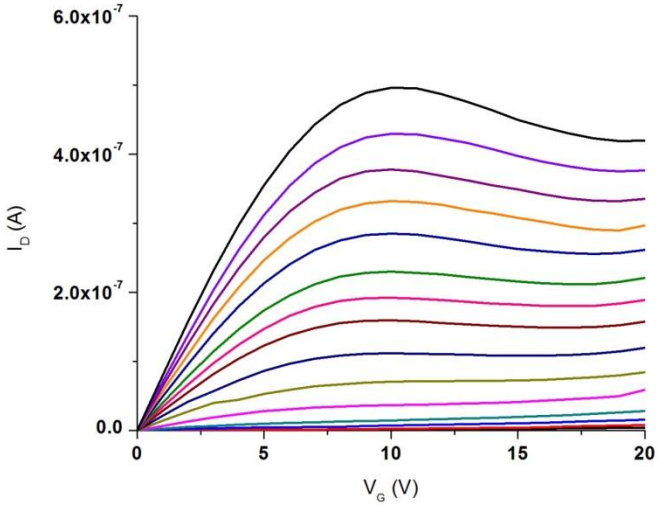

Figure 3.2.8 Output graph of Su8/SiO_2 GSZO TFT on PEN measured with normal 1 s delay.

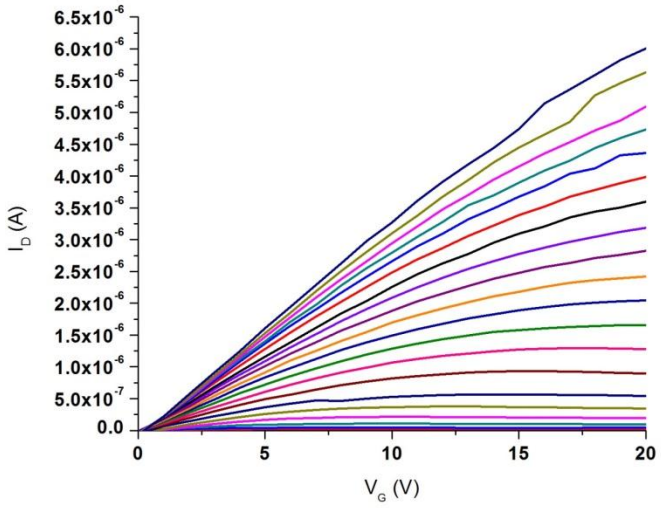

Figure 3.2.9 Output graph of Su8/SiO_2 GSZO TFT on PEN measured with faster 0.7 s delay.

TFTs A and B exhibit poor TFT performance with $I_{ON/OFF}$ ~10^2 and 10^3 with relatively large SS's of 8 V/dec and 5.4 V/dec. The substandard SS performance of the devices suggests a large density of shallow traps near the CBM. Also degrading the SS may be the high conductivity of the films (Equation 3) due to the relatively large I_{OFF} of 10^{10} and 10^{11} as compared to devices on Si (~10^{13}) [19]. Devices C and D, which contained an su-8 planarization layer showed large improvements in $I_{ON/OFF}$ (10^5), SS (0.6 V/dec and 0.7 V/dec) and μ_{FE} (0.5 $cm^2/V{\cdot}s$ and 0.7 $cm^2/V{\cdot}s$). It is well known that su-8 serving as a planarization layer reduces surface roughness of the PEN and the PECVD deposited gate oxide[20]. This is likely the cause of the large improvement in μ_{FE} which is degraded with increased surface roughness scattering. Both devices show low I_{OFF} current near 0 V however I_D increases nearly 3 orders of magnitude upon negative V_{GS} sweep. This increase in carrier concentration is likely due to the presence of holes in the films since the gate insulators were PECVD grown instead of thermally oxidized TFT-D exhibited negative slope in saturation region of the I-V output characteristics suggesting a decrease in μ_{FE}. This is characteristic of the device where the temperature has increased as it occurs only for large currents with V_D and V_G approaching high voltages (15-20 V). The lower PEN thermal conductivity does not allow the dissipation of heat readily at high currents leading to the heating of the device and mobility degradation. To confirm, TFT-D was then tested with decreased time delay and the output saturation and indeed μ_{FE} degradation did not occur.

In conclusion, TFTs with 15 nm GSZO films deposited at an increased deposition temperature (100 °C), chamber pressure of 5 mTorr and annealing duration of 3 hours were shown to produce the best TFTs for plastic substrates. Bottom-gate TFTs on PEN with su-8 planarization layer produced good TFT performance comparable to IGZO TFTs ($I_{ON/OFF}$ ~10^5, SS ~0.7 and µFE ~0.7 $cm^2/V{\bullet}s$).

3.3 TFT Fabricated on Si at Higher Annealing Temperature of 450°C

In this section the focus is on GSZO TFTs on Si with the channel layers annealed up to 450 °C. GSZO films were deposited at 100 ^{o}C. The effects of different deposition contacts mainly Al and Ti/Au contacts, the effect of oxygen flow and the decrease in the active layer thickness on the TFT performance are presented. Further enhancement of the GSZO TFT performance by carrying out post deposition treatment including post oxygen annealing and exposing the device to N_2+H_2.

(a) Annealing Temperature

This study focussed on the high temperature annealing of 450 °C which have a drastic improvement in the characteristic performance of the device. Table 3.3.1 summarizes the electrical characteristics of the TFTs with the low and high temperature annealing. With increasing annealing temperature the drain current and the on/off ratio has increased by 2 orders of magnitude and SS decreased by 5 times. It is evident that the carrier concentration has significantly increased due to increasing annealing temperature.

Table 1.3.1 *Comparison between low and high temperature annealing*

Annealing Temperature (°C)	I_D	Ion/Ioff	V_{ON}	SS
140	10^{-8}	10^{4}	-1	4
450	10^{-6}	10^{6}	-6	0.8

The I-V plot has been plotted in Figure 3.3.1. This drastic improvement at higher annealing temperature as discussed earlier is due to the enhancement of Sn^{4+} content as determined from XPS data earlier in section 3.1(a)-iv. This is the reason why at higher annealing temperature there are more concentration of Sn^{4+} and hence Sn is a suitable candidate for replacing Indium.

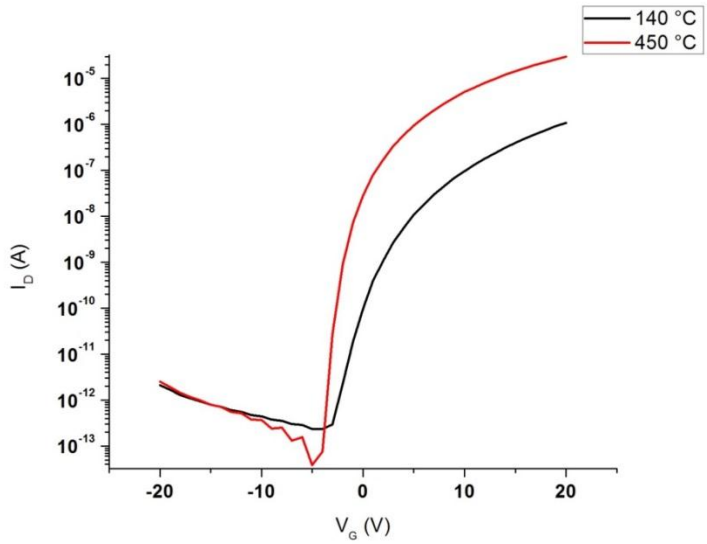

Figure 3.3.1. I-V plot for 140 °C and 450 °C annealed

(b) Effects of Deposition Contacts

The effects of different S/D contacts deposited by E-Beam on the performance of the TFTs were investigated. Two contacts examined were: Al and Ti/Au with a thickness of 100 nm and 20/100 nm respectively. The I-V plot, output plot, and electrical characteristics are illustrated in Figure 3.3.2, Figure 3.3.3 and Table 3.3.2, respectively. Both TFTs exhibit good overall performance with Al contact slightly better drain current, $I_{ON/OFF}$ ratio, V_T and a field-effect mobility of 3.4 cm^2/Vs. The output characteristics of the two devices also exhibit good Ohmic contact property and current saturation behaviors. The I_D has increased with Al contact. This increase in I_D can be understood in the same manner as conventional metal-oxide-semiconductor transistor structures, which is the reduction of parasitic contact resistance between the electrode and channel layer.

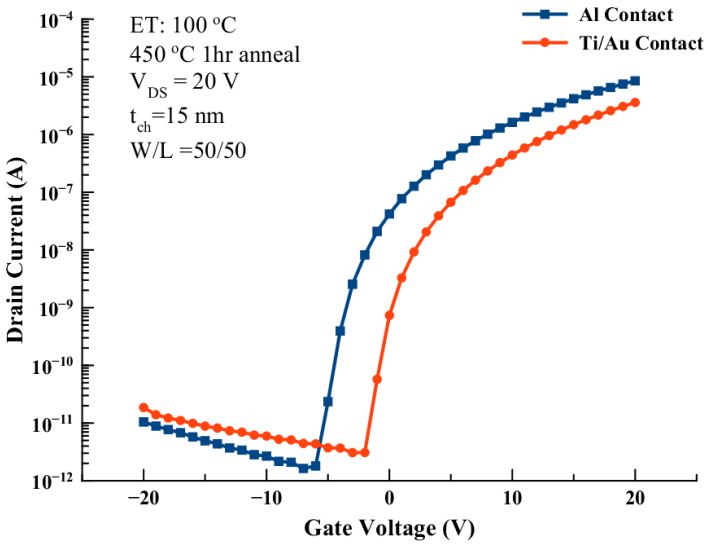

Figure 3.3.2. Al and Ti/Au I-V characteristic

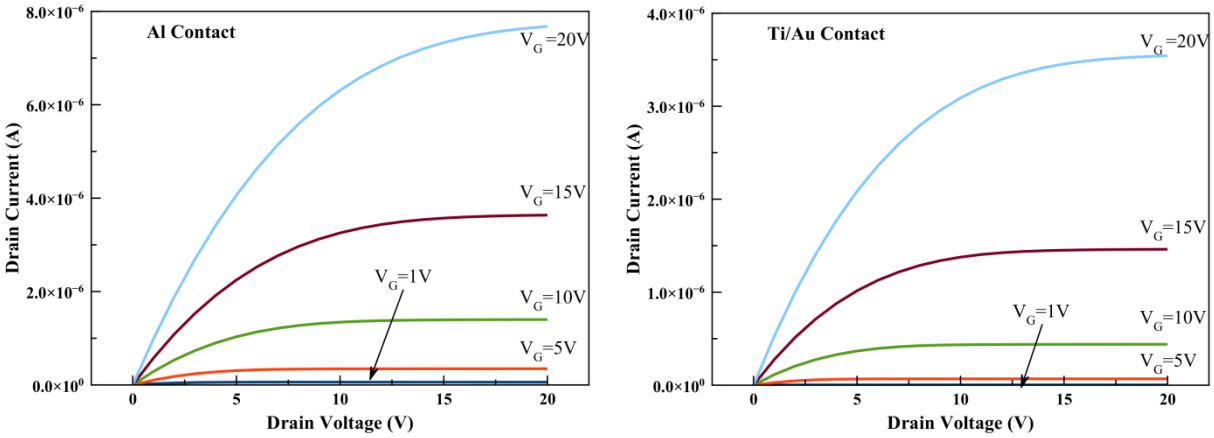

Figure 3.3.3. Al and Ti/Au output characteristic plot

Table 3.3.2 *TFT characteristics of Al and Ti/Au contacts*

Contact	I_D (A)	$I_{ON/OFF}$	V_{ON} (V)	SS (V/dec)	μ_{FE} (cm^2/V-s)
Al	$8.5x10^{-6}$	$4.7x10^{6}$	-6	0.8	3.4
Ti/Au	$3.5x10^{-6}$	$1.1x10^{6}$	-2	0.78	1.9

(c) Effect of Oxygen Flow

The influence of oxygen incorporation in the deposition process has been investigated. During this experiment TFTs were produced with 2 and 10 sccm oxygen flow. For both TFTs the GSZO channel was 15 nm and was annealed in air at 450 °C for 1 hr. The electrical performances of these devices are shown in Figures 3.3.4- 3.3.6. Table 3.3.3 shows the electrical performance of the two TFTs. Here it is observed that with increasing oxygen flow there is a positive shift in V_{ON} from -6 to -2 V. The I_{OFF} current has also reduced in the 10 sccm TFT. The sub-threshold remains the same for both samples at 0.8 V/dec and the field-effect mobility has reduced from 3.4 to 2.7 cm^2/Vs with increasing oxygen flow.

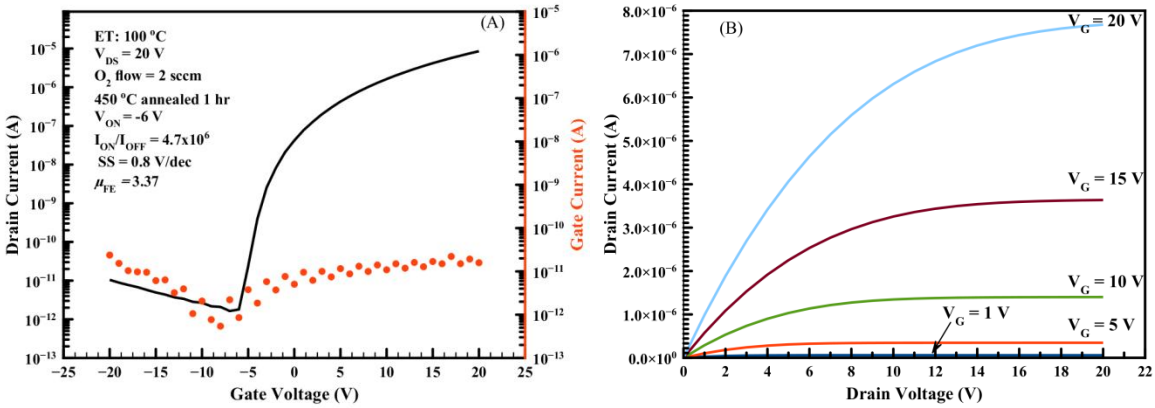

Figure 3.3.4. ET 450 ^{o}C annealed 2 sccm O_2 TFT (a) transfer and (b) output characteristics

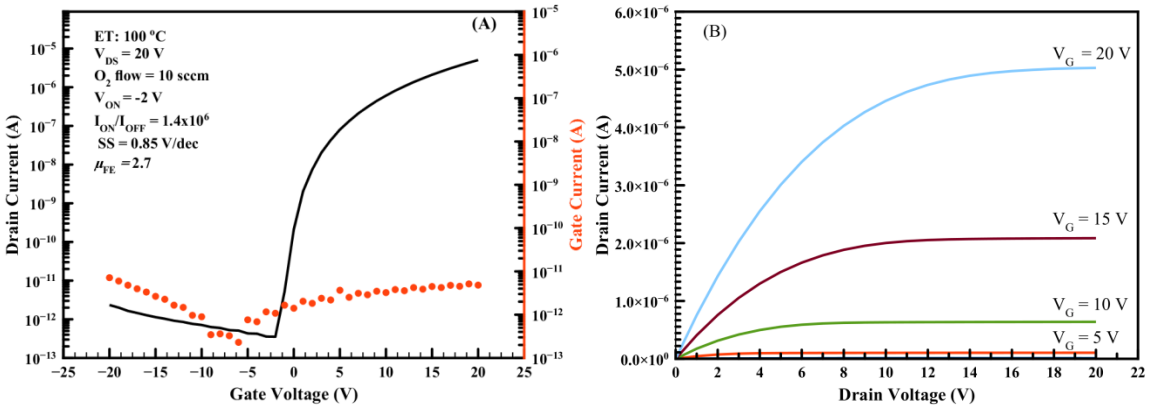

Figure 3.3.5. ET 450 ^{0}C annealed 10 sccm O_2 TFT (a) transfer and (b) output characteristics

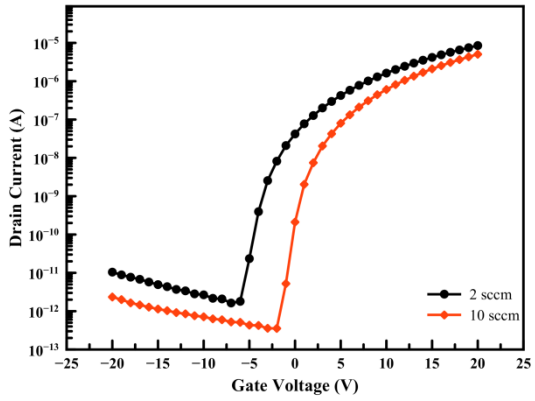

Figure 3.3.6. Transfer characteristic comparison between 2 and 10 sccm O_2 flow

Table 3.3.3 *Comparison between TFT with 2 and 10 sccm O_2 flow performance*

Oxygen Flow (sccm)	I_D (A)	I_{ON}/I_{OFF}	V_{ON} (V)	SS (V/decade)	μ_{FE} (cm^2/V-s)
2	$8.5x10^{-6}$	$4.7x10^{6}$	-6	0.8	3.37
10	$5.00x10^{-6}$	$1.4x10^{7}$	-2	0.85	2.7

We have earlier shown that the elemental at.% concentrations were slightly varied as O_2 was increased during the deposition of GSZO film. The differing trends of O_2 flow and Oxygen at.% is attributed to both a reduction in surface point defects and chemisorption of O_2 molecules onto the films surface. Surface defects are reduced with increased O_2 during deposition, thereby reducing the dangling bonds available to induced chemisorption**.** With the positive change in V_{ON} and the decreased in the field-effect mobility as shown in Figure 3.3.7, this may be caused by the disorder that produces tail states in the vicinity of the band edge and leads to the reduction of the band gap (E_g)**.** The optical band gap was not conducted for this research, but Shin et al.[21] has reported that with increasing oxygen flow the E_g decreases. Therefore, μ_{FE} degrades gradually with increasing oxygen content. Also, from Tanina's dissertation[2] as the Ga/OI ratio increases the carrier concentration in the film is decreased because Ga is considered as scavenger of oxygen vacancies due to its strong bonding with oxygen. This is consistent with V_{ON} shifting in the positive direction as in Fig.3.3.7. Thus, a higher gate voltage is required to turn on the TFT at higher oxygen concentration.

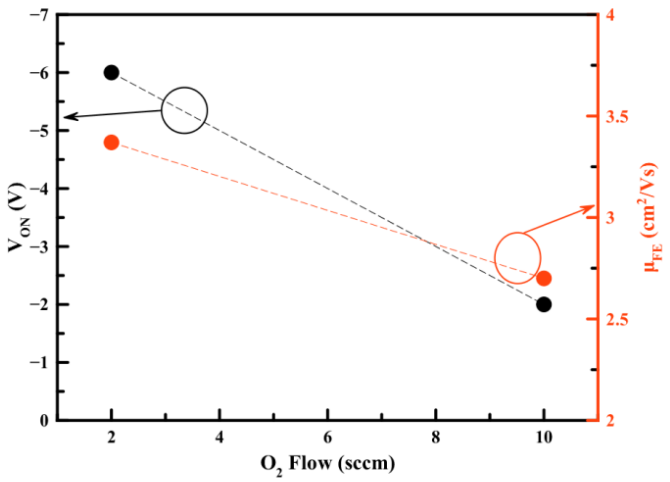

Figure 3.3.7. Threshold voltage and field-effect mobility as a function of O_2 flow

(d) Active Layer Thickness

The channel thickness of GSZO was varied to examine the effect on the electrical properties of the devices. The transfer characteristic of 15 and 8 nm channel devices are plotted in Figure 3.3.8 – Figure 3.3.10 with Figure 3.3.11 providing the comparison of the SS, V_T,

and μ_{FE} as a function of channel thickness. Their electrical characteristics are listed in Table 3.3.4. Both I_{ON} and I_{OFF} decrease with decreasing channel thickness, with on/off ratio slightly better with the 8 nm channel. V_{ON} has largely shifted in the positive direction from -9 V to 1 V with the 8 nm device. SS also improves significantly from 0.91 to 0.3 V/dec with reduction in channel thickness; however, the field-effect mobility has decrease from 4 to 0.87 cm^2/Vs.

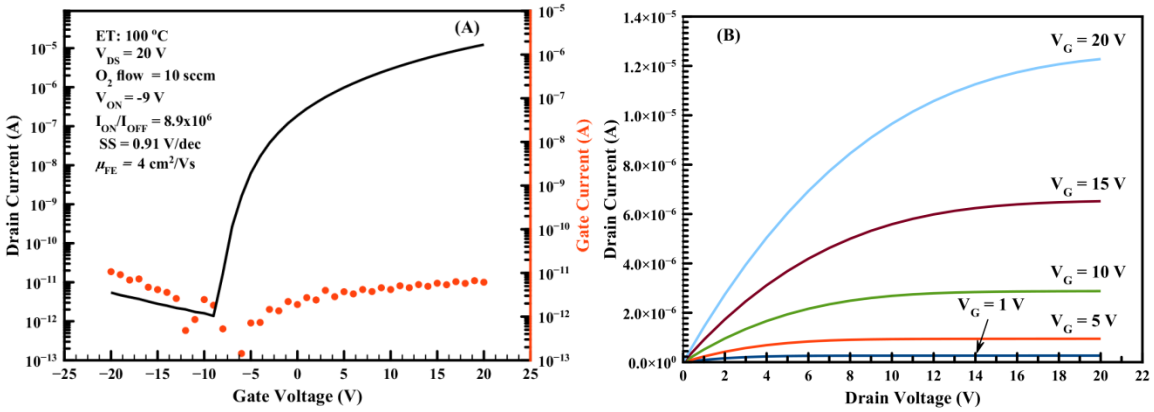

Figure 3.3.8. ET 450 °C annealed 15nm (a) transfer and (b) output characteristics.

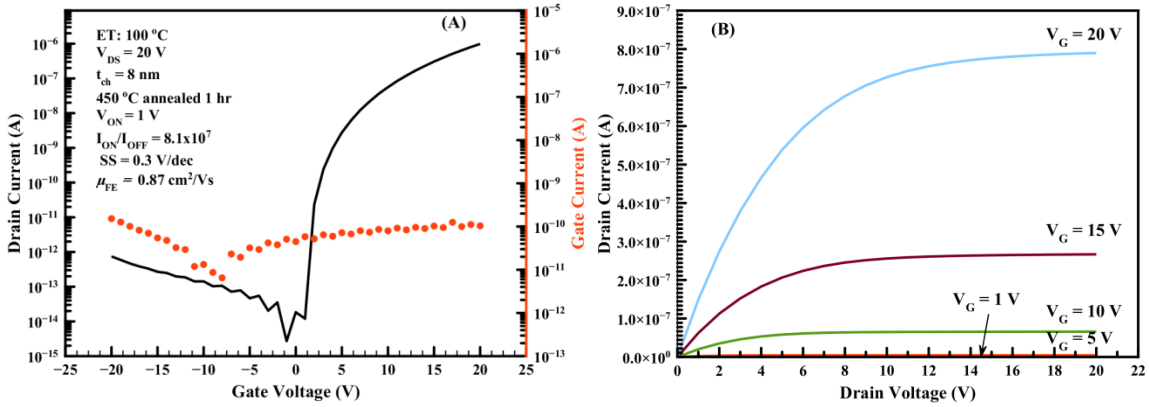

Figure 3.3.9. ET 450 °C annealed 8 nm (a) transfer and (b) output characteristics

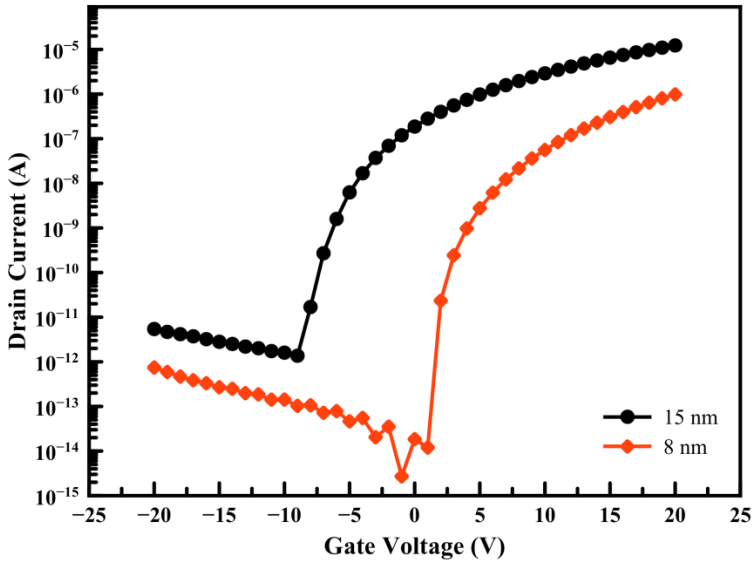

*Figure 3.3.10.*Channel layer thickness transfer characteristic comparison between 15nm and 8nm

Table 3.3.4 *Electrical characteristic comparison for 15 nm and 8 nm channel*

Channel Thickness (nm)	I_D (A)	I_{ON}/I_{OFF}	V_{ON} (V)	SS (V/decade)	μ_{FE} (cm^2/V-s)	Density (g/cm^3)
15	$1.2x10^{-5}$	$8.9x10^{6}$	-9	0.91	4	~5.9
8	$9.8x10^{-7}$	$8.1x10^{7}$	1	0.3	0.87	~7

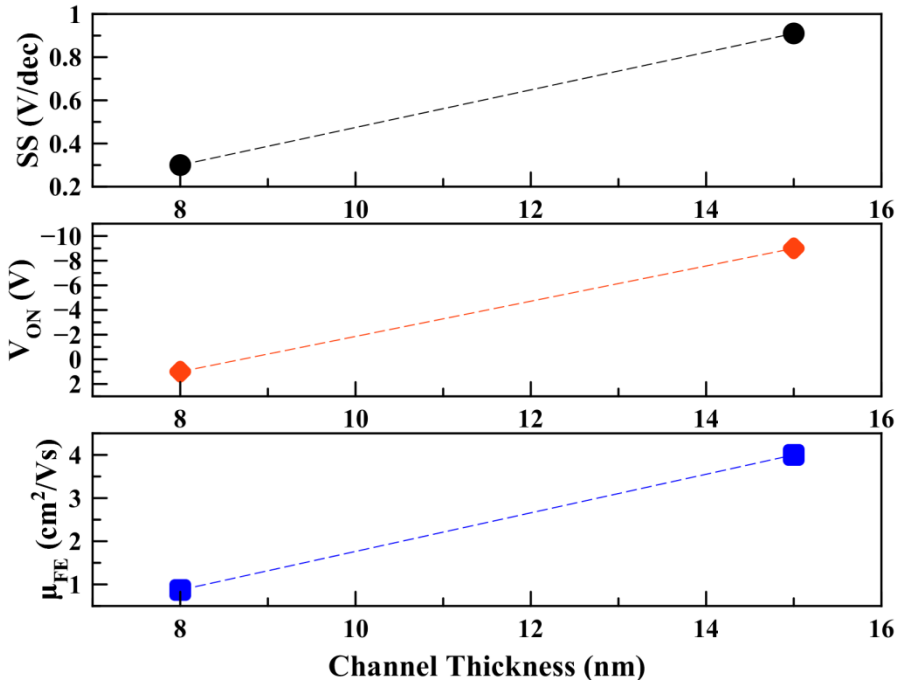

Figure 3.3.11. The changes in sub-threshold swing, voltage threshold, and field-effect mobility as a function of channel thickness.

With the reduction in the active layer thickness, the TFT electrical performance has improve significantly. To explain this first, the channel layer thickness extends only a couple of nm from the SiO_2/GSZO interface and second, the thinner channel layer is denser and exhibit smoother interface as given in Table 9 which gives rise to a better SS value. The thicker channel layer impacts the TFT performance by contributing to the background carrier concentration resulting in the negative V_{ON} shift with increase in I_{OFF}. The increase in I_{OFF} is directly proportional to the channel thickness, from Equation 2.

To explain the positive shift in V_{ON} and the decrease in I_D, the surface of the channel is sensitive to the oxygen adsorption from the ambient forming different bonded negative ionic species such as O^{2-}, O^- and aids in creating the depletion region at the surface. A significant of this is happening in the thinner channel, which restrict the channel conductivity and give rise to the decrease in drain current which was observed in the 8 nm channel. Also, the fully depleted region have already formed in the 8 nm channel when a small positive gate voltage is applied which leads to a positive V_{ON} at 1 V. Furthermore, it has been observed from previous work done by our group that lower channel thickness in GSZO seems to result in denser layer and smoother interfaces. Thus, the reduction in channel thickness is more advantage in the performance for GSZO TFT.

(e) Post Deposition Treatment

Following the fabrication of the GSZO TFTs post treatment was done to the TFTs to investigate their effect on the characteristic performance. These post treatment include post oxygen annealing (POA), exposing the TFTs to forming gas (N_2H_2) in order to enhance the TFTs characteristic.

Annealing Ambient

After fabrication of the GSZO TFTs the sample was annealed in oxygen at 200 °C for 5 min for two set of samples, 2 and 10 sccm oxygen flow. The transfer and output characteristic are plotted in Figure 3.3.12 - Figure 3.3.15 and Figure 3.3.16 comparing the 2 and 10 sccm I-V characteristic behavior. The electrical properties are given in Table 3.3.5.

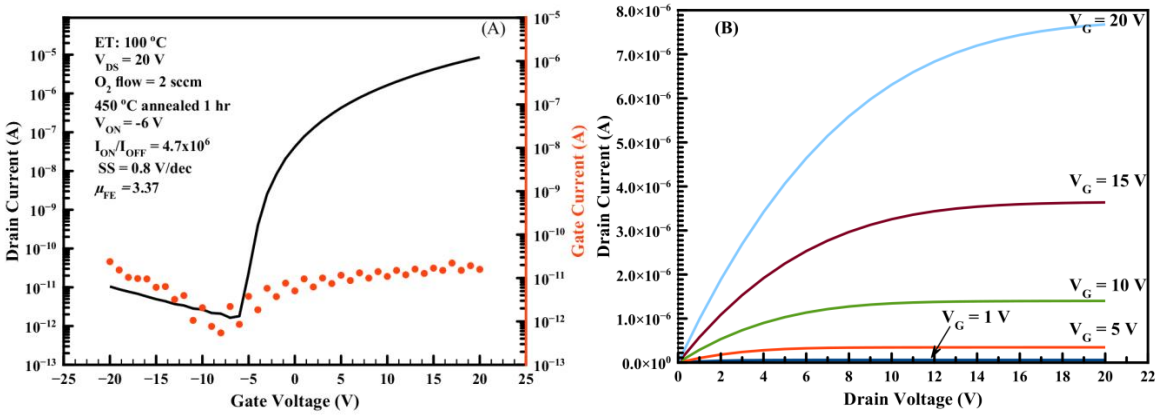

Figure 3.3.12. As-deposited 2 sccm (a) transfer and (b) output graph

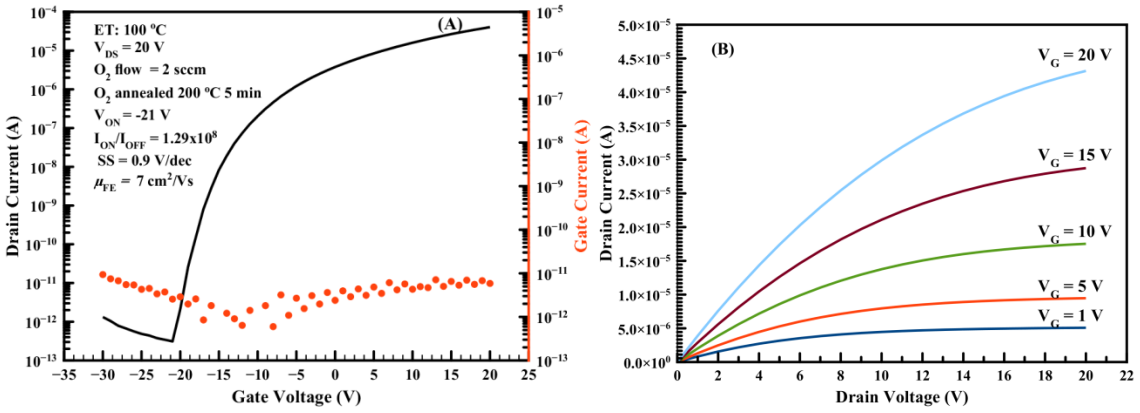

Figure 3.3.13. 200 °C O_2 annealed 2 sccm (a) transfer and (b) output characteristics

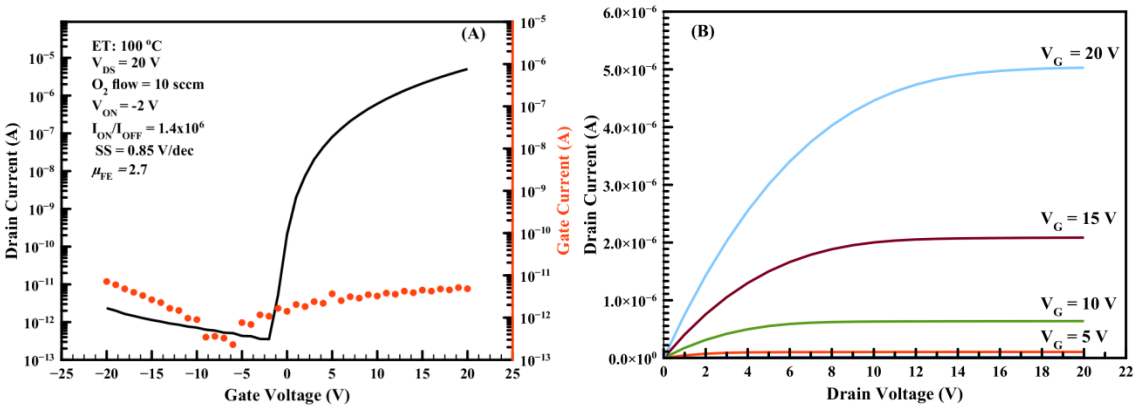

Figure 3.3.14. As-deposit 10 sccm (a) transfer and (b) output graph

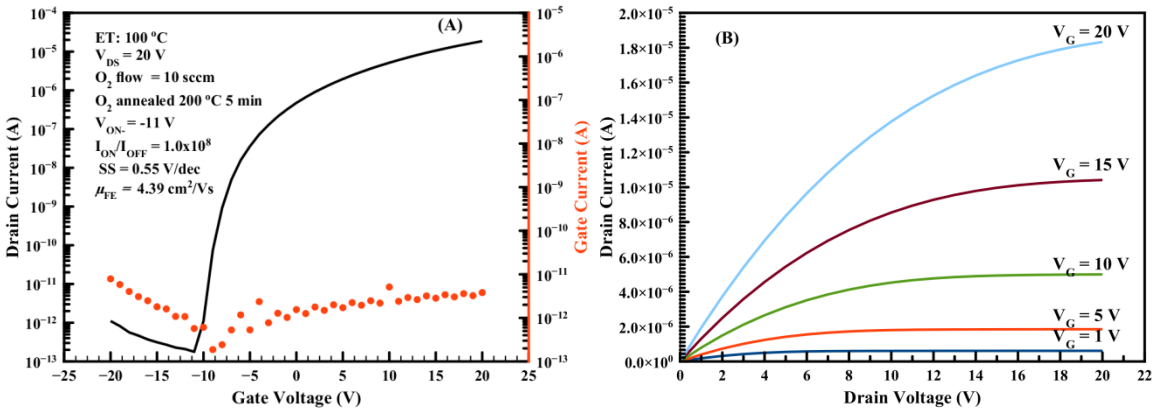

Figure 3.3.15. 200 °C O_2 annealed 10 sccm (a) transfer and (b) output graph

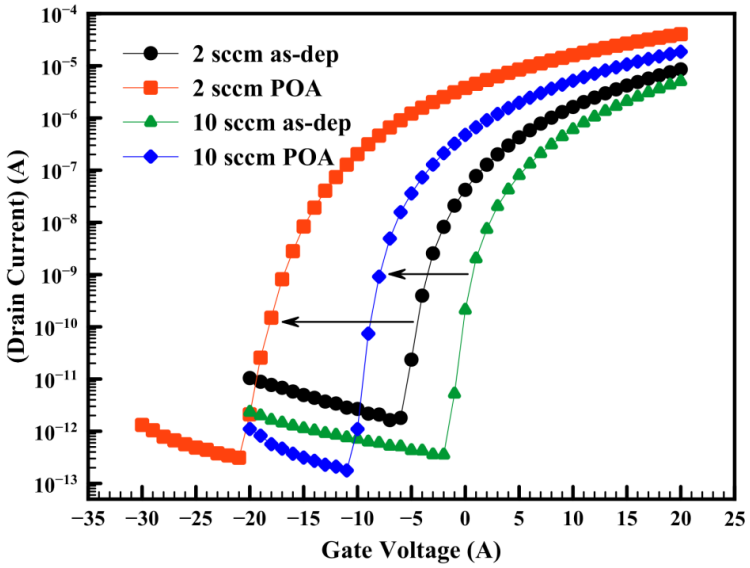

Figure 3.3.16. Effect after POA I-V showing V_{ON} shifted negatively

Table 3.3.5: *POA electrical performance*

Condition	O_2 flow (sccm)	I_D (A)	I_{ON}/I_{OFF}	V_{ON} (V)	SS (V/decade)	μ_{FE} (cm^2/V-s)
As-dep.	2	$8.5x10^{-6}$	$4.7x10^{6}$	-6	0.8	3.37
	10	$5.0x10^{-6}$	$1.4x10^{7}$	-2	0.85	2.7
POA	2	$4.0x10^{-5}$	$1.29x10^{8}$	-21	0.9	7
	10	$1.8x10^{-5}$	$1.0x10^{8}$	-11	0.55	4.39

After POA both devices show overall improvement in their electrical characteristic. I_D has increase for both O_2 flow from $8.5x10^{-6}$ A to $4.0x10^{-5}$ A for 2 sccm and from $5.0x10^{-6}$ A to $1.8x10^{-5}$ A for the 10 sccm device with a corresponding increase in on/off ratio for both TFTs. SS also improve and μ_{FE} also increase from 3.37 to 7 cm^2/Vs and from 2.7 to 4.39 cm^2/Vs for both 2 and 10 sccm TFTs, respectively. It is observed in both O_2 flow cases V_{ON} after POA has shifted negatively. Figure 3.3.16 illustrates the shifting of the I-V characteristic and V_T change.

After POA, further investigation was done to both POA devices by exposing the sample to forming gas (N_2H_2) to find out if there is any improvement to the TFTs performance. Figure 3.3.17 shows the I-V characteristic compare with as-deposit and POA with N_2H_2. Table 3.3.6 shows the electrical characteristic result. From the I-V graph it is observed that there is a large negative shift of -15.5 V in the threshold voltage from the POA state and V_{ON} has also shift negatively to -26 V. I_D has a small increase to $6.4x10^{-5}$ A with I_{OFF} stays relatively the same at 10^{-13} A range.

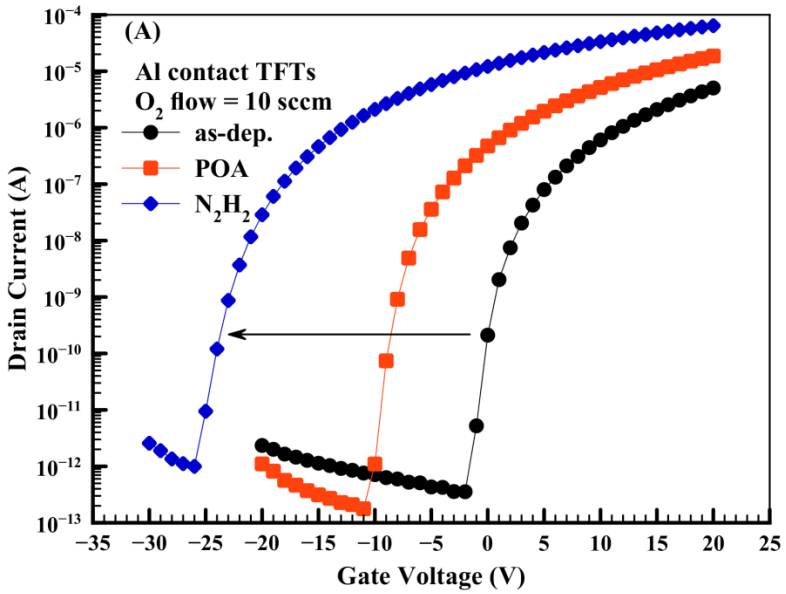

Figure 3.3.17. I-V characteristic after exposing to N_2H_2

Table 3.3.6 *Electrical performance after exposing to N_2H_2*

Condition	I_D (A)	I_{ON}/I_{OFF}	V_{ON} (V)	SS (V/decade)	μ_{FE} (cm^2/V-s)
As-dep.	$5.0x10^{-6}$	$1.4x10^{7}$	-2	0.85	2.7
POA	$1.8x10^{-5}$	$1.0x10^{8}$	-11	0.55	4.39
N_2H_2	$6.4x10^{-5}$	$5.7x10^{7}$	-26	0.9	7.2

(f) Conclusion

In conclusion, increased annealed temperature from 140 °C to 450 °C, with Al contact and 2sccm oxygen flow, with reduction in channel thickness to 8nm and post oxygen annealing treatment lead to significant improvement in the TFT characteristics.

Following Table 3.3.7 compares the best data obtained from this study to the best IGZO published work, Kawamura et al.[22]

Table 3.3.7. *Comparison of our study with best IGZO data*

	V_{ON} (A)	I_{ON}/I_{OFF}	SS (V/decade)	μ_{FE} (cm^2/V-s)
Our Study	1	10^7	0.3	0.87
Kawamura et al.[22]	0	10^8	0.082	3.1

3.4 Electrical and Optical Stability

In addition to the superior device characteristics, the device stability is another important requisite for these TFT applications. Hence in the following a comparison of the above two sets of devices with different channel annealing temperatures, under different gate bias and under illumination and a combination of the electrical and optical stress are presented.

(a) Positive Bias Stress (PBS)

Figure 3.4.1 exhibits the transfer characteristics for GSZO TFT's annealed at different temperatures: a) 140 °C b) 350 °C c) 450 °C and under PBS. V_{ON} increases and a gradual decrease in ΔV_{ON} (140°C -8.3 V 140°C = 8.3 V, 450°C = 0.24 V) under PBS. The TFT with large positive V_{ON} values corresponds to the TFT that is strongly influenced by the trapping in interface states and/or bulk traps in the channel band gap, thus has the worst stability. The positive shift is due to electron trapping at the gate insulator and/or interface. The more porous device showed the largest positive V_{ON} shift suggesting it has the highest concentration of shallow defects. This density of shallow defects decreases with increasing temperature suggesting the lower deposition temperature results in ionization energy too low to form GSZO film with little to no defects. An increase in deposition temperature results in a much more stable GSZO TFT with a ΔV_{ON} of only 0.75 V. A gradual increase in film density with deposition temperature from XRR data explains this gradual reduction of hump presence in the transfer I-V characteristics .

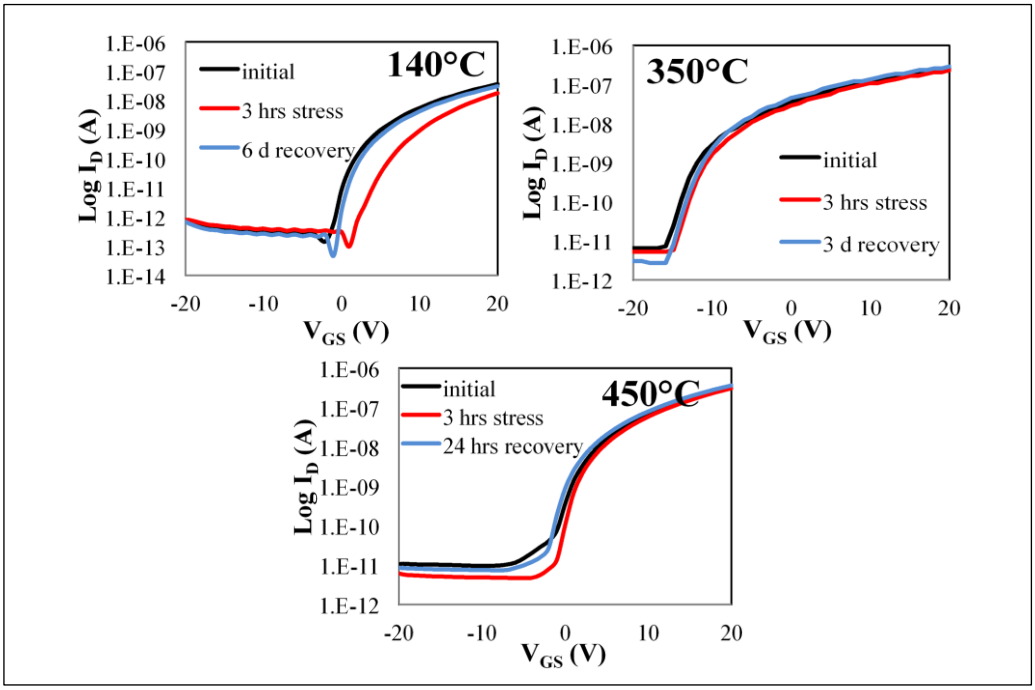

Figure 3.4.1 Transfer characteristics for GSZO TFT's annealed at different temperatures: a) 140°C b) 350°C c) 450° C

(b) Negative Bias Stress (NBS)

The variations in the transfer characteristics for the negative gate bias stress for different durations in GSZO TFTs annealed at 140 °C and 450 °C are displayed in Figure 3.4.2. The devices maintained good stability under negative bias stress as compared to the PBS stress consistent with those observed in other oxide devices[23]. Amongst the two devices, 140 °C annealed one showed the instability with the negative shift in V_{ON} with increased stress duration. This negative shift is attributed to the band bending resulting in positively charged donor states[23]. Under NBS, free holes are generated in the active region.

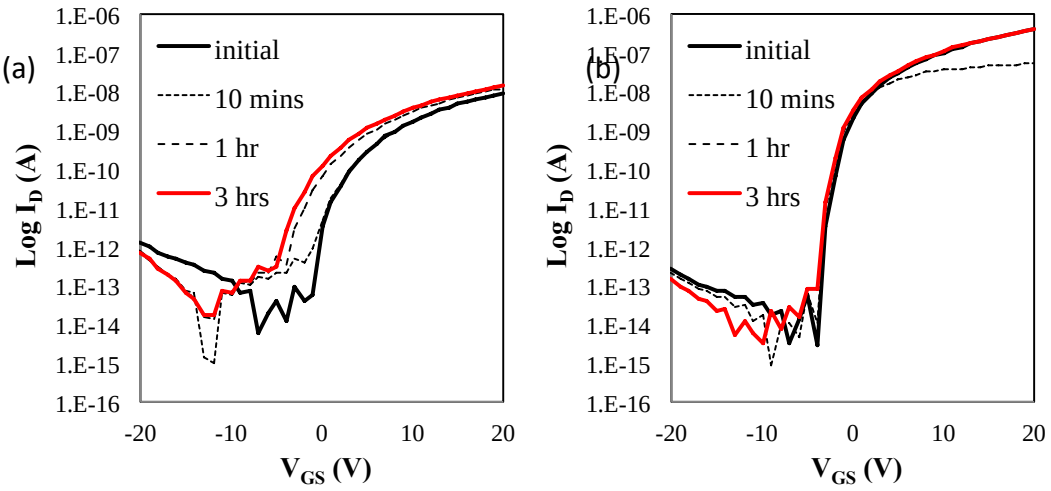

Figure3.4.2. Typical instability of GSZO TFT transfer characteristics under a (a) low temperature 140°C annealed and (b) high temperature 450°C annealed 5 mTorr device.

(c) Optical Stress

Figure 3.4.3 illustrates the photo-induced degradation under illumination of different wavelengths. It is evident that instability is always larger for 140 °C annealed device and most notably under λ =410 nm for both the devices.

The illumination of red light on 140°C annealed TFTs caused a positive V_{ON} shift (~4.2 V) within 10 mins, but become stable thereafter. Under 550 nm wavelength illumination, the positive shift observed within 10 minutes was comparatively less but V_{ON} gradually shifted negatively thereafter remaining stable after 1 hour. 410nm illumination produced the largest changes shifting negatively the transfer characteristics. In comparison, the 450°C annealed device transfer characteristics exhibited no shift under 650 nm and reduced negative parallel shifts under 550 nm and 410 nm illuminations.

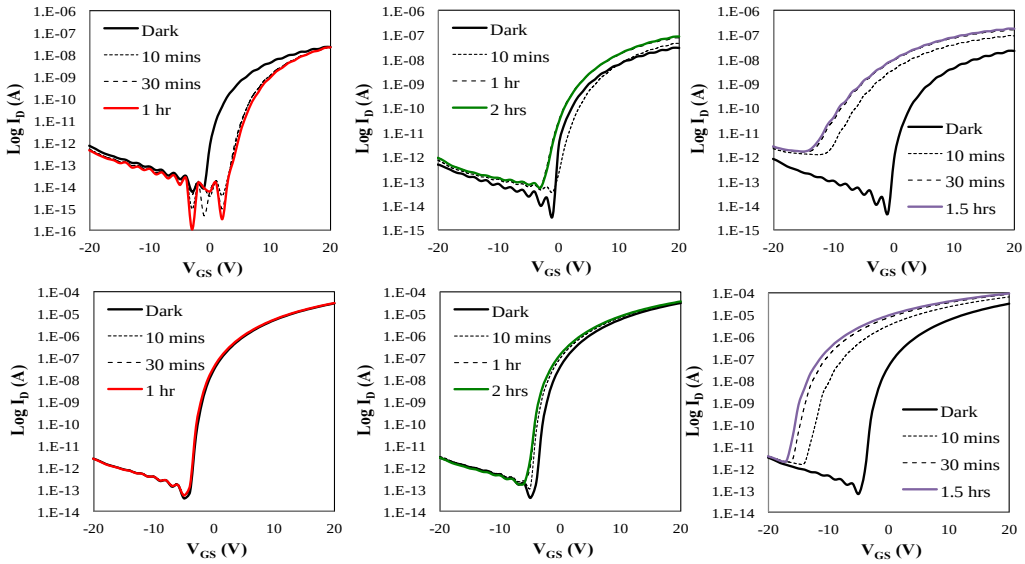

Figure 3.4.3. Typical transfer characteristics of GSZO under illumination stress: a) 650 nm, b) 550 nm, and c) 410 nm. The top row represents 140°C devices, and the 2nd row represents 450°C devices.

As is well established subgap states in these oxides are responsible for the observed optical instability. The changes induced under 650 nm illumination in 140°C annealed device only, is indicative of presence of large photo-induced shallow trap states in these devices. Since a positive shift in V_{ON} constitutes a net decrease in electrons within the film, the induced traps can be attributed to electron traps. After 10 minutes equilibrium is reached between the rate of carriers being generated and trapped. Exposure to shorter wavelength leads to activation of deeper traps in the band gap. It is well known that deep traps in ZnO films mainly consist of neutral oxygen vacancies (V_o) which is relaxed forming a fully occupied deep state about 2.3eV below the conduction band. Under light illumination of $\lambda \leq 550$ nm V_o is photoexcited exciting 2 electrons into the conduction band minima (CBM) simultaneously creating interface trap density, D_{it}, associated with V_O^{2+} forming a shallow level close to the conduction band. The negative shift observed is consistent with the increased channel conductivity and the increases SS observed is indicative of increased D_{it}. At 410 nm larger negative shifts in comparison to those observed at higher wavelengths cannot be accounted by deep traps alone. This can be explained only by the transition from valence band tail state of very high density. The lack of shift in 450°C annealed devices under 650nm illumination and much less shift under lower wavelength suggests significantly reduced trap density throughout the band gap. Also lack of any change in SS throughout the optical stress indicates that the induced traps are more likely originating from interface states in the high temperature annealed devices.

Thus the instability in low temperature devices are caused by the subgap states extending throughout the band gap from shallow to deep to valance band tail states in contrast to high temperature devices where the degradation is primarily caused by interfacial states near the valence band.

However, under NBS with illumination (NBIS) at λ=550 nm, as shown in Fig. 3.4.3 large negative V_{ON} shift is induced on both the low and high temperature annealed devices, though higher shift exhibited by the low temperature annealed devices. The contribution to the high conductivity in this case is not only due to the electron-hole pair generation from the deep trap but also caused by the transport of V_o^{2+} towards the interface screening the gate bias resulting in an additional negative shift in V_{ON}. The large changes observed in low temperature annealed device is consistent with the XPS results indicating that these films are characterized by large density of oxygen vacancy and can be correlated to higher film porosity, high surface and interface roughness as determined from AFM and XRR measurements. Thus annealing removes some of the weak chemical bonds leading to improved channel quality, smoother surface interfaces leading to overall reduction in the subgap states thereby influencing the stability.

(d) Stretched-Exponential Equation

In order to further characterize the bias-stress effect, the measure of decay and recovery under an applied positive gate was estimated using the following equation 5

$$\Delta V_{ON} = \Delta V_{ON_0}\{1 - (\exp(-(t/\tau)^{\beta}))\}, \quad (5)$$

where ΔV_{ON_0} is the ΔV_{ON} at infinite time, β is the stretched-exponential exponent, and τ is the trapping time for the stress phase and detrapping time for recovery phase. The τ has been commonly associated with the duration for which the electrons are trapped or the average time for oxygen adsorption on the surface. In our case, the following results can be better explained when τ is considered as the duration associated with the trap rather than oxygen adsorption. As observed in Table 3.4.1, τ is smaller at 450°C annealed samples (~10^1) than at 140°C annealed samples (~10^2) by an order of magnitude. A smaller τ means long term stability, consistent with our earlier results that post annealing treatment at higher annealing of GSZO thin films leads to improved stability of the device.

Table 3.4.1. *Stress and recovery data extracted using the stretched exponential equation.*

Condition	Stress/ Recovery	τ (s)	β
140°C 5 mTorr 10 sccm	Stress	1.6 x 10^2	0.6
	Recovery	4.0 x 10^3	0.5
450°C 1hr 5 mTorr 10 sccm	Stress	5.0 x 10^1	0.5
	Recovery	2.0 x 10^3	0.4

(e) C-V Analysis of Optical Stress

The optical stress measurements using I-V characteristics were complimented by C-V characteristics. The evolution of C-V curves of different 140 °C and 450 °C annealed GSZO TFTs as a function of wavelength is shown in Figure 3.4.4,All the devices except one exhibited the two regions of operation, the accumulation region corresponding to the large constant value of C beyond the turn on voltage and the depletion region begins where the capacitance decreases with the decreasing voltage and the range where the C values reaches minimum and remains constant is the region correspond to fully depleted GSZO film. There are salient differences between the C-V characteristics of the two devices. The 450 °C annealed devices exhibited sharper transition from complete depletion to accumulation regions, slightly higher values of C in accumulation region , the transition voltage being always negative and optical stress producing only parallel negative shifts, latter increasing with decreasing illumination wavelength. All these are signatures of conductive channel, lower shallow trap density and induced states being surface states further attesting to the earlier conclusions. On the contrary in the low temperature devices the transitions were gradual and the illumination at the lowest wavelength of 750 nm produced a positive shift with the accumulation region not being fully formed even at high positive voltage of 20 V. The latter is indicative of the dominance of photo-induced shallow electron traps preventing the formation of the channel. The higher value of C in the accumulation region and hard saturation for 550 nm, 410 nm and NBIS optical stress indicative of conducting channel though lower than 450°C annealed devices. The slope in the transition region is attributed to the large presence of trap density. The calculated values of trap density are listed in the Table 3.4.1

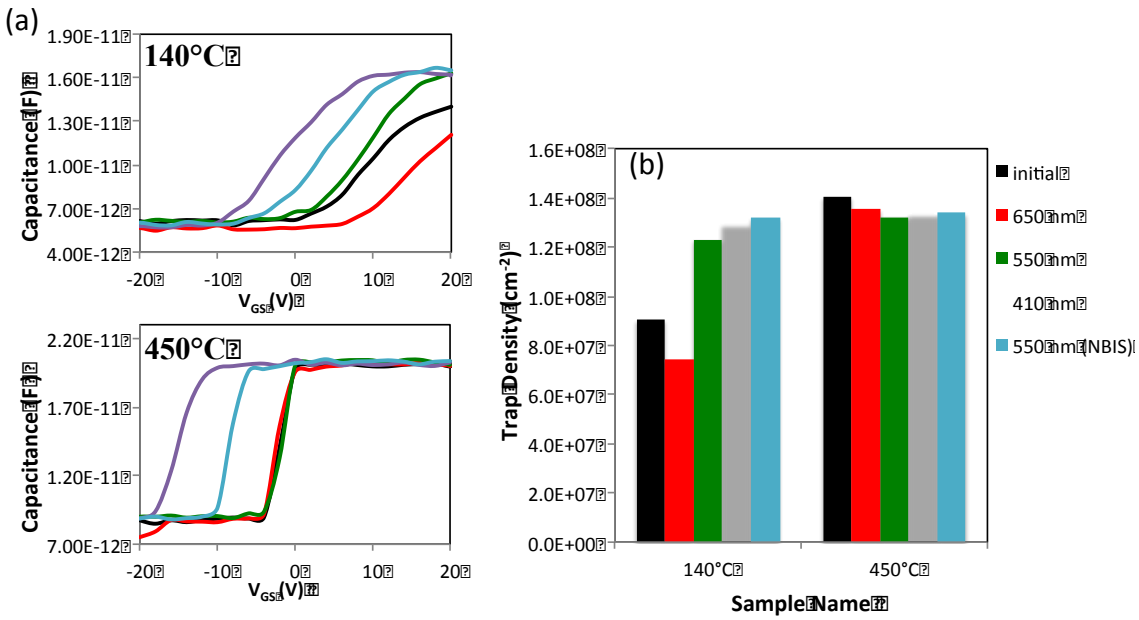

Figure 3.4.4. The (a) C-V measurements of 140°C and 450°C annealed GSZO TFTS and (b) the calculated trap density of each sample under different wavelength illumination.

(f) Shelf Life Stability

It was observed that thin films could degrade after being exposed to room air for several weeks. Figure 3.4.5 shows how varying annealing time affects the amount of shift in V_{ON} over a period of 11 weeks. Although the 12 hr sample had poorer shelf life stability, V_{ON} for both the devices tends to merge after 2 weeks and remained stable after that. A possible explanation of this behavior could be hydrolyzation by air moisture.

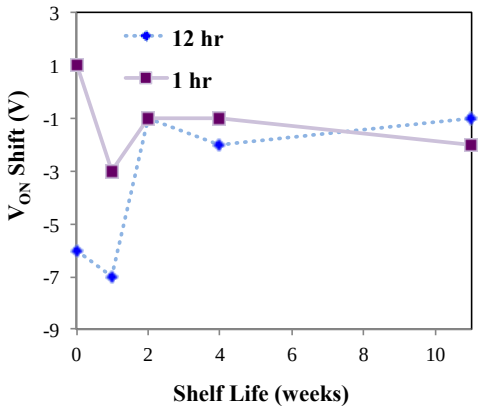

Figure 3.4.5. V_{ON} shift as a function of shelf life for GSZO TFTs which employ different annealing duration: 1hr and 12hr at 140 °C post deposition.

(g) Conclusion

In conclusion, the post deposition annealing temperature of 350°C has the dominant effect on the reduction of the deep and shallow states, thereby making the device more stable. This also explains the superior performance of the initial device. However, density of VB tail states is still large enough to significantly contribute to the degradation of these devices under 410nm and NBIS.

3.5 AIM-Spice Simulation Results

A physical I-V model based on the exponential density of deep and tail states has been developed and tested for modeling GSZO TFTs. The accuracy of the simulated curves using the parameters extracted is verified with measured and calculated data using the expressions contained in the Si:H TFT model level 15.

Table:3.5.1 *Parameters used to model the GSZO TFTs*

Name	**Units**	**Default**
ALPHASAT	-	0.6
CGDO	F/m	0
CGSO	F/m	0
DEF0	eV	0.6
DELTA	-	5
EL	eV	0.35
EMU	eV	0.06
EPS	-	11
EPSI	-	7.4
GAMMA	-	0.4
GMIN	$m^{-3}eV^{-1}$	1.00E+23
IOL	A	3.00E-14
KASAT	1/°C	0.006
KVT	V/°C	-0.036
LAMBDA	1/V	0.0008
M	-	2.5
MUBAND	m^2/V-s	0.001
RD	Ω	0
RS	Ω	0
SIGMA0	A	1.00E-14
TNOM	°C	27
TOX	m	1.00E-07
V0	V	0.12
VAA	V	7.50E+03
VDSL	V	7
VFB	V	-3
VGSL	V	7
VMIN	V	0.3
VTO	V	0

The linear characteristics calculated were compared with the experimental data and the simulated using AIM-SPICE. Both simulated and calculated are practically the same and fit well with the experimental data, validating the proposed new extraction method as shown in Figure 3.5.1.

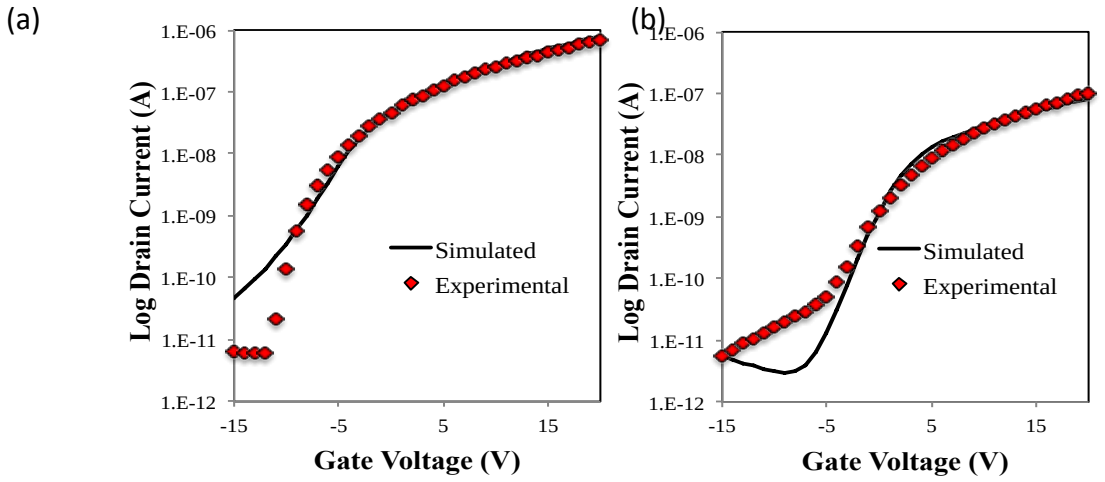

Figure 3.5.1. Comparison between simulation and measured data for devices with (a) W/L=100/50 and (b) 75/25 on a semi-log scale.

Some limitation of this software is that it could not fit the simulated data to the measured data in the region below V_{ON}. The extracted parameters varied per device are shown in Table 3.5.2.

Table:3.5.2 *Extracted parameters from AIM-Spice*

Sample	Gamma	Delta	Gmin ($m^{-3}eV^{-1}$)	Vmin (V)	Vaa (V)	Muband (m^2/V-s)
400°C 5 mTorr 10 sccm	1.4	10	1.00E+23	0.7	50	1.28E-04
350°C 5 mTorr 2 sccm	0.6	4	5.00E+20	0.4	80	2.06E-03
350°C 5 mTorr 2 sccm	1	10	1.00E+23	0.9	100	2.79E-05
350°C 5 mTorr 2 sccm	0.85	7	1.00E+23	0.8	40	7.60E-06
140°C 10 mTorr	0.45	9	1.00E+23	0.3	80	8.00E-06
140°C 5 mTorr	0.15	7	3.00E+23	0.3	750	4.10E-06
350°C 5 mTorr	0.55	9	1.00E+23	0.4	550	2.79E-04

The transfer curve simulated for each device varied in each extracted parameters: gamma, delta, gmin , vmin, vaa, and muband. There, was no trend in these parameters, however, for the gmin (density of trap deep states), the 140°C annealed 5 mtorr sample appeared to have the highest value (3.00E+23 $m^{-3}eV^{-1}$) while the 350°C annealed 5 mtorr had the least (5.00E+20 $m^{-3}eV^{-1}$). This is consistent with XRR analysis and stability measurements discussed earlier. All other variations in the other parameters are due to different fabrication conditions. The modeling was not extensively investigated.

3.6. Student Participation and Educational Component

During this period **Robert Alston** completed his Ph.D dissertation entitled "A Study of GSZO TFTs for Fabrication on Plastic Substrates" and **Briana McCall** completed her M.S.E.E thesis entitled "A Study of Electrical and Optical Stability of GSZO Thin Film Transistors". **Briana McCall** was a **GEM fellow** while **Robert Alston** was a **Title III fellow**. Both of them are **afro-american** students. **Robert Alston** was also one of the student who started working on this project as an undergraduate, continued to Master and PhD program. **Eric Forsythe** from ARL, MD and **Jay Lewis** from RTI International served on **Robert Alston's** dissertation committees. Third student **Ngoc Nguyen**, another Master student is currently working on his thesis which is more geared towards high temperature annealed TFTs.

There were 8 presentations made by all these three students during this period. Most noteworthy was **Iyer** being an **invited speaker** in **SPIE Photonics West 2013** and **Robert Alston's** oral presentation in **SPIE Photonics West 2014** Conference.

3.7 Infrastructure Development

During this last year of the grant period an optical bias testing was set up. The funds for purchasing Micro HR Horiba Scientific monochromator (Figure 3.7.1) were provided by Joint School of Nanoscience and Nanoengineering. The setup consisted of a white halogen lamp and the light was dispersed using Micro HR Horiba Scientific monochromator and SemiProbe LA-150 probe station and Keithley 4200 SCS for device testing as shown in the schematic (see Fig. 3.7.2).

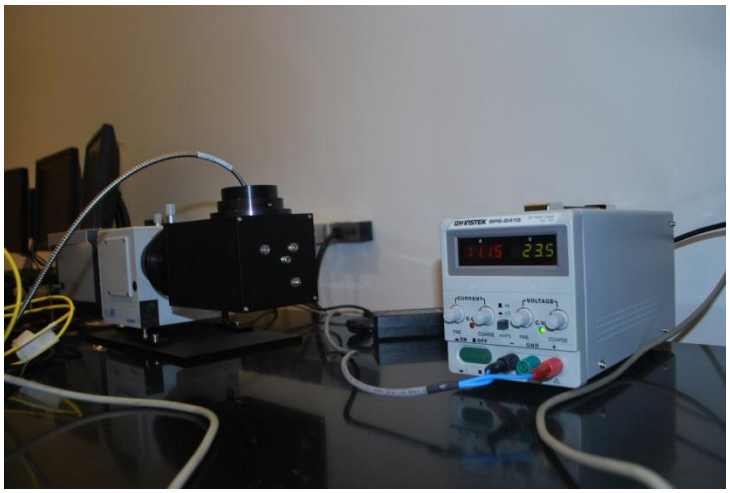

Figure 3.7.1 Micro HR monochromator used for optical stress characterization

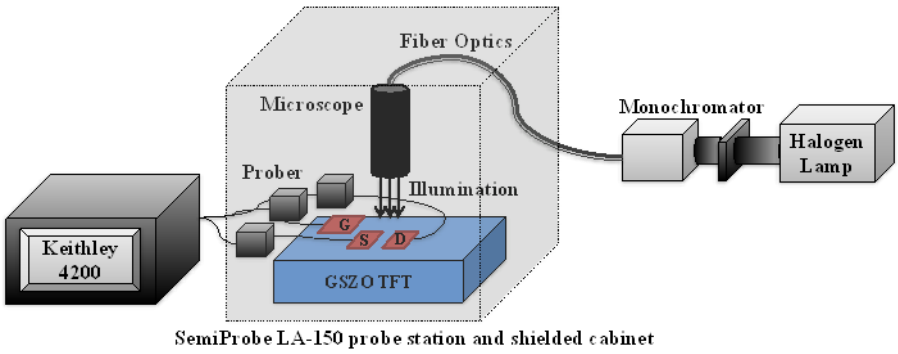

Figure 3.7.2 SemiProbe LA-150 probe station and Keithley 4200 SCS for device testing

The NC A&T and RTI facilities were well-suited for development and testing of TFTs and along with other characterization facilities added during this grant period enabled more rapid progress and higher quality devices.

3.8 Support from DOE-Title III Program

The ARO funding was leveraged to get further support from funding of Department of Education through the Title III program for students support, equipment and characterization service fees to Evans Analytical Group for the XPS and RBS measurements on selective samples.

3.9 Overall Assessment

Our extensive investigations on GSZO TFT behavior shows that the impact of deposition, annealing on the TFT performance and stability is very similar to IGZO TFTs. However, GSZO has added complexity due to the change in Sn valency to the undesirable Sn^{2+} state particularly at lower temperatures. However we have shown that deposition conditions can be manipulated to change this valency to the desired Sn^{4+}, though deep states still poses an issue. We have examined only one composition in the entire phase diagram of GSZO with very low Ga and Sn content and our TFT performance both at high temperature annealing and the ones that are compatible with flexible electronics at low temperature processing are very close to the best ones reported on IGZO TFTs. In the case of IGZO the entire phase diagram was examined before the industry decided on the optimum value. Overall we have shown that GSZO is an excellent candidate for replacing IGZO.

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