ARL-TR-7234 • MAR 2015

US Army Research Laboratory

Batteryless Electroencephalography (EEG): Subthreshold Voltage System-on-a-Chip (SoC) Design for Neurophysiological Measurement

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ARL-TR-7234 ● MAR 2015

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REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-0188

1. REPORT DATE *(DD-MM-YYYY)*	2. REPORT TYPE	3. DATES COVERED (From - To)
March 2015	Final	1 October 2013–30 September 2014

4. TITLE AND SUBTITLE
Batteryless Electroencephalography (EEG): Subthreshold Voltage System-on-a-Chip (SoC) Design for Neurophysiological Measurement

5a. CONTRACT NUMBER

5b. GRANT NUMBER

5c. PROGRAM ELEMENT NUMBER

6. AUTHOR(S)
W David Hairston, Rob Proie, Joseph Conroy, and William Nothwang

5d. PROJECT NUMBER

5e. TASK NUMBER

5f. WORK UNIT NUMBER

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
US Army Research Laboratory
ATTN: RDRL-HRS-C
Aberdeen Proving Ground, MD 21005-5425

8. PERFORMING ORGANIZATION REPORT NUMBER
ARL-TR-7234

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)

10. SPONSOR/MONITOR'S ACRONYM(S)

11. SPONSOR/MONITOR'S REPORT NUMBER(S)

12. DISTRIBUTION/AVAILABILITY STATEMENT
Approved for public release; distribution unlimited

13. SUPPLEMENTARY NOTES

14. ABSTRACT
There is a strong need for "real-world neuroimaging" tools that could provide the hardware substrates supporting the rapidly expanding work in developing optimized brain–computer interactive technologies in a fieldable format. It may be possible to support these needs with electroencephalography (EEG); however, current designs require too much power for long-term operation. Nonconventional, ultra-low power design will be necessary to achieve "wear and forget" systems for on-line, long-term neurological monitoring. One challenge to this goal is the relatively large dynamic range of EEG relative to a comparably low signal-to-noise ratio; this report demonstrates the initial design, simulation, and validation of an EEG data-acquisition, single-integrated-circuit system design that addresses this challenge using an analog front end that adapts on-line to keep the digitized signal within a much smaller dynamic range. This is accomplished through a combination of a voltage-offset controller, low-noise amplifier, low-bit rate analog-to-digital conversion, and a hardware-accelerated digital processor consuming less than 300 nW per channel. At that consumption, it is very feasible to design an entire system capable of operating solely on locally harvested power. Follow-up simulations demonstrate the approaches described here should still provide sufficient signal quality for targeted state monitoring applications.

15. SUBJECT TERMS
EEG, integrated circuits, low power, real-world neuroimaging, neuroscience

16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT	18. NUMBER OF PAGES	19a. NAME OF RESPONSIBLE PERSON
a. REPORT	b. ABSTRACT	c. THIS PAGE			W David Hairston
Unclassified	Unclassified	Unclassified	UU	20	19b. TELEPHONE NUMBER (Include area code) 410-278-5925

Contents

List of Figures

List of Tables

Acknowledgments

We would like to acknowledge the substantial efforts and contributions of Pavan Bhargava, Timothy Lee, and Joe Zhou to the integrated-circuit (IC) design and simulated verifications and Dr Vernon Lawhern for his contributions to the electroencephalography (EEG) validation with alpha-burst classifiers.

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1. Introduction

1.1 Vision

Our vision is the development of ultra-low-power data acquisition systems tuned to meet the extreme requirements of biosensing hardware operated solely from already-available sources, such as body heat from the user. Hardware capable of fulfilling the needs of electroencephalography (EEG) will not only provide the basis of "wear and forget" systems for neurological monitoring but also facilitate an entire class of maintenance-transparent acquisition systems.

1.2 Rationale

There is a strong need within the scientific and Defense community for developing "real-world neuroimaging" tools,[1] which could provide the hardware substrates supporting the rapidly expanding work in developing optimized brain–computer interactive technologies (BCITs)[2,3] in a fieldable format. At the moment, a major barrier is power consumption, where units require relatively large batteries—these are not only heavy but demand consistent charging and maintenance, dramatically decreasing actual usability in battlefield operations.

Advances in the field of subthreshold-voltage (sub-V_t) integrated circuit (IC) design, where the total power of the system is dramatically reduced (range of microwatts), suggest the possibly of creating complete ICs for biosensing applications that can operate on power supplied from the environment.[4] For example, Zhang et al.[4] have demonstrated a complete system-on-a-chip (SoC) IC design that is sufficient for collecting electrocardiogram in a package consuming only 19 microwatts. Such a small level of power can, for example, be harvested via thermoelectric coupling requiring only a 1 °C temperature gradient (supplied by the human scalp at ambient room temperature), suggesting the potential for a constant, biological power source and indefinite operational time.

While promising, to date the current approaches are not sufficient for use in measuring true brain-source signals with EEG, where the signal of interest is extremely small (1–10 μV), has a low signal-to-noise ratio (often <1), and falls within a much larger dynamic range (>800 mV).[5] To overcome this challenge, EEG data acquisition (DAQ) systems typically require very high sensitivity (>90 dB), strong amplification of the target signal, and high bit-depth resolution of the analog-to-digital conversion (ADC) to resolve the extremely small signal (ideally, 24 bits for research). However, these requirements greatly exceed what has been

achievable to date in a sub-V_t package (8-bit, 40–80 dB).[4] As a result, a dramatically different sub-V_t IC design is necessary in order to leverage current technology for batteryless EEG applications.

1.3 Objective

Our primary objective at the US Army Research Laboratory (ARL) was to significantly advance the state of the art for neurophysiological-data monitoring by providing the framework for an extremely low-power, complete-SoC IC design capable of operation without the need for external power. Upon accomplishing this, the goal was development and component-level demonstration of a novel design concept that uses sub-V_t ICs.

2. Approach

2.1 Advanced Sub-V_t AFE Design for EEG Applications

Prior work from Zhang and colleagues[4] has demonstrated the foundation for the IC portion of this work. While their system represents a great technological achievement, the analog front end (AFE) of this previous design lacks the resolution and dynamic range necessary for EEG. Therefore, a key focus of this effort was to build off their system and develop a new AFE that significantly improves upon these deficiencies and enables accurate recording of EEG signals.

Key Hypothesis: By using an adaptive, variable fidelity-on-demand approach to analog-to-digital conversion as part of the IC analog front end, substantial signal quality can be maintained while minimizing energy usage, enabling "batteryless" EEG when used in conjunction with sub-V_t optimized power-monitoring schemes within the integrated system.

Classically, a high amplification and ADC resolution is necessary because the potential dynamic range of the voltage inputs is extremely large (± several millivolts) compared to the target fluctuations of brain-originated signals (single microvolts). This results in the vast majority of the dynamic range going unused except during extreme fluctuations. While this is a trivial problem for conventional high-resolution systems where power is readily available, it is a source of tremendous loss in applications where power is constrained (e.g., increasing power necessity per bit). An alternative, previously unexplored approach would be to aggressively adapt the resolution proportional to the signal on line constantly maximizing the power efficiency.

The proposed AFE is shown in Fig. 1. To accomplish this, a hybrid system is proposed, composed of several key components: per-channel amplifier chain, low-power ADCs, and a hardware-accelerated digital signal processor (DSP) controller. The amplifier chain will consist of a differential low-noise amplifier (LNA) with digitally modulated, voltage-offset control and a variable-gain amplifier (VGA); this provides a combined gain of up to 70 dB (based on the work of Zhang et al.[6]). This would enable the system to account for external voltage offsets and very small fluctuations while minimizing the ADC's dynamic-range requirements to reduce the total power consumed. All on-line adjustments are recorded as part of the data stream to enable accurate recreation of the measured signals. Multiple amplifier chains would be used, one per channel, and time division multiplexed into a single set of ADCs using a technique similar to that reported by Zhang et al.[4]

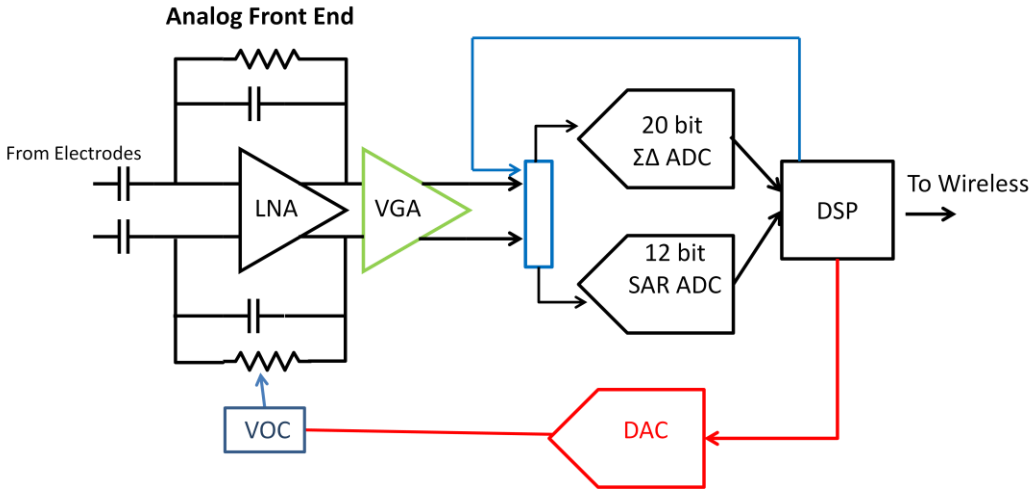

Fig. 1 Block diagram of proposed EEG system

A dual-ADC design is proposed as one method to deal with the signal dynamic range which is potentially large but, during most times, fairly restricted. Work under these efforts focuses primarily on the first (primary) ADC. This is designed as a 12-bit, successive approximation register (SAR) ADC, because it provides the lowest power-conversion energy at the cost of speed per bit.[7] In most instances, it is expected this resolution, combined with the amplifier chain controls, will provide sufficient dynamic range for the EEG signals. In situations where additional dynamic range is required, a SAR ADC's sampling rate would potentially become impractical. Therefore, a second ADC would also be available with a 20-bit, delta sigma (ΔΣ) ADC. The ΔΣ ADC is typically a more complex system, requiring careful design to achieve a low-power implementation, but will enable additional resolution without sacrificing sampling speeds.[7] (Implementation of such a design is outside the scope and timetable of these efforts and will be addressed in future work.) The third component of the AFE is a hardware-accelerated DSP, which

serves 3 purposes. First, it will provide feedback control over the amplifier chain gain, allowing it to dynamically fluctuate on a sample-to-sample basis, providing appropriate coverage for the signal range as it expands and contracts. Second, it provides feedback to a VOC to dynamically subtract a baseline from the incoming signal; this has the net effect of keeping the signal "centered" near zero voltage. Finally, the DSP also provides an on-line selection of the appropriate ADC. These determinations will be based on a combination of factors including, but not limited to, the current power available to the system, prior recorded data, and resolution requirements for the current EEG application.

2.2 Comparing Efficacy against Conventional Approaches

Because circuit design and fabrication are time consuming and expensive, it is valuable to assess whether the proposed designs would, in fact, yield data that are generally "usable" for targeted, fieldable EEG applications. In order to assess the level of anticipated efficacy of the design proposed above, a simple, virtual model of the system was created using Matlab tools and evaluated using pre-existing data. Specifically, we leveraged data previously collected during a paradigm of simulated driving using a high-end, commercial off-the-shelf EEG system. These data were chosen because 1) the system has no onboard filtering, modification, or baseline correction of the original raw per-channel voltage; 2) the system collects a very wide (24 bit) dynamic range; and 3) other efforts have already developed classifiers for extracting target-neural events from the data.[8] Because the primary question of concern was the degree to which a 12-bit ADC would suffice, the raw data (originally collected at 24-bit ADC) were run through a series of successively decreasing, simulated re-quantization steps—simulating different bit-rate ADCs—in conjunction with VOC as described above.

3. Results

3.1 IC Design Performance

Spice simulations were performed on the proposed topologies to validate the effectiveness of individual components in light of anticipated power consumptions. Overall, the implemented front-end design shows an input-referred noise of 1.77 μVrms, comparable to other EEG acquisition systems, while using less than one-third of the power. The most relevant statistics are highlighted in gray in the Table.

Table Comparison of the ARL design's performance with 4 others, including common-mode rejection ratio (CMRR) and power-supply rejection ratio (PSRR)

This Work at ARL	Supply (V)	Power Consumption (µW)	Input Referred Noise (µVrms)	Noise-Power Product	Input Impedance (MΩ)	Gain (dB)	CMRR (dB)	PSRR (dB)
	0.75	0.26	1.77	.46	> 8	53–63	120	100
Verma et al.[9]	1	3.5	1.3	4.55	> 700	60	60	–
Denison et al. [10]	1.8–3.3	1.8-3.3	0.95	1.71–3.13	> 8	41, 51.5	80	100
Harrison et al. [11]	+–2.5	0.9	1.6	1.44	–	39.8	> 86	> 80
Zhang et al. [6]	1.2	6.4	0.46	2.94	> 4	40–74	80	60

In addition, Fig. 2 shows an example of spectral sensitivity at 3 different amplifier-gain settings (different colors); in this case, it is easy to see the potential expansion of the dynamic range (in dB) that could be covered. The shaded region denotes the typical frequency range for EEG and is reasonably flat except on the very edges.

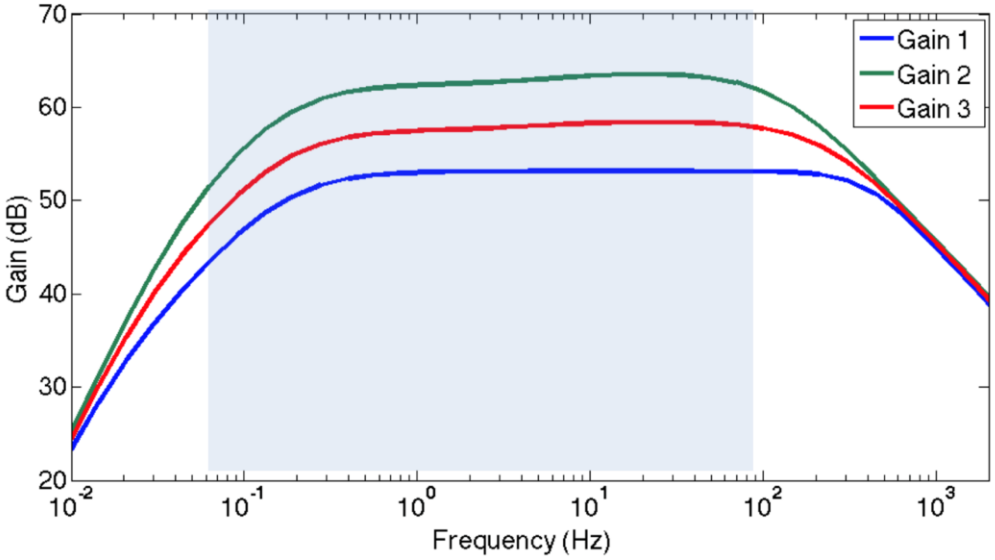

Fig. 2 Gain plots showing performances of LNA and VGA

Additionally, the effect of the DSP-mediated VOC is shown in Fig 3. In this case, a 0.33-Hz waveform, representing long-term capacitive drift common in EEG, has been superimposed on top of a 10-Hz signal (show in red). Prior to utilization of the VOC, the total dynamic range of the signal covers more than 400 µV, necessitating a very wide dynamic range and potentially clipping an ADC. However, with the VOC implementation (in blue) the range is greatly restricted and remains close to zero voltage. In this case, the VGA can be relaxed substantially;

diminishing power consumption increases the minimum vertical voltage resolution of the ADC. The functional result is performance similar to an on-line filter but with the advantage of digital-level control and dynamic tunability.

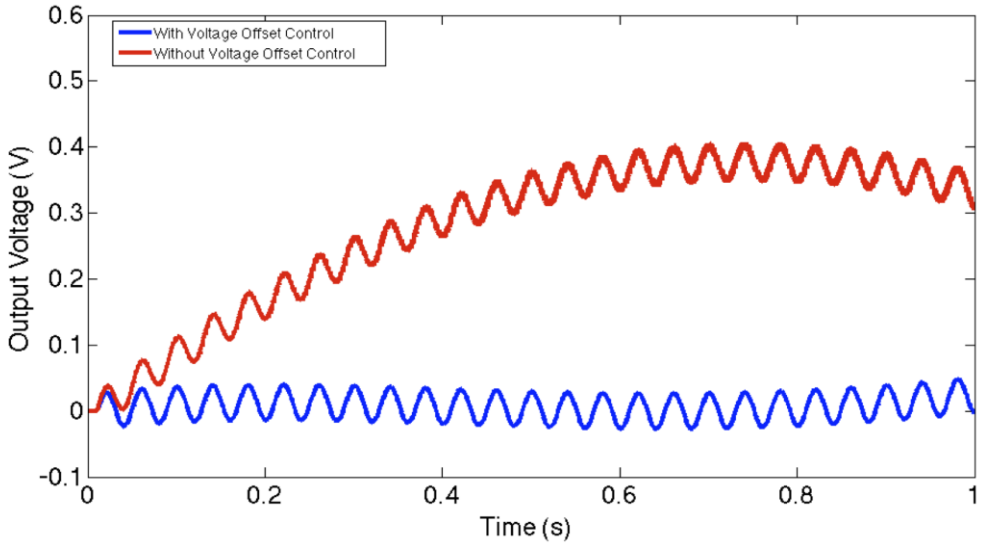

Fig. 3 Effects of VOC on dynamic range

3.2 Efficacy with EEG Application

The use of a 12-bit SAR ADC for digitization will inevitably result in decreased vertical resolution of the digitized signal, even in conjunction with the VOC/VGA modulation described above. Figure 4 shows results of an alpha-burst detection classifier described previously[8] when using data successively degraded to simulate lower-bit-rate ADCs, so that the minimum data resolution (in microvolts) increases.

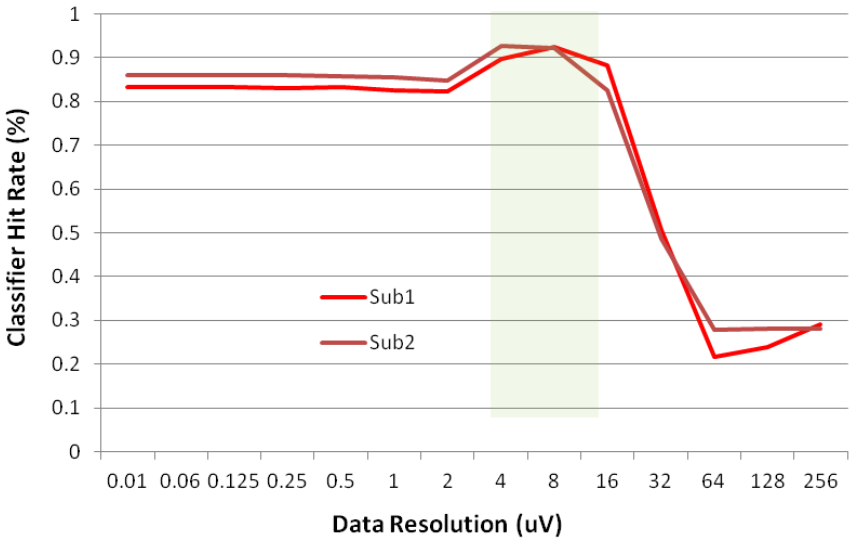

Fig. 4 Alpha-burst classifier's performance with increasing minimum resolution

Note that for both of the subject datasets tested, performance of the classifier remains relatively stable (with an unexpectedly small, but not significant, increase) up through a minimum resolution of approximately 16 µV. This suggests there is substantial room for degradation of the acquired signal before it becomes unusable for targeted applications and, more importantly, that this proposed design should work effectively in this particular case.

4. Conclusions

These efforts have demonstrated the initial feasibility of EEG data-acquisition system design using sub-V_t techniques and ultralow power-saving techniques. In this particular case we are able to show that the primary DAQ components can be created using less than 300 nanowatts per channel. At that consumption, it is very feasible to design an entire system capable of operating solely on locally harvested power. This is achieved by using sub-V_t design in combination with a novel "adapt-on-demand" approach, which dramatically conserves power by using only minimum-necessary ADC resolution for that particular moment. Aside from performance validation of the design schematics, we have verified that our novel approach is still effective for alpha-burst detection, a target application of fieldable EEG used for detecting moments of mental fatigue or drowsiness.

While promising, these initial efforts only open the door for substantial additional work. In particular, our initial attempts have focused only on the design of a single SAR ADC. Inclusion of a secondary delta-sigma ADC, as in the overall schematic, will dramatically improve overall performance while maximizing flexibility across applications. Additionally, while we have provided results verifying our design will work for a single, specific application (alpha-burst detection), there is a wide range of classification applications for which EEG would likely be used in the field. True verification will require modeling for each of several classes of uses, covering a range of applications for EEG. Such a heterogeneous approach will, in turn, enable our understanding of which statistical features of the signal are most important to consider in future iterations of low-power IC design.

5. References and Notes

1. McDowell K, Lin C-T, Oie K, Jung T-P, Gordon S, Whitaker K, Li S-Y, Lu S-W, Hairston W. Real-world neuroimaging technologies. IEEE Acc. 2013;1:131–149.

2. Lance B, Kerick S, Ries A, Oie K, McDowell K. Brain–computer interface technologies in the coming decades. Proc IEEE. 2012; 100:1585–1599.

3. Liao L-D, Lin C-T, McDowell K, Wickenden A, Gramann K, Jung T-P, Ko L-W, Chang J-Y. Biosensor technologies for augmented brain–computer interfaces in the next decades. Proc IEEE. 2012;100:1553–1566.

4. Zhang Y, Zhang F, Shakhsheer Y, Silver J, Klinefelter A, Nagaraju M, Boley J, Pandey J, Shrivastava A, Carlson E, et al. A batteryless 19μW MICS/ISM-band energy harvesting body sensor node SoC for ExG applications. IEEE J Sol-Sta Cir. 2013;48(1):199–213.

5. In this case, "dynamic range" refers to the total potential span of values that may be encountered for any given situation or record.

6. Zhang F, Mishra A, Richardson A, Otis B. A low-power ECoG/EEG processing IC with integrated multiband energy extractor. IEEE Trans Circ Sys—1: Reg Pap. 2011;58(9):2069–2082.

7. Allen P, Holberg D. CMOS analog circuit design. New York (NY): Oxford University Press; 2012.

8 Lawhern V, Kerick S, Robbins K. Detecting alpha spindle events in EEG time series using adaptive autoregressive models. BMC Neurosci. 2014;14:101–106.

9. Verma N, Shoeb A, Bohorquez J, Dawson J, Guttag J, Chandrakasan A. A micro-power EEG acquisition SoC with integrated feature extraction processor for a chronic seizure detection system. IEEE J Sol-Sta Circ. 2010;45(4):804–816.

10. Denison T, Consoer K, Santa W, Avestruz A-T, Cooley J, Kelly A. A 2 μW 100 nV/rtHz chopper-stabilized instrumentation amplifier for chronic measurement of neural field potentials. IEEE J Sol-Sta Circ. 2007;42(12):2934–2945.

11. Harrison R. A low-power, low-noise CMOS amplifier for neural recording applications circuits and systems. ISCAS 2002. Proceedings of the IEEE International Symposium on Circuits and Systems. 2002; vol.5; p.V-197–V-200.

List of Symbols, Abbreviations, and Acronyms

ADC	analog-to-digital conversion
AFE	analog front end
ARL	US Army Research Laboratory
BCIT	brain–computer interactive technology
DAQ	data acquisition
DSP	digital signal processor
EEG	electroencephalography
IC	integrated circuit
LNA	low-noise amplifier
SAR	successive approximation register
SoC	system-on-a-chip
Sub-V_t	subthreshold voltage
VGA	variable-gain amplifier
VOC	voltage offset controller

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