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ELECTRO-THERMO-MECHANICAL TRANSIENT MODELING OF STRESS DEVELOPMENT IN ALGAN/GAN HIGH ELECTRON MOBILITY TRANSISTORS (HEMTs) (POSTPRINT)

Eric R. Heller
AFRL/RXAN

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Interim Report

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14. ABSTRACT
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Electro-thermo-mechanical Transient Modeling of Stress Development in AlGaN/GaN High Electron Mobility Transistors (HEMTs)

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ABSTRACT

In this paper, we present a coupled small-scale electro-thermal model for characterizing AlGaN/GaN HEMTs under direct current (DC) and alternating current (AC) power conditions for various duty cycles. The calculated electrostatic potential and internal heat generation data are then used in a large-scale mechanics model to determine the development of stress due to the inverse piezoelectric and thermal expansion effects. The electrical characteristics of the modeled device were compared to experimental measurements for validation as well as existing simulation data from literature. The results show that the operating conditions (bias applied and AC duty cycle) strongly impact the temperature within the device and the stress fluctuations during cyclic pulsing conditions. The peak stress from the inverse piezoelectric effect develops rapidly with applied bias and slowly relaxes as the joule heating increases the device temperature during the on state of the pulse leading to cyclic stresses in operation of AlGaN/GaN HEMTs.

KEY WORDS: AlGaN/GaN HEMTs, transient, pulsed devices, electro-thermo-mechanical simulation

NOMENCLATURE

V_{gs}	Applied Gate Voltage
V_{ds}	Applied Drain Voltage
I_{ds}	Drain-to-Source current
MPa	Megapascals
σ_{xx}	x-Component of Stress

INTRODUCTION

Gallium nitride (GaN) based high electron mobility transistors (HEMTs) have recently been under intense research and are becoming attractive devices for high voltage and high-power applications at radio frequencies (RF). Although GaN has lower maximum electron drift mobility compared to GaAs based devices, GaN has a larger peak electron velocity, larger saturation velocity, higher breakdown voltage, and better thermal stability – all of which contribute to making these devices very suitable for RF power devices [1]. Development and fabrication of reliable AlGaN/GaN HEMTs has significantly advanced in recent years to enable the production of high quality, commercially available devices in a wide variety of high power and high frequency applications. To further study these devices, it is important to investigate the reliability physics associated with AlGaN/GaN HEMTs. Several researchers have previously outlined degradation mechanisms within these devices, but the underlying mechanisms for degradation has yet to be fully understood [2-4]. Electrical degradation is characterized by the onset of gate leakage in the device, loss of power added efficiency, current collapse, change in transconductance, and gate current noise [2, 5, 6]. In addition, physical mechanical degradation in the form of cracking or pitting of devices around the edges of the gate contact has been reported in [2, 5-8]. This is not unexpected in that there are a number of large sources of stress and strain that are most active near the drain edge of the gate footprint. Electric fields and inverse piezoelectric generated mechanical stress contributions will typically peak here [5] as well as temperature gradients from non-uniform and bias dependent heating [9] which generate stress through thermal expansion. Complicating the issue, this same region is usually at the junction of low coefficient of thermal expansion SiN, high coefficient Au gate metal and middle valued III-N semiconductor and separately will also be highly affected from any built in stress in the overlayers (SiN in particular can be deposited in a highly stressed state) [10] and of course the AlGaN layer has large amounts of tensile strain from pseudomorphic growth on GaN.

With these many competing effects it is critical to be able to separate the distinct contributions to the stress and strain so as to be able to understand the physics of failure within the device. While temperature, stress, and strain profiles have been extensively studied using numerical multi-physics coupled simulations [4, 11, 12] and experimentally during DC electrical testing [2, 13], few have studied the transient stress development even though these devices have numerous applications in the RF regime [14].

In this work, an electro-thermo-mechanical model is presented to predict the development of stress within a device under RF conditions. In doing so, the magnitude and distribution of stress present in a device while under cyclic bias conditions is revealed. In particular, our method allows transient components (from near gate edge thermo-elastic, inverse piezoelectric) to be convincingly separated from and measured independently of the steady-state contributions (from steady-state temperature rise and temperature gradients, pseudomorphic growth, and built-in process stress).

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DEVICE STRUCTURE

Figure 1 represents the simplified device structure of an AlGaN/GaN HEMT. Devices are constructed by first depositing a thin nucleation layer on a SiC substrate for the semi-insulating GaN layer. After depositing the GaN layer, a thin layer of AlGaN is pseudomorphically grown on top of the GaN layer. Pseudomorphic growth induces large amounts of tensile strain within the AlGaN layer due to lattice mismatch with the GaN layer resulting in stresses over 1 GPa in the AlGaN layer [2]. The gate is centered between the source and drain ohmic contacts, with Si_3N_4 passivation. This layer is critical for device performance by greatly reducing dispersion between the large signal AC and DC characteristics of the HEMT device [15-17].

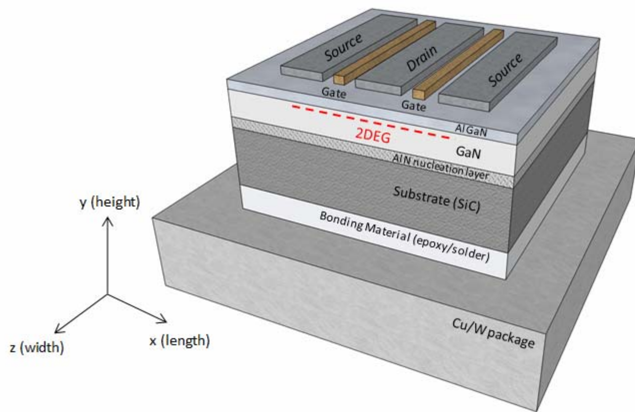

Figure 1. Representative device structure of an AlGaN/GaN HEMT including substrate, bonding, and package materials. Devices were Si_3N_4 passivated (not shown).

Spontaneous and piezoelectric polarization effects in the AlGaN and GaN layers result in a positive charge in the AlGaN layer near the interface. To compensate for the positive charge, a tightly confined 2 dimensional electron gas (2DEG) develops approximately 80-100 Angstroms (Å) below the AlGaN/GaN interface in the GaN layer which has a lower bandgap than the AlGaN layer [18]. This 2DEG layer imparts the large current carrying capability in AlGaN/GaN HEMTs and has been shown to have sheet carrier concentrations up to 2×10^{13} cm^{-2} without doping [1]. The conduction of this channel and thus the power dissipated by the device is controlled by the applied drain and gate biases (V_{ds} and V_{gs}, respectively). When a negative V_{gs} bias is applied, the 2DEG becomes depleted and conduction of current is reduced. Further decreasing V_{gs} will completely deplete a section of the 2DEG, yielding a "pinchoff" state where power is not dissipated by the device. Under pulsed conditions, a single cycle consists of an OFF-state period where no power is supplied to the device, followed by an ON-state period where power is supplied to the device and the device heats due to joule heating. The percentage of a single cycle in which the device is powered is called the duty cycle.

MODEL DESCRIPTION

A combination of two modeling packages (a small-scale electro-thermal model and large-scale mechanics model) was used to construct a complete electro-thermo-mechanical model of AlGaN/GaN HEMTs. First, the electro-thermal behavior in 2 dimensions was captured using drift-diffusion electron and hole carrier equations using the commercially available Sentaurus Device simulator [19]. This model was used to determine the coupled electrical and thermal response of 2-finger, gate-centered, AlGaN/GaN HEMT test devices. This software couples the electron and hole transport equations with the thermodynamic model to obtain the current densities within a semiconductor device. In doing so, it is possible to determine the electric potential distribution and joule heating profile within the device as a function of bias conditions. The validity of using this software to accurately model these devices has been demonstrated previously in [9, 20, 21].

The material properties and inputs for the electro-thermal model including temperature dependent thermal conductivities, heat capacities, and temperature- and mole-fraction-dependent semiconductor band gaps have been taken from [21] and [22]. The overall thermo-electric model structure includes a silicon carbide (6H-SiC) substrate for a single channel of the device (symmetry line exists through the center of the drain contact in Figure 1). The ohmic (source and drain) and Schottky (gate) contacts were modeled as thin gold (Au), with the inclusion of a 20 nm thick layer of Ni under the gate. The thicknesses of the AlGaN and GaN layers were assumed to be 20 nm and 1.8 μm, respectively.

Special attention was paid to the channel dimensions (source-to-drain, source-to-gate, and gate-to-drain), which were determined from optical and scanning electron microscope (SEM) images. The gate has a T-gate structure with a nominal length (footprint on the AlGaN layer) of 0.5 μm, and the gate connected field plate (GCFP) on the source and drain sides were 0.25 μm and 0.3 μm, respectively. Electrical contacts were defined around the perimeter of the ohmic and Schottky contacts.

For AlGaN/GaN Ga-face HEMT devices, the 2DEG comes from spontaneous and piezoelectric polarization induced positive charge at the AlGaN/GaN interface which pulls the conduction band down to the Fermi level, and does not require dopants as for example in AlGaAs/GaAs devices. We use a charge of 2.0×10^{-6} C/cm^2 from an interpolation of results from Ambacher *et al.* [1] for our AlGaN mole fraction. To a good approximation this is a fixed and uniformly-distributed surface charge density at the AlGaN/GaN interface. Since the electro-thermal model is small-scale (i.e. does not include a full substrate), a thermal resistance of 0.002 cm^2KW^{-1} was applied to the bottom of the SiC area to simulate the full substrate of an actual device. Packaged devices, similar to Figure 1, can contain multiple layers including a die attach solder material, device package frequently of Cu/W mixture, and a mounting plate [21]. The thermal resistance value was determined through matching of experimental I_{ds}-V_{ds} curves with the developed numerical model values, which is shown in Figure 3. The bottom of the modeled structure is held at 300 K and all other boundaries are assumed to be adiabatic.

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To directly calculate the mechanical response of the modeled device, the electrical potential and the thermal heat generation distributions were transferred to a large-scale model developed in COMSOL Multiphysics to calculate the stress and strain profiles for given bias conditions. The workflow for combining the two modeling packages is shown in Figure 2.

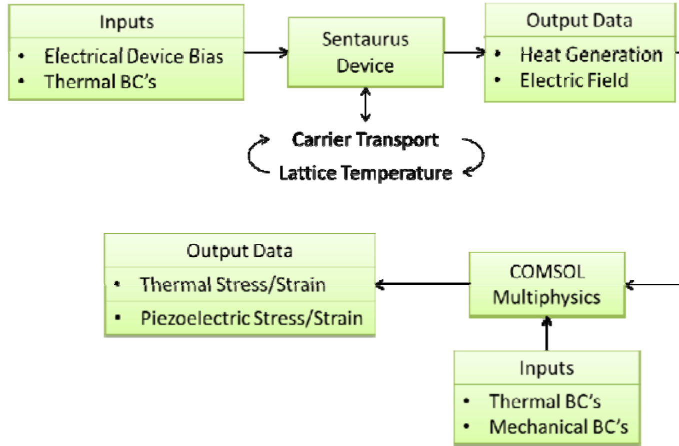

Figure 2. Coupled small-scale Sentaurus Device and large-scale COMSOL Multiphysics modeling procedure to create a electro-thermo-mechanical model. COMSOL includes a more representative device structure including mechanical boundary conditions (BC's) to determine the corresponding stress and strain profiles within a device.

This approach to modeling allows for the decoupling of the thermal and piezoelectric stress and strain profiles as demonstrated in [4]. The COMSOL material properties including anisotropic stiffness matrices and temperature dependent conductivities have been taken from [21] and electrical properties including permittivity and piezoelectric coefficients have been taken from [4]. The large-scale mechanical model used identical device dimensions and material properties, but included a full 120 µm (height) x 300 µm (length) SiC substrate. Both the GaN and Si_3N_4 layers extend the full width of the SiC substrate. Similar to the Sentaurus Device model, a thermal boundary of 300K was applied to the bottom of the SiC substrate and adiabatic boundary conditions were placed on all other surfaces, including the symmetry line through the center of the drain. A fixed mechanical boundary condition was placed on the bottom of the package and an x-direction fixed mechanical boundary condition was placed along the symmetry line, which is consistent with [21], and all other surfaces are unrestrained.

RESULTS AND DISCUSSION

DC Results

The numerical model was validated by comparing the simulated and experimental I_{ds}-V_{ds} responses under DC bias. The results are shown in Figure 3. Good agreement was seen between the numerical model and the experimental data across a broad range of bias conditions (V_{gs} ranges from -3 V to +1 V). Dotted and solid lines correspond to the numerical model and experimental results, respectively. In addition, the model effectively accounts for the current "droop" due to the joule heating within the device [13].

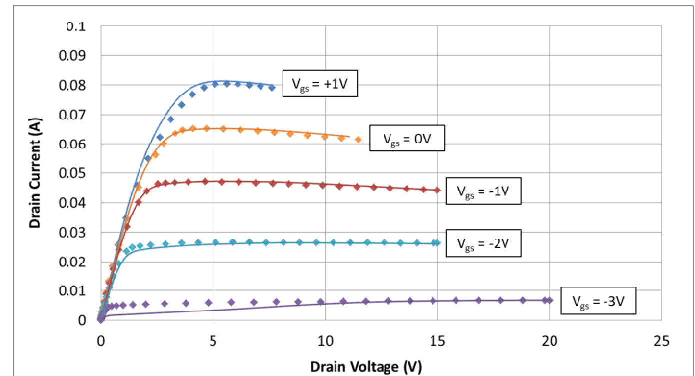

Figure 3. Comparison of numerical and experimental device characteristics showing model accuracy across a wide range of bias conditions. Numerical model (dotted) captures the electrical characteristics of a device including the current droop caused by self-heating within the device.

To further validate the model, two bias conditions of equal power dissipation (6 W/mm) were compared to determine the temperature rise in a device as a function of bias conditions. Previous work has shown that the temperature in these devices will have a strong bias dependence due to the confinement or spreading of the heat generation region [20, 23]. In this work, V_{ds} and V_{gs} were 48 V and -2.68 V, respectively, for the first case, and 28 V and -2.2 V, respectively, for the second. Figure 4 shows the temperature profile across the AlGaN/GaN interface for these two cases. These results are consistent with similar numerical models from literature [20]. The model predicted a 7 K higher peak temperature for the 28 V_{ds} case, even though the power dissipation was equal. In addition, the higher drain bias of 48V shifts the temperature location to be further away from the gate edge and towards the drain ohmic contact (to the left in Figure 4) by approximately 150nm, being on the order of the gate length.

Modeling results showed that higher electric fields were seen for the 48 V_{ds} case, as shown in Figure 5. For GCFP devices, two peaks in electric field exist: one on the drain side of the gate at the GCFP corner and another under the GCFP around the AlGaN/GaN interface on the drain side. The 48 V_{ds} case, however, has a larger distribution of electric field at the GCFP corner and extends to the AlGaN/GaN interface in the device channel. Higher stress and strain values due to the inverse piezoelectric effect are expected in the 48 V_{ds} case because of the larger electric fields, while higher thermoelastic stress and strain is expected for the 28 V_{ds} case because of the higher peak temperature.

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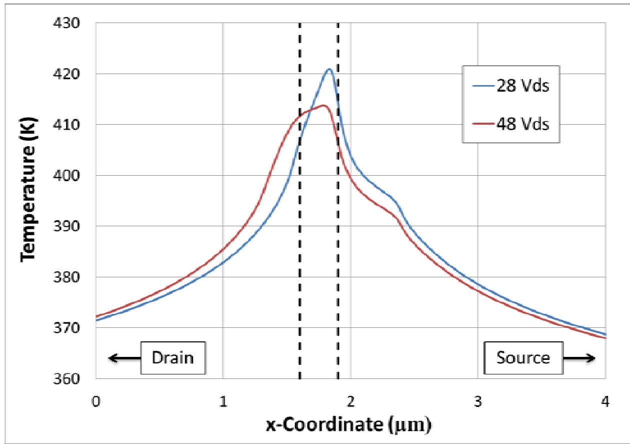

Figure 4. AlGaN/GaN interface temperature profile for a DC drain voltage of 48V and 28V and DC gate voltage of -2.68V and -2.2V. Dashed vertical lines correspond to the GCFP edge on the drain side (left vertical line) and the gate footprint edge (right vertical line).

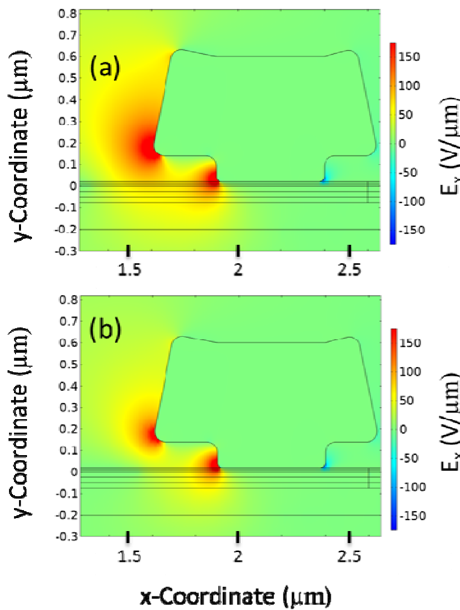

Figure 5. x-Component of the electrical field distribution (E_x) in V/µm for a DC drain voltage of 48V (a) and 28V (b).

AC Results

Next, the response of the AlGaN/GaN HEMTs to pulse conditions was determined. The simulated device was pulsed at 48 V_{ds} at a constant gate bias of -2.68 V_{gs} and duty cycle of 50% at 100 kHz frequency from a starting temperature of 300 K to characterize the development of stress in the device. The model assumed a transition period length of 100 ns from OFF-state, where V_{ds} = 0 V and V_{gs} = -2.68 V, to ON-state, where V_{ds} = 48 V and V_{gs} = -2.68 V. This creates a rapid shift in voltage to simulate actual operating conditions. The transition period begins at a time corresponding to 4.95e-6 seconds and reaches the desired 48 V_{ds} at a time of 5.05e-6 seconds for the first pulse. Similarly, the transition from ON- to OFF-state occurs from 9.95e-6 seconds to 10.05e-6 seconds. The applied V_{ds} value changes rapidly compared to the thermal response of the device. Because of this, the bulk of the piezoelectric portion of stress is expected to develop almost instantaneously because of the sudden voltage potential rise, while the thermal contribution to stress will increase throughout the ON-state portion due to the joule heating in the device. Because of the electro-thermal coupling, it is expected for both the electrical and thermal profiles to change throughout the ON-state portion of the pulse.

Figure 6 shows the x-component of piezoelectric stress along the AlGaN/GaN interface from just before the ON-state V_{ds} pulse (time = 4.95e-6 seconds), to just before the end of the ON-state (time = 9.95e-6 seconds). During the OFF-state and prior to the V_{ds} pulse, stress is nearly symmetrical around the gate. At this time, electrical potentials on both the drain (left of the gate) and source (right of the gate) are 0 V, leading to an equivalent electrostatic potential on either side of the gate structure. This profile is not exactly symmetrical, however, because the gate structure itself is not symmetrical. As the drain bias rapidly increases, the peak stress along this interface shifts towards the drain side of the gate structure.

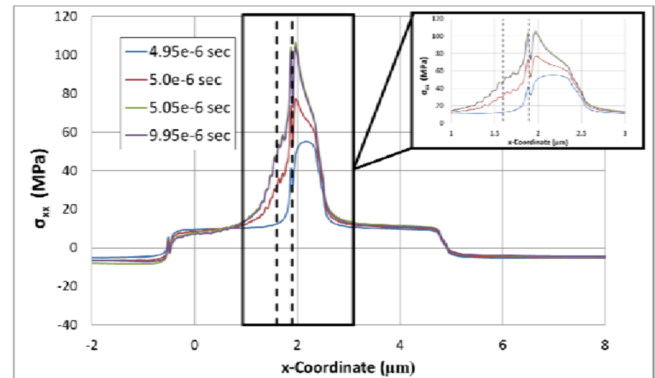

Figure 6. x-Component of piezoelectric stress along the AlGaN/GaN interface for a single pulse. As with Figure 4, vertical lines correspond to the GCFP and gate footprint edges on the drain side of the device.

The peak corresponds to under the gate footprint, near the peak electric field located at the AlGaN/GaN interface shown in Figure 5 (a). At this location, the electrostatic potential within the AlGaN (and GaN) layer rapidly changes from the applied 48 V_{ds} to a value influenced by the -2.68 V_{gs}. It should also be noted that little change is seen in Figure 6 between the 5.05e-6 sec time (which corresponds to right after the 48 V_{ds} is reached) and the 9.95e-6 time (which corresponds to nearly the end of the pulse). This is caused by the sharp increase in electric potential of the device in response to the sudden increase in V_{ds}. From the OFF-state to the ON-state, over 50 MPa increase in stress state at the AlGaN/GaN interface is seen. In addition, the peak location of the maximum stress state shifts towards the drain ohmic contact by 0.2 µm. This is not the maximum amount of piezoelectric stress induced in the device, but rather the x-component of stress at the AlGaN/GaN interface. The peak x-component of stress in the device occurs within the AlGaN layer where the electric field is highest. In the OFF- state, the peak x-component of stress is found to be at the gate footprint

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edge on the drain side with a value of 127 MPa, and increases to 288 MPa by the end of the ON- state. The OFF-state stress is attributed to the negative applied gate voltage, which is held constant during V_{ds} pulses.

The thermal response due to the joule heating lags behind the piezoelectric. Figure 7 (a) and (b) show the temperature gradient and x-component of thermoelastic stress, respectively, at the AlGaN/GaN interface for the same time steps from Figure 6.

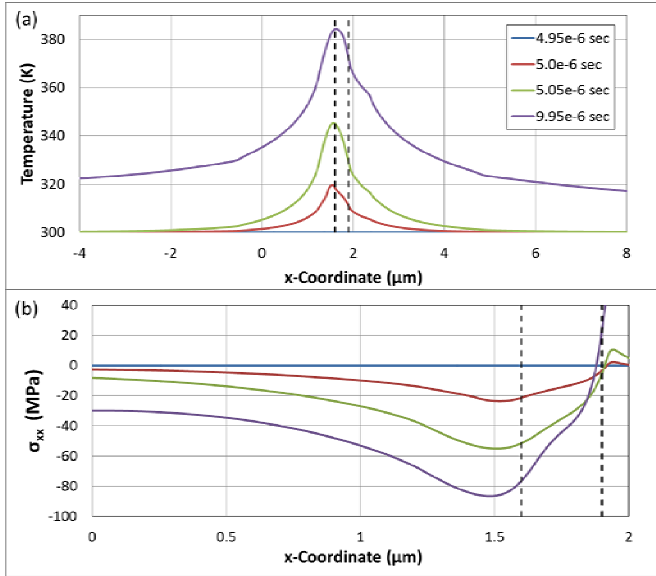

Figure 7. AlGaN/GaN interface temperature (a) and x-component of thermoelastic stress (b) during the ON-state of the first V_{ds} pulse.

As with the piezoelectric stress, these values do not represent the maximum amount of thermoelastic stress in the device. The maximum and minimum x-component of thermoelastic stress is found to be 160 MPa and -83 MPa, respectively. The piezoelectric portion of stress is present immediately after the 48 V_{ds} value is reached, while the magnitude of thermoelastic stress increases during the entire ON-state. Similar to the piezoelectric stress, the peak temperature and stress points shift toward the drain ohmic contact during the ON-state pulse.

These results indicate the stress along this interface is not only under cyclic loading due to the OFF- and ON- states, but also the maximum point location of stress is changing throughout the duration of the ON-state. The thermoelastic stress, however, is compressive whereas the piezoelectric stress is tensile. Because of this, the stress along the AlGaN/GaN interface relaxes during the ON-state because of the joule heating. Figure 8 shows the stress at a point corresponding to directly under the GCFP edge along the AlGaN/GaN interface as a function of time. As before, this does not account for additional residual stress within the devices as a result of fabrication and lattice mismatch.

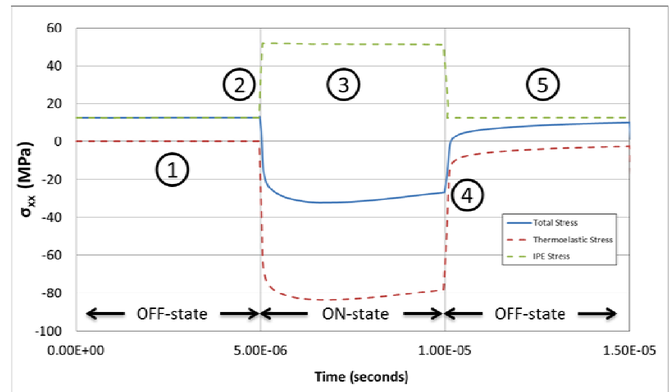

Figure 8. Representative stress profile at the AlGaN/GaN interface due to intrinsic, piezoelectric, and thermal stresses throughout V_{ds} pulsing of the device.

Prior to the first pulse and in the OFF-state, stress exists due to the gate bias corresponding to location ①. Nearly immediately after the ON-state, further tensile stress is induced because of the inverse piezoelectric stress effect of the AlGaN and GaN materials caused by the applied bias condition ②. Simultaneously, the device begins to rapidly heat, yielding a compressive stress. During the ON-state ③, the device relaxes due to the thermoelastic stress until the OFF-state from ④ to ⑤, where the tensile strain due to the inverse piezoelectric stress is removed. Throughout the OFF-state, the device cools, returning to the initial intrinsic stress within the device. For Figure 8, the point chosen corresponds to nearly the center of the hottest point within the device, which is why the rapid transition in thermoelastic stress is seen. If a point closer to the drain is chosen, then the rapid increase in tensile stress from the inverse piezoelectric effect will be seen, but the relaxation due to joule heating will develop slower than is represented in Figure 8.

The amount of relaxation due to the thermoelastic stress is directly dependent on the duty cycle. As previously mentioned, the results presented are for 50% duty cycle. If, for instance, a duty cycle of 5% or less was chosen, the majority of cyclic stress would be due to just the inverse piezoelectric effect, and little relaxation would occur. As evident from Figures 6 and 7, discrete points along the AlGaN/GaN interface will undergo varying levels of cyclic stress due to the inverse piezoelectric and thermoelastic stress occurring.

Figure 9 represents the combined inverse piezoelectric and thermoelastic stress in the device at the time corresponding to 9.95e-6 seconds (end of ON-state). Here, the maximum x-component of stress in the device exists at the corner of the gate footprint on the drain side and is found to be around 375 MPa.

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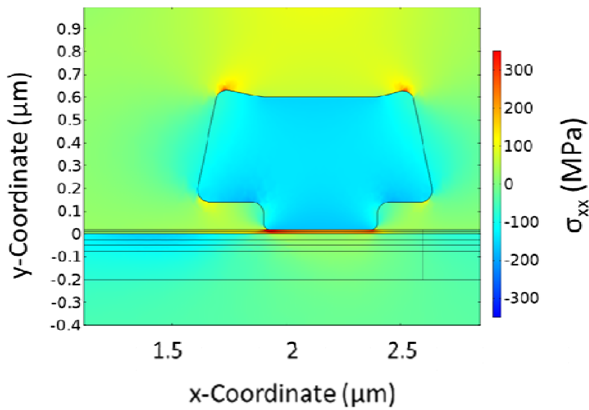

Figure 9. Stress distribution due to thermal and piezoelectric effects at the end of the first ON-state pulse. High amounts of stress exist underneath the gate footprint as a result of high electric field and CTE mismatch of AlGaN, GaN, Au, and Si_3N_4 layers.

This is due to the large electric fields and coefficient of thermal expansion mismatch of the Si_3N_4, AlGaN, and Ni/Au materials around this point. It has been previously shown that the intrinsic stress plays a large role in the onset of degradation within the device [4] and increasing the tensile load within the AlGaN makes this layer vulnerable to mechanical failure [24]. Reference [4] calculated the intrinsic stress within AlGaN layer in the region of the gate edge to be around 3 GPa for AlGaN/GaN HEMTs on SiC substrates with degradation expected around a combined intrinsic, inverse piezoelectric, and thermoelastic stress of 3.75 GPa. It should be noted that the degradation point will be different between varying device structures, but bias conditions and cyclic loading of the device will contribute to degradation of the device if the combination of intrinsic, inverse piezoelectric, and thermoelastic stress exceeds the expected degradation point for the device. The stresses at the beginning of the pulse in the device occur from residual + inverse piezoelectric stresses in the AlGaN layer. However, these stresses are relaxed upon joule heating, but the CTE mismatch between the gate metal and the AlGaN layer induces an additional stress. Thus, for devices which are cycled at a low duty cycle versus high duty cycle, differences in failure rates may occur not simply due to heating, but due to the peak in stress states and where they occur in the device.

CONCLUSION

Two dimensional electro-thermo-mechanical simulations were conducted to determine the magnitude and development of stress profiles within an AlGaN/GaN HEMT under pulsed bias conditions. It was found that during the ON-state of a device under pulsed conditions, tensile stress between the AlGaN/GaN layers quickly rises and shifts towards the drain side of the gate edge due to the inverse piezoelectric effect. This is attributed to the sharp rise in drain bias and change in electrostatic potential within the device from V_{ds} to V_{gs}. During the ON-state, this stress is relaxed by the compressive thermoelastic stress, which builds during the ON-state due to joule heating. It was shown that the peak from the inverse piezoelectric stress effect and thermoelastic stress change in magnitude and position between localized areas under the gate structure to the gate foot print during pulsed operations which may lead to duty cycle dependent degradation rates in AlGaN/GaN HEMTs.

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