A HIGH FREQUENCY MOSFET DRIVER FOR THE TITAN FACILITY AT TRIUMF[*]

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Abstract

TRIUMF's Ion Trap for Atomic and Nuclear Science (TITAN) Radio Frequency Quadrupole (RFQ) Beam Cooler is a device cools and collects short-lived isotopes, with half-lives as short as 10 ms, created by an Isotope Separator and Accelerator (ISAC). An RF square wave driver (RFSWD), that must have rise and fall times of less than 125 ns (10% to 90%), performs 2-dimensional focusing of the ion beam within the RFQ, along planes normal to the beam's intended trajectory, to confine ion motion along a stable path; hence the ions can be trapped and collected for extraction. The RFSWD, which is based on previous kicker designs developed at TRIUMF [1], employs stacks of MOSFETs, operating in push-pull, to generate High Voltage (HV) rectangular waveforms at a prescribed frequency and duty cycle. Currently a 500 V, 2 MHz drive system is undergoing tests, however, the system configuration allows for operation with higher voltage amplitudes and a repetition rate from 300 kHz up to 3 MHz, continuous. Technical details of the design, operation and performance of the RFQ system, in particular of the drive system, are presented.

I. INTRODUCTION

The TITAN group is developing a state-of-the-art Penning trap facility to exploit the high intensity beams of exotic nuclei at the TRIUMF ISAC facility. This system will be used to measure the mass of exotic isotopes to a very high accuracy [2]. The resolution of the isotope mass measurements is proportional to the charge state of the ions [3]. The RFQ is a "first line" beam-processing device that converts a continuous ion beam into a series of cool bunches at a prescribed rate. This allows for efficient injection into post apparatus that operates with a preset duty cycle, i.e. the apparatus accepts beam only for a particular time period.

An RF square wave voltage, applied to four semicircular poles (Fig. 1), is used to provide radial confinement of the ions [2]. The poles are segmented into electrodes, to allow for the application of a longitudinal electric field, to control the motion of the ions in the third dimension. Once "trapped" the ions are cooled via interactions with an inert buffer gas such as helium. The ions are then extracted from the trap in bunches [2].
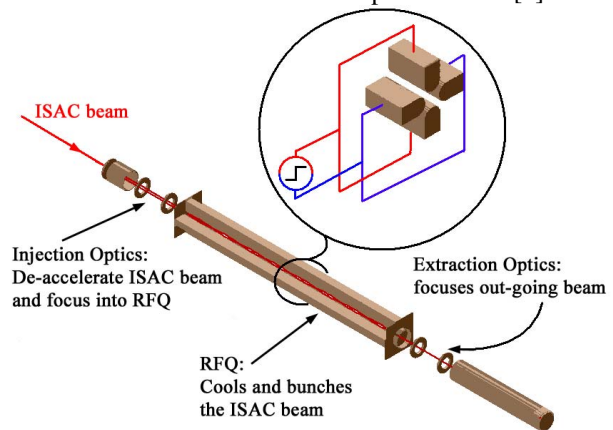
Figure 1. RFQ structure and optics.

The stability parameter of the ions in the RFQ is proportional to the charge to mass ratio multiplied by the voltage and divided by frequency[2]. Hence if the voltage is increased, to store more ions by increasing the space charge limit of the trap, then frequency must be increased.

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14. ABSTRACT

TRIUMFs Ion Trap for Atomic and Nuclear Science (TITAN) Radio Frequency Quadrupole (RFQ) Beam Cooler is a device cools and collects short-lived isotopes, with half-lives as short as 10 ms, created by an Isotope Separator and Accelerator (ISAC). An RF square wave driver (RFSWD), that must have rise and fall times of less than 125 ns (10% to 90%), performs 2-dimensional focusing of the ion beam within the RFQ, along planes normal to the beams intended trajectory, to confine ion motion along a stable path; hence the ions can be trapped and collected for extraction. The RFSWD, which is based on previous kicker designs developed at TRIUMF [1], employs stacks of MOSFETs, operating in push-pull, to generate High Voltage (HV) rectangular waveforms at a prescribed frequency and duty cycle. Currently a 500 V, 2 MHz drive system is undergoing tests, however, the system configuration allows for operation with higher voltage amplitudes and a repetition rate from 300 kHz up to 3 MHz, continuous. Technical details of the design, operation and performance of the RFQ system, in particular of the drive system, are presented.

15. SUBJECT TERMS

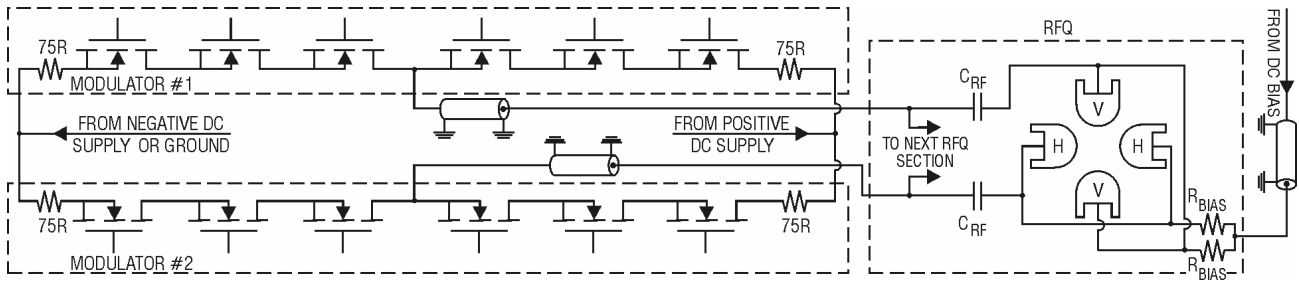| 16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT	18. NUMBER OF PAGES	19a. NAME OF RESPONSIBLE PERSON
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Figure 2. RFSWD H-Bridge Modulator and RFQ.

Present technology uses sinusoidal waveforms, amplified by an RF amplifier, coupled to the electrodes using passive elements (inductors, capacitors, ferrite cores etc.). Coupling via a resonant circuit results in very narrow bandwidth requiring retuning of the system every time there is a need to alter the frequency of operation, or change the load, in order to achieve constant amplitude over the required frequency range. Manual tuning of conventional systems is tedious and cumbersome.

The RFQ driver developed for the TITAN system is capable of generating a rectangular voltage waveform with a variable duty cycle and pulse repetition rate up to 3 MHz. This system has a flat frequency response that is load independent within its operational specifications. Unlike conventional RF ion device drivers, this system does not need to be tuned for a specific load and impedance matching networks are not required.

II. SYSTEM OVERVIEW

A. Driver

The HV RFSWD developed for TITAN's RFQ Ion Trap generates two square wave signals of opposite phase at a pulse repetition rate of up to 3 MHz, continuous, with rise and fall times of less than 125 ns.

The design of the RFSWD is based on ±12.5 kV, 75 kHz, modulators developed at TRIUMF for the MuLan experiment at the Paul Scherrer Institut (PSI) in Northern Switzerland [1,4]. The TITAN RFSWD consists of two modulators (Fig. 2). Each modulator contains two stacks of FETs with 3 FET cards per stack. Hence there are presently a total of 12 FETs for the two modulators

The four stacks are in an H-bridge arrangement (Fig. 2). The two FET stacks in a modulator operate in "push-pull" mode: when one stack is on the other stack is off. The three FETs closest to the positive DC supply and the three FETs closest to the negative DC supply (or ground), in each modulator, form the "pull-up" (PUP) and "pull-down" (PDN) stacks, respectively. Each modulator drives two opposite poles of the RFQ (Fig. 2). When the PUP (PDN) stack is turned on, ~40 ns after turn-off of the PDN (PUP) stack, the voltage swing at each modulator output is equivalent to the supply voltage. Each signal is fed to the RFQ via a 50 Ω SHV cable and an SHV connector (4.7 pF) mounted on the RFQ tank: a capacitor C_{RF} (Fig. 2) couples the signal to pairs of electrodes.

The FET cards used for the RFSWD are very similar to those developed for MuLan [1]. The only differences relate to the higher repetition rate of the RFSWD:

- A capacitive load is being driven, hence the losses in each FET mainly occur during turn-on. The increased repetition rate results in higher losses and hence the surface area of the heat sink is increased from 24.6 cm^2 to 167.5 cm^2 by adding fins [5]. The new heat sink results in a temperature rise of 10°C with a dissipation of 70 W per FET and an airflow of 800 linear feet per minute [5].

- The total effective output capacitance of the FET driver and input capacitance of the FET is 11 nF with 0 V drain to source [1]. The average current drawn by the FET and driver is, for a given supply voltage (~16 V) and Miller charge, proportional to the repetition rate. Hence, to allow for 3 MHz operation of the RFSWD, resistor R10 (Fig. 3), which was 4.7 Ω and 0.25 W [1], is now a 1.2 Ω, 1 W, resistor.
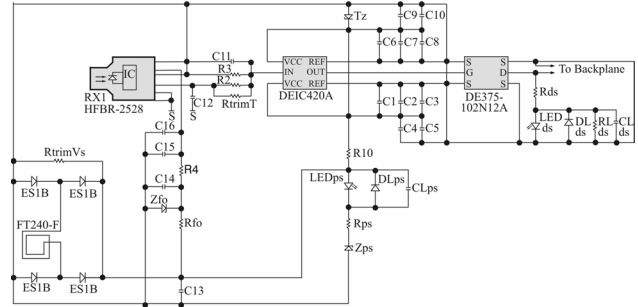

Figure 3. Electrical schematic of a 1 kV MOSFET card.

The FET used on each card is the DE375-102N12A from DEI [6]: a DEIC420 FET driver is used to directly drive the DEI FET. The power for each FET driver is derived by magnetically coupling energy to a gate-source power supply via a ferrite [1]. The primary pulse current is ~2.2 A, with fast rise and fall times. The primary current is derived from a 240 V power supply: a series 60 Ω resistance and a DE375-102N12A FET generate the current pulse. For the MuLan kicker system the 2.2 A, 1 μs wide, pulse is at a fixed rate of 90 kHz [1,4]. However since the RSWFD can operate, continuously, at any frequency in the range from 300 kHz to 3 MHz, the required repetition rate of the primary current pulse is set by the control system depending upon the required rate of the RSWFD [5].

An HFBR-2528 fiber optic receiver from Agilent is used to provide the turn-on and turn-off trigger signal to each FET driver. This receiver provides a CMOS/TTL

output (and is therefore compatible with the TTL input of the DEI FET driver) and is specified over an operating range from DC to 10 MBd. The DC rating minimizes the susceptibility to erratic switching due to noise. The receiver is sensitive to electric fields and is hence covered with a copper shield, which is at source potential.

The relative switching times of the FETs affects power dissipation in each FET [1]. Ideally, the three cards in a stack will turn on simultaneously, i.e. the cards in a stack will have equal propagation delays between the inputs to the fiber optic transmitters to the collapse of drain to source voltages on the FETs. The fiber optic receivers are the most significant source of differences in relative timings [1]: a capacitor (C11 in Fig. 2), on each FET card, is used to trim this propagation delay to synchronize the switching of all FETs in a stack [1]. Time trimming, however, does not compensate for pulse width distortion (PWD). A programmable delay line allows for the turn-on drive to the transmitters to be delayed relative to the turn-off. This allows the effect of PWD in the receivers to be compensated for so that there is no overlap between the conduction of the pull up and pull down stacks [1].

B. RFQ Structure

The RFQ (Fig. 4) has 4 stainless steel poles of length 0.7 m. Each pole consists of 24 electrodes, separated by 0.5 mm gaps. The shortest electrodes are 8 mm long, and the longest electrodes are 40 mm long. Electrical isolation between adjacent electrodes is necessary for independently assigning DC potentials to the electrodes in order to form the trapping potential. The 24 electrodes of each pole are secured to a U-shaped ceramic insulator (Fig. 4). In the present design the four insulators are secured to three stainless steel support frames (Fig. 4) attached to the RFQ box lid: the support frames and box are at ground potential. The ceramic insulator is used to electrically isolate the electrodes from the support frames.

The output from a modulator is connected, via an hermetically sealed SHV connector on the RFQ tank, to a busbar that spans the length of a pole. There are 2 busbars: one for each set of opposite poles. The horizontal poles ("H") and vertical poles ("V") are shown in Fig. 2. The last 3 electrodes (electrodes 22 to 24), of each set of poles, are referred to as extraction electrodes. The value of the coupling capacitor, C_{RF}, is 220 pF for the 22nd and 24th electrodes and 5.6 nF for each of the other 22 electrodes per pole pair. Each of the 44 coupling capacitors for all the electrodes except 22 and 24 connect one of the busbars to an electrode in each of two opposite poles (Fig. 2). Each of the 4 coupling capacitors for electrodes 22 and 24 couple from a pair of these electrodes to an SHV connector: electrodes 22 and 24 are pulsed independently of the other electrodes [7].

A DC coupling resistor (R_{BIAS} in Fig. 2) connects from a set of horizontal electrodes to an SHV connector: similarly a DC coupling resistor also connects from the corresponding set of vertical electrodes to the same SHV connector (Fig. 2). Hence DC bias is applied from one SHV connector to both a horizontal set and vertical set of electrodes (Fig. 2): there are a total of 24 SHV connectors for applying DC bias. The voltage swing on a pole, during charging and discharging, is equal to the supply voltage. The poles are charged from their bias level minus half the supply voltage to their bias level plus half the supply voltage, and then discharged to their bias level minus half the supply voltage.
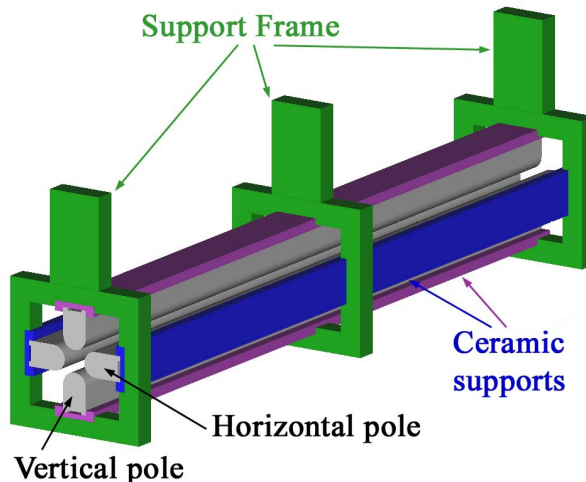

Figure 4. RFQ structure showing 4 poles, ceramic insulators and window frame supports.

C. Main Circuit

Since the poles of the RFQ are capacitively coupled to the modulator output by capacitor C_{RF} (Fig. 2) the voltage swing, rather than the absolute voltage, at the output of the modulator is important. Therefore one of the DC supplies (Fig. 2) can be replaced by a connection to ground. Presently a single positive 600 V, 2 A, DC supply charges storage capacitors: these capacitors provide the pulse current to the RFQ load. The total capacitive load consists of the RFQ structure, the off-state FET stacks, and parasitic capacitances to ground of the FET stacks turning on [7]. The DE375-102N12A FET is rated at 72 A pulsed. For operation at 1 kV peak-peak, a resistance of 13.9 Ω would limit the current to a maximum of 72 A. However the current limiting resistor has a value of 75 Ω (Fig. 2). This value limits the power dissipation in the FETs while still satisfying the required rise/fall times of 125 ns. PSpice simulations show that the 75 Ω resistors dissipate approximately 80% of the total power dissipated in the system [7]. The 75 Ω non-inductive resistors are type 886SP, from Kanthal Globar [8] and are rated at 90 W each, average power dissipation, at an ambient temperature of 40°C [8]. Airflow of 800 linear feet per minute increases the power rating of the 75 Ω resistors to approximately 200 W: this rating permits the RFSWD to generate 1 kV pulses at 540 kHz, continuous.

III. CAPACITANCE OF RFQ

The capacitance of the RFQ directly affects the rise and fall times of the pulse voltage at the RFQ poles, the

losses in the RFSWD, and the rating of the power supplies. Simulations of the RFQ have been carried out using 3D code Coulomb [9] and the predictions were used as a basis for modifying the original RFQ structure. Originally, the support frame was a solid stainless steel bar spanning the pole length. The solid frame design presented 33% of additional effective capacitance to ground compared to the present design (three 19 mm long window frame supports) [7]. The solid support frame would therefore have resulted in a total power consumption and RFQ rise/fall times almost 33% larger than the current, window frame, design of the RFQ.

IV.   MEASUREMENTS

The RFQ driver has been tested in several different modes. Fig. 5 shows the measured pulse voltage, on the two sets of RFQ poles, for operation at 600 V peak-peak and 750 kHz. The rise time (123 ns) and fall time (118 ns) are obtained with 75 Ω resistors in the PUP stack and PDN stack (Fig. 2): the rise and fall times are within specification (125 ns). The effective capacitance of a pole pair, modulator and cabling, has been derived from the measured rise and fall times to be 750 pF. A total effective capacitance of 1.8 nF, for the complete system, has been determined based on measurements of charge drawn from the DC supply during operation: this capacitance includes the window frames of the RFQ, the RFSWD and cabling.

Measurements have also been carried out with a single modulator and a dummy load capacitor, of approximately 1 nF, replacing the RFQ. With the capacitor load a modulator, with 4 FETs per stack, generated 600 V peak-peak at 2.2 MHz, and 500 V peak-peak at 3.0 MHz [10].

V. SUMMARY & ONGOING WORK

The RFSWD has been tested at TRIUMF at 600 V peak-peak at 2.2 MHz, and 500 V peak-peak at 3.0 MHz. The rise and fall times are within specification but could be further reduced, without significantly affecting the power dissipation in the FETs or current limiting resistors, by reducing the value of each current limiting resistor from 75 Ω to 60 Ω.

The RFQ is presently being operated at 600 kHz and 400 V peak-peak. Future developments include upgrading the RFSWD to generate pulses of up to 1 kV at 3 MHz, continuous, for driving the effective capacitance of 1.8 nF: 5.5 A average will be drawn from a 1 kV supply. The dissipation will be 1.1 kW per 75 Ω current limiting resistance, and 70 W per FET, with 4 FETs per stack. The 1 μs wide primary current pulse should be derived from a 270 V power supply, a series 40 Ω resistance and a FET: the required frequency of the 1 μs wide pulse, for a RFSWD frequency in the range 300 kHz to 3 MHz, is 75 kHz to 420 kHz.
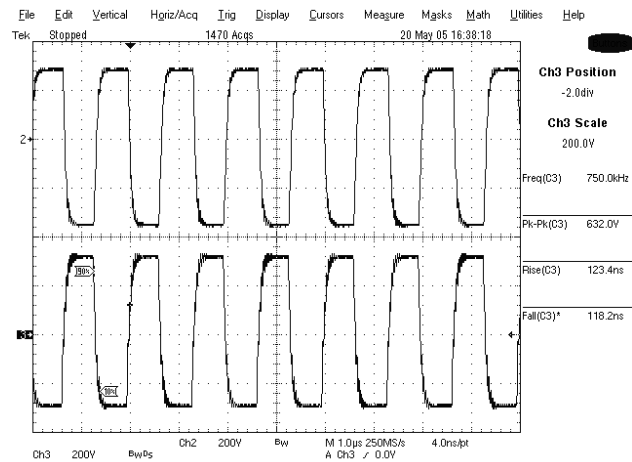

Figure 5. RFQ voltage, during operation at 600 V peak-peak and 750 kHz (200 V/division, 1 μs/division).

VI.   ACKNOWLEDGEMENT

VII.   REFERENCES

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