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**POLYMERIC AND MOLECULAR MATERIALS FOR ADVANCED ORGANIC ELECTRONICS**

**TOBIN MARKS  
NORTHWESTERN UNIVERSITY**

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Final Report**

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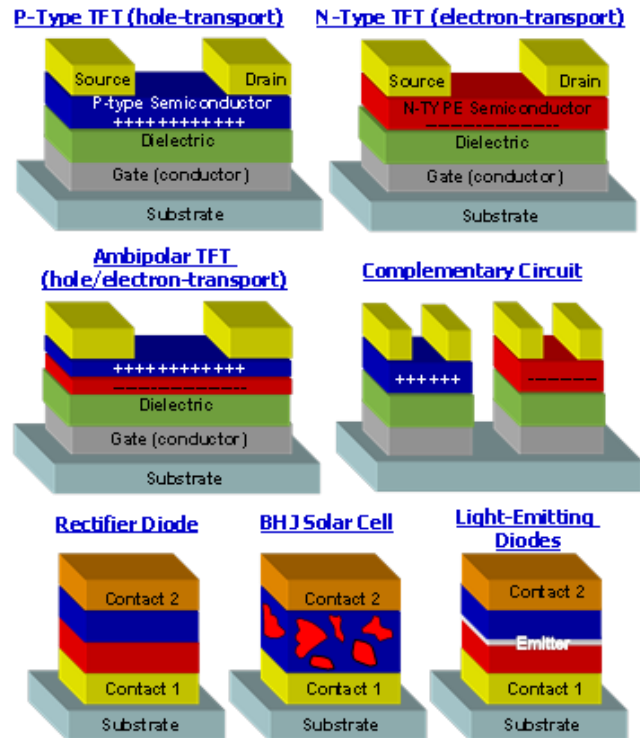
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## Introduction. CMOS, p/n-Junction Devices, and Flexible Electronics

Flexible/printed electronics is a revolutionary new concept for fabricating optoelectronic devices using high-throughput, inexpensive solution process/printing methodologies on flexible plastic foils, contrasting the large chip plants used today for silicon.<sup>i,ii</sup> With a fundamental materials understanding base,<sup>iii</sup> these technologies could enable inexpensive, lightweight, flexible, optically transparent, and unbreakable components for displays, cell phones, medical diagnostics, rf-id tags, and solar modules which can then be integrated with textiles, printed batteries, solar cells, and aircraft/satellite structures.<sup>iv</sup> The enabling materials component of all these technologies (among other essential materials) is the semiconductor where charge transport, light absorption, and/or light generation occur. To broaden device functionalities and applications, two types of semiconductors are required: p-type (hole-transporting) and n-type (electron-transporting). The use/combination of these two types of semiconductors enables the fabrication of elementary electronic building blocks for driving displays, harvesting light, generating light, carrying out logic operations, and sensor functions (Fig. 1).

Conventional Si technologies are based on vapor-deposited materials (semiconductor, dielectric, contacts, interlayers, passivation layer) and typically involve high-temperatures and subtractive photolithographic patterning. *Note that such processes are incompatible with new product concepts requiring mechanical flexibility, large areas, compatibility with plastic substrates and fabrics, new form-factors, and production which is low-cost and easily reconfigurable.* These new-generation products will require new types of semiconductors and other materials, less capital-intensive thin film deposition by solution methodologies and at low temperatures, with performance comparable to amorphous or low-quality polycrystalline silicon. Furthermore, such performance must ultimately be achieved in a printed platform with plastic substrates, printed electrodes, and solution-processed semiconductor and dielectric films, all handled under ambient conditions--a challenging task. From a scientific viewpoint, it is essential to understand how these unconventional semiconductors and related materials behave in combination versus conventional materials, how performance is affected by novel growth techniques, and how the resulting devices operate.

Current state-of-the-art solution-processable p- and n-type organic and hybrid semiconductors, and the corresponding integrated p/n-TFTs (typically referred as organic CMOS) and pn junctions, are limited in performance, processing window, and scope. While single-component



**Figure 1.** Structures of optoelectronic devices used to fabricate electronic and photonic products with the indicated p-type (blue) and n-type (red) materials.

TFT devices with good charge transport (carrier mobility  $> 10 \text{ cm}^2/\text{Vs}$  for holes,  $> 5 \text{ cm}^2/\text{Vs}$  for electrons) have been demonstrated, optimum semiconductor performance is typically not achieved for film/devices deposited by printing (carrier mobility  $< 0.5 \text{ cm}^2/\text{Vs}$ ) without the aid of specialized approaches. Furthermore, no efficient integration of fully printed p- and n-type semiconductors has been achieved surpassing the performance of amorphous Si. Therefore, understanding how to enable *both* high performance p- and n-type semiconductors and developing efficient methodologies to integrate them into single polarity TFT devices, integrated CMOS, and in pn junction devices are keys to advancing the science of flexible/printed optoelectronic circuits and devices.

The goal of the proposed work presented here is to build on previous AFOSR-funded Marks/Facchetti achievements<sup>v</sup> and to investigate new solution-processable, eventually printable, p- and n-type semiconducting materials and to integrate them into flexible unconventional pn junction devices. Furthermore, we will develop the necessary corollary device materials, particularly the critical gate dielectric and interfacial layers, for optimal TFT performance and stability. Finally, we will characterize charge transport characteristics to elucidate differences from more conventional electronic materials.

### **Results from Previous AFOSR-Sponsored Research Under FA9550-11-1-0142**

To achieve high-performance p/n-materials and devices and to address the aforementioned challenges hindering the progress of printed electronics, it is first necessary to develop new materials (semiconductors, dielectrics, and conductors), understand/optimize critical processes, study materials interfaces affecting charge injection (contact-semiconductor) and transport (dielectric-semiconductor) as well as understand/model charge transport in these unconventional devices. Before detailing the proposed research and deliverables, we summarize results from the previous Northwestern (NU) AFOSR-supported program. Significant advances were possible through the highly productive and close collaboration between the NU PIs, other NU faculty, and collaborations involving academic groups (e.g., Stanford U., UIUC, U. of Minnesota, U. Groningen, Purdue U., UCSB, Cambridge U.), national laboratories (Argonne Nat. Lab., AFML, NIST, NASA Ames), and our industrial transition partner (Polyera Corp.). Such interactions have been crucial to advancing this program and will continue in future research.

#### **1. Organic Semiconductor Synthesis, Characterization, and Function**

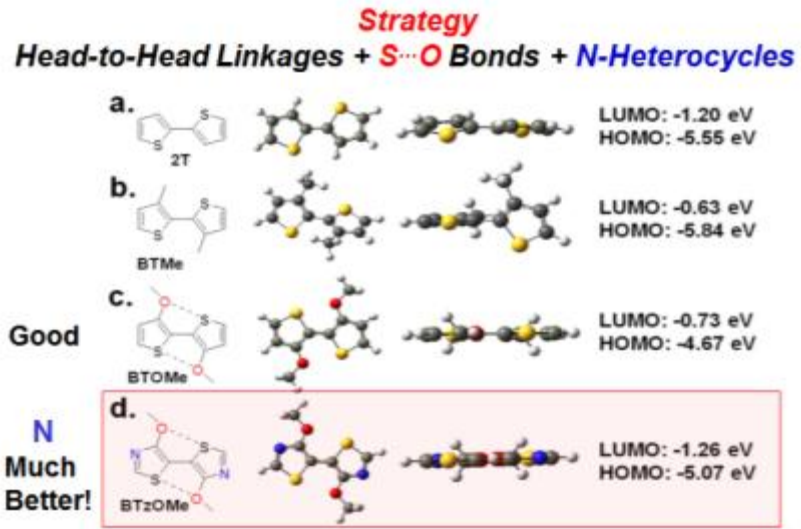
Here we summarize selected achievements in realizing new molecular and polymeric organic semiconductors for TFTs, with emphasis on key figures-of-merit achieved in conventional TFT architectures. This work was motivated by the fact that organic semiconductors exhibiting high mobility and current modulation in air are crucial to achieving high-speed low power organic CMOS (complementary) circuits, where both p- and n-type transistors must be fabricated and integrated. Here we targeted the greatest challenge, n-type semiconductors, where the principal synthetic strategy was to modify established, stable, high-performance p-type cores to create n-type cores, and to design completely new electron-poor  $\pi$ -conjugated building blocks. This results in lower HOMO and LUMO energies, with the latter being the frontier MO into which the electron charge carriers are injected during transport. The outcome of these efforts was greater electron stabilization, which induces a majority carrier “flip” from p  $\rightarrow$  n (if the unsubstituted core is intrinsically hole-transporting) and enhance environmental stability (if the material is electron-transporting). All of this much be achieved while enforcing planarity of the  $\pi$ -system and solubility via appropriate substituents.

In the area of new polymer semiconductors, we advanced considerably in the development of

new  $\pi$ -conjugated moieties as building blocks for both molecular and polymeric semiconductors. Thus, we achieved the design and synthesis of the new head-to-head (H-H) dialkoxy bithiazole (BTzOR) unit and the corresponding polymers.<sup>vi</sup> As is our general procedure, these studies combine synthesis with extensive characterization by x-ray reflectivity, grazing incidence x-ray scattering, cyclic voltammetry, GPC, AFM, UV photoelectron spectroscopy, DFT molecular and electronic structure analysis, TGA/DSC, electrical characterization by TFT and space-charge limited mobility measurements, and when the optical absorption is appropriate, by photovoltaic cell evaluation.

**Fig. 2** shows how the synergy of installing both attractive, planarizing (thiazolyl) $S\cdots O$ (alkoxy) supramolecular interactions (worth  $\sim 8$  kcal/mol) and electronegative N atoms in the  $\pi$ -rings maintains planarity while significantly dropping the LUMO energies. The result is several new polymer families based on this and related core structures. This includes new polymers exhibiting complementary transport characteristics, yielding TFTs with mobility up to  $0.5$   $\text{cm}^2/\text{Vs}$ , all-polymer-based CMOS circuits, and all-polymer solar cells. We designed a completely new building block, 4,4'-dialkoxy-5,5'-bithiazole, BTzOR (**Fig. 2**). In comparison to previously reported N-free 3,3'-dialkoxy-2,2'-bithiophene (BTOR), BTzOR is promising in view of the thiazole geometric and electronic properties by:

(a) replacing (thiophene) $C-H$  with (thiazole) $N$  which reduces steric repulsion in  $-BTzOR-Ar$  dyads by eliminating repulsive  $C-H\cdots H-C$  interactions with neighboring arene units, thereby enhancing  $\pi-\pi$  overlap, film crystallinity and carrier mobility (**Fig. 3**); (b) the thiazole electron deficiency compensates alkoxy substituent electron-donating characteristics, thereby lowering the BTzOR polymer HOMO versus that of the BTOR analogues. Thus, the new BTzOR polymers show substantial hole mobilities ( $0.06-0.50$   $\text{cm}^2/(\text{V s})$ ) and very stable operation because of the depressed HOMOs. Specifically, the electron-deficient thiazoles offset the alkoxy substituent electron-donating characteristics, rendering BTzOR-based polymers extremely ambient-stable. The result is a new, highly ordered

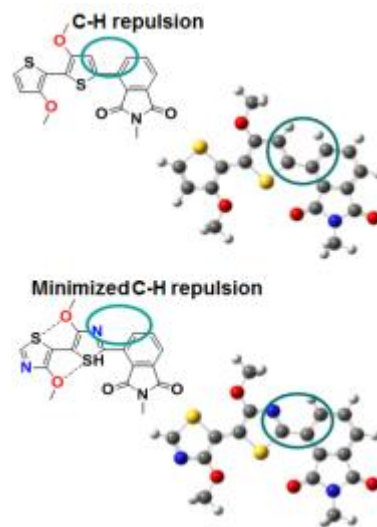


**Figure 2.** Strategy to enforce polymer  $\pi$ -planarity while lowering LUMO energies and

electrical characterization by TFT and space-charge limited mobility measurements, and when the optical absorption is appropriate, by photovoltaic cell evaluation.

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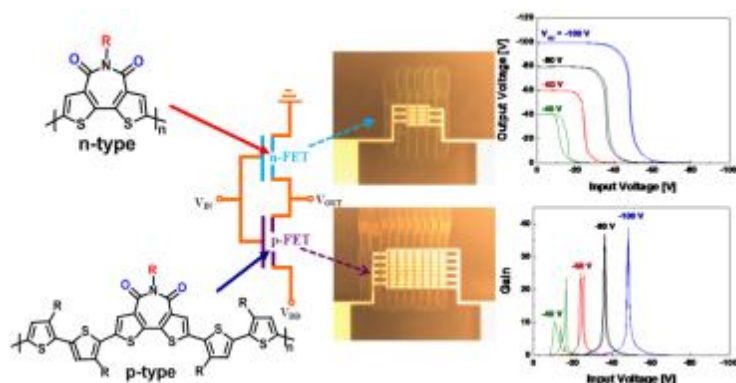
**Figure 3.** DFT computed effects of N for C-H substitution on intramolecular

polymer family with carrier mobilities  $> 0.5 \text{ cm}^2/\text{Vs}$ , TFT ambient stability  $> 200$  days in air, good TFT bias stress stability, and exceptional processing versatility.

In parallel work, we developed families of thieno[3,4-*c*]pyrrole-4,6-dione (TPD) and bithiophene-imide (BTI)-based polymers with highly informative properties.<sup>vii</sup> This includes polymers where electron-poor BTI is co-polymerized with electron-rich R<sub>2</sub>Si/R<sub>2</sub>Ge-bridged dithiophene co-units for organic photovoltaics having power conversion efficiencies (PCEs) of 6.83%. We also continued investigations of the

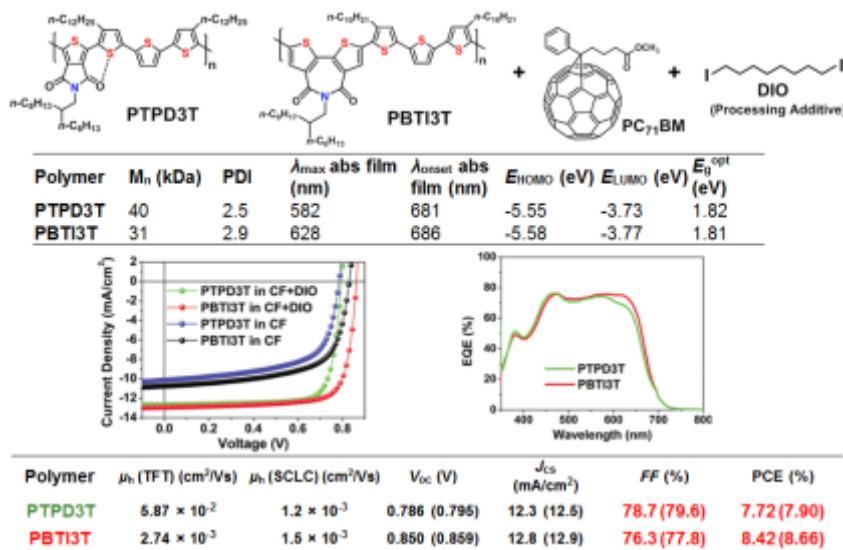
first molecular semiconductors incorporating the arylacetylenes with hole mobilities,  $> 0.2 \text{ cm}^2/\text{Vs}$ , n-type anthracenediimide semiconductors, and rylene structures which clarified the effects of core planarity on hole vs. electron transport. We also implemented or discovered new building blocks for molecular and polymeric hole- and electron transporters. Based on these results and our expertise in imide-based

semiconducting polymers, we were able to substantially lower the HOMOs while preserving excellent TFT hole transport, and investigated their use in bulk-heterojunction organic photovoltaics (OPVs) since  $V_{oc}$  should increase as the donor HOMO energy falls (see more below); the fabrication to complementary inverters is shown in **Fig. 4**.



**Figure 4** RTI polymers designed for n- or p-type transport used to inkjet

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**Figure 5**. Properties of in-chain donor-acceptor polymers with record photovoltaic fill-

With BTI and the related TPD building block, we recently synthesized a new series of in-chain donor-acceptor co-polymers based on BTI and TPD units co-polymerized with dialkyl-terthiophenes (**Fig 5**). The results, published in *Nature Photonics*,<sup>viii</sup> reported highly ordered active layers exhibiting very large  $V_{oc}$ s (0.8-0.9V), unprecedented fill factors (FFs) reminiscent of inorganic solar cells ( $\sim 80\%$ ), in accord with excellent long-range order and charge collection efficiency, and with state-of-the-art power conversion efficiencies (**Fig. 5**). In the coming project period we will focus on better understanding design factors that long range polymer order, environmental stability, and TFT bias stress stability.

## 2. TFT Gate Dielectrics

Under this program we greatly expanded the available classes of self-assembled high- $k$  nanodielectrics (SANDs), with each class customized to address a different challenge (Fig. 6).<sup>ix</sup> These

materials are characterized by AFM, conducting AFM, XPS, x-ray reflectivity (XRR), standing wave x-ray reflectivity (SWXRR), x-ray fluorescence (XRF), variable frequency capacitance measurements, TGA, complex impedance spectroscopy, TGA, MIM structures, TFT characterization, radiation hardness measurements, and quantum chemical computation of dielectric constants. Remarkably, for semiconductors as

diverse as organics, sorted carbon nanotubes, single-layer graphene, metal oxide films (both polycrystalline and amorphous) and nanowires, silicon nanomembranes, GaAs, and 2-D chalcogenide films, the effects of the SAND gate dielectrics are striking: greatly reduced operating voltage, greatly enhanced mobility, and greatly suppress transfer curve hysteresis. The former property can be understood since in TFTs the current between source and

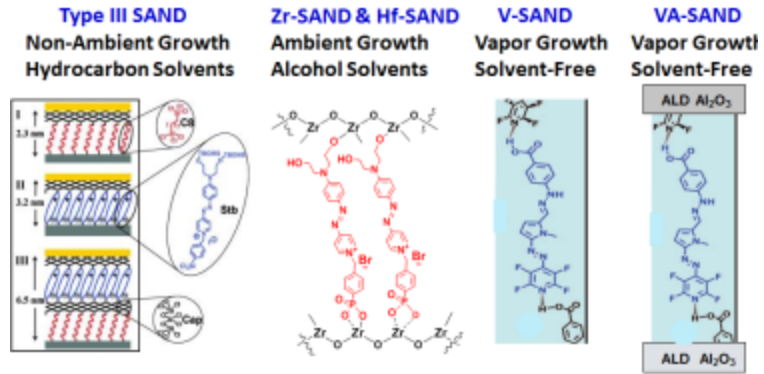


Figure 6. High- $k$  SAND gate dielectrics designed to answer various questions

$$I_{DS} = \frac{W}{2L} \mu C_i (V_G - V_T)^2 \quad (1)$$

drain contacts ( $I_{DS}$ ) in saturation is modulated by the gate bias ( $V_G$ ) according to eq.1 where  $W/L$  is the channel width/length,  $C_i$  is the areal dielectric capacitance,  $\mu$  is the carrier mobility,  $V_G$  is the gate voltage, and  $V_T$  is the threshold voltage. For low power applications such as RF-ID tags, flat panel displays, and portable electronics, it is mandatory to achieve high TFT drain currents ( $I_{DS}$ ) at the lowest operating voltages possible (ideally  $< 4V$ ). According to eq. 1, an attractive approach to achieve this is to increase the capacitance of the gate dielectric. Note from eq. 2 that increasing the dielectric constant ( $k$ ) or decreasing the thickness

$$C_i = \epsilon_0 \frac{k}{d} \quad (2)$$

(d) of the gate dielectric layer increases the capacitance. An increase in the  $k/d$

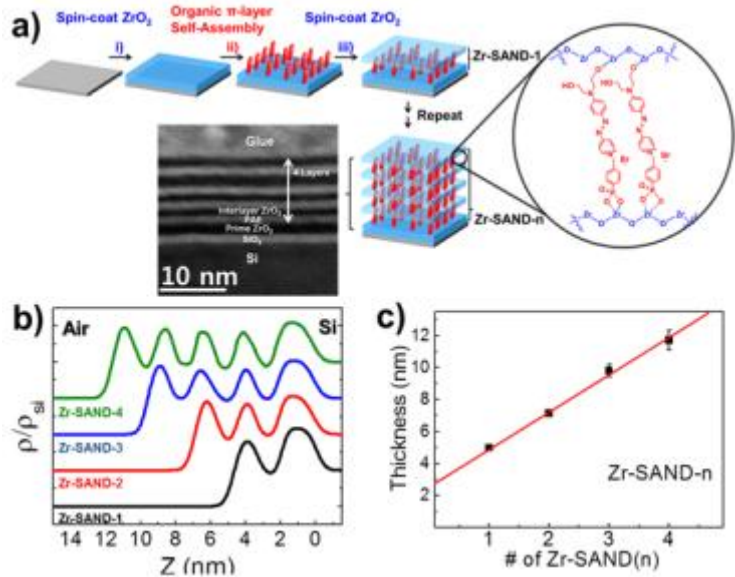
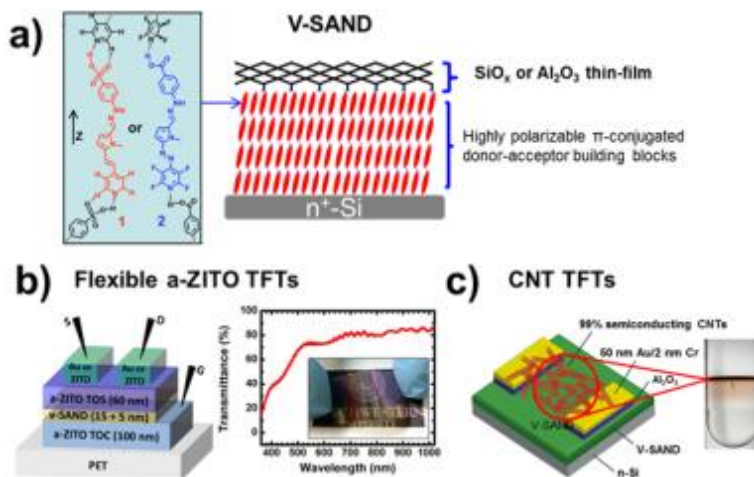


Figure 7. (a) Fabrication of Zr-phosphonate self-assembled nanodielectric (Zr-SAND). i) Spin-coat  $ZrO_2$  primer layer ii) Self-assembly of phosphonic acid-based organic  $\pi$ -electron layer, iii) Spin-coat  $ZrO_2$  for interlayer (Inset: Cross-sectional TEM image of the Zr-SAND film. Labels indicate layer identities). (b) Specular XRR-derived electron density profiles (normalized to  $\rho_{Si}$ ) as a function of height  $z$  above the Si

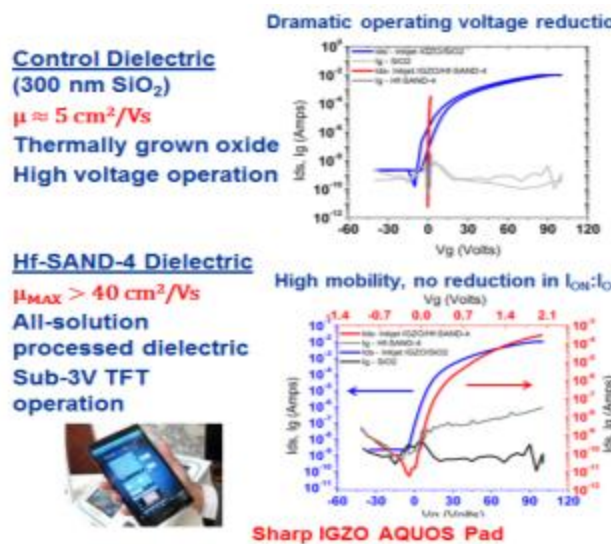
ratio is necessary for efficient device size reduction (scaling) which supports low-power TFT operation. As an example, **Fig. 7** shows the straight-forward ambient self-assembly and structural characterization of Z-SAND.<sup>x</sup> Zr-SAND is stable to 300°C in air, with the XRR revealing only a slight contraction in the layer spacing which by eq. 2 increases the capacitance. The Hf analogue, Hf-SAND, has the largest capacitance achieved to date for a SAND dielectric, 1  $\mu\text{F}/\text{cm}^2$ . How SAND lowers TFT operating voltage is understandable in terms of eqs. 1 and 2, but how mobility is increased and hysteresis decreased are a mystery and will be investigated in the coming project period.<sup>xi</sup> Nevertheless, the ability of SAND dielectrics to enhance the performance of TFTs fabricated with a great many (but not all) semiconductors is established (e.g., **Fig. 8**), and the scope will also be explored in the coming grant period, testing SAND and specifically modified SAND derivatives against a variety of unusual but potentially informative semiconductors, to test key mechanistic hypotheses.



**Figure 8.** (a) Schematic of vapor-deposited SAND (V-SAND) and structures of the organic components. (b) Architecture, transmission optical spectrum, and image of a transparent a-ZITO TFT array fabricated on plastic and bent over a

### 3. Hybrid Materials Systems

Optimization of growth processes leading to high-quality interfaces between TFT component materials, and understanding those chemical, morphological, and nanostructural phenomena which best optimize hysteresis-free charge flow in TFTs is arguably as important as developing new materials. Thus, the current carrying channel in most TFTs is only a few nm thick and in close proximity to the semi-conductor-dielectric interface. And of course such hybrid phenomena are most intriguing when the interface between them involves very different kinds of materials. A striking example is the case of amorphous metal oxide semiconductors, which are prepared by a low-temperature “combustion synthesis” route invented at NU under AFOSR support and published in *Nature Materials*.<sup>xii</sup> Here fuels and oxidizers in a metal-organic sol-gel precursor produce atomically local heating and greatly reduce the thermal input required to densify the lattice of this highly cross-linked inorganic polymer. The In-Ga-Zn-O material (“IGZO”) is an excellent semiconductor which, due to its high mobility and optical transparency, is



**Figure 9.** Dramatic performance differences in transfer plots of IGZO/SiO<sub>2</sub> vs IGZO/Hf-SAND TFTs. Inset: Bred type device with



replacing amorphous Si TFTs in the driving TFT electronics of numerous displays (e.g., the iPad Mini). To date, IGZO TFTs are grown by capital-intensive sputtering, followed by subtractive wet-etch patterning, however a printing process would be highly desirable for fabricating IGZO TFTs. In recent work at Northwestern, IGZO TFTs were fabricated by inkjet with a variety of gate dielectrics including SiO<sub>2</sub>, HfO<sub>2</sub> grown by atomic layer deposition or combustion, and Hf-SAND, and the TFT response evaluated. As can be seen in **Fig. 9**, the operating voltage and mobility of IGZO TFTs on Hf-SAND is dramatically lower than that on SiO<sub>2</sub>. Although not shown, the same is true for IGZO on high-*k* HfO<sub>2</sub> dielectrics. Furthermore, and most intriguing, the mobility of the IGZO/Hf-SAND is far greater and the hysteresis is far less.<sup>xiii</sup> Since Hf-SAND is terminated by a HfO<sub>2</sub> nanolayer (**Fig. 7**), this is particularly curious. Those factors which underlie the striking differences of TFTs based on SAND will be a focus in future research.

### Publications Acknowledging Support by this AFOSR Program

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