WIDE-PULSE EVALUATION OF 0.5 CM^2 SILICON CARBIDE SGTO

Heather O'Brien, Aderinto Ogunniyi, Charles J. Scozzie
U.S. Army Research Laboratory, 2800 Powder Mill Road
Adelphi, MD 20783 USA
William Shaheen
Berkeley Research Associates, 6551 Mid Cities Ave
Beltsville, MD 20705 USA
Anant Agarwal
Cree, Inc., 3026 E. Cornwallis Rd
Research Triangle Park, NC 27709 USA
Victor Temple
Silicon Power Corp., 958 Main St., Suite A
Clifton Park, NY 12065 USA

Abstract

Silicon carbide Super-GTOs are being pursued by the Army as a replacement for current silicon-based, high-power pulse switches. In this study, 0.5 cm^2 silicon carbide SGTOs were evaluated in an RLC pulse circuit which provided a half-sine shaped pulse at a width of 1 ms. The parameters assessed were peak current capability, 1000-shot reliability, and current sharing between parallel switches. SGTOs were pulsed as high as 1600 A, but 1250 A was found to be the most reliable and repeatable current level for most devices. This current waveform corresponds to an action of 850 A^{2}s and a current density over the emitter area of 3.5 kA/cm^2. SGTOs were pulsed for over 1000 single shots without any significant change in forward voltage drop. A pair of parallel SGTOs was pulsed up to a total of 2600 A, and repeatedly at 2500 A, with current sharing within ± 1%. This paper details the evaluations of individual and paralleled devices which are being studied in preparation for future work with multi-chip modules.

I. INTRODUCTION

To support the development of compact, light-weight, power-dense switches for mobile platforms, the U.S. Army Research Laboratory (ARL) is researching the capabilities of silicon carbide Super-GTOs. As material development improves, silicon carbide SGTOs of larger area and higher hold-off voltage are being fabricated at reasonable wafer yield levels [1]. The SGTOs evaluated in this study are four times the area of the last generation of SiC SGTOs and have almost double the voltage blocking. In the current ARL evaluations, silicon carbide SGTOs show wide-pulse (1-ms width) current capabilities with a factor of 1.5 times higher current and 2.5 times higher action compared to similar 3.5 cm^2 silicon devices when normalized for footprint area [2]. The benefits of silicon carbide include high breakdown electric field, high thermal conductivity, and wide energy bandgap [3]. Compared to silicon power switches, silicon carbide SGTOs show lower voltage drop at high current densities, which leads to lower losses in high-power systems. Silicon carbide's high current density pulse capabilities and potential for 10-20 kV forward voltage blocking will allow for fewer parallel and series switches and an overall reduction in weight and volume for Army systems [4, 5].

The Super-GTO design, originated by Silicon Power Corp., is being pursued because of the high level of performance it demonstrated on larger-scale switches for narrow-pulse vehicle applications. The prefix "Super" denotes a thin chip with a multi-zone high voltage termination and specially designed gate and cathode contacts [6]. If the SGTOs continue to show power-dense, reliable performance for wide-pulse applications, they will become critical components for Army vehicle systems.

II. DESIGN AND PACKAGING

A. Description of the SGTO

The silicon carbide SGTO was designed and fabricated for ARL through cooperative agreements with Silicon Power Corp. and Cree, Inc. It has a footprint of 0.49 cm^2 and a central active area (or mesa) of 0.36 cm^2. It is built on an n$^+$ SiC substrate, which results in much higher conductivity as compared to p-type substrates in SiC (Fig. 1). A 15-zone JTE and a 60 um thick blocking epi-layer allow for forward voltage hold-off beyond 5 kV. The SGTOs have limited reverse blocking capability. All of the devices evaluated in this study are from one 75 mm 4H-SiC wafer with low basal plane dislocations (Fig. 2).

Report Documentation Page

Form Approved
OMB No. 0704-0188

1. REPORT DATE	2. REPORT TYPE	3. DATES COVERED
JUN 2009	**N/A**	**-**

4. TITLE AND SUBTITLE	5a. CONTRACT NUMBER
Wide-Pulse Evaluation Of 0.5 Cm2 Silicon Carbide Sgto	5b. GRANT NUMBER
	5c. PROGRAM ELEMENT NUMBER
6. AUTHOR(S)	5d. PROJECT NUMBER
	5e. TASK NUMBER
	5f. WORK UNIT NUMBER
7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES) **U.S. Army Research Laboratory, 2800 Powder Mill Road Adelphi, MD 20783 USA**	8. PERFORMING ORGANIZATION REPORT NUMBER
9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)	10. SPONSOR/MONITOR'S ACRONYM(S)
	11. SPONSOR/MONITOR'S REPORT NUMBER(S)

12. DISTRIBUTION/AVAILABILITY STATEMENT
Approved for public release, distribution unlimited

13. SUPPLEMENTARY NOTES
See also ADM002371. 2013 IEEE Pulsed Power Conference, Digest of Technical Papers 1976-2013, and Abstracts of the 2013 IEEE International Conference on Plasma Science. IEEE International Pulsed Power Conference (19th). Held in San Francisco, CA on 16-21 June 2013., The original document contains color images.

14. ABSTRACT
Silicon carbide Super-GTOs are being pursued by the Army as a replacement for current silicon-based, highpower pulse switches. In this study, 0.5 cm2 silicon carbide SGTOs were evaluated in an RLC pulse circuit which provided a half-sine shaped pulse at a width of 1 ms. The parameters assessed were peak current capability, 1000-shot reliability, and current sharing between parallel switches. SGTOs were pulsed as high as 1600 A, but 1250 A was found to be the most reliable and repeatable current level for most devices. This current waveform corresponds to an action of 850 A2s and a current density over the emitter area of 3.5 kA/cm2. SGTOs were pulsed for over 1000 single shots without any significant change in forward voltage drop. A pair of parallel SGTOs was pulsed up to a total of 2600 A, and repeatedly at 2500 A, with current sharing within ± 1%. This paper details the evaluations of individual and paralleled devices which are being studied in preparation for future work with multichip modules.

15. SUBJECT TERMS

16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT	18. NUMBER OF PAGES	19a. NAME OF RESPONSIBLE PERSON
a. REPORT	b. ABSTRACT	c. THIS PAGE			
unclassified	**unclassified**	**unclassified**	**SAR**	**4**	

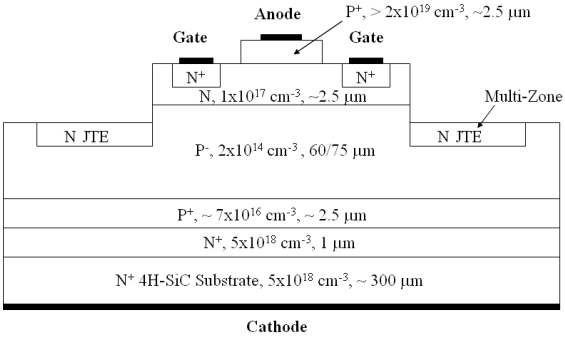

Figure 1. Cross section of the 0.5 cm^2 SGTO fabricated by Cree.

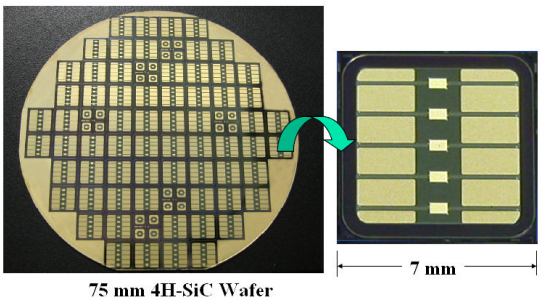

Figure 2. Images of SGTO wafer and enlarged single device. Gold anode and gate pads are shown on the surface of the chip.

B. Packaging at ARL

The SGTOs were individually packaged at ARL. The cathode of each die was attached to a commercially-available power package with eutectic AuSn die attach solder. Five-mil aluminum wire bonds were attached to the anode and gate pads on the surface of the device, totaling 48 wires for the anode and five wires for the gate (Fig. 3). The shallow well of the power package was filled with a clear silicone-based potting compound in order to prevent high-voltage flashover and provide some mechanical protection for the wire bonds.

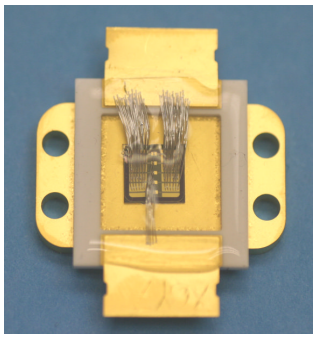

Figure 3. SGTO packaged at ARL using power package, AuSn die attach, 5-mil wire bonds, and silicone-based potting.

C. Static Characteristics

Seven of the packaged SGTOs were high-potted to roughly 0.1 mA/cm^2 current leakage. Six of them showed blocking voltages greater than 7.0 kV DC prior to pulse switching. The forward voltage drop (V_{ak}) at turn-on was 2.9 V, with an applied gate current of 100 mA between the gate and anode (Fig. 4). The reverse gate-anode blocking capability varied across the wafer, but was most commonly found to be greater than 20 V. The gate current for the 1-ms, high-current switching was a -1.2 A pulse of 30 us duration.

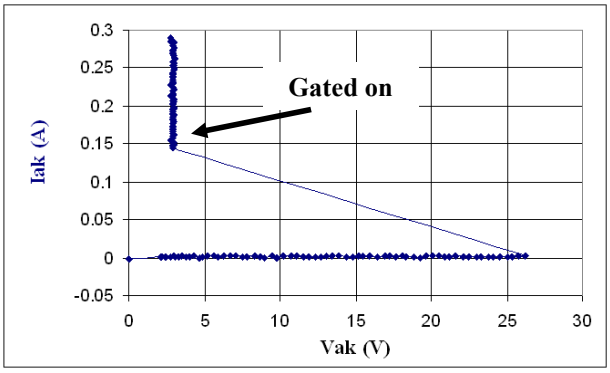

Figure 4. Turn-on of SGTOs as recorded on curve tracer.

III. EVALUATION METHODS

A. Evaluation

The focus of the study was to determine the switching capabilities of the 0.5 cm^2 SGTO under sinusoidal, 1-ms wide, single-shot pulse conditions. The key parameters considered were repeatable peak current, current sharing between parallel SGTOs, Tq recovery, and dV/dt immunity, with the latter two parameters being reported on separately [7]. System switching requirements were determined and integrated into the test circuit design in order to evaluate the SGTOs under application-specific conditions. Similar ongoing evaluations of silicon SGTOs were being conducted at ARL, so the same test circuit was used for these silicon carbide SGTOs [2]. The circuit consists of a high-energy capacitor bank, an inductor constructed at ARL, and a high-wattage, low-ohm resistive load. Diodes are used to clamp negatively ringing current and to create a symmetrically blocking switching unit (Fig. 5).

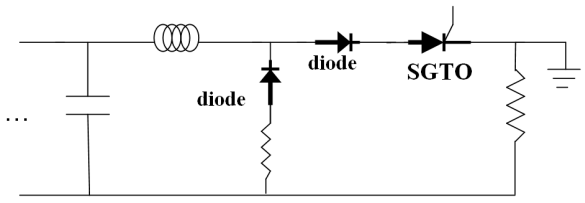

Figure 5. Schematic of the test circuit for the SGTO.

To find the peak current rating of the SGTO under wide-pulse conditions, current was slowly stepped up at intervals of 100 A to a point where the forward voltage drop of the device began to change. When anode-cathode current was pushed too high, the voltage drop would spike soon after the peak of the current waveform. This resulted in extra heating within the device and would lead to catastrophic failure if repeated several times. Once a safe, repeatable current was determined for each device, one thousand low duty cycle shots were programmed utilizing nine-second gaps between switching events. Upon completing this test, the SGTOs were high-potted to look for any change in blocking capability. This procedure was previously used to monitor degradation in smaller silicon carbide switches [8].

Additionally, one pair of SGTOs was connected in parallel in the same circuit in order to evaluate the potential for current sharing between multiple devices. The two SGTOs were in separate packages with the inductance and resistance of their circuit connections roughly matched (Fig. 6). The same single gate driver was used to circulate current through two parallel gate resistors. The high-level pulse currents through the SGTOs were monitored with Rogowski coils at the devices' anode connections. Sharing was monitored up through 1000 single pulses.

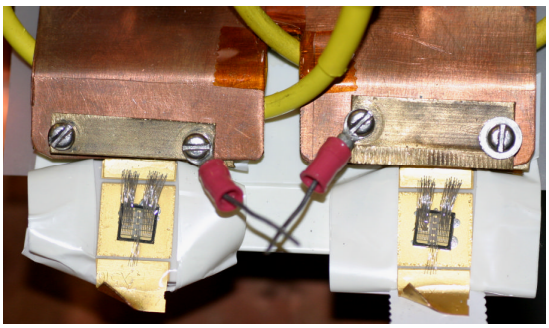

Figure 6. Pair of SGTO packages connected in parallel. Protruding wires at the center were used to connect the anode return side of the gate driver. Rogowski coils used to monitor current sharing can be seen near the top of the photo.

B. Results

SGTOs were pulsed as high as 1.6 kA, or a current density of 4.4 kA/cm^2 over the active area. For the range of devices evaluated, 1.25 kA was a common repeatable current at 3.5 kA/cm^2 (Fig. 7). Forward voltage drop was monitored over the course of 1000 shots and was not seen to increase significantly (Fig. 8). Typical peak power dissipation during a single pulse was 12 kW. When the SGTOs were repeatedly pulsed beyond 1.3 kA, the forward voltage drop would increase with each subsequent shot. Figure 9 shows an example of this. For three single-shot, sequential pulses of 1.3 kA, the V_{ak} increased by 1.2 V (>1 kW additional) per pulse. Continuing switching at 1.3 kA or higher would have brought upon thermal runaway and failed this device short. Possible reasons for this change in the voltage waveform include current crowding at the high current level, or lingering heating effects from the previous pulse, contributing to a higher overall internal temperature. When the current level was lowered below 1.3 kA, forward drop returned to normal levels. For some SGTOs, this change to the V_{ak} did not occur until higher pulse current levels, up to the aforementioned 1.6 kA. For this reason, 1.25 kA was chosen as the safe, across-the-board operational current level for the 1-ms pulse. This current value and density correspond to the peak current reliably pulsed with 0.16 cm^2 SiC SGTOs previously [2].

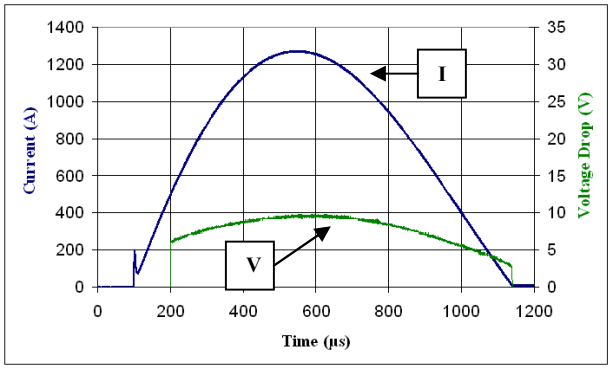

Figure 7. Peak reliable current (1250 A) and recorded anode-cathode voltage drop (9 V) for the SGTO. Voltage measurement was not introduced until the time t=200 µs.

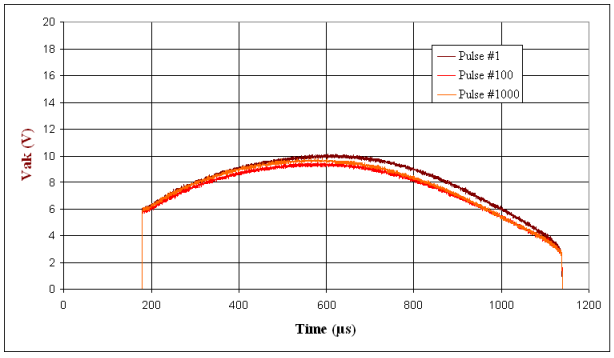

Figure 8. Little variation in anode-cathode voltage drop over the course of 1000 pulses.

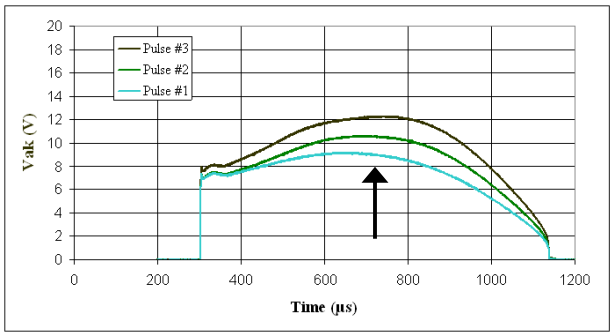

Figure 9. V_{ak} rising when the current level was pushed too high (1300 A) for one of the SGTOs. Current was reduced for subsequent pulses, and the V_{ak} returned to its original relatively flat shape.

The paralleled SGTOs shared gate current and cathode current well. The original gate current of 1.2 A was split between the two devices' gates. At the peak of the cathode current pulse, each device carried ± 10 A, or within 1% of ideal, even current sharing (Fig. 10). The total current output was 2.5 kA. This pair of SGTOs was switched 1000 times without any change in current sharing.

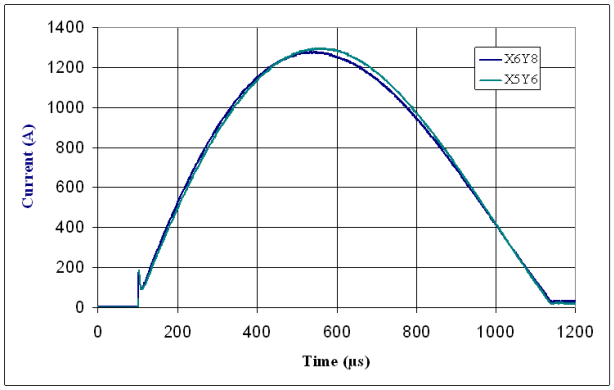

Figure 10. Overlying currents carried by two parallel SGTOs (identified as X6Y8 and X5Y6). Total combined current was 2.5 kA. Sharing was within ± 1%, with X6Y8 peaking at 1.27 kA and X5Y6 peaking at 1.29 kA.

C. Further Testing

Silicon Power Corp. is directing assembly of four-chip SGTO modules for further parallel device switching. Groups of four SGTOs will share a common cathode plate and utilize Silicon Power's ThinPak lid rather than wire bonds. These modules will be used to verify packaging performance and parallel integration of several SGTOs. The modules are expected to block greater than 5 kV and switch about 5 kA of current. Information garnered from this portion of the study will aid the follow-on development of larger, higher current silicon carbide SGTO modules using the current silicon SGTO hardware.

IV. SUMMARY

Silicon carbide SGTOs fabricated at 0.5 cm^2 die area were switched up to 1.25 kA at a 1-ms wide pulse width. SGTOs were pulsed over 1000 times without increase in forward voltage drop or signs of degradation. Pairs of devices were also switches in parallel and demonstrated current sharing within 1% of ideal sharing. Current division remained consistent through 1000 switching events. These results suggest that six of these 0.5 cm^2 SGTO could replace one current-generation 3.5 cm^2 silicon SGTO and carry 40% more current and handle more than twice the action in a smaller footprint. The results support further development of larger area, higher voltage silicon carbide SGTOs to meet the Army's pulsed power switching needs.

V. REFERENCES

[1] M. J. O'Loughlin, *et al*, "Silicon Carbide Hot-Wall Epitaxy for Large-Area, High-Voltage Devices," Materials Research Society Symp. Proc., vol. 1069, Spring 2008.

[2] H. O'Brien, W. Shaheen, V. Chiscop, C. J. Scozzie and M. G. Koebke, "Evaluation of Si and SiC SGTOs for High-Action Army Applications," IEEE Trans. Magnetics, vol. 45, no. 1, pp. 402-406, Jan. 2009.

[3] "SiC Physical & Electronic Properties," Cree, Inc., Durham, NC, [Online], 2009 [cited June 2009], Available: http://www.cree.com Directory: products File: sic_sub_prop.asp

[4] A. Agarwal, Q. Zhang, A. Burk, R. Callanan, and S. Mazumder, "Prospects of Bipolar Power Devices in Silicon Carbide," Proc. of the 34th Annual IEEE IECON, pp. 2879-2884, Nov. 2008.

[5] T. Burke, K. Xie, H. Singh, T. Podlesak, J. Flemish, J. Carter, S. Schneider, and J. Zhao, "Silicon carbide thyristors for electric guns," IEEE Trans. Magn., vol. 33, no. 1, pp.432-437, Jan. 1997.

[6] V. Temple, " 'Super' GTO's push the limits of thyristor physics," Proc. of the 35th IEEE PESC, pp. 604-610, June 2004.

[7] A. Ogunniyi, H. O'Brien, W. Shaheen, C.J. Scozzie, and V. Temple, "Comparison of Recovery Time and dV/dt Immunity for Si and SiC SGTOs," Proc. of the 17th IEEE PPC, 30 June – 2 July 2009, Washington, D.C.

[8] H. O'Brien, W. Shaheen, S. B. Bayne, "Evaluation of 4 mm x 4 mm Silicon Carbide Thyristors," IEEE Trans. Dielectrics and Electrical Insulation, vol. 14, no. 4, pp. 986-993, Aug. 2007.