REPORT DOCUMENTATION PAGE

Form Approved

OMB No. 0704-0188

1. REPORT DATE *(DD-MM-YYYY)*	2. REPORT TYPE	3. DATES COVERED *(From - To)*
24-Jun-2014	Final	9 June 2011 to 8 Dec 2013

4. TITLE AND SUBTITLE

Electrically Tuneable EBG Integrated Circuits

5a. CONTRACT NUMBER
FA2386-11-1-4046

5b. GRANT NUMBER
Grant AOARD-114046

5c. PROGRAM ELEMENT NUMBER
61102F

6. AUTHOR(S)

Dr. Michael Heimlich

5d. PROJECT NUMBER

5e. TASK NUMBER

5f. WORK UNIT NUMBER

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
Macquarie University
Level 2, Building E6A
Sydney 2109
Australia

8. PERFORMING ORGANIZATION REPORT NUMBER
N/A

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)

AOARD
UNIT 45002
APO AP 96338-5002

10. SPONSOR/MONITOR'S ACRONYM(S)
AFRL/AFOSR/IOA(AOARD)

11. SPONSOR/MONITOR'S REPORT NUMBER(S)
AOARD-114046

12. DISTRIBUTION/AVAILABILITY STATEMENT

Approved for public release.

13. SUPPLEMENTARY NOTES

14. ABSTRACT

The goal of this research effort is to implement dynamically-tuneable Electromagnetic BandGap (EBG) circuits for filtering in an integrated circuit (IC) fabrication processes leveraging a technique previously developed for Printed Circuit Board (PCB).

15. SUBJECT TERMS

Metamaterials, Radio Frequency Transmission Lines

16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT	18. NUMBER OF PAGES	19a. NAME OF RESPONSIBLE PERSON
a. REPORT	b. ABSTRACT	c. THIS PAGE			Seng Hong, Ph.D.
U	U	U	SAR	17	19b. TELEPHONE NUMBER *(Include area code)* +81-3-5410-4409

Dynamically-Tuneable EBG Integrated Circuits: Final Report

Grant No. FA2386-11-1-4046 AOARD 114046

Principal Investigators:
Prof. Michael Heimlich, Prof. Karu Esselle, A/Prof. Matekovits.

Program Manager: Lt. Col David R. Hopper, PhD

December 2013

Summary

The goal of this work is to implement dynamically-tuneable Electromagnetic BandGap (EBG) circuits for filtering in an integrated circuit (IC) fabrication processes leveraging a technique previously developed for Printed Circuit Board (PCB). Early design work demonstrated a minimal dielectric thickness separating the two key metal layers as critical to using the previous circuit design technique, however commercially available IC processes are almost an order of magnitude below this value. Requests for special processing by commercial IC fabricators were unsatisfied. In light of this, a new circuit design technique was developed which showed reduced performance, but nonetheless demonstrated tuneable EBG effects. Measured performance of fabricated circuits have not exhibited the simulated characteristics. Analysis to date continues along two lines of investigation but no firm conclusions are available at this time. Work will be continuing nonetheless.

The report begins with background and overview of EBG and earlier work and then leads into the design work, fabrication, and measured results. Sections follow which discuss project management, publications, intellectual property development, and following on-funding, and work continuing on beyond the project termination date.

Background – EBG concepts and Previous Work

Electromagnetic Bandgap (EBG) structures exhibit large continuous operational regions as a function of frequency over which they will not allow a signal to propagate. A subclass of bandstop filters, EBG structures "stop" a signal from passing through by having signals not propagate (vs. some other means of signal rejection, like reflection) in abeyance of Maxwell's Equations. Typically, EBG performance is achieved by modulating the geometric properties of an electromagnetic-guided or radiating structure so as to create a periodicity which induces the EBG and as such is not tuneable [1] if implemented as integrated circuits (IC) or printed circuit boards (PCB).

Previous work by this research team under Grant No. FA2386-10-1-4040 AOARD 10404 implemented a dynamically-tuneable EBG structure using printed circuit board technology at a few GHz. The periodic structure is implemented as a single, main transmission line, on top of regular series of short "patches". The transmission line and patches are separated by a dielectric whose properties are chosen to give the desired effect EBG effect (Figure 1). In the absence of the patches, the structure would be an ideal microstrip configuration.

Tuning is accomplished by using a pair of RF/microwave switches at opposite ends of the patches (not sown in Figure 1) to isolate or connect the patch to ground, typically on the backside of the structure. With the switches open, or in the "0" state, the transmission line has a current return path dominated by the true, backside ground. With the switches closed, or in the "1" state, the current return path is dominated by a coupling from the transmission line to the patch and through the switches to ground. By choosing different combinations of switches, different periodic structures can be obtained which give rise to a variety of

electromagnetic, and EBG, characteristics. to move the effective ground plane of a guided structure. A detailed analysis of this can be found in [6].

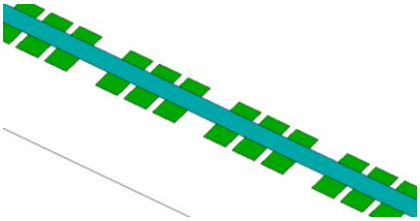

Figure 1 – Periodic two-layer EBG structure with main transmission line on top layer (blue) and patches in 4 groups of 3 on second layer (green).

The benefit of these structures are large bandwidth switching whose switching times would be on the order of switching time of the underlying device. Whereas MEMs structures would be on the order microseconds, and packaged FET switches on the order of tens of hundreds of nanoseconds, an IC process which integrated these structures could in theory switch at sub-nanosecond rates.

The aim of the previous project was to create a PCB demonstrator of the switchable EBG structure based on the prior theoretical study on IC [2,3].

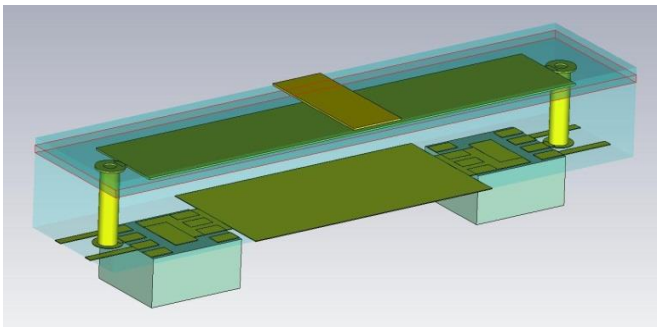

Figure 2 – Conceptual design used for PCB demonstrator: thru-vias (yellow) connect the patch to the backside switches (gray blocks) to open/close current path to ground plane (large green rectangle on lower level). Top level (green) line is the main transmission line

Because of PCB fabrication requirements, the initial structure was modified as shown in Figures 2 and 3. Instead of switches on the front, the switches were placed on the back with the normally uniform ground plane corrupted and broken up so as to support switching control lines to the edges and active signal lines from the thru-vias to the switch pads. 48 switches, or 24 patches were constructed to give a high variety of switched states, which were mainly grouped as 8 unit cells of 3 patches.

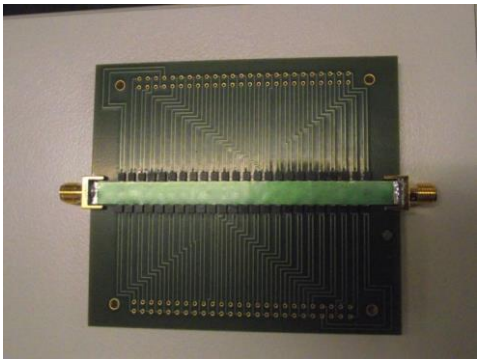

Figure 3 – Fabricated EBG Demonstrator with mounted switches

Measured data for the PCB demonstrator were encouraging (Figure 4). Extremely steep transitions from transmission to non-transmission were observed in the switched states with somewhat higher than desired insertion loss in the 0000… state. Changes in switching states could accomplish as much as a 2x change in the bandwidth of the stopband.

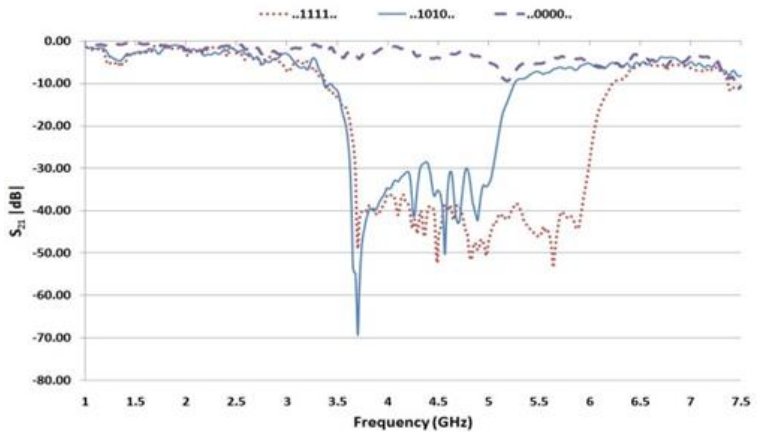

Figure 4 – EBG Demonstrator PCB with configurations "...1111…", "…1010..." and "…0000.." [3]

The aim of this current project is to return to the original concept of front-side, integrated switching, with a uniform backside ground plane, and implementation in IC technology. The benefit of such and EBG structure with IC technology is to incorporate it with higher levels of integration as well as to provide higher reliability.

Detailed Project Objective and Initial Designs

According to [2], the structure needs to have several key features (as shown in Figure 1):

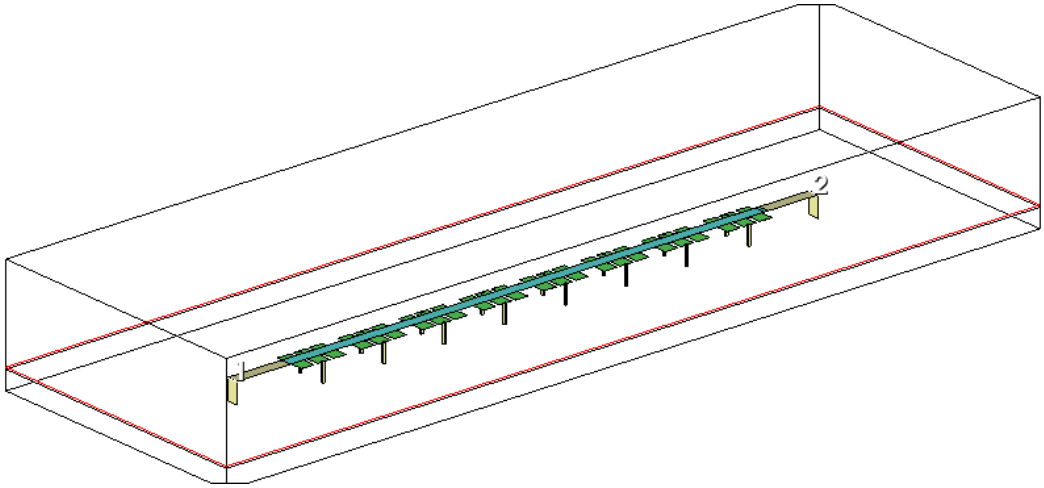

Figure 5 – Theoretical EBG structure for IC

1. A thick, low-loss dielectric substrate with a ground plane on the back. Bottom-most layer shown in box edges in Figure 1.
2. A top-layer metal conductor which, when placed on the top of item 1, implements a high-quality microstrip transmission line. Blue line in Figure 1.
3. A very thin, low-loss dielectric layer inserted between items 1 and 2. Middle (reddish) layer shown in box edges in Figure 1.
4. Periodic metal patches transverse to item 2 and on the bottom side of item 3(i.e. between the items 1 and 3). Green structures in Figure 1.
5. Conducting vias located beyond the ends of metal patches in item 4 which connect to the ground plane of item 1 through a selectable electronic switch capable of passing RF/microwave signals at some lower frequency switching rate; the switching speed is unimportant for this project. Gold vertical rectangles in Figure 1.
6. Switches connecting the vias, item 5, to the patches, item 4. Not shown in Figure 1.

Initial design considerations focused on the dielectrics and their thicknesses that physically separate items 1, 2, and 3. Nominally, the "height", of a microstrip transmission line is defined by the distance between items 1 and 2. This height is referred to here as h_1. If item 3 is acting as a surrogate or weak ground for the main transmission line (item 1), then the separation (or height or thickness) between items 2 and 3 is also of importance. This height is referred to here as h_2. Thus, the EBG effect can be understood in this interpretation as a dynamic changing of the distance between item 1 and its "ground" when switched patches in a series create a periodic pattern. Large changes in this effective ground plane height give rise to large changes in the effective dielectric constant of the microstrip configuration, thereby creating the EBG effect if repeated in a a regular, periodic manner [2].

Using values of h_1 = 51 µm and h_2 = 1µm for a GaAs IC process, simulations showed promising results for a 12 patch structure that had patches 28 µm wide on 150 µm centers. The main transmission line structure was chosen to be 31 µm wide which gave a

nominal 50 ohm characteristic impedance on 2 mil (50 µm GaAs). All metallization is gold. This structure, if fabricated on a theoretical GaAs IC process was simulated using AWR AXIEM 3D planar EM solver (Figure 6) to have an EBG in the 30-150GHz range depending on quality of the switches, the thru-via configuration, and the metallization among these switching-related structures.

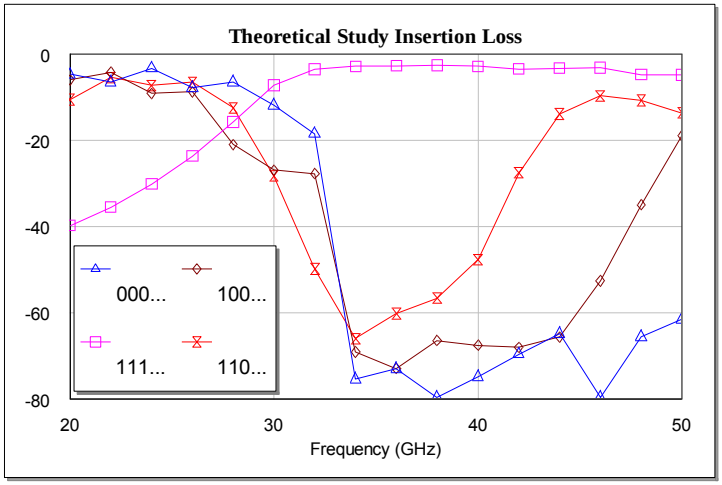

Figure 6– Theoretical study on 50um GaAs IC for 4 dynamic switching states shows expected performance per earlier PCB study.

Implementation and Redesign

The basic design was transitioned to WIN Semiconductor's recently released PP10 GaAs pHEMT process on 50 um substrates. PP10 was chosen mainly because of its very high f_t (160 GHz in wafer-probed PCMs and over 250 GHz for the intrinsic devices in separate unpublished work done by these researchers) would allow the focus of this study to be on metallization configurations rather than switch limitations.

Simulated results in the production PP10 process immediately revealed two shortcomings with PP10 as a candidate process. Firstly, h_2 is a thin 0.15µm rather than the thicker 1µm that had initially been used in the theoretical studies. This by itself had the effect of making the coupling so strong between the transmission line and patches that it was the dominant effect rather than the perturbation to the typical microstrip configuration with the ground plane on the back. Secondly, this was exacerbated by the default WIN metal 2 (transmission line structure) being deposited on top of silicon nitride. While the latter was easily mitigated by using "airbridge" to substitute relatively benign air for the higher dielectric silicon nitride, the former became the focus of an intense and in-depth redesign.

The immediate remedy to this problem was to find a commercial IC process which had a thicker interlayer dielectric among the metallization layers. WIN did not offer such an option, nor did Triquint Semiconductor (USA, GaAs vendor) or Silanna (Australia, silicon on sapphire). It was decided to continue with PP10, again because its superior bandwidth gave greater latitude in observing EBG effects.

A redesign of the structure was undertaken which essentially required minimizing the capacitive coupling between the transmission line on layer 2 and the patches on layer 1 with h_1 = 50µm and h_2=0.15µm, the nominal values for PP10.

The design finally settled upon is somewhat of a departure from all the previous concepts or implementations of EBG structures by this research team. Instead of a continuous patch under the transmission line, the patch is split at the mid-way point under the transmission line and pulled back symmetrically as shown in Figure 7. In this example, the pullback is so extreme as to use purely edge coupling of the EM field lines with no physical overlap. Several different configurations for the pullback where designed and implemented. Simulations using AWR's AXIEM 3D planar EM solver are shown in Figure 8 for a variety of switching configurations. This design technique is referred to as a "split patch" rather than a full patch design.

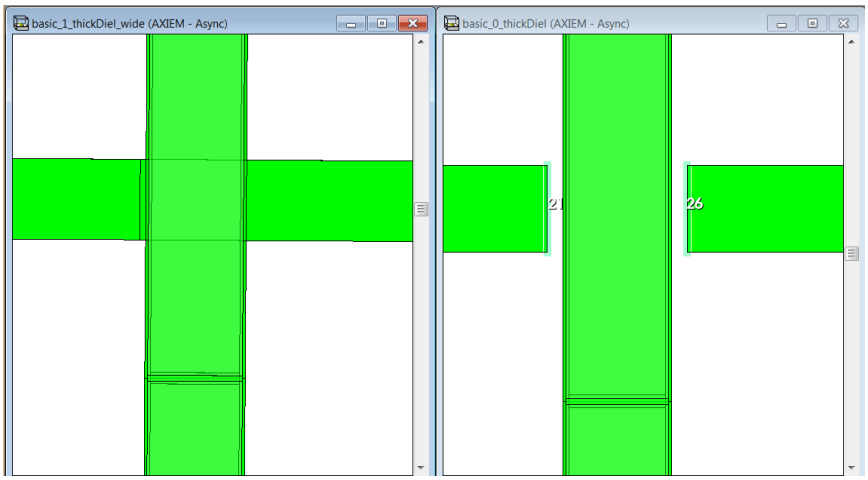

Figure 7 – Traditional (left) versus redesigned (right) IC EBG structure with the path metal (left-to-right) pulled-back from underneath the transmission line (top-to-bottom). The segmentation of the transmission line signifies use the of airspan to anchor the line in air to the substrate at distances prescribed by the PP10 process rules

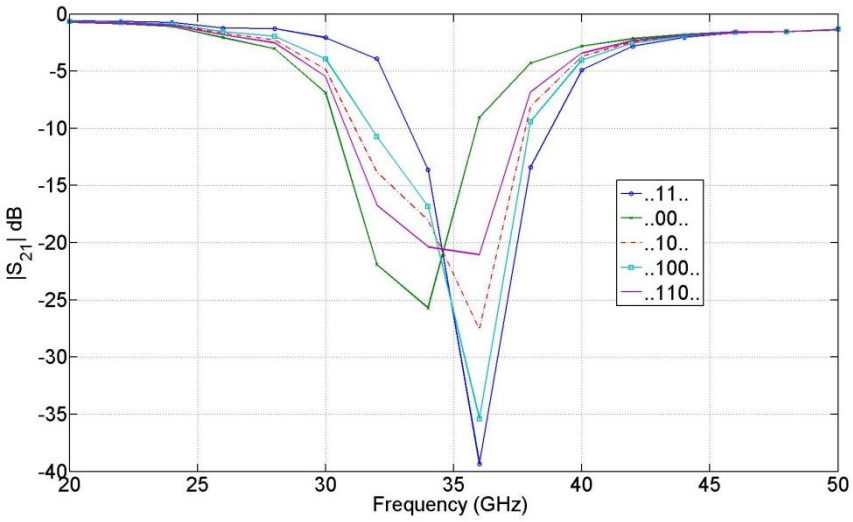

Figure 8 – Simulated results for redesigned configuration shown in Figure 6 (right). Bandwidth and roll-off at band-edge severally degraded from theoretical IC EBG structure.

The most notable feature of this redesign over full patch design with the thin dielectric is the return of some sort of controlled relationship between switching states and transmission characteristics which had been lost with the full (vs split) patch and thinner interlayer dielectric. However, the switching states no longer have as dramatic effect as with the PCB demonstrator or the IC theoretical structures presumably owing to the weaker perturbation to the ground return currents. Also note that as compared to the PCB Demonstrator, the effect of the split patch is to move the lower stopband edge rather than the upper stopband edge.

Fabrication

Basic designs were created based on a 12 pulled-back patch configuration requiring 24 pHEMT switches (Figure 9). This is a factor of 2 smaller configuration than what was used with the PCB demonstrator. This was done to both minimize precious space on the wafer as well as to simplify testing.

One additional challenge driving the reduced patch count was to minimize control voltages to the switches in a desired pattern. To simplify wafer probing, separate designs were included where the patterns were already "hard-wired" onto the IC to minimize the number of probes needed to get the voltages on to the IC. The microwave signal parts of the IC were identical across all designs. However, these designs all had similar, but not identical control, feed lines to the pHEMT switches, thus there are expected to be some differences in the performance from one hard-wired configuration to another. Simulations suggested that these would be minimal. Figure 10 shows one of the designs specifically created to test the 1010… configuration. Additional structures were included to do hard-wired testing of 110 and 001 testing as these are the states which, based on the PCB demonstrator, corresponding to unique transmission characteristics of the EBG structure.

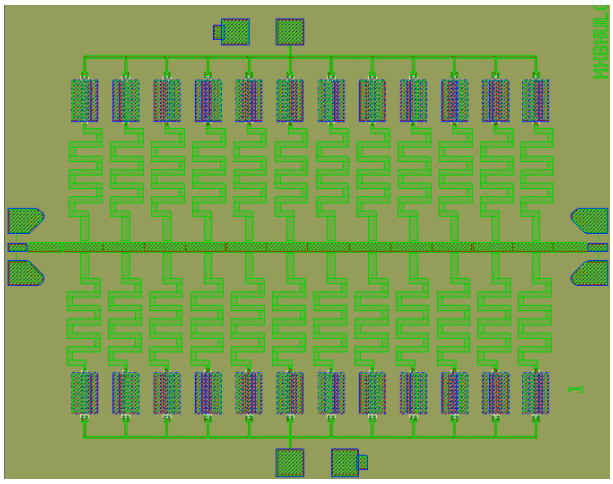

Figure 9 – nominal design used for 111…. And 000… testing

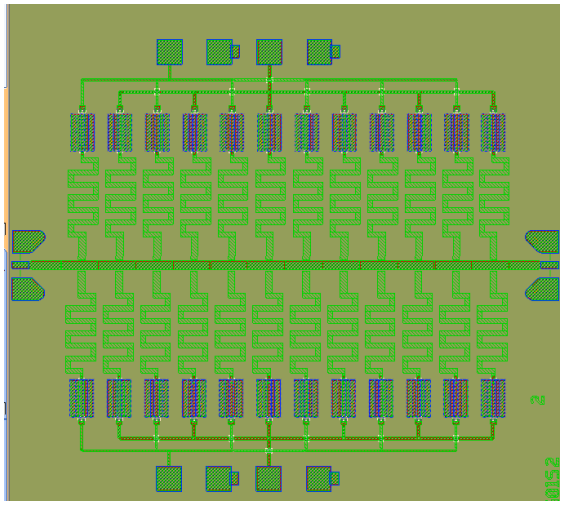

Figure 10 – design used for 1010…. Configuration. Note difference in control lines from top/bottom pads to pHEMT gate as compared to Figure 8.

Designs were fabricated at WIN Semiconductor's Taiwan GaAs foundry in the PP10 process with a wafer thickness of 50um. Wafer-probable samples were delivered with an option for post-test dicing that has not yet been exercised.

Measurement Procedure

S-parameter measurements were taken with an HP8510 vector network analyzer at the wafer level using 67GHz probes from GGB Industries. Data was taken from 10GHz to 50GHz SOLT calibration was done using the on-wafer calibration structures provided by WIN Semiconductor.

Results and Analysis

Initial results on the circuit shown in Figure 9 with the expected performance for the 000… and 111….states simulated in Figure 8 are shown in Figure 11.

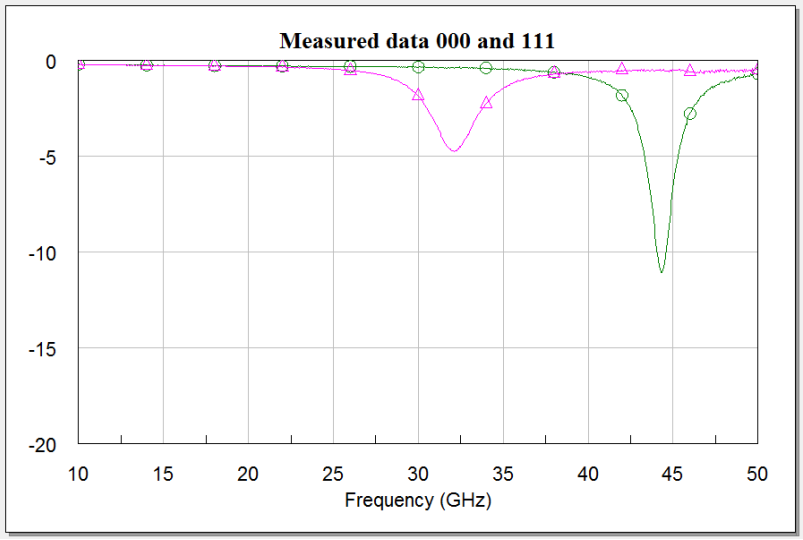

Figure 11 – Measured data for 000... and 111… states.

Two key features of these results are evident as compared to the simulated results. Firstly, one of the stopband edges is not approximately constant. In the simulated and measured (PCB demonstrator) data one of the consistent features of EBG behaviour for this class of structures is the nearly constant lower stopband edge; in the simulated split-patch design the upper band stopband edge is approximately constant. Secondly, there is a resonance in the 000… state data which has not been seen previously in simulation or measurement. When viewed together with the stopband edge phenomena, it appears that this is not an EBG circuit any longer, but instead is a resonant circuit in which the transmission line is coupling and the degree and nature of that coupling shifts the transmission characteristics. This is much more similar to changing the capacitive loading of a circuit, for example, then it is to an EBG effect.

Analysis of this data proceeded by returning to various simulation techniques with the precise layout configurations used, including the pHEMT itself which was initially ignored. Among the EM analyzers used were CST's Microwave Studio FDTD method and our own in-house

CELANE solver. Results for the CELANE solver, comparing these measured data to other states—in the off chance that there was a wiring error in hard-wired state designs—is shown in Figure 12. These data to a large degree confirm the AXIEM simulations but do show among the "simulated configurations" the 000…. state having a resonance.

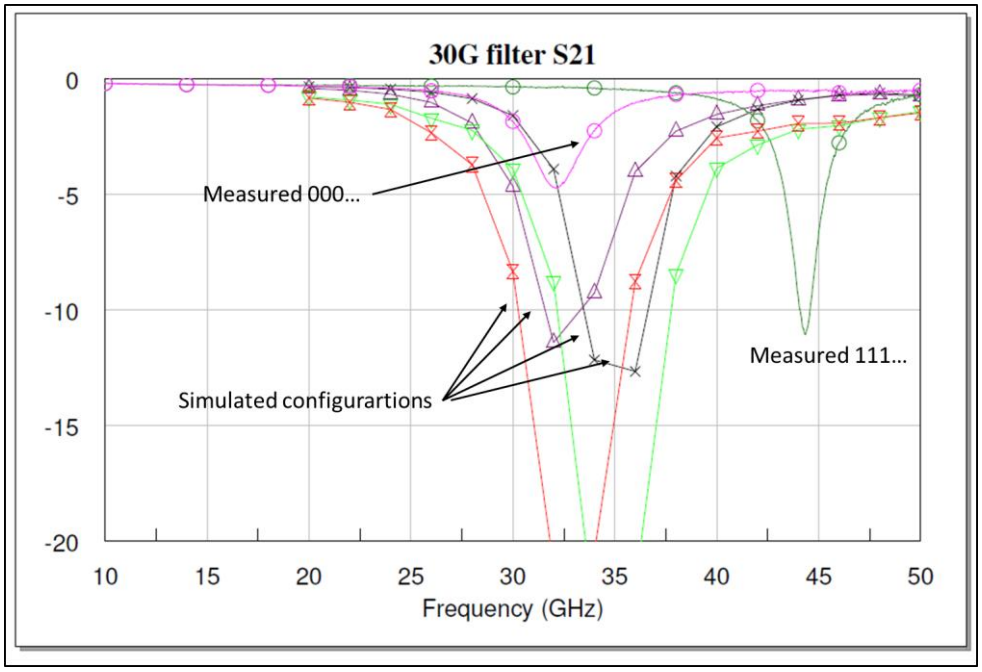

Figure 12 – Measured data (000… and 111… configurations) for CELANE solver data for several configurations, including 000….

The source and nature of this resonance have been the focus of an on-going investigation. Original effort focused on the control lines, but this has not provided any conclusive evidence and the investigation has shifted into two avenues being pursued. In the first, the difference between the EM simulations done with AXIEM and those done with CELANE are shown in Figure 13. The AXIEM simulations have a less dense array of thru-wafer vias while the CELANE simulations have the actual vias, at four per pHEMT switch, so as to provide a good ground for a larger device which gives lower insertion loss [5] (than a smaller switch which have used only 1 via). This supposition is somewhat supported by the fullwave nature of the CELANE solver which would be more likely to incorporate effects on the order of the chip size in three-dimensions which could arise from a resonant box whose walls are composed of these dense vias. Simulations across multiple solvers with simplified structures representing this possibility will be continued beyond the termination of this project.

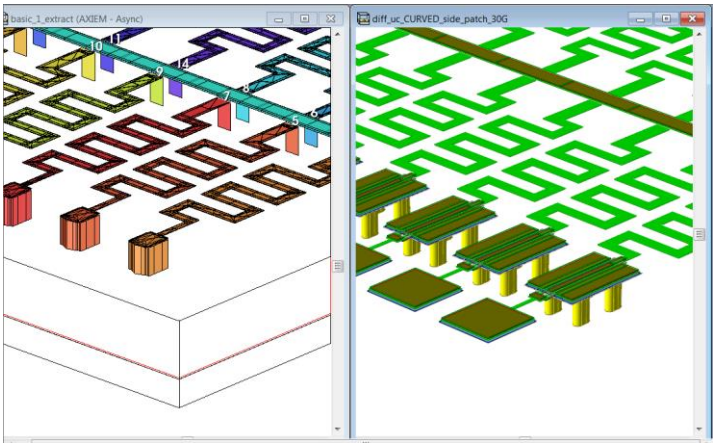

Figure 13 – AXIEM structure fo simplified circuit (right) versus CELANE structure for more complete circuit (left). Note density of vias in the lower portion of each sub-figure.

The second area of investigation is looking at whether EBG behaviour is at all present in this series of design. Clearly the signature marks of EBG propagation (or lack thereof) have not been seen here. However, it is possible that at higher frequency the tell-tale shift to non-propagating values for the propagation constant will be seen and transmission will cease for some finite bandwidth only to be followed by a secondary propagation mode at even higher frequencies. This effort is underway but requires improvements in our calibration technique and an upgrade to our VNA measurement capability to 145 GHz which is expected in H1 2014.

Project Management

This project was awarded in Q2 2012 with funding put in place in Q3 2012. At that time, the PhD student on the PCB Demonstrator project was finishing his thesis and was not available to immediately join this project. Since the time to train a post-doctoral investigator was thought to be in excess of simply waiting for the original PhD student to finish, progress was slow for the first quarter, until the thesis was completed. Because the researcher support was part time on both this project and 124062 "2D Electronically Tuneable EBG Integrated Circuits", the same researcher was brought on to this project. The benefit of this approach was that the researcher was already well-acquainted with the subject area, challenges, and methodologies, however it did push out progress by a quarter.

After one of us (Heimlich) visited Wright Patterson Air Force Base (WPAFB) in January 2012 it was also hoped that instead of a commercial GaAs foundry, WPAFB's semiconductor fabrication facility could be used. WPAFB. Collaborators at WPAFB pursued this but for a variety of reasons it was deemed unavailable to this project by early in H2 2012.

Using the newly released PP10 GaAs pHEMT process from WIN Semiconductor, design began in August 2012. PP10 was selected mainly because of its very high frequency performance which has the potential for lower switching speeds at mm-wave frequencies. We had already completed our first design/measurement cycle on this process on a separate project and had seen good mm-wave performance and in agreement with simulation.

The issue with the redesign has been discussed extensively in the previous technical sections. While disappointing that the PCB Demonstrator performance was not to be "cut-and-paste" on to an IC, it was rewarding in its own right because of the challenge of getting EBG performance in a more demanding form factor.

Redesign with the split-patch technique occurred in October with designs in several configurations of microwave and mm-wave frequencies and unit cell patterns completed. Layout was finished in November and manufacturing readiness (DRC/LVS and reticule generation) was completed in early December. Tape-out to WIN's Taiwan manufacturing facility occurred in mid-December. Circuits completed fabrication in February 2013 and were received in early March 2013.

During the fabrication of the circuits at WIN, the post-doc working on the project took a full-time position at a company near Macquarie University and was being retained part-time on the project to complete the testing of the PP10 circuits, but this fell through about half-way thorugh the testing mainly due to the testing difficulties. A 6 month extension to the project was lodged in June 2013 due to this and the other, previous delays to the progress.

Testing took place in April-June and was made difficult by the calibration with extra DC probes in place as well as because of the unexpected nature of the results. One of us (Matekovits) oversaw testing until a new post-doc was secured for the project in July-August 2013.

Pending the results of testing the first iteration designs, we planned a second run to improve the performance. This redesign and fabrication would have been done in time for a short period of testing before the new official December 2013 close to the project. The unexpected measurement results from the first-pass circuits have led to an extensive period of post-measurement analysis which has yet to yield conclusive results, but which has precluded releasing a second set of designs.

Work will continue on this project at least for the near-term based on our ability to leverage our progress accomplished under this funding for an Australian Research Council (ARC) Discovery Project grant which will run from 2013-2016.

Project Outcomes

As we have yet to ascertain a root cause for the departure among simulated and measured data for the split-batch EBG IC design(s) we have not been in a position to publish our results. However, there have been several related outcomes which would not have occurred without AOARD funding of this project.

First, an innovation disclosure has been prepared internal to Macquarie University for the split-patch design technique. This is the first step in our patent application process. Should this pass review of this initial process, the split-patch design technique and related circuits would be submitted to the formal international patent process. Should this progress beyond an internal review, AOARD will be informed

Second, while the PhD student from the PCB Demonstrator project did not see this project through to completion, the weight of activity in this area allowed us to attract a second PhD student who used our AOARD-funded work as a springboard to his research. While no funding from any AOARD project has been used in his research and he has not directly contributed to this project, his research outputs would not be such as there without the AOARD projects. Publications by this PhD student with the AOARD team as co-authors are given in the reference section as references 7-9.

Finally, the critical mass of research in this area at Macquarie University and Politecnico di Turino enabled us to successfully apply for an ARC Discovery Project in 2012 with funding commencing in 2013. This is a 3-year project with $AUS 450K funding from ARC plus additional internal University support. The EBG work done here will be extended under this project to leaky-wave structures and beam steering techniques leveraging what has been learned under the AOARD series of projects from 2010 to 2013.

Conclusion

Leveraging the EBG PCB Demonstrator into an IC configuration has been attempted. Lack of an available semiconductor fabrication process with the desired characteristics led to an innovate redesign of the EBG IC circuits with expected narrower bandwidth in the 30-50GHz range. A variety of configurations were fabricated and tested in WIN Semiconductor's PP10

mm-wave process. Measured results did not agree with simulated data and is the subject of continuing investigation.

Several project management challenges arouse during the course of this project. The project was delayed in starting due to availability of appropriate personnel and then once they were on the project, left at a critical time in the project execution. Similarly, availability of a semiconductor process with thicker inter-metal dielectric would have simplified progress; progress was made nonetheless in transitioning a PCB design onto IC for potential high integration functionality. An extension of 6 months was applied for and granted in light of this.

While these setbacks limited the overall outcomes, several key outcomes have been enabled by project funding. A new, innovative EBG circuit design technique has been developed. Follow-on funding for 3 years by the Australian Research Council has been enabled by this project and will allow us to pursue some of the analysis suggested here but which will extend beyond this project's completion date.

ACKNOWLEDGEMENT

The researchers would like to thank Dr. Gregg Jessen for his support in the proposal and early phases of this project. Without his keen interest, this project and the potential collaboration which arouse from a visit to WPAFB would not have been possible. We gratefully acknowledge the stewardship of Lt. Col David Hopper, PhD in his recommendations for project extension and the preparation of documentation for this project.

References

[1] L. Matekovits, G. Vietti Colomè, M. Orefice, ―Controlling the Bandlimits of TE-Surface Wave Propagation Along a Modulated Microstrip-Line-Based High Impedance Surface,‖ IEEE Trans. Antennas and Propagat., Vol. 56, No. 8, August, 2008, pp. 2555–2562.

[2] L. Matekovits, M. Heimlich, K. Esselle, "Tunable Periodic Structures on GaAs Wafer, Progress in Electromagnetics Research (PIER) Vol. 97, October 2009.

[3] D. N. P. Thalakotuna, L. Matekovits, M. Heimlich, K. P. Esselle, "Harnessing the Properties of Periodicity Towards Achieving Reconfigurable Wide Stopbands in Microwave Frequencies", IEEE Microwave and Wireless Components Letters, September 2011.

[4] D. N. P. Thalakotuna, L. Matekovits, M. Heimlich, K. P. Esselle, "Dynamic Tuning of Electromagnetic Bandgap", Proceedings of 5th European Conference on Antennas and Propagation (EuCAP) 2011, 11-15 April 2011, Rome, Italy.

[5] L. Matekovits, D. N.P. Thalakotuna, M. Heimlich, K.P. Esselle, "Investigation on FET Switch Integration Techniques for a Tunable Microwave Periodic Structure"
Proceedings of 2012 8th IEEE International Workshop on Antenna Technology: Small Antennas and Unconventional Applications (IWAT2012), Tucson, USA, March 2012.

[6] D. N.P. Thalakotuna, L. Matekovits, K.P. Esselle, S. G. Hay, **M. Heimlich**, "Dispersion Analysis of a Reconfigurable Unit Cell in a One Dimensional Periodic Architecture" Proceedings of 6th IEEE European Conference on Antennas and Propagation (EuCAP 2012), Prague, Czech Republic, March 2012.

[7] D. Karmokar, D. Thalakotuna, K. Esselle, L. Matekovits, M. Heimlich, "Reconfigurable half-width microstrip leaky-wave antenna for fixed-frequency beam scanning", Proceedings of 7th IEEE European Conference on Antennas and Propagation (EuCAP 2013),pp 1314-1317., The Haque, The Netherlands. April 2013.

[8] D. Karmokar, D. Thalakotuna, K. Esselle, M. Heimlich, L. Matekovits "A leaky-wave antenna for beam steering in forward and backward directions ", IEEE Region 10 Spring Conference, pp 47-50, Sydney Ausralia, April 2013.

[9] D. Karmokar, D. Thalakotuna, K. Esselle, M. Heimlich, L. Matekovits, "Fixed-frequency beam steering from a stub-loaded microstrip leaky-wave antenn ", Proceedings of the 13th International Symposium on Electromagnetic Theory (EMTS), pp 436-439, Hiroshima Japan, May 2013.