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Electrical transport and low-frequency noise in chemical vapor deposited single-layer MoS_2 devices

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Abstract

We have studied temperature-dependent (77–300 K) electrical characteristics and low-frequency noise (LFN) in chemical vapor deposited (CVD) single-layer molybdenum disulfide (MoS_2) based back-gated field-effect transistors (FETs). Electrical characterization and LFN measurements were conducted on MoS_2 FETs with Al_2O_3 top-surface passivation. We also studied the effect of top-surface passivation etching on the electrical characteristics of the device. Significant decrease in channel current and transconductance was observed in these devices after the Al_2O_3 passivation etching. For passivated devices, the two-terminal resistance variation with temperature showed a good fit to the activation energy model, whereas for the etched devices the trend indicated a hopping transport mechanism. A significant increase in the normalized drain current noise power spectral density (PSD) was observed after the etching of the top passivation layer. The observed channel current noise was explained using a standard unified model incorporating carrier number fluctuation and correlated surface mobility fluctuation mechanisms. Detailed analysis of the gate-referred noise voltage PSD indicated the presence of different trapping states in passivated devices when compared to the etched devices. Etched devices showed weak temperature dependence of the channel current noise, whereas passivated devices exhibited near-linear temperature dependence.

Keywords: 2D materials, low-frequency noise, MoS_2, flicker noise, generation recombination (G–R) noise

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(Some figures may appear in colour only in the online journal)

1. Introduction

Graphene's high carrier mobility and saturation velocity are very attractive features, but the lack of inherent band gap is a challenge for switching applications and low-power electronics [1]. This has led to an exploration of alternative two-dimensional (2D) semiconductor materials. In recent years, molybdenum disulfide (MoS_2) has attracted significant

interest due to the observation of an indirect (1.29 eV) to direct (1.8 eV) band gap transition in monolayer films [2], which opens up exciting possibilities of realizing low-power, high-speed electronic, and optical devices on flexible substrates. MoS_2 transistors have exhibited high on–off ratios ($\sim 10^7$), and have shown a subthreshold swing of 74 mV/decade [3]. Combined with high thermal stability and chemical robustness [3, 4], it promises to play an important role in future generation electronics. Few of the recently explored fields include digital electronics [5–7], chemical sensing [8], valley polarization [9, 10], photovoltaics, and photocatalysis [11, 12]. Most of these applications require low distortions in the conduction process and often $1/f$ noise is the most dominant noise mechanism at low frequencies. Numerous studies have been conducted to understand and reduce $1/f$ noise in conventional metal–oxide field-effect transistors (MOSFETs) [13–17]. Recently, various groups have also studied $1/f$ noise in graphene devices [18–20], and lately on MoS_2 FETs [21]. Particularly for MoS_2 devices, there exists a lack of understanding of the dominant mechanisms responsible for the observed current noise. The study of the effect of passivation on LFN in these 2D materials is critical for understanding of the current noise, which is essential for future device applications.

In this paper, we explore the effect of top-surface passivation on the transport and LFN in single-layer MoS_2 FETs. Temperature-dependent (77–300 K) transport and LFN measurements in single-layer MoS_2 back-gated FETs with and after etching Al_2O_3 passivation are presented. We observed significant nonlinearity and an order of magnitude reduction of channel current after the top passivation layer was etched. Temperature-dependent two-terminal resistance of the passivated devices showed a clear fit to the activation energy model for the entire temperature range (77–300 K), suggesting a band-like transport. For the etched devices two different regimes were identified, indicating a defect-mediated transport. LFN measurements were conducted at various temperatures on both the passivated and etched devices at various back-gate biases. We calculated Hooge parameters in the range of 0.01–0.0001 and 5–0.01 for passivated and etched devices, respectively. The observed gate-dependent noise in both passivated and etched devices could be explained by carrier number fluctuation arising from random trapping and de-trapping of the channel charge carried by the oxide interface traps and correlated surface mobility fluctuation arising from fluctuation of the scattering rates of these traps [22, 23]. Temperature-dependent noise measurement also showed very different behavior for passivated and etched devices.

2. Material and methods

Monolayer MoS_2 films were grown directly on a SiO_2-coated (285 nm) Si substrate using the procedure described in detail by Najmaei *et al* [24]. In brief, high aspect-ratio MoO_3 nanoribbons were used as precursor along with sublimated sulfur in a chemical vapor deposition chamber. The growth process resulted in single crystal MoS_2 triangles with a side length of (13 ± 2.5) μm. Electron-beam lithography (EBL) was used to fabricate variable channel length FETs directly onto the single-layer material avoiding grain boundaries and other defects. The MoS_2 layer was patterned using a CH_4/O_2 plasma etch, and source and drain contacts were formed by depositing Ti/Au (15 nm/85 nm) using an electron-beam evaporator. A 20 nm thick Al_2O_3 dielectric was deposited over the samples using atomic layer deposition (ALD), with O_2 plasma and tetramethyl aluminum (TMA) precursors. For the measurements on unpassivated devices, Al_2O_3 was selectively etched by placing it in MIF300 developer (tetramethylammonium hydroxide based metal–ion free developer) for 30 min at room temperature, followed by a de-ionized water/acetone/isopropanol rinse. Additional details about the processing steps can be found in [25].

The temperature-dependent parametric measurements were performed in an open-cycle cryogenic probe station from Lakeshore using an Agilent B1500A semiconductor parameter analyzer (disclaimer in the notes section). LFN measurements were performed using a cross-correlation technique to minimize the effect of instrument noise [26]. The source–drain bias was provided by the internal batteries of the two independent SRS 570 amplifiers and the gate bias was provided using an independent battery source. A double channel dynamic spectrum analyzer HP 35670A was used in cross-spectrum mode to measure the PSD of the channel current. The LFN measurements were conducted between 1 and 1000 Hz, with frequency resolution of 0.25 Hz and the data was averaged over 20 sets of readings. The temperature-dependent LFN measurements were performed from 77 to 300 K, starting from the lowest temperature.

3. Results and discussion

Figures 1(a) and (b) show the drain–source current (I_{DS}) versus drain–source voltage (V_{DS}) characteristics of a MoS_2 transistor at 300 K with gate length (L) and width (W) of 400 nm and 1000 nm, respectively, before and after etching of the top Al_2O_3 passivation layer. Measurements were performed on both passivated and etched devices in vacuum with chamber pressure in the range of 10^{-3} Pa. The inset of figure 1(a) shows a scanning electron microscope (SEM) image of a typical device. Significant reduction of the channel current (almost an order of magnitude) and non-linearity in the current–voltage characteristics were observed for devices after the passivation was removed (figure 1(b)). A transfer characteristics plot (I_{DS} versus V_{GS} at $V_{DS} = 0.5$ V) is shown in figure 1(c) for the same device with passivation and after passivation has been removed. Clear depletion-mode n-channel behavior can be seen in these devices, which is in good agreement with what has been also observed by other groups [2, 3, 27]. The field-effect mobility (μ_{FE}) for these devices was calculated using the following equation:

$$\mu_{FE} = \frac{\partial I_{DS}}{\partial V_{GS}} \frac{L}{W C_{OX} V_{DS}}, \quad (1)$$

where C_{OX} is the gate capacitance per unit area, L is the channel length, W is the channel width, V_{DS} is the source–drain voltage, and $\partial I_{DS}/\partial V_{GS}$ is the slope of the

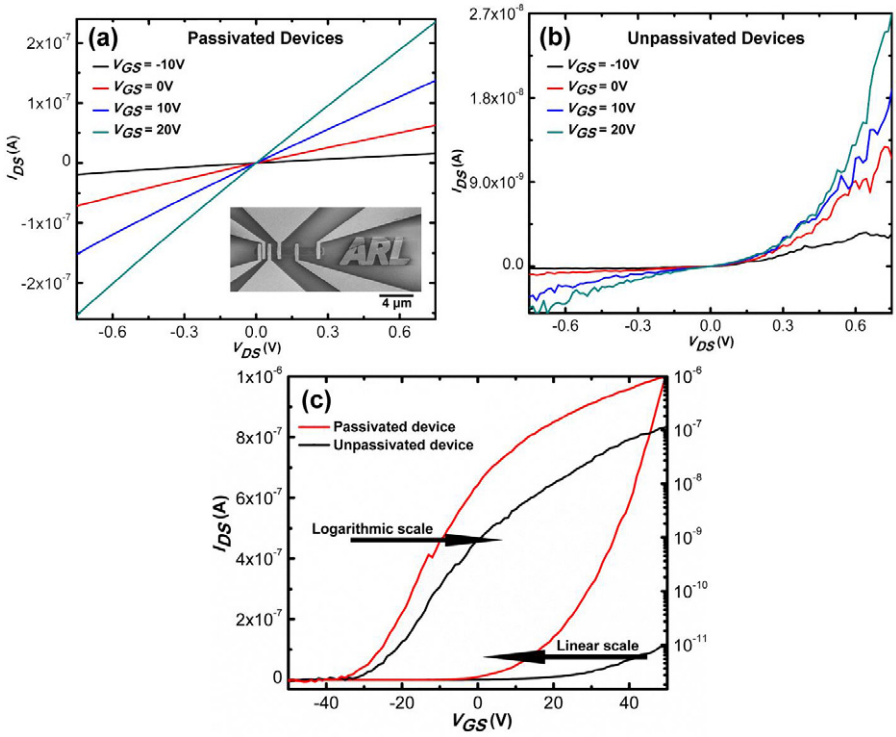

Figure 1. I_{DS}–V_{DS} plot at 300 K for MoS_2 FET (a) before and (b) after etching of the top passivation. All the I–V curves were taken at constant drain–source voltage ($V_{DS} = 0.5$ V). The inset in (a) shows an SEM micrograph of a typical device. (c) I_{DS}–V_{GS} plot of the passivated and unpassivated devices plotted in both linear and logarithmic–linear scales at 300 K.

I_{DS}–V_{GS} characteristics taken in the linear region. At 300 K the measured field-effect mobility values were (35.5 ± 2.5) cm^2 V^{-1} s^{-1} and (12.1 ± 1.9) cm^2 V^{-1} s^{-1} for passivated and etched FETs, respectively. All mobility values were measured using four-probe measurement techniques on Hall bar devices at a I_{DS} of 500 fA, to reduce the contribution of the contact resistances.

The two-terminal channel resistance for these MoS_2 FETs as a function of measurement temperature is shown for both passivated and etched samples in figure 2. The passivated devices exhibited a good fit to the activation energy model at different gate biases over the entire measurement temperature range, i.e., 77–300 K, as is evident in figure 2(a). This indicates a transport mechanism involving well-defined bands. Using the relationship [22]

$$\ln(R) = \ln(R_0) + E_a/2k_B T, \qquad (2)$$

where R_0 is the intercept, E_a is the thermal activation energy of the dopant, k_B is the Boltzmann constant and T is the absolute temperature, we can calculate the activation energy for conduction in these devices. From the slopes of different curves at different back-gate biases it is clear that the activation energy decreases with increasing back-gate bias (figure 2(a)). On the other hand, etched devices showed two different regimes of conduction for the entire investigated temperature range, with higher activation energy between 200 and 300 K, and weaker temperature dependence between 77 and 200 K, for all three back-gate biases (figure 2(b)). The calculated activation energies at 20 V back-gate bias were ≈56 meV for passivated devices and ≈32 meV (in the 200–300 K temperature range) for etched devices. In a recent report, Radisavljevic and Kis measured the temperature dependence of the conductance in monolayer MoS_2 back-gated FETs (unpassivated) as a function of back-gate bias [28]. Although a thermally-activated transport model was used to explain the trend, the fit was evident only for temperatures between 166 and 250 K, below which the conductance showed very weak temperature dependence. Surprisingly, the activation energy (computed from their data) is in the range of 20–60 meV for back-gate biases ranging from 2 to 40 V. A very similar trend was also observed by Ayari *et al* for two-probe conductance variation with temperature for unpassivated MoS_2 monolayers [29]. The calculated activation energy for their result is close to 50 meV for 9 V back-gate bias. The close agreement of the activation energy values for conduction obtained in MoS_2 samples fabricated by different methods might indicate the presence of a native defect, which manifests itself as a shallow donor in monolayer materials. Very recently, Qiu *et al*, reported a very similar trend for temperature-dependent conduction in single-layer MoS_2 FETs and successfully explained the observed trend using hopping conduction through defect-induced localized states [30]—they concluded that the responsible defects were sulfur vacancies. Comparing our results on passivated devices, it is clear that the top-surface passivation renders these surface defects inactive and could be partially responsible

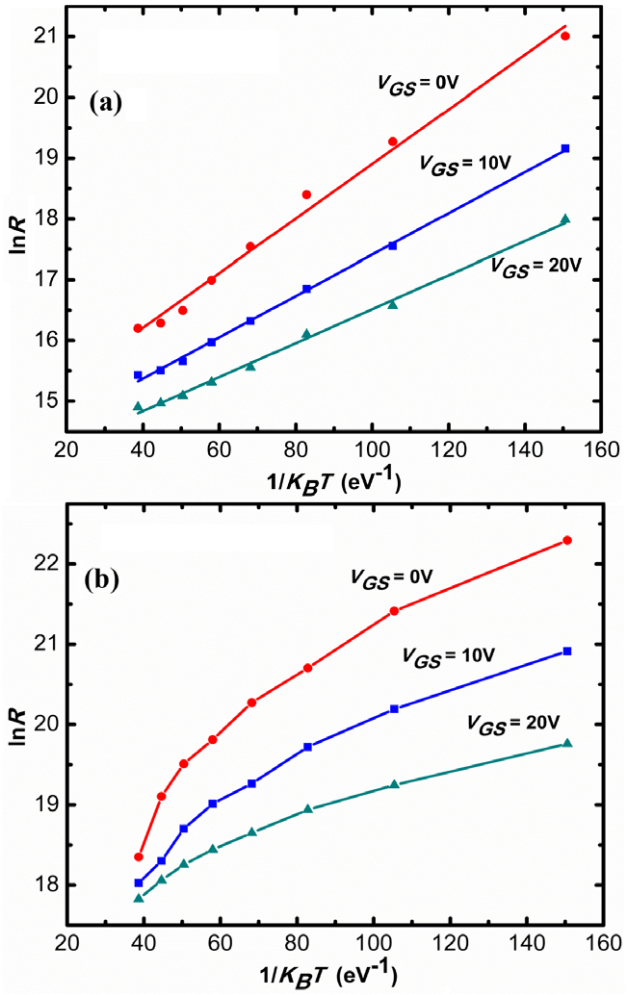

Figure 2. Arrhenius plot of the drain–source resistance of the passivated and unpassivated (after etching of the top passivation) FETs at three different gate biases is shown in (a) and (b), respectively. Temperature is in the range of 77–300 K. All the readings were taken at a constant drain–source voltage ($V_{DS} = 0.5$ V).

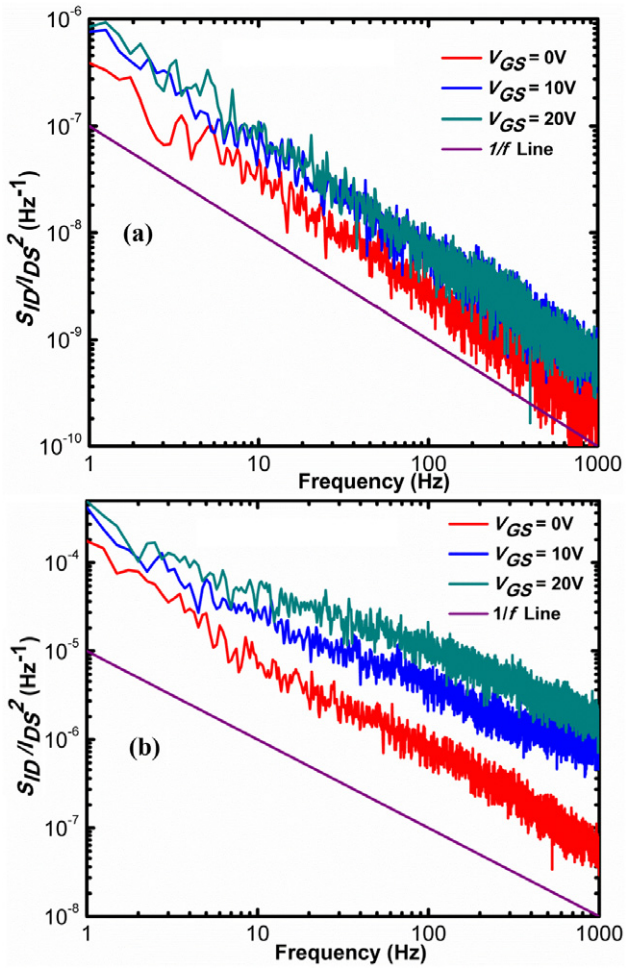

Figure 3. Room temperature ($T = 300$ K) normalized PSD of the drain current for (a) passivated and (b) unpassivated (after etching of the top passivation) devices at different V_{GS}. A $1/f$ trend line is shown for comparison. All the readings were taken at a constant drain–source voltage ($V_{DS} = 0.5$ V).

for the improved electrical characteristics observed for MoS_2 devices. Raman spectroscopy measurements (see supplemental section available at stacks.iop.org/Nano/25/155702/mmedia) on etched devices did not indicate any significant structural damage to the MoS_2 layer due to passivation etch.

The normalized drain current PSD ($= S_{ID}/I_{DS}^2$) for both passivated and etched devices measured at 300 K at three different gate biases is shown in figures 3(a) and (b). An increase of almost two orders of magnitude in the normalized drain current PSD was observed after the etching of the passivation layer. When V_{DS} was varied from 0.2 to 2 V, the normalized PSD did not change, indicating that the measured noise is originating from the channel, with minimal contribution from the contacts. The S_{ID}/I_{DS}^2 at 10 Hz were in the range of (1–10) $\times 10^{-8}$ Hz^{-1} and (1–10) $\times 10^{-5}$ Hz^{-1} for passivated and etched devices, respectively. In the case of graphene devices, several groups have reported S_{ID}/I_{DS}^2 in the range of 10^{-9} Hz^{-1} to 10^{-7} Hz^{-1} at 10 Hz [19, 20, 31].

Irrespective of the mechanisms responsible for the noise, for a device exhibiting $1/f$-type noise, the measured PSD can always be described using Hooge's empirical relationship:

$$S_{ID}/I_{DS}^2 = \alpha_H/Nf^{\beta}, \quad (3)$$

where α_H is the Hooge constant, β (exponential factor) is ideally 1 and N is the total number of carriers approximated as $N = (V_{GS} - V_T) \times L \times W \times C_{OX}/q$ where q is the charge of an electron, V_{GS} is gate to source voltage, and V_T is the estimated threshold voltage. Although for 2D materials, the validity of the model is questionable, it provides a figure of merit, i.e., Hooge constant, which allows for direct comparison of the noise levels in various devices. In our case the calculated variation in β is 1 ± 0.2 for etched devices and 1 ± 0.09 for passivated devices. The calculated Hooge parameter ranges are between (0.01 and 0.0001) and (5 and 0.01) for passivated and etched devices, respectively. Recently, a Hooge parameter ranging between 0.005 and 2 has been reported for unpassivated MoS_2 FETs [21].

We have used the 'unified model' which takes into account both carrier number fluctuation along with correlated mobility fluctuation to explain the observed LFN trends in these devices.

Carrier number fluctuations arise from dynamic trapping and de-trapping of free carriers by oxide–semiconductor interface traps. In addition, trap charge fluctuations may result in scattering rate fluctuations, which causes fluctuation of the inversion layer mobility. It is worth pointing out that the Hooge mobility fluctuation is a bulk effect, whereas the correlated mobility fluctuation is a surface effect resulting from carrier number fluctuation through interface traps. In analyzing the noise, we have used the framework proposed by Ghibaudo *et al*, where normalized drain current spectral density ($S_{ID}/I_D{}^2$) and input-referred gate-voltage spectral density (S_{VG}) are given by the following relationships [22, 23]:

$$\frac{S_{ID}}{I_D{}^2} = \left(1+\alpha\mu_{eff}C_{OX}\frac{I_D}{g_m}\right)^2\left(\frac{g_m}{I_D}\right)^2(S_{VFB}) \quad (4)$$

$$S_{VG} = S_{VFB}\left[1+\alpha\mu_{eff}C_{OX}\left(V_{GS}-V_T\right)\right]^2, \quad (5)$$

where α is the Coulomb scattering coefficient ($\approx 10^4$ V s C^{-1} for electrons and $\approx 10^5$ V s C^{-1} for holes), μ_{eff} is the low-field effective mobility, C_{OX} is the gate capacitance, V_T is the threshold voltage and S_{VFB} is the flat-band voltage spectral density. The S_{VFB} is related to interface charge spectral density per unit area (S_{Qit}) as $S_{VFB} = S_{Qit}/(WLC_{OX}{}^2)$. It should be mentioned that equations (4) and (5) are generally valid for inversion-mode MOSFETs [22, 23]. Although MoS_2 FETs presented in this study are *n*-channel depletion-mode devices, the close proximity of the channel charge carriers to the interface can lead to similar fluctuation mechanisms as in inversion-mode FETs. In our case, all measurements were performed in the linear region of operation. The dominant mechanism can be highlighted by plotting the normalized drain current spectral density as a function of drain current (I_{DS}) in a log–log scale. In the case of Hooge's mobility fluctuation, i.e., bulk mobility fluctuation, the normalized drain–current PSD should be proportional to $1/I_{DS}$. If the normalized drain–current PSD varies with the drain current as $(g_m/I_{DS})^2$, i.e., $S_{ID}/I_{DS}{}^2 \propto (g_m/I_{DS})^2$, then it is likely that the carrier number fluctuation is the dominant source of the $1/f$ noise. Moreover, if the associated gate-referred voltage PSD (S_{VG}) exhibits parabolic gate-voltage dependence, then correlated mobility fluctuation is also present. Figures 4(a) and (b) present $S_I/I_{DS}{}^2$ as a function of drain current in a log–log plot. It is worth pointing out that significant variation in $S_I/I_{DS}{}^2$ as a function of I_{DS} is observed by varying V_{GS} in a wide range of values. As is evident from figure 4(a) the passivated device demonstrates a near-ideal fit. The deviation at higher drain currents is due to the excess noise from the source/drain contact resistances [22]. For etched devices (figure 4(b)) the agreement is not exact. Figures 5(a) and (b) present gate-referred voltage PSD (S_{VG}) as a function of (V_{GS}–V_T). For both passivated and etched devices the parabolic dependence is evident, indicating that correlated mobility fluctuation is also present. In the absence of correlated mobility fluctuation, the gate-referred noise voltage will be constant as a function of gate bias. For passivated devices, a minimum in the plot of gate-referred voltage PSD as a function of (V_{GS}–V_T) is observed. Interestingly, Ghibaudo

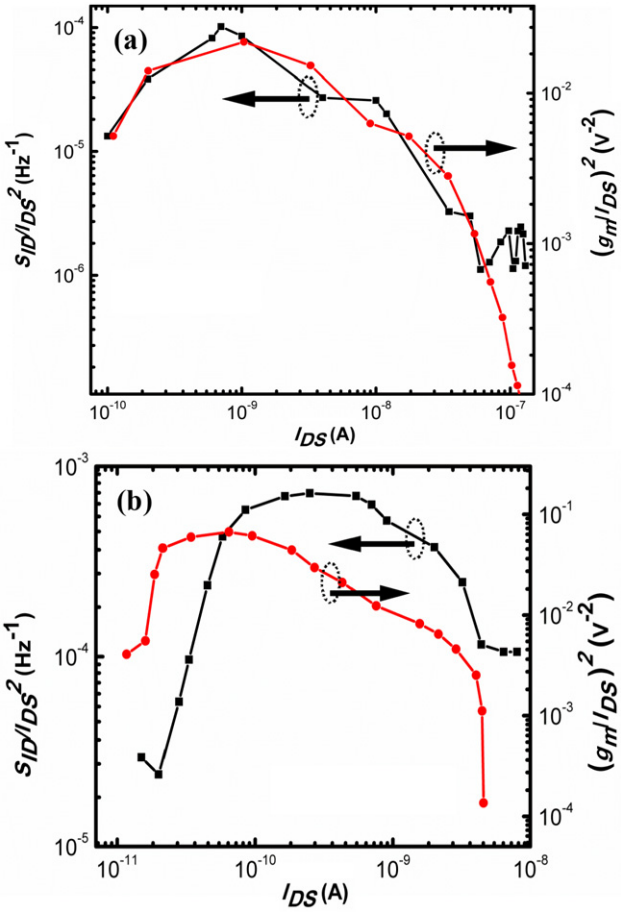

Figure 4. Comparison of normalized PSD of the drain current at $f = 1$ Hz and $(g_m/I_{DS})^2$ at different I_{DS} for passivated and unpassivated (after etching of the top passivation) devices in (a) and (b), respectively. All the readings were taken at a constant drain–source voltage ($V_{DS} = 0.5$ V).

et al demonstrated that by mixing acceptor- and donor-like traps in the noise model, one can generate a minimum in the parabolic plot of gate-referred voltage PSD, whereas a pure acceptor-like trap has no minimum, as seen in the case of the etched devices [23].

Figure 6 presents temperature-dependent $S_I/I_{DS}{}^2$ at 10 Hz for both etched and passivated devices at three different gate biases. The drain current noise in the etched device shows very weak temperature dependence at all three gate biases. This could indicate that the physical trapping mechanism responsible for $1/f$ noise is dominated by a tunneling process. In contrast, the nearly linear normalized drain current spectral density at 0 V gate bias indicates a more thermally-activated trapping process [22, 23]. However, the reason behind the increase in noise due to positive gate bias in the case of passivated devices is not clear. It is also interesting to note that the temperature-dependent field-effect mobility measured on passivated and etched devices showed very similar trends, i.e., the measured field-effect mobility had linear dependence with temperature for the passivated devices, whereas for the etched devices the mobility showed very weak temperature dependence [25]. We can speculate that the nature of transport

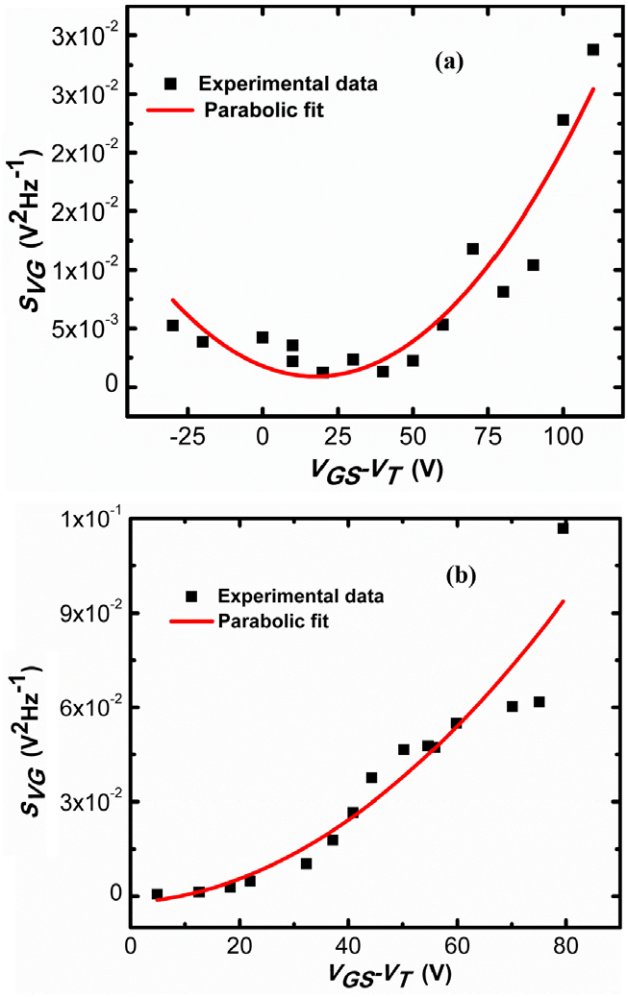

Figure 5. The experimental input gate-referred PSD voltage obtained at different V_{GS} values for (a) passivated and (b) unpassivated (after etching of the top passivation) devices. Parabolic fit to the measured data points is also shown. All the readings were taken at a constant drain–source voltage ($V_{DS} = 0.5$ V).

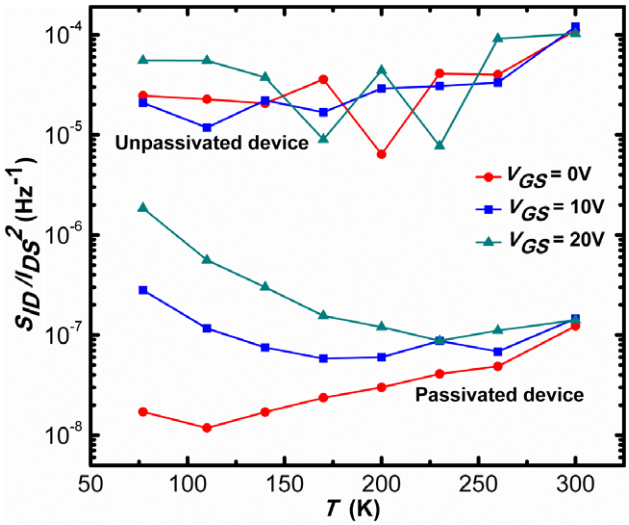

Figure 6. Temperature-dependent (77–300 K) normalized PSD of the drain current noise at $f = 10$ Hz at different temperatures for passivated and unpassivated (after etching of the top passivation) devices. All the readings were taken at constant drain–source voltage ($V_{DS} = 0.5$ V).

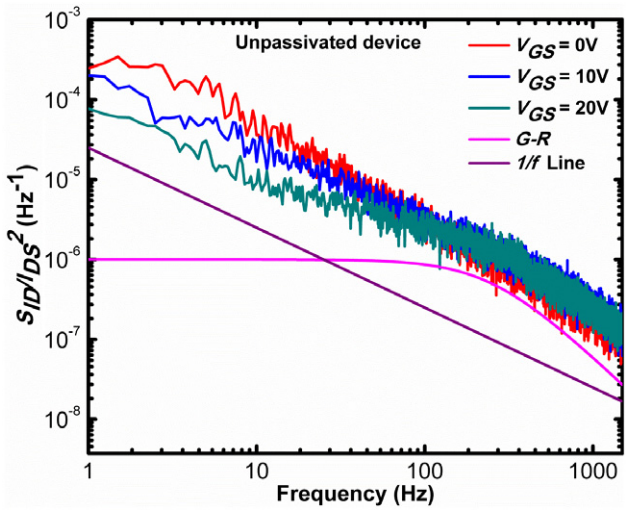

Figure 7. Normalized PSD of the drain current noise for unpassivated (after etching of the top passivation) devices at $T = 170$ K. The $1/f$ trend line as well as ideal single time constant Lorentzian-type PSD, i.e. $S_I = A/(1 + (f/f_0)^2)$ due to G–R noise are shown for illustration. The green line (PSD at $V_{GS} = 20$ V) clearly indicates the presence of G–R noise in addition to excess $1/f$ noise. All the readings were taken at constant drain–source voltage ($V_{DS} = 0.5$ V).

is different in passivated and etched devices, which ultimately determines the temperature-dependent characteristics of noise in the single-layer MoS_2 devices.

Etched devices showed the presence of Lorentzian peaks associated with generation–recombination (G–R) noise in addition to $1/f$ noise. However, for all the etched devices, transition from G–R to $1/f$ and vice versa was observed during the course of repeated measurements. The PSD associated with G–R noise exhibits a Lorentzian behavior, i.e., $S_{ID} = A/(1 + (f/f_0)^2)$, where A is the low-frequency amplitude and f_0 is the characteristic frequency. Figure 7 shows the PSD of an etched device at 170 K exhibiting G–R related Lorentzian shape in addition to the excess $1/f$ noise. In the case of graphene, few groups have reported G–R noise and this is attributed to defects on the edges of Graphene channels giving rise to a characteristics time constant in the fluctuations of carriers [20]. A recent report by Sangwan *et al* also showed the presence of G–R peaks at low temperature in unpassivated MoS_2 devices [21]. The single time constant Lorentzian peaks in $1/f$ PSD is due to the presence of discrete traps or G–R centers within the band. For unpassivated devices this could result from the defect sites on the top surface of the MoS_2 film. However, the unstable nature of the G–R peaks observed in unpassivated devices might be associated with adsorption of molecules at surface defect sites. For example, Balandin *et al* clearly showed the evolution of characteristic Lorentzian peaks in $1/f$ spectra in graphene devices, due to the adsorption of specific molecules [18].

4. Conclusion

In summary, we have examined the effects of passivation on transport and LFN in single-layer MoS_2 FETs. Temperature-dependent resistance measurements in single-layer MoS_2 FETs passivated with ALD-deposited Al_2O_3 indicated a band-like transport mechanism, whereas for etched devices weak temperature dependence of the resistance pointed to a defect-mediated transport mechanism. It was clear that top-surface passivation significantly reduces the drain current noise. For both passivated and etched devices, the bias-dependent LFN at 300 K can be explained by carrier number fluctuation and correlated mobility fluctuation; both related to surface effects. Correlation to the bulk mobility fluctuation model (Hooge's model) was not observed. Temperature-dependent noise measurements showed very weak dependence for etched devices compared to passivated devices. In general, the findings presented in this paper should contribute to the much needed advancements in 2D material interface engineering for device applications.

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