ARMY RESEARCH LABORATORY

Monolithic Microwave Integrated Circuit (MMIC) Frequency Doublers—2nd Pass Correction

by John E. Penn

ARL-TN-0580 **September 2013**

NOTICES

Disclaimers

The findings in this report are not to be construed as an official Department of the Army position unless so designated by other authorized documents.

Citation of manufacturer's or trade names does not constitute an official endorsement or approval of the use thereof.

Destroy this report when it is no longer needed. Do not return it to the originator.

Army Research Laboratory
Adelphi, MD 20783-1197

ARL-TN-0580 **September 2013**

Monolithic Microwave Integrated Circuit (MMIC) Frequency Doublers—2nd Pass Correction

John E. Penn
Sensors and Electron Devices Directorate, ARL

REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-0188

1. REPORT DATE *(DD-MM-YYYY)*	2. REPORT TYPE	3. DATES COVERED (From - To)
September 2013	Final	

4. TITLE AND SUBTITLE
Monolithic Microwave Integrated Circuit (MMIC) Frequency Doublers–2nd Pass Correction

5a. CONTRACT NUMBER

5b. GRANT NUMBER

5c. PROGRAM ELEMENT NUMBER

6. AUTHOR(S)
John E. Penn

5d. PROJECT NUMBER

5e. TASK NUMBER

5f. WORK UNIT NUMBER

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
U.S. Army Research Laboratory
ATTN: RDRL-SER-E
2800 Powder Mill Road
Adelphi, MD 20783-1197

8. PERFORMING ORGANIZATION REPORT NUMBER
ARL-TN-0580

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)

10. SPONSOR/MONITOR'S ACRONYM(S)

11. SPONSOR/MONITOR'S REPORT NUMBER(S)

12. DISTRIBUTION/AVAILABILITY STATEMENT
Approved for public release; distribution unlimited.

13. SUPPLEMENTARY NOTES

14. ABSTRACT
Frequency multiplier microwave monolithic integrated circuits (MMICs) can be used for a variety of radio frequency (RF) and microwave systems. Several frequency doublers were designed using a 0.13-µm gallium arsenide (GaAs) pseudomorphic high electron mobility transistor (PHEMT) process from TriQuint Semiconductor. The original design and fabrication of these circuits was performed as part of the fall 2011 Johns Hopkins University (JHU) MMIC Design Course, taught by the author. As noted in the previous technical note, ARL-TN-0517, *Monolithic Microwave Integrated Circuit (MMIC) Frequency Doublers*, the measured results for the open circuit stub to attenuate the fundamental harmonic indicated that an electromagnetic (EM) simulator, such as Sonnet EM, more accurately modeled the performance compared to a standard microwave linear simulator. The length of the stub attenuators were corrected and refabricated as part of the fall 2012 JHU MMIC Design Course. The measurements of the second pass 8- and 16-GHz frequency doublers with harmonic stubs are documented in this follow up technical note.

15. SUBJECT TERMS
GaAs, MMIC, frequency doubler

16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT	18. NUMBER OF PAGES	19a. NAME OF RESPONSIBLE PERSON
a. REPORT	b. ABSTRACT	c. THIS PAGE			John E. Penn
Unclassified	Unclassified	Unclassified	UU	16	19b. TELEPHONE NUMBER (*Include area code*) (301) 394-0423

Contents

List of Figures iv

List of Tables iv

Acknowledgments v

1. Introduction 1

2. Frequency Doubler at 8 GHz with a Fundamental Harmonic Stub Attenuator 1

3. Frequency Doubler at 16 GHz with a Fundamental Harmonic Stub Attenuator 4

4. Conclusion 6

5. References 7

Distribution List 8

List of Figures

Figure 1. S-parameters of the 8-GHz doubler (measured-solid, re-simulations-dotted). 2

Figure 2. The 8-GHz doubler 2nd harmonic output vs. input power at 8 GHz (measured-solid, re-simulations-dotted). 2

Figure 3. Layout plot of the 8-GHz frequency doubler second pass 2012 (~0.65 x 1.2 mm). 3

Figure 4. S-parameters of the 16-GHz doubler (measured-solid, re-simulations-dotted). 4

Figure 5. The 16-GHz doubler 2nd harmonic output vs. input power at 17 GHz (measured-solid, re-simulations-dotted) 5

Figure 6. Layout plot of the 16-GHz frequency doubler second pass 2012 (~0.6 x 0.8 mm). 6

List of Tables

Table 1. Measured performance of the 8-GHz doubler (second pass 2012). 3

Table 2. Measured performance of the 16-GHz doubler (second pass 2012). 5

Acknowledgments

I would like to acknowledge the U.S. Army Research Laboratory (ARL) in supporting my part-time passion of teaching the Johns Hopkins University (JHU) Monolithic Microwave Integrated Circuits (MMIC) Design Course, as well as TriQuint Semiconductor for fabricating designs for JHU students since 1989. Software support for these JHU designs is provided by Applied Wave Research (AWR), Agilent, Inc., and Sonnet Software.

INTENTIONALLY LEFT BLANK.

1. Introduction

Frequency multiplier microwave monolithic integrated circuits (MMICs) can be used for a variety of radio frequency (RF) and microwave systems. Three frequency doubler circuits were designed and fabricated using a 0.13-µm gallium arsenide (GaAs) pseudomorphic high electron mobility transistor (PHEMT) process from TriQuint Semiconductor. The fabrication was performed as part of the fall 2011 Johns Hopkins University (JHU) MMIC Design Course, taught by the author. As noted in the previous technical note, ARL-TN-0517, *Monolithic Microwave Integrated Circuit (MMIC) Frequency Doublers* (*1*), the measured results of the original designs were shifted in frequency. This shift was due to errors in modeling the open circuit stubs, which attenuate the fundamental harmonic input. An electromagnetic (EM) simulator, such as Sonnet EM, more accurately models the performance compared to the standard analytical microstrip models used in linear simulators. The length of the stub attenuators was corrected and the modified designs were refabricated as part of the fall 2012 JHU MMIC Design Course. The measurements of the second pass 8- and 16-GHz frequency doublers with harmonic stubs are documented in this follow up technical note.

2. Frequency Doubler at 8 GHz with a Fundamental Harmonic Stub Attenuator

A harmonic stub was added to attenuate the fundamental input frequency, but was shifted up in frequency in the first pass design. The measured second pass "corrected" design versus EM stub re-simulations show good agreement (figure 1). Figure 2 shows the measured performance of the second harmonic versus input power level at 8 GHz, showing good agreement with the nonlinear re-simulations. Table 1 shows the measurements of the doubler with about a 6-dB conversion loss from fundamental input power level to 2^{nd} harmonic output power at drive levels of 8 to 12 dBm with attenuation of the fundamental output below the 2^{nd} harmonic output. Additional filtering of these doublers could be added externally or in a future redesign. Figure 3 shows the actual layout of the second pass 2012 design with the only change being the longer meandered stub attenuator.

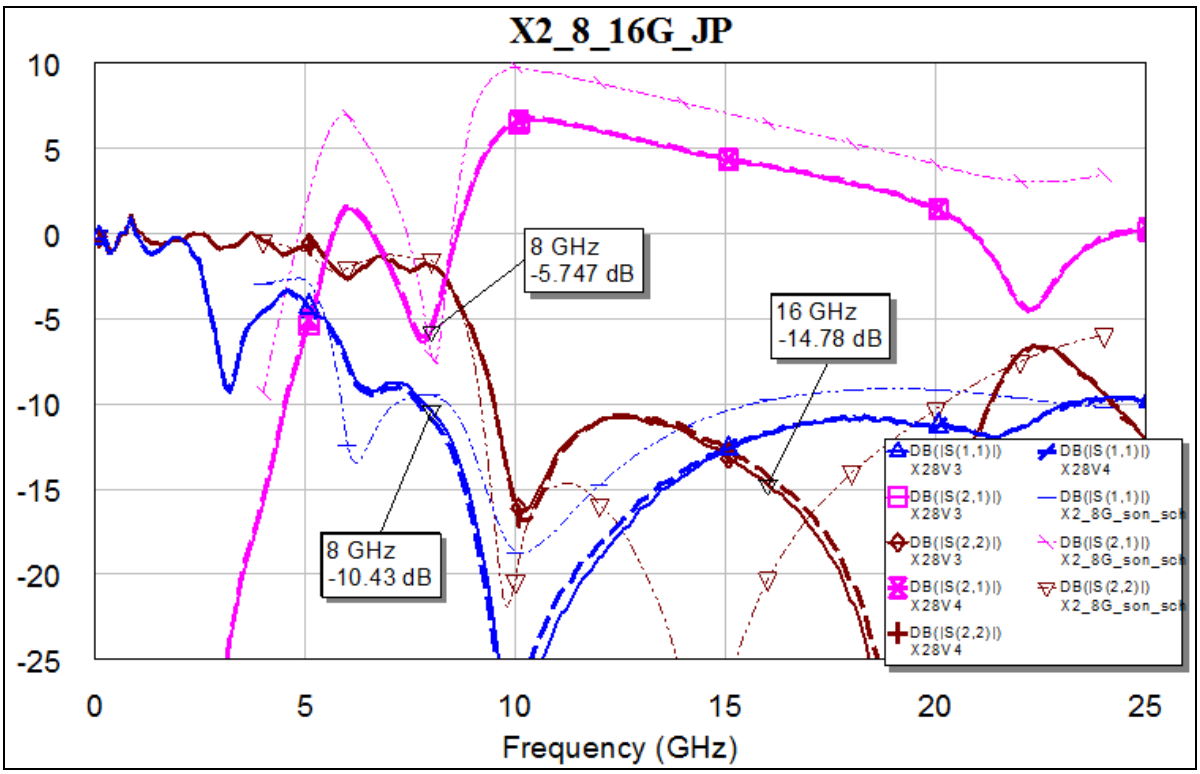

Figure 1. S-parameters of the 8-GHz doubler (measured-solid, re-simulations-dotted).

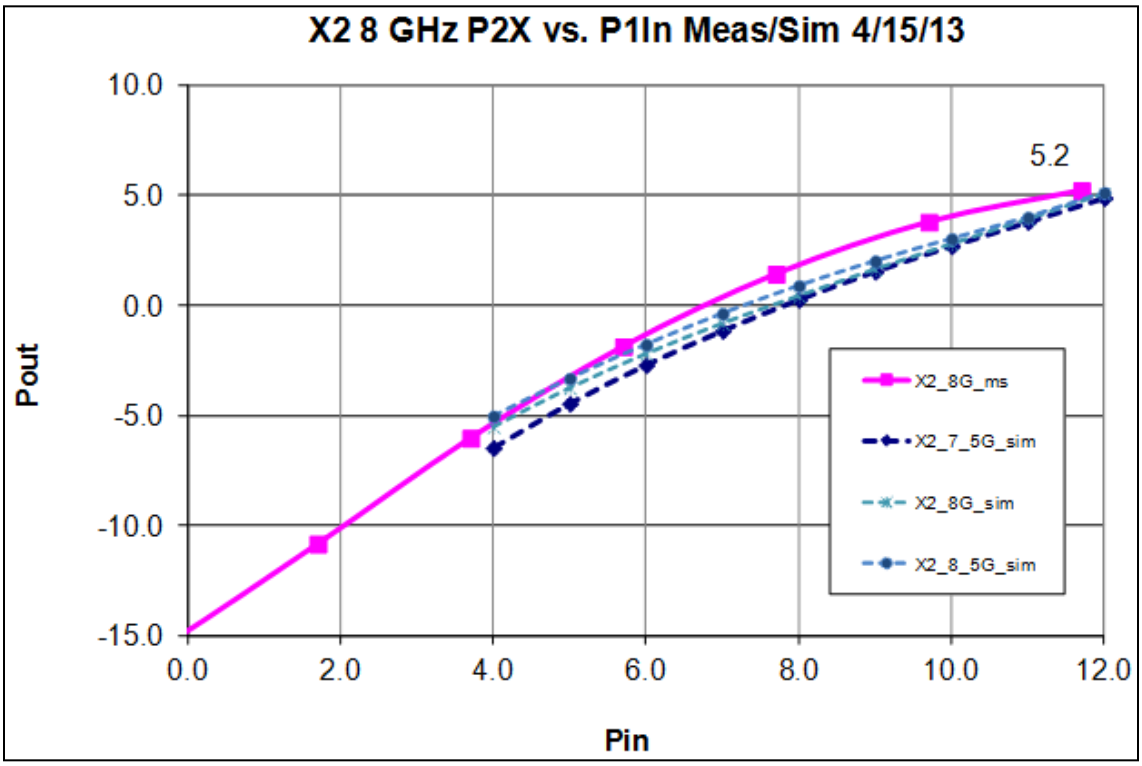

Figure 2. The 8-GHz doubler 2nd harmonic output vs. input power at 8 GHz (measured-solid, re-simulations-dotted).

Table 1. Measured performance of the 8-GHz doubler (second pass 2012).

Doubler 8G		4V at 39mA, vg=-1.5v			Die #1	7.8GHz		
SG	Pin(corr)	Pout8G(m	Pout16G(ms	Pout24G(ms	Pout(corr)	Pout2X(corr)	Pout3X(corr)	Cnvloss
-4.0	**-6.3**	-14.3	-30.9		**-12.3**	**-27.9**		21.6
-2.0	**-4.3**	-12.4	-27.0		**-10.4**	**-24.0**		19.7
0.0	**-2.3**	-10.4	-22.7		**-8.4**	**-19.7**		17.4
2.0	**-0.3**	-8.5	-18.4		**-6.5**	**-15.4**		15.1
4.0	**1.7**	-6.6	-13.8	-33.2	**-4.6**	**-10.8**	**-28.7**	12.5
6.0	**3.7**	-4.9	-9.0	-24.8	**-2.9**	**-6.0**	**-20.3**	9.7
8.0	**5.7**	-3.4	-4.8	-18.7	**-1.4**	**-1.8**	**-14.2**	7.5
10.0	**7.7**	-1.9	-1.6	-14.3	**0.2**	**1.5**	**-9.8**	6.3
12.0	**9.7**	-0.5	0.8	-10.2	**1.5**	**3.8**	**-5.7**	5.9
14.0	**11.7**	0.6	2.2	-6.8	**2.6**	**5.2**	**-2.3**	6.5

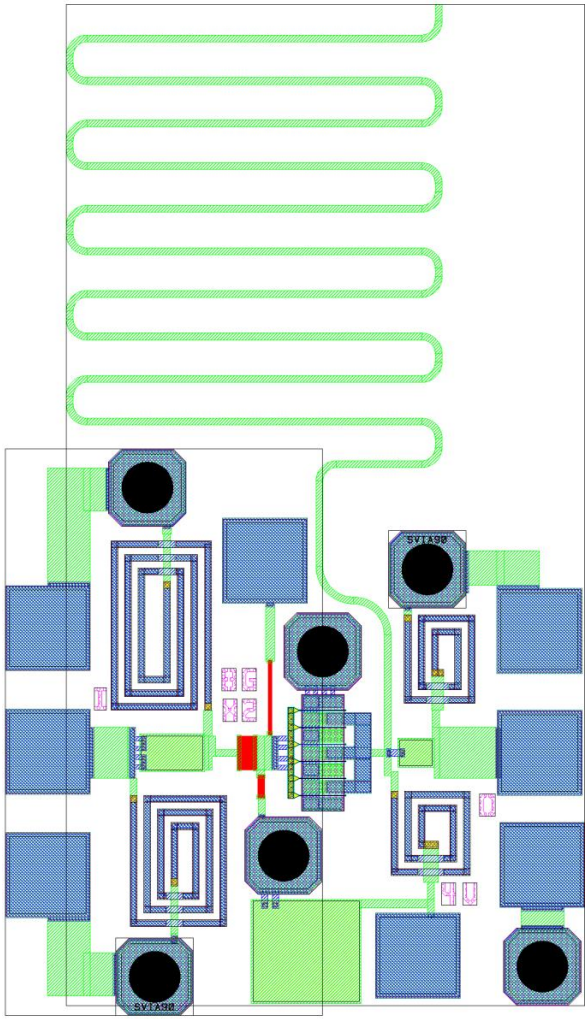

Figure 3. Layout plot of the 8-GHz frequency doubler second pass 2012 (~0.65 x 1.2 mm).

3. Frequency Doubler at 16 GHz with a Fundamental Harmonic Stub Attenuator

A harmonic stub was added to attenuate the fundamental input frequency, but was off in frequency in the first pass design of the 8- and 16-GHz doublers. The measured versus EM stub re-simulations show good agreement for the 16-GHz doubler (figure 4). Figure 5 shows the measured performance of the 2nd harmonic output versus fundamental input power level at 17 GHz, showing fairly good agreement with the nonlinear re-simulations, especially at higher input drive levels. Table 2 shows the measurements of the doubler showing about a 12-dB conversion loss from fundamental power level to 2nd harmonic output power at drive levels of 10 to 14 dBm. Even with a stub attenuator, the fundamental output power is still slightly higher than the 2nd harmonic. Additional filtering of these doublers could be added externally or in a future redesign. Figure 6 shows the actual layout of the second pass 2012 design with the only change being the longer meandered stub attenuator.

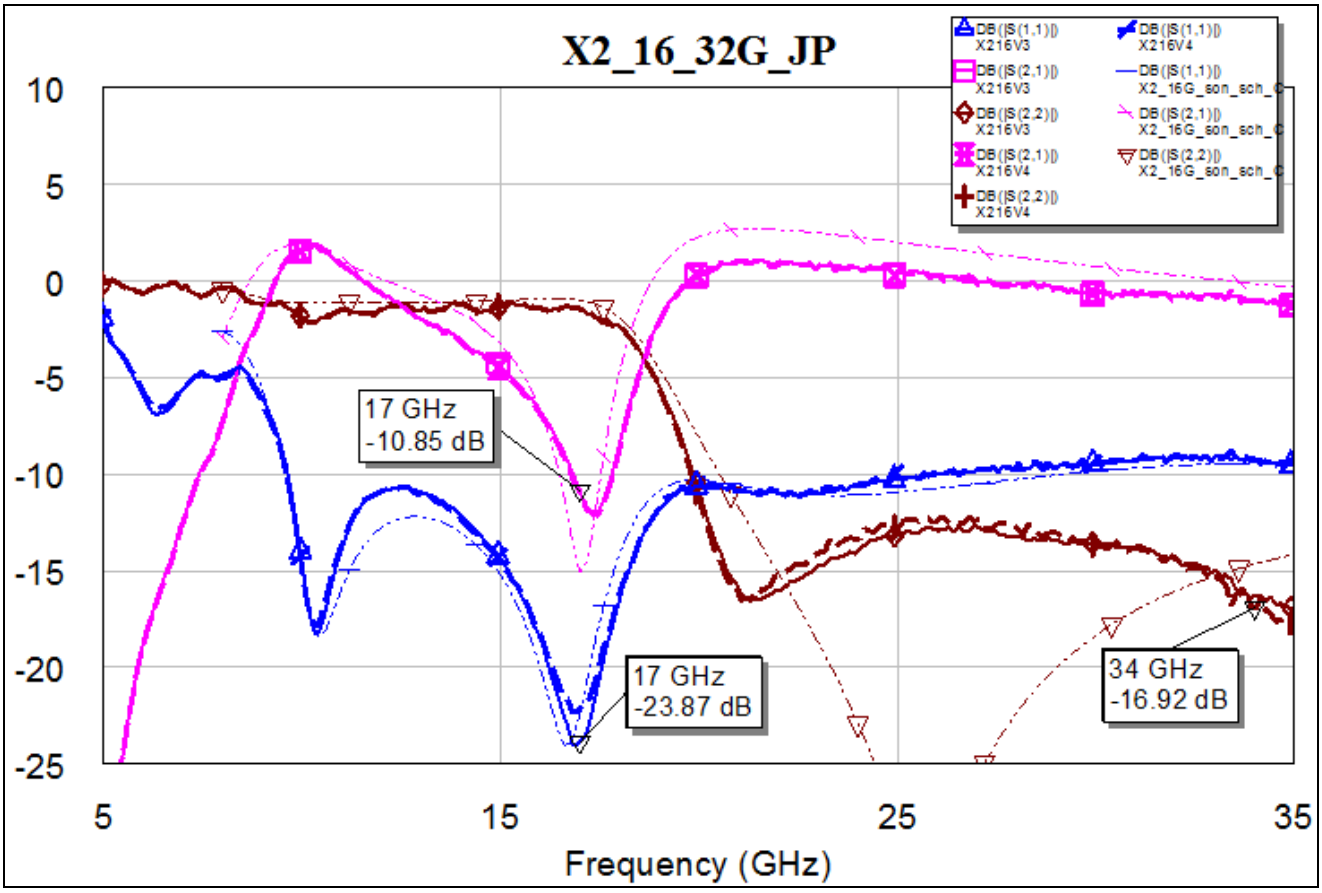

Figure 4. S-parameters of the 16-GHz doubler (measured-solid, re-simulations-dotted).

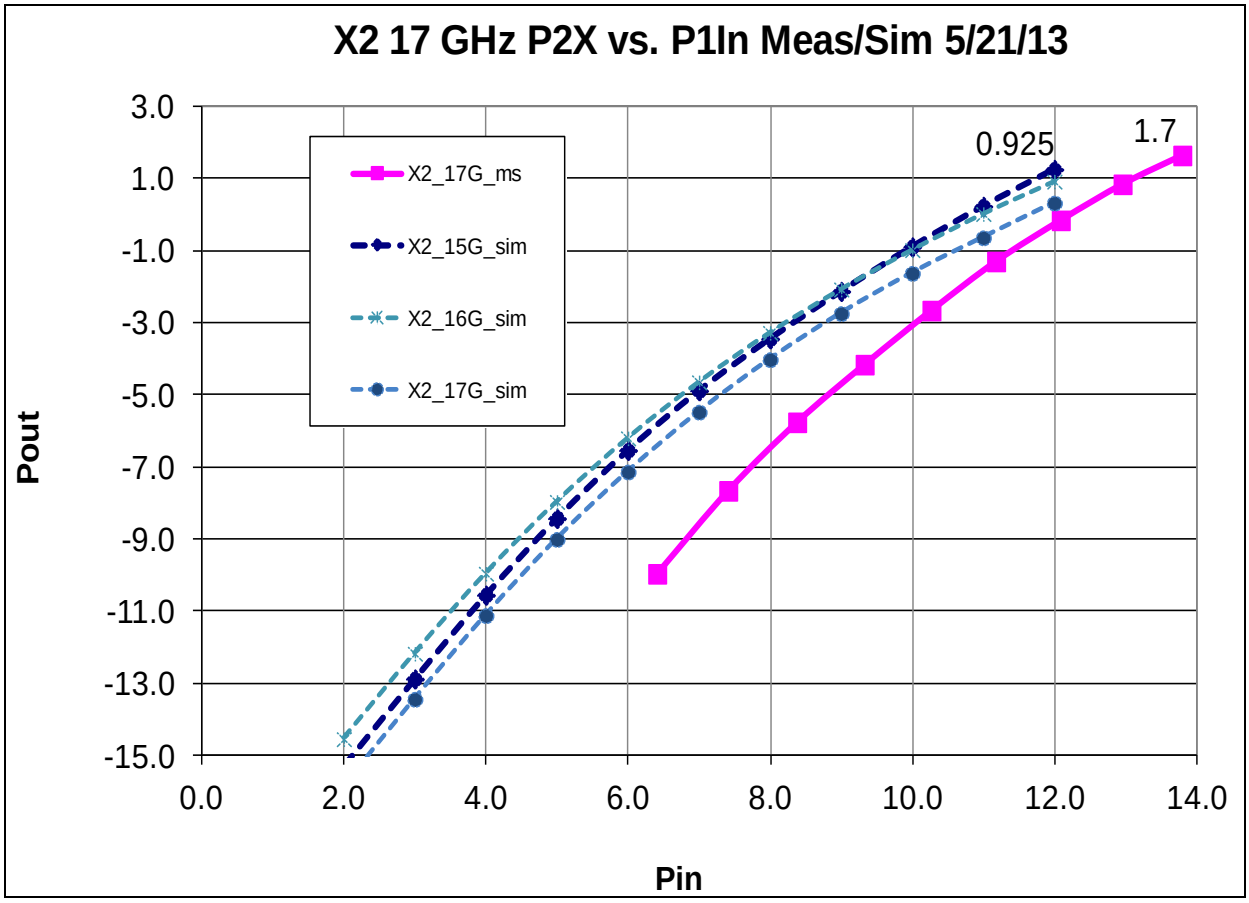

Figure 5. The 16-GHz doubler 2nd harmonic output vs. input power at 17 GHz (measured-solid, re-simulations-dotted)

Table 2. Measured performance of the 16-GHz doubler (second pass 2012).

5/21/2013		17.0 GHz						
Doubler 16G		4V at ~34mA, vg=-3v			Die #2			
Pin(SG)	Pin(A)	PoutX1(m	PoutX2(r	Pout(corr)	Pout2X(cc	Cnvloss	dBc	I(4V)
-8.00	**6.4**	-8.08	-17.00	**-2.4**	**-10.0**	16.4	7.6	40.3
-7.00	**7.4**	-7.11	-14.70	**-1.4**	**-7.7**	15.1	6.3	43.8
-6.00	**8.4**	-6.22	-12.80	**-0.5**	**-5.8**	14.1	5.2	47.7
-5.00	**9.3**	-5.32	-11.20	**0.4**	**-4.2**	13.5	4.5	52.2
-4.00	**10.3**	-4.44	-9.70	**1.3**	**-2.7**	12.9	3.9	57.0
-3.00	**11.2**	-3.60	-8.34	**2.1**	**-1.3**	**12.5**	3.4	62.2
-2.00	**12.1**	-2.81	-7.20	**2.9**	**-0.2**	**12.2**	3.1	67.5
-1.00	**13.0**	-2.07	-6.20	**3.6**	**0.9**	**12.1**	2.8	72.8
0.00	**13.8**	-1.42	-5.40	**4.3**	**1.7**	**12.2**	2.6	77.8

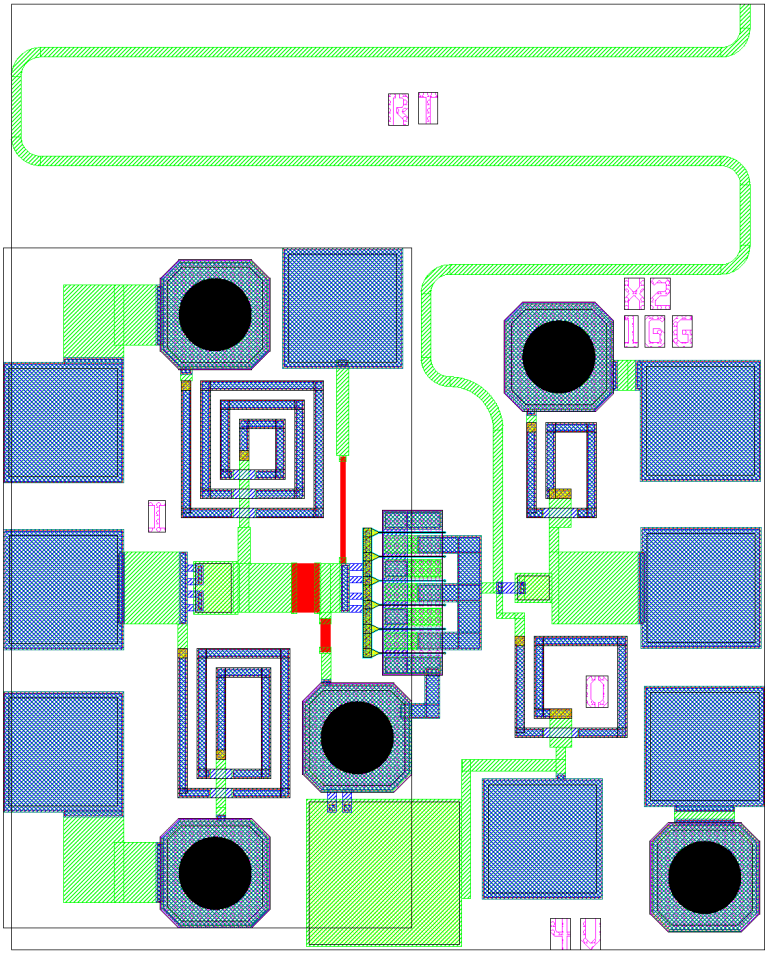

Figure 6. Layout plot of the 16-GHz frequency doubler second pass 2012 (~0.6 x 0.8 mm).

4. Conclusion

These frequency doubler circuits worked well and compared well with the original simulations, after adjusting for the significantly different simulations of the meandered open circuit stub attenuator between the linear simulator and the Sonnet EM simulations of the physical layout. Based on the previous first pass designs documented in the reference 1 and 2, the stub attenuator lengths were lengthened to retune the designs to the desired operating frequency. Otherwise, both 2012 frequency doublers were identical to the original 2011 designs. Particularly for higher frequency designs and dense MMIC layouts, an EM simulator, such as Sonnet, may be needed to more accurately predict actual layout parastics.

5. References

1. Penn, J. *Monolithic Microwave Integrated Circuit (MMIC) Frequency Doublers*; ARL-TN-0517; U.S. Army Research Laboratory: Adelphi, MD, December 2012.

2. Penn, J. MMIC Frequency Doublers. *High Frequency Electronics* **February 2013**.

1 DEFENSE TECHNICAL
(PDF) INFORMATION CTR
DTIC OCA

2 DIRECTOR
(PDFS) US ARMY RESEARCH LAB
RDRL CIO LL
IMAL HRA MAIL & RECORDS MGMT

1 GOVT PRINTG OFC
(PDF) A MALHOTRA

4 DIRECTOR
(PDFS) US ARMY RESEARCH LAB
4 RDRL SER
(HCS) PAUL AMIRTHARAJ (PDF)
RDRL SER E
ROMEO DEL ROSARIO (1 HC)
JAMES WILSON (PDF)
JOHN PENN (3 HCS)
ROBERT PROIE (PDF)
ED VIVEIROS (PDF)
2800 POWDER MILL RD
ADELPHI MD 20783-1197
RDRL SER E