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THESIS

SYNTHETIC SPACE VECTOR MODULATION

by

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June 2013

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13. ABSTRACT (maximum 200 words)

Alternating current motors are used throughout the fleet because of their rugged construction and nearly maintenance free operation. Since the U.S. Navy is exploring and acting on the possibilities of DC distribution systems, the need exists for simple, reliable three-phase voltage source inverter (VSI) powered induction machines. Until recently, VSIs utilized a pulse width modulation (PWM) scheme controlling the frequency and amplitude of each phase. A novel and simple hardware centered VSI controller was designed, simulated, built and tested featuring a type of space vector modulation (SVM). Design criteria evaluated such as VSI frequency response, switching losses, dead-time and SVM switching sequences were considered. Specifically, modulo-6 and 12 synthetic SVM units were evaluated for future Department of Defense use.

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SYNTHETIC SPACE VECTOR MODULATION

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ABSTRACT

Alternating current motors are used throughout the fleet because of their rugged construction and nearly maintenance free operation. Since the U.S. Navy is exploring and acting on the possibilities of DC distribution systems, the need exists for simple, reliable three-phase voltage source inverter (VSI) powered induction machines. Until recently, VSIs utilized a pulse width modulation (PWM) scheme controlling the frequency and amplitude of each phase. A novel and simple hardware centered VSI controller was designed, simulated, built and tested featuring a type of space vector modulation (SVM). Design criteria evaluated such as VSI frequency response, switching losses, dead-time and SVM switching sequences were considered. Specifically, modulo-6 and 12 synthetic SVM units were evaluated for future Department of Defense use.

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LIST OF ABBREVIATIONS AND ACRONYMS

AC   Alternating Current
Alt-Rev   Alternating-Reversing

CAD   Computed Aided Design
CPU   Central Processing Unit

DC   Direct Current
DoD   Department of Defense
DSP   Digital Signal Processer

FPGA   Field Programmable Gate Array

Mod-6   Modulo-6
Mod-12   Modulo-12
Mux   Multiplexer

PWM   Pulse Width Modulation

RF   Radio Frequency

SVM   Space Vector Modulation

VCO   Voltage Controlled Oscillator
VSI   Voltage Source Inverter

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EXECUTIVE SUMMARY

Alternating current motors are used throughout the fleet because of their rugged construction and nearly maintenance free operation. Since the U.S. Navy is exploring and acting on the possibilities of DC distribution systems, the need exists for simple, reliable three-phase voltage source inverter (VSI) powered induction machines. Until recently, VSIs utilized a pulse width modulation (PWM) scheme controlling the frequency and amplitude of each phase. A novel and simple hardware centered VSI controller was designed, simulated, built and tested featuring a type of space vector modulation (SVM). Design criteria evaluated such as VSI frequency response, switching losses, dead-time and SVM switching sequences were considered. Specifically, modulo-6 and 12 synthetic SVM units were evaluated for future Department of Defense (DoD) usage.

Direct current machines are known for variable speed and torque operations. Direct current machines can operate with reliable DC power supplies especially batteries without fancy controls. Inherently, DC machine commutation is environmentally sensitive and maintenance intensive at well as electrically noisy (audible and RF). However, the AC machine's basic construction is much simpler and consequently more reliable. It can operate in caustic environments and requires little maintenance. The problem with the AC machine is providing a reliable power source for variable speed and torque operations. The goal of this thesis is to mitigate some of the disadvantages of sourcing an ac machine by utilizing a DC supplied VSI.

Because of the inherent hardware-only design of the synthetic SVM unit, it is believed that certain desirable benefits will be derived. Many of the benefits listed below are a direct result of the fact that the hardware does not require a CPU, FPGA or software.

(1)   Reliability: Although not provable, the simplicity of the logic based hardware should be more reliable than a software based system.

(2)   Cost: Without a CPU, FPGA or software, the cost is dramatically reduced from a conventional SVM unit.

(3)   Maintenance: Other than potentially cleaning cooling fins, there is little to maintain. There is no software upgrade required, since there is no software.

(4)   Expandability: As seen with the hardware and modeling effort, the synthetic SVM methodology can be expanded from mod-6 to mod-N where N is an even integer.

After construction of modulo-6 and 12 units, testing results correlated closely with simulation results. As expected, the higher modulo number designs exhibited waveforms with less harmonic content.

ACKNOWLEDGMENTS

My wife, colleagues and coworkers put up with me while I stumbled through the hours and weeks of deadlines and rewrites. Some of the best insights came from their admonitions such as, "seek profound simplicity" and "the best information is 'up to the minute' yet timeless."

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I.   INTRODUCTION AND OVERVIEW

Modern mobile electronics depend on switching power supplies and the U.S. Navy is capitalizing on this technology. The advancement in power supplies has enabled the practicality of replacing many direct current (DC) machines with three-phase alternating current (AC) machines, as AC machines generally require more complicated electronics. This replacement of DC machines requires the following components: (1) a three-phase motor, (2) a voltage source inverter (VSI) and (3) an inverter controller. The VSI controller has traditionally been operated by hardwired pulse-width modulation (PWM) or the use of a programmable microprocessor system. Both hardware and software approaches to implementing PWM depend on a saw-tooth waveform carrier with a significantly higher frequency than the fundamental waveform the VSI is producing for the ac machine. For instance, the triangle wave used to create PWM signals may have a frequency of 5 kHz while the fundamental may be 60 Hz. The interaction between the high and low frequency waveforms produces gating signals for the VSI. In other words, the VSI is used as a high power digitizer. The output voltage is a chopped representation of the low frequency fundamental and must be filtered prior to (or by) the machine. Any ripple in the voltage will be seen as torque pulsations in the motor. As the switching (or carrier) frequency increases with respect to the machine's mechanical time-constant, the torque pulsations are minimized. Unfortunately, high switching frequencies produce higher switching losses, which increase linearly with frequency.

This same concern for minimizing switch stress has been seen in digital electronics and gave rise to the "Gray code" as a switch minimization strategy.   The power field has benefited by digital strategies like the Gray code and this thesis intends to capitalize on known switch stress minimization methods. Before we can discuss the VSI further, consider the six-switch (transistor) schematic in Figure 1. Each of the three transistor pairs can be gated via the outputs of three clocked (synchronized) flip-flops where Q gates the upper transistor and Q' gates the lower. If the VSI's transistor pairs are considered digital switches, it can be observed that they have six useful states and two

"zero" states, which will be discussed later. Assuming the VSI switches are characterized as part of a digital system, it is reasonable to expect them to transition from one state to the next following a Gray sequence (as opposed to a binary sequence) in order to minimize switching events. Currently, proponents of digital strategies such as space-vector modulation (SVM) frequently claim that their systems allow only one (VSI) switch transition per clock cycle. Whether acknowledged or not, this behavior is a type of Gray coding.
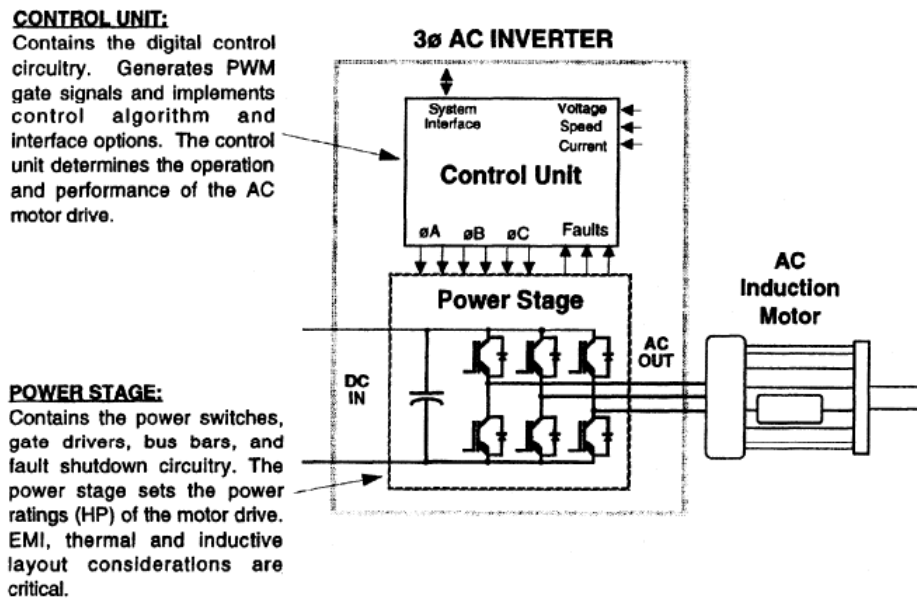
Figure 1.   Control unit, VSI power stage and AC induction motor. From [1].

Traditionally, PWM units employed "edge-aligned" saw-tooth signals as opposed to "center-aligned" because they were easier to develop. Unfortunately, edge-aligned saw-tooth carriers produce multiple transitions during each switching event. This was replaced by center-aligned saw-tooth (or triangle waves) signals for digitizing, which produces center-aligned pulse-trains and only one switch state change per cycle. It is interesting to note, that center-aligned sine-PWM can be made to mimic SVM control. In fact, an experimental unit was tested comparing the two control strategies, revealing that the upstream and downstream equipment behaved identically with either control. What

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was discovered was a dramatic reduction in the effort required to make an SVM enabled VSI controller by using certain types of sine-PWM hardware.

Since procuring some of the reading materials for this thesis, it has been further uncovered that SVM switching signals can be mimicked by multiplexing center-aligned pulse trains forming a synthetic SVM. Ultimately, the developed electronics and simulation work from this thesis means that an SVM-like VSI controller no longer requires special hardware or software. The U.S. Navy, or anyone, now has a solution for the replacement of complex control hardware and software with a low cost VSI controller for DC to AC power conversion. Further, the synthetic SVM scheme envisioned in this thesis produces a digital stream where the carrier frequency is always the same fixed integer multiple greater than the fundamental frequency. The primary difference between SVM and synthetic SVM is the implementation strategy of software versus inexpensive hardware, respectively.

A.   VSIS INTRODUCE SWITCHING SPEED LIMITS

When replacing DC motors with three-phase AC motors, a power stage or VSI is usually included at each motor's location. This VSI converts the available DC into variable speed, three-phase AC via PWM or SVM signals fed to it from a VSI controller unit. Presently, most VSI controller units do two things: (1) house a feedback algorithm, producing commanded parameters, and (2) operate on those parameters to producing VSI gating signals.

A control algorithm produces commanded voltage and frequency from monitored signals such as rotor speed and current. Once desired voltage and frequency are determined, the synthetic SVM hardware produces the proper gating signals for the VSI.

For its part, the three-phase power stage (or VSI) of Figure 1 can be thought of as three separate push-pull driver stages with each pair driven by logical input signals such that the upper transistor-switch is driven by the lower switch's logical inverse. Each pair is usually driven independently of the other two by way of a PWM scheme as illustrated in Figure 2 and in [1]. The independence of the three PWM circuits might be unsettling, but the modulating signals are almost always uniform in (1) shape, (2) frequency,

(3) amplitude and (4) phase-delay (120 degrees out of phase with each other). As shown in Figure 2, there is usually a common triangle signal for all three phases that produce the PMW signals.
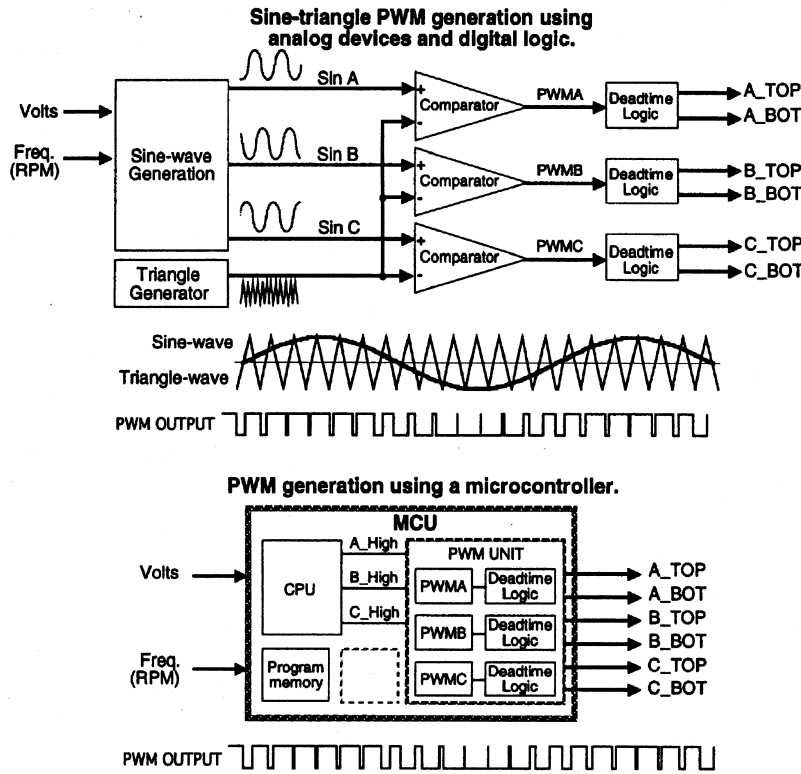
Figure 2.   PWM generation methods. From [1].

Pulse width modulation is a waveform digitization scheme whereby, once digitized, the waveform is amplified and reconstructed at the point of application via filtering. Without a digitization scheme, the amplification would be performed linearly and losses would be exorbitant. Pulse width modulation signals may be constructed using analog or digital methods, as depicted in Figure 2, but the exact reconstruction of the original waveform is dependent on the sawtooth's frequency being several times higher than the modulation signal's frequency; however, for power electronics devices higher switching frequencies result in higher switching losses as detailed in [2] and [3].

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Before SVM was developed, PWM was routinely used. As stated before, an accurately reproduced sine wave depends on a high frequency triangle wave. The switch losses, depicted in Figure 3, are dependent on frequency, and are described by:

$$P_{sw} = f_{sw}(W_{c(on)} + W_{c(off)}) \tag{1}$$

where P_{sw} is switching power loss in watts, f_{sw} is switching frequency in Hz , and $W_{c(on)}$ and $W_{c(off)}$ are turn-on and turn-off energy, respectively, in joules [2].
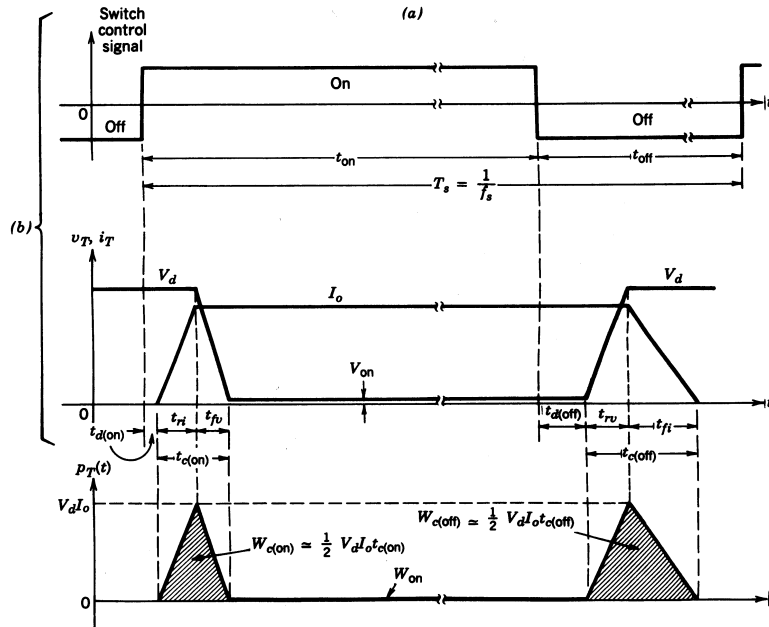
Figure 3.   Switching losses. From [2].

The 60-degree PWM method was developed as an answer to the enhanced switching losses higher frequencies engendered. The sixty degree PWM method method is a modification of the 3rd harmonic injection where the switch is held high (or low) for 60-degrees out of every half-cycle of the fundamental. This strategy clearly reduces P_{sw}. Even if the switches could be commanded to operate at a very high frequency, real transistors have a limited cycle speed depending on the technology and power levels [1], [2]. Further, it is obvious that the speed of the control algorithm is limited by the switching frequency and the switching frequency is limited by acceptable losses [4].

B.   THREE-PHASE AC INDUCTION VERSUS DC MACHINES

Direct current machines are known for variable speed and torque operations. Direct current machines can operate with reliable DC power supplies especially batteries without fancy controls. Inherently, DC machine commutation is environmentally sensitive and maintenance intensive at well as electrically noisy (audible and radio frequency (RF)). However, the AC machine's basic construction is much simpler and consequently more reliable. It can operate in caustic environments and requires little maintenance. The problem with the AC machine is providing a reliable power source for variable speed and torque operations. Table 1 was developed for this thesis as a short summary of the major features of DC and AC machines

Table 1.   DC machine versus AC induction machine.

	Advantages	Disadvantages
DC Machine	Simplistic Electrical Interface	Electrically Noisy
	Suitable for Battery Operation	Maintenance Issues
	Easily Controllable	Environmentally Sensitive
AC Induction	Rugged & Reliable	Source Dependent Speed
	Low Speed Torque	Load Dependent Speed
		High Starting Current

It is the goal of this thesis is to mitigate some of the disadvantages of sourcing an ac machine by utilizing a DC supplied VSI.

C. THIRD HARMONIC INJECTION

It is prudent in many higher voltage PWM inverters to maximize the amount of output voltage obtainable from the input DC bus. Maximizing output voltage generally improves efficiency and helps limit the required semiconductor blocking voltages. Over-modulation (a modulation index greater than one, $m > 1$) can be used to improve bus utilization for low pulse-count three-phase waveforms (i.e., three or nine pulses per half-cycle). It does not cause distortion in the output waveform until 'pinch-off' occurs. 'Pinch-off' occurs when $m > 1$ and the center pulse of each half-cycle touches (merges with) the adjacent pulses; subsequently, voltage control is lost. However, when high frequency (HF) PWM is used (greater than 100 pulses per half-cycle of the output fundamental), 'pinch-off' occurs as soon as the modulation index exceeds one, rendering over-modulation useless. As a note, over-modulation is more popular with low pulse-count single-phase inverters than poly-phase systems [5].

A more accepted and effective means of improving DC bus voltage (V_b) utilization in a three-phase system is third harmonic injection. In a floating wye-connected (or delta-connected) three-phase system, the third harmonic components cancel and only the fundamental appears. By examining the three composite pole templates in

$$
\begin{aligned}
v_a &= V_{a1}\sin\left(\omega t + 0°\right) &&+ \quad V_{a3}\sin 3\left(\omega t + 0°\right) \\
v_b &= V_{b1}\sin\left(\omega t - 120°\right) &&+ \quad V_{b3}\sin 3\left(\omega t - 120°\right) \\
v_c &= V_{c1}\sin\left(\omega t + 120°\right) &&+ \quad V_{c3}\sin 3\left(\omega t + 120°\right)
\end{aligned}
\tag{2}
$$

it is apparent that the subtraction of any two waveforms yields only the fundamental. However, the entire load is oscillating at the third harmonic with respect to the dc source. As long as there is no return path between the load and the source, the third harmonic will not be present in any of the output line-to-line or line-to-neutral voltages [5].

By overlaying the theoretical optimal $16.\overline{6}\%$ third harmonic on the fundamental, ~15.47% more fundamental output voltage can be produced with the same bus voltage (the theoretical maximum). Figure 4 contains two possible template waveforms ("sine" and "fundamental + third") with the same normalized peak value of 1.0. The black line

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represents a pure sine template while the red line represents a composite template with third harmonic. Both of these waveforms require the same normalized input dc bus voltage of 1.0, since they both have the same peak value. However, the optimal composite waveform (red) is the addition of the two blue waveforms where the peak value of the fundamental waveform is $V_{a1} = 2/\sqrt{3} \approx 1.1547$ and the peak value of the third harmonic waveform is $V_{a3} = V_{a1}/6$. Figure 4 demonstrates the ($\sim 15.47\%$) additional fundamental output voltage obtained with a ($16.\overline{6}\%$) third harmonic given the same normalized input dc bus voltage of 1.0. The theoretical maximum line-to-line output voltage possible given an input DC bus voltage (without third harmonic and with third harmonic, respectively), are given by

$$V_{ll-rms} = \frac{\sqrt{3}}{2\sqrt{2}}V_b \approx 0.61237V_b \qquad (3)$$

$$V_{ll-rms-3rd} = \frac{1}{\sqrt{2}}V_b \approx 1.15470(0.61237V_b) \approx 0.70711V_b \qquad (4)$$

It is interesting to note that optimal third harmonic injection of $V_{a3} = V_{a1}/6$ allows the bus to be utilized in a fashion identical to a single-phase H-bridge inverter [5].
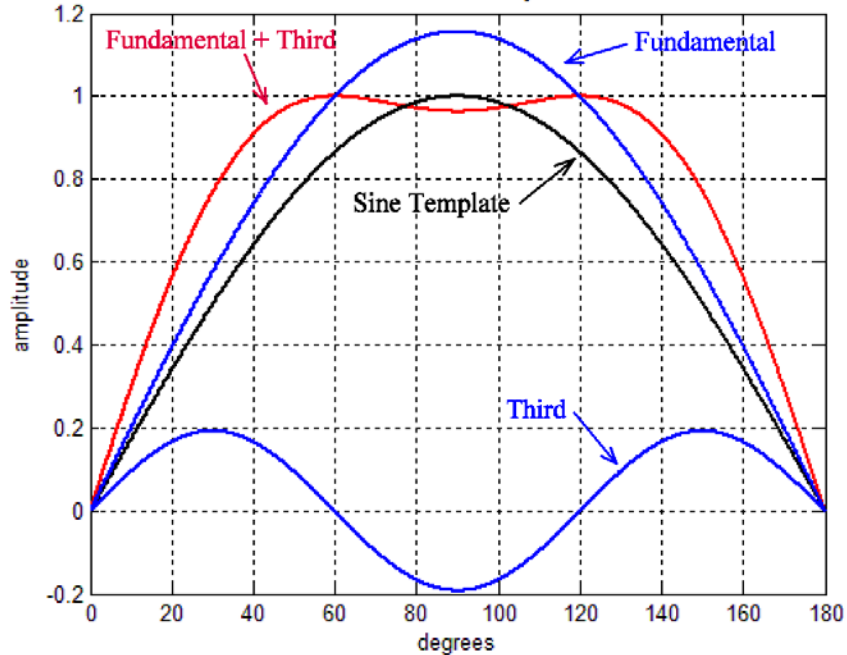
Figure 4.   Effect of third harmonic injection. From [5].

D.   SPACE VECTOR MODULATION

Until recently, SVM was mostly a software algorithm whereas PWM could be implemented in either in a hardware or software format. Detractors of SVM point out its numerically intense conversion process between polar and rectangular coordinates (fostering the growth of digital signal processors (DSPs) and field programmable gate array (FPGA) solutions) and the speed bottlenecks its use entails. Proponents of SVM point out the reduced switching stress the algorithm brings about as well as the ~15.47% downstream voltage improvement its use has over standard sine PWM.

Each of the three transistor pairs can be gated via the outputs of three clocked (synchronized) flip-flops where Q gates the upper transistor and Q' gates the lower. Furthermore, reduced switch operation in one leg frequently produces more simultaneous switching in the other legs with several switching sequences presented later in this paper illustrating the point. Not all types of SVM are equally qualified for switch stress reduction. The Gray code influence (only one switch changing state at a time) on the switching sequences seen in [1] and [6] are some of the hallmarks of SVM. It be should noted that the traditional SVM six member sequence surrounding most hex diagrams as

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seen in Figure 5 is important to the SVM software explanation and reproduced in the right-hand columns of Table 2 are both Gray code compliant. The right-hand columns of Table 2 can be produced using the Johnson counter sequence expressed in the left-hand column. Further, a more intricate observation reveals the inherent 120 degree phase shift between A, B and C.
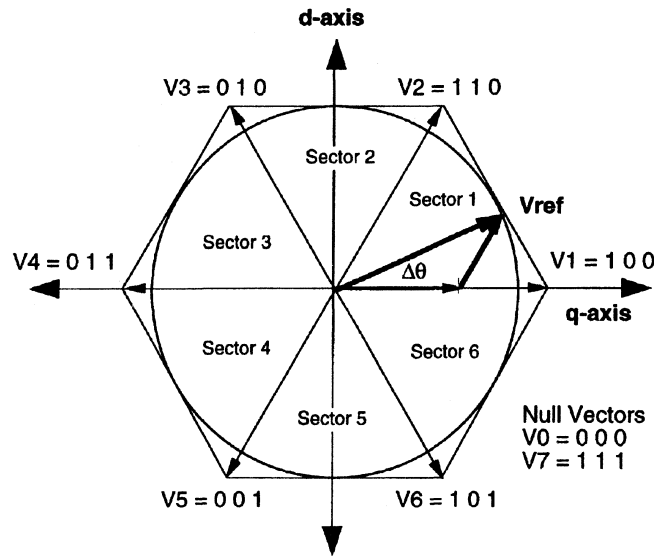
Figure 5.   Example of SVM hexagram for software coding. From [1].

Table 2.   A six state (modulo-6) counter sequence fed to the multiplexers.

Count_Sequence (Johnson Counter)			Gray_Code/120° phase sequence (180° "on", 180° "off" & 120° "out-of-phase")		
A	B	C	A	B'	C
0	0	0	0	1	0
1	0	0	1	1	0
1	1	0	1	0	0
1	1	1	1	0	1
0	1	1	0	0	1
0	0	1	0	1	1

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One of the switching waveforms presented later in this thesis is described as the Alternating-Reversing (Alt-Rev) switching sequence and the similarity in shape between its phase-to-neutral voltage waveform and the pre-encoded outline of a third harmonic injected phase-to-neutral voltage is striking. Because the voltage increase transmitted by way of SVM (over sine-PWM) is comparable to the voltage increase gained by using third harmonic injection PWM (over sine-PWM) one could easily recognize the assertion of [7] that the two are fundamentally the same. A typical three-phase wye-connected source is show in Figure 6 and can be used as a reference for phase-to-neutral and phase-to-phase voltages.
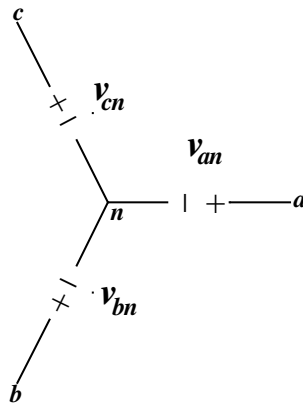
Figure 6.   Three-phase wye-connected source. From [5].

E.   SYNTHETIC SPACE VECTOR MODULATION

Space vector modulation can be reproduced using center-aligned pulse-trains on PWM equipment. The thesis will demonstrate synthetic-SVM, to be independent of software or PWM equipment. Since synthetic-SVM hardware produces the same behaviors in upstream and downstream equipment as authentic SVM equipment, it can be considered equivalent. Reference [7] simulated third harmonic injected PWM and SVM waveforms in Simulink. The results produced for third harmonic injected PWM so closely reproduced the results produced for SVM the researchers concluded the two voltage production methods were practically identical.

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As for my own examination of the Alt-Rev SVM sequence, the switching pattern was clearly reproducible by multiplexing three center-aligned pulse-trains. The electronics designed for this thesis began with (1) an oscillator at the desired frequency (six times the fundamental), (2) a center-aligned pulse train generator, (3) a modulo-6 counter and (4) a three-phase multiplexer using the counter's output for synchronization as shown in Figure 7. The counter reproduces the sequence found on the left side of Table 2 and shown in Figure 8. Given the above in conjunction with a VSI, there are other considerations for functionality of the system. First, in order to prevent shoot-through in a VSI switch leg, dead-time must exist between the turn-off of one switch and the turn-on of the other switch. Shoot-through occurs if both switches are simultaneously 'on' due to the characteristics of real switch operations. The shoot-through or short-circuit path is across the DC bus feeding the VSI. Second, in order to control the rotational speed of the load machine, the oscillator should have an adjustable frequency. Thirdly, in order to control the magnitude of the output voltage, the modulation index or pulse train width must be adjustable. Dead-time, frequency control and modulation index are addressed in separate sections of this thesis.
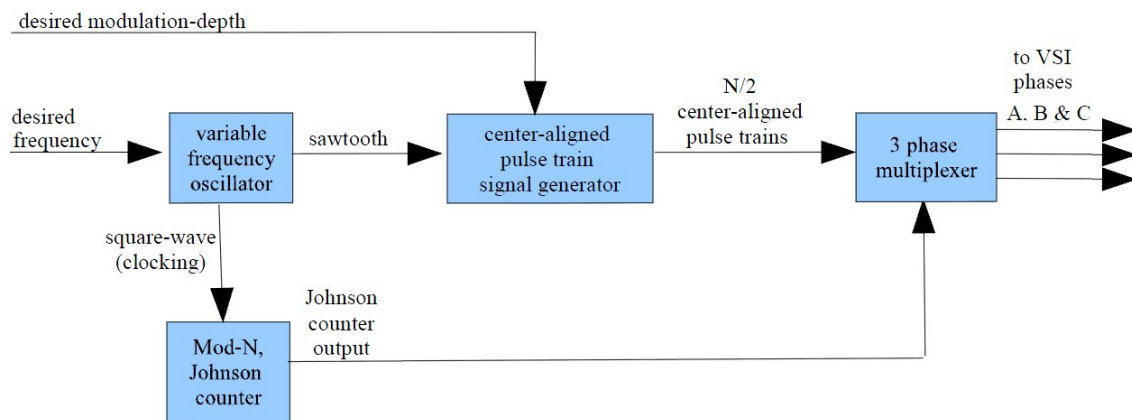
Figure 7.   Block diagram of thesis electronics.

The essentials of the first synthetic SVM unit are illustrated in Figure 7 with more detail in Appendix B-1 and B-2. The appendix contains the schematics for (1) a three

flip-flop modulo-6 counter designed in conjunction with (2) a variable frequency variable modulation-depth center-aligned pulse-train signal generator and (3) a three-phase multiplexer. The output of the pulse-train generator shown in Figure 9 and the output of the six state (modulus of six: mod-6) counter shown in Figure 8 are sent to a three-phase multiplexer (Appendix B-2) and each phase sent a signal the multiplexer produces both a signal and the signal's logical inverse. Both signals are then amplified, sent through a turn-on delay then sent through another amplifier (voltage follower) where it is made available to the VSI. Drawings are made available in Appendix B-2 for anyone wishing to confirm how this is done. The upper transistor gating signals for the VSI are 120 degrees out of phase with each other and sequenced to change state one switch at a time [8].
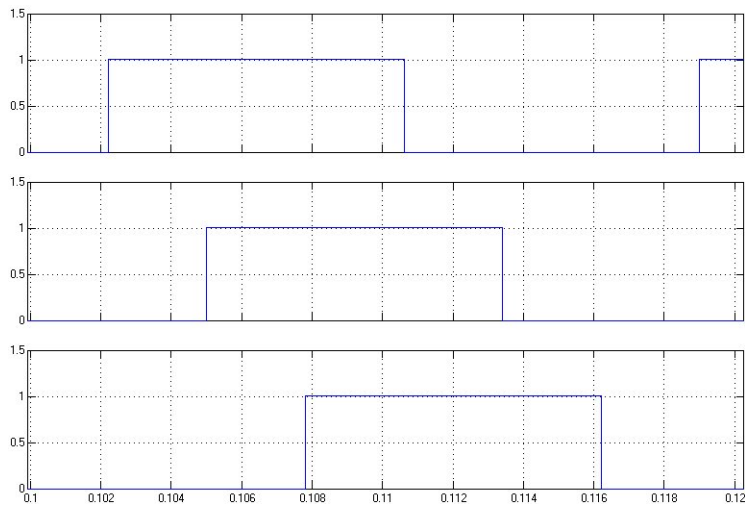
Figure 8.   Output of modulo-6 counter. From [5].
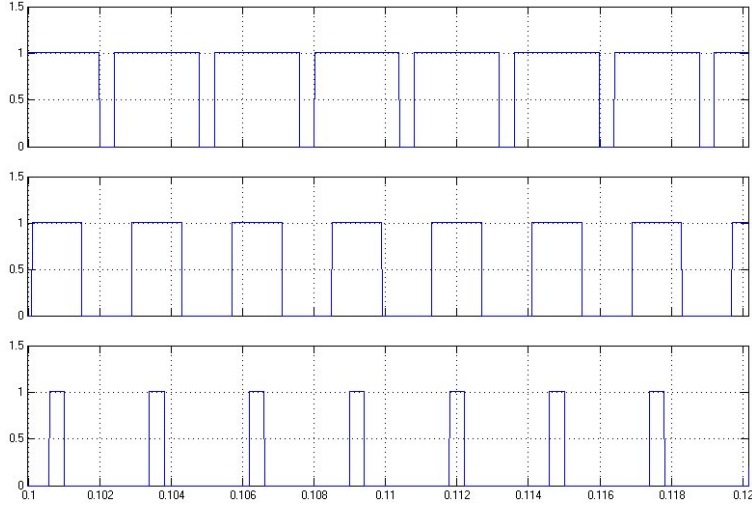
Figure 9.   Center aligned pulse trains. From [5].

In summary, the largest advantages of SVM over three-phase sine-PWM are reduced switching frequencies (resulting in lower switch stress) and a fifteen percent gain in the fundamental line-to-line voltage. The distinct advantages of the synthetic-SVM of this thesis are simplicity, cost, reliability and software independence. The mod-6 synthetic-SVM unit's printed circuit boards are populated with one clock, nine dual op-amps, five dual comparators, three multiplexers, four flip-flops, two low voltage regulator chips, several 7400 series logic ICs and some resistors and capacitors. There are no microcontrollers or FPGAs necessary to produce Alt-Rev SVM.

F.   DUAL OUTPUT VARIABLE FREQUENCY OSCILLATOR

After examining the literature, an NE566 voltage controlled oscillator (VCO) chip as seen in Figure 10 was used to design a circuit that produced the needed square-wave and triangle wave with capabilities from 150 Hz to 15 kHz. The square-wave clocks the mod-6 counter and the triangle wave is necessary for the production of the center-aligned pulse train.

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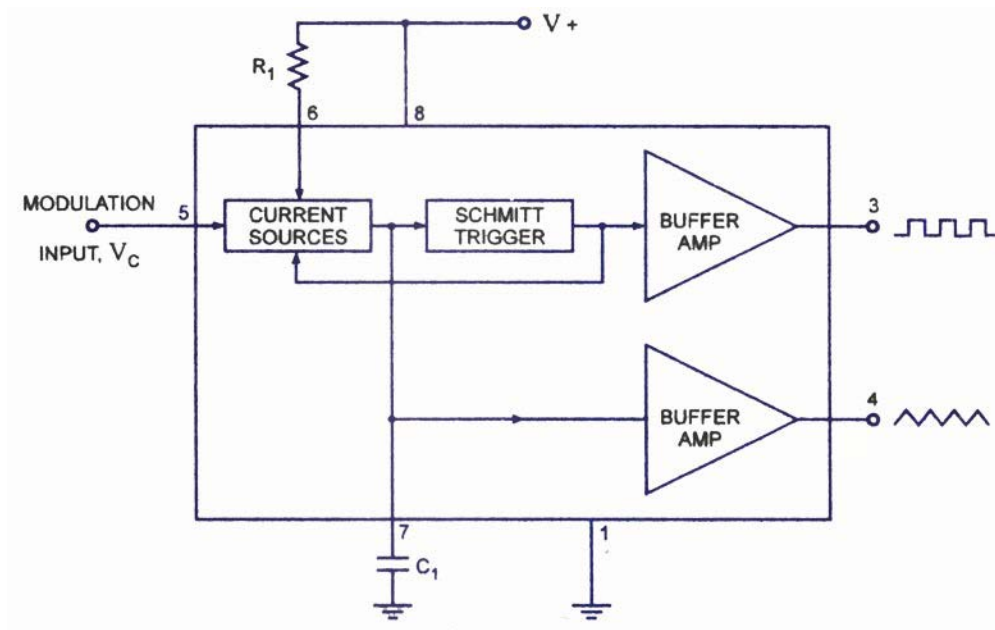
Figure 10.   NE566 Voltage Controlled Oscillator. From [9].

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II. BASIC CONCEPTS

A. SEQUENTIAL SYSTEMS AND COUNTERS

The significant parts of the synthetic SVM device are (1) an oscillator at the desired frequency, (2) a center-aligned pulse train generator, (3) a modulo-NN counter and (4) a three-phase multiplexer. This section will describe in part counters and in particular mod-6 and mod-12 counters.

A system is defined as a "sequential system" if the determination of the present outputs of the system requires knowledge of the system's previous outputs (or states). Alternatively, a "sequential system" is a system making use of memory such as a traffic light or a counter. A flip-flop may be considered the simplest memory system.

The synthetic SVM circuit demanded "time division" (not "frequency division") multiplexing, so electing to use the 74251s (as opposed to using other multiplexing methods) was rational. With frequency division, all signals are available simultaneously, but with time division multiplexing, signalss are available sequentially as selected. The system design envisioned feeding the digital multiplexer's "select" inputs from the mod-6 counter as seen in Figure 8. The other inputs to the multiplexer would come from the appropriate comparator-developed center-aligned pulse trains as seen in Figure 9. Since synthetic SVM mimics SVM, but not SVM's careful attention to field angles or its iconic Gray code hexagon, we can dispense with the use of of the hexagon. Further, it is not guaranteed that the counter will "wake-up" in a known state more than any other, so all states have to have a path into the main sequence (the counter has to be self-correcting).

1   Self-Correcting Counters via Transition State Mapping

Developing a counter usually proceeds in two or three steps as follows: (1) determine the number of required bits, (2) define the sequence of output numbers and (3) convert the signal descriptions into circuits. In the synthetic SVM system the counter has to produce equal length time segments and they have to be an equal number of steps up then down within one SVM cycle just as one would require a modulo-20 counter to multiplex ten pulses growing progressively wider and ten pulses becoming progressively

narrower for one complete cycle. With this in mind, we will now relate "transition state" mapping to the actual design of a modulo-N counter.

Table 3 with listed transitions is referred to after one has developed a Karnaugh map and wants to convert that map into equations.   Interest in this mapping technique has resurfaced recently and therefore we shall provide two examples of "transition state mapping" corresponding with the mod-6 and mod-12 synthetic SVM counters in this thesis. We shall use, as a first example, the modulo-6 counter (as found in Appendix B-1). It can be deduced that this counter requires only three bits and could be represented by the following mod-6 counter states listed under "Behavior" in Table 4.

Table 3.   Basic rules of "transition state mapping." From [10].

Flip-Flop Input	Must Include	Must Avoid	Redundant
S	α	0, β	1, X
R	β	1, α	0, X
J	α	0	1, β, X
K	β	1	0, α, X
D	1, α	0, β	X
T	α, β	0, 1	X

Note: X is "undefined" behavior.

Definitions of Symbols:

A	to	A'	is defined as	__	behavior
0	to	1	is defined as	α	behavior
1	to	0	is defined as	β	behavior
1	to	1	is defined as	1	behavior
0	to	0	is defined as	0	behavior

a.   *Mod-6 Counter*

The counter states referred to in Table 4 are those of a "Johnson (shift) counter" and because this kind of counter just "shifts" data from the output of one flip-flop to the next we only really have to concern ourselves with what flip-flop A is using as input therefore only the leftmost bits in column A require equations. The entries in column B come from those of column A and the entries of column C come from the entries in column B immediately preceding it, but for completeness the equations corresponding to the development of each flip-flop will be looked at.

Table 4.   Modulo-6 counter desired behavior.

Present State			Desired Next State			Behavior		
A	B	C	A'	B'	C'	A"	B"	C"
0	0	0	1	0	0	α	0	0
1	0	0	1	1	0	1	α	0
1	1	0	1	1	1	1	1	α
1	1	1	0	1	1	β	1	1
0	1	1	0	0	1	0	β	1
0	0	1	0	0	0	0	0	β

Three flip-flops are known to develop eight states and we've only developed six so we develop a table listing all the possible states three flip-flops can get into. Given a list of present states, what states can a Johnson counter move to in one clock "tick?" Since we can figure out what the B flip-flop will be, given the A flip-flop's current state, we really only have to concern ourselves with what sets or resets flip-flop A. We can put "X" in places where we are unsure what state A will be in and write it all down and what we have is Table 5. We only have two "X" states the designer of a self-correcting counter should avoid. The next step is to make Karnaugh maps from the columns of the "Behavior" matrix.

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Table 5.   This is the mod-6 counter's eight state desired behavior.

Present State			Desired Next State			Behavior		
A	B	C	A'	B'	C'	A"	B"	C"
0	0	0	1	0	0	α	0	0
0	0	1	0	0	0	0	0	β
0	1	0	x	0	1	x	β	α
0	1	1	0	0	1	0	β	1
1	0	0	1	1	0	1	α	0
1	0	1	x	1	0	x	α	β
1	1	0	1	1	1	1	1	α
1	1	1	0	1	1	β	1	1

Although "transition state mapping" rules for 'D', 'JK', 'T' or 'SR' flip-flops were considered, it was convenient to use the "JK" flip-flops because of their availability and wiring flexibility.

Under normal conditions the use of "undefined" states are "optional", but because self-correcting counters require care in their design, these normally "optional" states are going to be avoided. It also needs to be stated that the designations in the following Karnaugh maps "ρA," "ρB" and "ρC" are used to indicate the input sides of each flip-flop and all other references to "A," "B" and "C" refer to the output side of each flip-flop. Further, the logical inversion of A, B and C is designated as A', B' and C' where $A' = \overline{A}$, $B' = \overline{B}$ and $C' = \overline{C}$.

Referencing rules in Table 3 and avoiding the "undefined" states, we see that $\rho A_J = B'C'$ and $\rho A_K = BC$ are the results of using the Karnaugh map in Table 6. These equations define the first flip-flop in the Johnson counter circuit.

Table 6.   Karnaugh map of the mod-6 counter's first bit.

ρA / A \ BC	00	01	11	10
0	α (0)	0 (1)	0 (3)	x (2)
1	1 (4)	x (5)	β (7)	1 (6)

Referencing rules in Table 3 and avoiding the "undefined" states, we see that $\rho B_J = A$ and $\rho B_K = A'$ are the results of using the Karnaugh map in Table 7. These equations define the second flip-flop in the Johnson counter circuit.

Table 7.   Karnaugh map of the mod-6 counter's second bit.

ρB / A \ BC	00	01	11	10
0	0 (0)	0 (1)	β (3)	β (2)
1	α (4)	α (5)	1 (7)	1 (6)

Referencing rules in Table 3 and avoiding the "undefined" states, we see that $\rho C_J = B$ and $\rho C_K = B'$ are the results of using the Karnaugh map in Table 8. These equations define the third flip-flop in the Johnson counter circuit.

Table 8.   Karnaugh map of the mod-6 counter's third bit.

ρC / A \ BC	00	01	11	10
0	0 (0)	β (1)	1 (3)	α (2)
1	0 (4)	β (5)	1 (7)	α (6)

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The three pairs of equations just developed can be realized in the Johnson counter depicted in Figure 11. From this figure, it follows that "A" corresponds to the output of the leftmost flip-flop, "B" corresponds to the center flip-flop and "C" corresponds to the rightmost flip-flop. The A', B' and C' correspond to the logical inversions of the flip-flop outputs.
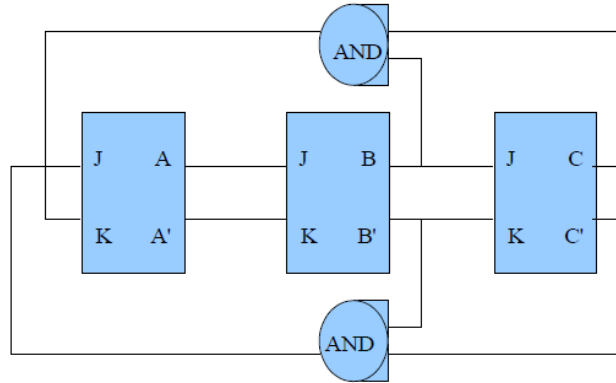
Figure 11.   Mod-6 Johnson counter circuit.

That concludes all the associations between "transition state mapping," the mod-6 counter and multiplexing on the mod-6 synthetic SVM VSI controller of this thesis' circuit board as well as the simulation.

b.   *Mod-12 Counter*

For the second example of sef-correcting modulo-N counters developed with "transition state mapping" N is chosen to be 12. The finalized design can be found in Appendix C-1, but inescapably, we recognize designing a mod-12 counter requires twelve choices, which means four flip-flops are necessary. Thus, it can be deduced that this counter requires only four bits and could be represented by the following mod-12 count states listed under "Behavior" in Table 9.

The counter states referred to in Table 9 are those of a "Johnson (shift) counter" and only columns A and D require equations. Simply put, the input of C comes from output of B and the input of B comes from the output of A. For the sake of

demonstration though, all the equations for the counter will be developed. In Table 10, Xs have been inserted for the four missing states.

Table 9.   Modulo-12 counter's desired behavior.

Present State				Desired Next State				Behavior			
A	B	C	D	A'	B'	C'	D'	A"	B"	C"	D"
0	0	0	0	1	0	0	0	α	0	0	0
1	0	0	0	1	1	0	0	1	α	0	0
1	1	0	0	1	1	1	0	1	1	α	0
1	1	1	0	0	1	1	0	β	1	1	0
0	1	1	0	0	0	1	0	0	β	1	0
0	0	1	0	0	0	0	1	0	0	β	α
0	0	0	1	1	0	0	1	α	0	0	1
1	0	0	1	1	1	0	1	1	α	0	1
1	1	0	1	1	1	1	1	1	1	α	1
1	1	1	1	0	1	1	1	β	1	1	1
0	1	1	1	0	0	1	1	0	β	1	1
0	0	1	1	0	0	0	0	0	0	β	β

Table 9 then becomes a starting place that when all states are accounted for will resemble Table 10.

Table 10.   All possible states of mod-12 counter.

Present State				Desired Next State				Behavior			
A	B	C	D	A'	B'	C'	D'	A"	B"	C"	D"
0	0	0	0	1	0	0	0	α	0	0	0
0	0	0	1	1	0	0	1	α	0	0	1
0	0	1	0	0	0	0	1	0	0	β	α
0	0	1	1	0	0	0	0	0	0	β	β
0	1	0	0	x	0	1	0	x	β	α	0
0	1	0	1	x	0	1	1	x	β	α	1
0	1	1	0	0	0	1	0	0	β	1	0
0	1	1	1	0	0	1	1	0	β	1	1
1	0	0	0	1	1	0	0	1	α	0	0
1	0	0	1	1	1	0	1	1	α	0	1
1	0	1	0	x	1	0	1	x	α	β	α
1	0	1	1	x	1	0	0	x	α	β	α
1	1	0	0	1	1	1	0	1	1	α	0
1	1	0	1	1	1	1	1	1	1	α	1
1	1	1	0	0	1	1	0	β	1	1	0
1	1	1	1	0	1	1	1	β	1	1	1

As we put Table 10's "Behavior" entries into Karnaugh maps, one column at a time, for the mod-12 example, we shall see that the entire procedure is very similar to the development that took place for the mod-6 example. We should expect the equations from the mod-12 Karnaugh maps are familiar and the circuit layout are expanded versions of the mod-6 example. As we proceed, we can check our work by comparing the mod-6 results with the mod-12 results.

Referencing rules in Table 3 and avoiding the "undefined" states, we see that $\rho A_J = B'C'$ and $\rho A_K = BC$ are the results of using the Karnaugh map in Table 11. These equations define the leftmost (or first) flip-flop in the mod-12 Johnson counter circuit.

Table 11.   Karnaugh map of mod-12 counter's first bit.

ρA | C D

A B	0 0	0 1	1 1	1 0
0 0	α 0	α 1	0 3	0 2
0 1	x 4	x 5	0 7	0 6
1 1	1 12	1 13	β 15	β 14
1 0	1 8	1 9	x 11	x 10

Referencing rules in Table 3 and avoiding the "undefined" states, we see that $\rho B_J = A$ and $\rho B_K = A'$ are the results of using the Karnaugh map in Table 12. These equations define the second flip-flop in the mod-12 Johnson counter circuit.

Table 12.   Karnaugh map of mod-12 counter's second bit.

ρB | C D

A B	0 0	0 1	1 1	1 0
0 0	0 0	0 1	0 3	0 2
0 1	β 4	β 5	β 7	β 6
1 1	1 12	1 13	1 15	1 14
1 0	α 8	α 9	α 11	α 10

Referencing rules in Table 3 and avoiding the "undefined" states, we see that $\rho C_J = B$ and $\rho C_K = B'$ are the results of using the Karnaugh map in Table 13. These equations define the third flip-flop in the mod-12 Johnson counter circuit.

Table 13.   Karnaugh map of mod-12 counter's third bit.

ρC / CD

AB \ CD	00	01	11	10
00	0 _(0)_	0 _(1)_	β _(3)_	β _(2)_
01	α _(4)_	α _(5)_	1 _(7)_	1 _(6)_
11	α _(12)_	α _(13)_	1 _(15)_	1 _(14)_
10	0 _(8)_	0 _(9)_	β _(11)_	β _(10)_

Referencing rules in Table 3 and avoiding the "undefined" states, we see that $\rho D_J = B'C$ and $\rho D_K = B'C$ are the results of using the Karnaugh map in Table 14. These equation define the fourth flip-flop in the Johnson counter circuit. The first three pairs of equations are identical to the three pairs of design equations used in the mod-6 counter and are supplemented be a fourth pair required for creating the mod-12 counter.For those interested, the transition state mapping techniques described above can be found in more detail in reference [10].

Table 14.   Karnaugh map of mod-12 counter's fourth bit.

ρD / CD

AB \ CD	00	01	11	10
00	0 _(0)_	1 _(1)_	β _(3)_	α _(2)_
01	0 _(4)_	1 _(5)_	1 _(7)_	0 _(6)_
11	0 _(12)_	1 _(13)_	1 _(15)_	0 _(14)_
10	0 _(8)_	1 _(9)_	β _(11)_	α _(10)_

The four pairs of equations just developed can be realized in the Johnson counter depicted in Figure 12. From the figure, it follows that "A" corresponds to the output of the leftmost flip-flop and "D" corresponds to the output of the rightmost flip-flop. In addition, the reader can observe that the first three pairs of equations (bits) are identical to the mod-6 example
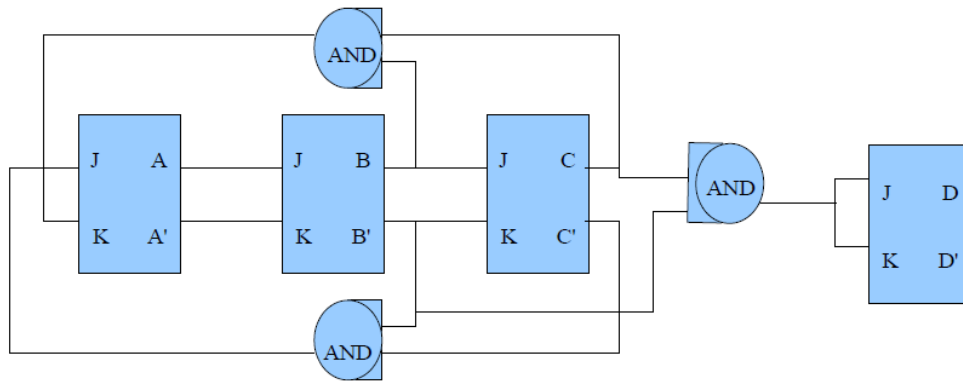

Figure 12.   Mod-12 Johnson counter circuit.

That concludes all the associations between "transition state mapping," the mod-12 counter and multiplexing on the mod-12 synthetic SVM VSI controller of this thesis' circuit board as well as the simulation.

2.   Pulse Train Generation

Before discussing pulse train generation, two rules should be kept in mind. The first rule is that any full-scale construction of these units should keep the switching speeds (or the oscillator's triangle signal) below the practical switching speed of the switches used in the VSI. The second rule is that one should make sure that a switch pair is never simultaneously 'on' by observing the use of a turn-on delay. Failure to observe this design step will lead to the failure of semiconductors caused by a short-circuit condition known as "shoot-through."

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a. Three-Pulse Trains for mod-6 Counter

Figure 13 illustrates the comparison of a triangle waveform to three voltage levels producing pulse trains. Once produced, the three resulting pulse trains are multiplexed to create three "raw" gating signals for the three upper switches in the VSI. For mod-6, one pulse train always remains at fifty percent duty cycle ($D_{p2} = 50\%$) while the other two ($P_1(t)$ and $P_3(t)$) are mirror opposites around $P_2(t)$. With duty cycle control, the mirror image pulse trains (upper and lower), vary in pulse-width in opposing ways as shown in Figure 14. Figure 14 illustrates three modulation indices of 5%., 50% and 95%. The entire theoretical continuous range of modulation is $0 \le m \le 100\%$. Applying the limits of the modulation index to the range for the duties cycle of the pulse trains results in the following duty cycle limits for pulse trains one and three:

$50\% \le D_{p1} \le 100\%$ and $0\% \le D_{p3} \le 50\%$.
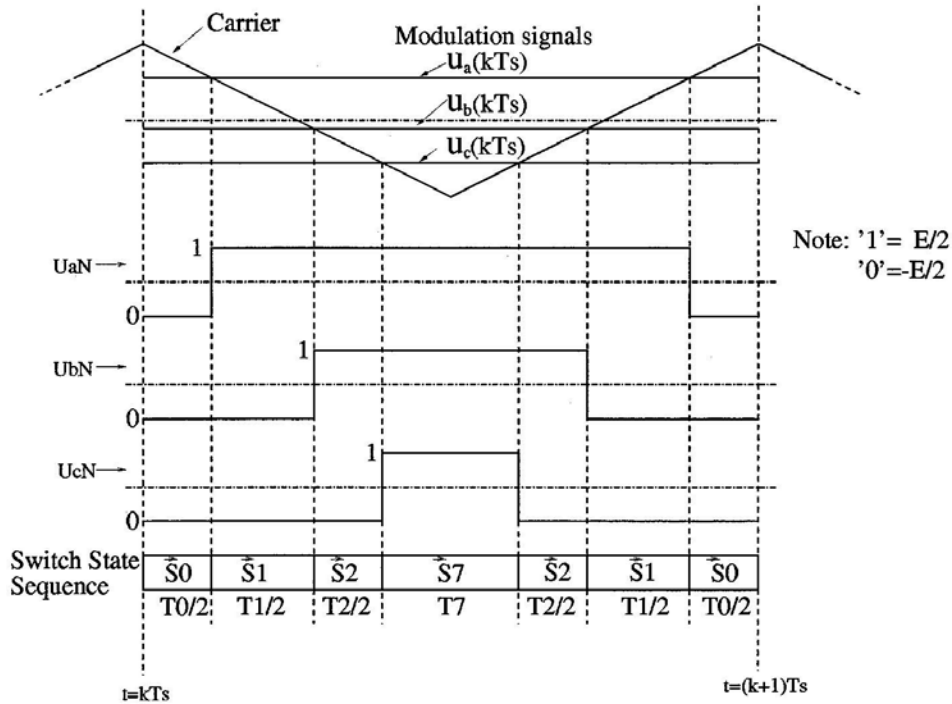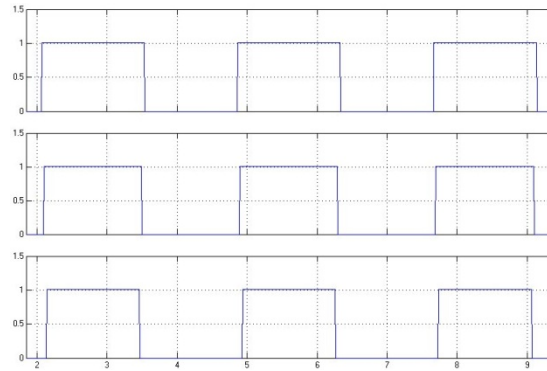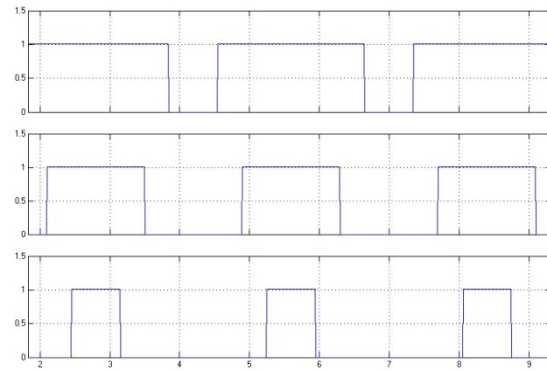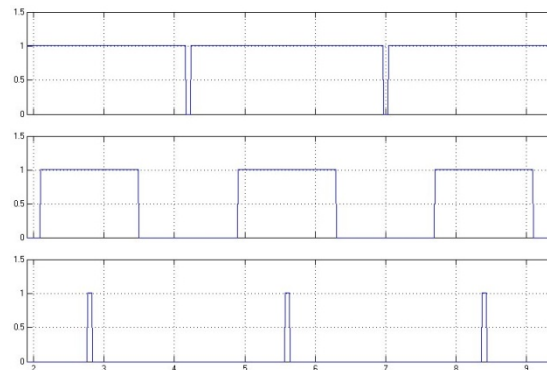

Figure 13.   Triangle wave to pulse train generation. From [3].

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(a) 5% Modulation

(b) 50% Modulation

(c) 95% Modulation

Figure 14.   Demonstration of mod-6 pulse-train modulation depth. From [5].

Figure 15 shows the three center-aligned pulse-trains labeled as signal "a," "b" and "c." The Johnson counter steps through its sequence and gates the three signals of Figure 15 into the three-phase multiplexer in the following manner as shown in Table 15.
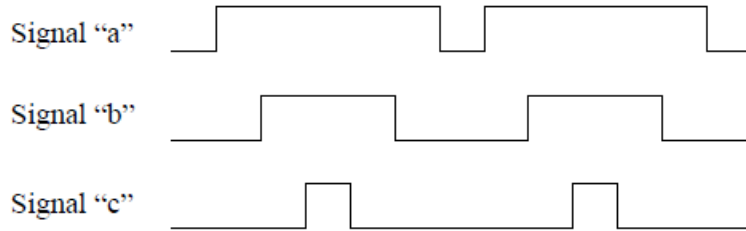

Figure 15.   Mod-6 counter gates to the three-phase multiplexer.

Table 15.   Mod-6 multiplexer gate signals to pulse train scheduling.

Johnson sequence A B C	Phase I signal	Phase II signal	Phase III signal
0 0 0	a	b	c
1 0 0	b	a	c
1 1 0	c	a	b
1 1 1	c	b	a
0 1 1	b	c	a
0 0 1	a	c	b

The Simulink reproduction of the mod-6 version hardware explicitly performs time division multiplexing as is found in [8]; however, the Simulink™ version omits the safety and motor-direction features found in the wire-wrapped hardware or computer aided design (CAD) versions of the circuit created.

b. *Six Pulse Trains for mod-12 Counter*

For the mod-12 synthetic-SVM unit, a comparison is made between a triangle waveform and six voltage levels producing six pulse trains. Once produced, the six resulting pulse trains are multiplexed creating three "raw" gating signals, one for each phase, for the three upper switches in the VSI. For mod-12, there are three-pairs of pulse trains that are mirrored around the fifty percent duty cycle point. We will define the mirror pairs as $P_1(t)$ and $P_6(t)$, $P_2(t)$ and $P_5(t)$, and $P_3(t)$ and $P_4(t)$. With duty cycle control, the mirror image pulse trains (upper and lower), vary in pulse-width in opposing ways as shown in Figure 16. Figure 16 illustrates three modulation indices of 5%., 50% and 95%. The entire theoretical continuous range of modulation is $0 \leq m \leq 100\%$. Applying the limits of the modulation index to the range for the duties cycle of the pulse trains results in the following duty cycle limits for pulse trains $P_1(t)$, $P_2(t)$ and $P_3(t)$ are $50\% \leq D_p \leq 100\%$, and $P_4(t)$, $P_5(t)$ and $P_6(t)$ are $0\% \leq D_p \leq 50\%$.

(a) 5% Modulation

(b) 50% Modulation
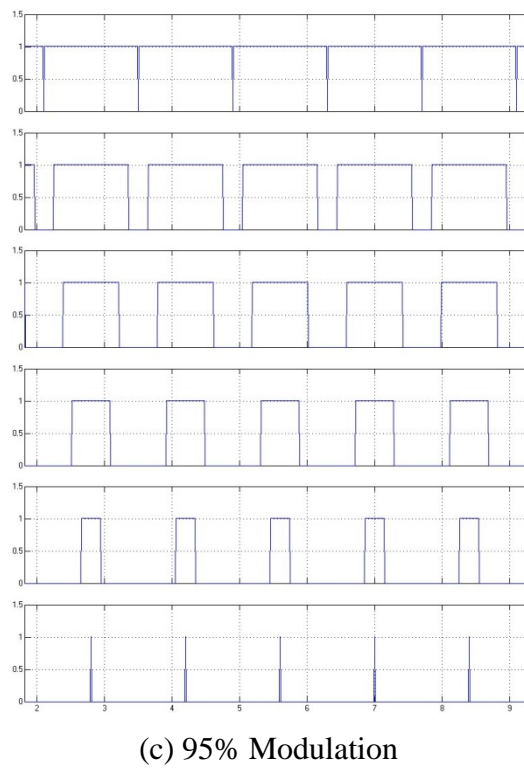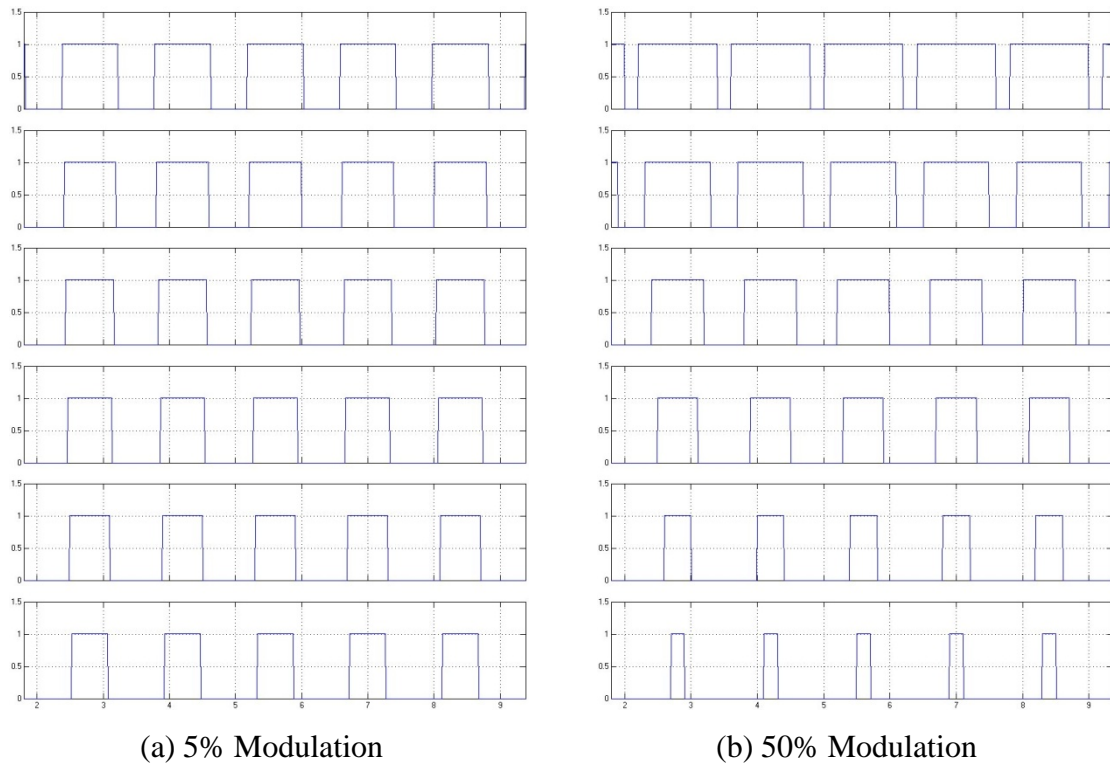
(c) 95% Modulation

Figure 16.   Demonstration of mod-12 pulse-train modulation depth. From [5].

The hardware version of the mod-12 synthetic-SVM unit was designed to limit the pulse train duty cycles via resistor dividers by pairs as follows:

$$50.00\% \leq D_{p1} \leq 91.67\% \text{ and } 8.33\% \leq D_{p6} \leq 50.00\%$$

$$50.00\% \leq D_{p2} \leq 75.00\% \text{ and } 25.00\% \leq D_{p5} \leq 50.00\%$$

$$50.00\% \leq D_{p3} \leq 58.33\% \text{ and } 41.67\% \leq D_{p4} \leq 50.00\%$$

Keep in mind, the present limits can be extended simply by reducing the amplitude of the triangle waveform by 16.67%.

Figure 17 shows the six center-aligned pulse-trains labeled as Signal "a," "b," "c," "d," "e" and "f." The Johnson counter steps through its sequence and gates the six signals of Figure 17 into the three-phase multiplexer as shown in Table 16.
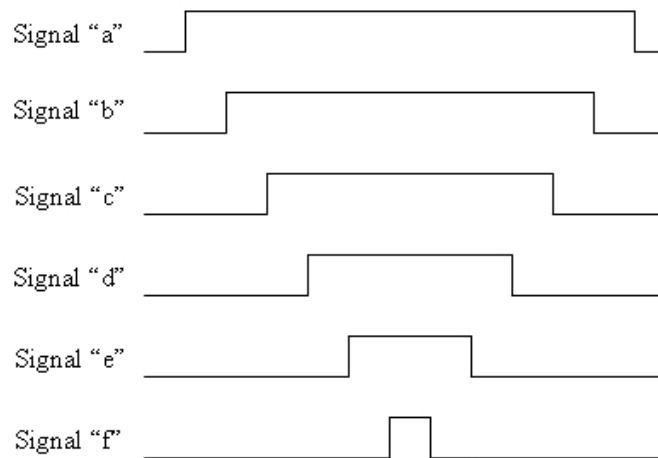

Figure 17.   Mod-12 counter gates to the three-phase multiplexer.

Table 16.   Mod-12 multiplexer gate signals to pulse train scheduling.

Johnson sequence A B C D	Phase I signal	Phase II signal	Phase III signal
0 0 0 0	a	d	e
1 0 0 0	b	c	f
1 1 0 0	c	b	f
1 1 1 0	d	a	e
0 1 1 0	e	a	d
0 0 1 0	f	b	c
0 0 0 1	f	c	b
1 0 0 1	e	d	a
1 1 0 1	d	e	a
1 1 1 1	c	f	b
0 1 1 1	b	f	c
0 0 1 1	a	e	d

c.   *Nine Pulse Trains for mod-18 Counter*

For the mod-18 synthetic-SVM unit, we are going to compare a triangle waveform to nine voltage levels producing nine pulse trains. Once produced, the nine resulting pulse trains are multiplexed creatingcreating three-phase "raw" gating signals, one for each of three pases, for the three upper switches in the VSI. For mod-18, one pulse train always remains at fifty percent duty ($D_{p5} = 50\%$) while the other eight can be grouped in four mirror image pairs: $P_1(t)$ and $P_9(t)$, $P_2(t)$ and $P_8(t)$, and $P_3(t)$ and $P_7(t)$, and $P_4(t)$ and $P_6(t)$. The pairs are mirror opposites around $P_5(t)$. With duty cycle control, the mirror image pulse trains (upper and lower), vary in pulse-width in opposing ways as previously shown for the mod-6 and mod-12 cases. The entire theoretical continuous range of modulation is $0 \leq m \leq 100\%$. Applying the limits of the modulation index to the range for the duty cycle of the pulse trains results in the following duty cycle limits for pulse trains $P_1(t)$ through $P_4(t)$ are $50\% \leq D_p \leq 100\%$, and $P_6(t)$ through $P_9(t)$

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are $0\% \leq D_p \leq 50\%$. There was no hardware version or software model created for mod-18 synthetic-SVM unit.

d.   *Twelve Pulse Trains for mod-24 Counter*

For the mod-24 synthetic-SVM unit, we are going to compare a triangle waveform to twelve voltage levels producing twelve pulse trains. Once produced, the twelve resulting pulse trains are multiplexed creatingcreating three-phase "raw" gating signals , one for each of three phases, for the three upper switches in the VSI. For mod-24, there are six-pairs of pulse trains that are mirrored around the fifty percent duty cycle point. With duty cycle control, the mirror image pulse trains (upper and lower), vary in pulse-width in opposing ways as previously shown for the mod-6 and mod-12 cases. The entire theoretical continuous range of modulation is $0 \leq m \leq 100\%$. Applying the limits of the modulation index to the range for the duties cycle of the pulse trains results in the following duty cycle limits for pulse trains $P_1(t)$ through $P_6(t)$ are $50\% \leq D_p \leq 100\%$, and $P_6(t)$ through $P_{12}(t)$ are $0\% \leq D_p \leq 50\%$. There was no hardware version or software model created for mod-24 synthetic-SVM unit.

No matter which mod-N version one chooses, the circuit is still a generic VSI controller. Thus, the synthetic SVM unit should appear in the block marked "thesis electronics" in Figure 18.
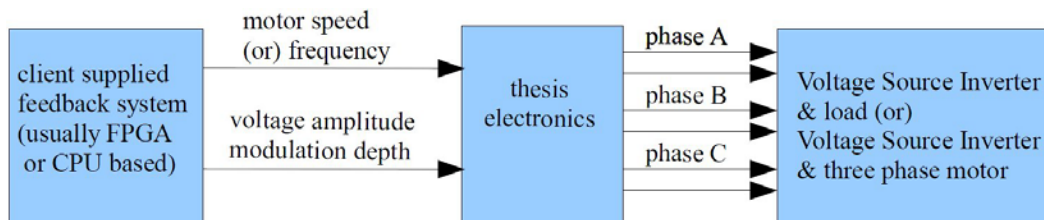

Figure 18.   Block diagram of synthetic SVM system.

3.   **Unresponsive Motor States and Safety Hazard**

In Figure 19, the VSI indicates two connections, which both represent zero voltage across the motor windings phase-to-phase. With the V0 state, the motor is clearly

connected to 0V, but with the V7 state, all of the windings are connected to the high side bus. Caution should be taken with either state, but the user may not be aware of the high voltage potential associated with V7. Differences in DC levels between any two of the three motor terminals will cause movement, but only a constantly changing voltage difference on the three terminals ensures rotation. Even if, as seen in Figure 20, the synchronously changing AC signals are multiplexed, there will still be no motor rotation. Again, for a three-phase AC motor, only a voltage difference between any two terminals will cause rotation.
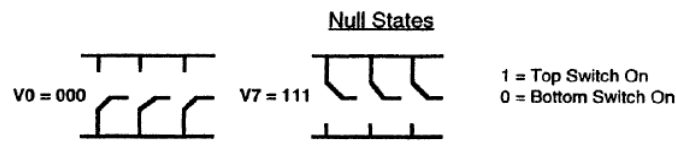
Figure 19.　　Two SVM zero states. From [1].
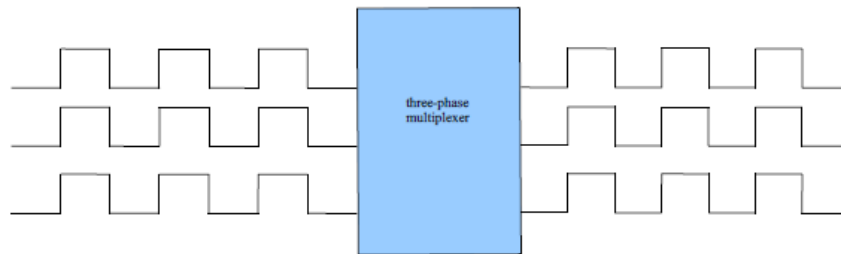
Figure 20.　　Input and output of multiplexed null vectors.

B.　　PWM, SVM AND OTHER WAVEFORMS FED TO VSIS

1.　　Pulse Width Modulation

a.　　Sine Wave

Figure 21 illustrates how most PWM is generated and sent to each of the three legs of a VSI. The method depends on the sine wave in each leg having the same frequency and amplitude, yet phase-shifted from one another by 120 degrees. The

depiction shown here indicates that "deadtime" is seemingly the responsibility of the lower part of the VSI "leg," but the deadtime is typically symmetric between upper and lower switches. It should be noted that most modern gate drivers have a built-in selectable deadtime time.
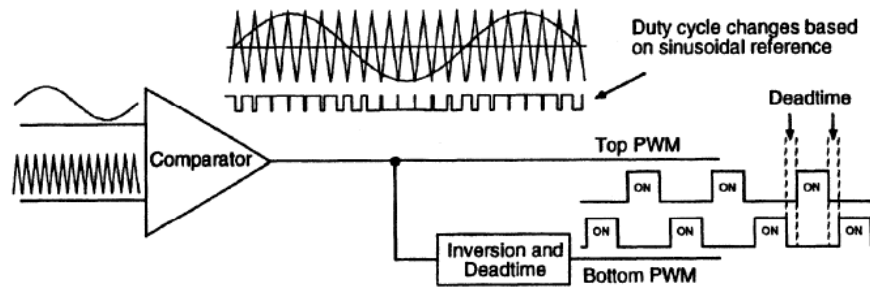

Figure 21.   Sine-triangle PWM generation of gating signals. From [1]

b.   *Sine Wave with Third Harmonic Injection*

Figure 22 illustrates both third harmonic injection and PWM. The reference waveform V_{ref} is the desired fundamental of the VSI three-phase output. The "Zero Sequence Waveform Generator" is the third harmonic (or a combination of third order harmonics) of the fundamental. The product of the reference and zero sequence create the "Modified Signal, which is sent to the "Comparator." The comparator utilizes a triangle "Carrier Signal" to produce the actual PWM "Output Pulses."
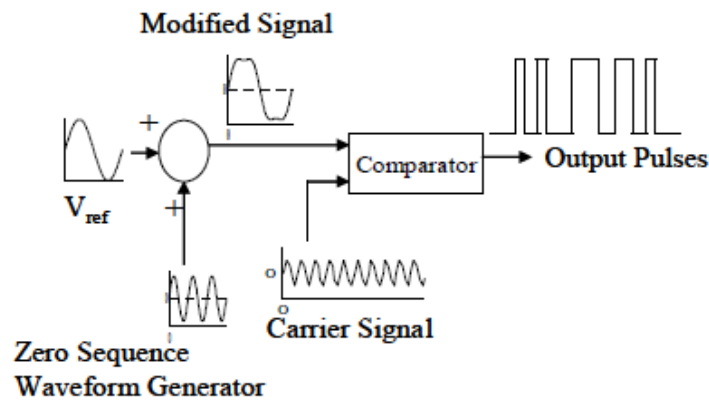

Figure 22.   Generation of third harmonic injected PWM. From [11].

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Figure 23 shows a six switch VSI with a simulated motor load where the neutral of the wye-connected load is floating. When utilizing third harmonic injection (or a combination of third order harmonics), the final output voltage and current waveforms are purely sinusoidal excluding carrier frequency ripple. The zero sequence components disappear in the line-line voltages (V_{ab}, V_{bc} and V_{ca}) and line-neutral voltages (V_{an}, V_{bn}, and V_{cn}). However, when viewing the output while referencing the ground node (V_{ag}, V_{bg}, and V_{cg}), all the third order components are present.
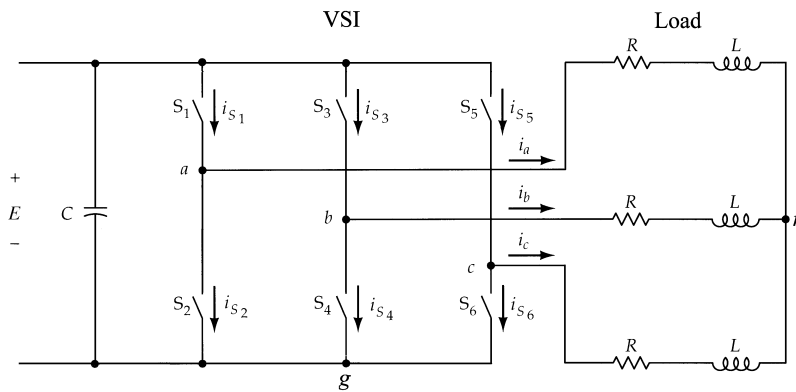
Figure 23.   Six-switch VSI with simulated motor load. From [5].
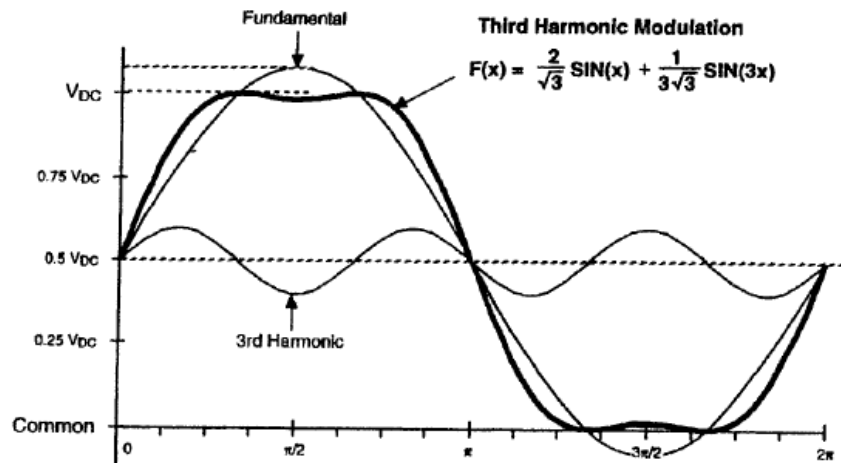
Figure 24.   Components of third harmonic injection template. From [1]

c.   *Sixty degree PWM*

Figure 25 depicts sixty degree PWM. Synthesizing Figure 25 by electronics hardware would require a look-up table, several synched-up overlapping sine wave generators or each point could be calculated on a fast central processing unit (CPU) using the following formula to calculate the points:

$$F(x) = \frac{2}{\sqrt{3}}\sin x + \frac{1}{2\pi}\sin 3x + \frac{1}{60\pi}\sin 9x + \frac{1}{280\pi}\sin 15x + \cdots. \qquad (5)$$
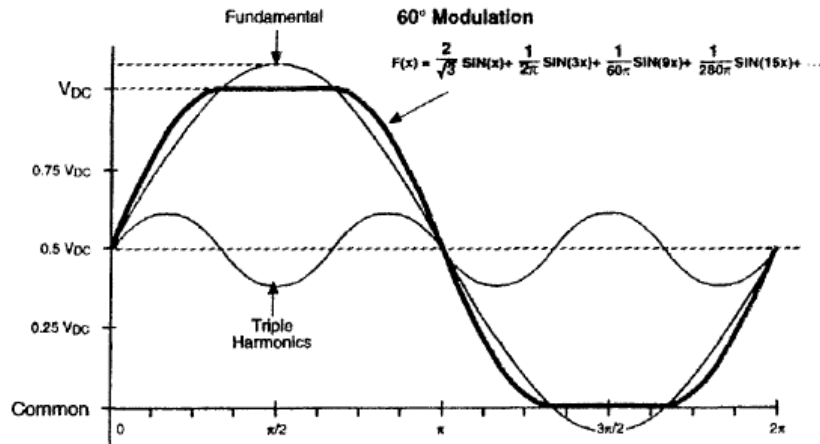

Figure 25.   Sixty-degree PWM wave-shape produced by CPU. From [1].

2.   Space Vector Modulation and Synthetic SVM

a.   *Characteristics of Space Vector Modulation*

The synthetic SVM circuit mimics SVM through the use of time division multiplexing and center-aligned pulse trains. Unless otherwise defined, PWM has been associated with comparing a high frequency carrier triangle waveform to a lower frequency sine wave, amplifying the resultant digital waveform and filtering the output waves reproducing the original sine. (Third order harmonic injection is a modification of the process that allows for greater DC bus utilization.)

For this thesis, two synthetic SVM units (mod-6 and mod-12) were designed and constructed. The schematics for the units appear in Appendices B and C

while a high-level block diagram is shown in Figure 26. The Signal Development block contains a function generator and comparator that produce the pulse trains and clocking signal. For both units, all three-phases shared a common triangle carrier wave generator. On the wire-wrapped version of the mod-6 and mod-12 Synthetic SVM units the triangle wave is produced using an NE566 function generator chip. The LM393 dual comparator chips produce the pulse trains.

The mod-N Clocking block is a Johnson counter. The mod-6 and mod-12 wire-wrapped Johnson counters constructed using 74112 JK flip-flops. The logic blocks, done in Simulink, represent partial internals of the 74251 multiplexer chips. The six outputs from the logic blocks (simulating multiplexer chips) are for the top and bottom switches of each of the VSI's three legs and are the gating signals for the VSI.
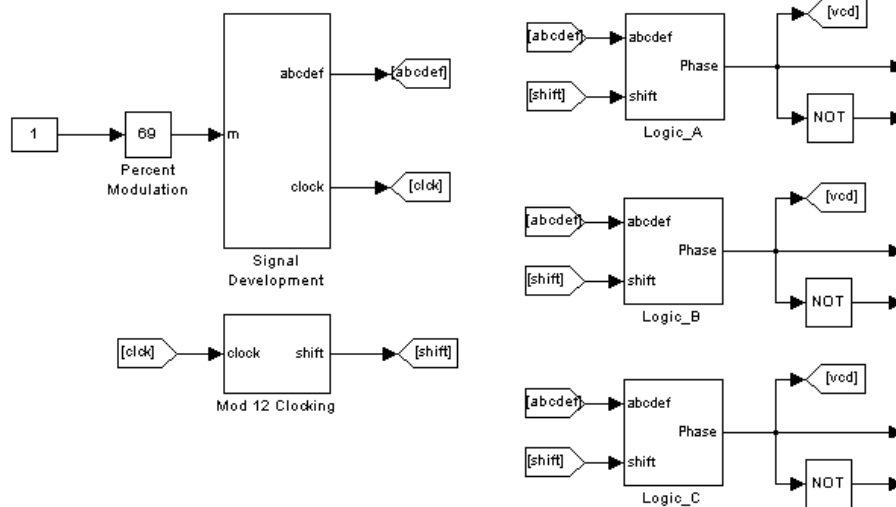

Figure 26.   Simulink™ block diagram of synthetic SVM unit. From [5].

With SVM, the VSI is treated much like a system of synchronous flip-flops; however, PWM treats the VSI as if it were push-pull amplifiers. This is the primary difference between the two methods. In short, SVM has at least three major characteristics distinguishing it from PWM. These are:

    (1)   the VSI is treated as if it were three flip-flops with eight possible states,

    (2)   the VSI upper and low switches are generally the logical inverse of

each other except when both switches are off for dead time and emergencies, and

(3)   the VSI switching minimization is similar to Gray codes found in digital electronics apparatus and texts.

The next sections will illustrate several variations of SVM switching sequences and show how center-aligned versions of the sequences are constructed. Center-aligned switching sequences, it can be observed, eliminate "simultaneous switching" phenomena reducing switch stress and are noticeably more Gray sequence observant than other SVM sequences.

c.   Variants of Space Vector Modulation

The Null = V0 sequence illustrated in Figure 27 is one of the best sequences for switch stress minimization. Each switch in the VSI remains "off" for 120 degrees of each 360-degree cycle. Unfortunately, this variation does not prevent simultaneous switching. When two or more switches change state at the exact same moment, this is called "simultaneous switching". Simultaneous switching is avoided as often as possible because it can induce high dv/dt (a rapid change in voltage) and di/dt (a rapid change in current) in the circuit possibly destroying the circuit's semiconductors. If the sequence is center-aligned, simultaneous switching is avoided.
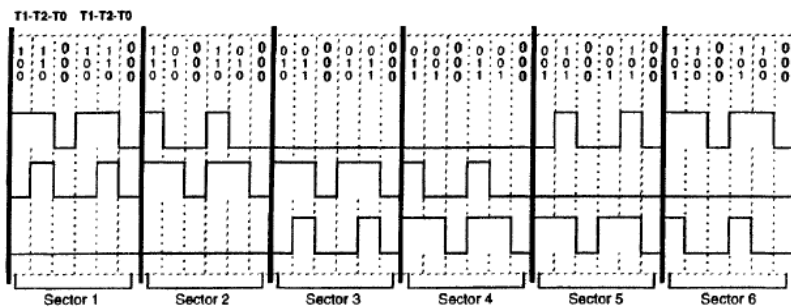

Figure 27.   "Null = V0" switching pattern. From [1].

In Figure 28 the null = 0 SVM switching sequence is performed in its center-aligned version and the phenomena of simultaneous switching is avoided.
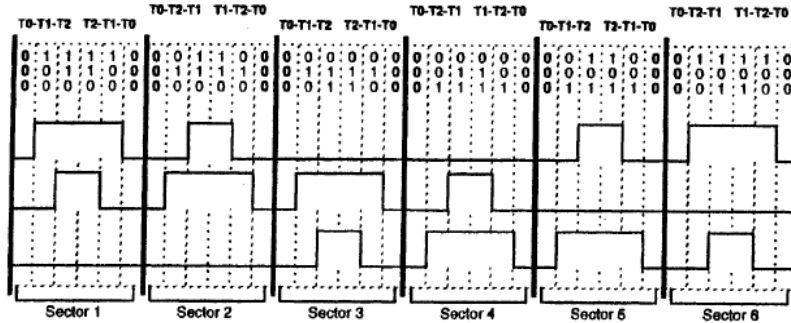
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Figure 28.   "Center-aligned null = V0" switching pattern. From [1].

In Figure 29 we see the generalized phase-to-neutral voltage produced by a VSI with an inductive load using null = V0. The inductive load filters the high frequency switching noise. Since the voltage waveform only contains the fundamental and odd triplet harmonics $\sum_{n=1,2,3,...} 3(2n-1) = (3,9,15,21,27,...)$, the phase current is purely sinusoidal. All third order harmonics cancel in an ungrounded three-phase system.
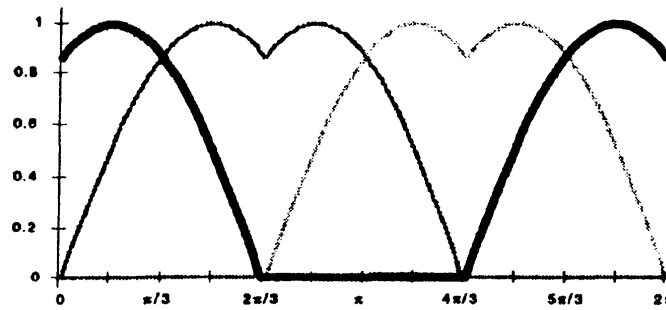
Figure 29.   "Null = V0" template of the output waveform. From [1].

The Null = V7 switching sequence of Figure 30 is another good sequence for switch stress minimization. Each switch in the VSI remains "on" for 120 degrees of each 360-degree cycle. If the sequence is center-aligned, the simultaneous switching is

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avoided. What follows in Figure 31 is the general form of the phase-to-neutral VSI output voltage resulting from a "null = V7" voltage switching sequence.
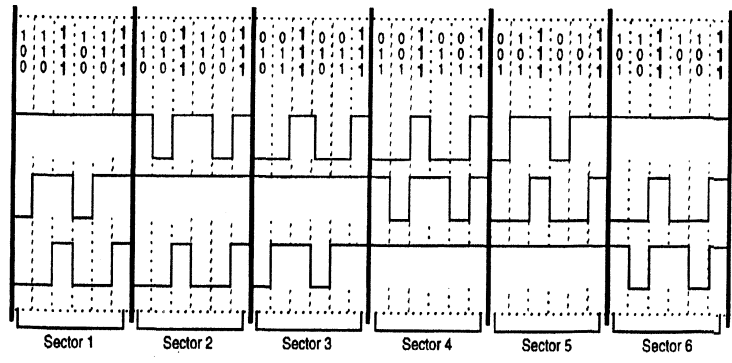

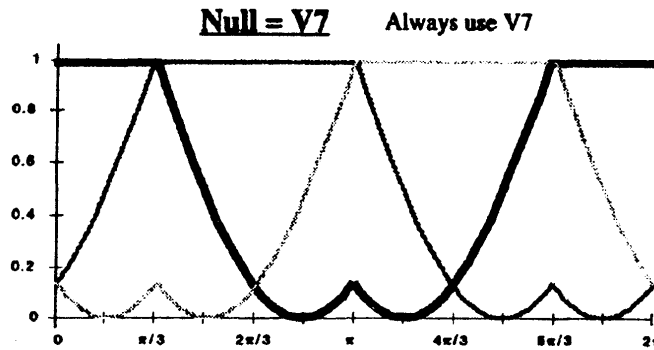Figure 30.   "Null = V7" switching pattern. From [1].

Figure 31.   "Null = V7 template of the output waveform. From [1].

If the Null = V0, V7 and null = V7, V0 sequences of figures 32 and 33 were not labeled, it would be difficult to tell them apart. The sequences break-up the long 120 degree periods of "no switch action" seen in Figures 27 and 30. The 120 degree periods are divided into two periods of sixty degrees each combining null = V0 and null = V7. Given center aligned pulse trains, simultaneous switching events should be avoidable for these sequences too.
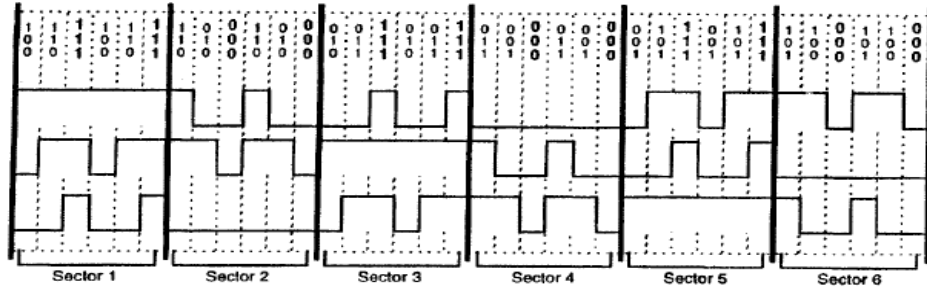
43

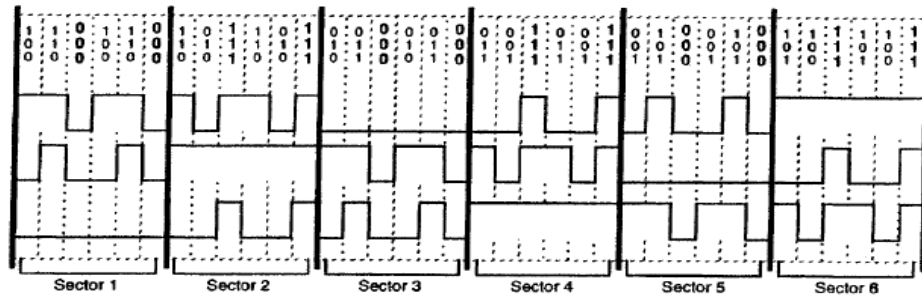Figure 32.   "Null = V7, V0" switching pattern. From [1].

Figure 33.   "Null = V0, V7" switching pattern. From [1].

If the SVM switching sequences of Figures 32 or 33 are chosen, the results are the phase voltage waveforms of Figure 34. As you can see, the two switching sequences are the inverse of each other and one might suspect the resulting currents are rich in harmonics.
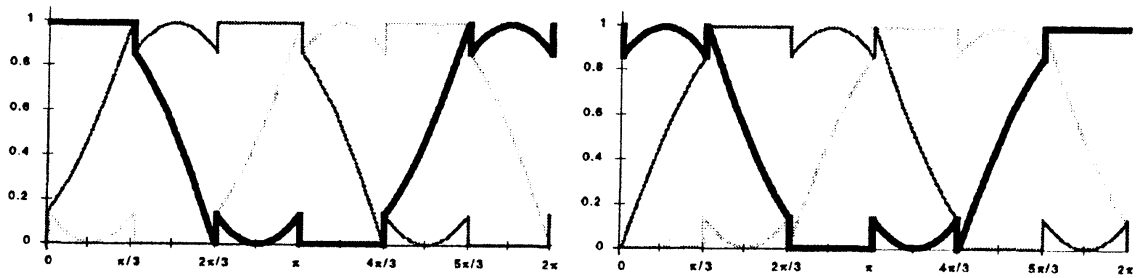

Figure 34.   "Null = V7, V0" and "null = V0, V7" templates of output waveforms. From [1].

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The "Alternating-Reversing" switching sequence of Figure 35 does not have simultaneous switching issues because it is inherently center-aligned. As it turns out, the Alt-Rev switching sequence is an optimal form of SVM. Furthermore, it mimics center-aligned sine-triangle PWM with third harmonic injection. As we will later see, this is the sequence that was implemented via synthetic SVM. Figure 36 encapsulates the raw phase waveform produced by the VSI.
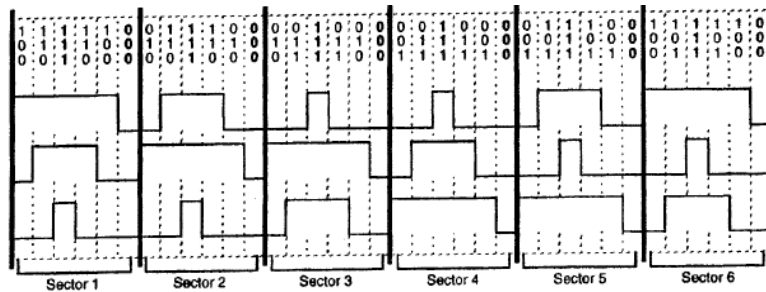

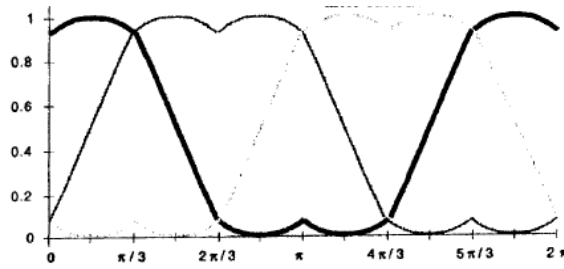Figure 35.   Alternating-Reversing switching pattern. From [1].

Figure 36.   Alt-Rev template for the output waveform. From [1].

3.   Six-Step

The Six-step switching sequence is an early technique used to control VSIs for variable speed motor applications prior to the advent of PWM. The VSIs using the six-step switching sequence experienced true switch transition minimization at the cost of current distortion. The distortion causes torque pulsations in motors that are exaggerated at low speeds. When PWM was first developed, slow speed operation was performed using PWM while high-speed operation utilized six-step switching. For efficiency purposes, the six-step switching sequence is still commonly used today for high-speed

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operation. Figure 37 shows the phase gating signals along with the line-neutral VSI output voltage.
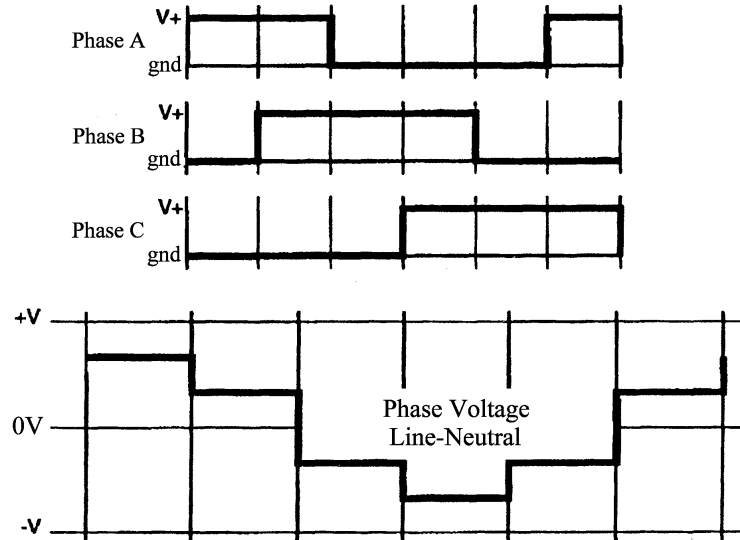

Figure 37.   Six-Step voltage sequence. From [1].

C.   DEADTIME PROBLEMS AND SOLUTIONS

In order to prevent shoot-through in a VSI switch leg, dead-time must exist between the turn-off of one switch and the turn-on of the other switch. Shoot-through occurs if both switches are simultaneously 'on' due to the characteristics of real switch operations. The shoot-through or short-circuit path is across the DC bus feeding the VSI.

Further, the introduction of unwanted torque pulsations from harmonics in the voltage waveform of a motor is undesirable from several standpoints and should be eliminated wherever and whenever possible and the "dead-time" during switch transitions of the VSI is often the culprit.

1.   Option 1: Minimizing Distortion with Software

There are published and practiced techniques minimizing the effects of dead-time created distortion. For instance, Motorola engineers designing with the MC68HC708MP16 microcontroller developed one useful technique. The engineers

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designed software for this microcontroller that polled its "on-board" voltage sensors during the power switch "dead-time," modified its waveforms accordingly and canceled out low frequency distortions and torque pulsations. The complete discussion can be found in [1]. This solution is unobtainable for this thesis because there is no software or processor on board the thesis electronics to adjust.

2.   Option 2: Handling Deadtime with Register Entry

Figure 38 shows the logic inversion of PWM1 with the delays included. As can be seen, the inversion of PWM0 is not perfect, because it contains additional delay. Figure 38 was extracted from [12] and represents deadtime entered by way of a registry entry. Unfortunately, This solution is also unobtainable for this thesis because there is no register of this sort on board the Synthetic SVM unit.
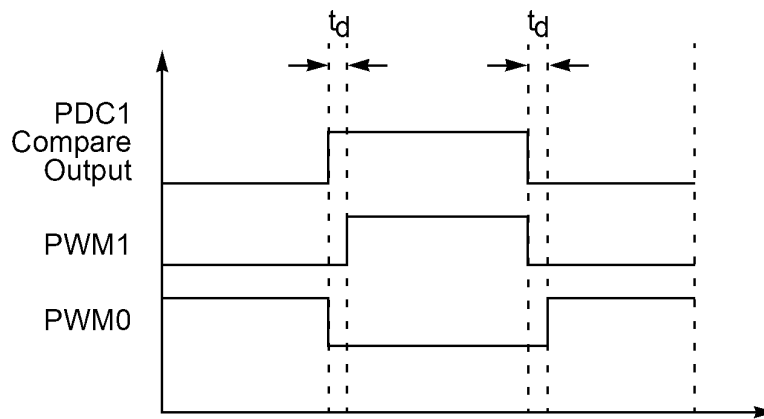

Figure 38.   Deadtime. From [12].

3.   Option 3: Handling Deadtime with Turn-on Delay (Selected)

After examining the literature, a simple pull-up resistor and pull-down capacitor pair driven by an Open-Collector (or Open-Drain) output transistor was all that was necessary to prevent "shoot through" [2]. Fortunately, the multiplexer (74251) provided both an output and its logical inverse that were then fed to "open collector" electronics, impedance matching circuitry (voltage follower) and passed to upper and lower VSI ransistor gating. Specifically the open-collector function was performed by 7405

inverters, but it could be done using LM393 (open collector) comparators. The schematic of the turn-on delay circuit is presented in Figure 39.
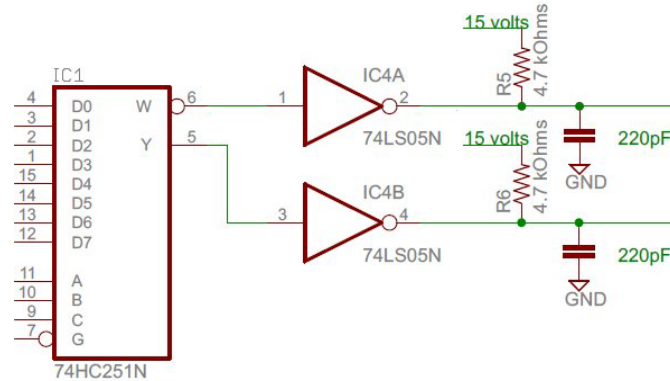

Figure 39.   Turn-on delay circuit.

D.   CONTROL STRATEGIES OVERVIEW

In order for the synthetic SVM unit to operate correctly, it requires "desired frequency" and "modulation depth". For the synthetic SVM hardware, the analog input expects $0V \leq V_f \leq 15V$ and will produce rectangular and triangular waveforms in the range of $1,270Hz \leq f \leq 12.4kHz..$ The requested modulation depth input expects an input voltage in the range of $0V \leq V_m \leq 15V$ and in response produces a modulation depth of $0\% \leq m \leq 70\%..$ In addition, the six output signals of the VSI controller (featuring synthetic SVM) to the VSI unit as seen in Fig 12 uses 0V and 15V to indicate "off" and "on," respectively. For completeness a short description of three feedback control types has been included.

1.   Constant Volts/Hertz

The speed of an induction motor can be easily controlled by varying the frequency of the three-phase supply; however, to maintain a constant (rated) flux density, the applied voltage must also be changed in the same proportion as the frequency (as dictated by Faraday's law). (In other words, the volt-seconds must remain constant.) This speed control method is known as Volts per Hertz. Above rated speed, the applied

voltage is usually kept constant at rated value; this operation is referred to as "constant horsepower." At low frequencies (i.e., speeds), the voltage must be boosted in order to compensate for the effects of the stator resistance [13].

2. Constant Slip-Speed

The constant slip-speed is a preferred and often used control algorithm for three-phase induction motors because of its simplicity, economy, robustness and energy efficiency [13]. An induction motor's maximum torque occurs at a load and frequency close to its maximum slip-speed. The simulation diagram of the "constant slip-speed" differential equations is shown in Figure 40.
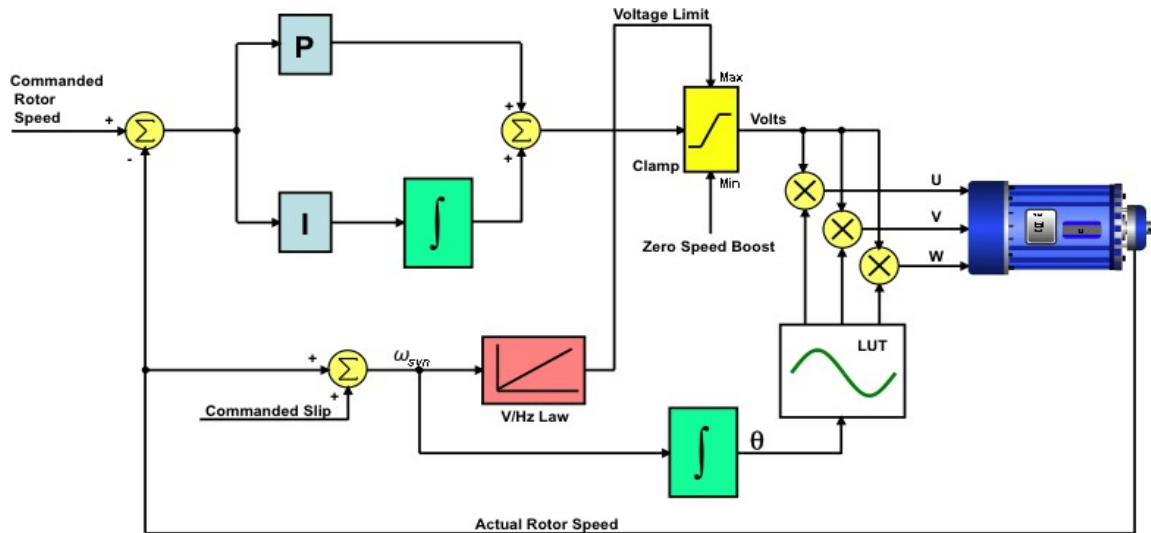

Figure 40.   Simulation diagram of the "constant slip-speed" algorithm. From [14].

3. Vector (Field-Oriented) Control

The majority of torque control drives implement vector control techniques in an effort to improve the transient response of the induction machine. To achieve this a microprocessor keeps track of the phase angle of a modulation wave and throws switches in the three VSI legs as necessary depending on angle, (hexagon) segment (6 segments, 60 degrees each) and loading. In a Root Locus controls sense, rotor field strength (or

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rotor current) is chosen making the system's response as quick as possible without any oscillatory behaviors according to [14]. As with the previous diagram, the simulation diagram in Figure 41 mostly draws from differential equations helping put the "field-oriented control" algorithm in perspective. Figure 42 compares the transient responses of the "field-oriented control" and "constant slip-speed" algorithms.
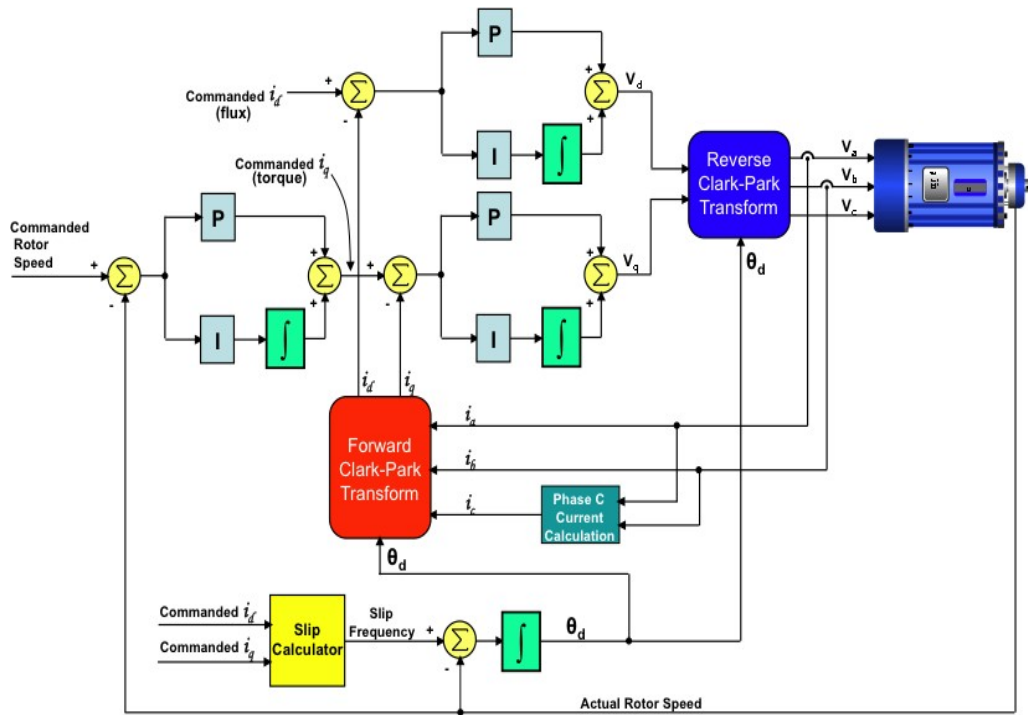

Figure 41.   Simulation diagram of the "field-oriented control" algorithm. From [14].
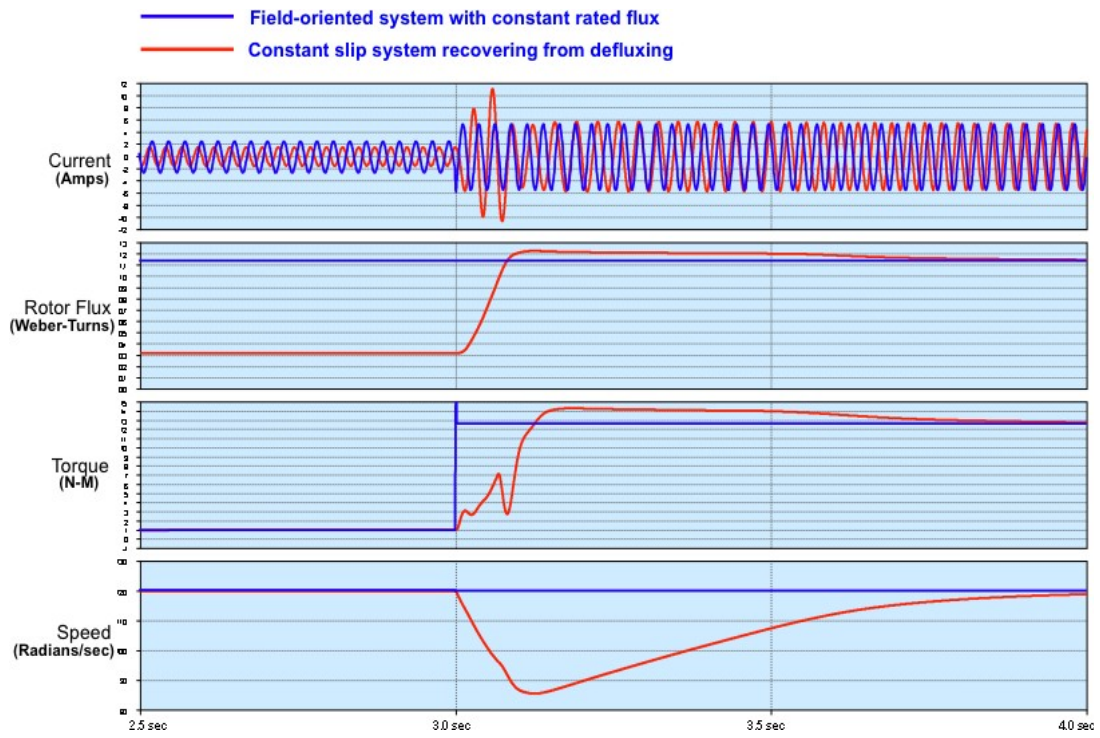
Figure 42.   (Red) "constant slip-speed" versus (blue) "field-oriented control."
From [14].

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III.   DESIGN, SIMULATE AND BUILD

A.   DESIGN, TEST, DOCUMENT AND BUILD

1.   Modulo-6

a.   *Counter and Three Pulse-Train Generator*

A wire-wrapped Mod-6 synthetic SVM unit can be seen in Figure 43. As expected, the mod-6 counter produced six, equally sized pulses with no time gaps or overlaps between the ending of one and the start of another as seen in Figure 44. The pulse train generator produced three center-aligned pulse trains with a fifty percent duty cycle when the modulation control voltage is adjusted to 0V (minimum) equating to $m = 0\%$. When the modulation control voltage is adjusted to 15V (maximum), the three pulse trains are approximately eighty five, fifty and fifteen percent duty cycles corresponding to $m = 70\%$. The analog frequency control is adjustable over the range of $1,270\text{Hz} \leq f \leq 12.4\text{kHz}$ (or $0\text{V} \leq V_f \leq 15\text{V}$). The circuit schematics may be found and inspected in Appendix B-1.
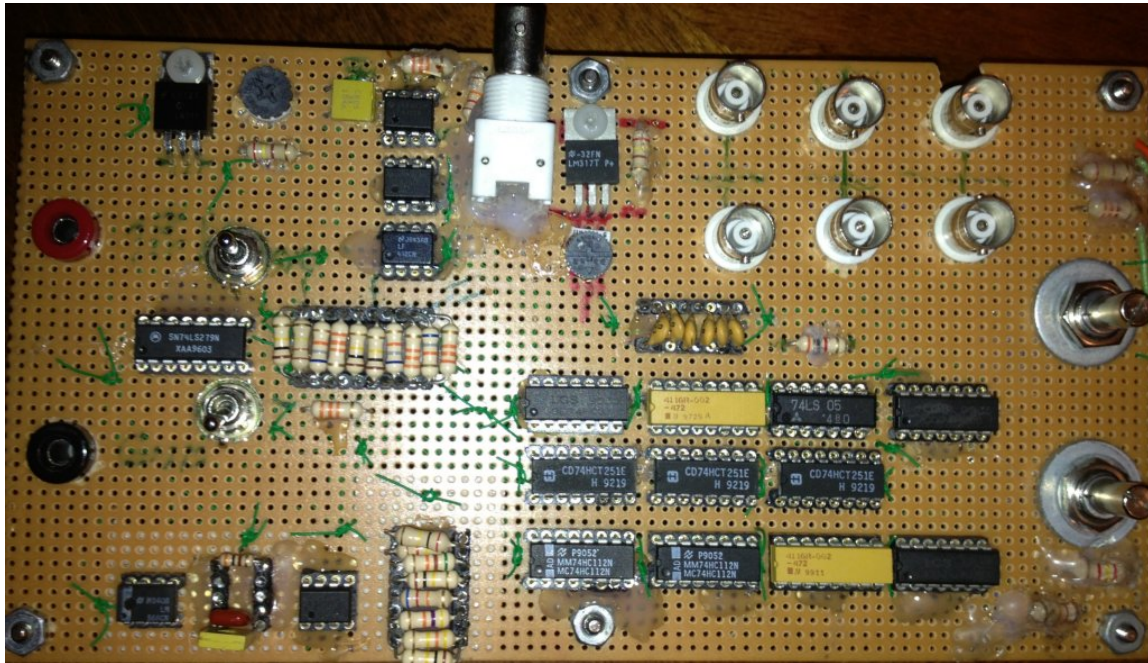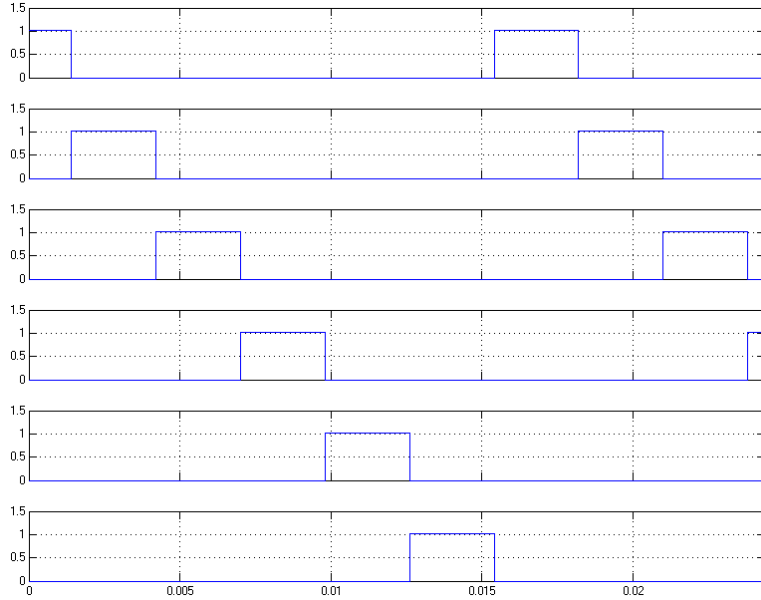

Figure 43.   Mod-6 bench top hardware.

Figure 44.   Mod-6 counter output. From [5].

b.   *Multiplexer and Turn-on Delays*

For the mod-6, wire-wrapped synthetic SVM circuit there was one
(74251) multiplexer chip required per phase where six of the possible eight inputs are
utilized. Further, the 74251 chips have both logic and inverse logic outputs. Unlike the
simulation, the hardware incorporated a a turn-on delay (dead-time) as explained in
Section II-C-3 and Appendix B-2.

c.   *Oscilloscope Results*

Figure 45 shows plots for the "as built" hardware extremes for the mod 6
synthetic SVM unit. The requested frequencies were $f = 1.27\text{kHz}$ and $f = 12.4\text{kHz}$
(where $\omega = 6,350\text{rpm}$ and $\omega = 62,000\text{rpm}$ for a 4-pole machine) while the requested
modulations were $m = 0\%$ and $m = 70\%$.

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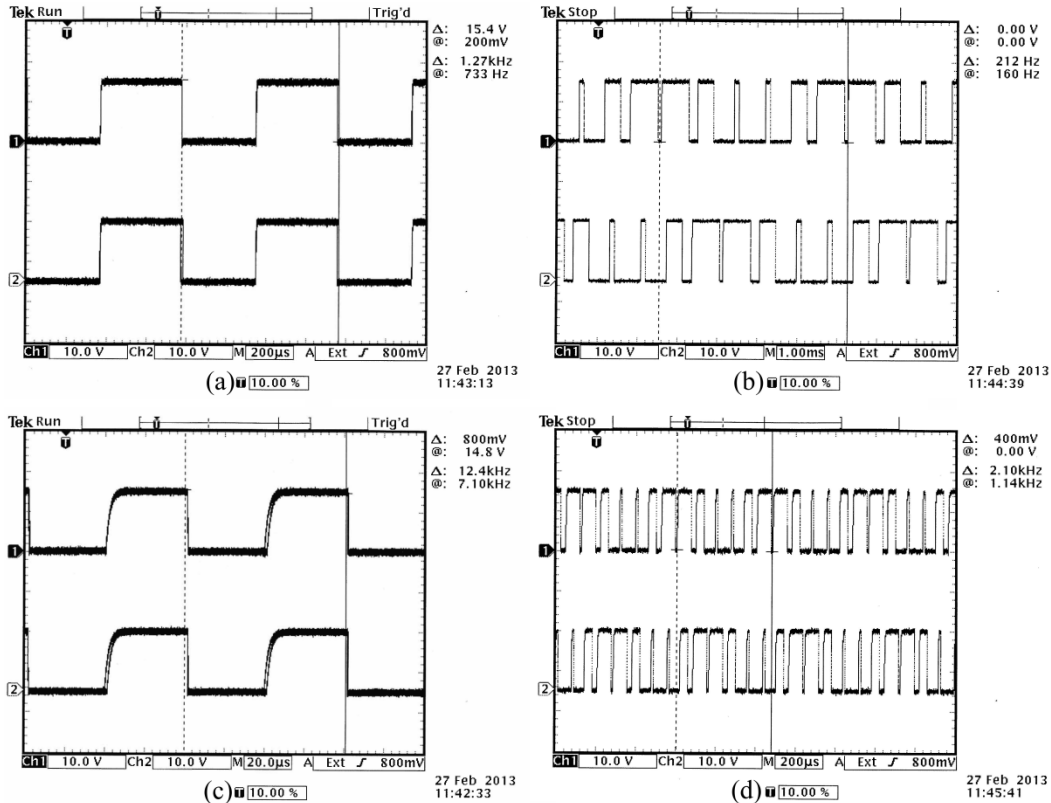
(a) $m = 0\%$ with $f = 1.27\text{kHz}$ (b) $m = 70\%$ with $f = 1.27\text{kHz}$

(c) $m = 0\%$ with $f = 12.4\text{kHz}$ (d) $m = 70\%$ with $f = 12.4\text{kHz}$

Figure 45.   Mod-6 SVM

2. Modulo-12

a. Counter and Six Pulse-train Generator

A wire-wrapped Mod-12 synthetic SVM unit can be seen in Figure 46. As expected, the modulo-12 counter produced twelve equally sized pulses with no time gaps or overlaps between the ending of one and the start of another. The pulse train generator produced six center-aligned pulse trains with a fifty percent duty cycle when the modulation control voltage is adjusted to 0V (minimum) equating to $m = 0\%$. When the modulation control voltage is adjusted to 15V (maximum), the six pulse trains are approximately ninety, seventy-four, fifty-eight, forty-two, twenty-six and ten percent duty cycles corresponding to $m = 65\%$. The analog frequency control is adjustable over

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the range of $227\text{Hz} \leq f \leq 5.32\text{kHz}$ (or $0\text{V} \leq V_f \leq 15\text{V}$). The circuit schematics may be found in Appendix C-1.
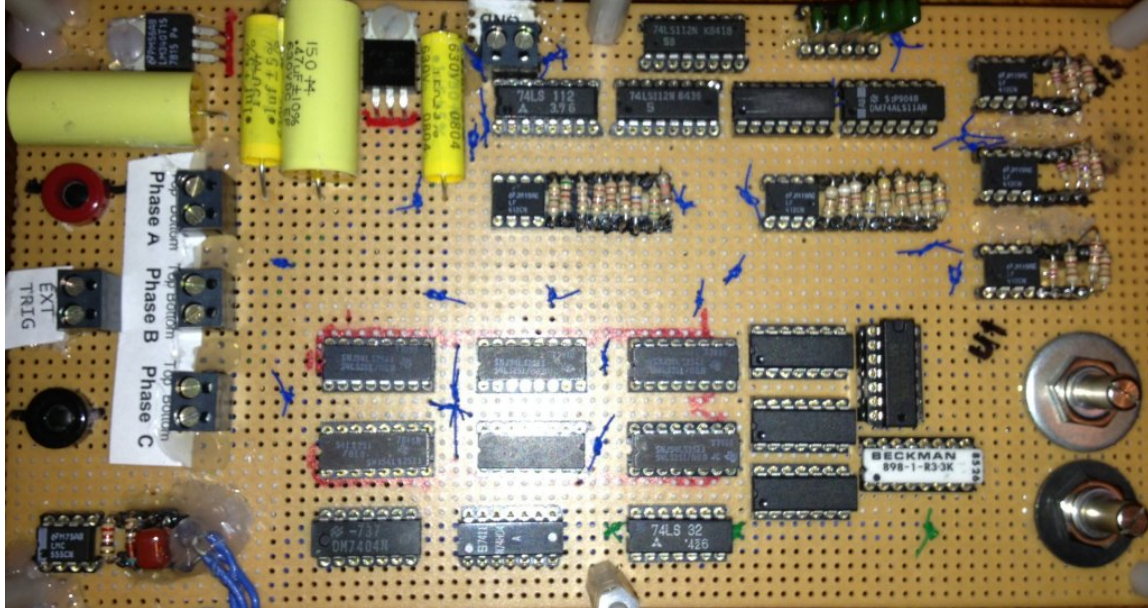

Figure 46.   Mod 12 bench top hardware.

b.   *Multiplexer and Turn-on Delays*

For the mod-12, wire-wrapped synthetic SVM circuit there were two (74251) multiplexer chips required per phase where twelve of the possible sixteen inputs are utilized. Further, the 74251 chips have both logic and inverse logic outputs. Unlike the simulation, the hardware contained turn-on delay (dead-time) as explained in Section II-C-3 and Appendix C-2.

d. Oscilloscope Results

Figure 47 shows plots for the "as built" hardware extremes for the mod 12 synthetic SVM unit. The requested frequencies were f = 434Hz to f = 5.3kHz while the requested modulations were $m = 0\%$ and $m = 65\%$.
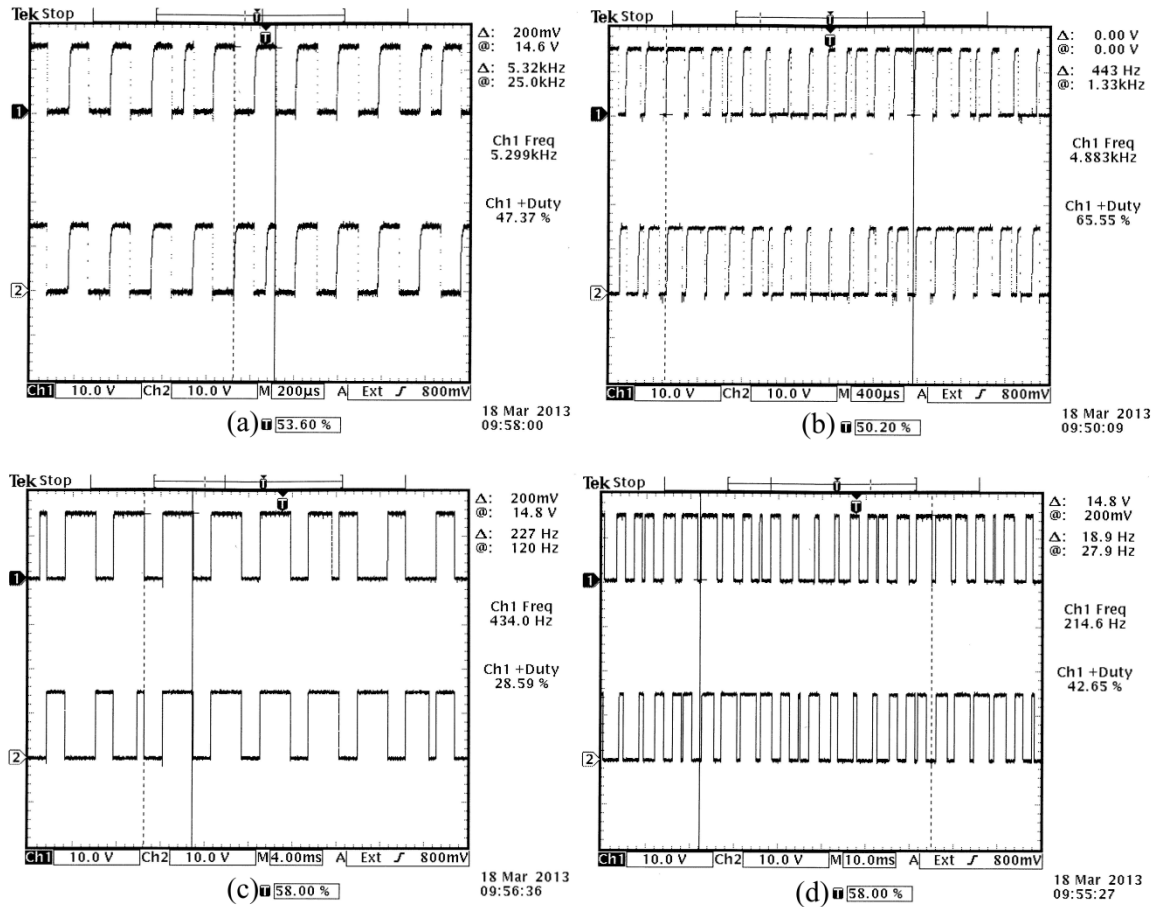
(a) $m = 0\%$ with $f = 227\text{Hz}$ (b) $m = 65\%$ with $f = 227\text{Hz}$

(c) $m = 0\%$ with $f = 5.32\text{kHz}$ (d) $m = 65\%$ with $f = 5.32\text{kHz}$

Figure 47.   Mod-12 SVM

B. SIMULATION IN SIMULINK™: (1) GENERAL CIRCUIT AND (2) VSI AND LOAD

The simulations of the modulo-6 and modulo-12 circuits have some structures in common that are presented in Figures 48 and 49. The general top view of the model is common to both as is the VSI and load. As shall be seen, the subsystem blocks marked "Signal Development," "Mod-N Clocking" and "Logic" are internally different for mod-6 and mod-12 versions of the simulation.
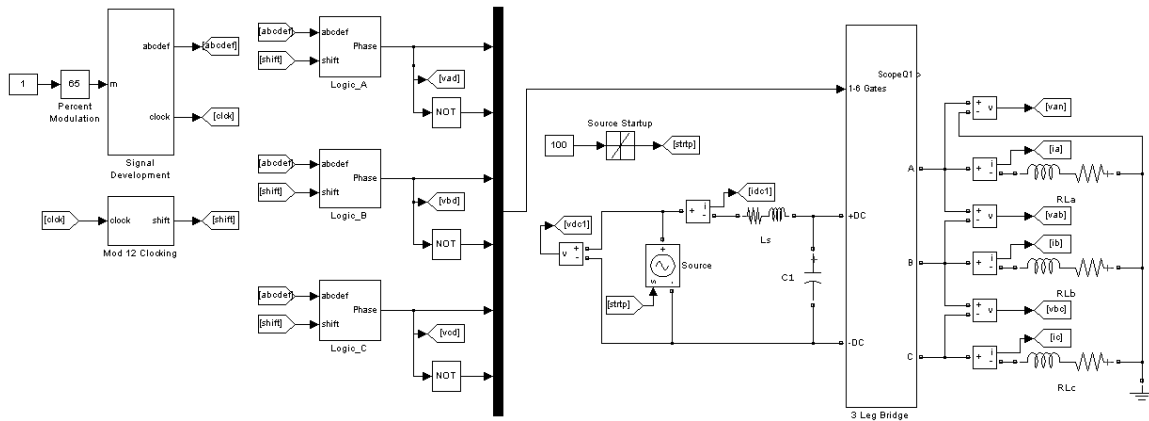

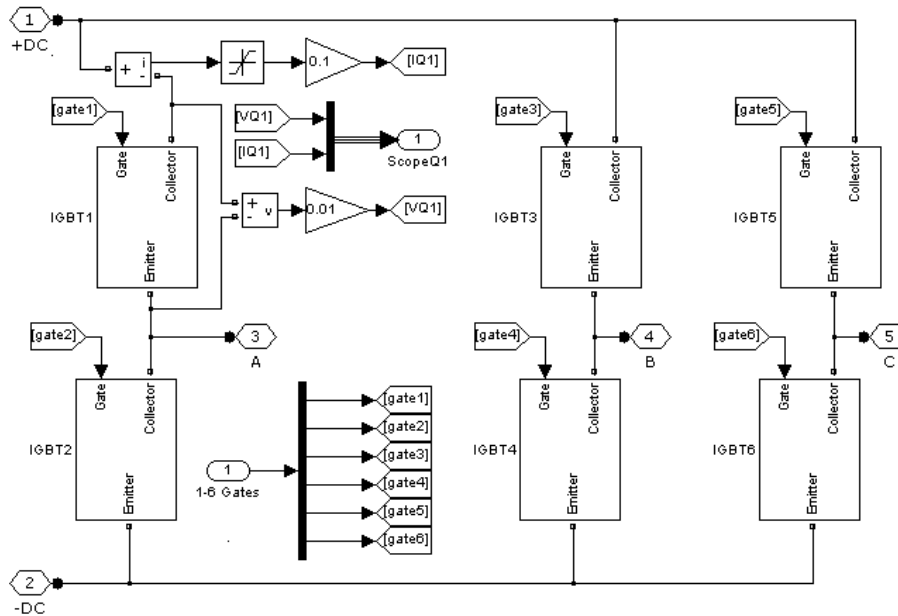Figure 48.   Top view of Simulink™ model for mod-6 or mod-12. From [5].

Figure 49.   The VSI subsystem block called "3-Leg Bridge." From [5].

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1.   Modulo-6 unit Design

a.   *Johnson Counter, Three Bit*

This counter synchronizes the multiplexers' input to output using the main clock signal as shown in Figure 50. Figure 51 depicts the output of the Johnson counter, which is three phase shifted signals used by the multiplexer logic. It operates at a switching frequency of exactly six times the desired output frequency of the VSI.
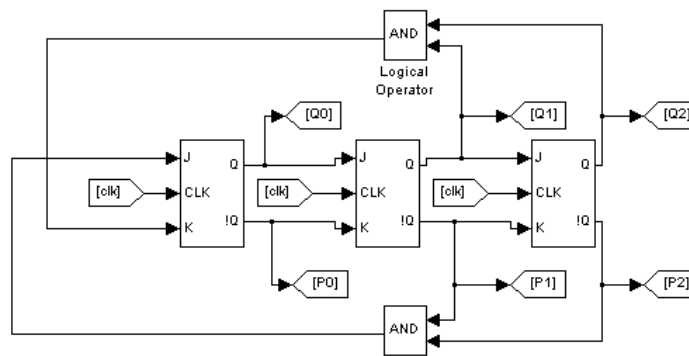

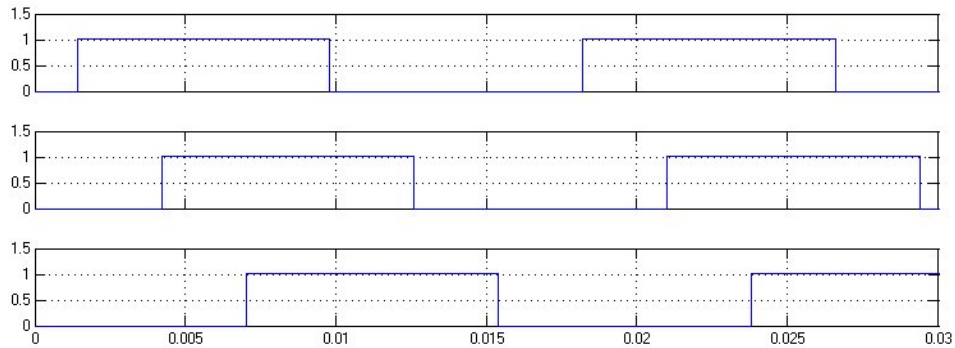Figure 50.   Three-bit Johnson counter for mod-6 simulation. From [5].

Figure 51.   Three-bit Johnson counter output for mod-6 simulation. From [5].

b.   *Generator, Three Center-aligned Pulse Trains*

The innards of the "Signal Development" subsystem block appear in Figure 52. The block produces a signal called "b" that remains at 50% duty cycle regardless of the modulation index or frequency. The other two input signals are adjustable with the first one handled by a slider control for modulation index and thefrequency may be changed by opening the triangle wave block and establishing new timing numbers. The sum of the low "c" and high "a" duty cycle signals is 1.0. Like the wire-wrapped version of the generator, the frequency is not affected by the modulation depth, nor is the modulation depth affected by the frequency.

It should be noted that a modulation depth of $m = 0$ should produce a duty cycle of 50% in all three signals and a fully adjusted modulation depth should produce three different signals of 99%, 50% and 1% duty cycles. The hardware (wire-wrapped) version was discussed in Chapter II Section A.2.a, which includes Figure 14. Furthermore, the circuit simulation may be examined in Appendix D-2.
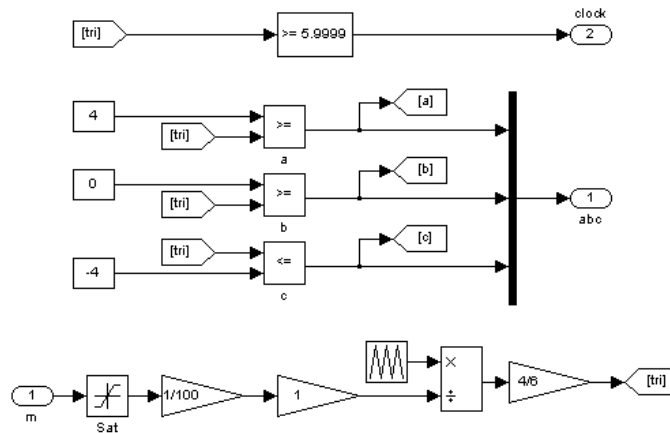

Figure 52.   Signal development subsystem for mod-6 simulation. From [5].

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c. *Multiplexer Shifter and Logic, Six Input*

A time division multiplexer (as opposed to a frequency division multiplexer) has no readily available equivalent in Simulink™. It was therefore built from basic logic in two separate pieces as contained within the "Mod-6 Clocking" block and the "Logic" blocks.   The shift portion is contained within the mod-6 clocking block and is common to all three-phases. The remaining individual logic for each phase in contained in the individual subsystems named Logic_A, Logic_B and Logic_C. Figure 53 contains the shifter and logic for phase A. Furthermore, a sequence of subsystem blocks is available in Appendix D.
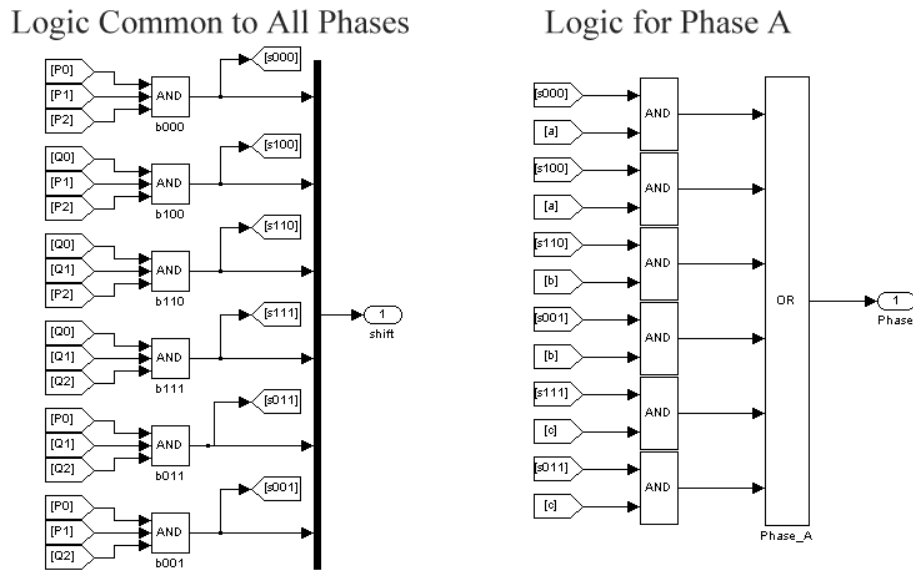

Figure 53.   Model equivalent multiplexer for mod-6 phase A. From [5].

e. *VSI Gating Signal and Output*

The three-phase multiplexer outputs are available at the "Phase" terminals of the Logic blocks as seen in Figure 48 and displayed in Appendix D. In reality, the three outputs are the gating signals for the upper three switches in the VSI. The lower three switches are gated using logic inversion of the upper switch signals. No matter how good the circuit looks, the real information is in how it acts. In six pulses, it cycles through the SVM "alternating-reversing" switching waveform in Chapter II Section

B.2.b.4. Simulated VSI output waveforms (V_{AN}, V_{AB}, I_A and I_B) are available for viewing in Appendix D.

2.   Modulo-12 Unit Design

a.   *Johnson Counter, four-bit*

This counter synchronizes the multiplexers' input to output using the main clock signal as shown in Figure 54. Note, the mod-12 simulation requires one additional flip-flop (compared to mod-6 unit) for realization. The top portions of Figures 50 and 54 are identical except for labeling. Figure 55 depicts the output of the Johnson counter, which is four phase-shifted signals used by the multiplexer logic. It operates at a switching frequency of exactly twelve times the desired output frequency of the VSI.
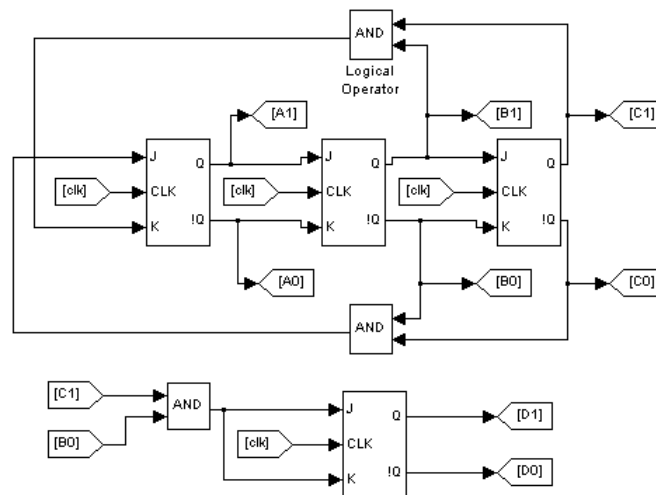

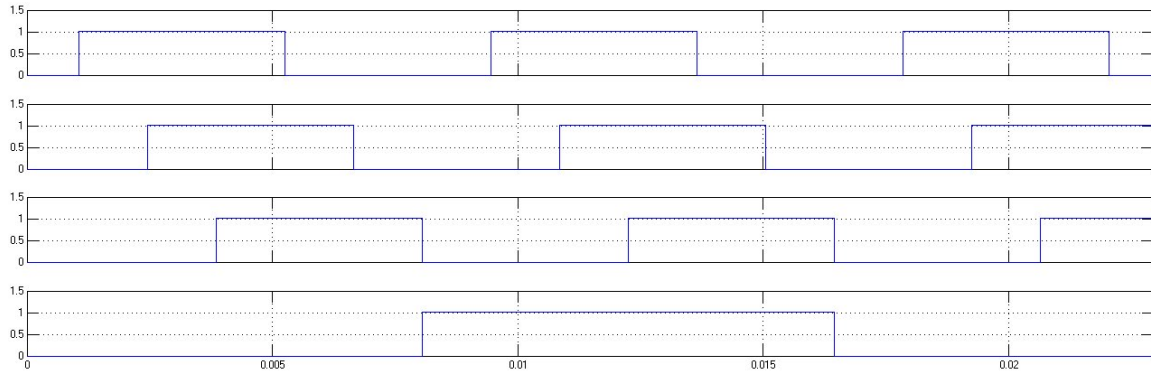Figure 54.   Four-bit Johnson counter for mod-12 simulation. From [5].

Figure 55.   Four-bit Johnson counter output for mod-12 simulation. From [5].

b.   *Generator, Six Center-aligned Pulse Trains*

The details of the "Signal Development" subsystem block appear in Figure 56. The six signals ("a" through "f") may be adjusted by a single slider the control modulation index. The frequency may be changed by opening the triangle wave block and establishing new timing numbers. The signals are grouped in additive pairs ($a + f = 1$, $b + e = 1$ and $c + d = 1$) such that the sum of the low and high duty cycle signals equals '1.0'. Like the (wire-wrapped) hardware version of the generator, the frequency is not affected by the modulation depth, nor is the modulation depth affected by the frequency.

Note, a modulation depth of $m = 0$ should produce a duty cycle of 50% in all six signals and a fully adjusted modulation depth should produce three different signals having 99%, 79.2%, 59.4%, 40.6%, 20.8% and 1% duty cycles in each. The hardware version was discussed in Chapter II Section A.2.a, which includes Figure 14. Furthermore, the circuit simulation is included in Appendix D.
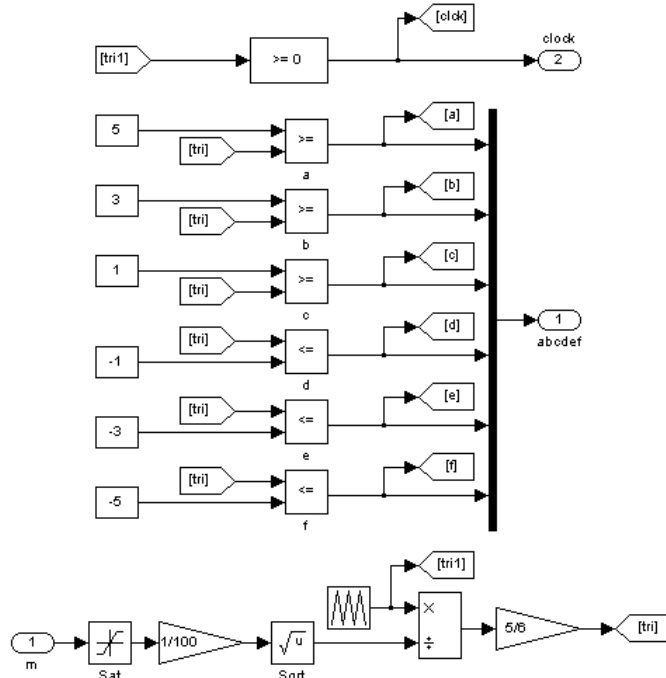
Figure 56.   Signal development subsystem for mod-12 simulation. From [5].

c.   *Multiplexer Shifter and Logic, Twelve Input*

A time division multiplexer (as opposed to a frequency division multiplexer) has no readily available equivalent in Simulink™. It was therefore built from basic logic in two separate pieces contained in the "Mod-12 Clocking" block and the "Logic" blocks.   The shift portion is contained within the mod-12 clocking block and is common to all three-phases. The remaining individual logic for each phase in contained in the individual subsystems named "Logic_A," "Logic_B" and "Logic_C." Figure 57 contains the shifter and logic for phase A. Furthermore, a sequence of subsystem blocks is available in Appendix E.
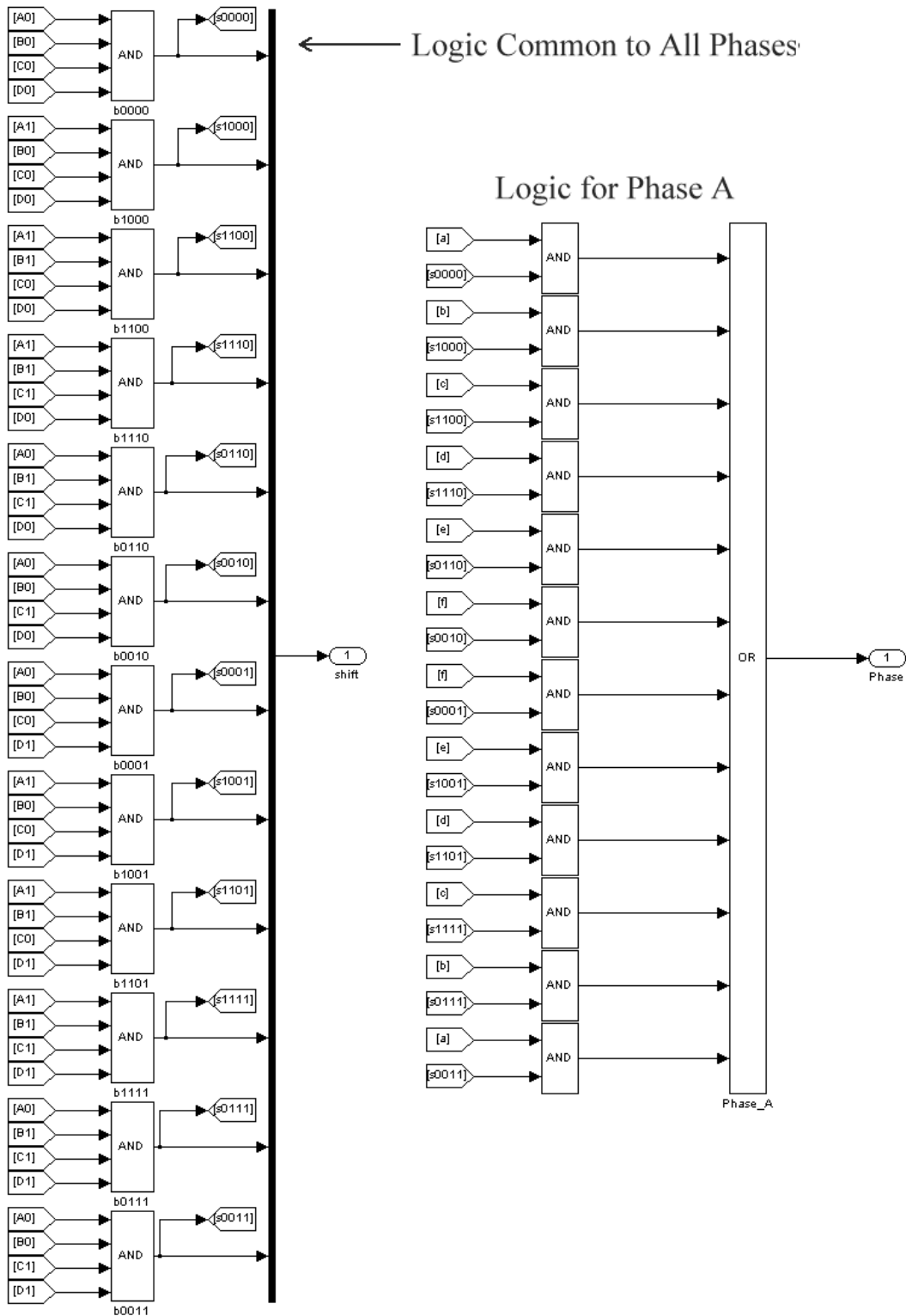
Figure 57. Model equivalent multiplexer for mod-12 phase A. From [5].

d. VSI Gating Signal and Output

The three-phase multiplexer outputs are available at the "Phase" terminals of the Logic blocks as seen in Figure 48 and displayed in Appendix E. In reality, the three outputs are the gating signals for the upper three switches in the VSI. The lower three switches are gated using logic inversion of the upper switch signals. No matter how good the circuit looks, the real information is in how it acts. In twelve pulses, it cycles through the SVM "alternating-reversing" switching waveform in Chapter II Section B.2.b.4. Simulated VSI output waveforms (V_{AN}, V_{AB}, I_A and I_B) are in Appendix E.

IV. REMARKS AND CONCLUSIONS

A. SPACE VECTOR MODULATION

In the literature, claims are made that "SVM closely resembles center-aligned PWM" [1]. Upon examination, the SVM Alt-Rev switching sequence looked like it could be reproduced (mimicked) by three multiplexed center-aligned pulse trains. Because the synthesized waveforms produced by the hardware built for this thesis are identical to the SVM switching waveforms, it became apparent that PWM equipment is not necessary for the production of SVM in spite of what the literature seems to claim.

Synthetic SVM signals exhibit a fixed relationship between the fundamental frequency and the switching frequency. PWM, on the other hand, generally has a switching frequency that is somewhat independent of the modulation frequency. For relatively low switching to fundamental frequency ratios, the pulse count for each half-cycle of the fundamental is locked to the switching frequency. The carrier (switching) frequency is therefore floating around some ideal center value that permits odd integer numbers of pulses per half cycle. These two methods are therefore inherently different in philosophy.

For synthetic SVM at any motor rotational speed, the speed limit becomes the modulo number (N) times the output fundamental frequency ($f_{\max} = Nf_{out}$) where $f_{\max}$ is the switching limit of the VSI. Space vector modulation may be beneficial for high speed motor operations where VSI limits are a concern.

1. Third Harmonic Injection PWM Versus SVM

The Alt-Rev switching scheme as presented in the synthetic SVM machine is inherently simpler than a third-harmonic injection PWM scheme. Traditional PWM schemes require a template adjustment where SVM inherently promotes third ordered harmonic injection $(3,9,15,27,...)$. As previously discussed, third harmonic injection allows for better DC bus utilization. For more discussion on the equivalency between various methods see [7].

2.   SVM Switch Stress Reduction

a.   *Minimized Switch Transitions (Gray Code) Per Cycle*

From the literature, some of the SVM switching sequences involve synchronous switching [1]. When the mentioned sequences are translated into center-aligned pulse train versions, they take on Gray code like characteristics where only one switch transition takes place at any one moment. Therefore, it produces a minimum number of switches per cycle.

b.   *Losses Versus Switching Frequency*

Before SVM was developed, PWM was routinely used. As stated before, an accurately reproduced sine wave depended on a high frequency triangle wave, where switching losses increase linearly with frequency. Further, it is obvious that the speed of the control algorithm is limited by the switching frequency and the switching frequency is limited by acceptable losses [4]. In conclusion, SVM in general limits switching losses beyond that of typical PWM.

B.   DEADTIME DISTORTION

The switching times between a pair of transistors in any leg of a VSI is critical in several ways. (1) Simultaneously conducting transistor pairs create a "shoot-through" condition resulting in a high current path. This condition is to be avoided as it generally results in switch failure. (2) Generally, simultaneously non-conducting pairs produce harmonic distortion (or in mechanical terms torque pulsations) in a three-phase VSI.

Compromise methods for handling both problems seem to be centered on three areas. First, a purely software method involves the minimization of distortion via PWM-centric software like the that developed by two Motorola engineers for an MC68HC708MP16 project in [1]. Secondly, a combo software and hardware method uses loaded periphery registers with an optimal deadtime as in [12]. Thirdly, a hardware only solution insures the turn-on delay for the switch pair eliminating simultaneously 'on' states [2]. Because the synthetic SVM unit has no CPU, neither method (1) or (2) will work. Deadtime on

the synthetic SVM unit is handled by method (3). The turn-on delay uses an open collector logic gating or a comparator (normally used with a pull-up resistor) with a capacitor to create the turn-on delay as previously discussed in this thesis.

C.   SIGNAL SYNTHESIS VERSUS SOFTWARE GENERATION

Familiarity with microcontrollers, assembly language, digital systems and signal synthesis led to the novel approach that the SVM switching signals could be mimicked with hardware only. Traditionally, SVM has been realized using a CPU and a significant amount of software or FPGA centric systems. Although others have noted that as long as SVM-like hardware systems produce equivalent gating signals to the VSI, and the up-stream and down-stream equipment cannot discern the difference, an equivalency has been found. This thesis presents an equivalent hardware solution.

D.   FUTURE WORK

With a VSI and controller equipped with the latest in SVM switching schemes, it should be possible to replace variable speed DC motors with high-efficiency, high-torque, reliable three-phase induction machines. In other words, it should be possible to replicate the DC motor characteristics with properly controlled AC machines. What follows are some possible control strategies and methods of analysis.

1.   Indirect Field-oriented Control

Linearizing a problem around an equilibrium point in a differential format generally produces good solutions for a large number of systems. The process inevitably assumes some of the variables in the differential matrices are constant. For instance, if the inductances in an induction machine are assumed to be constant, winding currents can be used as proxies for magnetic field strength. Using this proxy in a control system would be considered Indirect Field-Oriented Control. This linearizing assumption allows the use of low cost current sensors rather than problem-prone magnetic field strength sensors. Other available sensed parameters include rotor speed ω_{Rotor} and stator current i_{Stator}. Other available motor parameters might include the inputs of synchronous speed

$\omega_{Synchronuous}$ and stator voltage v_{Stator}. The resulting total differential equation might appear as follows:

$$\Delta i_{Rotor} = a_1 \Delta \omega_{Rotor} + a_2 \Delta i_{Stator} + a_3 \Delta \omega_{Synchronous} + a_4 \Delta v_{Stator} \quad (6)$$

where $a_1 = (\partial i_{Rotor} / \partial \omega_{Rotor})$, $a_2 = (\partial i_{Rotor} / \partial i_{Stator})$, $a_3 = (\partial i_{Rotor} / \partial \omega_{Synchronous})$, and

$a_4 = (\partial i_{Rotor} / \partial v_{Stator})$. The partial differentials a_1, a_2, a_3 and a_4 should look somewhat familiar to those acquainted with thermal analysis or transistor stability factor analysis [15]. If the "total differential can be used in "thermal analysis" or "stability factor analysis" it might be useful for some version of a motor controls scheme.

2. Jacobians Applied to Feedback

With ever increasing budget constraints, engineers are often called upon to produce physically realizable products within ever tightening economical constraints. That being so, it might be a good idea to re-investigate old ideas used in new ways and take advantage of relatively unsophisticated, but rugged sensors providing relatively maintenance-free operation. It could easily be that a Jacobian matrix feedback system similar to [16] would produce good results. "In a small neighborhood near a system's equilibrium point, a non-linear system behaves like a linear system" [17].

On an induction motor without unusual sensors or equipment, the easily available inputs are source voltage and frequency at the winding terminals. The motor outputs tell us motor loading conditions and behavior. The outputs that can easily be collected are shaft rotational speed ω_{ROTOR} and stator current i_{STATOR} while mapping these to loading. In fact, the Jacobian matrix in (7) may be used for the induction motor control system of Figure 58. The Jacobian representation is:

$$\begin{bmatrix} \Delta v_{STATOR} \\ \Delta \omega_{SYNCHRONOUS} \end{bmatrix} = \begin{bmatrix} \partial v_{STATOR} / \partial \omega_{ROTOR} & \partial v_{STATOR} / \partial i_{STATOR} \\ \partial \omega_{SYNCHRONOUS} / \partial \omega_{ROTOR} & \partial \omega_{SYNCHRONOUS} / \partial i_{STATOR} \end{bmatrix} \begin{bmatrix} \Delta \omega_{ROTOR} \\ \Delta i_{STATOR} \end{bmatrix} \quad (7)$$

where $\Delta \omega_{ROTOR}$ is rotor speed error and Δi_{STATOR} is stator current error.
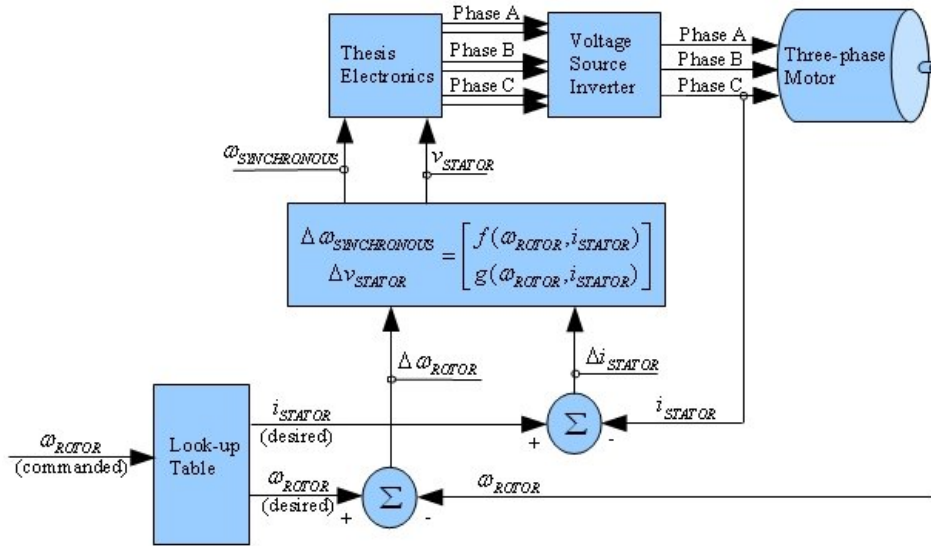
Figure 58.   A sample Jacobian feedback scenario.

3.   Transient Analysis of Synthetic SVM Circuit

Modulo-6 and mod-12 bench-top hardware units were designed, constructed and rudimentarily tested. A block diagram of a synthetic SVM System appears in Figure 59 where either hardware unit can be inserted in the "Thesis Electronics" block. This allows for easy comparison between units. As originally devised, the thesis units featured herein have potentiometer inputs for frequency and modulation-depth. Ideally, these inputs should be supplanted by an electronic input and a feedback system providing that input as depicted in Figure 59 and tested. The testing should include fixed and dynamic loading to evaluate transient response and stability.
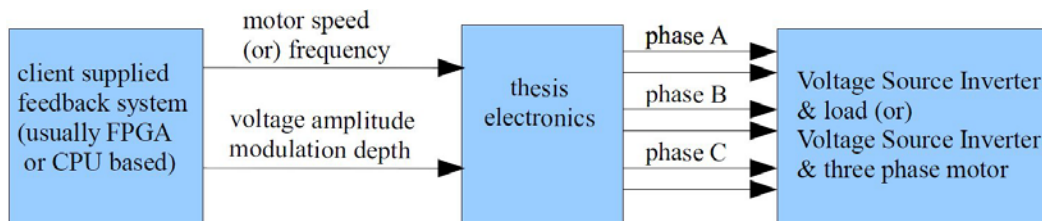
Figure 59.   Block diagram of synthetic SVM system.

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Since a closed-loop control system was not developed due to time constraints, the insertion and mathematical evaluation would be beneficial for the realization of a usable system. References on potential control systems and methods may be found in [17] through [19].

4. Potential Benefits of Synthetic SVM

Because of the inherent design of the synthetic SVM unit, it is believed that certain benefits will be derived. Many of the benefits listed below are a direct result of the fact that the hardware does not require a CPU, FPGA or software.

(1) Reliability: Although not provable, the simplicity of the logic based hardware should be more reliable than a software based system.

(2) Cost: Without a CPU, FPGA or software, the cost is dramatically reduced from a conventional SVM unit.

(3) Maintenance: Other than potentially cleaning cooling fins, there is little to maintain. There is no software upgrade required, since there is no software.

(4) Expandability: As seen with the hardware and modeling effort, the synthetic SVM methods can be expanded from mod-6 to mod-N

where N is an even integer and an unexplored number of output phases.

APPENDIX

A.   RELEVANT DATASHEETS

1.   Open Collector Inverter

FAIRCHILD
SEMICONDUCTOR™

August 1986
Revised March 2000

DM74LS05
Hex Inverters with Open-Collector Outputs

General Description

This device contains six independent gates each of which performs the logic INVERT function. The open-collector outputs require external pull-up resistors for proper logical operation.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_{CC}\,(Min) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_{CC}\,(Max) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$
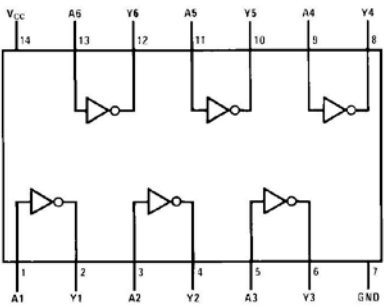
Where: $N_1\,(I_{OH})$ = total maximum output high current for all outputs tied to pull-up resistor

$N_2\,(I_{IH})$ = total maximum input high current for all inputs tied to pull-up resistor

$N_3\,(I_{IL})$ = total maximum input low current for all inputs tied to pull-up resistor

Ordering Code:

Order Number	Package Number	Package Description
DM74LS05M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
DM74LS05SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
DM74LS05N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram

Function Table

$Y = \overline{A}$

Input	Output
A	Y
L	H
H	L

H = HIGH Logic Level
L = LOW Logic Level

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2. Dead Time Insertion

18.7 Dead-Time Generators

In power inverter applications, where the PWMs are used in Complementary mode to control the upper and lower switches of a half-bridge, a dead-time insertion is highly recommended. The dead-time insertion keeps both outputs in inactive state for a brief time. This avoids any overlap in the switching during the state change of the power devices due to T_{ON} and T_{OFF} characteristics.

Because the power output devices cannot switch instantaneously, some amount of time must be provided between the turn-off event of one PWM output in a complementary pair and the turn-on event of the other transistor. The PWM module allows dead time to be programmed. The following sections explain the dead-time block in detail.

18.7.1 DEAD-TIME INSERTION

Each complementary output pair for the PWM module has a 6-bit down counter used to produce the dead-time insertion. As shown in Figure 18-17, each dead-time unit has a rising and falling edge detector connected to the duty cycle comparison output. The dead time is loaded into the timer on the detected PWM edge event. Depending on whether the edge is rising or falling, one of the transitions on the complementary outputs is delayed until the timer counts down to zero. A timing diagram, indicating the dead-time insertion for one pair of PWM outputs, is shown in Figure 18-18.

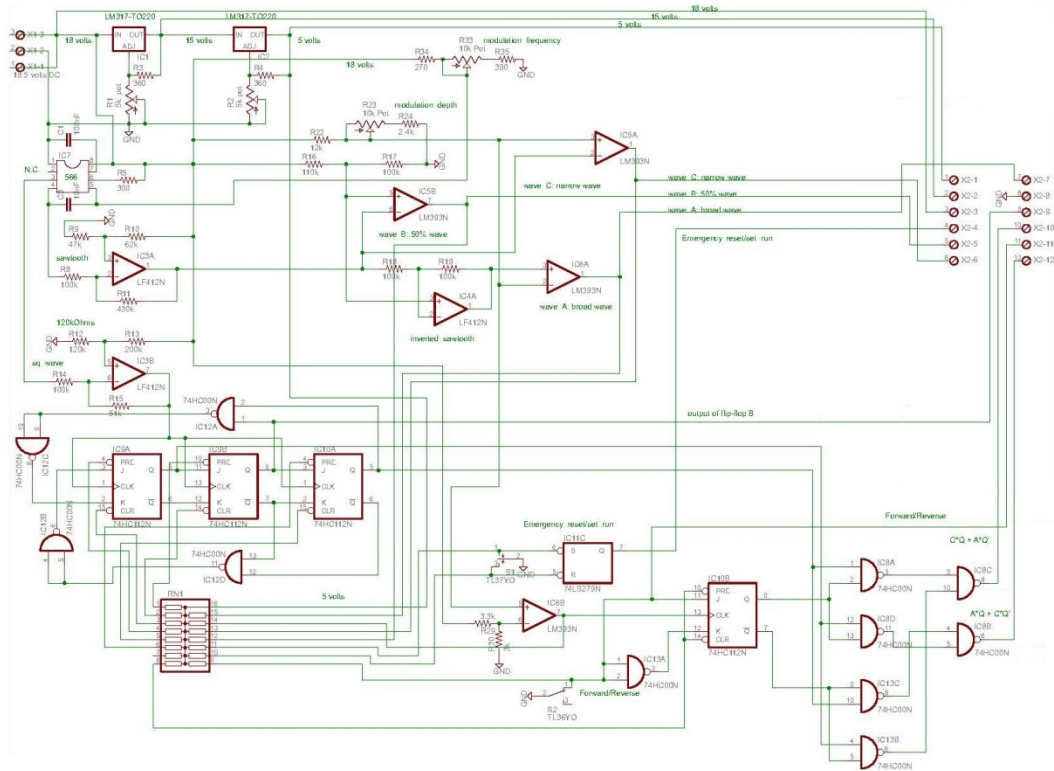**FIGURE 18-17: DEAD-TIME CONTROL UNIT BLOCK DIAGRAM FOR ONE PWM OUTPUT PAIR**
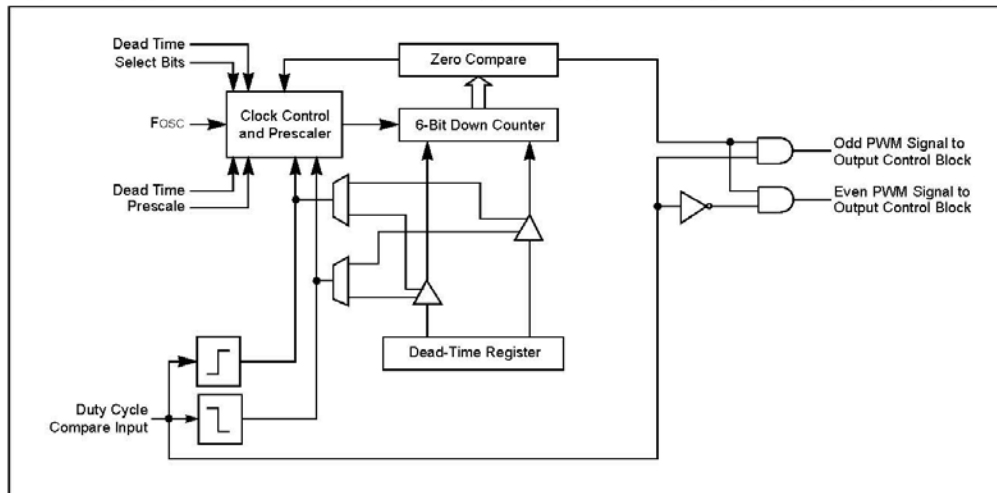
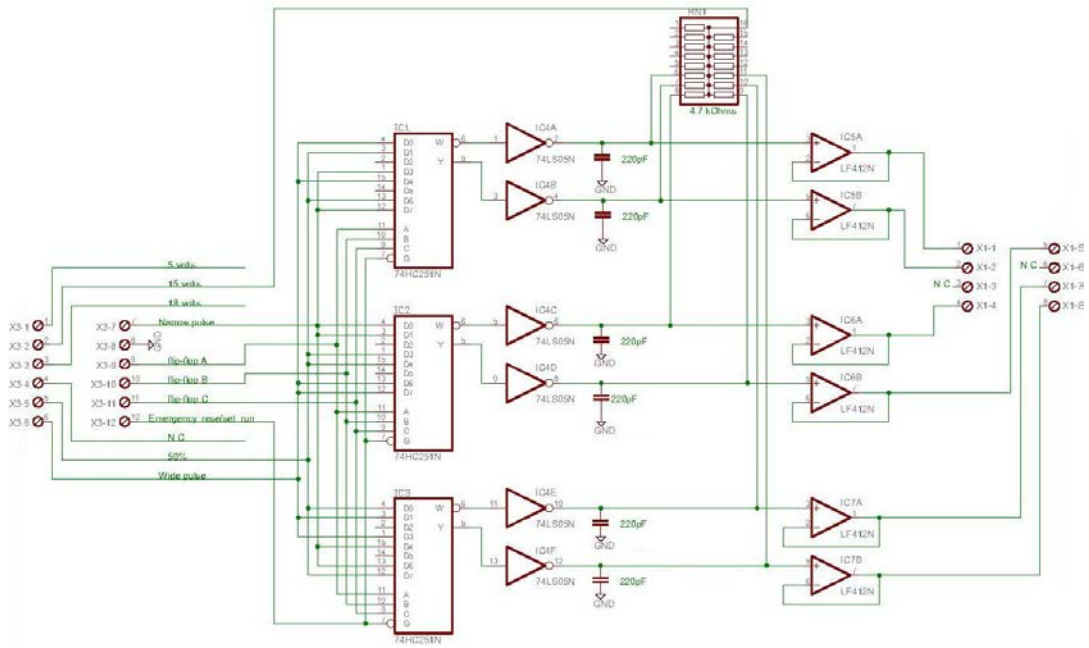**FIGURE 18-18: DEAD-TIME INSERTION FOR COMPLEMENTARY PWM**

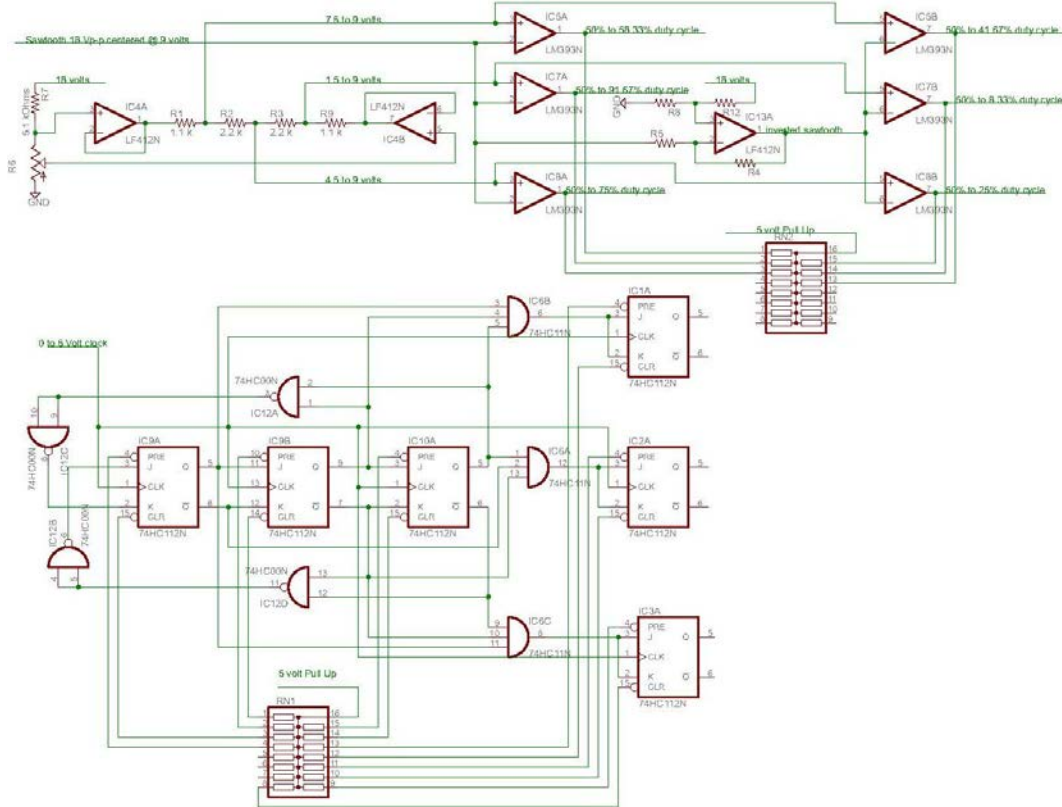## 1.   Mod-6 Counter and Three Pulse-train Generator

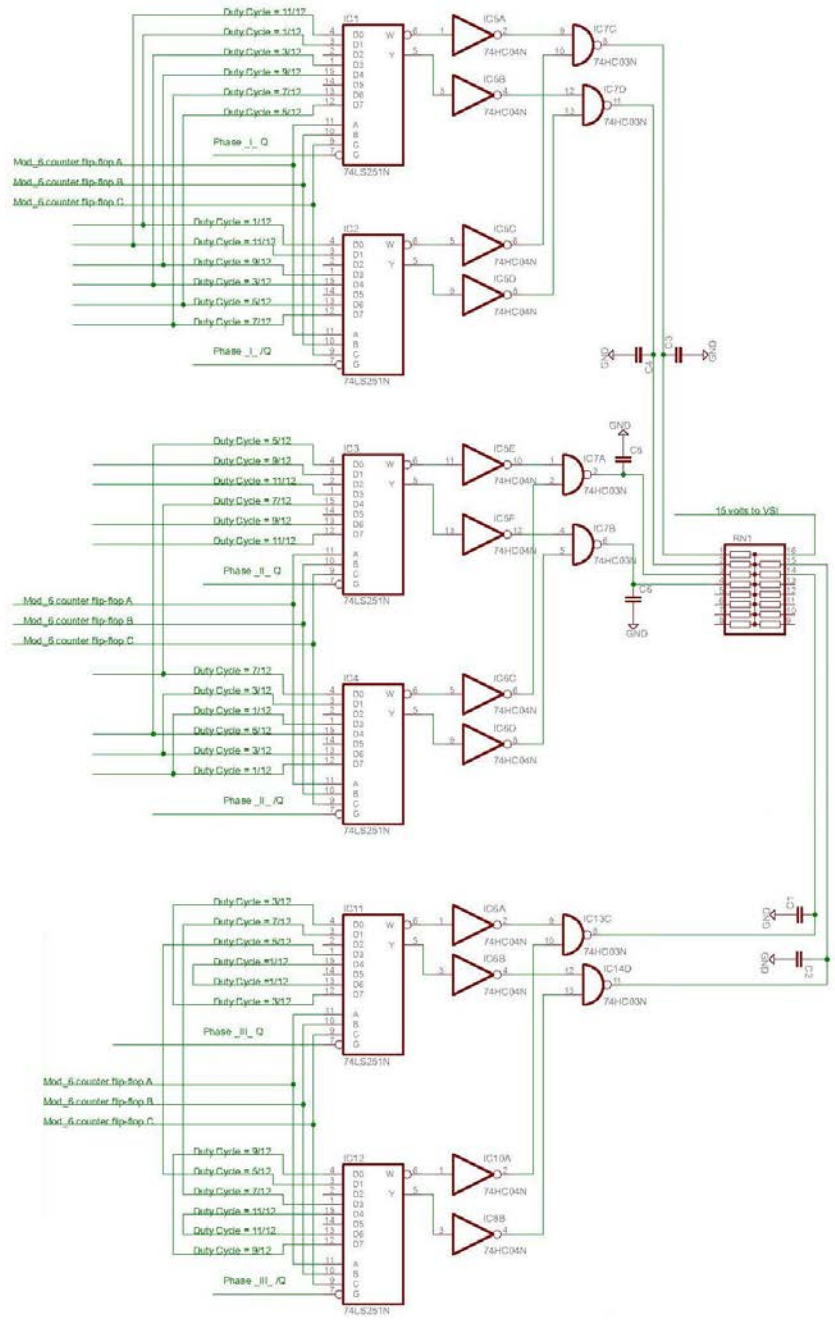## 2.   Three Pulse-Trains Multiplexed into Three Phases

C. MOD-12, SYNTHETIC-SVM, PRINTED CIRCUIT PLANS
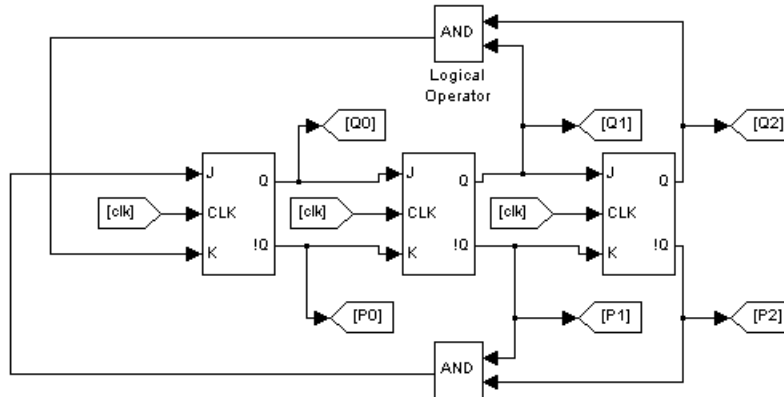
1. Mod-12 Counter and Six Pulse-Train Generator

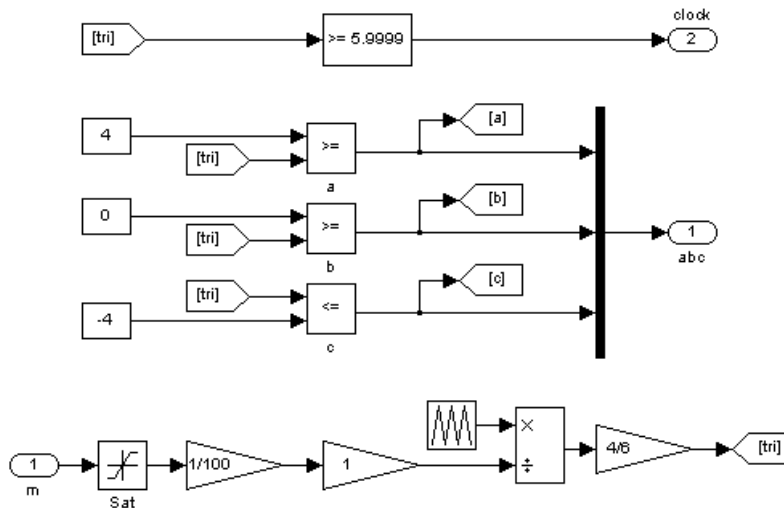## 2.   Six Pulse-Trains Multiplexed into Three Phases

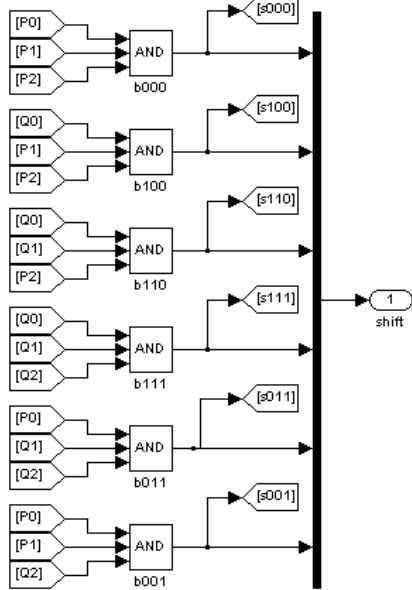## D.   MOD-6, SIMULATED SYNTHETIC-SVM

1.   Johnson Counter, 3-Bit

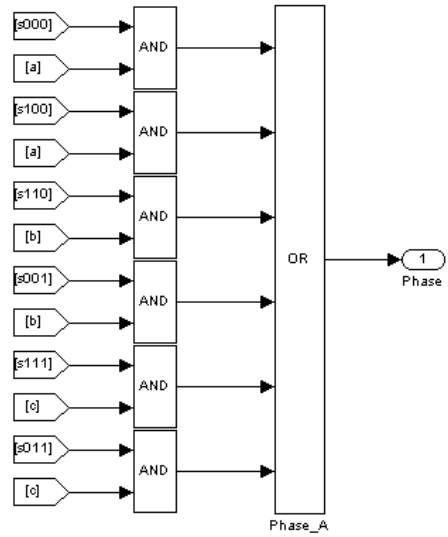### 2.   Signal Generator, Three Center-Aligned Pulse Trains
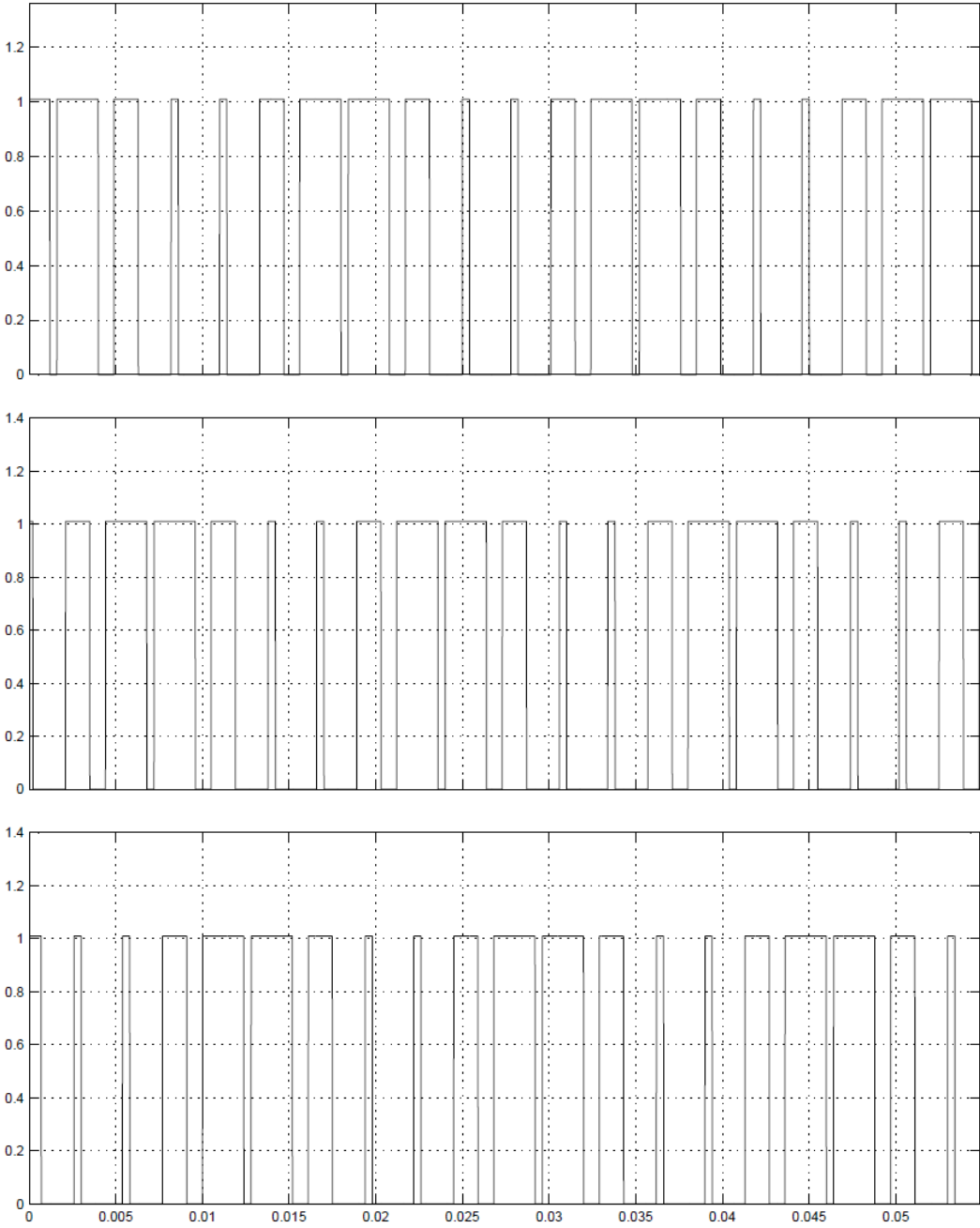
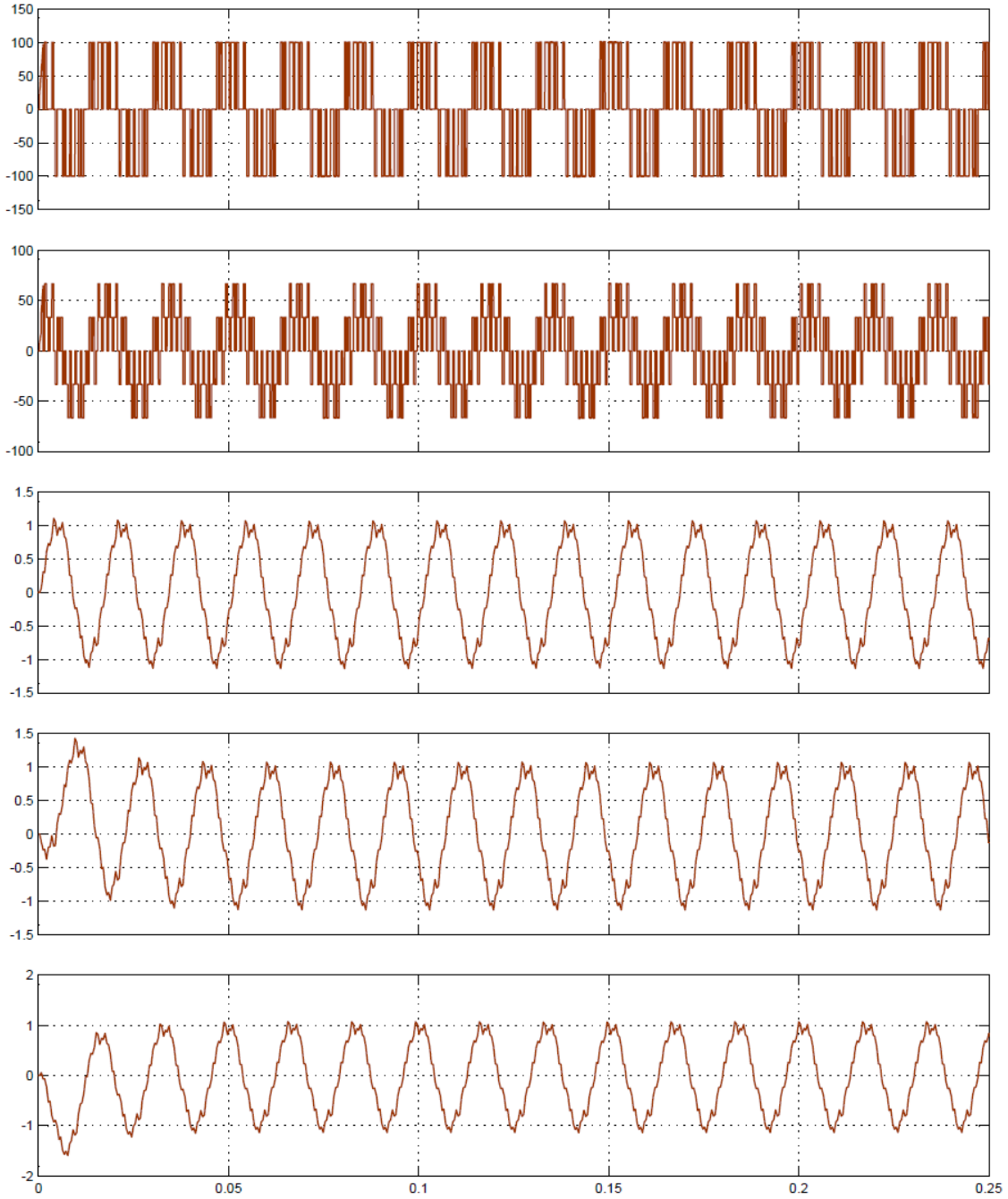### 3. Multiplexer, Six Inputs Per Phase

Logic Common to All Phases

Logic for Phase A
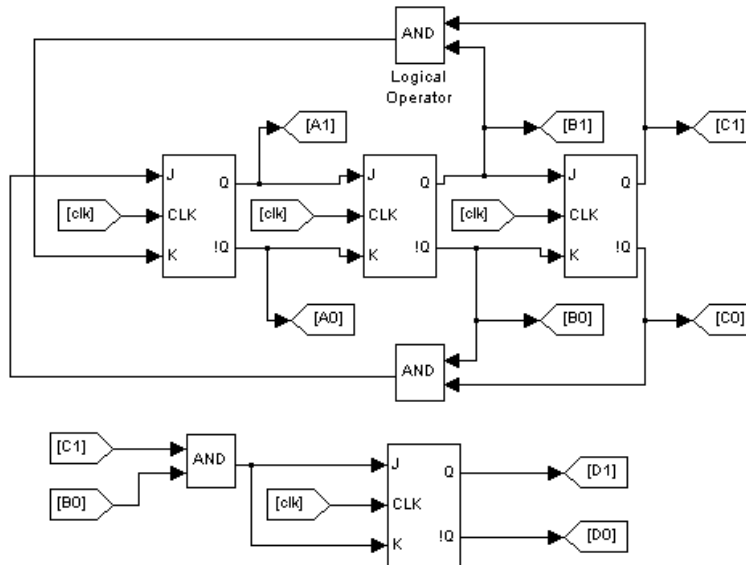
4.   Gating Signals for Upper Switches in VSI

5. **Selected Output Voltages and Currents:** V_{AN}, V_{AB}, I_A, I_B **and** I_C
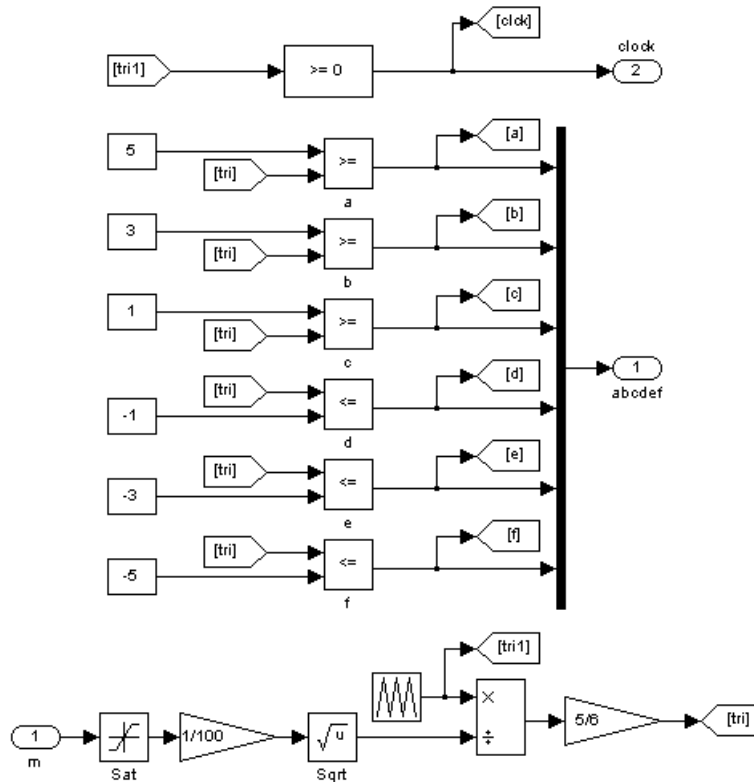
E. MOD-12, SIMULATED SYNTHETIC-SVM
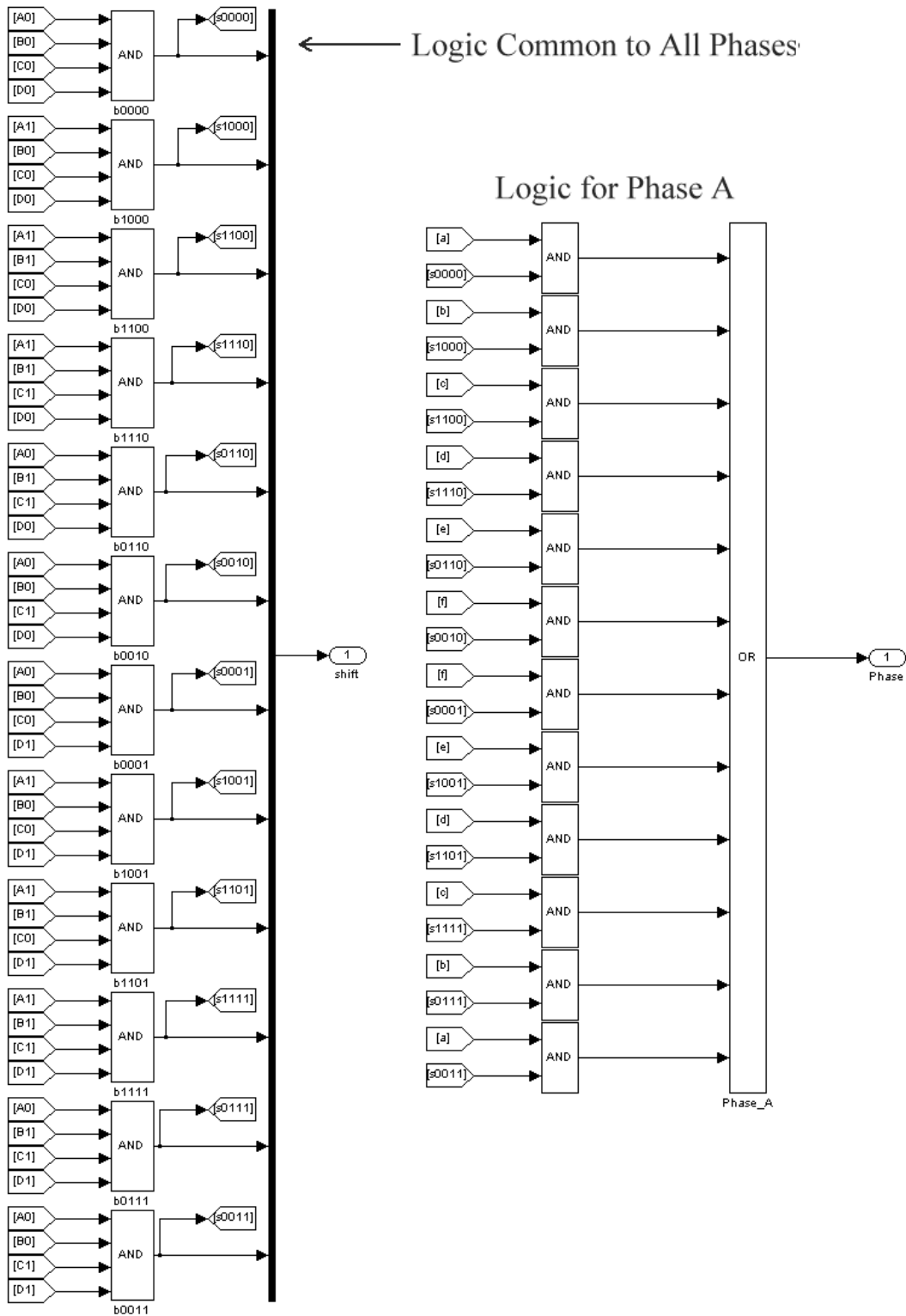
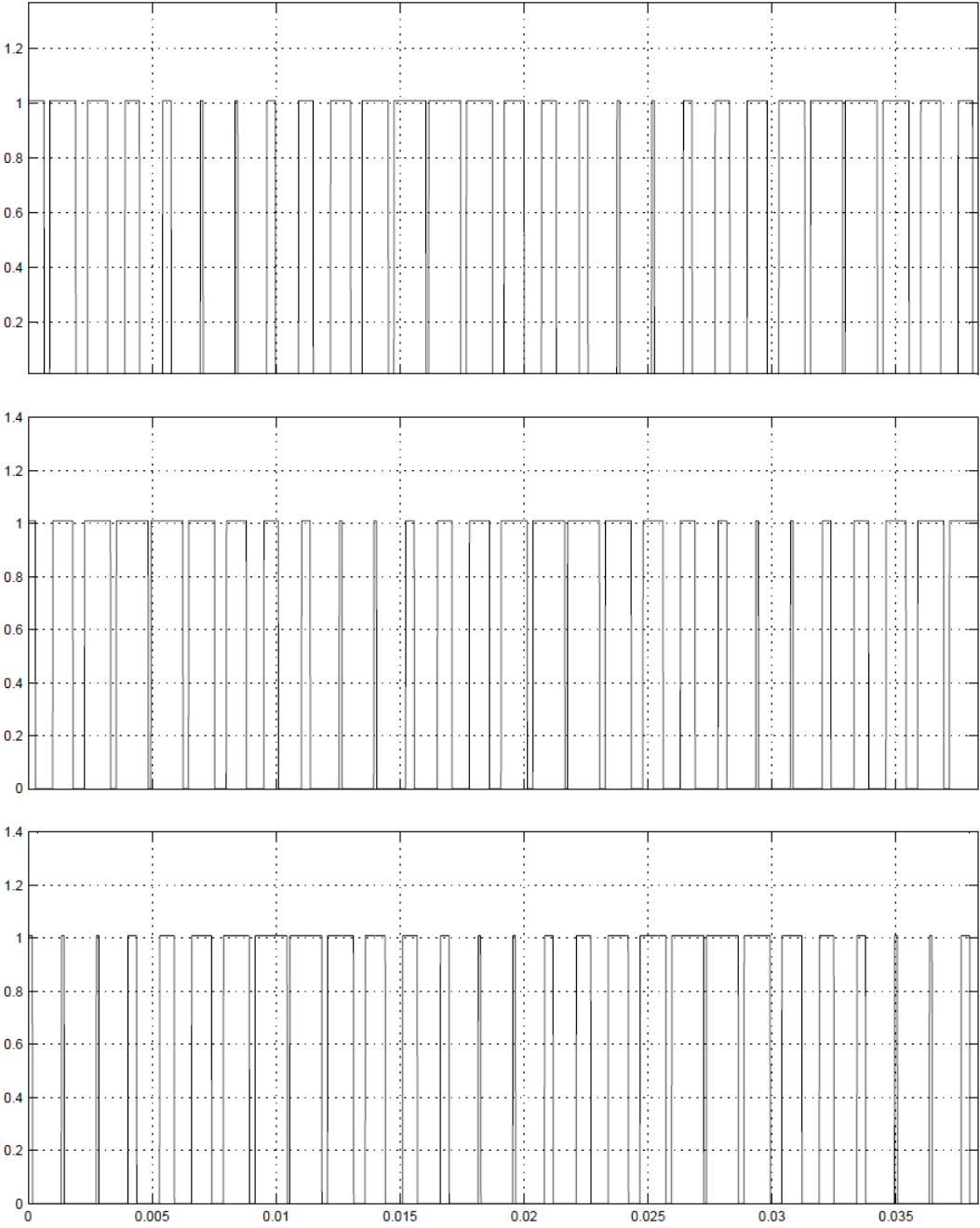### 1. Johnson Counter, 4-Bit

2.   Signal Generator, Six Center-Aligned Pulse Trains
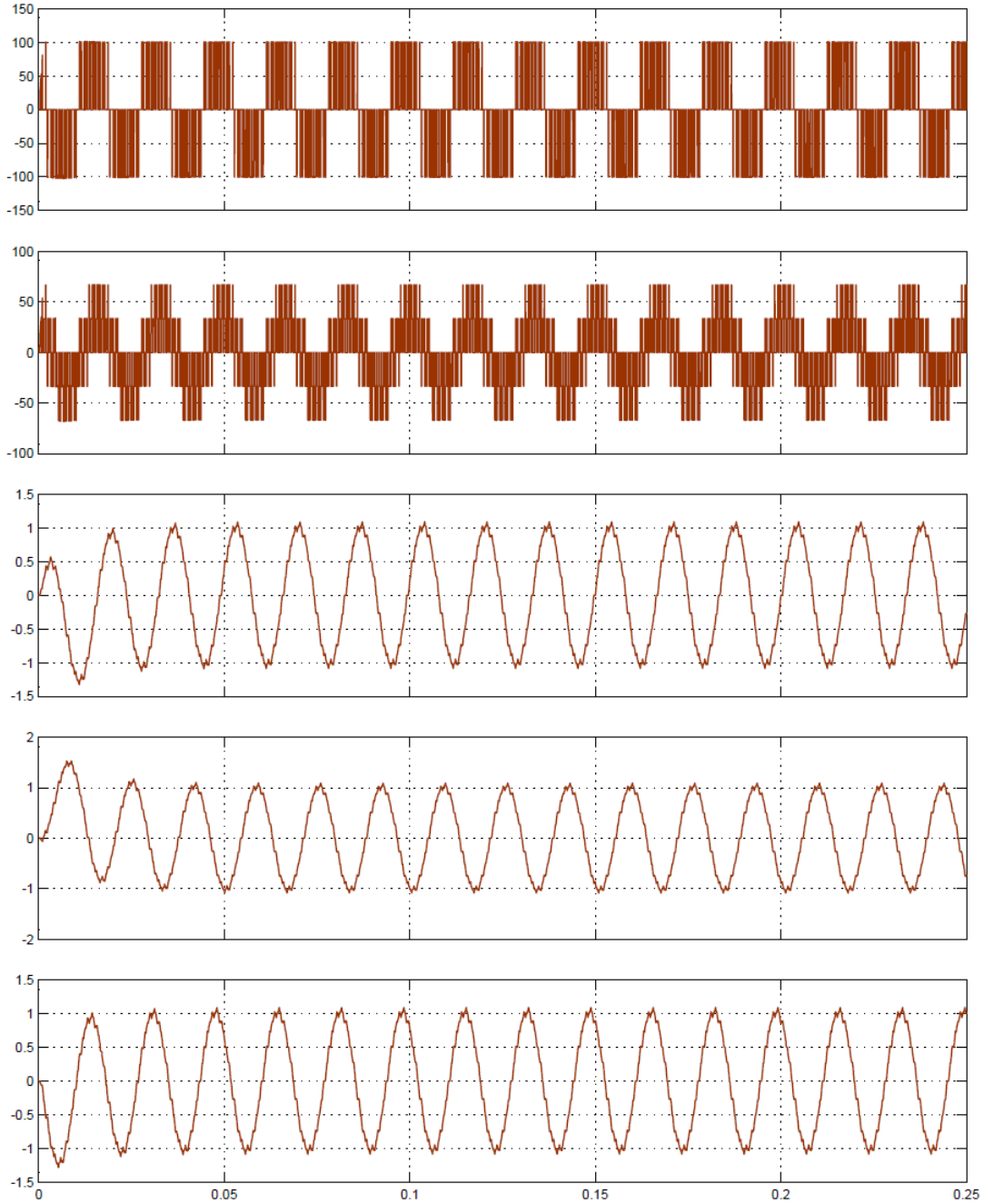
3. Multiplexer, Twelve Inputs Per Phase

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4. **Gating Signals for Upper Switches in VSI**

5. Selected Output Voltages and Currents: V_{AN}, V_{AB}, I_A, I_B and I_C

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