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SIMULATING AND TESTING A DC-DC HALF-BRIDGE SLR CONVERTER

by

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June 2013

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In order to obtain maximum battery lifetime and efficient operation, rechargeable batteries require unique charging profiles with an end-state, low current trickle charge. The series loaded resonant (SLR) charging system presented in this thesis meets the needs of an efficient, sensor integrated, and galvanically isolated trickle charger. The SLR DC-DC converter was successfully modeled in Simulink, and simulation results are verified in a laboratory application. The Simulink model and hardware are tested at several operating points. Component stresses are quantified and weak points are identified.

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SIMULATING AND TESTING A DC-DC HALF-BRIDGE SLR CONVERTER

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Submitted in partial fulfillment of the
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ABSTRACT

In order to obtain maximum battery lifetime and efficient operation, rechargeable batteries require unique charging profiles with an end-state, low current trickle charge. The series loaded resonant (SLR) charging system presented in this thesis meets the needs of an efficient, sensor integrated, and galvanically isolated trickle charger. The SLR DC-DC converter was successfully modeled in Simulink, and simulation results are verified in a laboratory application. The Simulink model and hardware are tested at several operating points. Component stresses are quantified and weak points are identified.

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LIST OF ACRONYMS AND ABBREVIATIONS

CCM	Continuous Conduction Mode
DC	Direct Current
DCM	Discontinuous Conduction Mode
FPGA	Field-programmable Gate Array
MOSFET	Metal-Oxide Semiconductor Field-Effect Transistor
NGIPS	Next Generation Integrated Power Systems
PCB	Printed Circuit Board
SLR	Series Loaded Resonant

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EXECUTIVE SUMMARY

The Navy's Next Generation Integrated Power Systems will require "an unprecedented level of technology development and systems engineering" to meet their goals of providing "smaller, simpler, more affordable and more capable ship's power systems" [1]. The ships of the future will include higher demands for power from advanced electronic weaponry and high powered sensors. Because some systems use a larger amount of energy over a shorter period of time, there are greater needs for more efficient methods of energy storage. Energy stored in a battery bank is moved to a capacitor bank to meet the needs of pulse power demands. The objective of this paper is to provide a model and implementation of a DC-DC series loaded resonant (SLR) power converter which can be used to charge a single battery cell in a battery bank. The model can be tested and validated and then scaled for use at higher voltages and larger systems.

The objectives of this research were to:

- Select a suitable topology for efficient battery charging
- Describe the theory of operation and the state machine equations
- Build a Simulink model corresponding to the state machine equations
- Build the SLR converter based on the simulation results
- Test the hardware in the lab to verify simulation results
- Optimize the design for efficiency, component stress and desired outputs
- Determine possible second order effects in the resonant converter
- Compare the results of the simulation to the hardware model in order to verify results and make recommendations for a smarter battery charging solution.

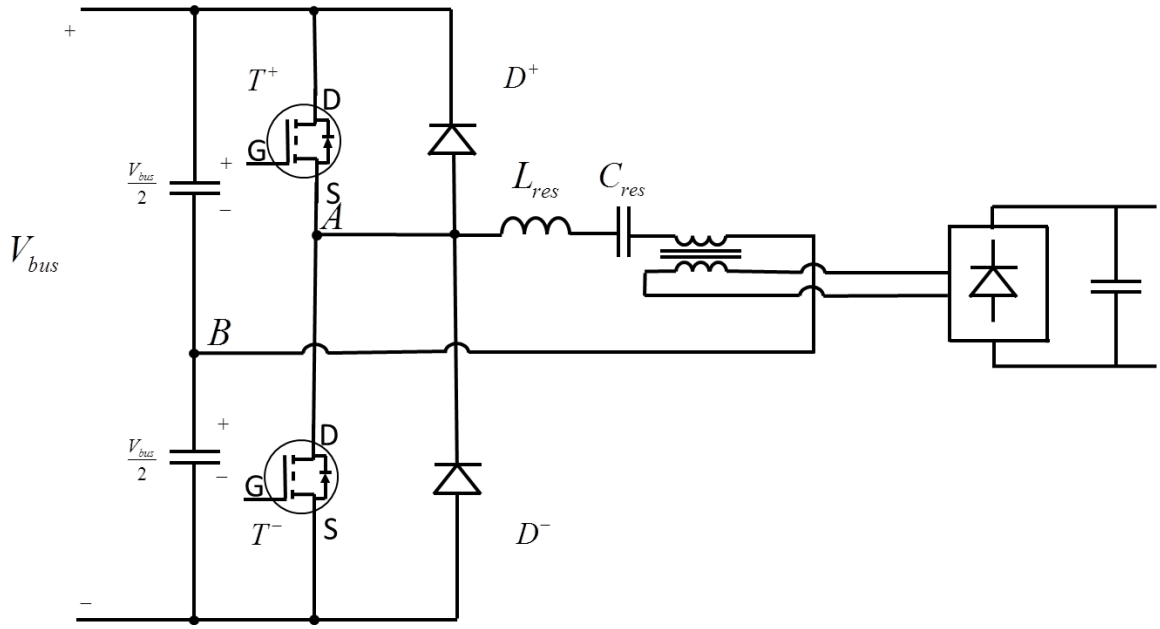

Figure 1. Half-bridge SLR converter topology. From [2].

The first step was to choose the topology shown in Figure 1 from [2]. The SLR circuit employs a resonant tank and metal-oxide semiconductor field-effect transistor switches to produce a resonant current. The resonant current is then rectified in the output diodes and capacitors to produce a flat DC output capable of charging a battery. The output transformer is added to produce galvanic isolation between the input and output and to allow us to boost or buck the voltage entering the battery. Once the topology was chosen, state equations were developed and a Simulink model was implemented based on the state equations. The Simulink model incorporated the state equations based on every mode of operation in the resonant converter, including the output transformer.

A series of trials were run on the SLR prototype and compared to the simulation results. The waveforms and comparable laboratory waveforms are shown in Figure 2.

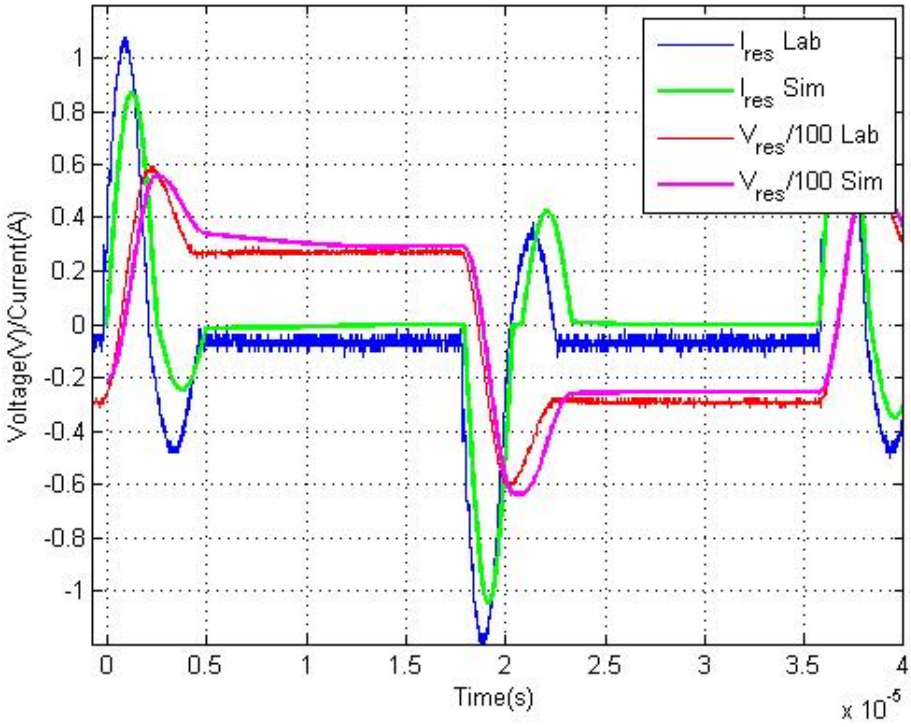

Figure 2. Resonant voltage and current compared from simulation and laboratory data in Trial 1.

The slight variataions are caused by measurement noise as well as unmodeled secondary and higher order effects within the laboratory system. The simulation and laboratory hardware were compared and the safe operating area was explored. The charger design was verified to be within component operating characteristics, and the simulation is a close enough match that further large scale design can be performed without creating a laboratory prototype for every model.

In summary, an SLR converter was modeled in Simulink, and the results were verified in the laboratory with a printed circuit board design.

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LIST OF REFERENCES

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I. INTRODUCTION

A. BACKGROUND

The Navy's Next Generation Integrated Power Systems (NGIPS) will require "an unprecedented level of technology development and systems engineering" to meet their goals of providing "smaller, simpler, more affordable and more capable ship's power systems" [1]. The ships of the future will include higher demands for power from advanced electronic weaponry and high powered sensors. Because some systems use a larger amount of energy over a shorter period of time (pulse power), there are greater needs for more efficient methods of energy storage.

In order to meet future pulse power demands with ship power, a large bank of capacitors or similar rapid discharge source is required. If capacitors are charged directly from the ship's power the load draw on current power systems would be too large to maintain all of the ship's capabilities. In this case, a battery bank is required to supplement the capacitors in a pulsed power system, averting the negative effects of large pulses of power by spreading the charging of the capacitor bank over a larger period of time. The current research in high voltage capacitor charging is discussed further in [2], [3], [4], [5], [6].

Battery banks need to be charged, and some methods are more efficient than others. Current research in battery charging has proliferated due to the recent advances in electric cars. Yilmaz and Krein's overview of battery charger topologies for electric and hybrid vehicles illustrates the benefits of specific charging topologies [7]. SLR converters are used in some of these battery chargers because they provide a current source ideal for battery charging, along with reduced metal-oxide semiconductor field-effect transistor (MOSFET) switching stress and losses.

B. OBJECTIVE

The objectives of this research are to:

- Select a suitable topology for efficient battery charging
- Describe the theory of operation and the state machine equations

- Build a Simulink model corresponding to the state machine equations
- Build the SLR converter based on the simulation results
- Test the hardware in the lab to verify simulation results
- Optimize the design for efficiency, component stress and desired outputs
- Determine possible second order effects in the resonant converter
- Compare the results of the simulation to the hardware model in order to verify results and make recommendations for a smarter battery charging solution.

The PCB is a proof of concept; it should serve primarily to validate the simulation models. The hardware solution should be optimized for maximum power, efficiency, and component lifetime.

C. APPROACH

The first step was to choose the SLR topology shown in Figure 1, which is described in [8]. This design offers the efficiency of zero current switching with the benefits of galvanic isolation. The figure displays the use of IGBTs as switches, but MOSFETS are more appropriate for low voltage and low current applications. The components were chosen based on the desired operating characteristics. The design was simulated in Simulink and then verified in the laboratory via a PCB. Experimental data was captured and compared to the theoretical data from Simulink.

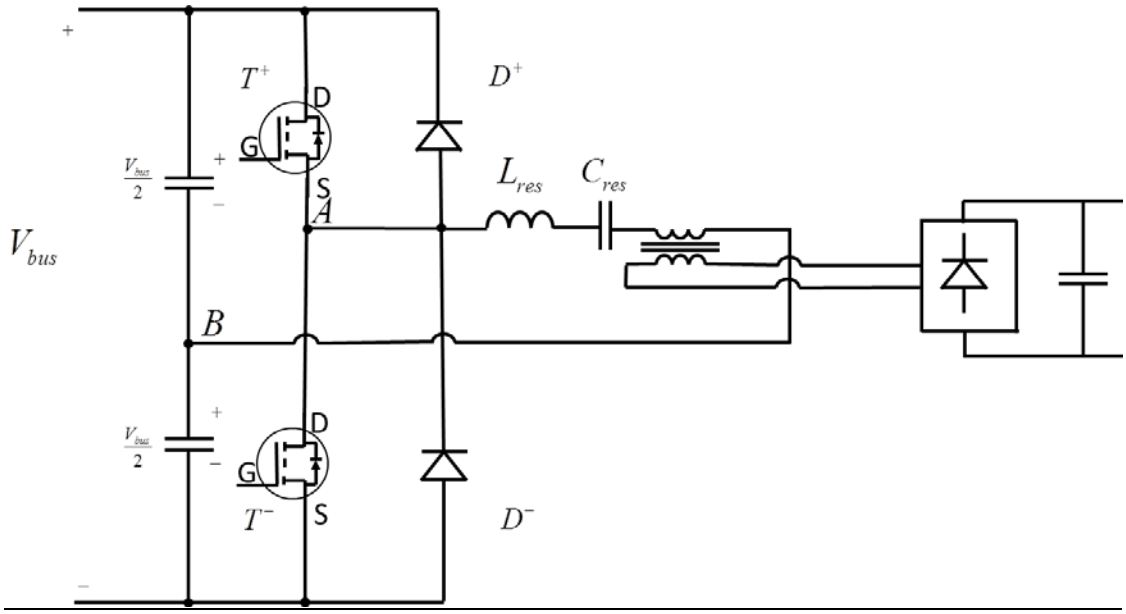

Figure 1. SLR DC-DC converter circuit topology.

D. THESIS ORGANIZATION

Battery management theory and design is the focus of Chapter II, while an overview of the Simulink model is detailed in Chapter III. An overview of the hardware design challenges and tradeoffs is given in Chapter IV, and the hardware results compared with the simulation outputs is given in Chapter V. Finally, the conclusions and future research questions are reviewed in Chapter VI.

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II. BATTERY MANAGEMENT AND SLR OPERATION

A. INTRODUCTION

Battery management covers a wide area of interest. Many different charging topologies are available and offer their own advantages and disadvantages. Essential to battery management theories are the physical properties of batteries. Charging time and battery lifetime are linked to the attributes of the battery charger [9]. Batteries are typically charged to just below rated capacity at a high rate of current and then must be maintained using a "trickle" charge current to allow for maximum battery lifetime without overcharging the battery. Modern day power electronics have enabled battery chargers to become "smarter," and more efficient.

B. CHARGER TOPOLOGIES

Numerous battery charger topologies exist, each with their own advantages and disadvantages. Yilmaz's research details the most common topologies for both unidirectional and bidirectional charging [7]. The operation of battery chargers depends on components, control, and switching strategies. Charger control algorithms are implemented through analog control, digital signal processors, microcontrollers, and specific integrated circuits. Design depends heavily on the level and type of input/output voltage and on the power output of a charger. AC input to chargers commonly utilizes a rectifier bridge to convert AC current into DC current. Most chargers use either a half-bridge (two switches) or a full bridge (four switches) topology. A half-bridge uses fewer components and costs less but exhibits higher components stress. A full bridge gains the advantage of reduced stress at the expense of added components.

Other commonly used topologies are the Buck, Boost, Buck/Boost, Flyback, Forward, Push-pull, CUK, and multilevel chargers; each contain their own advantages and disadvantages.

The design chosen was the SLR half-bridge topology. When used in conjunction with a transformer, the SLR offers the following advantages: reduced switching losses, galvanic isolation, lower component stress, and simple control.

C. SLR CONVERTER THEORY

The basics of SLR converter operation are thoroughly reviewed in [8] and in Lebel's SLR thesis [10]. Series loaded resonant converters utilize an inductor capacitor resonant tank. The fundamental element of a SLR converter is the damped resonant circuit shown in Figure 2. This circuit will form the basis of the model and printed circuit board. The equations governing operation are given in [8]. Only equations relevant to the design of the PCB are discussed in this section.

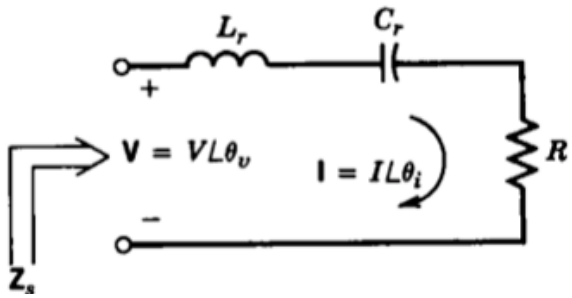

Figure 2. Basic series resonant circuit. From [8].

D. SLR OPERATION

Based on the inductor and capacitor chosen, every SLR circuit will have a resonant angular frequency ω_0. Equation (1) is from [8], and is used to calculate the resonant frequency as

$$f_0 = \frac{\omega_o}{2\pi} = \frac{1}{2\pi\sqrt{L_r C_r}} = \frac{1}{2\pi\sqrt{(32\ \mu\text{H})(18\ \text{nF})}} = 209\ \text{kHz}\,. \tag{1}$$

The resonant angular frequency ω_o is used to determine how to gate the MOSFET switches, achieving zero current switching. At switching frequencies ω_s, where $\omega_s < \omega_0 / 2$, the SLR converter enters discontinuous-conduction mode (DCM). At $\omega_0 / 2 < \omega_s < \omega_0$, the converter is in continuous conduction mode (CCM) as well as when $\omega_s > \omega_0$. These three separate modes determine the operating characteristics of the

converter. Each mode offers various advantages, which are discussed more thoroughly in [8]. For simplicity and to avoid switching losses as much as possible, the converter presented in this paper is designed to stay in DCM.

The SLR circuit used in the board is shown in Figure 1. The resonant tank shown in Figure 2 is represented in Figure 1 by its components L_{res} and C_{res}. In order to control the current through the tank into the waveforms desired, MOSFETS T^+ and T^- are switched at a rate of ω_s. As capacitors are charged to half of the bus voltage $V_{bus}/2$, the switches control the current through the tank and the diodes, D^+ and D^-. Lebel's thesis thoroughly describes the five voltage and current states present in the SLR topology. These are shown from left to right in Figure 3.

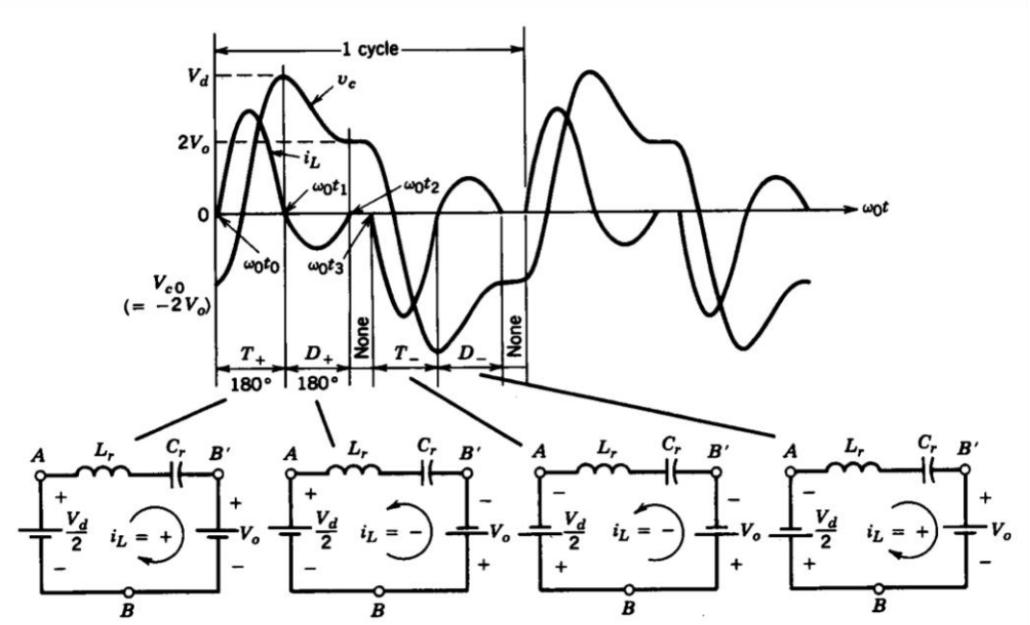

Figure 3. Discontinuous-conduction mode operation of the SLR converter. From [8].

Initially, T^+ is gated on and a single current pulse i_l resonates within the tank. As i_l turns negative, D^+ turns on to mark the second interval, until all of the energy in the tank is transferred to the load. The third interval is entered, and i_l remains at zero

until the next switching event occurs (this third interval must occur during DCM operations). MOSFET T^- is then gated on for the fourth interval, i_l starts negative, and when the current reaches a positive state, D^- is turned on until all of the energy is transferred to the load. The sixth interval has no current flowing and is identical to the first interval. These five states are later mapped out in the Simulink model.

E. CLOSED FORM EQUATIONS

The closed form equations for the resonant current in each mode of operation, as well as the average DC input current and the average DC output current are derived in [11]. For the first interval, $0 < t < t_1$, the resonant current i_{res} given in terms of the bus voltage V_{bus} and the output voltage V_{out} is

$$i_{res}(t) = i_{res_o} \cos \omega_o t + \frac{V_{bus}/2 - vr_0 - V_{out}}{\omega_o L_{res}} \sin \omega_o t. \tag{2}$$

This first current interval is the only time current flows through either of the MOSFETS, and it can be used to determine the average drain-source current through the MOSFET. In the second interval i_{res} goes negative, and the closed form solution is shown as

$$i_{res}(t) = \frac{V_{bus}/2 - vr_{t1} + V_{out}}{\omega_o L_{res}} \sin \omega_o (t - t_1). \tag{3}$$

In the fourth and fifth interval, the resonant current is fed from the negative DC bus, and (2) and (3) are negated. In order to predict steady-state operation of the resonant converter, the average input current from the DC source in DCM from [11] is

$$I_{in\_avg} = \frac{8V_{out}}{\omega_o^2 L_{res} T_{sw}} \ . \tag{4}$$

Finally, the average output current is only dependent on the bus voltage because the other variables are fixed and is shown as

$$I_{out\_avg} = \frac{8V_{bus}/2}{\omega_o^2 L_{res} T_{sw}}. \quad (5)$$

Because of zero current switching in DCM, the efficiency of operation is constant regardless of the switching frequency or input/output voltage.

F. TRANSFORMER THEORY

Transformers are often used in circuits to boost, buck, or isolate voltage. The SLR converter provides an easy path to transformer implementation. When modeling the transformer, the classic T-equivalent circuit is implemented.

1. T- Equivalent Circuit

A transformer is an electromagnetic device which uses two or more windings wrapped about the same ferromagnetic core. The core works to maximize mutual inductance between the windings, but no transformer is perfect. Every transformer will have some amount of leakage flux and core losses (except and air core) associated with the design of the transformer. In order to accurately model the behavior of the transformer, the T-equivalent circuit takes into account the losses in the windings of the transformer and the magnetizing and mutual inductance of the transformer. The equivalent circuit is displayed in Figure 4 from [12].

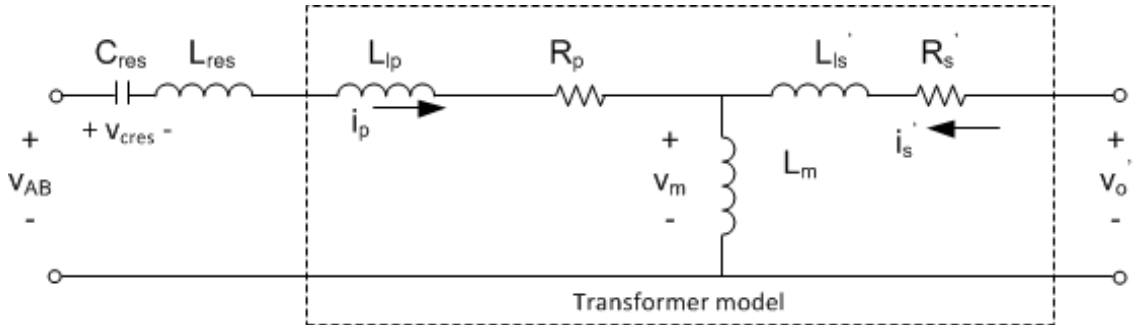

Figure 4. The T-equivalent circuit. From [12].

2. Modeling the T-Equivalent Circuit

The five terms that represent the lumped parameter model of the transformer are L_{lp}, L_{ls}', L_m, R_p', and R_s'. In order, these represent the leakage inductance of the primary, the leakage inductance of the secondary, the magnetizing inductance of the transformer, and the resistance of the primary and the secondary winding. These characteristics are important in modeling the output of the transformer and analyzing the resultant circuit.

3. Incorporating the Transformer into the SLR Circuit

Using Ohm's law around both secondary and primary loops of Figure 4, we obtain the matrix form of the voltages around the loop as

$$\begin{bmatrix} v_{AB} - v_{cres} \\ v_o' \end{bmatrix} = s \begin{bmatrix} L_{res} + L_{lp} + L_m & L_m \\ L_m & L_{ls}' + L_m \end{bmatrix} \begin{bmatrix} i_p \\ i_s' \end{bmatrix} + \begin{bmatrix} R_{Lres} + R_p & 0 \\ 0 & R_s' \end{bmatrix} \begin{bmatrix} i_p \\ i_s' \end{bmatrix}. \quad (6)$$

Using these parameters for the transformer, we can implement the transformer in the SLR converter model in Simulink, and analyze the results.

G. SWITCHING THEORY

1. Modeling a MOSFET

In Figure 5, the basic circuit equivalent of a MOSFET is shown. The three major components of the MOSFET are R_g, C_{gd}, and C_{gs} which represent the gate resistance, the gate-drain capacitance, and the gate-source capacitance, respectively. The two capacitances are not constant but vary with the voltage across them. This complicates even simple models of MOSFETS; although this equivalent circuit is not implemented into the Simulink model, it is used to predict turn switching effects in the circuit.

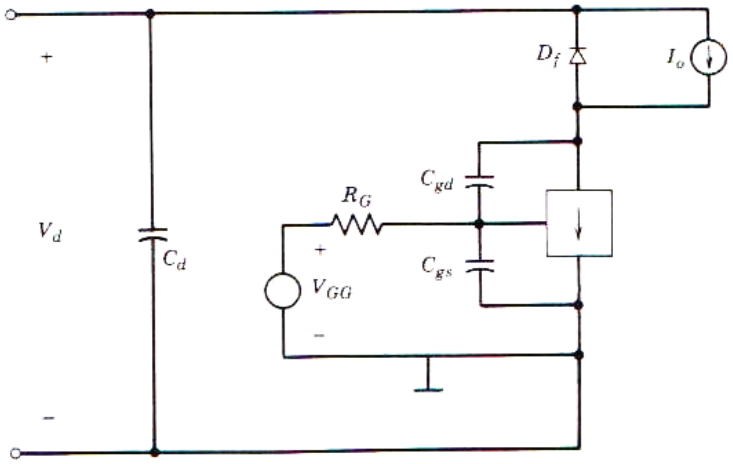

Figure 5. The circuit equivalent model of a MOSFET used to switch a diode-clamped inductive load. From [8].

2. Switching Waveforms

The voltage and current waveforms shown in Figure 6 are critical to understanding how voltage and current flow through a MOSFET during a switching event. The MOSFET's switching waveforms are broken up into four separate switching cycles: $t_{d(on)}, t_{ri}, t_{fv1}$, and t_{fv2}. The complex waveforms based on the physical properties of the MOSFET are explored further in [8]. The initial gate drive voltage is represented as a step function V_{GG} which is used to switch on the MOSFET. The turn on current i_g is at its highest in the first time interval of turn on $t_{d(on)}$, and the gate driver must be rated at this current or above in order to fully open the MOSFETS in the desired amount of time. Choosing i_g determines the amount of time necessary to fully open the MOSFET. The total gate charge is given as Q_g. It can be shown that the amount of time necessary to fully switch on a MOSFET is given by $T_{on} = Q_g / i_g$.

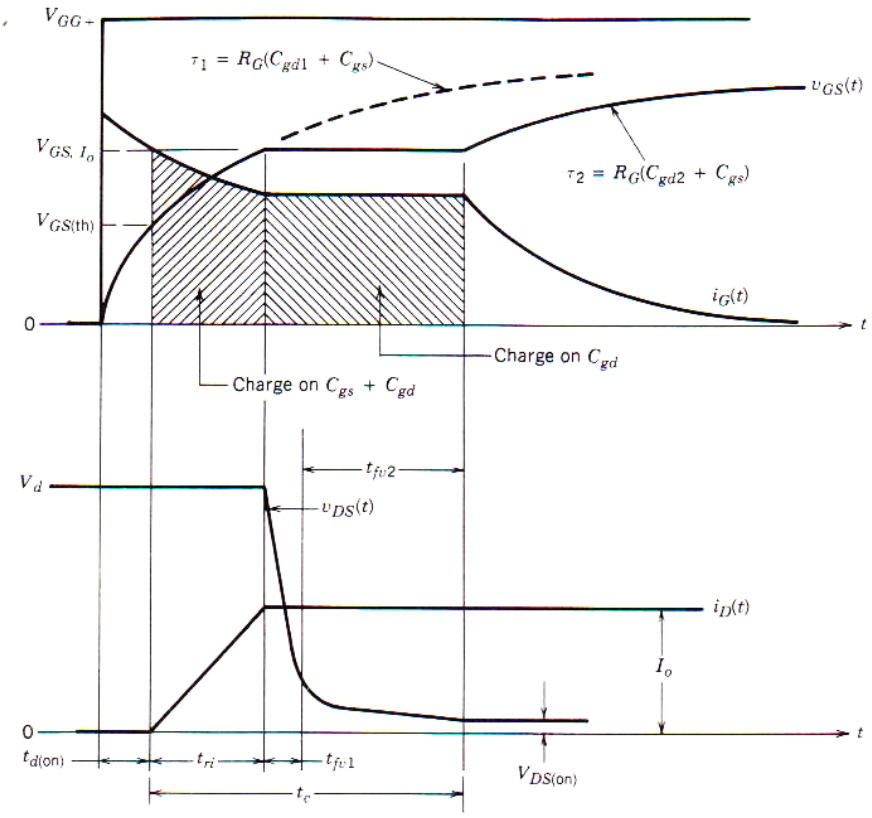

Figure 6. The turn-on voltage and current waveforms of the MOSFET with ideal freewheeling diode. From [8].

The MOSFET changes through four different equivalent circuits during turn on, as shown in Figure 7. These circuits are important to understanding how to model the MOSFET, and they are all useful in predicting second order effects during MOSFET turn on within the circuit.

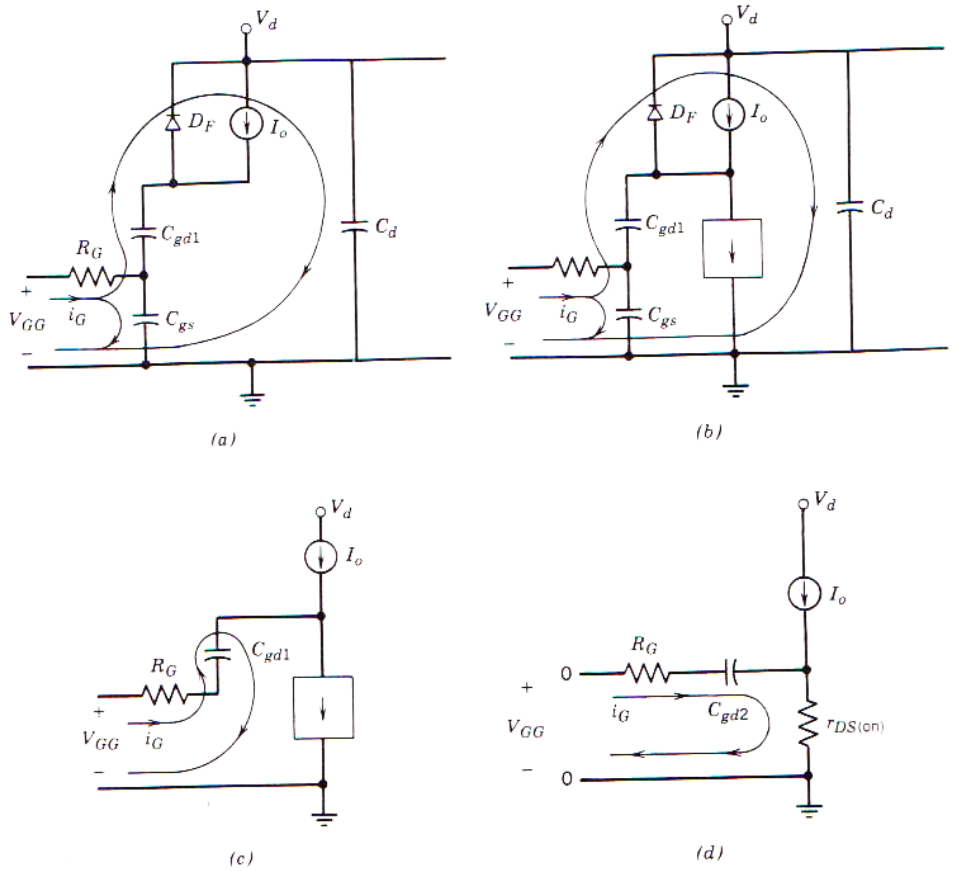

Figure 7. The equivalent circuits used to estimate the turn-on current and voltage waveforms of the MOSFET. From [8].

Shown in Figure 8 are the conduction waveforms driving a MOSFET from the datasheet [13]. These waveforms are critical to examining lab data from the final experiment; they illustrate which section of the resonant voltage and current are caused by conduction properties within the MOSFET.

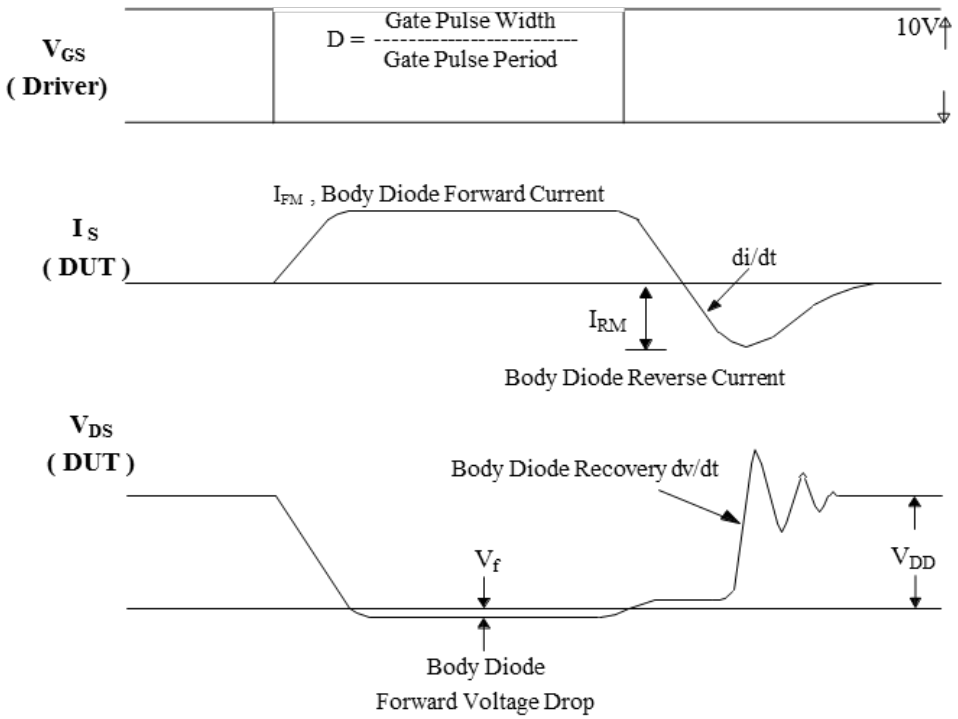

Figure 8. The MOSFET conduction waveforms. From [13].

As illustrated in Figure 8, the drain-source voltage V_{DS} does not fully drop to zero after a switching event. The body diode forward voltage drop creates a bias while the switch is on. Afterwards, V_{DS} does not return immediately to V_{DD}; the diode recovery creates high frequency oscillations.

H. CHAPTER SUMMARY

In this chapter, the fundamentals of battery management were discussed in addition to an introduction SLR converter operation, transformer theory, and MOSFET switching theory. In the next chapter, the Simulink design based on the SLR operation described in this chapter is presented.

III. SIMULINK: MODELING AND RESULTS

A. INTRODUCTION

Simulink is a powerful tool used to enhance an engineer's ability to accurately and quickly model a plethora of systems and how they interact with each other. In this model, the basic equations dictating how an SLR circuit operates are executed in a graphical block diagram form. Simulink uses blocks to define systems and subsystems. The source and the SLR converter are shown in the highest level section of the Simulink model in Figure 9.

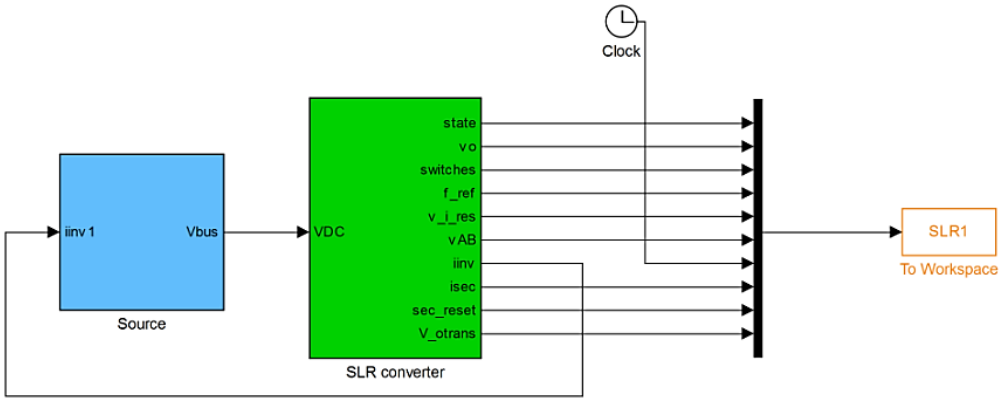

Figure 9. Block diagram of the SLR converter, source, and output variables.

B. MODELING THE SLR CONVERTER

The SLR converter block consists of two main blocks, the H-bridge, and the resonant tank and load, shown in Figure 10.

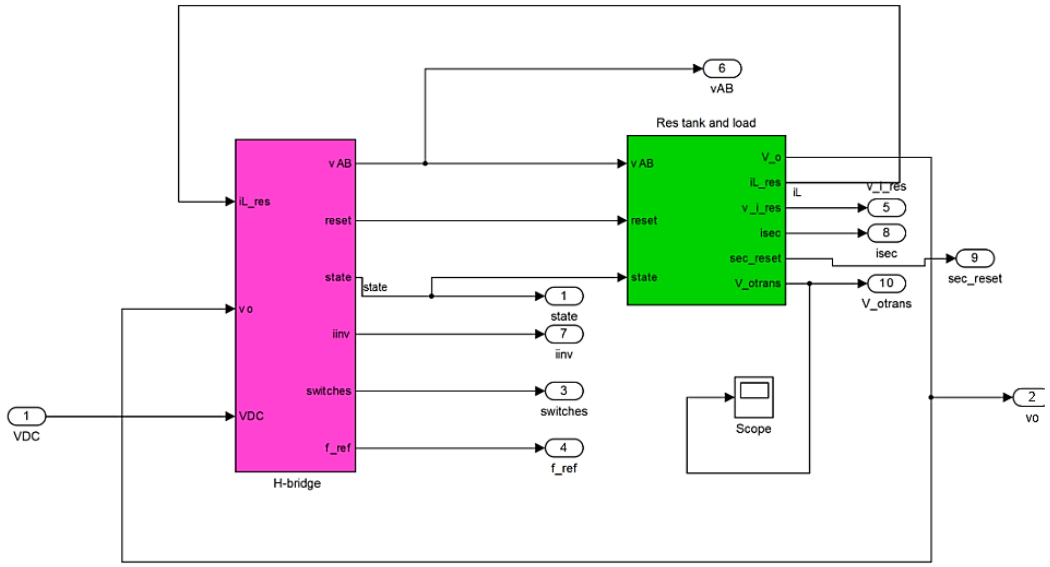

Figure 10. Resonant tank and H-bridge.

In its simplest form, the H bridge is simulated from the switching waveforms detailed in Section II.D. These five intervals are shown in the five states on the H bridge diagram in Figure 11. The state machine shown is logic based, and implements a certain pulse based on the state of the switches T^+ and T^- in addition to the resonant current i_l. The outputs of all the states are merged, and the voltage across the tank and load are chosen based on the state. The state and the voltages are then fed into the "res tank and load" block illustrated in Figure 10.

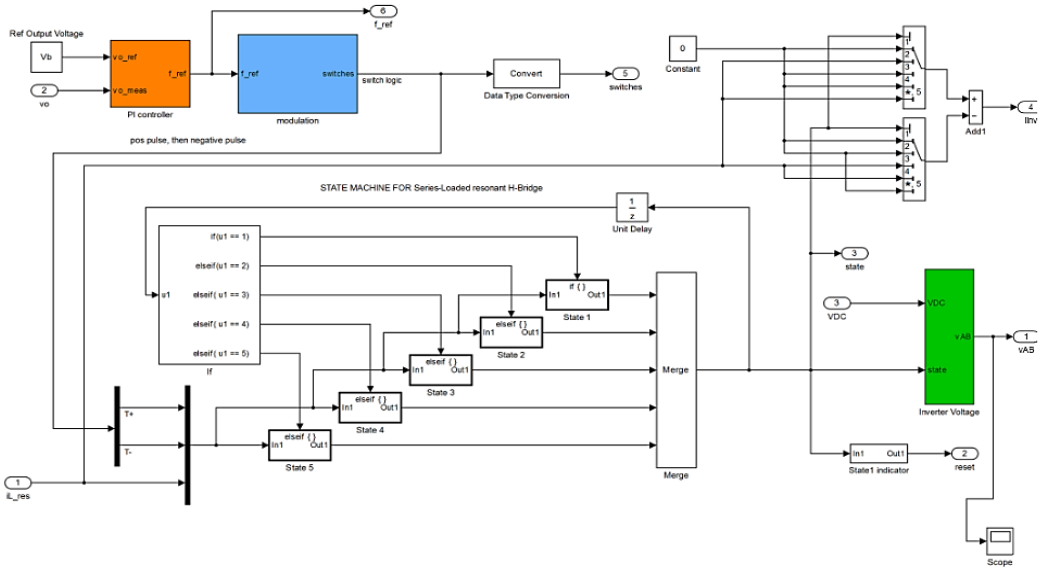

Figure 11. H-bridge subsystem.

The resonant tank and load model incorporates both the equations of the transformer and the resonant tank. The model of the transformer is done using the T-equivalent circuit model shown in Section II.F.2. The *A* and *B* matrices are calculated within the workspace code and shown in Figure 12. These gains are used in conjunction with integrator blocks to implement the states of the system, both the primary and secondary current. The current of the output, the current in the tank, and the voltage of the output and the voltage across the tank are all outputted by the resonant tank and load block. These outputs are fed into the workspace, where they can be graphically plotted and viewed.

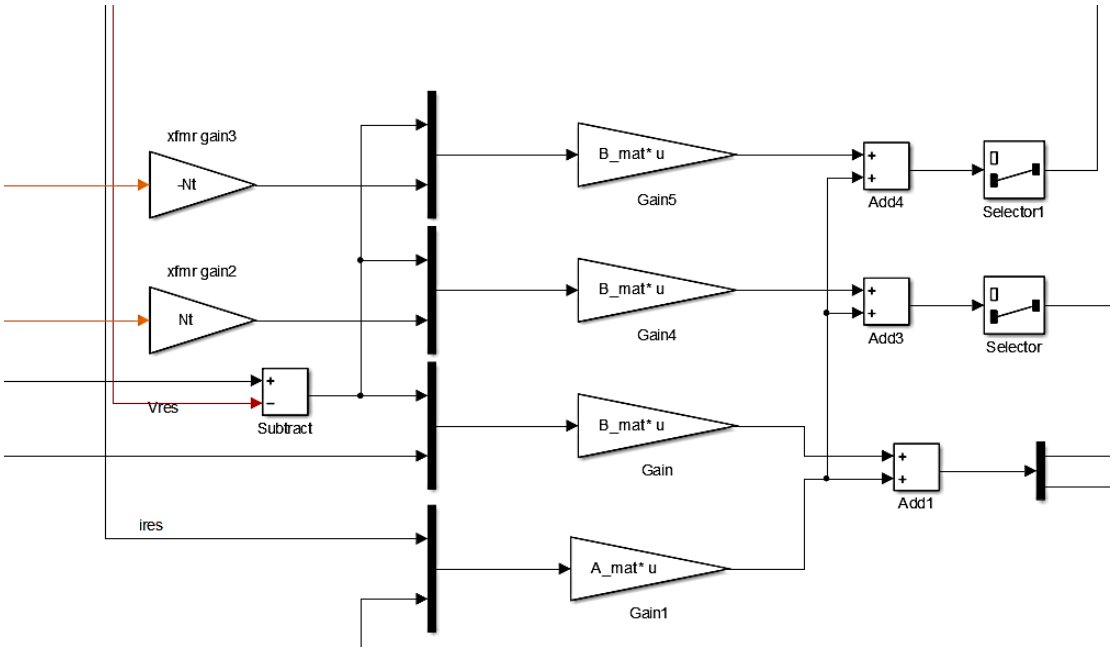

Figure 12. Implementation of a transformer in Simulink.

C. SIMULATION RESULTS

1. Simulation Inputs

Using the results of the board design section, we wrote the parameters into the simulation and analyzed the output. The initial parameters used in the simulation are shown in Table 1 which are used to produce Figure 13.

Table 1. Initial simulation parameters.

Parameter	**Symbol**	**Value**
Resonant capacitor	C_{res}	18 nF
Resonant inductor	L_{res}	32 µH
Bus voltage	V_{bus}	62.4 V
Simulation step time	t_{step}	30 ns

Parameter	Symbol	Value
Resonant inductor resistance	R_{lres}	4 mΩ
Primary transformer winding resistance	R_p	0.01 Ω
Secondary transformer winding resistance	R_s	0.01 Ω
Primary Inductance	L_{lp}	1 µH
Secondary Inductance	L_{ls}	1 µH
Magnetizing Inductance	L_m	2.4 mH
Transformer turns ratio	N_t	1.25
Output capacitance	C_{out}	30 µF
Voltage dropped across MOSFET	V_{FET}	0.5 V
Voltage dropped across diode	V_{diode}	0.5 V
Switching frequency	f_s	28 kHz

2. Results

The simulation produces the relevant waveforms in the resonant converter: the output voltage V_{out}, the voltage across the resonant tank V_{ab}, and the resonant and secondary current I_{res} and I_{sec} respectively. The current I_{res} is not seen in Figure 13 as it is concurrent with the current I_{sec}. These plots provide the starting point for board design and a verification of the equations developed in Section II.D.

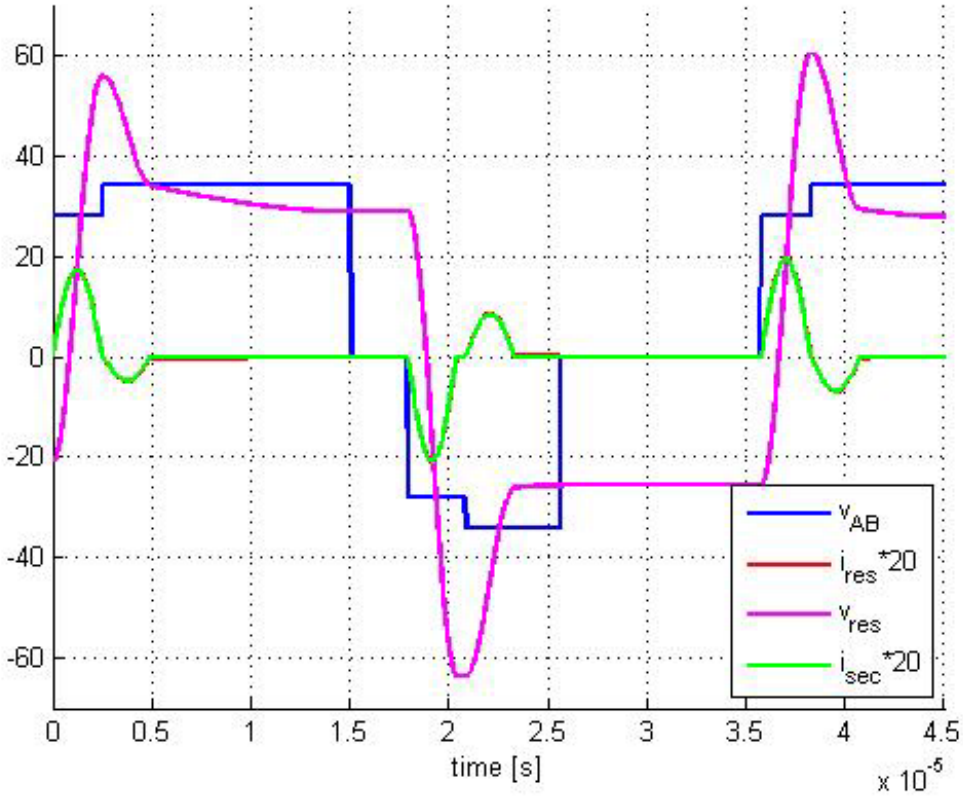

Figure 13. Simulated resonant current and voltage waveforms where scaled voltage (V) and current (A) are displayed on the Y-axis and time (s) is displayed on the X-axis.

D. CHAPTER SUMMARY

In this chapter, the SLR converter and transformer were implemented in Simulink. The inputs to the model were given and the results are shown. In the next chapter, the SLR hardware is designed and implanted through a printed circuit board.

IV. HARDWARE DESIGN

A. INTRODUCTION

Choosing every component of the SLR converter is a detailed process. Peak voltages, frequencies, and currents must be taken into account to ensure maximum lifespan, efficiency, and compatibility for every component on the board. Utilizing datasheets, equations, and Simulink, the component stress and operating area of the design is investigated. The schematic of the PCB is shown in Figure 14.

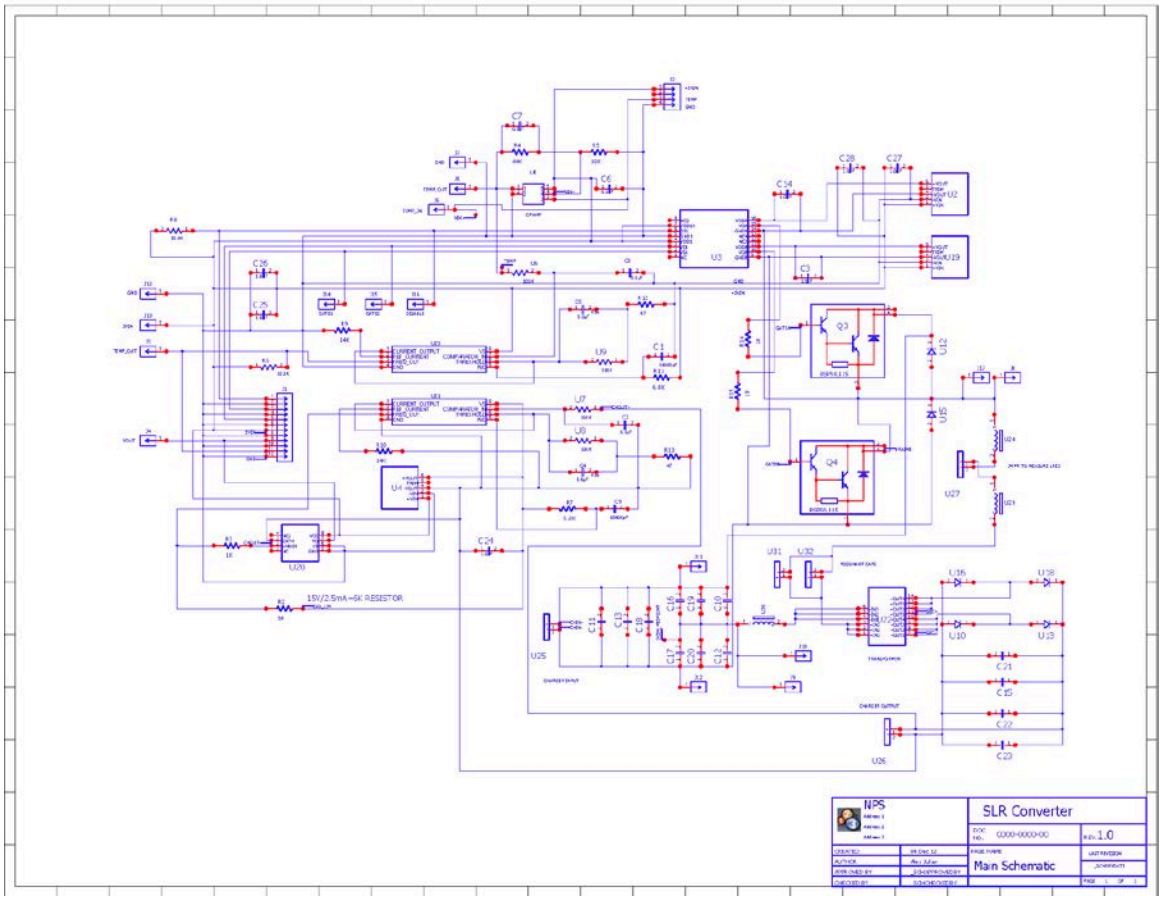

Figure 14. The PCB schematic includes the components discussed in Section IV.

B. SECONDARY COMPONENTS

In this section, the components explored are those which inherently should not be under great stress and, therefore, do not require complex analysis processes. While the most important operation of the PCB is to trickle charge a battery while monitoring temperature, other sections of the board are used to communicate with the controller.

1. Voltage-to-Frequency Converter

In order to measure and control the charging of the battery, the output voltage must be obtained and converted to a signal that the FPGA can read. This component was chosen based on the desired precision of the converter, 0.01 percent, and the relatively simple implementation. The LM231A converts voltage values of the circuit into frequency, which is then read by the Xilinx FPGA module. Additionally, the LM231A provides isolation for the Xilinx FPGA module from the final output voltage of the device. Based on the data sheet, the component values chosen are $R_s = 14\ \text{k}\Omega$ and $C_s = 0.1\ \mu\text{F}$.

2. Optocoupler

Part U20 on the schematic FOD2200SDV is an optocoupler which provides optical isolation from the output of the *V/f* converter to the Xilinx FPGA module. The optocoupler adds a level of protection should any high voltages leak from the charging side of the PCB, which would destroy the Xilinx FPGA module. Logic signals are transmitted with a maximum delay of 300 ns.

3. DC-DC Converter

Parts U4, U2, and U19 are DC-DC converters. U4 provides sufficient and consistent supply voltages to the *V/f* converter and the optocoupler so that the output voltage measurement is isolated from the digital input. U2 and U19 are the power supplies for the MOSFETs.

4. Instrumentation Amplifier

The ADuM7234 is a monolithic instrumentation amplifier used to interface the MOSFET with the gate signals coming from the Xilinx controller; amplifying the low level TTL gate signals to drive the MOSFETs and isolate the MOSFET gate signals from the input.

C. PRIMARY BOARD OPERATION COMPONENTS

The primary board operation components are the components modeled in Simulink and will endure the most stress under operation. These components include the resonant tank capacitor and inductor, the MOSFETS, and the transformer.

1. MOSFETs

Parts Q3 and Q4 on the schematic represent the MOSFETs, or the switches for the SLR converter. Shown in Table 2 from [13], are the most important restrictions related to failure and stress within the MOSFET.

Table 2. MOSFET maximum parameters. From [13].

V_{max} (V)	I_{max} (A)	F_{max} (MHz)	P_{max} (W)
$V_{DSS} = 100$	$I_d = 2.3$	200	2.4
$V_{GS} = \pm 20$	$I_{DM} = 18$		
	$I_{AR} = 18$		

The maximum parameters of the MOSFET will be compared against data from the simulation to determine areas of stress on the components.

a. Breakdown Voltage

The breakdown voltage of the MOSFET represented by $V_{DSS} = 100$ is the amount of voltage across the drain and source that causes failure of the MOSFET. Even the smallest overvoltage destroys the MOSFETs. In order to guard against this, high frequency bypass capacitors are placed in parallel with the MOSFETs to filter out any large voltage spikes. These are parts C18 and C13. The voltage applied from drain to source when the MOSFETs are switched to the off position is V_{bus} / 2 Therefore, the bus voltage should never be driven higher than $2V_{DSS} = 200 \text{ V} = V_{busmax}$.

b. Turn-on Voltage

The maximum turn on voltage $V_{GS} = \pm 20 \text{ V}$ is the maximum voltage applied to the MOSFET gate-source. Because the MOSFET gates are driven with an instrumentation amplifier, this is not a design concern.

c. Drain Current Pulsed

The maximum temporary current between the drain and source sustainable by the MOSFET before failure is I_{dm}. The simulation and the derivation of the SLR operation in Section II.E is used to calculate the maximum current in the MOSFET device.

d. Driving the MOSFET

The theory of driving the MOSFET is discussed in Section II.G; the goals are to turn the MOSFET on as quickly as possible. The ADuM7234 chip provides a maximum current of 4 A and enough voltage to bring the MOSFET into conduction. Using parameters from the MOSFET's datasheet [13], we find the predicted turn-on time of the MOSFET to be

$$T_{on} = \frac{Q_g}{I_g} = \frac{Q_g}{\frac{V_g}{R_g}} = \frac{22\text{nC}}{\frac{12}{18}} = 33 \text{ ns}. \quad (7)$$

The current I_g is determined by the gate resistance, which is 18 Ω, and the driver's output gate voltage V_g of 12 V.

2. Transformer

The transformer in the circuit performs two critical tasks: stepping down the output voltage to roughly 14 V for battery charging and creating galvanic isolation between the input and output of the charger. The requirements of the board drove our desire to make our own transformer. It may have been possible to buy an off-the-shelf commercial transformer to suit our design, but the realities of design gave greater weight to a more flexible option: winding our own transformer. Two transformers, Transformer A and Transformer B, were wound with different physical characteristics to test their effects on the performance of the SLR converter.

a. Design Theory

The Magnetics 2012 Ferrite catalog has a wide variety of ferrites to choose from [14]. The catalog also includes methods of selecting transformer cores for power applications. A core can be selected by either the power handling capability or from the $W_a A_c$ product, where W_a is the available core window area and A_c is the effective core cross-sectional area. The core is selected based on the $W_a A_c$ product and a safety factor. The transformer design section of the Magnetics-Inc catalog is shown in Appendix A.

There are many different core geometries available and each are suited for different power electronics applications. For a switching power supply, PQ cores optimize the ratio of core volume to winding and surface area. Power output, inductance, and winding area are maximized when compared to a toroid, planar, or pot core. The core used is part 0P-42020-UG. The $W_a A_c$ product equation from the catalog is

$$W_a A_c = \frac{P_o D_{cma}}{K_t B_{max} f_{max}} = 0.0642 \text{ cm}^4. \quad (8)$$

The power out (W) is P_o, D_{cma} is the current density (mils/amp), B_{max} is the flux density(gauss), K_t is the topology constant and f_{max} is the maximum frequency at which the transformer will operate at. The required parameters for the SLR charger are shown in Table 3.

Table 3. Transformer selection parameters used in conjunction with [14].

V_{xfmr} (V)	P_o (W)	D_{cma} (mils/amp)	B_{max} (gauss)	K_t	f_{max} (kHz)
12	12	750	1000	.0014	100

The output power P_o was chosen based on charging a maximum 1 A trickle charge at 12 V, D_{cma} is given in the text based on a conservative allowance for heat rise, B_{max} is given in the datasheet based on the desired minimum operating frequency, K_t is based on the half bridge topology constant, and $f_{\max}$ is the maximum desired switching frequency. The board is designed to run in DCM; therefore, $f_s < f_o / 2$, where $f_o / 2 \approx 100$ kHz.

The actual core chosen (42020-UG) had a minimum window product area of 0.23 cm^4, which is approximately four times as much as the minimum product area from equation (8). Therefore, overheating is not a concern, and the transformer has plenty of room left to run at higher frequencies if desired.

Using Faraday's law, we calculated the minimum number of turns to avoid saturation, $N_{t\min}$. Using the parameters from Table 3 and a cross-sectional core area A_c of 0.591 cm, we get the minimum number of turns

$$N_{t\min} \geq \frac{|V_{xfmr}|}{2\pi f_{\max} |B_{max}| A_c} \approx 14. \quad (9)$$

b. Voltage Output

The final output voltage is to be stepped down from the DC bus voltage V_{bus} of 72 V to the output battery voltage V_{out} of 14 V. However, the DC bus voltage is not the same as the amount of voltage across the primary windings of the transformer, due to losses in the MOSFETs , the resonant tanks L_{res} and C_{res}, and the output diodes.

Faraday's law also dictates the voltages on the output of an ideal transformer is

$$\frac{V_p}{V_s} = \frac{N_p}{N_s} = \frac{15}{12}. \tag{10}$$

The final ratio of 15/12 for transformer A was an educated guess based on the losses previously mentioned. After the laboratory data showed that the SLR circuit dropped nearly 5 V in MOSFET, inductor, and diode losses, Transformer B was wound using a turns ratio of 30/30. Using the turns ratio, we can predict the inductive properties of the transformer that affect the performance of the SLR circuit.

c. Magnetizing Inductance

From the magnetics datasheet, the core has a nominal area A_l of 3213 mH/1000T. Using this value and 15 turns on the primary, we get the self-inductance of the transformer to be

$$L_m = \frac{N^2 A_l}{10^6} = \frac{15^2 (3213)}{10^6} = 0.72 \text{ mH}. \tag{11}$$

The self-inductance is approximately equivalent to the magnetizing inductance. In the laboratory, two different boards were tested, one with 15 turns on the primary and one with 30 turns on the primary. For 30 turns, the theoretical self-inductance of the transformer increases to 2.89 mH. This was verified in the laboratory using a transformer with 24 turns on the primary. The magnetizing inductance was measured in the lab based on the T-equivalent circuit shown in Figure 4. The open circuit transformer

experiment performed is found in [12]. The power into the system may be expressed as $P = |\tilde{V}||\tilde{I}|\cos\phi$, where $\tilde{V}$ and $\tilde{I}$ are the voltage and current phasors and ϕ is the phase angle between $\tilde{V}$ and $\tilde{I}$. The power and voltage and current phasors are determined for an open circuit on the transformer secondary. The testing parameters of the circuit are shown in Table 4. The impedance of the circuit is

$$Z = \frac{\tilde{V}}{\tilde{I}} = \frac{\tilde{V}\angle 0^{\circ}}{\tilde{I}\angle -85.68^{\circ}} = (67.14 + j756.4)\ \Omega. \tag{12}$$

The reactive portion of the circuit is

$$X_{l1} + X_{m1} = 756.4\ \Omega. \tag{13}$$

Because the magnetizing inductance is much greater than the leakage inductance, the estimated magnetizing inductance is

$$X_{m1} \gg X_{l1}, Lm = \frac{756.4}{2\pi f} = 2.4\ \text{mH}. \tag{14}$$

The real part of the impedance is very sensitive to the measured phase angle. Because the transformer did not heat up in the lab, it is possible that there is error in our measurements for the phase angle between the voltage and current. Significant heating in the transformer would be expected if 1 A of current flowed through 67 Ω.

Table 4. Transformer magnetizing inductance test parameters.

V_{pp}	14.4 V
I_{pp}	19 mA
V_{rms}	5.09 V_{rms}
I_{rms}	6.71 mA
ϕ	85.68^{o}
f_{test}	50 kHz

Based on the 24 turns used in the transformer for this trial, the output can be scaled based on the ratio of turns squared. Therefore, a 30 turn transformer is

predicted to have a magnetizing inductance of $L_{m30} = (30/24)^2 2.41\ \text{mH} = 3.76\ \text{mH}$. Finally, a 12 turn transformer is predicted to have an output of $0.60\ \text{mH}$, similar to the prediction made on the datasheet in (11).

The results of the transformer tests and the measured/extrapolated values are shown in Table 5.

Table 5. Magnetizing inductance results.

Number of Turns	Predicted Value(mH)	Measured/Extrapolated Value(mH)
15	0.72	0.60(extrapolated)
24	1.85	2.41(measured)
30	2.89	3.76(extrapolated)

d. Current

The design of the SLR converter calls for a maximum of 1 A trickle charge. An average copper wire can handle about $500\ \text{A/cm}^2$, therefore a 30 gauge wire can handle approximately 0.25 A. Two transformers were tested using two differing boards. The first transformer, Transformer A, has one wire on the primary and two in parallel on the secondary. For the design of transformer B, in order to make room for more windings, there is only one wire used for the primary and one wire used for the secondary. The output current capacity is decreased in transformer B, but this allows us to use extra windings to increase the magnetizing inductance of the transformer.

e. Voltage Breakdown

Because the voltages in the transformer should not exceed 20 V, voltage breakdown is not a concern within the transformer.

f. Turns

The first board utilized transformer A with 15/12 turns, bucking the output voltage. The second board's transformer B had a turns ratio of 30/30, increasing the magnetizing inductance and increasing the voltage on the output. The two boards were tested and modeled.

g. Saturation versus Overheating

Both saturation and power consumption have been taken into effect when designing the transformer. Voltage would have to increase by a factor of 2 before saturation effects begin to occur, and the voltage output would have to increase by about five times before overheating damages the transformer.

D. BUILDING THE PRINTED CIRCUIT BOARD

The printed circuit board is shown in Figure 15. This design, implemented in PCB123 design software, had a few special considerations given the characteristics of an SLR circuit. The circuit's output side is galvanically isolated from the input side through the use of a transformer and a grounding plane. The board contains numerous points for pin out test interfacing, which are useful in the hardware testing side of the lab data.

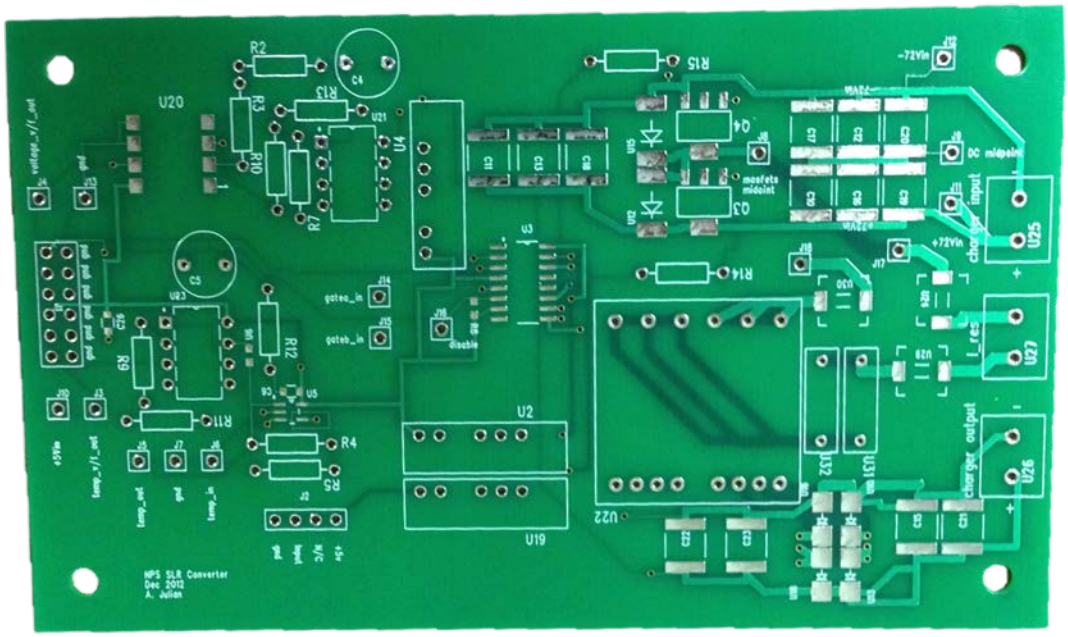

Figure 15. Final PCB before population.

The final PCB without the transformer is shown in Figure 16. The Xilinx FPGA module is connected at the 12 pin header on the left, and the batteries being charged are

connected to the screw terminals on the right. The test board is placed on a flat surface, and different pins act as test points to plot key voltages and currents in the circuit.

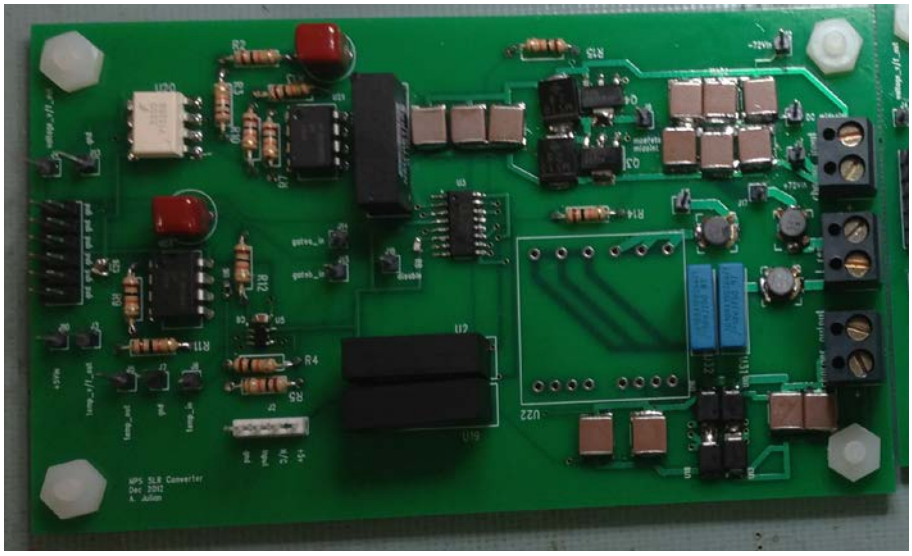

Figure 16. PCB after component population without transformer.

E. FPGA CONTROLLER

Illustrated in Figure 17 is the Simulink model of the Xilinx controller used to program the FPGA.

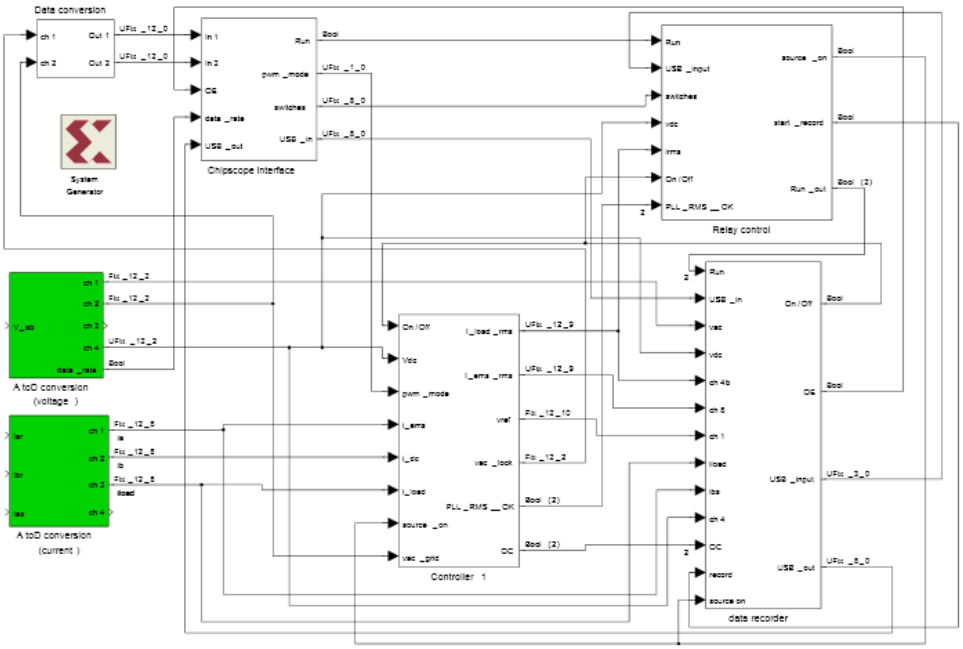

Figure 17. Programming the Xilinx controller implemented via Simulink.

The model used in this project is a derivative of the SLR controller used in [10]. The entire hardware setup is called the Student Design Center (SDC), using the Virtex-II reference board, Xilinx XC4VLX25-10SF363 FPGA, and four port voltage and current analog-to-digital converters [15]. In this project, we use the SDC to simply create a series of pulses to drive the MOSFETS. In the future, the FPGA could be used to join the SLR converter with other batteries being charged in parallel.

Figure 18 illustrates the controller 1 system. This block set demonstrates the ability to add control into the model at a later date. Load current enters the blocks as a floating point number and is filtered before being converted to an RMS value. The modulation subsystem contains a PI controller (currently shut off for these experiments) and can vary the output switching waveforms based on the proportional and integral gains. A fault management block helps protect the system from excess amounts of current caused by shorting the outputs.

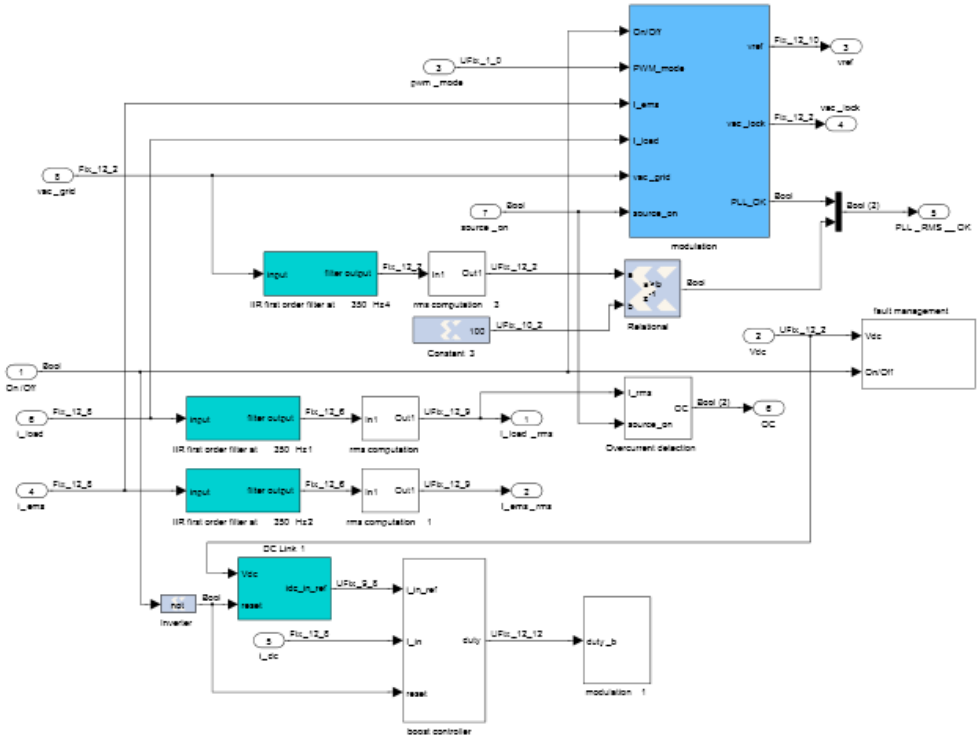

Figure 18. Controller 1 system can be used to monitor currents and voltages in future research.

F. CHAPTER SUMMARY

In this chapter, a hardware design capable of producing the desired output current and voltage was presented. Components of the board were examined, and the printed circuit board was revealed. The FPGA system capable of driving the MOSFETS was also introduced. The board test results are introduced in the following chapter.

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V. HARDWARE RESULTS

A. INTRODUCTION

In this section, the SLR PCB is tested at a variety of operating points. The results are documented alongside the simulation results, and the analysis of the board is performed.

B. EXPERIMENTS

Two separate trials were run in the lab. The first tested the output of the PCB with a resistor, and the second used an emulated battery on the output terminals. The basic setup for Trial 1 is shown in Figure 19. A DC source represents the bus voltage, V_{bus} and the outputs are measured via the oscilloscope. The data points captured are then formatted in Matlab and included as laboratory plots.

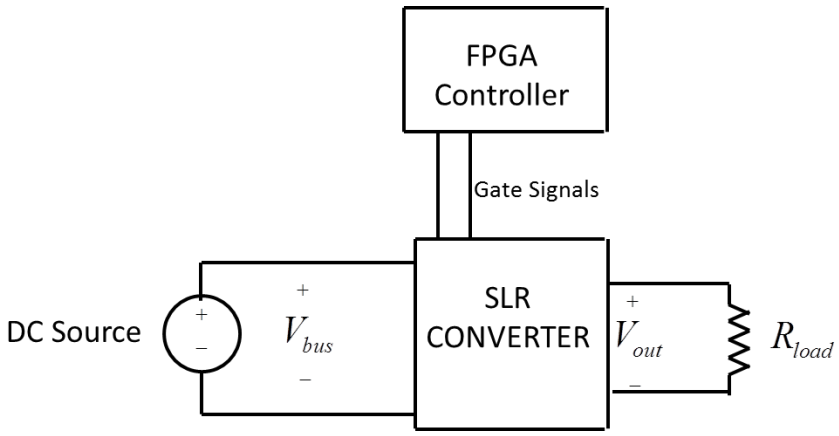

Figure 19. Basic laboratory setup with resistive load used only in Trial 1.

The waveforms captured on the oscilloscope are collected from the red lines in Figure 20. These waveforms are then compared to simulation data in the results section of each trial.

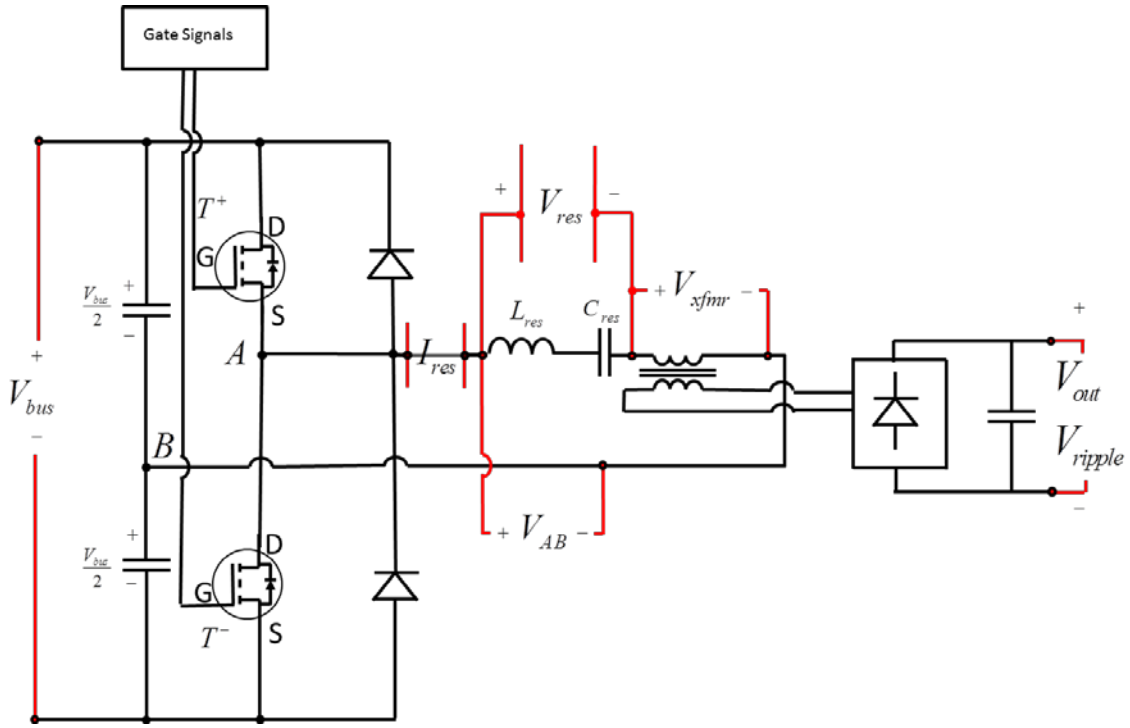

Figure 20. SLR topology including laboratory measurement points.

In Figure 21, the laboratory setup is pictured. At the bottom left is the Xilinx FPGA module, currently used to control the switching frequency on the MOSFETs. Trial 1 and Trials 2–5 used two separate boards with a different number of turns on the transformer.

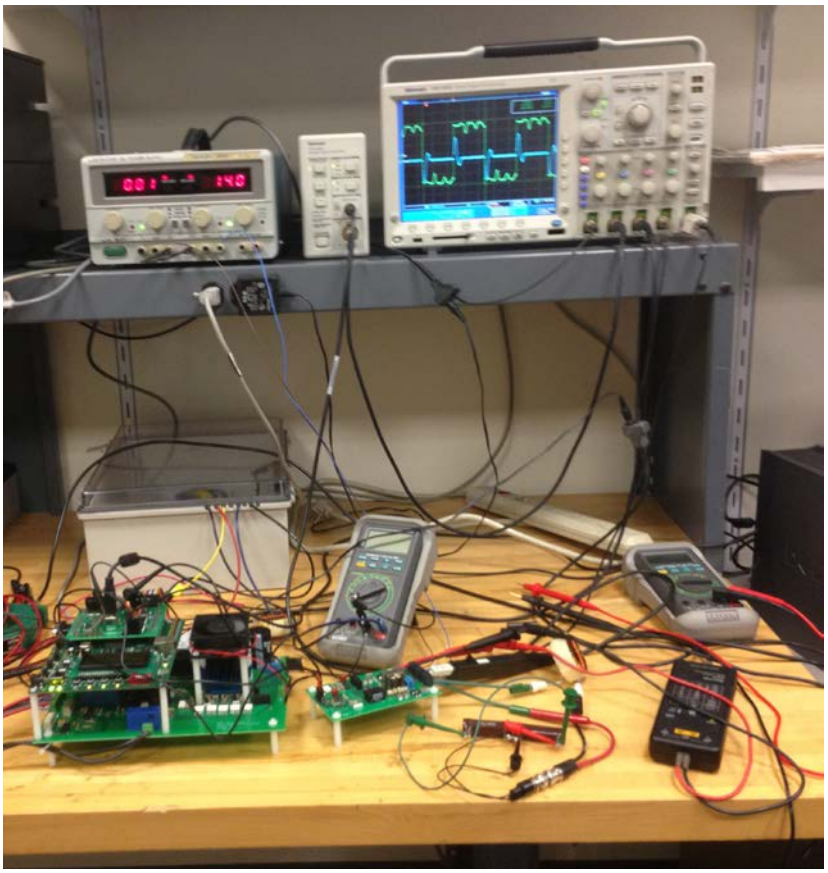

Figure 21. The laboratory setup includes the DC power source, SDC, and the oscilloscope.

C. TRIAL 1

1. Parameters

The parameters for Trial 1 are shown in Table 6. These parameters are similar to the simulation data, and some values are absent from the table that were hypothesized in the simulation.

Table 6. Trial 1 simulation and laboratory parameters.

Parameter	**Symbol**	**Value**
Resonant capacitors	C_{res}	20 nF
Resonant inductor	L_{res}	35 µH
Bus voltage	V_{bus}	62.4 V
Resonant inductor resistance	R_{lres}	420 mΩ
Magnetizing Inductance	L_m	0.7 mH
Transformer turns ratio	N_t	1.25
Output capacitance	C_{out}	30 µF
Switching frequency	f_s	28 kHz

2. Results

The results of Trial 1 are shown in Figure 22. The laboratory results are plotted against the simulation results for a close comparison of the waveforms. The waveforms shown are I_{res} and V_{res}, the current and the voltage across the resonant tank. There are a few disparities between the data which arise from a number of higher order effects not modeled in the Simulink model. The current reached −1 A in the simulation's second pulse, while the lab actually reached closer to −1.2 A. These non-symmetric differences could be an area for future research.

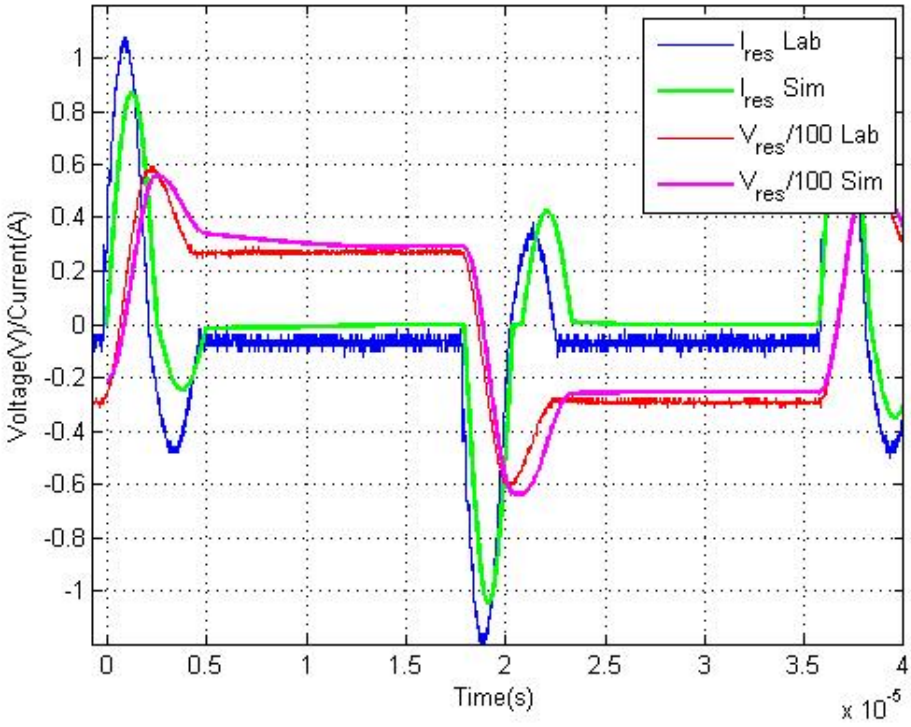

Figure 22. Resonant current and voltage waveforms from both laboratory and simulation, Trial 1.

Shown in Figure 23 is the voltage across the transformer V_{xfmr} from both the simulation and the laboratory. The main resonant intervals are identical, but the simulation does not accurately describe the zero voltage behavior on the transformer after the resonant tank has completed its first cycle. This does not appear on the waveforms from Figure 22. Additionally, a waveform present in the lab which was not implemented in the simulation is found after the initial pulse. These ringing effects are actually caused by the diodes D^+ and D^-. Once a diode shuts off, the diode behaves like a capacitor, and the circuit looks like a capacitor in series with the magnetizing inductance.

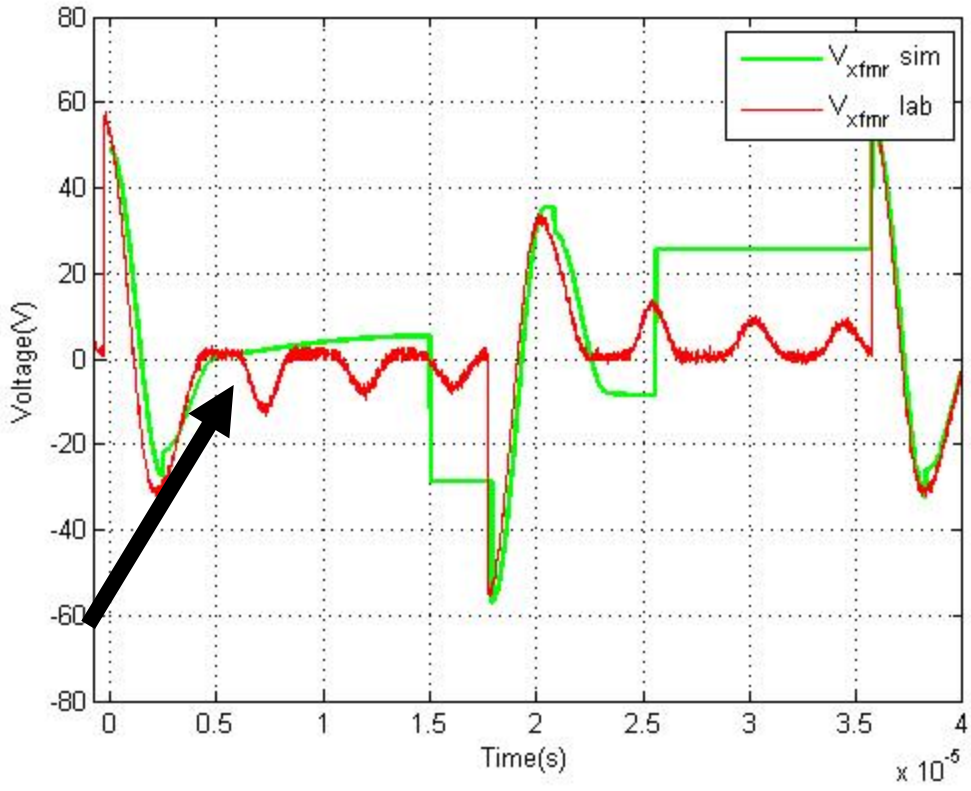

Figure 23. V_{xfmr} displays ringing that is not modeled in the simulation from Trial 1.

The effects of the MOSFET capacitance resonating after the switches closed are shown beneath the arrow. This frequency f_{s_off} is predicted to be the resonance of approximately

$$f_{s\_off} = \frac{\omega_o}{2\pi} = \frac{1}{2\pi\sqrt{2C_{ds}(L_m + L_{res})}} = \frac{1}{2\pi\sqrt{2(60\text{ pF})(.7\text{ mH} + 35\ \mu\text{H})}} = 535\text{ kHz}. \quad (15)$$

The voltage across the resonant tank V_{ab} is shown in both the simulation and the laboratory in Figure 24. Again, shown here are the second order effects caused by the conduction properties of the MOSFETS, discussed further in Section II.G. The simulation voltage is assumed to instantly drop to zero once the MOSFETs turn off, but in reality, the voltage stays high due to the residual charge left in the MOSFETS.

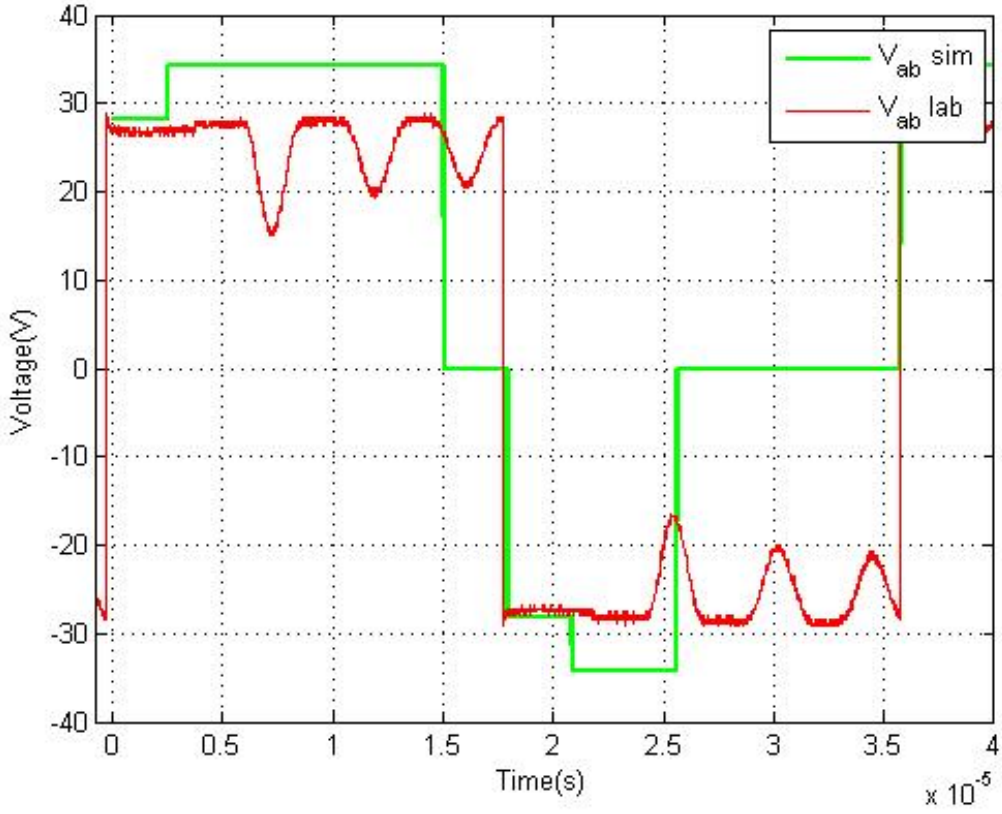

Figure 24. V_{ab} for both laboratory and simulation is shown from Trial 1.

D. TRIAL 2

1. Parameters

For Trials 2–5, the setup of the experiment is changed. The new setup is shown in Figure 25. A DC source is added across the output of the SLR converter to simulate the effects of a battery on the output of the converter. The output of the DC source V_{out} is changed to represent different charge states of the battery. In reality, this number fluctuates between 10 V and 14 V as a battery rises from its discharged state to a fully charged state. The parameters for Trial 2 are shown in Table 7.

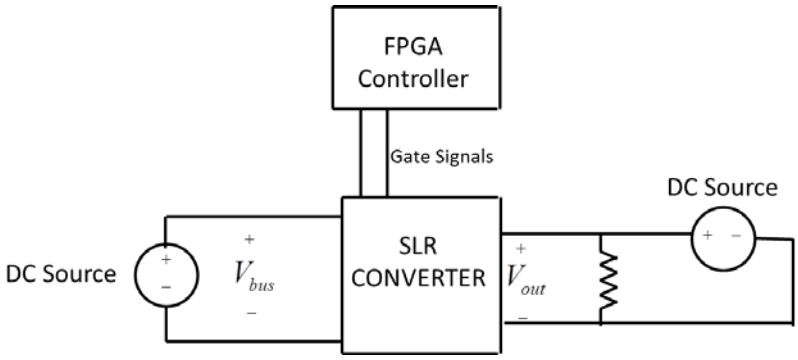

Figure 25. Testing with emulated battery output for Trials 2–5.

Table 7. Trial 2 simulation and laboratory parameters.

Parameter	**Symbol**	**Value**
Resonant capacitors	C_{res}	20 nF
Resonant inductor	L_{res}	35 µH
Bus voltage	V_{bus}	62.4 V
Magnetizing Inductance	L_m	3.76 mH
Transformer turns ratio	N_t	1
Switching frequency	f_s	48.6 kHz
Output Voltage	V_{out}	12.8 V
Output Current	I_{out}	226 mA

2. Results

The results of Trial 2 are shown in Figure 26. The arrow points to an area where the simulation and laboratory results do not align. In this area, the current in the simulation slowly decays and only switches into the second interval when $I_{res} = 0$. The

laboratory current decays much quicker into the negative pulse. The simulation does not account for laboratory effects which reset the transformer's core, and the waveforms do not align perfectly for this section.

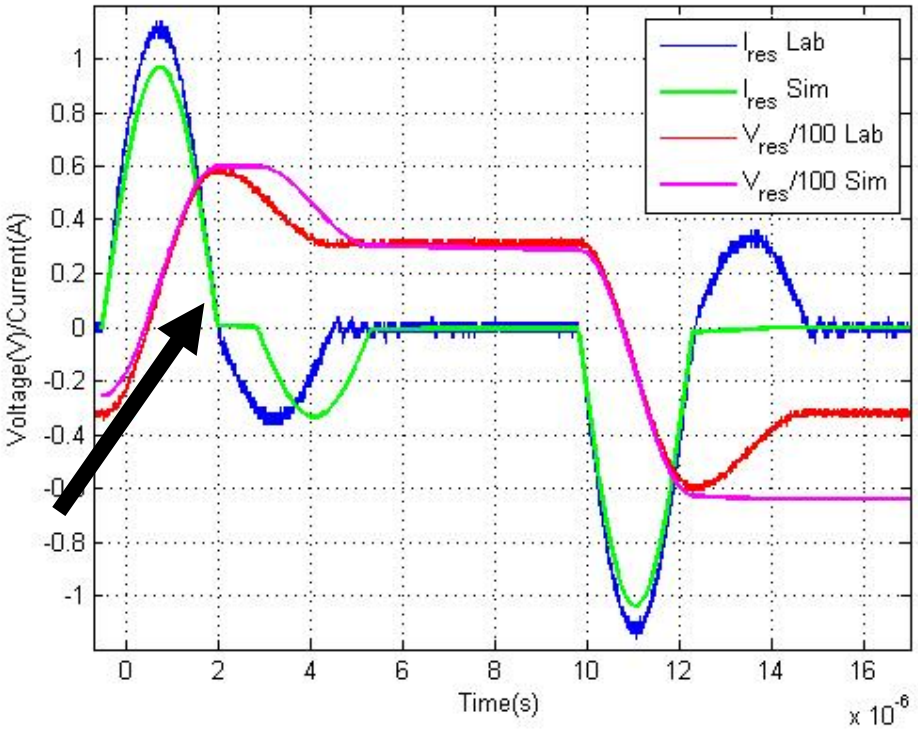

Figure 26. V_{res} and I_{res} are shown from simulation and laboratory for Trial 2.

The transformer voltage V_{xfmr} for both laboratory and simulation is shown in Figure 27. The same area mentioned in Figure 26 is pointed out with an arrow; the increased time between the positive and negative current pulse increases the amount of time it takes for the simulation V_{xfmr} to get back to zero.

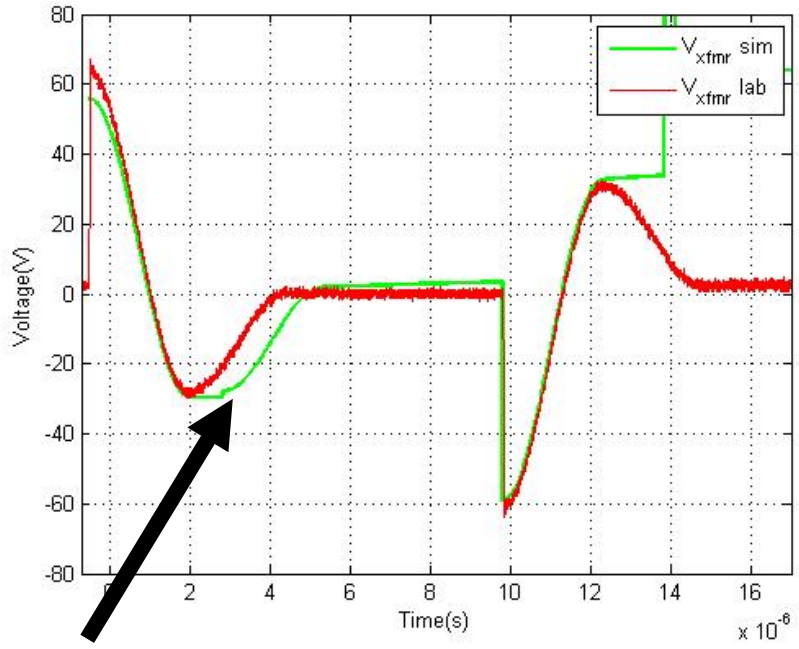

Figure 27. Transformer voltage V_{xfmr} is shown for both laboratory and simulation for Trial 2.

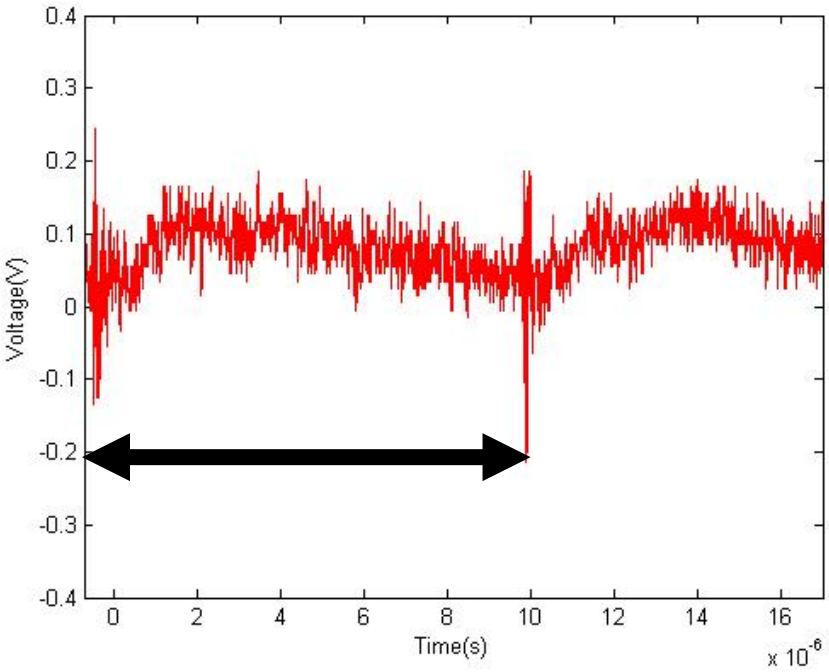

Figure 28. Voltage ripple V_{ripple} is shown after AC decoupling, laboratory only for Trial 2.

The ripple of the output voltage is shown in Figure 28. The frequency of the ripple is calculated using the time between the two spikes, annotated with a double arrow. The ripple frequency is 100 kHz, or approximately $2f_s$. This is consistent with two pulses per switching cycle, rectified at the output diodes of the converter.

E. TRIAL 3

1. Parameters

The parameters for Trial 3 are shown in Table 8.

Table 8. Trial 3 simulation and laboratory parameters.

Parameter	**Symbol**	**Value**
Resonant capacitors	C_{res}	20 nF
Resonant inductor	L_{res}	35 µH
Bus voltage	V_{bus}	62.4 V
Magnetizing Inductance	L_m	3.76 mH
Transformer turns ratio	N_t	1
Switching frequency	f_s	30.05 kHz
Output Voltage	V_{out}	12.8 V
Output Current	I_{out}	130 mA

2. Results

The results for Trial 3 are similar to the results from Trial 2. However, a decreased frequency led to a lower overall output current. The resonant current and voltage waveforms shown in Figure 29 are similar to the waveforms in Figure 26.

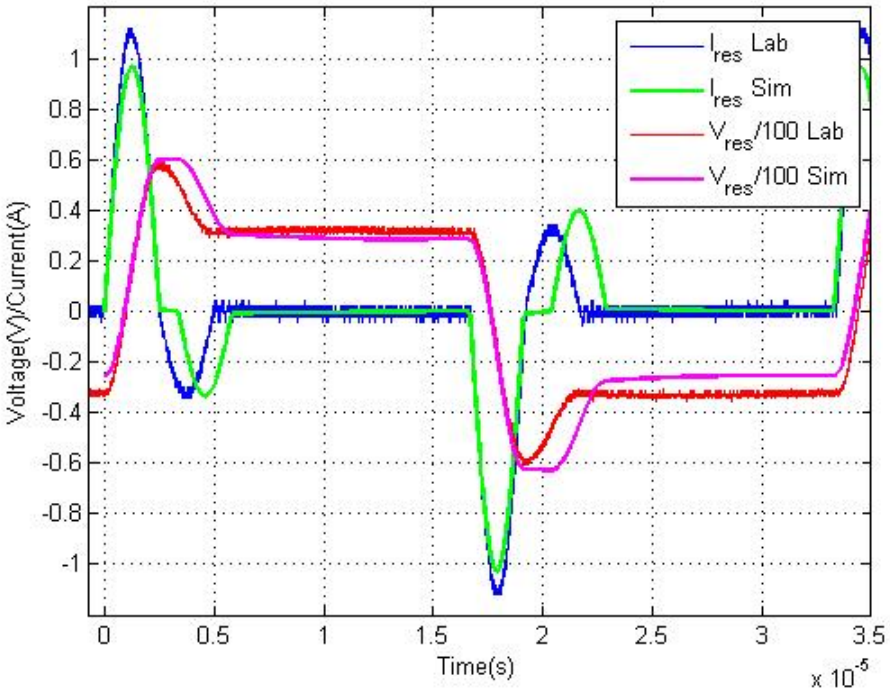

Figure 29. The resonant voltage and current V_{res} and I_{res} are shown from simulation and laboratory for Trial 3.

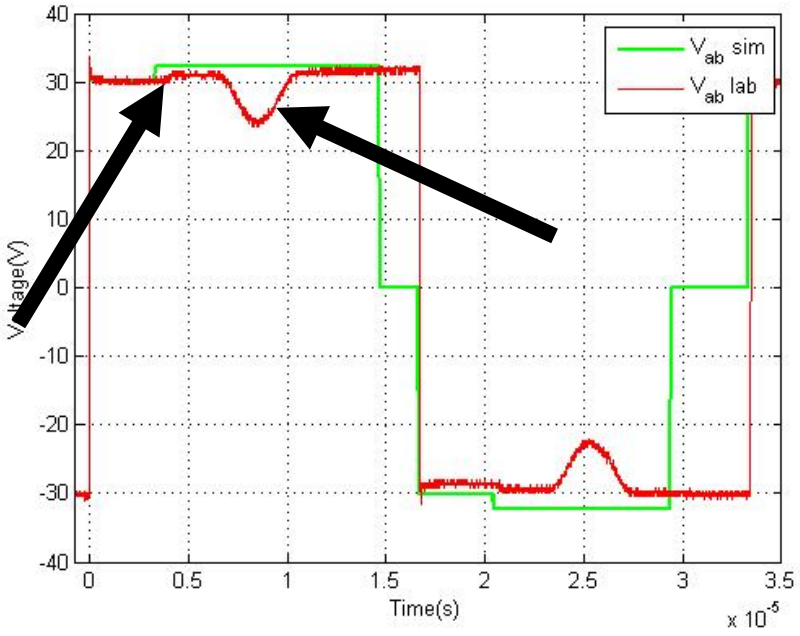

Figure 30. Voltage across the resonant tank and transformer V_{ab} is shown in both simulation and laboratory for Trial 3.

The voltage across the resonant tank is shown in Figure 30. At this output voltage and frequency, the arrows point out two events in the laboratory waveforms. The left arrow points to the switch turn off event. The voltage increases across the tank as the MOSFET switches off. This voltage is predicted to be 0.8 V at 0.6 A, based on the MOSFET data sheet for source-drain diode forward voltage [13]. The second arrow refers to the body diode recovery event briefly dropping the voltage as current flows out of the MOSFET. The voltage applied to the transformer for Trial 3 is shown in Figure 31.

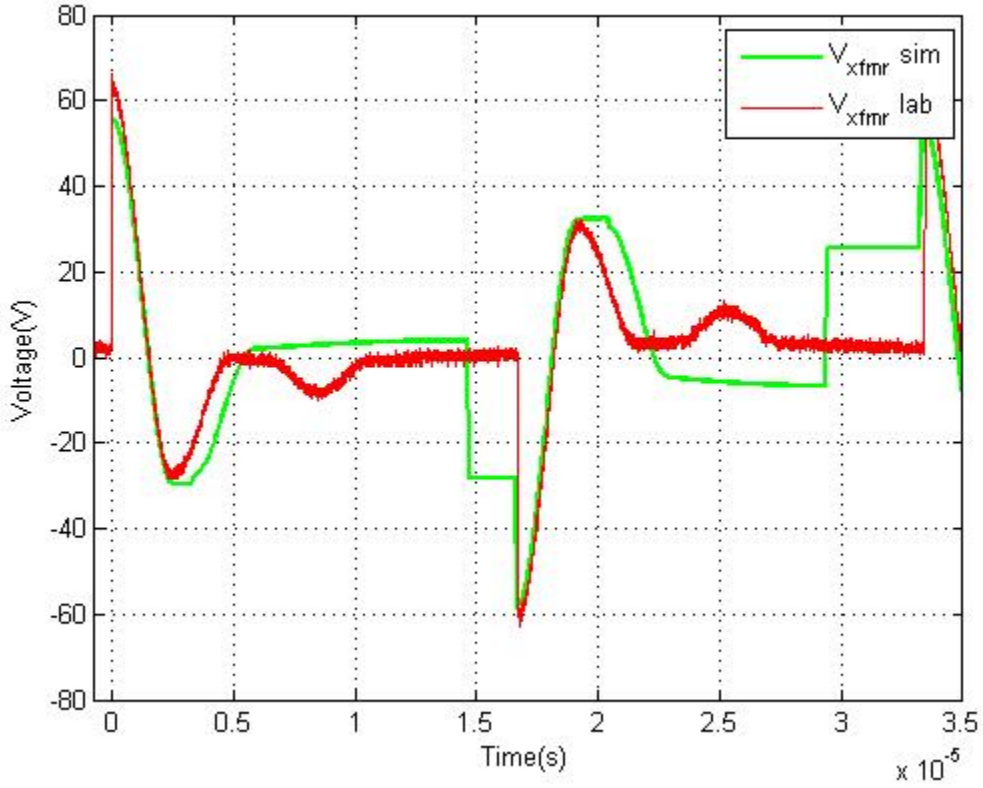

Figure 31. Transformer voltage V_{xfmr} is shown for both laboratory and simulation for Trial 3.

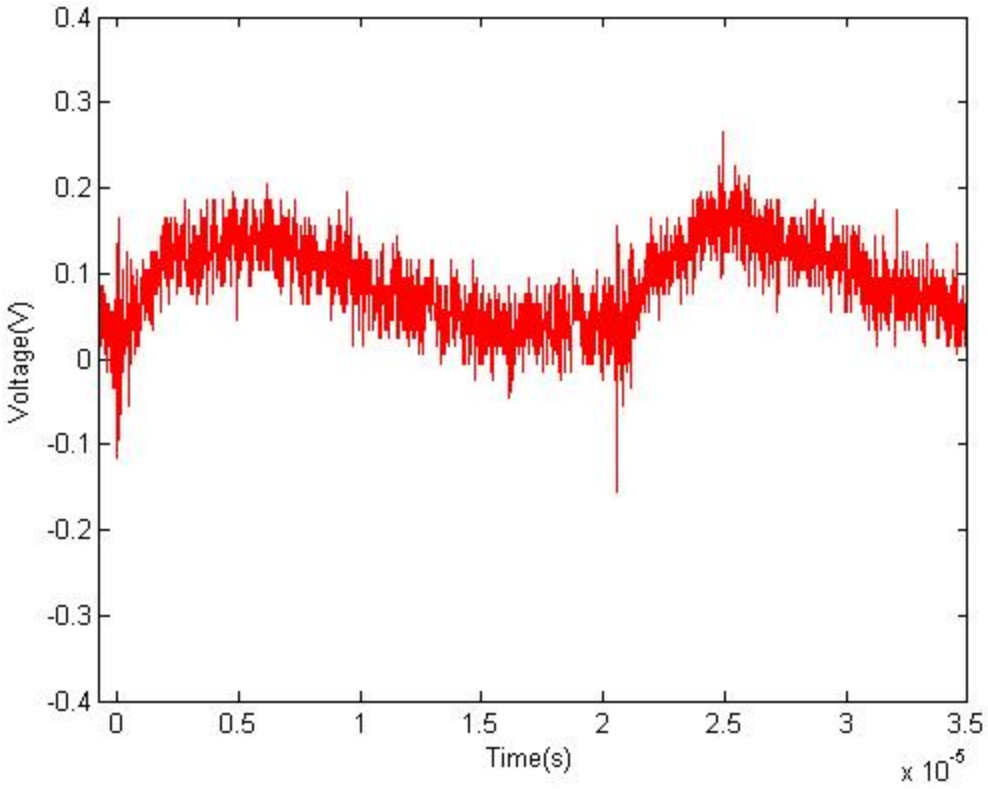

Figure 32. Voltage ripple V_{ripple} is shown after AC decoupling, lab only for Trial 3.

At a lower switching frequency, the frequency of the ripple voltage is now 58 kHz as shown in Figure 32.

F. TRIAL 4

1. Parameters

The parameters for Trial 4 are shown in Table 9. The converter is simulated and measured at a lower output voltage.

Table 9. Trial 4 simulation and laboratory parameters.

Parameter	**Symbol**	**Value**
Resonant capacitors	C_{res}	20 nF
Resonant inductor	L_{res}	35 µH
Bus voltage	V_{bus}	62.4 V
Magnetizing Inductance	L_m	3.76 mH
Transformer turns ratio	N_t	1
Switching frequency	f_s	24.4 kHz
Output Voltage	V_{out}	7.8 V
Output Current	I_{out}	130 mA

2. Results

At a lower output voltage, the converter's resonant current and voltage behave similarly to Trials 2 and 3, shown in Figure 33.

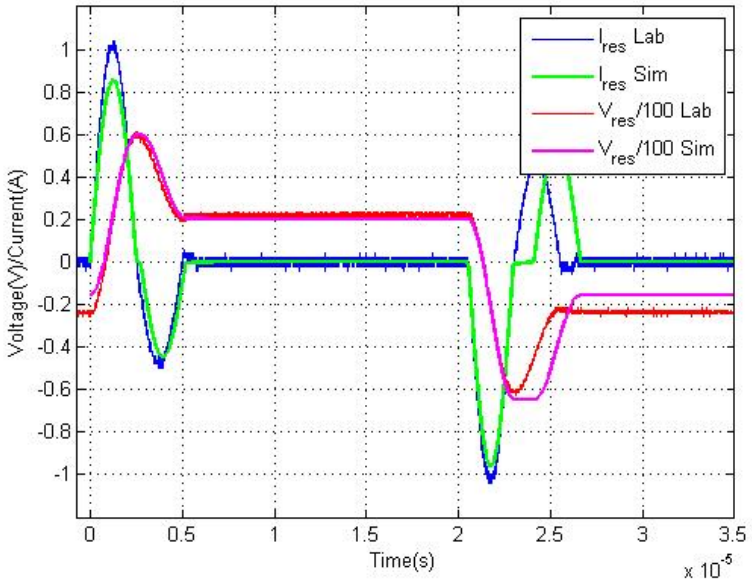

Figure 33. The simulation and laboratory V_{res} and I_{res} are shown for Trial 4.

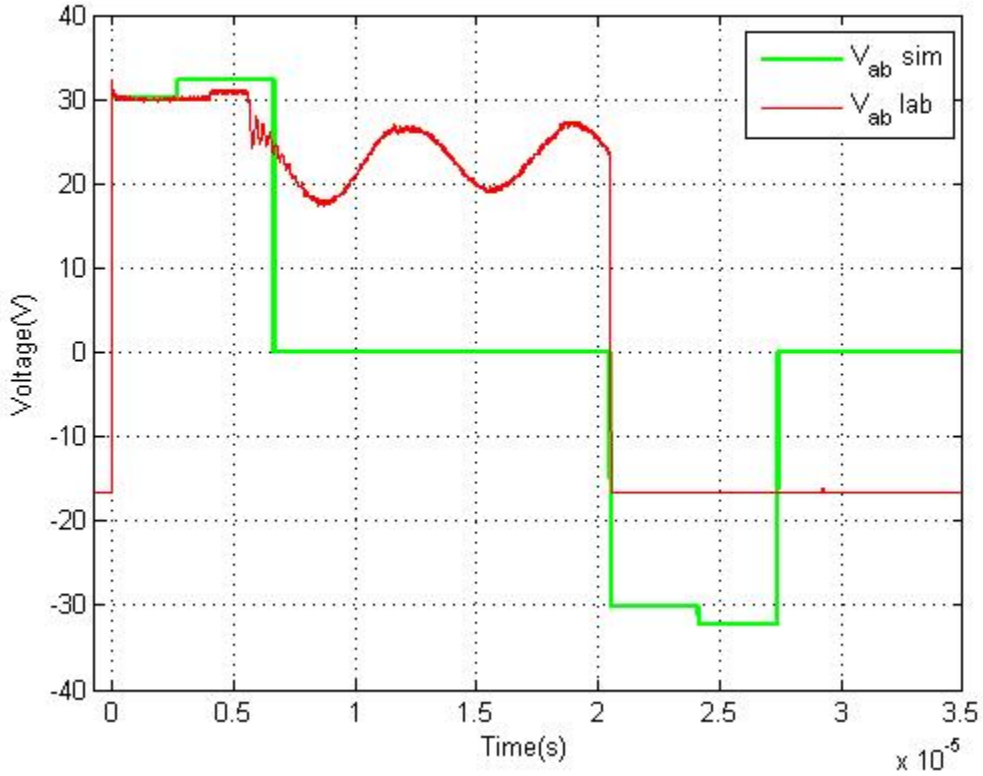

Figure 34. The simulation and laboratory V_{ab} is shown for trial 4.

At a lower output voltage shown in Figure 34, V_{ab} begins to resonate at a higher frequency that is consistent with the transformer magnetizing inductance in series with the MOSFET capacitance, which is measured to be 150kHz. Consistent with our hypothesis, the frequency is about three times lower than the frequency in Trial 1, as it is dependent on the magnetizing inductance L_m. The predicted frequency is

$$f_o = \frac{\omega_o}{2\pi} = \frac{1}{2\pi\sqrt{2C_{ds}(L_m + L_{res})}} = \frac{1}{2\pi\sqrt{2(60\text{ pF})(3.7\text{ mH} + 32\ \mu\text{H})}} = 237\text{ kHz.} \quad (16)$$

These second order effects are not captured in the simulation.

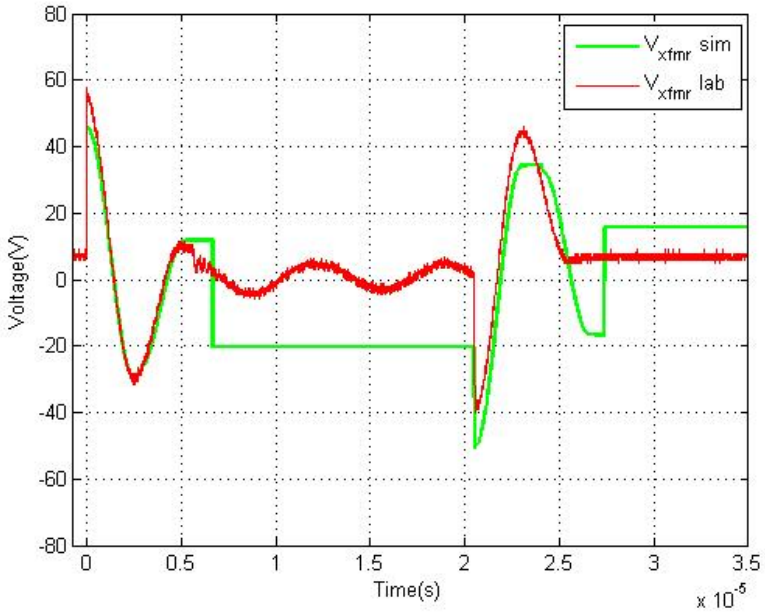

Figure 35. V_{xfmr} for both laboratory and simulation for Trial 4.

The same ringing effects are shown to occur in the voltage waveforms across the transformer as well in Figure 35.

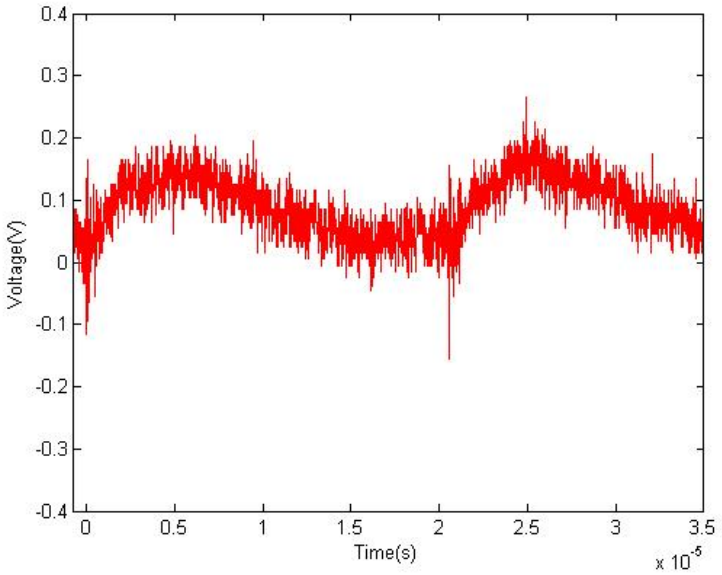

Figure 36. Voltage ripple V_{ripple} is shown after AC decoupling for laboratory only from Trial 4.

As expected the ripple voltage has a frequency of twice the switching frequency, 50kHz, shown in Figure 36.

G. TRIAL 5

1. Parameters

The parameters used for Trial 5 are shown in Table 10. The switching frequency is raised significantly, as well as the output voltage.

Table 10. Trial 5 simulation and laboratory parameters.

Parameter	**Symbol**	**Value**
Resonant capacitors	C_{res}	20 nF
Resonant inductor	L_{res}	35 µH
Bus voltage	V_{bus}	62.4 V
Magnetizing Inductance	L_m	3.76 mH
Transformer turns ratio	N_t	1
Switching frequency	f_s	78 kHz
Output Voltage	V_{out}	11.6 V
Output Current	I_{out}	3 mA

2. Results

The voltage and current resonant waveforms shown in Figure 37 are shown with only three total pulses (three switch on events). The simulation cannot handle high frequencies because state two relies on the current falling to zero before state three can occur. If this takes too long, the simulation will switch to the negative pulse while current is still flowing and enter undesirable states. These undesirable states are not pictured.

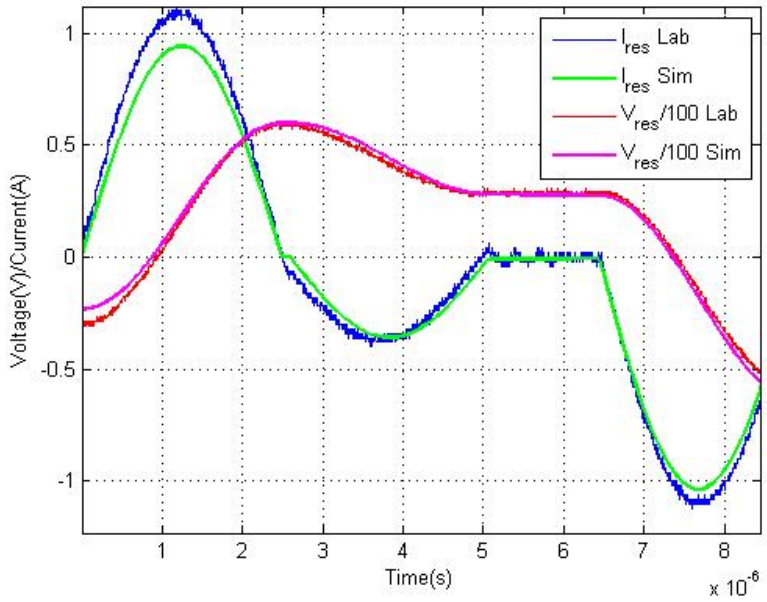

Figure 37. The resonant voltage and current V_{res} and I_{res} are shown from laboratory and simulation for Trial 5.

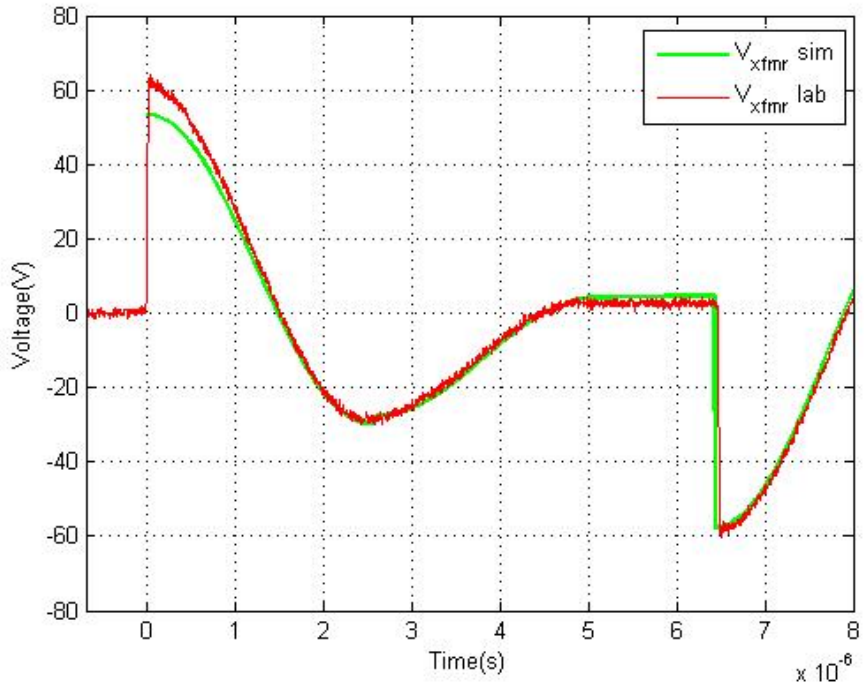

Figure 38. Transformer voltage V_{xfmr} is shown for both laboratory and simulation from Trial 5.

The transformer voltage for Trial 5 is shown in Figure 38. It behaves similarly to the simulation.

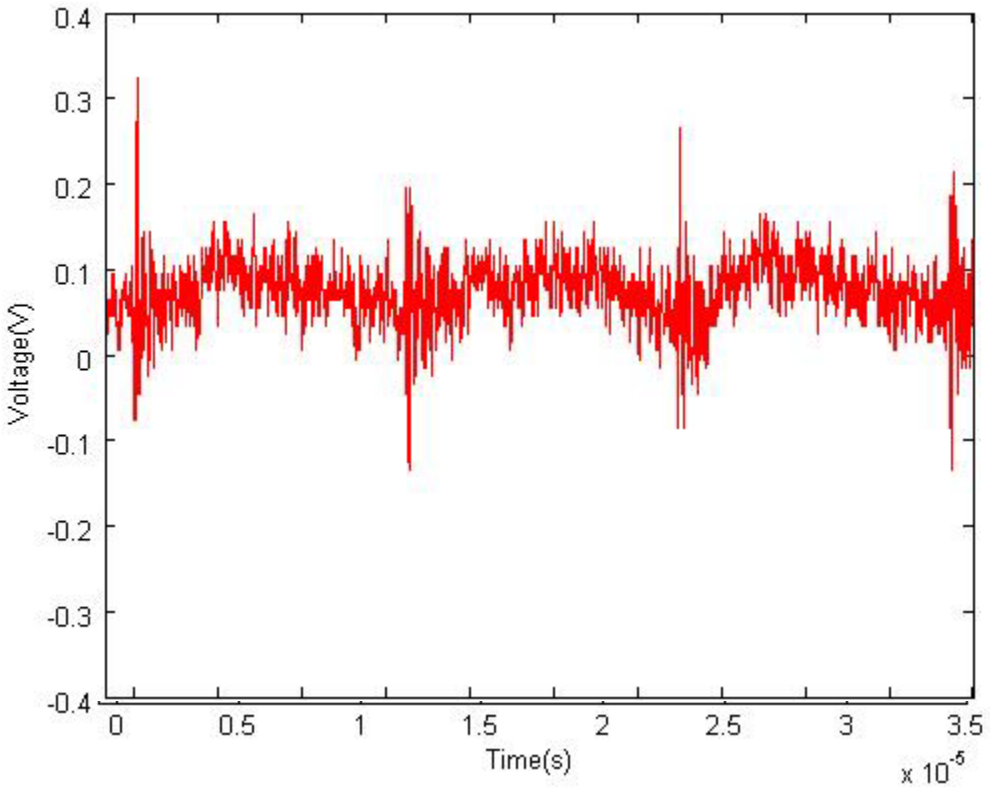

Figure 39. Voltage ripple V_{ripple} is shown after AC decoupling, lab only for Trial 5.

At higher frequencies, the output ripple voltage now jumps to 153 kHz shown in Figure 39.

H. FINAL RESULTS

The cumulative results from all five trials are tabulated in Table 11.

Table 11. Trial comparisons

	Trial 1	**Trial 2**	**Trial 3**	**Trial 4**	**Trial 5**
$V_{bus}(V)$	62.4	62.4	62.4	62.4	62.4
V_{out}(V)	8.4	12.8	12.8	7.8	11.6
f_{sw}(kHz)	28	48.6	30.05	24.4	78
$I_{out}lab$(mA)	-	226	130	119	363
$I_{out}sim$(mA)	127	220	127	110	354
$I_{res\_peak}lab$(mA)	1.05	1.05	1.1	1.02	1.08
$I_{res\_peak}sim$(mA)	1.00	.95	.97	.85	.95
$V_{res\_peak}lab$(V)	58	58	58	60	59
$V_{res\_peak}sim$(V)	62	60	60	60	60
ΔV_{ripple}	-	.15	.2	.2	.15
$f_{Vripple}$(kHz)	-	100	58	50	153
N_t	1.25	1	1	1	1

The amplitude of the output V_{ripple} signal is ΔV_{ripple} and is measured from the gathered laboratory data. The converter is shown to behave similarly to a current source, and the output current is verifies equation (5) in Section II.E, which was used to calculate the expected output current. At a constant input voltage, the converter maintains a peak resonant voltage of about 60 V across both laboratory and simulation data. As frequency changed and V_{bus} remained constant, the converter was able to shape the output current. Therefore, the converter is successful up to its peak output current of 373 mA for at switching frequencies of 78 kHz.

The amplitude of the voltage ripple remained relatively constant across all trials, as the output capacitors on the board remained the same for all trials. However, the frequency $f_{Vripple}$ increased or decreased in proportion to the switching frequency.

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VI. CONCLUSIONS AND FUTURE RESEARCH

A. CONCLUSIONS

The SLR converter presented in this paper has been verified to operate within the desired conditions. The equations were developed for each mode of operation and implemented in a Simulink model. The design was then implemented in the lab using a printed circuit board, and a FPGA was used to control the switching waveforms driving the MOSFETs.

A series of similar trials was performed to examine the effects of various output voltages and changing commanded switching frequencies on the board and its modes of operation. The board performed similarly to the simulation results and will be able to supply the necessary amounts of current to trickle charge a battery.

If the board is operated beyond the desired operating characteristics, the MOSFETS and the transformer will be the two components which limit the circuit the most. Primarily the MOSFETS will fail from overvoltage before the transformer overheats. The MOSFETS can fail instantly, but the transformer will take more time operating out of its designed operating zone to fail.

B. FUTURE RESEARCH

In order to more accurately predict the laboratory outcomes, higher order effects in the model will enable a more accurate simulation.

If this board is used in conjunction with other similar boards, it will be possible to regulate a string of batteries using individual control loops for each individual battery. The FPGA controller could easily be placed onto a single microprocessor for large scale manufacturing. Further design work could help to miniaturize components and optimize space consumption in the board.

Using the simulation, we could predict operation using other resonant frequencies, and optimize for different switching frequencies and design points.

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APPENDIX A. DATASHEETS

Advanced Power MOSFET **IRFM120A**

IEEE802.3af Compatible

FEATURES

- ❑ Avalanche Rugged Technology
- ❑ Rugged Gate Oxide Technology
- ❑ Lower Input Capacitance
- ❑ Improved Gate Charge
- ❑ Extended Safe Operating Area
- ❑ Lower Leakage Current : 10 μA (Max.) @ V_{DS} = 100V
- ❑ Lower $R_{DS(ON)}$: 0.155 Ω (Typ.)

BV_{DSS} = 100 V
$R_{DS(on)}$ = 0.2 Ω
I_D = 2.3 A

SOT-223

1. Gate 2. Drain 3. Source

Absolute Maximum Ratings

Symbol	Characteristic	Value	Units
V_{DSS}	Drain-to-Source Voltage	100	V
I_D	Continuous Drain Current (T_A=25℃)	2.3	A
	Continuous Drain Current (T_A=70℃)	1.84	
I_{DM}	Drain Current-Pulsed ①	18	A
V_{GS}	Gate-to-Source Voltage	±20	V
E_{AS}	Single Pulsed Avalanche Energy ②	123	mJ
I_{AR}	Avalanche Current ①	2.3	A
E_{AR}	Repetitive Avalanche Energy ①	0.24	mJ
dv/dt	Peak Diode Recovery dv/dt ③	6.5	V/ns
P_D	Total Power Dissipation (T_A=25℃) *	2.4	W
	Linear Derating Factor *	0.019	W/℃
T_J , T_{STG}	Operating Junction and Storage Temperature Range	- 55 to +150	℃
T_L	Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5-seconds	300	

Thermal Resistance

Symbol	Characteristic	Typ.	Max.	Units
$R_{\theta JA}$	Junction-to-Ambient *	--	52	℃/W

* When mounted on the minimum pad size recommended (PCB Mount).

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Rev. C

Electrical Characteristics (T_A=25℃ unless otherwise specified)

Symbol	Characteristic	Min.	Typ.	Max.	Units	Test Condition
BV_{DSS}	Drain-Source Breakdown Voltage	100	--	--	V	V_{GS}=0V, I_D=250μA
$\Delta BV/\Delta T_J$	Breakdown Voltage Temp. Coeff.	--	0.12	--	V/℃	I_D=250μA ***See Fig 7***
$V_{GS(th)}$	Gate Threshold Voltage	2.0	--	4.0	V	V_{DS}=5V, I_D=250μA
I_{GSS}	Gate-Source Leakage , Forward	--	--	100	nA	V_{GS}=20V
	Gate-Source Leakage , Reverse	--	--	-100		V_{GS}=-20V
I_{DSS}	Drain-to-Source Leakage Current	--	--	1	μA	V_{DS}=30V ⑤
		--	--	10		V_{DS}=100V
		--	--	100		V_{DS}=80V, T_A=125℃
$R_{DS(on)}$	Static Drain-Source On-State Resistance	--	--	0.2	Ω	V_{GS}=10V, I_D=1.15A ④
g_{fs}	Forward Transconductance	--	3.12	--	S	V_{DS}=40V, I_D=1.15A ④
C_{iss}	Input Capacitance	--	370	480	pF	V_{GS}=0V, V_{DS}=25V, f =1MHz ***See Fig 5***
C_{oss}	Output Capacitance	--	95	110		
C_{rss}	Reverse Transfer Capacitance	--	38	45		
$t_{d(on)}$	Turn-On Delay Time	--	14	40	ns	V_{DD}=50V, I_D=9.2A, R_G=18Ω ***See Fig 13*** ④ ⑤
t_r	Rise Time	--	14	40		
$t_{d(off)}$	Turn-Off Delay Time	--	36	90		
t_f	Fall Time	--	28	70		
Q_g	Total Gate Charge	--	16	22	nC	V_{DS}=80V, V_{GS}=10V, I_D=9.2A ***See Fig 6 & Fig 12*** ④ ⑤
Q_{gs}	Gate-Source Charge	--	2.7	--		
Q_{gd}	Gate-Drain("Miller") Charge	--	7.8	--		

Source-Drain Diode Ratings and Characteristics

Symbol	Characteristic	Min.	Typ.	Max.	Units	Test Condition
I_S	Continuous Source Current	--	--	2.3	A	Integral reverse pn-diode in the MOSFET
I_{SM}	Pulsed-Source Current ①	--	--	18		
V_{SD}	Diode Forward Voltage ④	--	--	1.5	V	T_J=25℃, I_S=2.3A, V_{GS}=0V
t_{rr}	Reverse Recovery Time	--	98	--	ns	T_J=25℃, I_F=9.2A
Q_{rr}	Reverse Recovery Charge	--	0.34	--	μC	di_F/dt=100A/μs ④

Notes ;

① Repetitive Rating : Pulse Width Limited by Maximum Junction Temperature
② L=35mH, I_{AS}=2.3A, V_{DD}=25V, R_G=27Ω, Starting T_J=25℃
③ I_{SD}≤9.2A, di/dt≤300A/μs, V_{DD}≤BV_{DSS}, Starting T_J=25℃
④ Pulse Test : Pulse Width = 250μs, Duty Cycle ≤ 2%
⑤ Essentially Independent of Operating Temperature
⑥ Adjusted for Cisco

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Fig 1. Output Characteristics

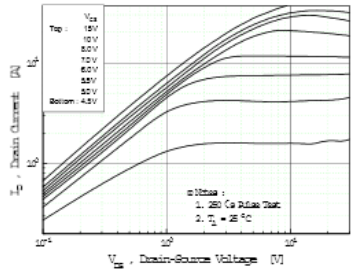

Fig 2. Transfer Characteristics

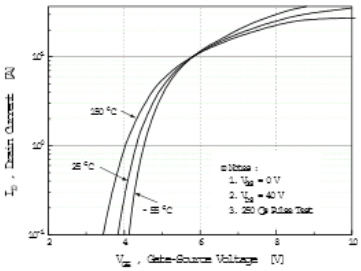

Fig 3. On-Resistance vs. Drain Current

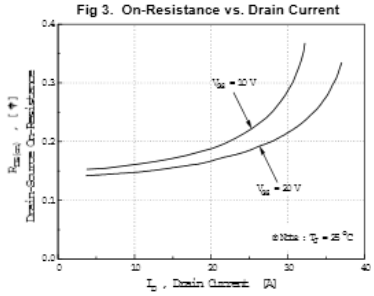

Fig 4. Source-Drain Diode Forward Voltage

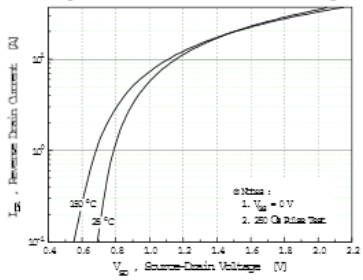

Fig 5. Capacitance vs. Drain-Source Voltage

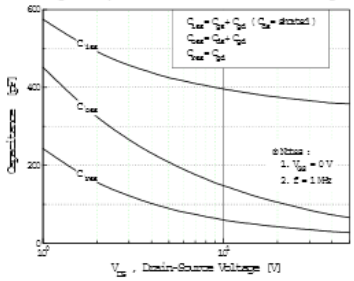

Fig 6. Gate Charge vs. Gate-Source Voltage

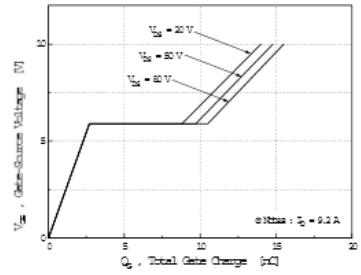

Fig 7. Breakdown Voltage vs. Temperature

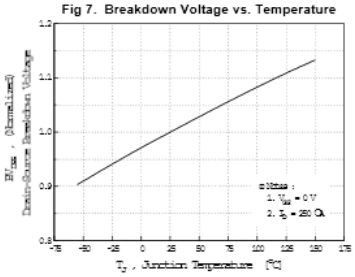

Fig 8. On-Resistance vs. Temperature

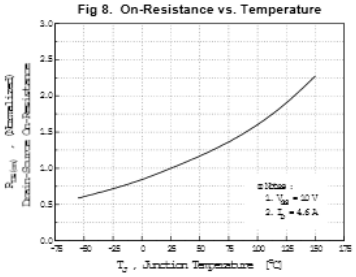

Fig 9. Max. Safe Operating Area

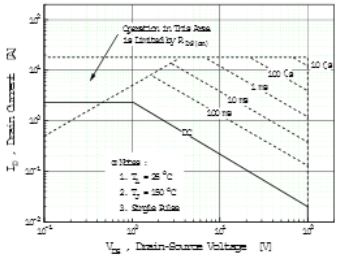

Fig 10. Max. Drain Current vs. Ambient Temperature

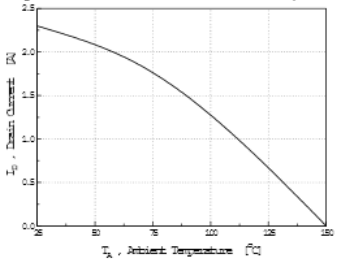

Fig 11. Thermal Response

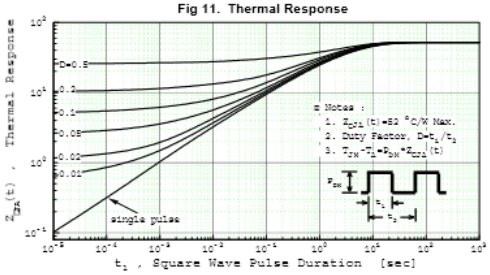

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Fig 12. Gate Charge Test Circuit & Waveform

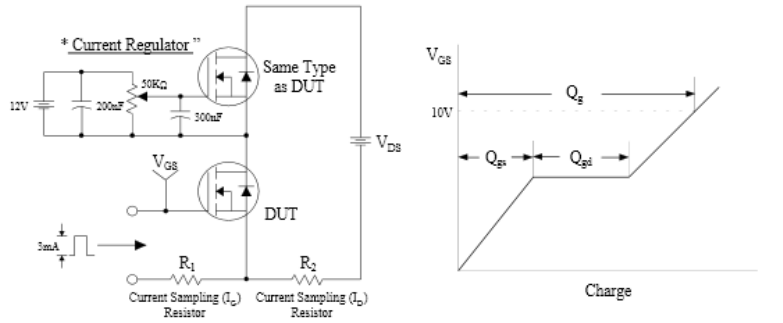


Fig 13. Resistive Switching Test Circuit & Waveforms

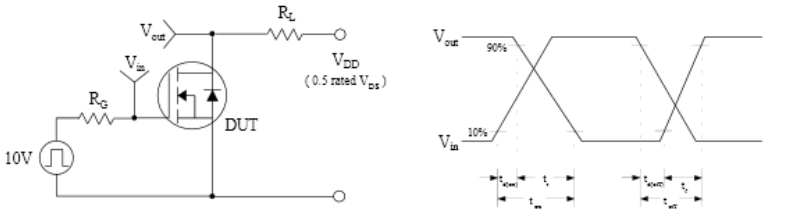


Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms

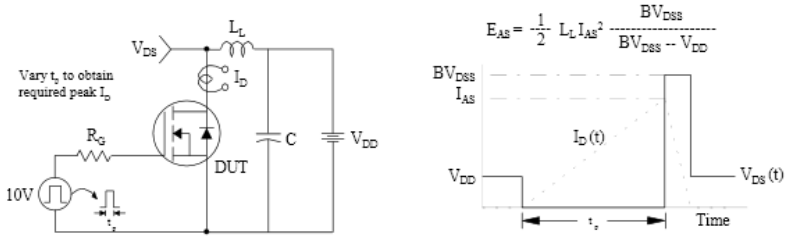
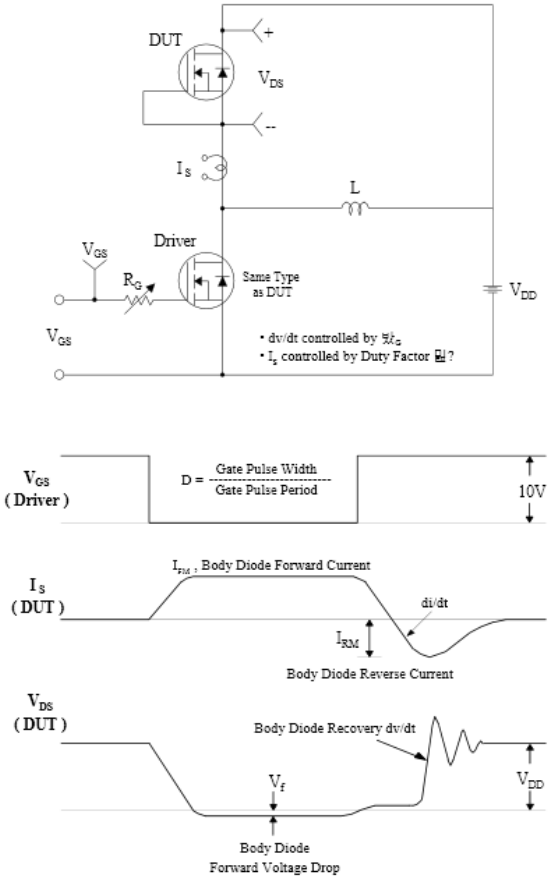


Fig 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms



Transformer Design

Magnetics offers two methods to select a ferrite core for a power application.

CORE SELECTION BY POWER HANDLING CAPACITY

The Power Chart characterizes the power handling capacity of each ferrite core based upon the frequency of operation, the circuit topology, the flux level selected, and the amount of power required by the circuit. If these four specifics are known, the core can be selected from the Power Chart on page 6.

CORE SELECTION BY WaAc PRODUCT

The power handling capacity of a transformer core can also be determined by its WaAc product, where Wa is the available core window area, and Ac is the effective core cross-sectional area. Using the equation shown below, calculate the WaAc product and then use the Area Product Distribution (WaAc) Chart to select the appropriate core.

$$WaAc = \frac{P_o D_{cma}}{K_t B_{max} f}$$

WaAc = Product of window area and core area (cm^4)

P_o = Power Out (watts)

D_{cma} = Current Density (cir. mils/amp) Current density can be selected depending upon the amount of heat rise allowed. 750 cir. mils/amp is conservative; 500 cir. mils is aggressive.

B_{max} = Flux Density (gauss) selected based upon frequency of operation. Above 20kHz, core losses increase. To operate ferrite cores at higher frequencies, it is necessary to operate the core flux levels lower than ± 2 kg. The Flux Density vs. Frequency chart shows the reduction in flux levels required to maintain 100 mW/cm^3 core losses at various frequencies, with a maximum temperature rise of 25°C. for a typical power material, MAGNETICS P.

A_c = Core area in cm^2

f = frequency (hertz)

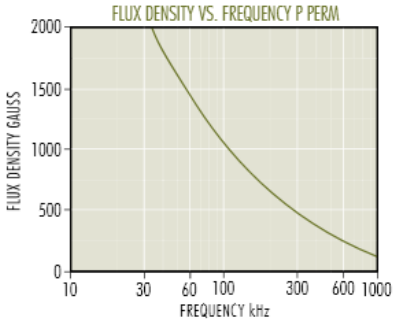
K_t = Topology constant (for a space factor of 0.4).

Topology constants K_t

Forward converter = 0.0005
Push-Pull = 0.001
Half-bridge = 0.0014
Full-bridge = 0.0014
Flyback = 0.00033 (single winding)
Flyback = 0.00025 (multiple winding)

For individual cores, WaAc is listed in this catalog under "Magnetic Data."

The WaAc formula was obtained from derivations in Chapter 7 of A. I. Pressman's book, "Switching Power Supply Design. Choice of B_{max} at various frequencies, D_{cma} and alternative transformer temperature rise calculations are also discussed in Chapter 7 of the Pressman book.



Once a core is chosen, the calculation of primary and secondary turns and wire size is readily accomplished.

$$Np = \frac{V_p \times 10^8}{4BA_c} \qquad N_s = \frac{V_s}{V_p} Np$$

$$I_p = \frac{P_{in}}{E_{in}} \frac{P_{out}}{eE_{in}} \qquad I_s = \frac{P_{out}}{E_{out}}$$

$KWa = N_pA_{wp} + N_sA_{ws}$
Where
A_{wp} = primary wire area A_{ws} = secondary wire area
Assume K = .4 for toroids; .6 for pot cores and E-U-I cores
Assume $N_sA_{ws} = 1.1\ N_pA_{wp}$ to allow for losses and feedback winding

$$\text{efficiency } e = \frac{P_{out}}{E_{in}} = \frac{P_{out}}{P_{out} + \text{wire losses} + \text{core losses}}$$

$$\text{Voltage Regulation (\%)} = \frac{R_s + (N_s/N_p)^2 R_p}{R_{load}} \times 100$$

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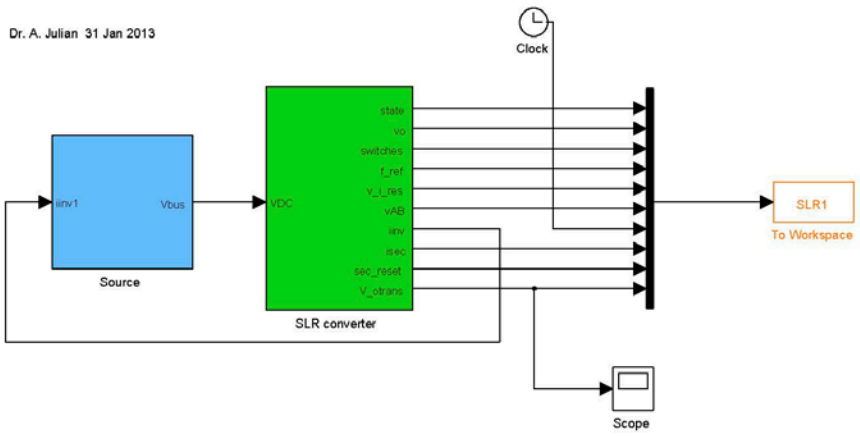
APPENDIX B. MATLAB CODE AND SIMULATION

```
%31 Jan 2013
% This code is run at the start of the simulation
close all;
clear all;
Vb=62.4;     % ideal source in battery model
% Cbus_ic=Vb;
Kp_v=200;
Ki_v=1000000;

Lres=32e-6;% only 35 in circuit, changed to 32 to match lab data
Cres=18e-9;
wo=1/sqrt(Lres*Cres)
Zo=sqrt(Lres/Cres);
tres=2*pi/wo;
tstep = 10e-9;
tstop=.0005;

R_ind=.14*3;
%fsw=wo/2/pi/12;
fsw=78000;
%fsw=wo/2/pi/2*1.9;
Lm=3700e-6;
Llp=1e-6;
Lls=2e-6;
Rp=.01;
Rs=.01;
N_mat= [Lres+Llp+Lm Lm; Lm Lls+Lm];
O_mat= [R_ind+Rp 0;0 Rs];
A_mat=-inv(N_mat)*O_mat;
B_mat=inv(N_mat);
%Transformer
Nt=1;    %

Vdcic2=11.6; %initial output voltage
Cout=30e-6;      % capacitor that is being charged
Rload=20;    % Resistive load on capacitor being charged

vr_ic2=-2*Vdcic2*Nt;
ir_ic=0;\
% IGBT characteristics
v_igbt=.5;
v_diode=.5;
```

SLR_charger_in_lab



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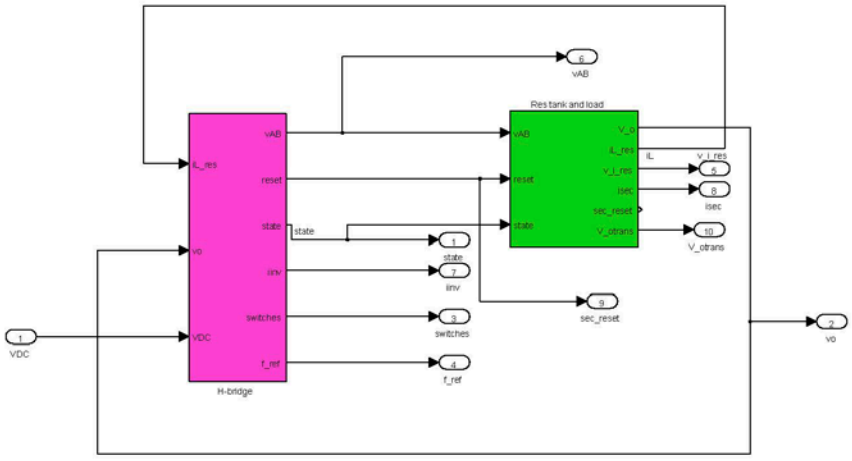
SLR_charger_in_lab/SLR converter



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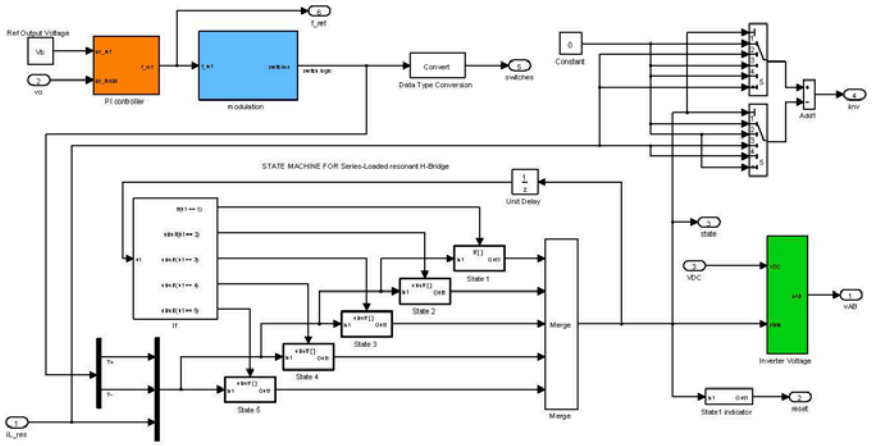
SLR_charger_in_lab/SLR converter/ H-bridge



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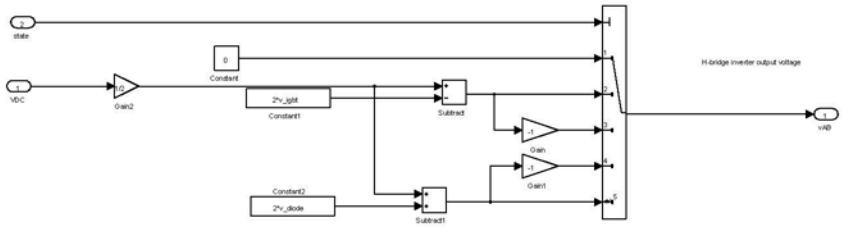
SLR_charger_in_lab/SLR converter/ H-bridge/Inverter Voltage



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SLR_charger_in_lab/SLR converter/ H-bridge/PI controller

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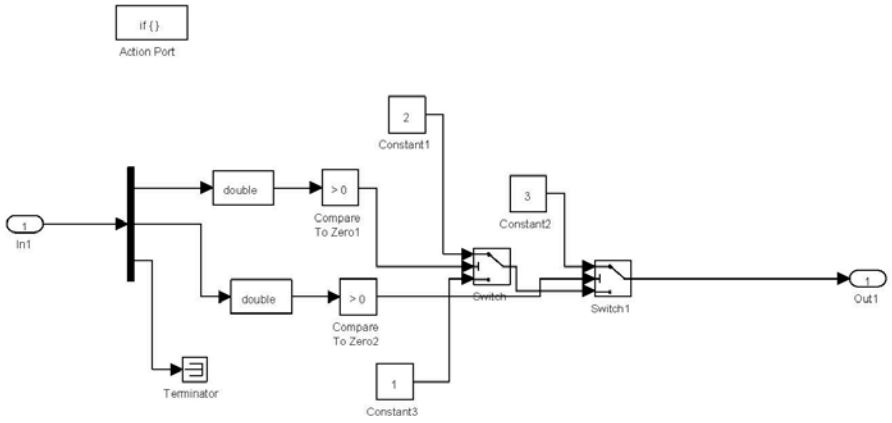
SLR_charger_in_lab/SLR converter/ H-bridge/State 1



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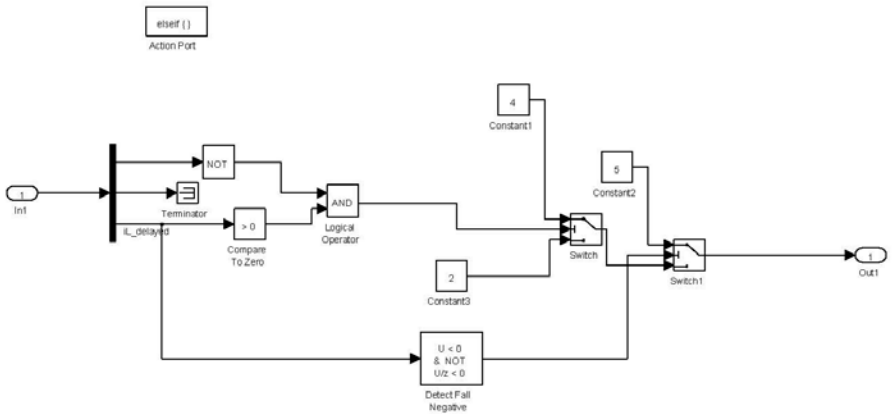
SLR_charger_in_lab/SLR converter/ H-bridge/State 2



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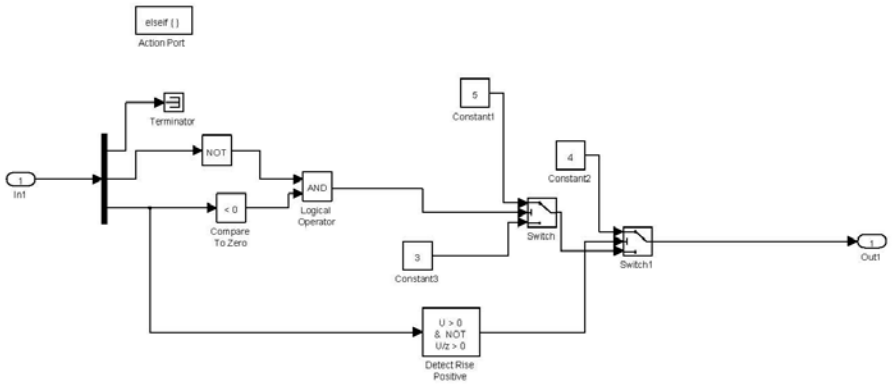
SLR_charger_in_lab/SLR converter/ H-bridge/State 3



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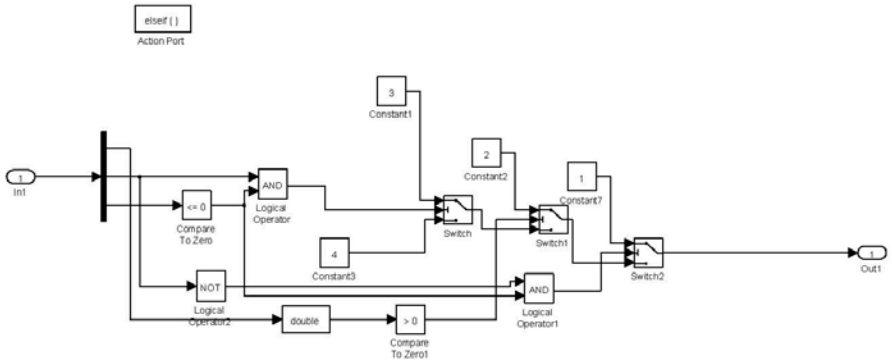
SLR_charger_in_lab/SLR converter/ H-bridge/State 4



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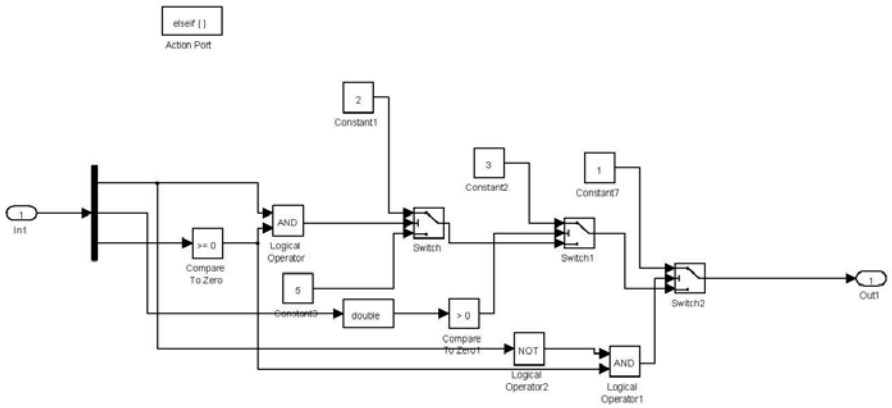
SLR_charger_in_lab/SLR converter/ H-bridge/State 5



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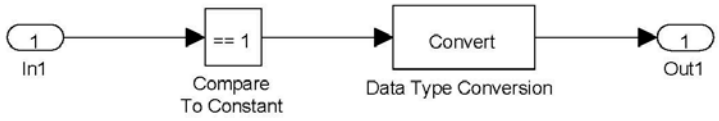
SLR_charger_in_lab/SLR converter/ H-bridge/State1 indicator



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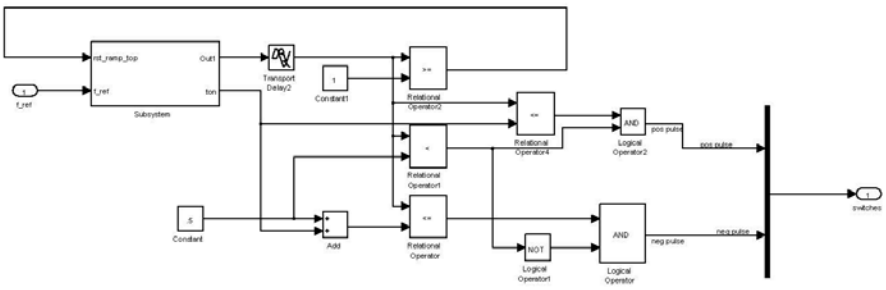
SLR_charger_in_lab/SLR converter/ H-bridge/modulation



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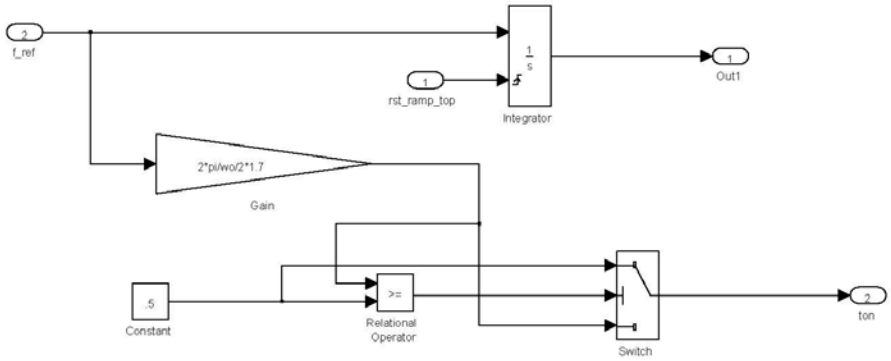
SLR_charger_in_lab/SLR converter/ H-bridge/modulation/Subsystem



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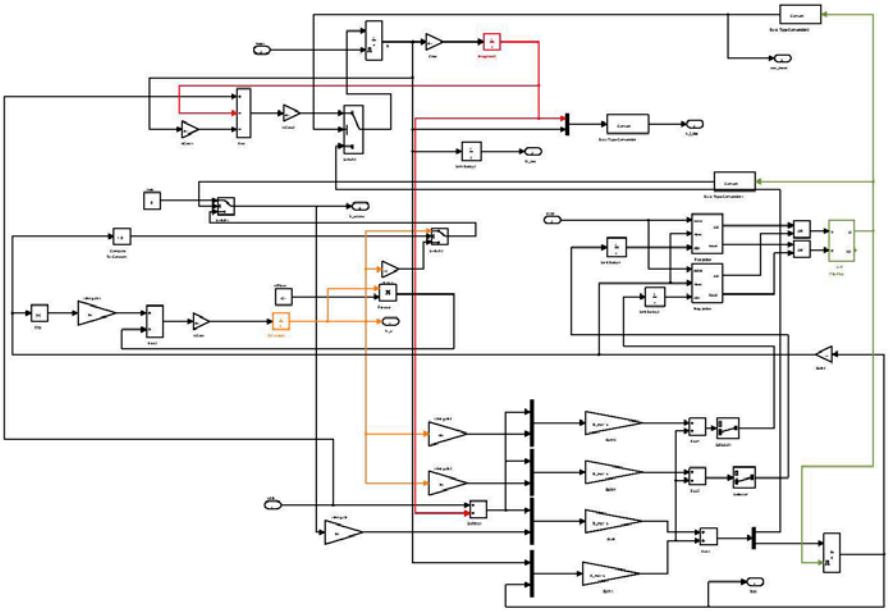
SLR_charger_in_lab/SLR converter/Res tank and load



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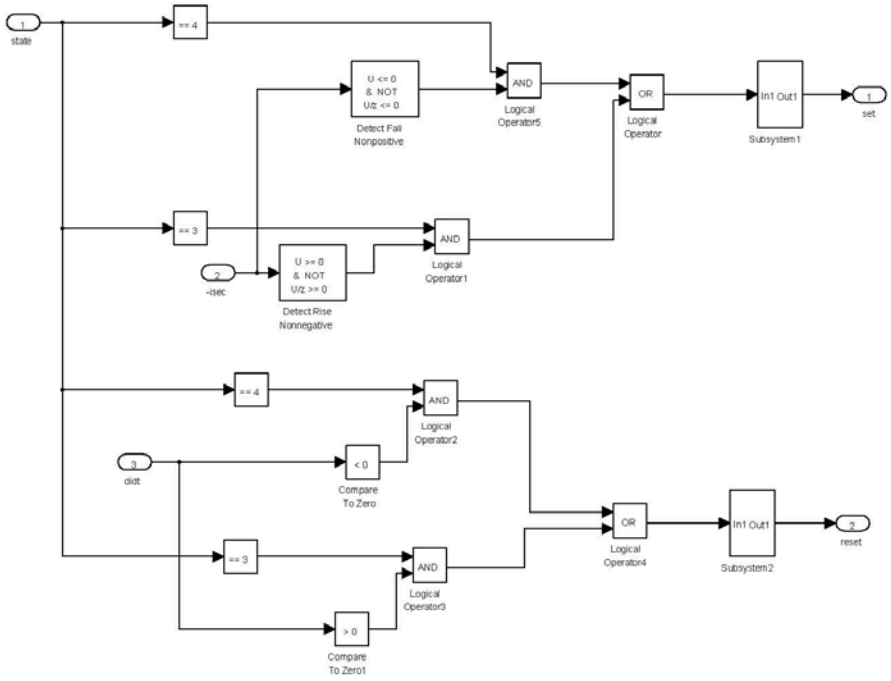
SLR_charger_in_lab/SLR converter/Res tank and load/Neg pulse



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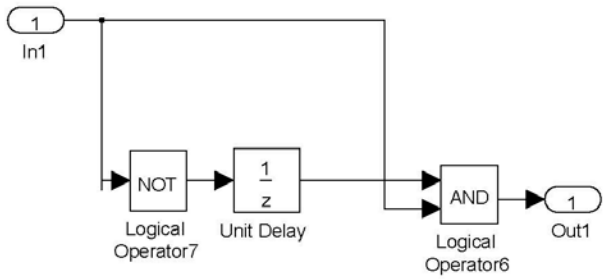
SLR_charger_in_lab/SLR converter/Res tank and load/Neg pulse/Subsystem1



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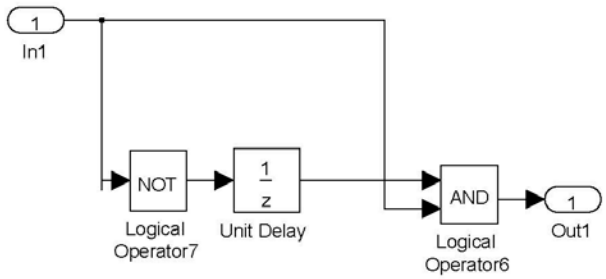
SLR_charger_in_lab/SLR converter/Res tank and load/Neg pulse/Subsystem2



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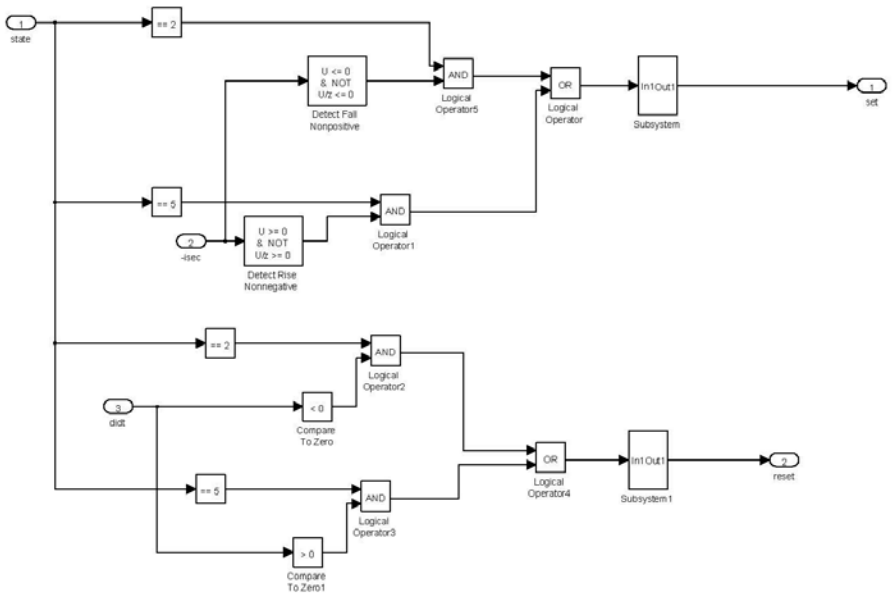
SLR_charger_in_lab/SLR converter/Res tank and load/Pos pulse



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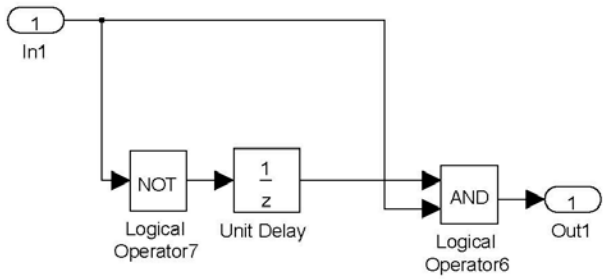
SLR_charger_in_lab/SLR converter/Res tank and load/Pos pulse/Subsystem



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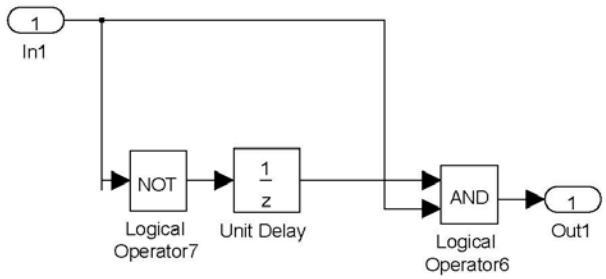
SLR_charger_in_lab/SLR converter/Res tank and load/Pos pulse/Subsystem1



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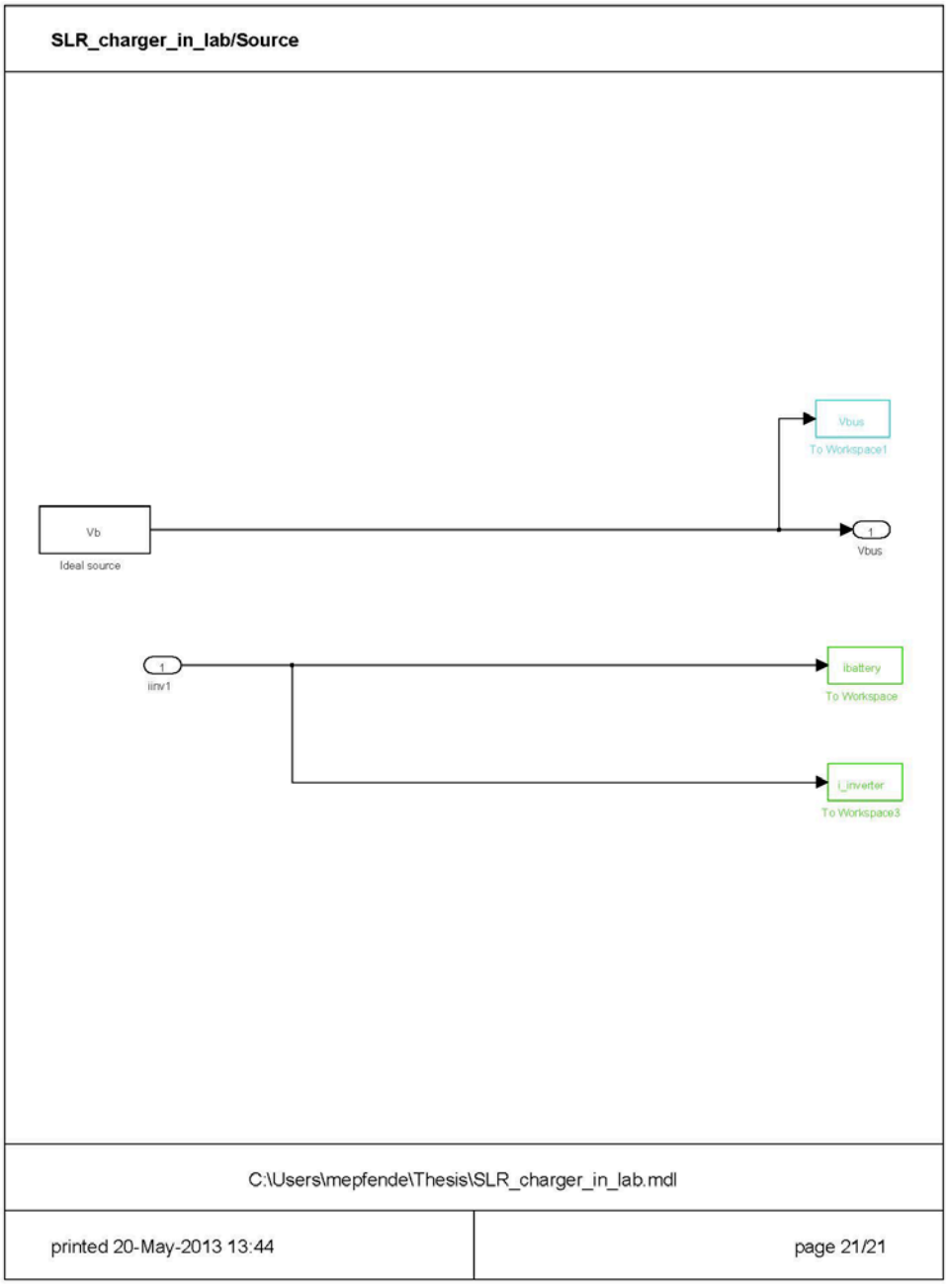
SLR_charger_in_lab/Source
Vbus
To Workspace1
Vb
Ideal source
1
Vbus
1
iinv1
ibattery
To Workspace
i_inverter
To Workspace3
C:\Users\mepfende\Thesis\SLR_charger_in_lab.mdl
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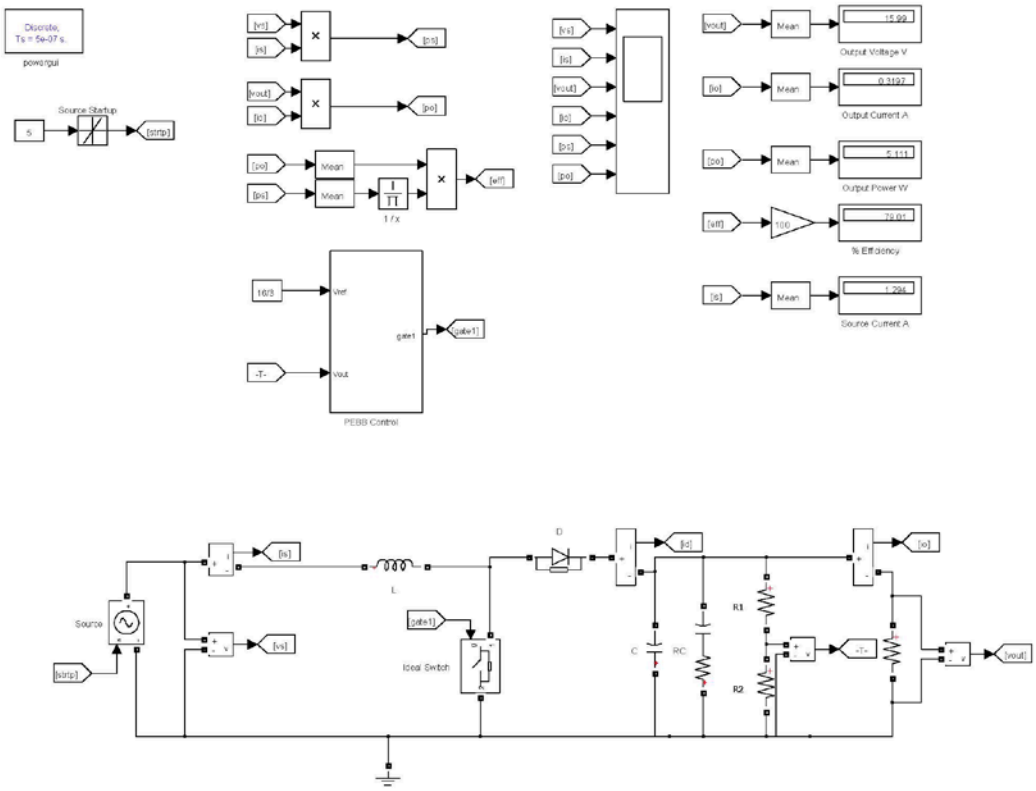
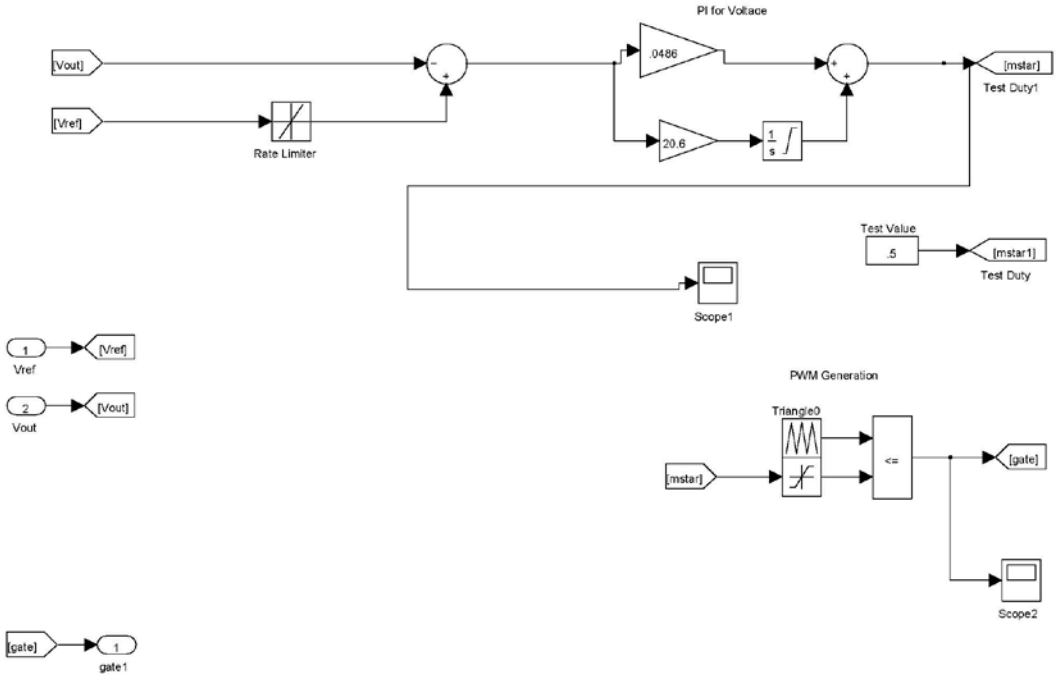

Discrete,
Ts = 5e-07 s.
powergui
Source Startup
.5
[strtp]
[vs]
[is]
[ps]
[vout]
[io]
[po]
Mean
Mean
1 / x
[eff]
[vs]
[is]
[vout]
[ps]
[ps]
[po]
[vout]
Mean
15.99
Output Voltage V
[io]
Mean
0.3197
Output Current A
[po]
Mean
5.111
Output Power W
[eff]
100
79.01
% Efficiency
[is]
Mean
1.294
Source Current A
16/3
Vref
gate1
[gate1]
-T-
Vout
PEBB Control
Source
[strtp]
[is]
[vs]
L
[gate1]
Ideal Switch
D
[ic]
C
RC
R1
R2
[io]
-T-
[vout]


PI for Voltage
[Vout]
[Vref]
Rate Limiter
.0486
20.6
1
s
[mstar]
Test Duty1
Test Value
.5
[mstar1]
Test Duty
Scope1
1
Vref
[Vref]
2
Vout
[Vout]
PWM Generation
Triangle0
[mstar]
<=
[gate]
Scope2
[gate]
1
gate1

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