ARMY RESEARCH LABORATORY

Graphene-based Nanoelectronics (Final Report)

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ARL-TR-6351 **February 2013**

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Army Research Laboratory
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ARL-TR-6351 **February 2013**

Graphene-based Nanoelectronics (Final Report)

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REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-0188

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1. **REPORT DATE** (*DD-MM-YYYY*)	**2. REPORT TYPE**	**3. DATES COVERED (From - To)**
February 2013	DSI	October 2011 to September 2012

4. TITLE AND SUBTITLE

Graphene-based Nanoelectronics (Final Report)

5a. CONTRACT NUMBER

5b. GRANT NUMBER

5c. PROGRAM ELEMENT NUMBER

6. AUTHOR(S)

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Contributors: Matthew Ervin, Matthew Chin, Barbara Nichols, Eugene Zakar, Amin Matin, Osama M. Nayfeh, A. Glen Birdwell, Terrance O'Regan, Frank Crowne, Pankaj Shah, Tomas Palacios, Jing Kong, Pablo Jarillo-Herrero, Mildred Dresselhaus, Pulickel M. Ajayan, Leela Mohana Reddy Arava, and Paresh Ray

5d. PROJECT NUMBER

ARL DSI-FY-11

5e. TASK NUMBER

5f. WORK UNIT NUMBER

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)

U.S. Army Research Laboratory
ATTN: RDRL-SER-L
2800 Powder Mill Road
Adelphi, MD 20783-1197

8. PERFORMING ORGANIZATION REPORT NUMBER

ARL-TR-6351

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)

10. SPONSOR/MONITOR'S ACRONYM(S)

11. SPONSOR/MONITOR'S REPORT NUMBER(S)

12. DISTRIBUTION/AVAILABILITY STATEMENT

Approved for public release; distribution unlimited.

13. SUPPLEMENTARY NOTES

14. ABSTRACT

Significant progress has been made in growing and characterizing graphene and fabricating and testing graphene-based devices. Growth parameters have been optimized for producing large area single- and bilayer graphene. These materials have been characterized using Raman spectroscopy methods developed in this program for determining layer number, stacking order, and defects in graphene. Device processing methods have also been developed, including atomic layer deposition of gate dielectrics with fabricated field-effect transistors (FETs) demonstrating 3-GHz threshold frequencies. A large measured device data set has been produced for circuit design and device modeling validation. Models have been developed to assist in the electrical characterization of the graphene/substrate interface that takes into account interface defects. Graphene FETs will find applications in high frequency communication and radar systems. The U.S. Army Research Laboratory (ARL) has demonstrated inkjet printed flexible graphene supercapacitors with the Stevens Institute of Technology. ARL has also used unique high-speed supercapacitors developed by an ARL Small Business Innovation Research (SBIR) performer, JME Inc., to demonstrate energy storage for a munitions energy harvesting system under development by the Armament Research, Development and Engineering Center (ARDEC). ARL developed supercapacitor technology will enable size, weight, shelf life, and reliability improvements for munitions' electronic systems.

15. SUBJECT TERMS

Graphene, CVD, Raman, FET, device modeling, supercapacitor, Director's Strategic Initiative (DSI)

16. SECURITY CLASSIFICATION OF:			**17. LIMITATION OF ABSTRACT**	**18. NUMBER OF PAGES**	**19a. NAME OF RESPONSIBLE PERSON**
a. REPORT	**b. ABSTRACT**	**c. THIS PAGE**			Madan Dubey
Unclassified	Unclassified	Unclassified	UU	72	**19b. TELEPHONE NUMBER** (*Include area code*) (301) 394-1186

Standard Form 298 (Rev. 8/98)
Prescribed by ANSI Std. Z39.18

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Acknowledgments

We gratefully acknowledge the skillful assistance of several summer students who provided their expertise and efforts in the growth of graphene, device fabrication, thin-film and device characterization, device modeling and simulation, and project presentation. We would like to thank Kevin Hauri, Albert Chu, Cheng Tan, Nick Landau, and Vinay Raju for their contributions to this work. The technical review by Dr. Rob Burke was highly appreciated. We are also thankful to Carol Johnson, technical editor, Technical Publishing Branch, Adelphi Laboratory Center (ALC), for her skillful editing of the manuscript.

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1. Introduction

Electronic phenomena in nanoscale structures have generated new challenges and opportunities for enabling new technologies never before realized. Recently, graphene has emerged as a novel material, especially for electronics, that could lead to devices in the quantum domain at room temperature (*1*–*5*). More generally, graphene represents a conceptually new class of materials that are only one atom thick (equivalent to 0.36 nm for graphene) (*6*), and which thus exhibit startlingly different phenomena from their traditional three-dimensional (3-D) analogs and potentially offer unexplored capabilities for novel electronic devices and applications. Graphene is the name given to a flat monolayer of carbon atoms tightly packed into a two-dimensional (2-D) honeycomb lattice, first isolated in 2004, and illustrated schematically in figure 1. It is the basic building block for graphitic materials of all other dimensionalities and can be wrapped up into zero-dimensional (0-D) fullerenes, rolled into one-dimensional (1-D) nanotubes, or stacked into 3-D graphite.

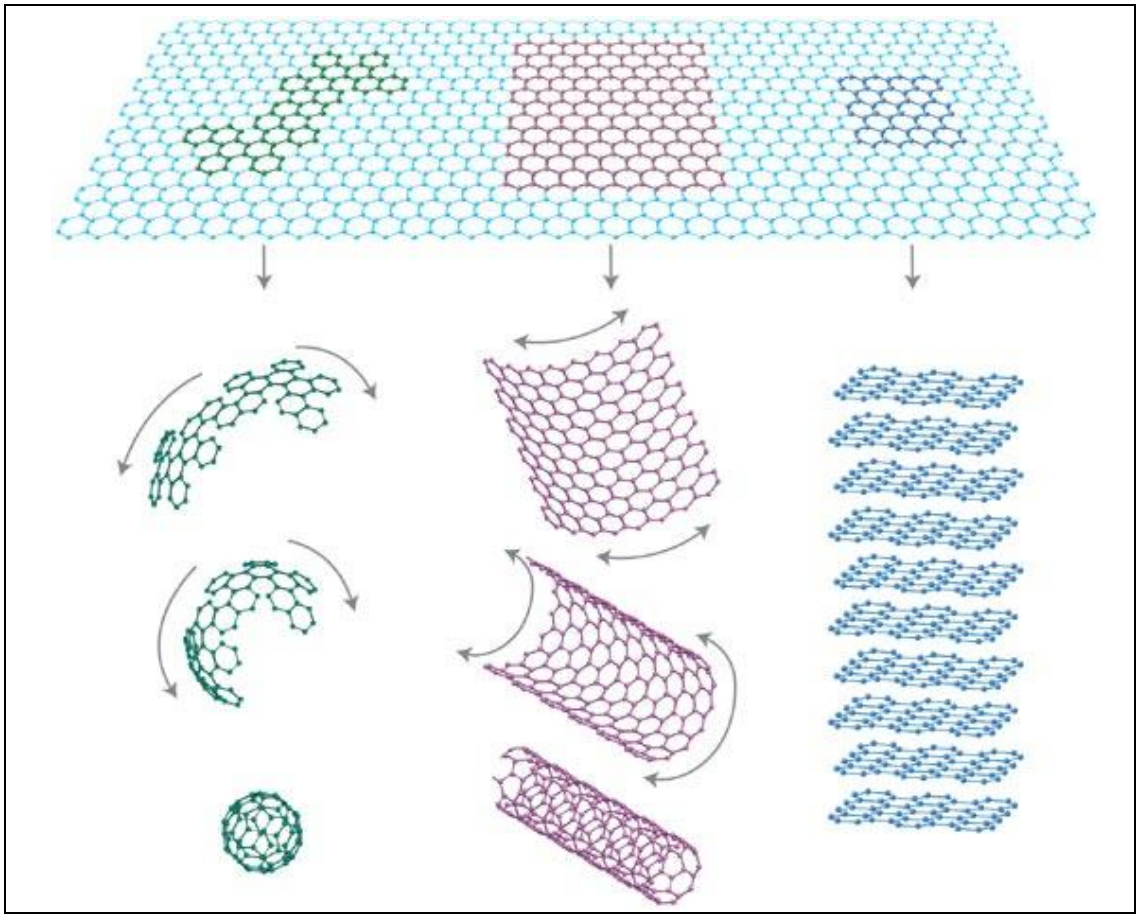

Figure 1. Graphene is a 2-D building material for graphitic materials of all other dimensionalities. It can be wrapped up into 0-D buckyballs, rolled into 1-D nanotubes, or stacked into 3-D graphite (*1*).

Graphene possesses a high electron and hole mobility with values shown as high as 200,000 cm^2/V-s (*7*), a high thermal conductivity of ~5 x 103 W/m-K (*8*), temperature stability to at least 2300 °C (but only ~500 °C in air [*9*]), extremely high tensile strength measured to be 1 TPa (*10*), quintessential flexibility, stretchability to 20% (*11*), a high breakdown current density exceeding 10^8 A/cm^2 (*12*), and superior radiation hardness (*13*). All of these qualities are desired in electronic materials. In addition to these advantageous characteristics, graphene also possesses very unique ambipolar properties (capable of conducting electrons when biased in one direction and holes when biased in the other direction) that open up a whole new class of electronic devices.

Graphene lacks a bandgap in its energy band diagram, and therefore, exhibits metallic conductivity even in the limit of nominally zero carrier concentration. At the same time, most electronic applications rely on the presence of a gap between the valence and conduction bands. Several routes have been reported to induce and control such a gap in graphene. Some examples include using the effect of confined geometries such as quantum dots or nanoribbons, doping the edge states or the bulk of the graphene, applying a transverse electric field to a bilayer of graphene (*14*), and exploiting the proximity effects from an adjacent substrate or insulator layer. Current research shows that graphene's atomic interaction with an epitaxial silicon carbide (SiC) substrate can induce a splitting of up to 0.3 eV between the maximum of the valence and minimum of the conduction bands at the Dirac-point (*15*).

We at the U.S. Army Research Laboratory (ARL) are harnessing the electronic properties of this newly discovered material, finding ways to develop and exploit a new generation of electronic and sensing devices for Army-specific applications. While many in the field are exfoliating micron-sized sections of graphene from chunks of graphite to study its fundamental physics or for measurements of unipolar complementary metal-oxide-semiconductor (CMOS)-like devices to extend Moore's Law, our approach is to synthesize our graphene using a manufacturable process, i.e., by chemical vapor deposition (CVD), and study a new class of graphene devices and circuits that harness the unique ambipolar properties of graphene. Such ambipolar devices and circuits hold the promise of more efficient and smaller analog circuits, increased frequency ranges, lower power consumption, and higher data transmission speeds, all in a transparent/invisible/durable/flexible form factor. This latter attribute could lead to wearable electronics woven into a Soldier's uniform (so-called electronic textiles or "e-textiles") for wireless communications or health and medical condition sensing. Medical sensors using graphene-based e-textiles, in turn, could be used to wirelessly transmit information to a central command node, trigger automated drug delivery (e.g., insulin), or be incorporated within "smart bandages," which could accelerate healing of wounds. Many of the military advantages listed above could be also transitioned to civilian and commercial usages, which could make a large impact on the day-to-day world in which we live.

Further, as more sophisticated electronics are deployed to the battlefield, energy requirements become a greater burden to the Soldier. Exploiting the unique properties of graphene, we are pursuing two avenues for solutions. First, as we have said, we are developing a new class of graphene-based nanoelectronic technology that would potentially replace larger, heavier, and power-hungry components in communications systems and portable electronics. Second, we are developing a new type of energy storage device called a supercapacitor, which uses graphene or carbon nanotubes (CNTs) and an electrolyte to produce ~100 times the specific power of batteries and fuel cells. Supercapacitors are capable of millions of charge/discharge cycles, rapid charge and discharge times, and high efficiencies. This research, in collaboration with the Communications-Electronics Research Development and Engineering Center (CERDEC) and the Armament Research Development and Engineering Center (ARDEC), aims to create a printable capacitor monolithically integrated with printable electronics to produce power for integrated electronic and sensor circuits.

The research we have performed under the ARL Director's Strategic Initiative (DSI) program has focused on developing in-house capabilities and infrastructures for producing electronic-grade graphene, characterizing its properties by a number of metrology tools, fabricating graphene test structures and graphene field-effect transistors (GFETs) incorporating a large variety of dielectric materials, testing these electronic structures and devices at DC to radio frequency (RF) frequencies, exploring the use of graphene in supercapacitor devices for energy storage, and initiating efforts to model and simulate graphene device performance.

The third and final year DSI efforts have been focused to achieve a reliable and consistence large area graphene routinely for devices; trusted and repeatable transfer or direct G-growth on device quality substrates; basic and fundamentals of graphene layers physics; chemistry and electronics; defects and doping characterization using Raman spectroscopy; routine and easy Hall mobility estimation; high resolution transmission electron microscopy; field-affect transistor (FET) electronic devices fabrication and measurements; and pulse power measurements for RF applications and device modeling, simulation, and validation.

This report encompasses all three years of the DSI research and development (R&D) efforts towards graphene nanoelectronics. Accordingly, this report aims to summarize the work done over the past three years and highlight important findings. It is divided into the following sections:

Section 1: Introduction

Section 2: Graphene Growth

Section 3: Characterization by Raman Spectroscopy

Section 4: Graphene Electronic Devices from CVD-grown Graphene

Section 5: Graphene Supercapacitors

Section 6: Conclusions

Section 7: Transitions

Section 8: References

1.1 Collaboration

We have established Cooperative Agreements with two universities that were executing strong programs on graphene and that had established capabilities and directions that were well aligned with our own goals. The first is the Massachusetts Institute of Technology (MIT)—Profs. Palacios (*16*, *17*), Kong (*18*, *19*), Jarillo-Herrero (*20*, *21*), and Dresselhaus (*22*), with significant progress in graphene-based ambipolar devices and circuits, as well as graphene growth by CVD and the production of suitable starting structures for device fabrication. The second is Rice University—Prof. Ajayan (*23*), who has made exciting progress on some key building blocks for high performance graphene electronics, such as the co-synthesis of graphene with boron nitride (another purely 2-D monolayer and an excellent dielectric material for advanced GFET devices), and the discovery of how to make graphene repetitively reconfigurable between semiconducting and insulating states. Collaborative arrangements have been established with both of these institutions in order to enhance our efforts, and these are reflected in this report. We are also working successfully with University of Texas, Austin under an Army Research Office (ARO)-funded 2-D materials program and Stanford University using the ARL-funded Army High Performance Computing Research Center program. Collaboration with the Stevens Institute of Technology has also been established using an ARL-Defense Advanced Research Projects Agency (DARPA) ongoing agreement.

2. Graphene Growth

2.1 Chemical Vapor Deposition Furnaces

The capability to produce graphene thin films in-house at ARL is important to the success of the Graphene DSI. Epitaxial graphene growth on SiC has been the primary graphene growth technique for over eight years; however, over the last four years, CVD of graphene on metal substrates has gained prominence as a viable method for graphene deposition. CVD offers lower processing temperatures and cheaper substrate materials, and is considerably less difficult to set up in a laboratory setting than a high temperature furnace for graphene growth on SiC.

Two CVD furnaces were established for in-house graphene growth: an atmospheric pressure chemical vapor deposition (APCVD) furnace and a low pressure chemical vapor deposition

(LPCVD) furnace. APCVD graphene growth was performed in an existing CNT furnace since growth conditions for CNTs and graphene are very similar. The APCVD furnace was primarily used to growth graphene on nickel (Ni) thin films. A new LPCVD furnace system was constructed at the Adelphi Laboratory Center during the first year of the DSI. It has been shown that single-layer graphene (SLG), while difficult to produce using APCVD, can be produced under low pressure on copper (Cu) foils (*24*, *25*). More details on the LPCVD system can be found in ARL-TR-5451 (*26*). The LPCVD furnace has primarily been used to pursue single- and bilayer graphene growth on Cu foils.

2.2 Growth on Copper

2.2.1 Introduction

The deposition of high quality, large area graphene and the subsequent transfer onto device-compatible substrates has played an important role in the Graphene DSI. Growth efforts have been geared toward producing graphene that is suitable for electronic device development and understanding the fundamental behavior of these devices. The first year of the DSI was considered to be a "building" phase for in-house growth efforts. In addition to the construction of the LPCVD growth system, the transfer process for graphene grown on Cu foil was transitioned from our university partner MIT and basic characterization of transferred graphene was performed using Raman spectroscopy (see reference 27 for more details).

For the second year, primary emphasis was given to improving the graphene transfer process and understanding transfer-related effects on the physical properties of graphene. The transfer process is extremely important because graphene grown on metal substrates are unsuitable for device fabrication. Key process improvements to the two steps, namely, the backside graphene removal and placement onto the desired substrate steps, increased the yield of successfully transferred and usable graphene to 95%. The removal method of the protective poly(methyl methacrylate) (PMMA) handle layer was also shown to impact the graphene physical properties. Thermal annealing was found to be more effective in removing the PMMA layer; however, Raman spectroscopy measurements showed increased blue-shifting of the characteristic graphene peaks as the annealing temperature increased. This shift is thought to arise due to increased doping of the graphene most likely arising from the silicon oxide substrates (see reference 24 for an in-depth discussion of the results).

The major focus for the final year of the DSI was to understand and improve the graphene growth by LPCVD. This was accomplished by two main methods: (1) characterizing the graphene via Raman mapping and (2) performing a series of experiments of key growth parameters, such as hydrogen partial pressure.

2.2.2 Raman Map Characterization of CVD Graphene

The acquisition of a WITec alpha300RA confocal Raman microscope (CRM) has allowed for the development of Raman feature maps over large areas of graphene, which has opened up a better understanding of the graphene structure. Previously, due to instrument limitations, an individual Raman spectrum was taken at various points across a large area (e.g., 40 x 60 μm) at intervals between 2 to 5 μm. While this approach allowed for basic characterization of the graphene, the number of spectra taken and the spacing did not provide details about possible variations of the graphene structure. The WITec alpha300RA CRM allows the acquisition of individual Raman spectra over large areas (up to 90 x 90 μm) at submicron spacing intervals. This capability has produced detailed views of the graphene films that reveal information about the number of graphene layers, structural stacking, and other features, such as wrinkles and graphene folds.

The results from a typical Raman scan map taken from the WITec CRM tool can be seen in figure 2. Figure 2a shows a 100 μm x 100 μm optical image (taken under a green filter) of a transferred graphene film (LPC069B1TC). For this film, the graphene was grown on Cu foil by LPCVD and transferred to a 3000-Å silicon dioxide (SiO_2)/silicon (Si) substrate using a process defined elsewhere (*27*). Prior to Raman spectroscopy the protective PMMA layer was removed by soaking the sample in chloroform. The optical image shows a large monochromatic field with multiple darker patches. Raman microscopy scans were taken over an 80 μm x 80 μm area with individual spectra taken at approximately 0.3-μm intervals. An individual Raman spectrum taken at one point can be found in figure 2b. The spectrum exhibited the characteristic Raman spectra for graphene, featuring the G' peak at ~2700 cm^{-1}, G peak at ~1580 cm^{-1}, and D peak at ~1350 cm^{-1}. Also present in the spectrum is a peak at 520 cm^{-1}, which arises from the Si substrate.

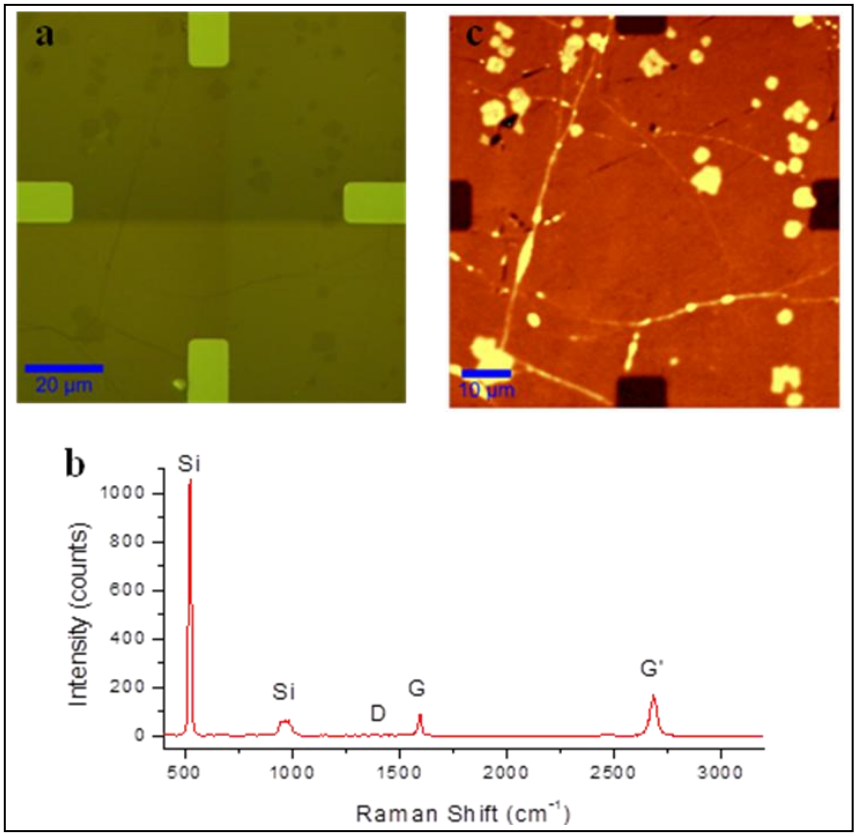

Figure 2. Optical and Raman map images of graphene: (a) 100 μm x 100 μm optical image of a graphene film grown by LPCVD and transferred onto 3000-Å SiO_2/Si substrates. The four rectangles represent 120-nm trenches etched into the silicon oxide layer and are used for identification purposes. (b) Raman spectrum taken from the graphene. (c) Map plotting the intensity ratio value between the G and Si peak (I_G/I_{Si}) in the Raman spectra.

Using the maps developed from the Raman spectra, one can correlate features in the optical image with those observed in the Raman maps. For example, the location of bright areas seen in the I_G/I_{Si} (intensity ratio between the G and Si peaks) map in figure 2c correspond to the dark patches in the optical image, revealing that the bright locations are composed of one or more additional graphene layers. It has also been shown that the intensity ratio between the characteristic G and G' peaks ($I_{G'}/I_G$) indicates the number of layers present in graphene (*28*, *29*). A map of the $I_{G'}/I_G$ ratio for the scanned graphene area can be found in figure 3. The majority of the map reveals a median intensity ratio of 1.75, near the $I_{G'}/I_G$ value of 2, which is indicative of SLG. However, the map also reveals areas with $I_{G'}/I_G$ values both significantly higher (~2.6) and lower than the median value (~0.7). The location of these areas correlate to the high I_G/I_{Si} ratio areas observed in figure 2c, showing the existence of additional graphene layers.

An examination of the G' peak full width half maximum (FWHM) values at these locations is also helpful. Based on the $I_{G'}/I_G$ intensity ratio and G' FWHM maps, three distinct areas have been identified and the representative Raman spectra of each area can be found in figure 3. The first distinct area represents the majority of the film. This area has a median G' FWHM value of 36 cm^{-1} and $I_{G'}/I_G$ intensity ratio of 1.75, which is indicative of SLG. The second area—the dark areas in the $I_{G'}/I_G$ intensity map—reveals $I_{G'}/I_G$ values less than 1 and a G' FWHM of 57 cm^{-1}. This signature is indicative of bilayer graphene (BLG) with Bernel (AB) stacking (*28*). Bernel stacking arises when the edge of the top graphene layer is aligned in the same direction as the bottom layer. This stacking is important in graphitic materials and gives rise to the unique properties of multilayer graphene. The third area reveals large $I_{G'}/I_G$ intensity ratio values (greater than 2.5) and narrow FWHM values of the G' peak (FWHM values ranging from 28–32 cm^{-1}). This area is indicative of turbostratic BLG (*28*). Turbostratic BLG arises when a top graphene layer is twisted or rotated at an angle of ~30° from the bottom layer. The identification of these distinct areas of graphene is extremely important to determine the quality of the graphene and the influence various LPCVD growth parameters have on its structural properties.

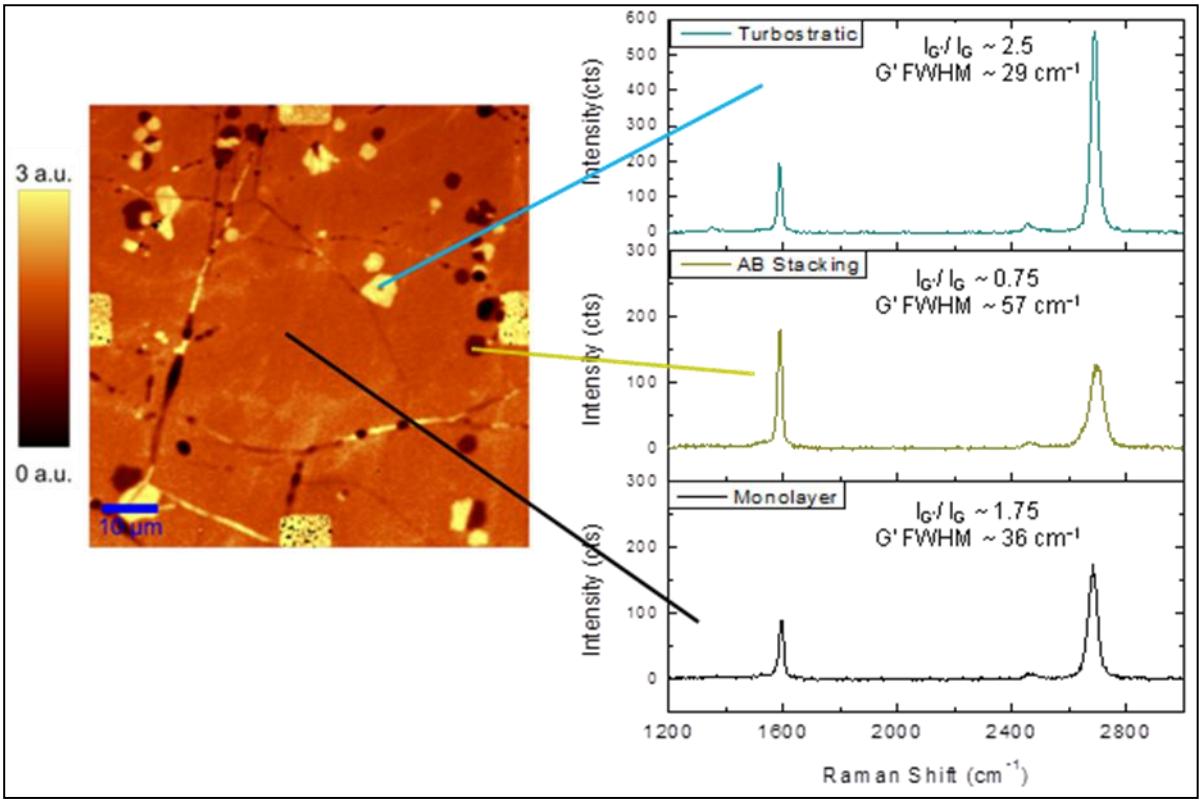

Figure 3. $I_{G'}/I_G$ intensity ratio map of the same area shown in figure 2. Lines are drawn from three distinct features in the map to the corresponding representative Raman spectra.

2.2.3 Experimentation and Results

Hydrogen (H_2) is known to play an important dual role in the growth of graphene by CVD methods. First, it acts as an activator for the surface bound carbon to form graphene; however, it can also act as an etching agent, which helps controls the size and shape of the graphene domains (*28*). The first set of experiments sought to explore the influence of the hydrogen partial pressure on the resulting graphene structure. For the experiments, the methane (CH_4) flow was fixed at 5 sccm; whereas, the hydrogen gas flow was varied from 0 to 500 sccm. Other growth parameters were kept constant, including temperature, pressure, and growth time. A summary of the growth conditions is shown in table 1. After LPCVD growth, the graphene samples were transferred onto 3000 Å SiO_2/Si substrates as discussed previously.

Table 1. LPCVD growth conditions for the experiments varying the H_2:CH_4 flow ratio.

Sample	H_2 Flow (sccm)	CH_4 Flow (sccm)	H_2:CH_4 Ratio	Time (min)	Pressure (Torr)	Temperature (°C)
LPC041	50	5	10	20	1.5	1000
LPC042	300	5	60	20	1.5	1000
LPC043	200	5	40	20	1.5	1000
LPC044	500	5	100	20	1.5	1000
LPC046	0	5	0	20	1.5	1000

Figure 4 shows the $I_{G'}/I_G$ intensity maps (50 x 50 μm area) for five graphene films grown for this experiment. The hydrogen-to-methane gas (H_2:CH_4) flow ratio for the graphene varies from 0 (no hydrogen during growth) to 100. The maps shown were taken with the PMMA still present on the surface to avoid any changes to the graphene structure due to thermal annealing. It has been reported that thermal annealing of graphene at temperatures ~350 °C and above (necessary to remove the PMMA) changes the Raman structure of graphene (*29*, *30*). While the existence of the PMMA may influence the intensity of the characteristic D, G, and G' peaks, general trends observed in the data should not be affected. The $I_{G'}/I_G$ maps for the five films show the three characteristics areas of SLG and BLG (as discussed in the previous section). The median $I_{G'}/I_G$ values for the films ranged from 1–1.5 and the median G' FWHM values ranged from 35 and 38 cm^{-1}. It has been reported that exfoliated SLG can exhibit $I_{G'}/I_G$ values close to 1 and G' FWHM values up to 40 cm^{-1} (*31*). Based on these results, it is assumed that the majority of the films are composed of SLG with areas of both turbostratic and AB-stacked BLG. For these growths, the percentage of SLG ranged from 85% to 92%, with most BLG exhibiting turbostratic properties. One trend that can be seen in the $I_{G'}/I_G$ ratio as a function of hydrogen flow is the size of the BLG areas. As the H_2:CH_4 ratio increased, the average size of the BLG area increased from less than 1 μm for H_2:CH_4 = 0 to 3 μm for H_2:CH_4 = 100. This suggests that the formation

of large BLG growth areas is influenced by the amount of hydrogen gas present during the growth and provides a pathway for producing large area coverage of BLG.

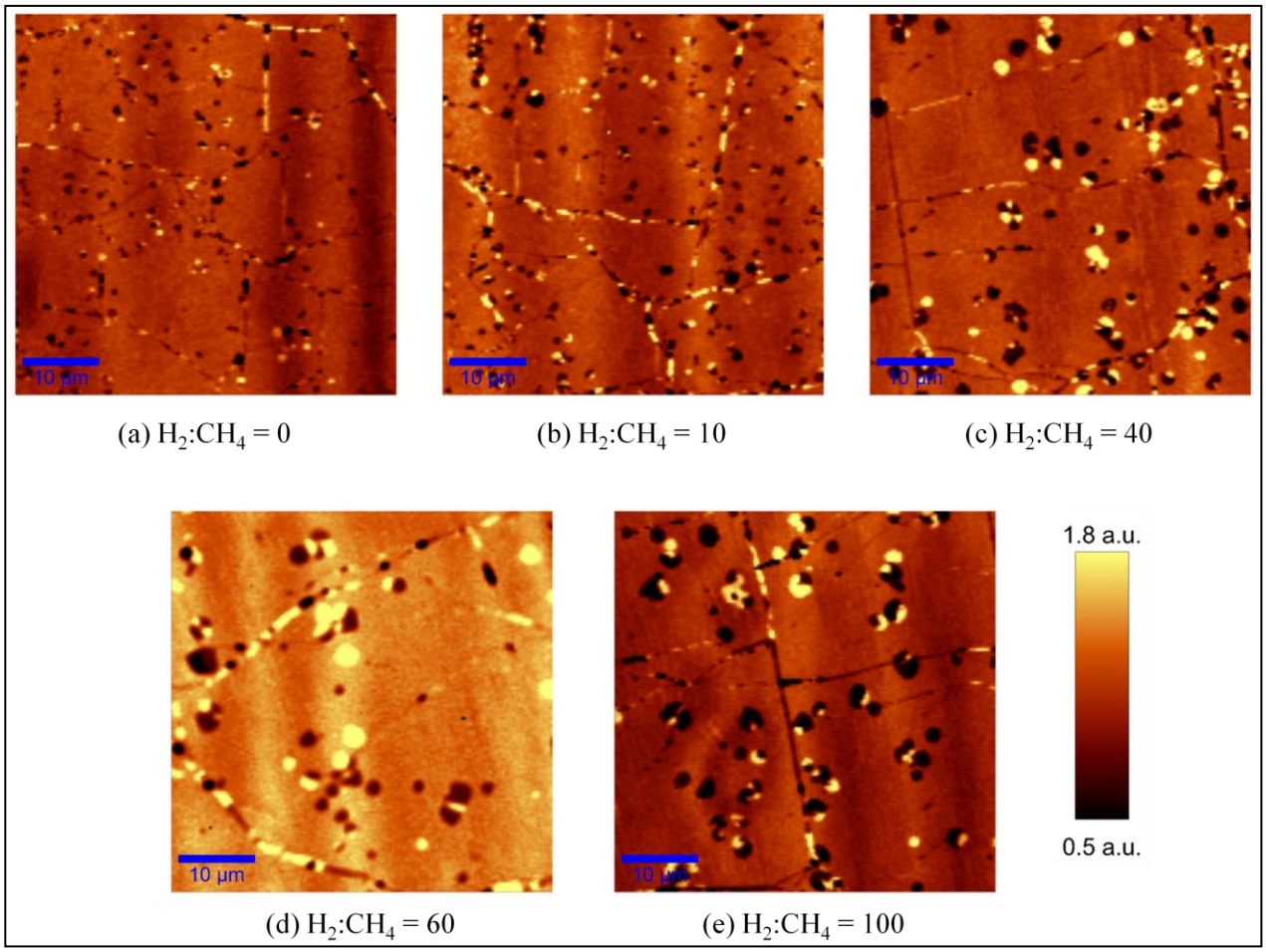

Figure 4. The 50 x 50 µm area $I_{G'}/I_G$ intensity ratio maps for five graphene films grown under varying H_2:CH_4 gas flow ratios: (a) H_2:CH_4 = 0, (b) H_2:CH_4 = 10, (c) H_2:CH_4 = 40, (d) H_2:CH_4 = 60, and (e) H_2:CH_4 = 100. The color scale shown in the figure was used for all five maps.

Based on the results from the hydrogen partial pressure experiments, the formation of the graphene layers, especially BLG, is of interest. One-minute growths for two different H_2:CH_4 ratios (10 and 100) were performed using the growth parameters described earlier. The $I_{G'}/I_G$ intensity maps for these two growths are shown in figure 5. While the two growths exhibit features similar to their 20-min growth counterparts, most striking is that there is full graphene coverage of the Cu foil after 1 min. This is an extremely fast growth rate. Reports on graphene growth by LPCVD show higher CH_4 concentrations and fast growth typically yield small domains/grain sizes (*32*, *33*). Small-grained graphene material (less than 5 µm) demonstrates significantly lower carrier mobilities than large-grain CVD graphene (*34*). In fact, in-house CVD graphene-based FETs exhibited mobility values of 800 cm^2/V s and less, which falls at the

extreme low end of reported mobility values for CVD graphene (500–20,000 $cm^2/V \cdot s$) (*34*). In order to improve the CVD graphene quality, promote the formation of large grains, and make graphene growth more controllable, lower CH_4 flows must be used. In order to achieve these lower CH_4 flows, a new mass flow controller (MFC) was obtained with a flow range of 0 to 5 sccm.

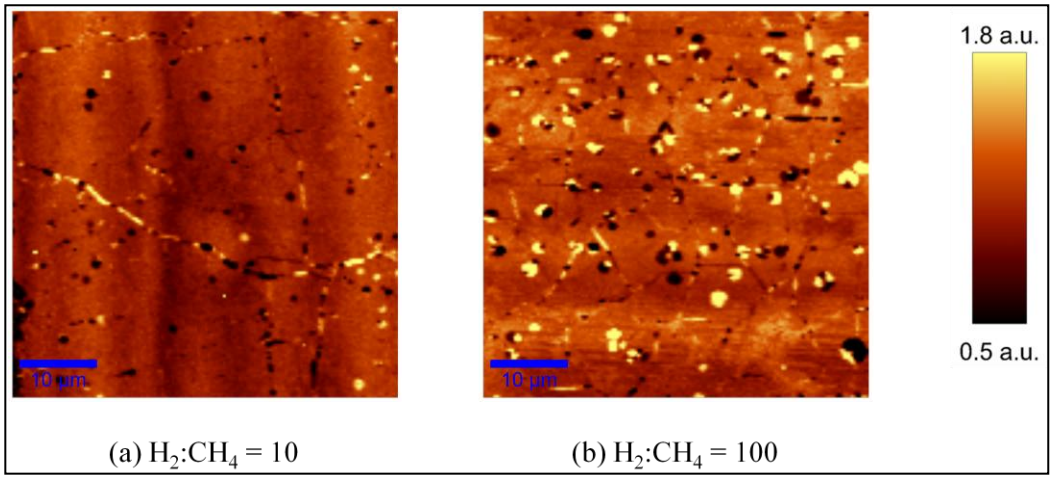

Figure 5. The 50 x 50 µm area I_G/I_G intensity ratio maps for two graphene films grown under varying H_2:CH_4 gas flow ratios for 1 min: (a) H_2:CH_4 = 10 and (b) H_2:CH_4 = 100. The color scale shown in the figure was used for both maps.

Upon installation of the low flow CH_4 MFC, growth experiments were performed decreasing the CH_4 flow from 5 to 0.5 sccm as the hydrogen flow rate was kept constant at 100 sccm. Of particular interest was the graphene film grown at 0.5 sccm of CH_4 for 20 min (LPC069ATC). The front and back sides of the graphene grown on Cu foils was examined by scanning electron microscopy (SEM) and Raman spectroscopy after transfer. SEM images of the top and bottom sides of the graphene can be found in figure 6. Images from the top side graphene reveal full coverage of graphene on the foil with darker areas indicating the presence of additional layers. In the image, the bilayer areas are typically hexagon-shaped (figure 6b). The bottom side graphene revealed the presence of discrete graphene grains that have not coalesced into the continuous film (figure 6c). A close-up of a discrete patch reveals the presence of a six-lobed star-shaped grain with a star-point-to-star-point distance of approximately 65 µm.

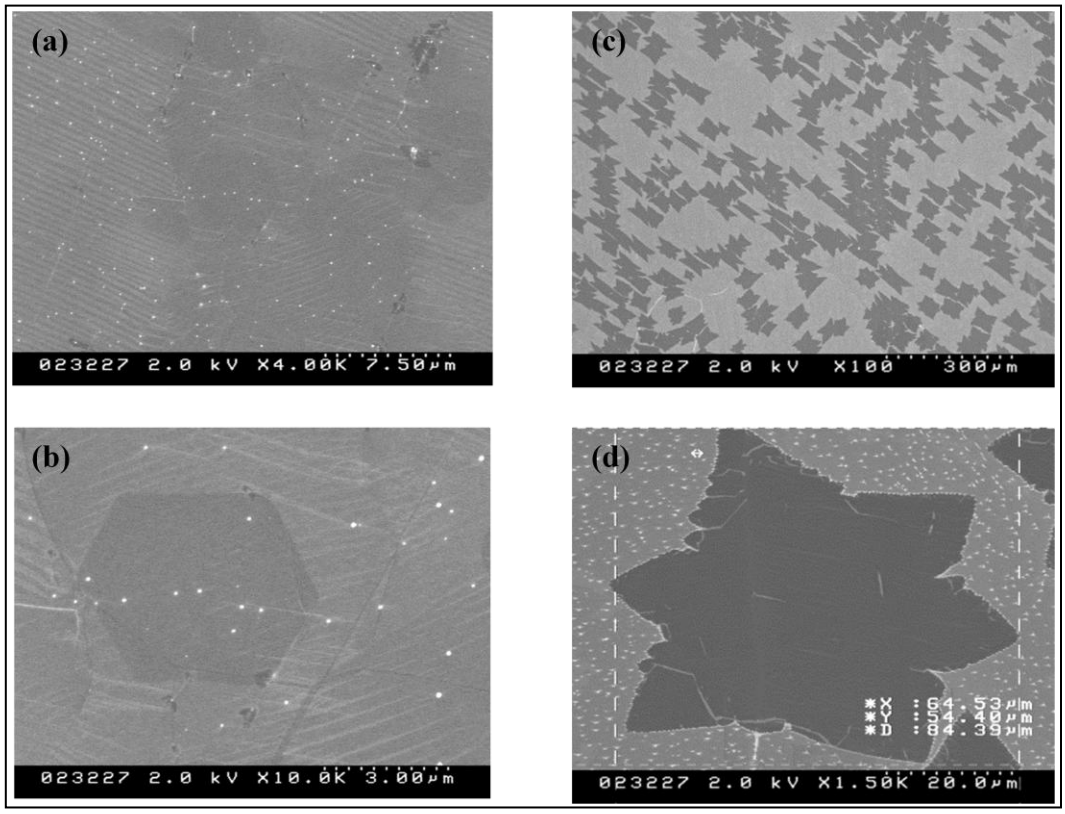

Figure 6. SEM images of the top ([a] and [b]) and bottom sides ([c] and [d]) of graphene grown on Cu foil with a CH_4 flow of 0.5 sccm and hydrogen gas flow of 100 sccm for 20 min.

The optical image and Raman spectroscopy map of the bottom side graphene shown in figure 6 (after transfer and PMMA removal) are shown in figure 7 (Raman scan maps of the front side graphene of a corresponding sample can be seen in figures 2 and 3). The images reveal lobed graphene patches at the beginning stages of coalescence. Even though the graphene has not formed into a continuous film, additional layers at the grain centers have already formed. Analysis indicates that the lobes mainly consist of SLG with BLG located at the center. In the case of the top right grain, the Raman spectra suggests that the center is composed of both bilayer and trilayer graphene. This suggests that the center of the grain acts as a nucleation site for SLG and the formation of additional layers.

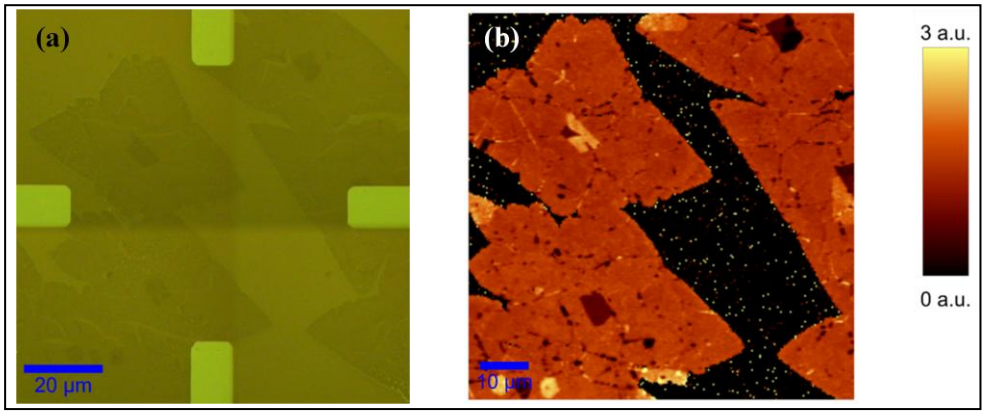

Figure 7. Optical image and the corresponding I_G/I_G intensity ratio from the bottom side graphene for the sample shown in figure 6.

Additionally, bright field transmission electron microscopy (TEM) was performed on the top side graphene shown in figure 2 (the graphene was grown at the same time as the sample in figures 6 and 7). Figure 8 shows a cross-sectional TEM image taken at 80 kV with the spherical aberration corrected (also referred to as a "Cs corrected") FEI Titan 80–300 High resolution TEM (HRTEM) at the CAMCOR facility of the University of Oregon. The "straight" dark lines in the image represent electron dense areas and are indicative of graphene. From the image, the number of layers varies between 1 to 3 layers depending upon the location of the film, with most areas either 1 or 2 layers. This roughly agrees with the Raman spectroscopy data, which indicate the presence of both SLG and BLG. The layer thickness was measured on average to be 0.377 nm, which is consistent with the 0.335-nm lattice spacing of graphite.

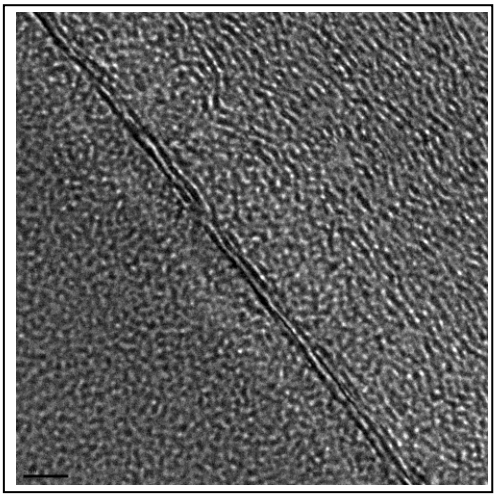

Figure 8. HRTEM image of 1 to 2 graphene layers.

2.2.4 Summary

The Raman mapping of CVD graphene has opened up a great understanding into the growth mechanism that has lead to the deposition of single- and bilayer graphene films. It has been shown that decreasing the graphene growth rate has been instrumental in producing large-grain graphene. The electrical measurements from these graphene growths are discussed in section 4 of this report.

2.3 Growth on Nickel

2.3.1 Introduction

Graphene growth can be synthesized on metal surfaces by APCVD. The challenge has been controlling the number graphene layers on metals and covering relatively large areas for application to electronic GFETS that can be manufactured in the semiconductor industry. Ni and Cu are readily available metals in the semiconductor industry, are affordable, and have a particularly low carbon solubility (~1%), which is needed in the process for growing graphene. The advantage of the APCVD method is that it does not require equipment to pump the CVD reaction chamber to low pressures. The first-year effort was devoted to modifying an existing atmospheric furnace for growing graphene and designing experiments for depositing thin-film Ni on an insulated semiconductor Si wafers using an in-house sputtering system. In the second year, we demonstrated few-layer and tri-layer growth graphene, and started understanding and controlling surface defects. In this third and final year of the program, we developed a process to further reduce the growth to single- and bilayer graphene, and correlated its favorable synthesis to the starting Ni properties.

We have found a key component of Ni's properties that can have a tremendous influence on the growth of graphene layers. Syntheses of graphene by APCVD on the [111] face of single crystal Ni favors the formation of highly uniform monolayer/bilayer graphene on the Ni surface, and simultaneously hinders the formation of multilayer graphene domains. These results are based on a diffusion-segregation model for carbon precipitation on a Ni surface, where the uniform and grain-boundary-free surface of the Ni [111] single crystal provides a smooth surface for uniform graphene formation. In contrast, the rough surface of polycrystalline Ni with its abundant grain boundaries facilitates the formation of multilayer graphene.

Historically thick foils and thin films have been used as catalysts for growing few-layer graphene by APCVD. Diluted methane 2–16 vol.% (*35–38*, *42*) and less than 2 vol.% (*39–41*) were successfully employed for growing few-layer graphene on foils and evaporated thin films. The sputtered method employed in the preparation of the Ni catalyst is more complex than evaporation method or use of commercial quality thick foils. The sputtered method can directly change the properties of Ni due to additional deposition parameters such as the temperature and pressure options not available in the previously mentioned methods. The influence of sputter

temperature and pressure variations on the preparation of Ni, including growth of graphene on top the Ni catalyst by APCVD using diluted CH_4, is reported.

2.3.2 Experimental Procedure

The Ni film was deposited on SiO_2/Si substrates by sputtering to a thickness of 300 nm using a CVC-601 system equipped with a quartz heating lamp. The sputtering was performed at a temperature of 25, 100, and 250 °C each with a pressure of 2 and 20 mTorr. The substrate was then loaded into the APCVD furnace and the temperature was ramped up to 900 or 975 °C. The annealing process was carried out at atmospheric pressure with an H_2 flow rate between 300 to 700 sccm with the balance being argon (Ar) to maintain a total flow of 1000 sccm. Graphene growth was accomplished by flowing 3–5 sccm of CH_4 for 10 min. After the graphene growth step, we ramped down the temperature of the furnace at a rate of 5 °C/min while maintaining the same flow rates of CH_4, H_2, and Ar. The Ni surface morphology was analyzed using an atomic force microscope (AFM) model Veeco NanoScope V in the contact mode. Powder x-ray diffraction (XRD) pattern analysis was conducted using Rigaku Ultima III with the Bragg-Brentano focusing method using CuKα1 and $\lambda = 1.5406$ Å. Graphene films were characterized by Raman spectroscopy using a WITec Alpha 300RA system under the high intensity, low noise settings of the charge-coupled device (CCD). Spectra were measured in the backscattering configuration using the 532 nm line of a frequency-doubled neodymium (Nd):yttrium aluminum garnet (YAG) laser as the excitation source (~1.5 mW at sample) with a 100× objective and 600 grooves/mm grating with a 0.5-s integration time.

2.3.3 Ni Film Preparation

The Ni films prepared by sputtering at 25 °C had grain sizes of 35 nm with an average roughness value R_a of 5.2 nm. Sputtered thin films deposited in a condition of supersaturation typically result in small grain sizes due to a high rate of nucleation (*46*). Sputtering at 100 °C and 2 mTorr resulted in grains approximately 90 nm in size with a R_a of 9.3 nm. An increase in the sputtering temperature to 250 °C produced noticeably larger grains of roughly 600 nm in size with a proportionally higher R_a of 27 nm.

2.3.4 Ni Annealing

Annealing is necessary for grain growth and the stability of the film. Figure 9a–c shows the grain growth in annealed Ni for 20 min at 975 °C and its relationship to the initial sputtering conditions.

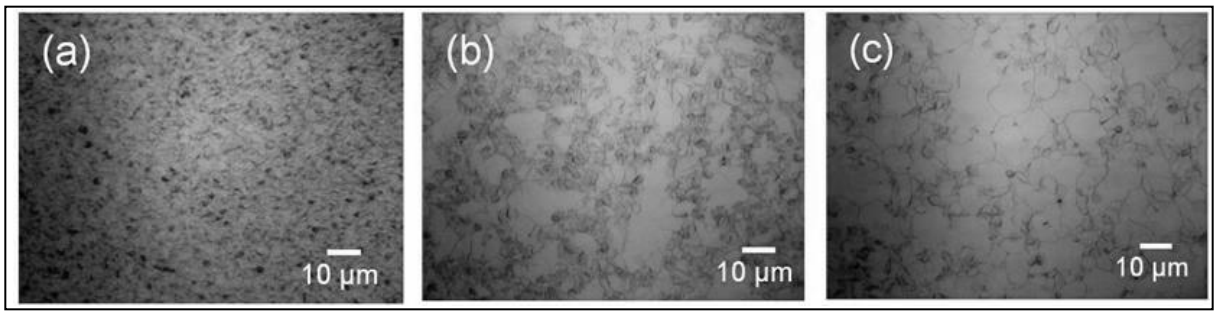

Figure 9. Grain boundary in Ni after annealing relative to the initial sputtering conditions (a) 25 °C at 2 mTorr, (b) 100 °C at 2 mTorr, and (c) 250 °C at 2 mTorr.

The average grain size increased approximately 10 times its original deposited size. Increasing the sputter deposition temperature (*44*) is an approach for promoting enhancement of large grains. The final grain boundary density after annealing was calculated as 0.175, 0.08, and 0.0352 counts per square micron for sputtering temperatures of 25, 100, and 250 °C, respectively. The grain boundary density was calculated by taking the product of the grain boundary count across the length and width of the images at 100× magnification, and dividing by the image area. The number of grain boundaries diminished when the sputtering temperature was higher and the grain size larger.

A factor that is expected to influence graphene formation on top of Ni is the surface termination and orientation of the metal substrate atoms. For Ni with a face-centered-cubic (f.c.c.) structure, the preferred orientation should be [111], since both this surface and the honeycomb structure of graphene have a hexagonal symmetry. Ni films generally exhibit XRD planes [111], [200], [220] with 2θ peaks corresponding to 44.4°, 51.8°, and 76.4°, respectively. After annealing our sputter-prepared Ni film for 20 min at 975 °C, the intensity peaks [111] and [200] were detected but not the [220], as shown in figure 10a. The intensity peak for the [111] increased (figure 10b) when the Ni was prepared by sputtering at 100 °C. The [111] peak was even greater at the sputter temperature 250 ºC according to figure 10c. We found that the Ar pressure during sputtering can accelerate or hinder the surface termination of Ni. An increase of sputtering pressure from 2 to 20 mTorr at 250 °C had accelerated the transformation of Ni to [111], and no [200] was detected at the sputter temperature of 250 °C.

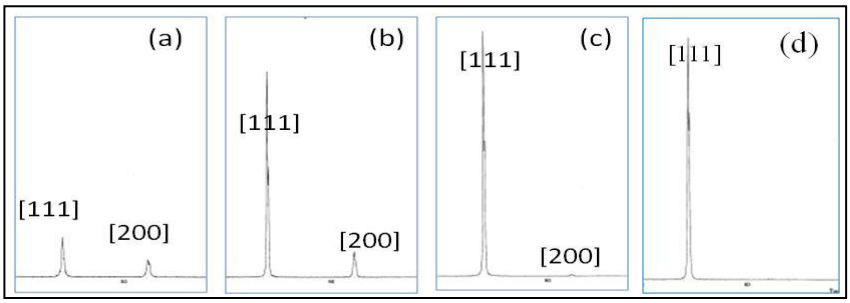

Figure 10. XRD patterns of Ni film after annealing relative to the initial sputtering conditions (a) 25 °C at 2 mTorr, (b) 100 °C at 2 mTorr, (c) 250 °C at 2 mTorr, and (d) 250 °C at 20 mTorr.

2.3.5 Role of H_2 in the APCVD Process

H_2 is needed during elevated temperature annealing and growth of graphene, otherwise oxidation will take over the process and prevent the diffusion, segregation, and precipitation process of carbon to the Ni surface. A deficient amount of H_2 will lead to oxidation of Ni that is characterized by darkening and roughening of the surface. When an excessive amount of H_2 over 40 vol.% was introduced during the annealing step, pinhole defect count increased astronomically, as shown in figure 11, for Ni samples initially prepared by sputtering at a temperature of 100 °C.

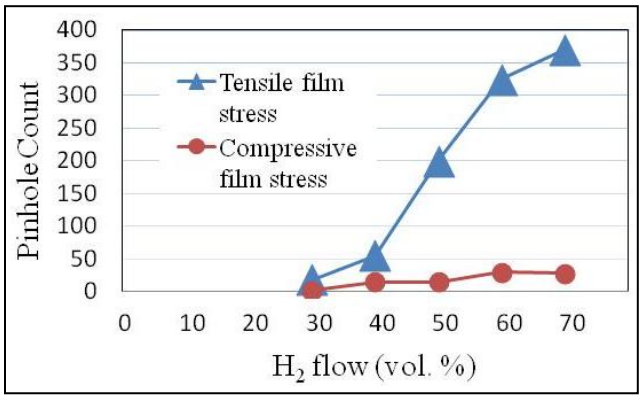

Figure 11. Pinhole count in Ni catalyst sputtered at 100 °C and 2 mTorr after annealing.

Pinhole defects were kept low with flow rates generally in the vicinity of 30 vol.%, but we found this varied more or less with the Ni grain boundary. We maintained a record of the minimum amount of H_2 needed to prevent oxidation and it appears to correlate linearly with the number of grain boundaries contained in Ni, as plotted in figure 12. A high flow of 40% H_2 was needed to prevent Ni oxidation when the number of grain boundaries was high compared to a low flow of 20% H_2 when the grain boundary count was low. The optimum concentration of H_2 was found to be directly dependent on the Ni grain boundary density, which is the inverse of the grain size.

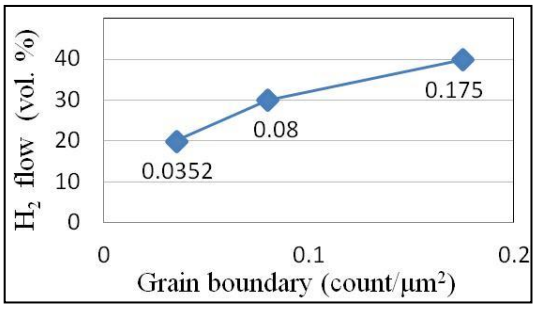

Figure 12. Influence of Ni grain boundary on H_2 flow requirement during annealing.

The relationship of residual film stress and the pinhole count was partially studied, and the results are shown in figure 12. The residual stress of sputtered 300-nm Ni film was typically tensile and above 100 MPa. We decided to prepare the Ni in a way to bring the stress to a compressive state. We did this by rapidly passing the wafer across the sputtering target, which decreased the deposition rate to 135 Å/min. The compressive films with residual stress of 12 MPa had fewer pinholes but each was much larger in size. Graphene growth was not reproducible on these samples possibly due to the excessive number of passes and layers needed to achieve a film thickness of 300 nm.

2.3.6 Graphene Growth

Ni catalyst was introduced into the APCVD system and the temperature was ramped up to between 900 and 975 °C. Graphene growth was accomplished by flowing 3–5 sccm of CH_4 for 10 min. After the graphene growth step, we ramped down the temperature of the furnace at a rate of 5 °C/min while maintaining the same flow rates of CH_4, H_2, and Ar. Figure 13a shows micro-Raman data from Ni sputtered at 25 °C with very broad peaks and relatively high I_D/I_G ratio greater than 10% that are indicative of high disorder in the graphene layer. When the Ni film was prepared by sputtering at 100 °C or higher, the peaks became sharp and more characteristic of crystalline materials, as shown in figure 13b, although the D peak is still very pronounced. When the samples had an additional annealing at 400 °C for 15 min before the start of the high temperature anneal and growth, the D peak was reduced.

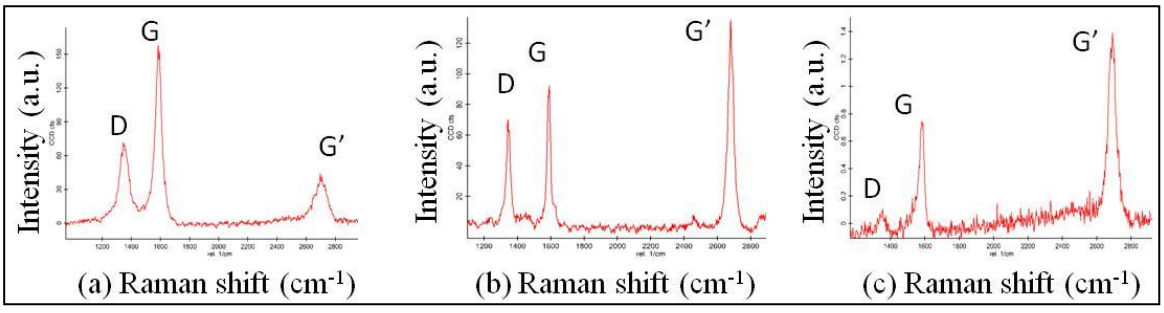

Figure 13. Micro-Raman data of APCVD grown graphene layers from Ni catalyst initially prepared by sputtering at (a) 25 °C, (b) 100 °C, and (c) 100 °C with additional 400 °C annealing.

BLG grown by APCVD on Ni substrates results in a turbostratic relationship between the individual layers (*45*). In this case, the stacking of the graphene layers is rotationally random with respect to one another along the c-axis. As discussed in reference 12, the Raman G' band appears as a single Lorentzian, just as in monolayer graphene but with a larger linewidth. The absence of an interlayer interaction between the graphene planes causes the Raman spectra of turbostratic BLG to look much like that for monolayer graphene, but now with a broader FWHM of ~45–60 cm^{-1} (*46*, *47*). Also the relative intensity of the G' feature to that of the G-band ($I_{G'}/I_G$) is much smaller for turbostratic graphene and the frequency is upshifted from that of exfoliated monolayer graphene. We postulate that BLG exists in our samples when the ratio $I_{G'}/I_G$ values is between 1 to 2 and the FWHM of the G' peak is between 45–60 cm^{-1}. We identified bilayer regions in figure 13c by the ratio $I_{G'}/I_G$ of ~1.85 and measured G' of ~55 cm^{-1} at FWHM.

2.3.7 Summary

We have studied the influence of the concentration of Ni interface boundaries on the formation of multilayer graphene domains. Syntheses of graphene by APCVD on the [111] face of single crystal Ni favors the formation of highly uniform monolayer/bilayer graphene on the Ni surface, and simultaneously hinders the formation of multilayer graphene domains. These results are based on a diffusion-segregation model for carbon precipitation on Ni surface, where the uniform and grain-boundary-free surface of Ni [111] single crystal provides a smooth surface for uniform graphene formation. In contrast, the rough surface of polycrystalline Ni with abundant grain boundaries facilitates the formation of multilayer graphene.

During the annealing and growth process of APCVD graphene, the grain size of the Ni catalyst can grow in various proportions and the initial sputtering temperature has a tremendous impact. The sputtering temperature needed to transform polycrystalline Ni film to the preferred [111] orientation was 250 °C, but this was accomplished with a high 20-mTorr Ar pressure that accelerated the process. The elevated sputter temperature process increased the grain size and greatly diminished the pinhole defect count in Ni catalyst. Bilayers of graphene were grown by APCVD method but any disorder was drastically diminished by annealing the sputtered Ni catalyst film at 400 °C prior to the high temperature annealing and growth process.

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3. Characterization by Raman Spectroscopy

3.1 Introduction

Raman spectroscopy (RS) has emerged as one of the most important metrology tools for study of the intrinsic properties of graphene. RS provides atomic-level structural, chemical, and even topological information. Such information is critical to the device fabrication engineer so that

judicial decisions can be made during the fabrication process of graphene-based nanoscale devices and sensors. A brief review of RS and its applications to graphene characterization can be found in pages 24–38 of ARL-TR-5873 (*27*). Other authoritative reviews are given in references 48 and 49.

Examples of the above-mentioned intrinsic properties of graphene are layer count, layer quality, stacking order, doping effects, and interface effects. However, it should be mentioned from the outset that the interpretation of the data collected by RS can be complicated or even intractable due to many interfering phenomena. Therefore, times do arise when corroboration by other techniques (e.g., TEM) is required. Regardless, the power of the technique for characterizing graphene and its related systems cannot be denied. Here we present examples from numerous case studies where RS has provided very valuable information related to these key material properties. Each example includes samples produce by mechanical exfoliation (ME) and CVD growth. We end this section with a few comments that we classify as "lessons learned" along with a brief update with regard to the established Raman mapping capability at ARL.

3.2 Case Studies

3.2.1 Layer Count

Ferrari and co-workers showed that it is possible to use the second-order G' feature in the Raman spectra of graphene to unambiguously determine number of layers in a ME graphene sample (*50*). In this study, the ME sample consisted of well-ordered Bernal AB stacking of graphene layers. The identification of the number of layers in CVD-grown samples can be more difficult due to the largely turbostratic relationship between the individual layers. For simplicity, recent work that has resulted in AB stacked BLG grown by CVD is shown here. The ME graphene work is part of a collaboration with the Jarillo-Herrero group, while the CVD graphene is with the Kong group, both of MIT.

The optical and Raman images of a ME graphene flake are shown in figure 14. The Raman image is formed via a cluster analysis algorithm that groups similar spectra. Groups are illustrated by color in the image below, and reveal regions of different layer count. A careful analysis of the symmetry of the G' peak can be used to determine precisely the number of layers in each region (*50*). Details related to stacking order (e.g., ABAB stacked) are discussed in subsection 3.2.3.

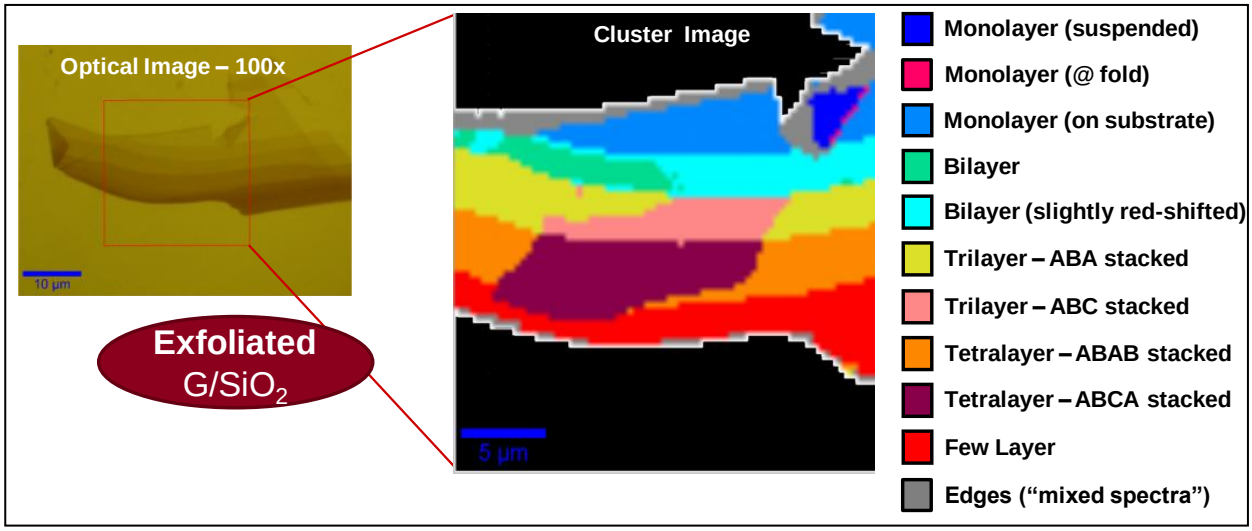

Figure 14. Optical and Raman image of a ME graphene flake. Layer count and stacking sequence (see subsection 3.2.3) are illustrated by color as indicated by the key to the right.

The optical and Raman image of a CVD-grown graphene region is shown in figure 15. In this work a method was developed to study BLG interactions and growth mechanisms using isotopic labeling of CVD-grown $^{12}C/^{13}C$ BLG. RS of these isotopically labeled bilayer samples shows a clear signature associated with AB stacking between layers, enabling rapid large-area differentiation between turbostratic and AB-stacked bilayer regions.

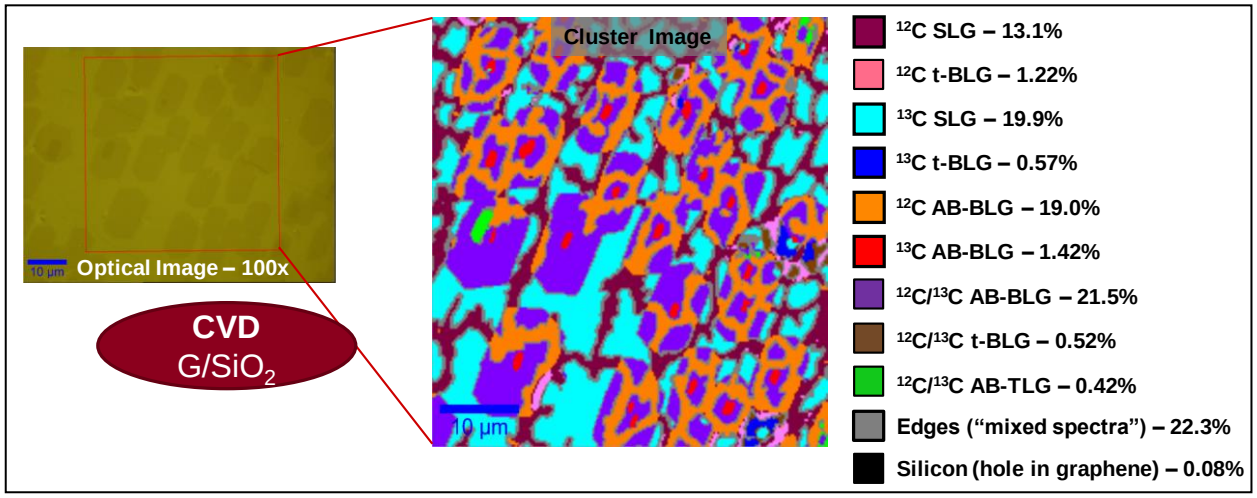

Figure 15. Optical and Raman image of a CVD graphene transferred onto a SiO_2/Si substrate. Layer count and stacking sequence (see subsection 3.2.3) are illustrated by color as indicated by the key to the right.

3.2.2 Layer Quality

Layer quality can be ascertained by monitoring the defect-related D peak. The D peak intensity is not related to number of layers, but rather to disorder in the widest possible meaning (*51*). In addition to disorder in the graphene crystal lattice, bubbles, folds, wrinkles, and tears in the

graphene layers can be easily distinguished from a Raman image. Examples of the latter for a ME graphene flake on a hexagonal boron nitride (hBN) substrate is shown in figure 16. An application of monitoring the D peak intensity in CVD-grown BLG is illustrated in figure 17. Here it was observed that D peak values "spike" in the ^{12}C BLG adjacent to ^{13}C layer growth in the isotopically labeled samples introduced in subsection 3.2.1.

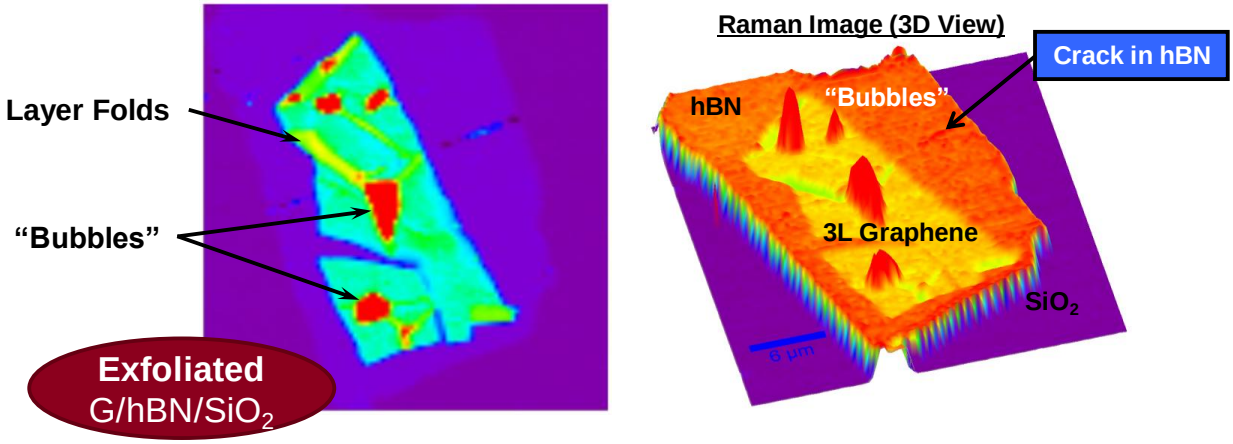

Figure 16. (Left) Raman image of a trilayer graphene (3LG) on a ME exfoliated hBN substrate and (right) a 3-D image of the background fluorescence revealing trapped organics between the graphene and hBN.

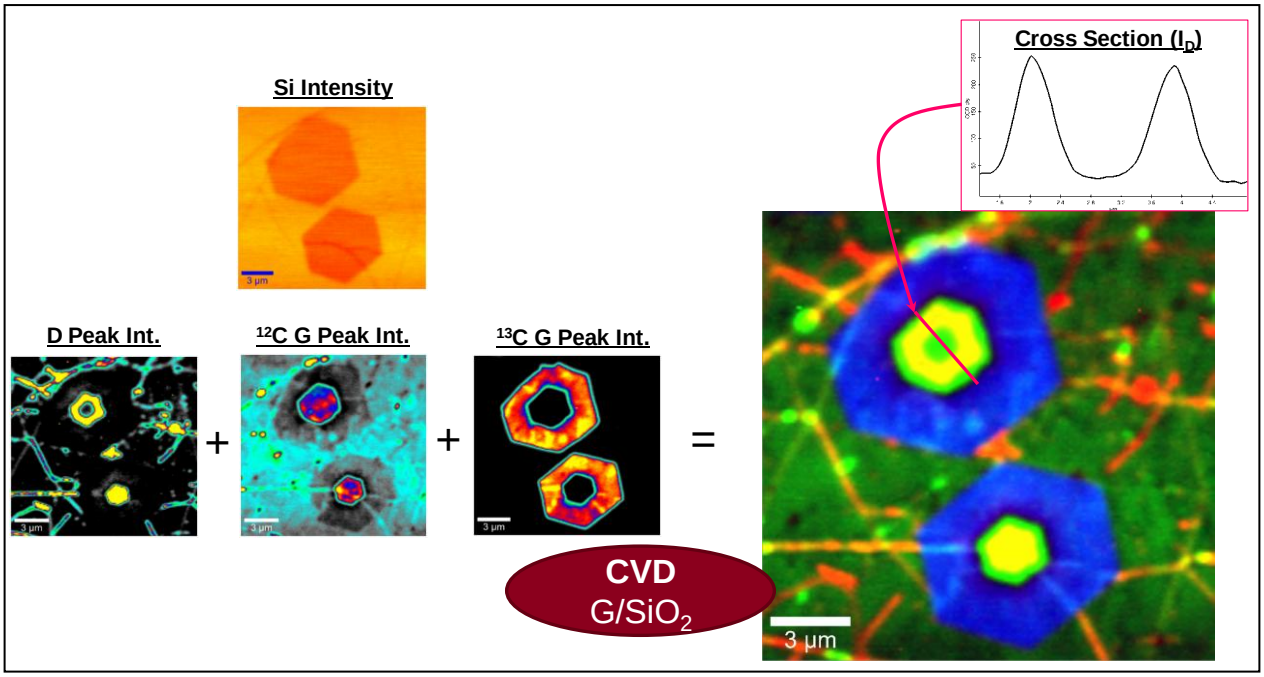

Figure 17. Raman image for the Si substrate together with Raman images for the intensity of the D band and G band for both ^{12}C and ^{13}C. The image and cross section on the right reveals that the "spike" in the D peak intensity (I_D) occurs with the ^{12}C second layer growth.

3.2.3 Stacking Order

The crystallographic stacking sequence of tri- and tetralayer graphene strongly influences the material's electronic properties. Seminal work on ME graphene on SiO_2 by the Heinz Group at Columbia University (*52*) and Dresselhaus Group at MIT (*53*) has demonstrated that RS can be an accurate and efficient method for characterizing stacking order by analyzing the distinctive features of the G' mode. Raman imaging allows for a direct visualization of the spatial distribution of Bernal (ABA) and rhombohedral (ABC) stacking in tri- and tetralayer graphene. Examples of ARL's efforts on stacking sequence identification of ME graphene on hBN and CVD-grown bilayer graphene on SiO_2 are shown in figures 18 and 19, respectively.

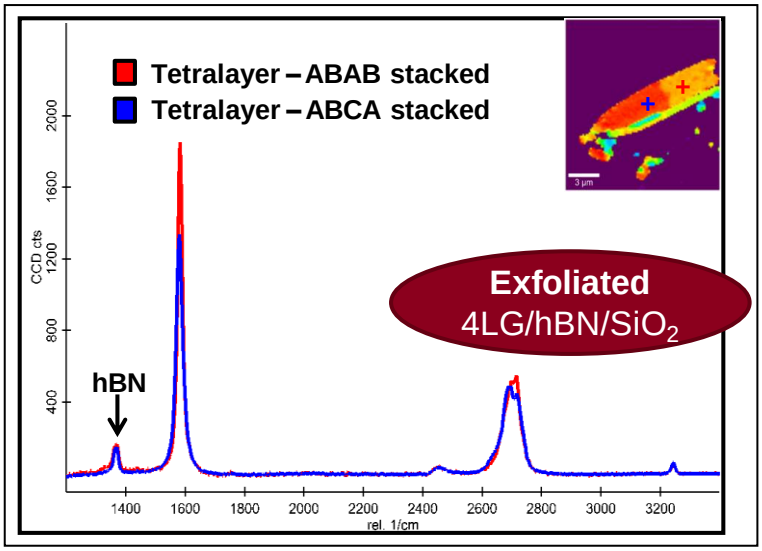

Figure 18. Raman spectra collected on a tetralayer graphene (4LG) ME flake. A change is stacking order from ABAB (Bernal) to ABCA (rhombohedral) is revealed by differences in the symmetry of the G' peak. The representative Raman image of the G' width (FWHM) is shown in the upper right-hand corner.

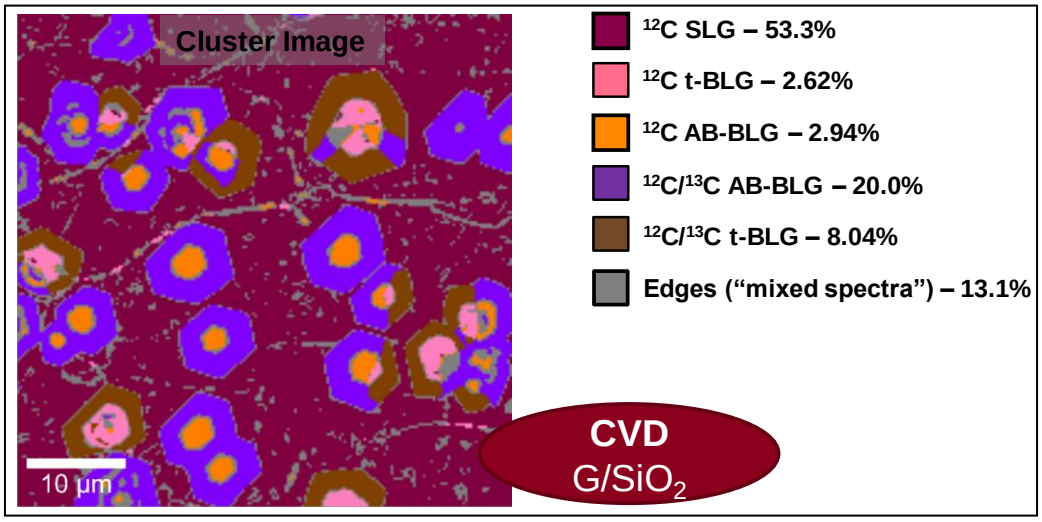

Figure 19. Raman image of a CVD-grown graphene transfer onto SiO_2. Layer count (SLG and BLG) and stacking sequence (t = turbostratic and AB = Bernal stacked) are illustrated by color as indicated by the key to the right. The percentage of the total area covered by each is provided.

3.2.4 Doping Effects

Raman measurements show that the G and G' peaks have different doping dependence and the $I_{G'}/I_G$ height ratio changes significantly with doping, making Raman spectroscopy an ideal tool for monitor the doping in graphene. The G band (found in all sp^2 bonded carbon materials) located at ~1580 cm^{-1} is sensitive to the C-C bond length, and its line width sharpens and peak position blue-shifts for both electron and hole doping. The G' band shows a different response

to holes and electrons. Therefore, its position can be used to distinguish between electron doping and hole doping. A red-shift indicates electron doping, while a blue-shift signifies holes (*54*).

An example of electron doping on a ME graphene monolayer on SiO_2 is illustrated in figure 20. In this case, the source of the doping is the substrate itself. The Raman image in figure 21 is of a heavily hole doped CVD-grown graphene layer on SiO_2. In addition to wrinkles in the layer, this image of the G peak position reveals evidence for charge (i.e., doping) inhomogeneities.

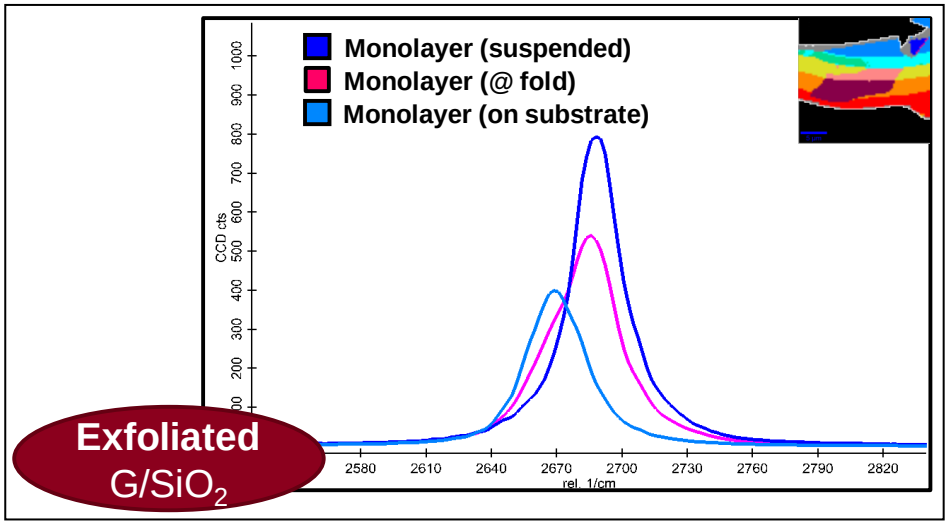

Figure 20. Raman spectra collected on the monolayer regions of a ME flake. Red-shifting of the G' peak indicates electron doping. See figure 14 for more image details.

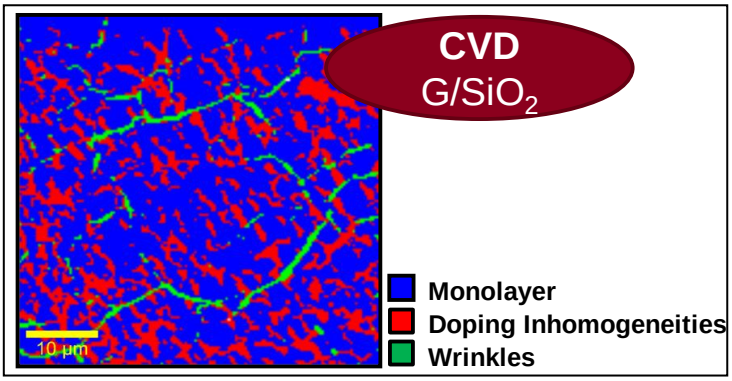

Figure 21. Raman image of a heavily hole doped CVD-grown graphene layer on SiO_2. This image of the G peak position reveals evidence for doping inhomogeneities, i.e., red areas are more heavily hole doped than those in blue.

3.2.5 Interface Effects

The current standard practice for the transfer of both ME and CVD-grown graphene does not take place in a cleanroom environment. Consequently, the potential for trapped particles and/or mixtures of water and organics to occur between the graphene and substrate are high. Trapped

particles often apply a stress to the graphene overlayer and organics tend to fluoresce. An example of a trapped particle beneath ME graphene is shown in figure 22, and a trapped carbon-containing fiber that occurred during a CVD-graphene transfer is shown in figure 23.

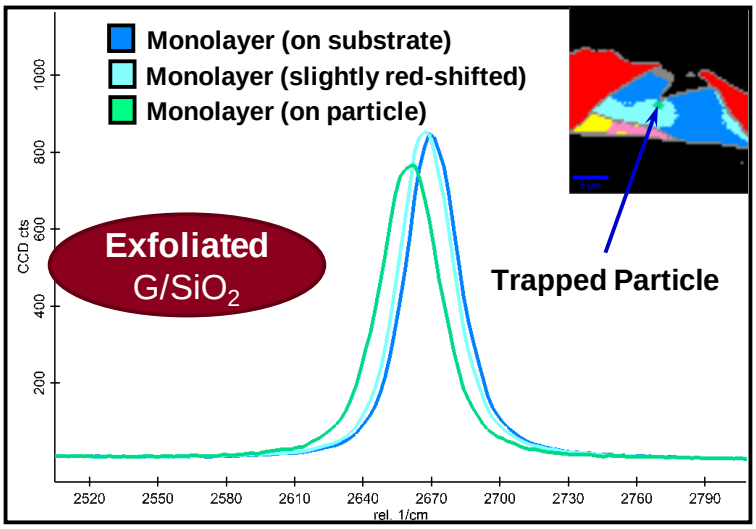

Figure 22. Trapped particle creates a stress field in the ME graphene flake that results in a red-shifted and broader G' peak. The representative Raman image of the G' peak position is shown in the upper right-hand corner.

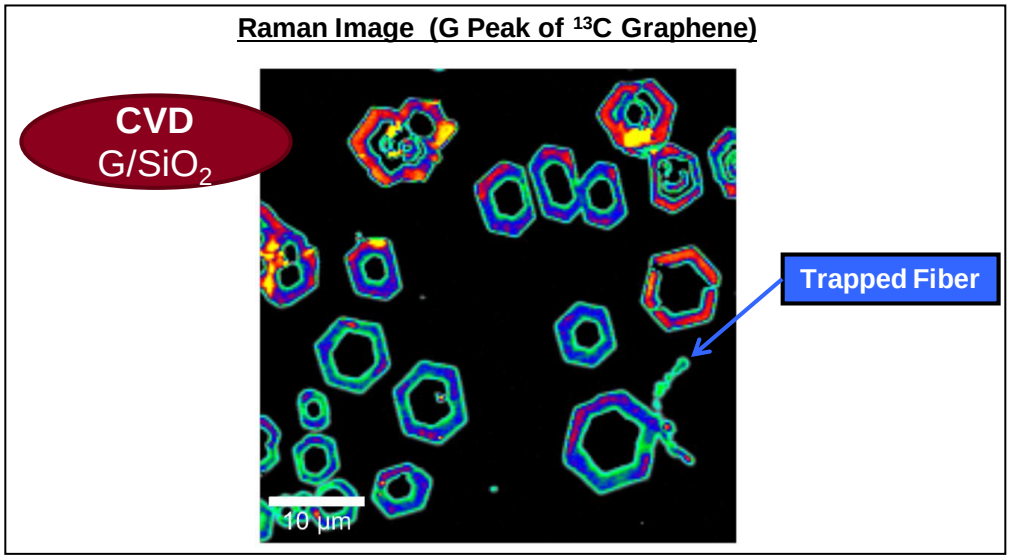

Figure 23. Raman image of the G band for ^{13}C only in an isotopically labeled CVD-grown $^{12}C/^{13}C$ BLG sample. A trapped carbon-containing fiber that is likely a result of the CVD-graphene transfer process is identified.

3.3 Conclusions

3.3.1 "Lessons Learned"

Raman lineshape analysis is best understood for ME graphene (bulk graphite + tape ⇒ graphene on substrate). In this case, standards have been developed and correlated to other techniques (e.g., TEM) that shed light on the number of layers, stacking order, and defects present in the exfoliated structures. On the other hand, accurate interpretation of the Raman spectra of CVD-grown graphene continues to pose a significant hurdle due to the turbostratic-like stacking that occurs for layer numbers >1. For example, the absence of an interlayer interaction between the graphene planes causes the Raman spectra of turbostratic BLG to look much like that for monolayer graphene. These issues are further complicated when the graphene is transferred to a substrate (e.g., SiO_2) due to peak height/position variations related to doping effects, as illustrated in figure 21. Therefore, it must be realized that it is not currently possible to precisely identify layer count information on CVD-grown graphene (with turbostratic stacking) from Raman spectroscopy alone.

3.3.2 Established Raman Mapping Capability

ARL's Raman mapping capability, established in some measure by the Graphene-based Nanoelectronics DSI, is recognized as state of the art by fellow researchers at MIT, Rice University, and the National Institute of Standards and Technology. A detailed summary of this capability is provided on page 36 of ARL-TR-5873 (*27*). It should be mentioned that continual efforts are being put forth in order to broaden these capabilities. In the past year, a heating stage that mounts directly to the high-resolution piezo stage (allowing for the required scanning action) has been added to the system. This stage allows for precise temperature-dependent measurements in both single-point and scanning modes. Additionally, a 488-nm laser and considerable software functionality was acquired.

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4. Graphene Electronic Devices from CVD-grown Graphene

4.1 Device Fabrication and Design

In this third year, substantial progress was made in developing improved fabrication processes (as shown in figure 24) and device designs (with examples shown in figure 25) to increase electrical performance such as the FET mobility and explore other device structures for extracting resistance measurements including transmission line model (TLM) structures and Hall bar structures.

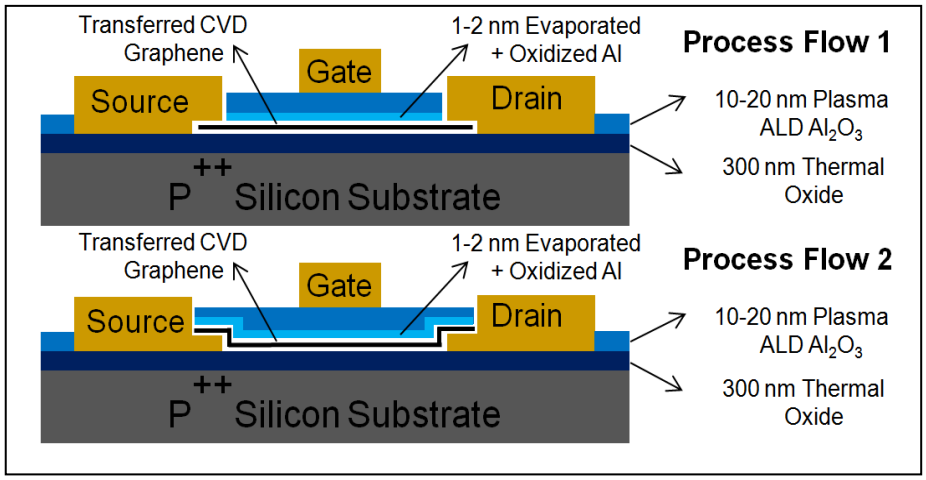

Figure 24. Schematics of two of the updated process flows. SiO_2 on Si substrates are used as the foundation for these two processes. Graphene is transferred onto these substrates using cleaner methods than used a year ago, providing better quality graphene with reduced contamination and trap charge issues. Metals are deposited via e-beam evaporation, thermal evaporation, and sputtering depending on the metal, and dielectrics such as aluminum oxide (Al2O3) is deposited via atomic layer deposition.

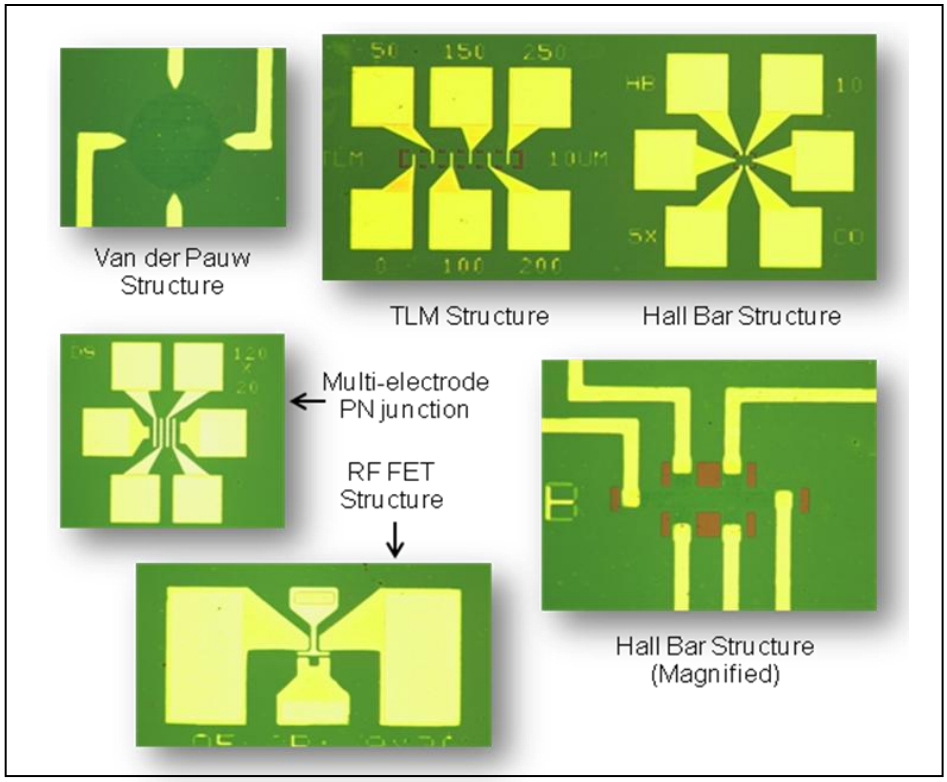

Figure 25. Optical micrographs were taken from various graphene test structures sitting on Si/SiO_2 substrates. These structures provide the capability to inspect different electrical properties of the graphene, as well as different methods to review the same electrical properties in some cases.

4.1.1 Initial Graphene Electronic Device Fabrication and Characterization Efforts

At the beginning of the program in FY 2010, fabricated devices were based on replications or technical transfers of processes and designs from university partners such as MIT. The initial devices fabricated and characterized at ARL were GFETs with a bottom and top gate structure. The GFETs were patterned using a standard optical lithography with gate-lengths ranging from 20 to 3 µm. In the first year, the best devices possessed carrier mobilities of approximately 530 $cm^2/V•s$ for holes and 336 $cm^2/V•s$ for electrons. Additionally, the maximum extrinsic cut-off frequency (f_T) achieved with these GFETs was approximately 1 GHz using both top and bottom gating. In the second year of the program (FY 2011), we were able to improve the GFET extrinsic cut-off frequency to 3 GHz (threefold increase) through improved processing, while exploring ways of increasing the carrier mobilities of our devices. Boron nitride substrates were explored, replacing SiO_2 as the base substrate for our GFETs, allowing the carrier mobilities of our devices to reach a peak of 3,000 $cm^2/V•s$ for holes and 1,500 $cm^2/V•s$ for electrons. Figures 26 and 27 from ARL-TR-5873 (*27*) provide schematics and the field-effect mobility plots for example devices of GFETs described above.

4.1.2 Improved Graphene Structures and Process Flows for Photolithography

In the final year of the DSI, new mask designs and process flows were developed for photolithography to improve upon previously used designs and processes, providing more reliable, better performing graphene devices. The addition of alignment and marker layers has allowed for direct inspection and interrogation of the active/channel areas of the graphene devices using Raman spectroscopy, AFM, optical microscopy, and compositional analysis (such XRD and energy-dispersive x-ray spectroscopy [EDX]). Going beyond proof-of-concept devices, graphene devices fabricated on Si/SiO_2 substrates needed to be improved to be able to be made readily and reliably to support efforts in developing compact models of graphene FET structures. Both p- and n-type graphene FETs were fabricated, as shown in figure 26, along with the Raman mappings of the graphene channel, showing the D- and G/2D-peak intensities. The updated designs and process flows have netted an average of 5–10 times improvement over devices fabricated in the previous year. Typical carrier mobility values from last year's devices fabricated on Si/SiO_2 substrates ranged from <100 to 1,000 $cm^2/V•s$ from devices with gate lengths ranging from 1 to 50 µm. Recent devices have typically shown carrier mobility values ranging from 500 to 5,000 $cm^2/V•s$ from devices with gate lengths ranging from 10 to 30 µm.

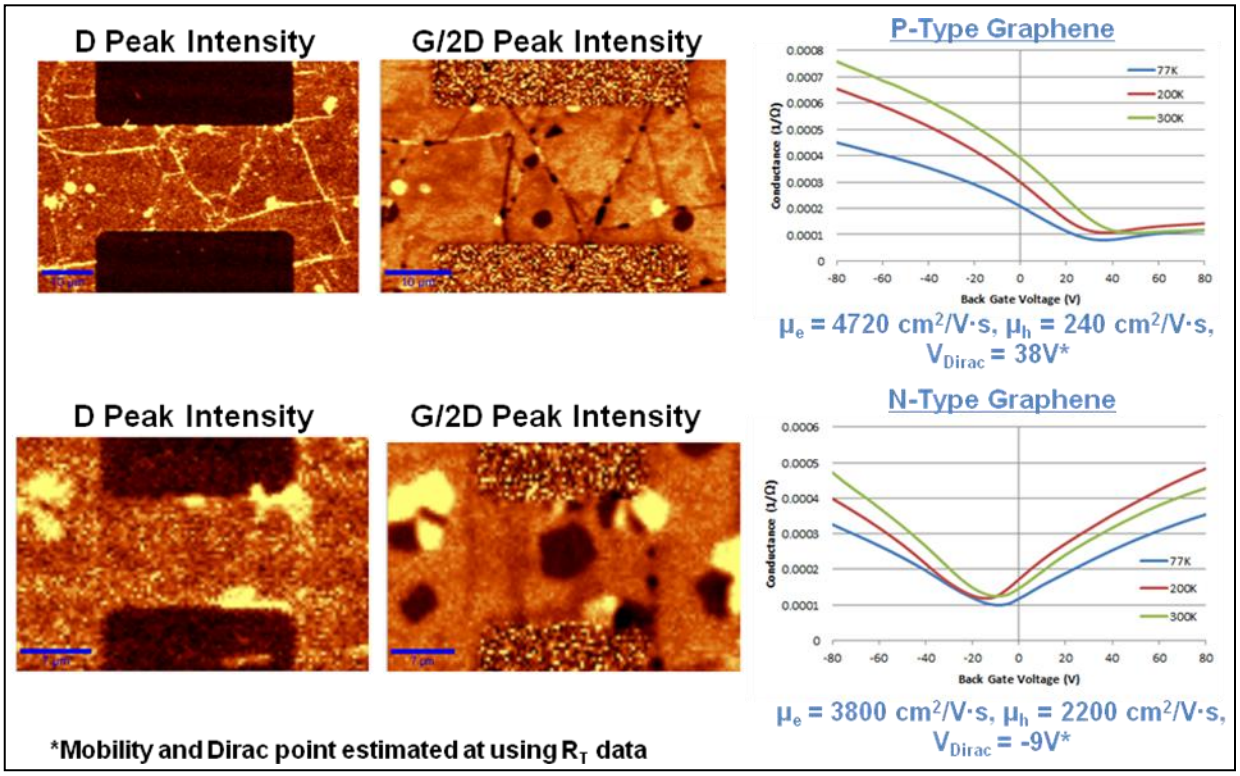

Figure 26. The D- and G/2D-peak intensities from the RS mappings of the graphene channel for two graphene FETs. The conductance vs. back gate voltage for a graphene FET with (top) a p-type graphene channel with an electron mobility estimated to be around 4,720 $cm^2/V•s$, and a hole mobility of approximately 240 $cm^2/V•s$ and (bottom) a n-type graphene channel with an electron mobility estimated to be around 3,800 $cm^2/V•s$ and a hole mobility of approximately 2,200 $cm^2/V•s$. Electron and hole mobilities in excess of 5,000 $cm^2/V•s$ have been measured from graphene FET devices designed and fabricated at ARL with typical channel dimensions of 20 µm (W) x 80 µm (L), sitting on Si/SiO_2 substrates.

Complementary graphene test structures were also designed including Hall bar, van der Pauw, TLM, capacitor, tunneling, internal photoemission, and p-n junction structures. These structures, shown in figure 25, allowed for additional properties to be directly reviewed. Graphene FET structures were specially fabricated for both DC and RF measurements. The development of these test structures has been complemented in parallel with the installation and development of associated test systems including a custom-built cryostat unit capable of testing packaged graphene devices with up to 40 DC electrical connections and 1 RF electrical connection. Current and voltages can be both measured and sourced at values ranging from 1 pA to 100 mA, and 1 mV to 20 V, respectively. Devices can be tested in various conditions, including pressures ranging from 800 to $1x10^{-6}$ Torr, magnetic fields ranging from –1 to 1 T, and temperatures ranging from 77 to 400 K. This system, shown in figure 27, was constructed this year to perform resistivity measurements as well as Hall effect measurements. Additionally, ARL has continued to pursue the fabrication of graphene FETs on flexible polyimide substrates. Process refinements have led to a greater repeatability and reliability among the devices fabricated. Performance

values at this time are similar to what have been published previously with carrier mobility values in the low hundreds. Additionally, graphene devices have been fabricated on a variety of flexible substrates to review the feasibility of creating flexible graphene electronics. Devices have been fabricated and demonstrated on Kapton tape, polyimide wafers, and polyethylene terephthalate (PET) sheets, with devices successfully tested on all three materials. Effective carrier mobility values were all approximately an order of magnitude lower than those demonstrated on SiO_2 substrates.

Figure 27. The cryostat unit constructed for measuring graphene resistivity and the Hall effect. This system is fully automated, using custom-written software (on a computer not shown in the image), and is capable of changing various environmental conditions including pressure, temperature, and magnetic field.

4.1.3 Graphene Transistors and Novel Structures using E-beam Lithography

To be able to explore the ballistic carrier conduction properties in graphene and review novel device structures such as metal-insulator-graphene tunnel junctions, designs and fabrication processes were developed based on e-beam lithography (EBL) capable of minimum feature sizes of 7 nm. A variety of high-resolution photoresists were tested with the EBL system to produce graphene structures with reduced dimensions. Device structures that were fabricated include RF FETs for RF analog switches, metal-insulator-graphene (MIG) tunnel junctions, metal-insulator-graphene-insulator-metal (MIGIM) transistors, Hall bar test structures, and TLM test structures. All devices and test structures were fabricated with various dimensions ranging from 300 nm up to 90 µm as the critical dimension. Figure 28 provides a micrograph of a completed device set. The devices were tested through typical electrical current-voltage (I-V) characterization using a Keithley 4200 semiconductor characterization system and a cryogenic probe station. An example of such measurements can be seen in figure 29, depicting the I-V characteristics of a MIG tunnel junction at different back-gate bias values.

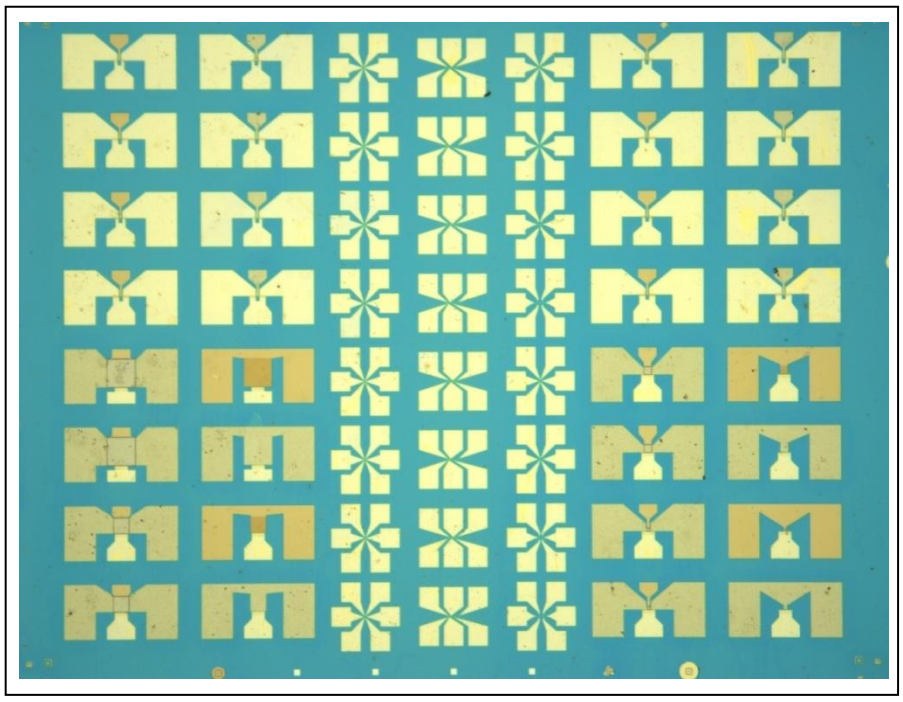

Figure 28. Micrograph of a set of fabricated graphene-based devices is shown here with three metal layers, two insulator layers, and a transferred graphene layer. Device designs include transistors, MIG structures, MIGIM transistors, Hall bar structures, and TLM test structures.

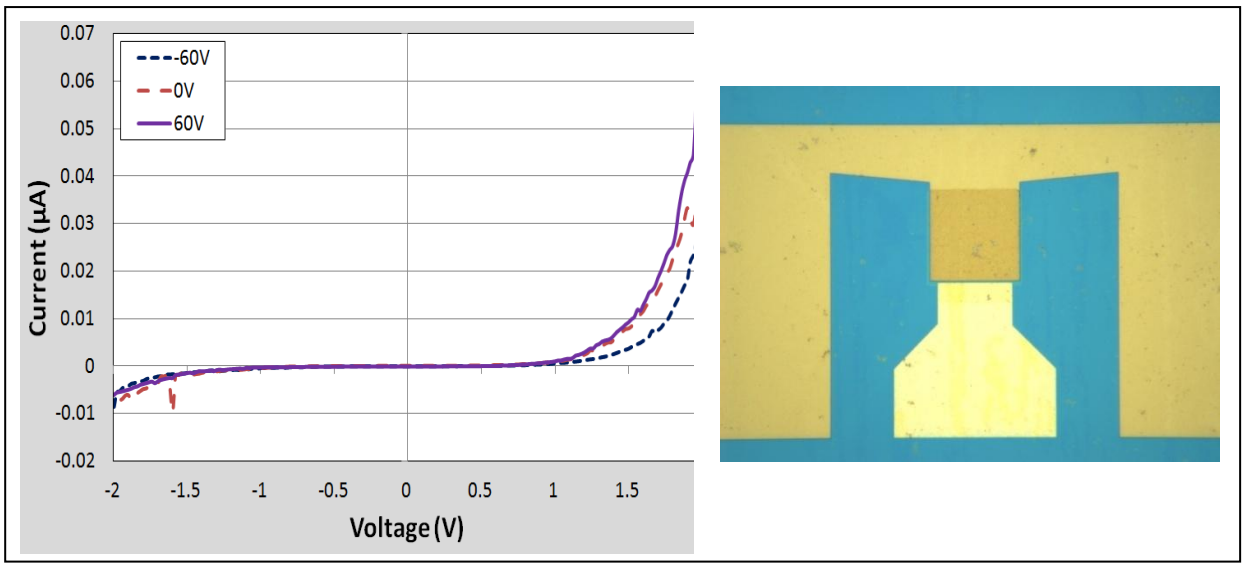

Figure 29. I-V characteristics for a typical MIG device using an aluminum (Al) top electrode, 5-nm-thick aluminum oxide (Al_2O_3) insulator layer, and a graphene bottom electrode. Each trace represents a back-gate bias applied to the entire tunnel junction between the n++ Si substrate with 300 nm of SiO_2 and the tunnel junction.

4.2 Modeling and Simulation

4.2.1 Initial Efforts: Gradual-channel Modeling

Work in the first year of the graphene modeling effort focused on laying the groundwork for a device simulation program that could incorporate the unique features of graphene into a standard package for circuit simulation and device synthesis. With the goal of avoiding large-scale computer simulation except when necessary, the modeling approach was to combine graphene physics with traditional analytic ("physics-based") device models, which were based on bulk semiconductor properties and classical electrical/fluid dynamic analysis. These models were found to be unsatisfactory due to unphysical features of the electrical characteristics (e.g., negative resistance) which were not seen in experiments with fabricated devices. Early results included the following:

- A lengthy ARL technical report (ARL-TR-5281) on the gradual-channel modeling of graphene FETs (*55*) based on current III-V high electron mobility transistor (HEMT) device models, including low dimensionality and ambipolar character of the charge transport. Several types of carrier scattering were included, and the differing I-V curves resulting from these scattering assumptions were detailed.
- Development of an RF equivalent circuit, as part of a fitting program to link RF measurements with device electrical and material parameters.
- A second ARL technical report (ARL-TR-5481) on the modeling of graphene-loaded capacitors/varactors (*56*). This report discussed the simplest model of the graphene FET gate structure, i.e., a parallel-plate capacitor with a graphene layer sandwiched between two dielectrics (figure 30 shows a drawing of the capacitor).

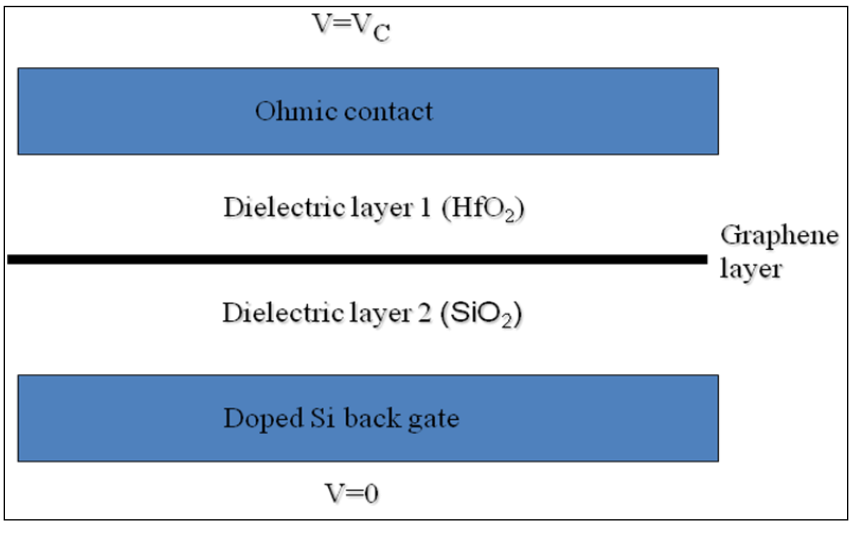

Figure 30. Graphene-loaded capacitor.

Due to its simplicity, this structure can be analyzed in great detail, making it possible to replace the empirical voltage of the graphene FET on channel density with a true quantum-mechanical expression. An additional byproduct of this analysis is the possibility of studying the capacitor itself at large signal levels, i.e., treating it as a varactor. Figure 31 shows the response of the graphene varactor at the 2nd harmonic of the applied voltage.

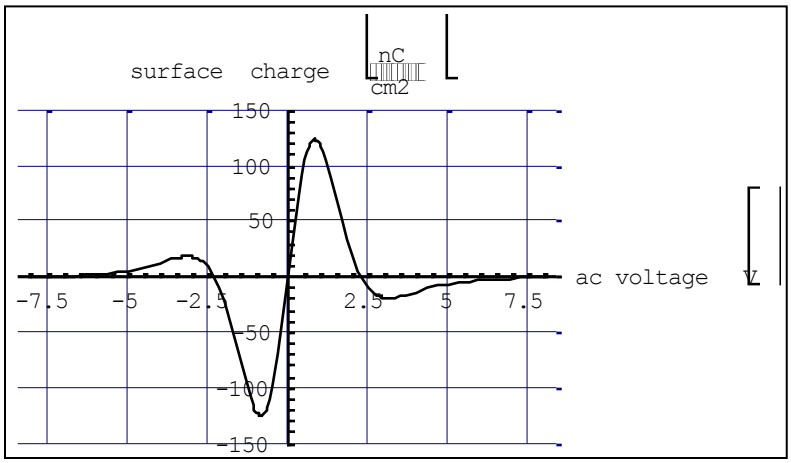

Figure 31. The 2nd harmonic surface charge density vs. AC voltage.

The feasibility of using graphene capacitor structures was evaluated in the studies that are described in section 4.2.2.

4.2.2 MIGCAP Modeling

Capacitance-voltage (C-V) measurements can be used to characterize metal/insulator/graphene capacitors (MIGCAPs) to judge the quality of the material interfaces. By comparing the measured C-V to the modeled C-V, the interfacial-defect density (D_{it}) and distribution as a function of energy can be extracted. With this in mind, we have developed a model (*56*, *57*) and corresponding computer code to calculate the ideal C-V and the C-V including a constant D_{it} distribution. Figure 32 shows the planar MIGCAP geometry; the effective circuit model used to calculate the gate C-V (C_G) and the equations for C_G, the oxide capacitance (C_{OX}); the interface-defect capacitance (C_{it}); the electron and hole concentrations (n and p, respectively); and the quantum capacitance in graphene (C_Q).

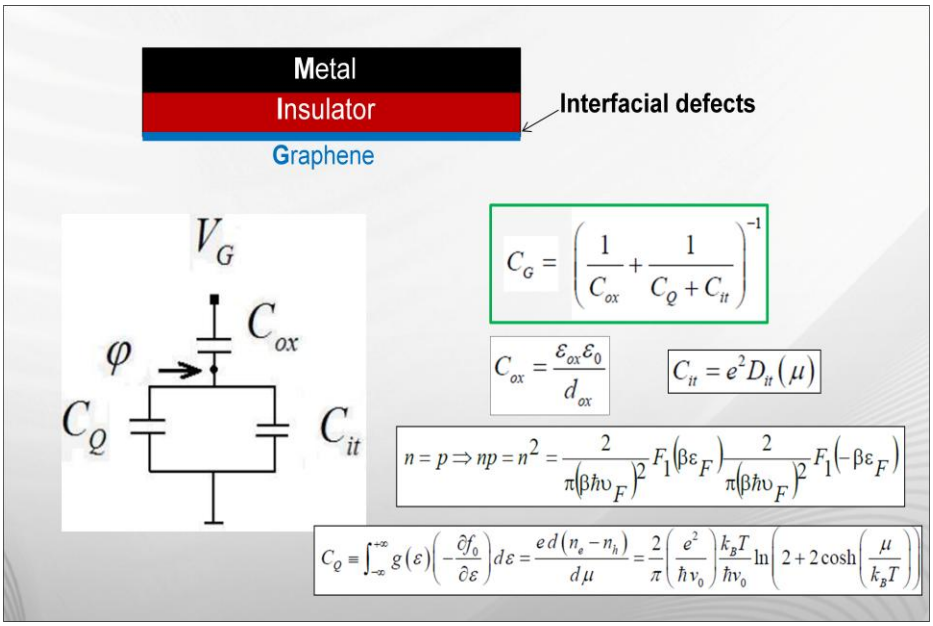

Figure 32. MIGCAP sketch and equivalent circuit model.

Figure 33 shows the linear bandstructure of graphene and two possible D_{it} distributions, constant and parabolic. In this work, we have assumed a constant D_{it} distribution when calculating C_G, where the magnitude of D_{it} can be varied to fit the measured CV.

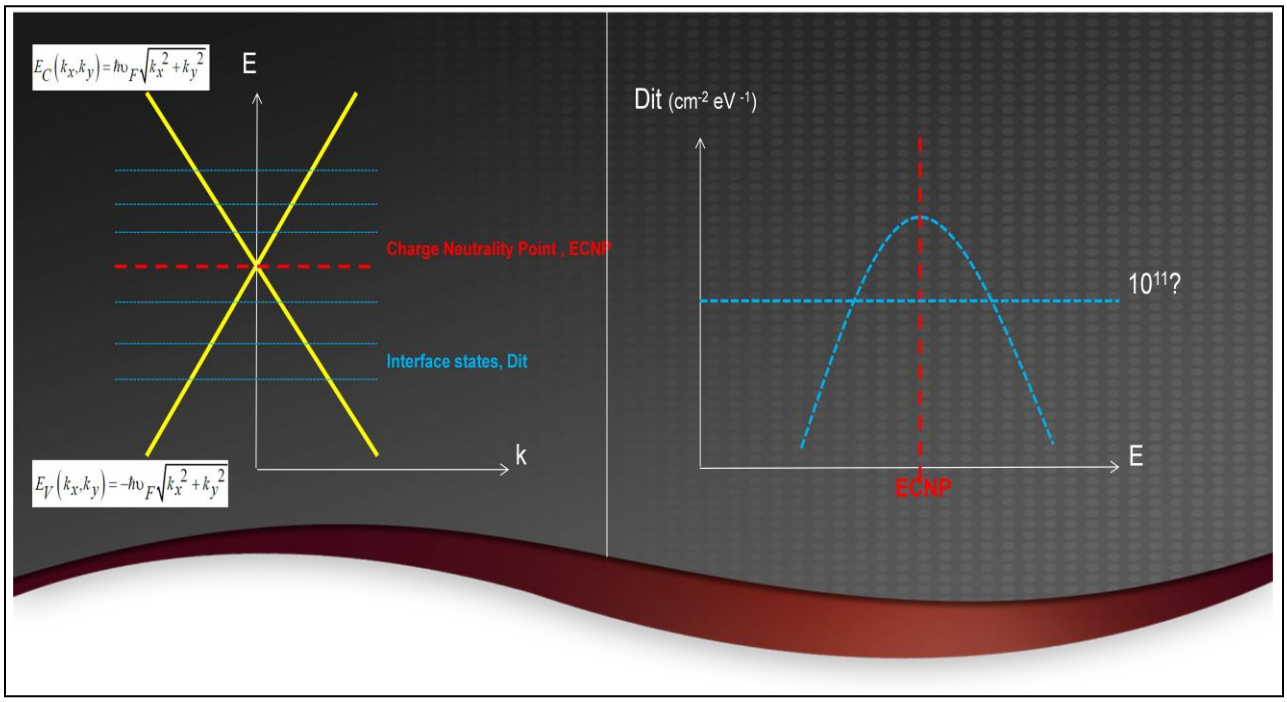

Figure 33. Graphene bandstructure and example D_{it} distributions.

Figure 34a shows the Fermi level reference to the charge-neutrality point of graphene as a function of the gate voltage (V_G) and for different constant values of D_{it}. This figure illustrates the Fermi-level pinning effect, where it takes a larger V_G to move the Fermi-level when there is a large D_{it} present. This is further illustrated in figure 34b, where we see a lower electron (or le) concentration as D_{it} is increased and V_G is held constant. In other words, more of V_G is dropped to charge D_{it} states as D_{it} increases and less V_G contributes to the creation of mobile charge. Finally, figure 35 shows C_G as a function of V_G for various values of D_{it}. This figure shows the tell-tale signs of D_{it} that can be seen experimentally observed, that is, an increase of the minimum and an overall smearing out of the capacitance as D_{it} increases.

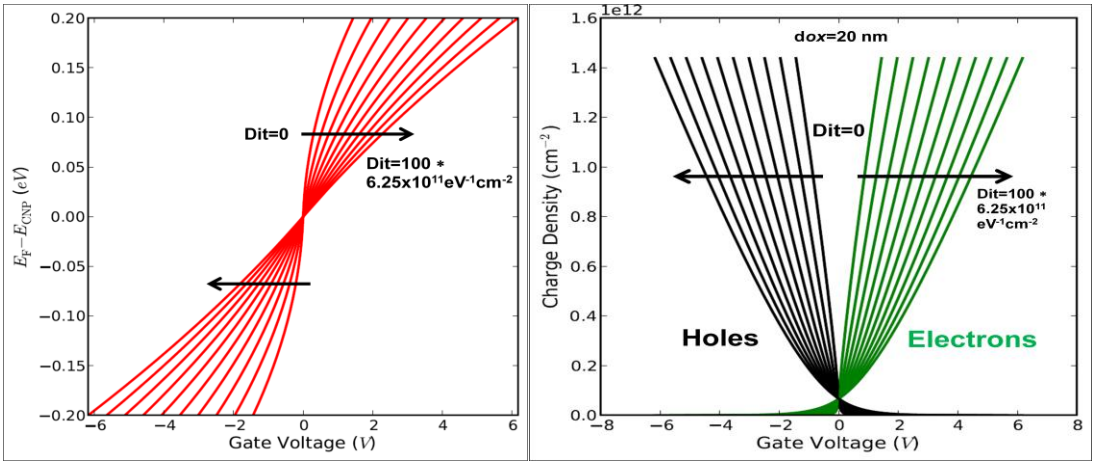

Figure 34. Fermi level pinning. (a) The Fermi-level reference to the charge-neutrality point. (b) Electron and hole concentrations for increasing D+.

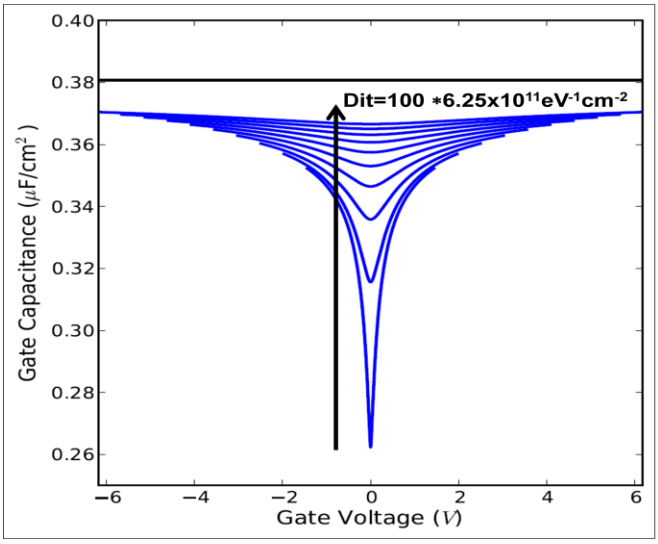

Figure 35. The calculated gate capacitance for increasing D_{it}.

4.3 Application-related Device Performance

In order for graphene-based devices to be used in place of other technologies in applications, certain specific tests need to be done mimicking situations that will be encountered in real-world applications. One particular test is to pulse the drain-to-source or gate-to-source bias voltages with signals having a very short rise time to observe the effects of charge carrier traps. This biasing configuration is that of a common source amplifier and in this test we would observe timing issues within the device due to charge carriers being trapped or de-trapped by traps at various physical locations in the transistor. Here we test the graphene FET (GE-W258-X-F1) having chromium (Cr)/gold (Au) contacts. The DC and transient device electrical characteristics were analyzed using ground-signal-ground coplanar waveguide probes connected to high-speed pulsers through SMA cables. Figure 36 shows the probed device. The DC characteristics are shown in figure 37.

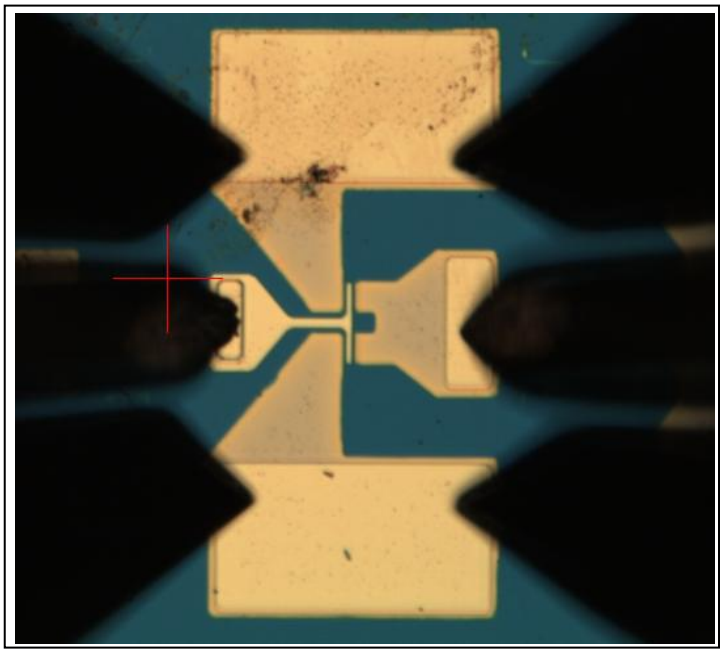

Figure 36. Graphene FET in a coplanar waveguide layout configuration being probed with ground-signal-ground probes.

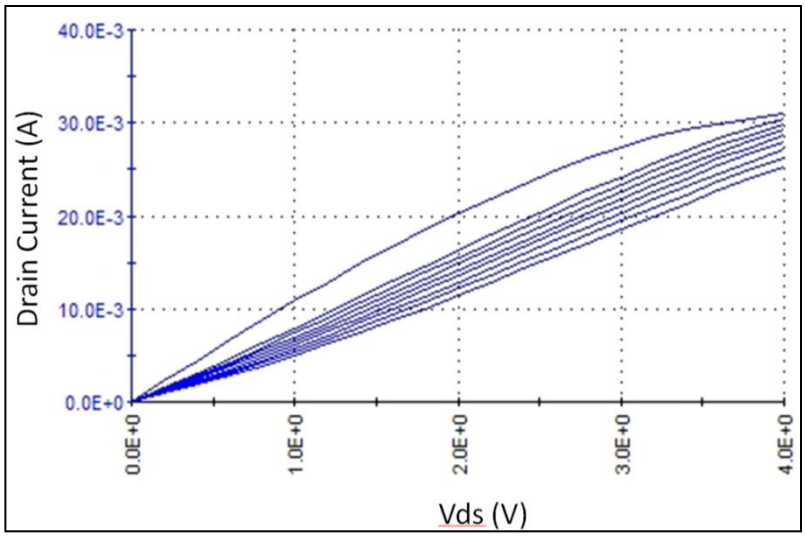

Figure 37. DC I-V data of a graphene FET. The curves from top to bottom correspond to gate biases of –4 to 4 V in steps of 1 V.

The pulsed drain current and gate voltage characteristics are shown in figure 38 for a previously unprobed device of the same design as that measured for figure 37 and the same device after 5 min of operation. The gate-to-source potential is pulsed from 0 to 4 V while the drain-to-source potential is simultaneously pulsed from 0 to 9 V. Both pulses are 5 μs long with a duty cycle of 0.1% to minimize device heating. The pulsed results indicates that drain current has an overshoot and then decays to a steady level within a microsecond, after which the current appears to slowly increase again. The initial drop could be due to carriers being trapped by fast-acting traps after the device is turned on. Then the current increases slowly between 2 and 5 μs due to free carriers being released from these and/or other traps. Traps responsible for this behavior are possibly located at the interface between the graphene layer and the SiO_2 passivation layer. Also, one notices in figure 38, that the on-state drain current drops from around 15 to 5 mA after 5 min of operation. This is a reliability issue of the current graphene FET that is being looked into.

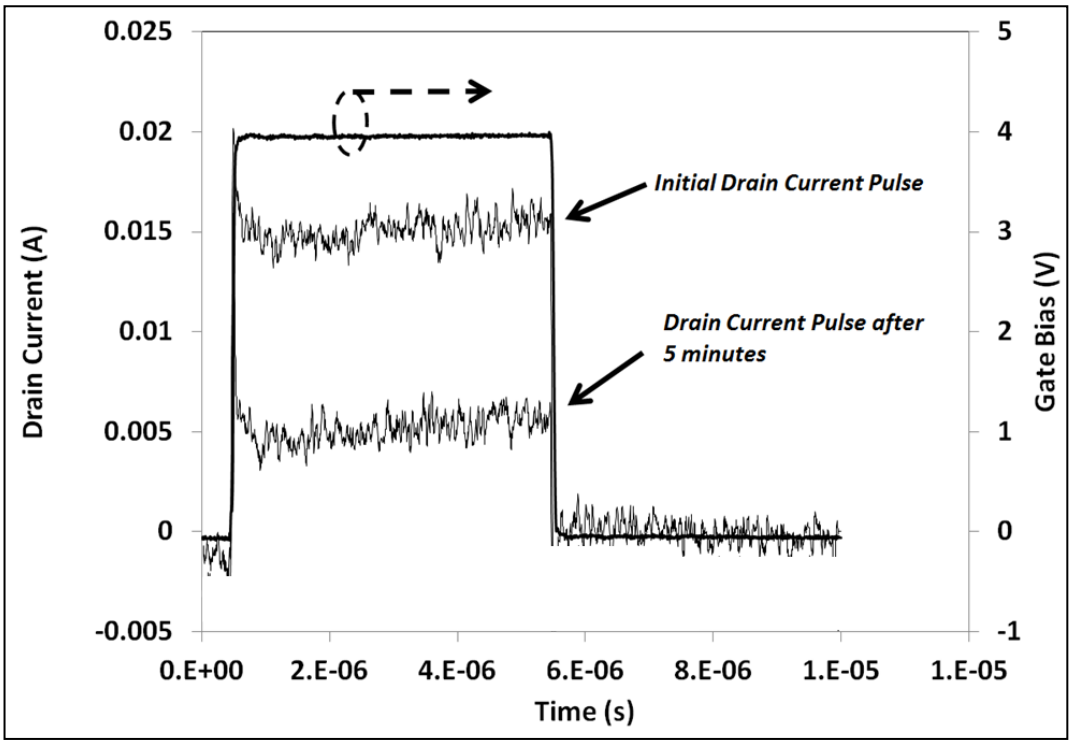

Figure 38. Transient analysis of a graphene FET. The gate-to-source potential is pulsed from 0 to 4 V while the drain-to-source potential is simultaneously pulsed from 0 to 9 V. Both pulses are 5 µs long with a duty cycle of 0.1%

5. Graphene Supercapacitors

5.1 Introduction

Electrical energy storage and handling is a critical and ubiquitous need of the Army. Supercapacitors have several advantages over conventional batteries, including higher specific power (~2 orders of magnitude higher), higher cycle life (millions of charge/discharge cycles), rapid charge/discharge times (seconds to minutes), high efficiencies (up to 98%), and unaltered performance in extreme heat and cold (*58*). Increasing supercapacitor energy and power densities will make them more useful for portable power applications. Carbon materials with improved surface area would increase the capacitance of supercapacitors. Graphene (G) is a candidate material being studied at ARL for supercapacitor applications. Extremely large capacitances may be obtainable if G can be assembled in a manner that optimizes the electrode surface area that is accessible to the electrolyte.

Previous supercapacitor work under this DSI (*24*, *27*) has focused on developing CNT- and G-based electrodes that will store more energy and deliver more power than activated carbon electrodes, which are the commercial standard. The initial work focused on a systematic

comparison of CNT solution preparations and deposition methods. It was found that the solution composition was critical as many additives coated the CNTs, greatly decreasing the porosity and capacitance of the resulting electrodes. The deposition methods were found to have minimal effect on the specific capacitance, which was about 35 F/g for single-wall CNTs (SWCNTs), which is less than expected. Our experiments with metallic and semiconducting CNTs have shown that density of states/quantum capacitance is not limiting the capacitance achieved with CNTs. Therefore, it is likely that bundling of the tubes is limiting the capacitance achieved. As a result, SLG was investigated as a more suitable electrode material, as was adding additional nanomaterials for improving performance. Our work with model SLG electrodes demonstrated a potential capacitance increase of over four times more than activated carbon, which is used in commercial supercapacitors (if the electrode fabrication can be fully optimized). Our SBIR partner Vorbeck Materials has already captured a large fraction of this potential performance (200 F/g) while our other SBIR partner JME, Inc., has demonstrated high frequency performance opening up new applications. In the most recent year, the work has focused on three aspects: including additional nanomaterials to increase energy storage through pseudocapacitance, developing inkjet printed flexible supercapacitors, and demonstrating an energy harvesting application using high frequency supercapacitors.

5.2 Pseudocapacitors

Supercapacitors have significantly lower energy densities than batteries, which limit the applications for supercapacitors. The addition of pseudocapacitance, that is, chemical reactions similar to those in batteries but which behave electrically like a capacitance, can be used to increase the energy density of supercapacitors (*59*). This work focused on increasing the capacitance of CNT- or G-based supercapacitors by adding pseudocapacitive manganese oxide (MnO_x) nanoparticles (NPs) (*60*). Solution-based processing was chosen for this work as it is manufacturable and it does not impose significant thermal and chemical constraints on the underlying current collector. A number of methods were investigated for fabricating CNT/graphene/MnO_x composite electrodes using the thermal reduction of manganese acetate (MnAc) to produce MnO_x NPs: dry mixing and grinding, solution mixing, solution freeze drying to prevent segregation, hydrothermal synthesis at 200 °C for 14 h, and spray drying, which was done with the assistance of Prof. Hongwei Qiu at the Stevens Institute of Technology. Some methods (dry/solution mixing) were abandoned as they did not result in sufficient mixing of the MnO_x and G/CNTs. Another (freeze drying) was abandoned due to the difficulty in making sufficient material on a laboratory scale. Both hydrothermal processing and spray drying appear to be promising methods for coating G/CNTs with NPs. MnO_x NP pseudocapacitance has been successfully incorporated into CNT/G-based supercapacitors using the hydrothermal and spray dried methods, as can be seen in figures 39, 40, and 41.

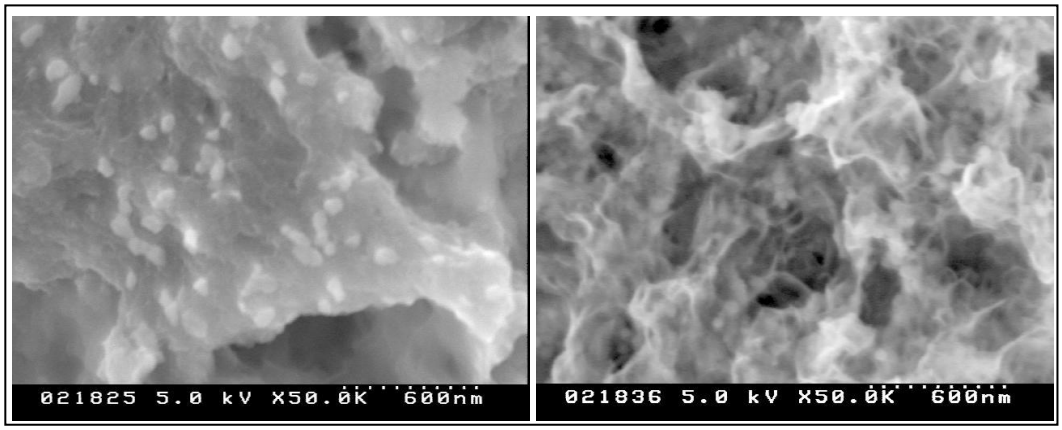

Figure 39. SEM images of hydrothermally produced MnO_x NPs on CNTs (left) and reduced graphene oxide (rGO) (right).

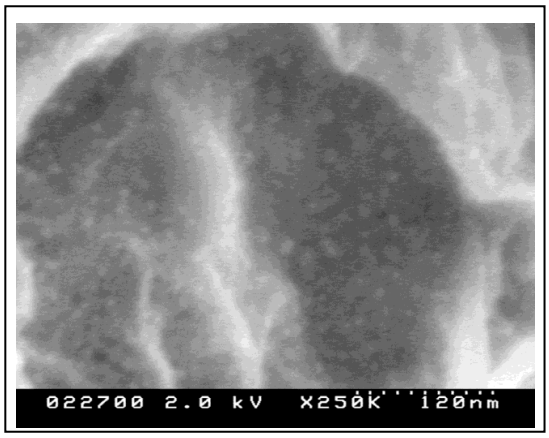

Figure 40. SEM of MnO_x NPs formed on rGO using the spray dry process.

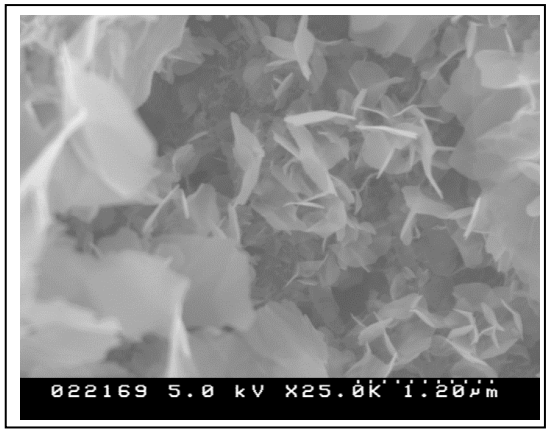

Figure 41. SEM image of MWCNT/MnO_x NP electrode after 9000 cyclic voltammetry (CV) cycles showing MnO_x NP platelet formation.

Electrodes were fabricated by drop casting solutions containing the graphene oxide (GO)/CNT/MnAc materials onto titanium (Ti) or stainless steel current collectors and then annealing them to reduce the GO or convert the MnAc to MnO_x as needed. Testing was performed using CV and electrochemical impedance spectroscopy (EIS) on a potentiostat typically using a three-electrode setup with a large excess of electrolyte. The CV scan rate for the majority of the testing was 20 mV/s. The voltage range of scan was 0 to 0.7 V (versus the silver/silver chloride electrode when using the three-electrode mode). The electrolyte typically used in this study was 0.5 M potassium sulfate (K_2SO_4).

When an electrode was cycled for many cycles, the capacitance was observed to increase. After subtracting out the capacitance expected from the multi-wall CNTs (MWCNTs) alone, the specific capacitance of the MnO_x NPs was calculated to increase from 8.3 to 31.8 F/g after 1200 cycles. It is believed that this increase is due to the conversion of the MnO_x from its initially synthesized phase, believed to be Mn_3O_4, to the more electrochemically active birnessite phase. It was also seen that the morphology of the MnO_x changed with cycling, as can be seen in the SEM image in figure 41. There may be a potential issue with the MnO_x dissolving during part of the CV cycle and then redepositing later in the cycle. In this case, the capacitance was still increasing, but the significant changes in morphology could be an issue in a practical device.

The cycled electrode was subsequently tested in the three electrolytes in succession. The observed capacitances were 85.7 F/g in K_2SO_4, 97.8 F/g in sodium chloride (NaCl), and 153 F/g in calcium chloride ($CaCl_2$) electrolyte at a 2 mV/s scan rate. In this electrolyte study, a specific capacitance of 84 F/g was obtained at 20 mV/s in $CaCl_2$ electrolyte. This is the combination of the double-layer capacitance of the SWCNTs and rGO combined with the pseudocapacitance of the MnO_x NPs. Extracting the pseudocapacitance of the MnO_x NPs is somewhat difficult and requires some approximations. If one assumes that the GO has a C_7O_3 stoichiometry and the MnAc converts to MnO_2 and that the rGO contributes 50 F/g (based on a similar electrode with no MnO_x) and the SWCNTs contribute 35 F/g (based on previous work), then one can calculate the MnO_x NPs are contributing 108 F/g of pseudocapacitance at 20 mV/s. This is a reasonable result when compared to the literature for MnO_x electrodes (*60*), but is it lower than some reports in the literature for MnO_x/G or CNT electrodes. Since redox reaction based pseudocapacitance is slower than the double-layer capacitance contribution, the measured pseudocapacitance would be higher at slower scan rates.

In future work, the best ratio of MnO_x:G/CNT should be determined. The energy and power requirements of the ultimate application are liable to determine the optimum ratio of materials. In much of the reported MnO_x:G/CNT composite electrode work, the G/CNT is merely an additive that increases the electrical conductivity of the MnO_x. Additional synthesis routes for producing the most electrochemically active MnO_x phase should be investigated. Finally, more electrode fabrication process optimization is required to prevent the electrode deterioration that is

sometimes seen. While incorporation of MnO_x NPs may increase energy density through increased accessible surface area and pseudocapacitive contributions, the NPs may also reduce the power density by reducing the electrode electronic conductivity, and it may reduce the cycle life through the incorporation of redox reactions.

5.3 Inkjet Printed Supercapacitors

Printed, flexible electronics are desirable as they offer the promise of low-cost, readily customizable, and rugged electronics along with volume and weight savings. In order to fully realize these advantages, a flexible power source must be developed. Presently, batteries are the go-to solution for powering most of the Army's portable electronics; however, there are good reasons for considering the use of supercapacitors for some applications. Commercial supercapacitors have electrodes made with activated carbon. Activated carbon has high surface area, which yields high specific capacitances, but it is composed of brittle particles that are not highly conductive. As a result, activated carbon electrodes are made with the addition of binders and conductivity enhancers. Graphene, single-atom-thick graphite sheets, on the other hand, has superior electrical and mechanical properties compared to activated carbon. Graphene is being widely studied for supercapacitor applications due to its high surface area and high electrical conductivity. Graphene is especially attractive for printing flexible supercapacitors as it is a very strong and flexible material, and its oxidized form (aka GO) makes a good inkjet printable ink when dissolved in water. Once the GO is printed onto the substrate, it must be reduced to the conductive graphene form, which is done with a thermal bake.

In collaboration with Prof. Lee of the Stevens Institute of Technology, ARL has demonstrated the first inkjet printing of graphene supercapacitor electrodes onto flexible substrates for making flexible supercapacitors. These flexible supercapacitors will enable printed, flexible munitions initiation circuits being developed by ARDEC. Previously, we reported good capacitor performance with inkjet printed graphene on metal foil current collectors, which were assembled into a prototype device using a Celgard separator and a rigid fluoropolymer clamp, as shown in figure 42a (*61*). The achieved specific capacitance of 132 F/g is similar to that obtained for graphene using other electrode fabrication methods. This demonstrates that inkjet printing is a viable method of electrode fabrication. While it is expected that eventually the metal current collector, graphene active electrode material, and perhaps the electrolyte and separator will all be inkjet printed, in the initial packaged prototype, the metal current collectors were shadow-masked metal films evaporated onto Kapton. In the current work, the next step in printing flexible supercapacitors was undertaken with the printing of graphene electrodes onto flexible metal/Kapton FN substrates, which are composed of fluorinated ethylene propylene (FEP) and polyimide layers. The FEP coating of the Kapton is what allows the Kapton to be heat sealed to seal the electrolyte in. A prototype flexible graphene/Kapton supercapacitor is shown in figure 42b. This prototype yielded lower performance, with specific capacitance of 32.2 F/g, due

to overly resistive current collectors made of Ti evaporated onto bare Kapton. Although low specific capacitance was achieved in the initial device, the observed capacitance was largely maintained during bending of the device through various radii, indicating that flexible devices are possible. A subsequent attempt with evaporated metal is underway while we work on developing printed current collectors. The printed silver attempt initially does not survive electrochemical cycling in the electrolytes tested, so printed Au current collectors are under development. In future work, various considerations for achieving good flexible supercapacitors will be addressed including the thermal budget, heat sealing issues, package permeability, printing alignment, etc.

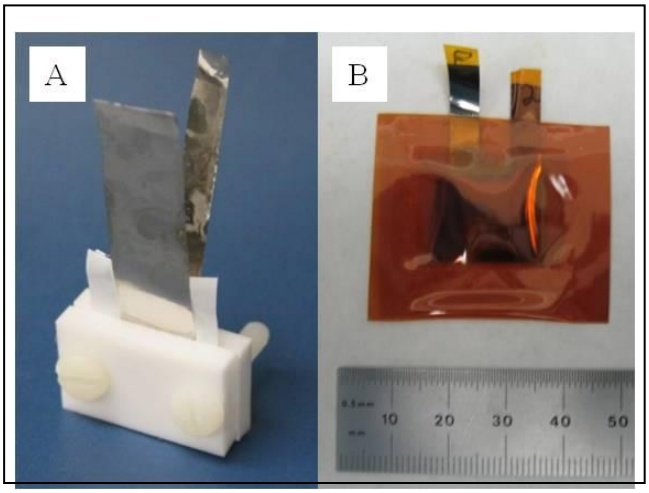

Figure 42. (a) Inkjet printed graphene on metal foil current collectors tested in a rigid clamp and (b) heat sealed device made with inkjet printed graphene on evaporated metal current collectors on Kapton.

5.4 Supercapacitors for Energy Harvesters

Through a collaborative effort between ARL, ARDEC (Carlos Pereira), and JME Inc., graphene-based supercapacitors were successfully demonstrated for munitions energy harvesting (*62*). During gun launch and flight, munitions experience very high setback accelerations and vibrations. It is desirable to convert a small portion of this mechanical energy into usable electrical energy to meet onboard power requirements for precision guidance and fuzing systems. In addition, there is a need to develop munition power supplies that are highly reliable and inherently safe to handle by the Warfighter, which can meet full military operational and storage temperature ranges, and satisfy shelf life requirements of more than 20 years. To meet these criteria, ARDEC is developing a new class of energy harvesters for gun launch and flight environments. The harvested energy is then stored in capacitors. We have collaborated with ARDEC on measuring the efficiency of the conversion and storage of energy for producing usable electrical energy. The resulting usable energy is a function of optimized energy

harvesting and storage. A novel high frequency electrochemical capacitor may be a superior storage solution due to greater capacitance per mass and volume compared to other types of capacitors.

ARL has investigated a unique high-speed supercapacitor developed by an ARL SBIR performer, JME Inc., for addressing the power storage needs of such a system. These supercapacitors have electrodes made using vertical graphene arrays grown directly onto metal current collectors, as shown in figure 43. Supercapacitors made with these electrodes operate at four orders of magnitude higher frequency than traditional supercapacitors (*63*). The high frequency performance of these electrochemical capacitors is enabled by electrodes with better electronic and ionic conductivities due to better contact resistance to the current collector and increased porosity for electrolyte ion transport compared to conventional electrochemical capacitors. In order to demonstrate energy storage, a projectile launch energy harvesting simulator built by Omnitek Partners, LLC (shown in figure 44) was used. The fast supercapacitors were found to store the energy as well as electrolytic capacitors in a projected ~10 times smaller form factor. This makes them viable for energy harvesting applications and especially attractive for applications such as munitions, which have severe space constraints. This was also the first ever, high frequency, high overvoltage demonstration of supercapacitor charging. These fast supercapacitors will be more reliable and have better shelf life than electrolytic capacitors, enabling them to replace electrolytic capacitors for many applications.

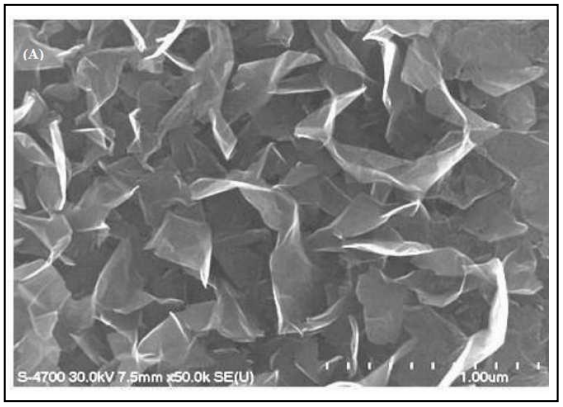

Figure 43. SEM of vertical graphene sheet array electrode.

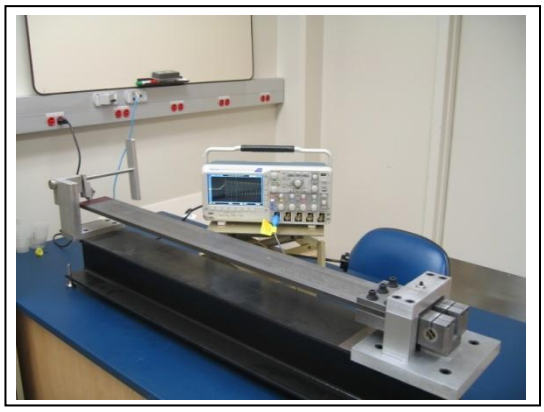

Figure 44. Mechanical simulator of a munition energy harvesting system.

5.5 Conclusion

Supercapacitors have several advantages over conventional batteries. Increasing supercapacitor energy and power densities through the use of graphene will make them useful for many more portable power and power conditioning applications. Adding additional nanomaterials may be a viable route to improving performance through the incorporation of pseudocapacitance. Inkjet technology has great promise for reducing the weight and volume carried by a Soldier or other system requiring energy storage while also enabling flexible and conformal form factors for flexible electronics applications. Our SBIR partner JME, Inc., has demonstrated high frequency performance, opening up many new applications for supercapacitors. While supercapacitors may find niche applications where they can be the sole power source, in most applications, they will be part of a hybrid system providing load leveling to a battery, fuel cell, energy harvester, or other energy source. In this way, the supercapacitor will enhance the performance of the battery or other power source. In addition, there will also be important supercapacitor improvements due to the mechanical properties of CNTs/graphene. For instance, CNTs and graphene lend themselves to flexible, conformal, or integrated supercapacitors that would be useful for applications where there is little available space.

5.6 Transition

ARL developed supercapacitor technology will enable size and weight savings for munition electronic systems. They will also yield improvements in reliability and shelf life over electrolytic capacitors. Collaborations with ARDEC on using inkjet printed and high frequency supercapacitors for munitions power systems will help these technologies transition to systems that benefit the Soldier. A recognition of the potential of the inkjet printing approach was received in the form of a joint paper “Inkjet Printed Graphene for Energy Storage” being awarded the R&D Award at the Printed Electronics 2012 Conference, Santa Clara CA, 1 December 2011.

The demonstration of 15-kHz supercapacitors by our phase II SBIR partner, JME, Inc., is an important milestone as it will allow supercapacitors to compete for applications previously reserved for dielectric or electrolytic capacitors. These results are so promising that the largest U.S. electrolytic capacitor manufacturer has joined the Phase II SBIR effort, expressing their interest in commercializing this technology by donating most of their program support. Their participation will be a great asset in pushing this technology forward to commercialization and deployment.

6. Conclusions

The following tasks were accomplished:

- Successful growth graphene of single, bi-, and multiple layers using low and atmospheric pressure CVD systems.
- Developed transfer process for graphene onto device-quality substrates.
- Developed process for ALD for dielectrics and metallic atomically smooth layers.
- Modeled, designed, and fabricated graphene FETs.
- Established a novel infrastructure for testing and evaluation of graphene transistors and electronics.
- Tested graphene devices for RF performance up to 3 GHz.
- Demonstrated Inkjet printed flexible supercapacitors.
- High frequency supercapacitors have the potential to replace electrolytic capacitors for many applications.

7 Transitions

We developed a Technology Program Annex (TPA) with CERDEC and started two SBIRs on the technology of graphene supercapacitors. Discussion is in progress with ARDEC for energy harvesting and Defense Advanced Threat Reduction Agency (DATRA) on sensor applications.

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List of Symbols, Abbreviations, and Acronyms

0-D	zero-dimensional
1-D	one-dimensional
2-D	two-dimensional
3-D	three-dimensional
3LG	trilayer graphene
4LG	tetralayer graphene
AFM	atomic force microscopy
Al	aluminum
Al_2O_3	aluminum oxide
ALC	Adelphi Laboratory Center
ALD	atomic layer deposition
APCVD	atmospheric pressure chemical vapor deposition
Ar	argon
ARDEC	Armament Research, Development and Engineering Center
ARL	U.S. Army Research Laboratory
ARO	Army Research Office
Au	gold
BLG	bilayer graphene
$CaCl_2$	calcium chloride
CCD	charge-coupled device
CERDEC	U.S. Army Communications-Electronics Research, Development and Engineering Center
CH_4	methane
CMOS	complementary metal-oxide-semiconductor

CNT	carbon nanotube
Cr	chromium
CRM	confocal Raman microscope
CV	cyclic voltammetry
C-V	capacitance-voltage
Cu	copper
CVD	chemical vapor deposition
DARPA	Defense Advanced Research Projects Agency
DATRA	Defense Advanced Threat Reduction Agency
DSI	Director's Strategic Initiative
e-textiles	electronic textiles
EBL	e-beam lithography
EDX	emergy-dispersive x-ray spectroscopy
EIS	electrochemical impedance spectroscopy
f.c.c.	face-centered-cubic
FEP	fluorinated ethylene propylene
FET	field-effect transistor
F/g	Farads per gram
FWHM	full-width- half-maximum
G	graphene
GFET	graphene field-effect transistor
GO	graphene oxide
H_2	hydrogen, the diatomic molecule
hBN	hexagonal boron nitride
HEMT	high electron mobility transistor
HRTEM	high resolution TEM

I-V	current versus voltage
LPCVD	low pressure chemical vapor deposition
K_2SO_4	potassium sulfate
ME	mechanical exfoliation
MFC	mass flow controller
MIG	metal-insulator-graphene
MIGIM	metal-insulator-graphene-insulator-metal
MIGCAPs	metal/insulator/graphene capacitors
MIT	Massachusetts Institute of Technology
MnAc	manganese acetate
MnOx	manganese oxide
MWCNT	multi-wall CNT
NaCl	sodium chloride
Nd	neodymium
Ni	nickel
NP	nanoparticle
O_2	oxygen
PET	polyethylene terephthalate
PMMA	poly(methyl methacrylate)
R&D	research and development
RF	radio frequency
rGO	reduced graphene oxide
RS	Raman spectroscopy
SEM	scanning electron microscopy/graph
Si	silicon
SiC	silicon carbide

SiO_2	silicon dioxide
SLG	single-layer graphene
SWCNTs	single-wall CNTs
Ti	titanium
TEM	transmission electron microscopy
TLM	transmission line model
TPA	Technology Program Annex
XRD	x-ray diffraction
YAG	yttrium aluminum garnet

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1	U.S. ARMY NATICK SOLDIER RESEARCH DEVELOPMENT AND ENGINEERING CENTER NANOMATERIALS SCIENCE TEAM ATTN AMSRD NSR WS B NS R OSGOOD 15 KANSAS ST BLDG 110 NATICK MA 01760
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