NAVAL POSTGRADUATE SCHOOL

MONTEREY, CALIFORNIA

THESIS

TRAP CHARACTERIZATION IN HIGH FIELD, HIGH TEMPERATURE STRESSED GALLIUM NITRIDE HIGH ELECTRON MOBILITY TRANSISTORS

by

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March 2013

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REPORT DOCUMENTATION PAGE			Form Approved OMB No. 0704-0188

1. AGENCY USE ONLY *(Leave blank)*	2. REPORT DATE March 2013	3. REPORT TYPE AND DATES COVERED Master's Thesis

4. TITLE AND SUBTITLE TRAP CHARACTERIZATION IN HIGH FIELD, HIGH TEMPERATURE STRESSED GALLIUM NITRIDE HIGH ELECTRON MOBILITY TRANSISTORS	5. FUNDING NUMBERS
6. AUTHOR(S) Kevin B. Pham	
7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES) Naval Postgraduate School Monterey, CA 93943-5000	8. PERFORMING ORGANIZATION REPORT NUMBER
9. SPONSORING /MONITORING AGENCY NAME(S) AND ADDRESS(ES) N/A	10. SPONSORING/MONITORING AGENCY REPORT NUMBER

11. SUPPLEMENTARY NOTES The views expressed in this thesis are those of the author and do not reflect the official policy or position of the Department of Defense or the U.S. Government. IRB Protocol number ___N/A_____.

12a. DISTRIBUTION / AVAILABILITY STATEMENT Approved for public release; distribution is unlimited	12b. DISTRIBUTION CODE A

13. ABSTRACT (maximum 200 words)

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14. SUBJECT TERMS Capacitance-Voltage, Interface Trap Density, Gallium Nitride, GaN, High electron mobility transistors	15. NUMBER OF PAGES 71
	16. PRICE CODE

17. SECURITY CLASSIFICATION OF REPORT	18. SECURITY CLASSIFICATION OF THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
Unclassified	Unclassified	Unclassified	UU

NSN 7540-01-280-5500 Standard Form 298 (Rev. 2-89)
Prescribed by ANSI Std. 239-18

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TRAP CHARACTERIZATION IN HIGH FIELD, HIGH TEMPERATURE STRESSED GALLIUM NITRIDE HIGH ELECTRON MOBILITY TRANSISTORS

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Submitted in partial fulfillment of the
requirements for the degree of

MASTER OF SCIENCE IN ELECTRICAL ENGINEERING

from the

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ABSTRACT

Gallium Nitride (GaN) high electron mobility transistors (HEMTs) offer higher power output over existing technology. However, issues such as current collapse and kink effect hinder GaN HEMTs performance. The degraded performance is linked to traps within the device. Capacitance-voltage (C-V) and current-voltage (I-V) measurements were performed on commercially available GaN-on-Si to characterize traps before and after high field, high temperature stressed conditions. The results revealed the devices had less gate current leakage after stressing and the C-V characteristics changed dramatically after a 24 hour recovery period.

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LIST OF ACRONYMS AND ABBREVIATIONS

GaN	Gallium Nitride
Si	Silicon
GaAs	Gallium Arsenide
HEMT	High Electron Mobility Transistor
I-V	Current-Voltage
C-V	Capacitance-Voltage
RF	Radio Frequency
2DEG	Two-Dimensional Electron Gas
D_{it}	Interface Trap Density
I_{ds}	Drain-Source Current
I_{gs}	Gate-Source Current
V_g	Gate Voltage

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EXECUTIVE SUMMARY

Silicon (Si) based solid state power amplifiers and traveling wave tubes amplifiers (TWTAs) have dominated RADAR and satellite communications applications. Of the two amplifier options, TWTAs offer higher power output compared to Si-based solid state power amplifiers; however, the vacuum enclosure abates the reliability of TWTAs compared to solid state power amplifiers.

Gallium Nitride (GaN) high electron mobility transistors (HEMTs) technology has shown improvement over the last few years and is on the verge of replacing TWTAs and Si-based solid state power amplifiers. GaN HEMT solid state power amplifiers maintain the reliability of solid state power amplifiers with four to five times greater power density compared to Si-based power amplifiers. The wide band gap of GaN HEMTs allows for the device to operate in a high voltage and temperature environment. However, due to the operational environment and the early stages of GaN HEMT technology, the reliability of the GaN-on-Si HEMTs needs to be further investigated.

The purpose of this thesis was to investigate and characterize unstressed and stressed GaN-on-Si HEMTs through capacitance-voltage (C-V) measurements and current-voltage (I-V) measurements. The devices underwent a ramp stress test that held the devices in reverse bias for 200 s with a 200 s recovery period. The voltage ranged from 0 V to -50 V in -1 V steps. The C-V measurements allowed for the calculation of interface trap densities D_{it}. The C-V measurements were recorded prior to stressing, after

stressing and after a day of recovery to characterize the interface trap densities during those periods and its relative location within the band energy. During the stressing period, the drain and gate currents were monitored to track the trapping and detrapping transients and monitor for the critical voltage where the device breaks down. The threshold voltage for the device was monitored between stressing and recovery to determine if the shifts in threshold voltage had a dependency on time, voltage, or temperature.

The devices under test (DUT) were commercially available GaN-on-Si HEMT dies manufactured by Nitronex. GaN-on-Si HEMTs have gained interest over competing materials such as GaN-on-Silicon Carbide (SiC) due to the fact that the GaN-on-Si are significantly cheaper to produce.

Results from the experiment showed that these devices do not behave in the manner seen in prior work. The DUT had less gate leakage after stressing. The activation energies for these devices showed voltage dependence. The capacitance of the device drastically changed after recovering for a day. The information extracted from this research will help further understand AlGaN/GaN-on-Si HEMT degradation and improve device simulation and device manufacturing.

ACKNOWLEDGMENTS

Ad astra per aspera

I like to thank my family for the love and support during these difficult times. They inspired me to better myself every day.

To my friends who dealt with me during some of my most stressful moments. They offered solace when I needed it the most.

My advisor, Dr. Todd Weatherford, thank you for keeping your doors open.

Last, but not least, I truly would like to thank my roommate and friend Matthew Porter. Thank you for the support.

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I. INTRODUCTION

Wide band gap semiconductors offer multiple advantages over conventional semiconductor transistors and are considered to be hopeful contenders for next generation power electronics applications such as microwave power amplifiers, high-voltage switches, and microwave transmitters for communications and RADAR systems. The most promising wide band gap semiconductor is Gallium Nitride (GaN). GaN high electron mobility transistors (HEMTs) have garnered an abundant amount of research due to their unique semiconductor properties that are superior to competing semiconductor materials. GaN HEMTs can operate in high voltage and temperature, have a higher output power density, and have high input impedance.

Even though research has proven that GaN HEMTs offer great possibilities for radio frequency (RF) communications, there is still a need for a well-defined physics of failure, stressor(s), and fail metric(s) to provide an accurate estimate for GaN HEMTs long term reliability. A major driver of GaN HEMT degradation is material defects which present as charge carrier trapping states. Carrier trapping states are more apparent with GaN-on-Silicon (GaN-on-Si) devices. These states have been found to vary in energy, spatial location within the device, and concentration. The specific type of stress applied drives generation of these states. It has been found that a major driver of trap state generation is high electric fields in the device [1]. However, the identity and physical mechanisms driving generation of these traps

remain poorly understood. Charge carriers within these states exhibit lifetimes ranging from microseconds to days, inducing changes in device characteristics which are not normally quantified in an unstressed device.

The purpose of this research is to characterize degradation in commercially fabricated GaN HEMTs through the quantification of the effects of trap states which originate during strenuous device operation. The work outlined in this research uses novel charge characterization through capacitance–voltage (C–V) measurements, along with traditional device characterization through current-voltage (I–V) terminal measurements, to characterize the evolution of charge carrier trapping after high field stressing. Simulation of the device structure through the Silvaco ATLAS™ device physics suite is used to correlate data to various spatial and energetic distributions of trap states to examine various hypotheses regarding the underlying physics of trap state generation due to high field stress in GaN HEMTs.

A. IMPORTANCE TO DEPARTMENT OF DEFENSE

In general, the power amplifiers installed in RADAR and satellite communications systems have been either traveling wave tube amplifiers (TWTAs) or solid state power amplifiers (SSPAs). While TWTAs offer higher output power compared to SSPAs [2], high-voltage thermionic, life-limited emitters operating in a high vacuum enclosure abates the reliability of TWTAs [3] and the requirement for TWTAs to "warm-up." GaN HEMTs based SSPAs can fire up instantly and have the potential to operate at 200 C continuously without failure up to 1 million hours as

compared to the typical lifetime of TWTAs of 100,000 hours. Compared to current SSPAs designs using GaAs or Si, GaN HEMTs-based SSPAs offer equal power-added efficiency (PAE) but at four to five times greater power density [4]. The Department of Defense (DoD) wishes to replace aging TWTAs with more cost-efficient SSPAs and have invested approximately $800M with several defense research offices - the Defense Advanced Research Projects (DARPA), Army Research Laboratory (ARL), Air Force Research Laboratory (AFRL), Office of Naval Research and Naval Research – and a plethora of universities across the United States to the development and maturation of GaN HEMTs [5].

One specific program, the wide band gap semiconductors for radio frequency application (WBGS-RF), is a three phase program supported by DARPA being conducted to advance Gallium Nitride-on-Silicon Carbide (GaN-on-SiC). The goals for the program were to be able to manufacture reliable GaN-on-SiC based devices and monolithic microwave integrated circuits (MMIC) with high yield that could operate at frequencies ranging from 3 to 40 GHz with a mean time-to-failure (MTTF) over 100,000 hours at high RF output power [6]. AFRL, NRL and ARL are collaborating with contractors to independently evaluate the reliability and performance of devices on wafers.

The first phase of the program focused on the material improvement of the SiC substrate. The initial phase resulted in an increase availability of a SiC substrate that provides sufficient thermal conductive substrate that makes development for GaN HEMTs feasible. In the second phase of the program, X-band, wideband, and Q-band

transistors were developed and tested by three teams: Raytheon/Cree, Triquint, and Northrop Grumman. The primary focus of the development was to improve process control and uniformity in order to improve reliability and prolong the life of GaN HEMT with a high power output while remaining efficient. All RF performance goals were met, and some exceeded, that which have been achieved previously with stable devices. Lifetime for the parts developed was increased by a factor of 10^5 [6]. A PAE of 62% was achieved for frequencies ranging from 8 to 12 GHz. The benefit of the second phase of the WBGS-RF program was to improve the manufacturing of the GaN HEMTs by identifying factors that lead to degradation, allowing them to be eliminated. The third phase is similar to phase II; however, the goal is to improve MMIC reliability with high output power.

The WBGS-RF project has proven the potential that GaN HEMTs devices can provide; however, there is room for improvement. Defects such as traps and trap locations within GaN HEMTs hinder the performance of GaN HEMTs.

B. RESEARCH OBJECTIVE

The goal of this research is to continue to investigate the physical degradation of GaN-on-Si HEMTs. GaN-on-Si is a cheaper alternative to GaN-on-SiC that will lead to savings of cost per part in terms of redundancy and replacement. Prior work recorded I-V DC characteristics and recorded the presence of traps in the devices. Further characteristics of GaN-on-Si die device traps are investigated in this thesis in two parts: C-V measurements are performed with devices both unstressed and post-stressed. Then a model is developed to correlate with the

recorded data to give further understanding of GaN-on-Si device characteristics to improve reliability and performance.

C. PRIOR WORK AT NPS

More than a decade of research on GaN HEMT reliability has been carried out at NPS. Prior research conducted at NPS has focused upon modeling and simulation of GaN HEMTs to explore the device characteristics to improve reliability. Initial research on GaN HEMT reliability was conducted in 2001 utilizing the Silvaco Software Suite [7]. The focus was to develop a model based on the fundamental principles that incorporate piezoelectric strain on GaN HEMTs. Follow-up research continued in 2002 that developed a model based on devices tested by NRL [8].

In 2005, research began to design and model GaN HEMTs on various substrates to address the issue of self-heating to further improve reliability. The use of sapphire and diamond as a substrate to improve thermal characteristics was investigated. The investigation revealed an increase in power density and lower channel temperatures. The modeled utilized the Albrecht low-field mobility model to realistically model channel mobility, thus, improving accuracy and further validating the Silvaco ATLAS™ suite as a semiconductor physics simulator and ushering in more simulation and modeling research [9] [10] [11].

Research into the thermal characteristics of GaN HEMTs, specifically, thermal heating, continued in 2007 [12]. Utilizing the newly developed thermal simulation model from Silvaco, Giga, a two-dimensional and a three-dimensional model were created based on a device provided

by AFRL, SP3, and Nitronex. The model simulated GaN HEMTs on diamond substrates and sapphire substrates at various temperature gradients to obtain DC characteristics. From the research, it was shown that diamond substrates offer better thermal management compared to sapphire and have better reliability and performance. The follow up project, started in 2008, modeled GaN HEMTs to match the DC characteristics of GaN HEMTs created by AFRL [13]. GaN HEMTs created by AFRL have a number of device fingers, so the model was modified accordingly. The thermal effects when operating in high frequency transient conditions were investigated and found intra-device heating inherent to transient operation.

Further efforts were focused on the piezoelectric effect on GaN HEMTs. The degradation of GaN HEMTs was investigated. It had been theorized that, over time, a fissure forms at the edge of the gate of a GaN HEMT which causes a pathway for electrons to travel up from the substrate. This degradation was simulated and the cause was theorized as due to the high electric field strain induced by the piezoelectric and pyromechanical effects coupling at high frequency operations [14].

The most recent research was an investigation of the physical degradation of GaN-on-Si-based HEMTs. GaN-on-Si offers a cheaper alternative to GaN HEMTs compared to GaN-on-SiC; however, little reliability testing has been performed on GaN-on-Si. DC tests were performed on commercially available GaN-on-Si HEMT devices under two conditions: the device under normal operations and post-stress. The results showed some devices exhibit higher

current outputs post-stress when compared to pre-stressed devices [14]. The work performed matched the predictions from prior works.

D. THESIS OUTLINE

This thesis is organized into four chapters. The background information on GaN HEMTs such as material properties and physical characteristics is discussed in Chapter II. Device characterization methods and theory are also included in Chapter II. The design of the experiment for this research is explained in Chapter III and the measurement set up is covered. All experimental results are included in Chapter IV. The evaluation of data obtained during the research, conclusions, and recommendations for future work are contained in Chapter V.

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II. BACKGROUND

A. ALGAN/GAN HEMT FUNDAMENTALS

An Aluminum Gallium Nitride (AlGaN)-GaN heterostructure is formed from a complex interaction of piezoelectric polarization strained between epitaxially grown materials from the III-V Nitride family. The bond and crystalline structure of GaN also produce a spontaneous polarization. The piezoelectric polarization and the spontaneous polarization can aid or oppose each other depending on the strain induced. When AlGaN is grown on GaN, the tensile strain produces a net positive charge at the interface.

The larger energy gap of AlGaN compared to GaN causes a small triangular region in the conduction band that forms at the interface. This region is known as the potential well. The positive net charge produced by the net polarization attracts electrons into the well where they are confined. This concentration of electrons is referred to as a two-dimensional electron gas (2DEG). The confinement of the electrons in the 2DEG reduces scattering and increases electron mobility. Depicted in Figure 1 is the band diagram of an AlGaN/GaN heterostructure and polarization.

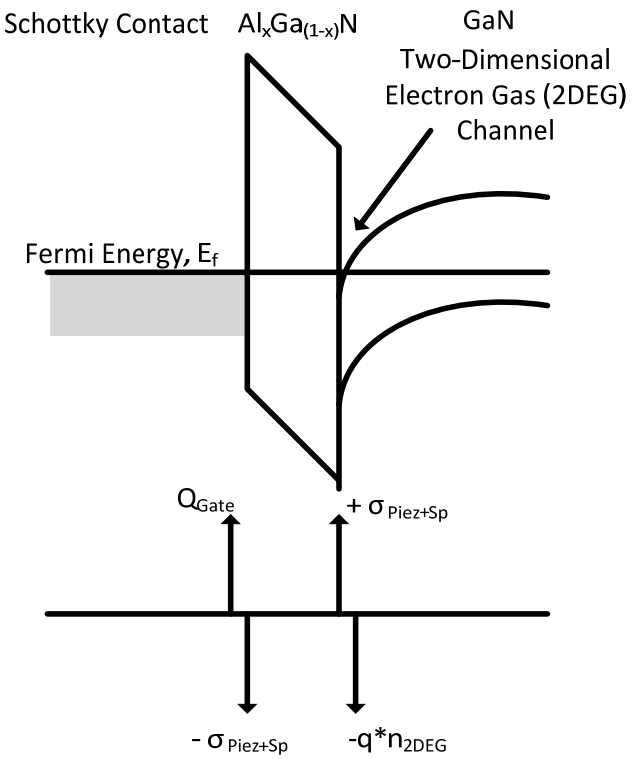

Figure 1. Band diagram of AlGaN/GaN HEMT and interface polarization.

B. TRAPS

Defects occur either when foreign atoms are unintentionally introduced into the substrate during doping or when a crystalline defect occurs during the growth process. The results from these defects perturb the crystalline structure of the semiconductor, which creates discrete energy levels within the band gap. These discrete energy levels are called traps.

Traps act like generation and recombination centers in the semiconductor. Four possible events can occur between the conduction band E_c, trap energy level E_T, and valance band E_V. The first interaction is the capture of an electron e from the E_c to E_T level as shown in Figure 2(a). The electron at E_T can be either be emitted back to the E_c as

seen in Figure 2(b) or it can capture a hole p from E_v as seen in Figure 2(c). The captured hole can then either be emitted back to E_v or capture an electron.

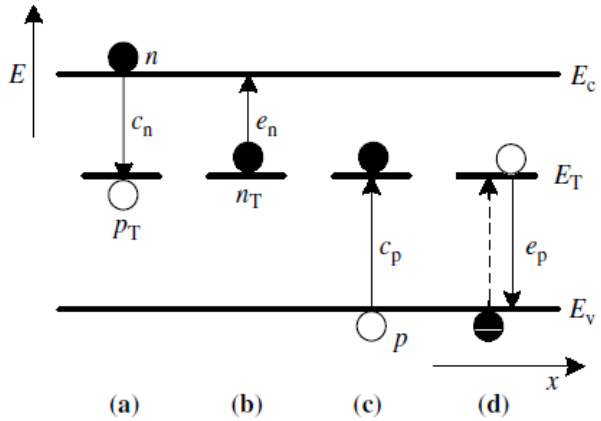

Figure 2. The band diagram of a semiconductor containing deep level impurities and various states of carrier generation and recombination. From [15].

The types of traps associated within a semiconductor device are interface trapped charge, fixed oxide charge, trapped charge, and mobile charge. Interface trapped charges can be positive or negative charges and occur due to structural defects. Fixed oxide charges are due to charges at the interface of the channel and insulator. Trapped charge is either positive or negative charge caused by holes or electrons, respectively, trapped in the material. Mobile charge is caused by ionic impurities. Possible trapping locations in AlGaN/GaN-on-SiC HEMT are depicted in Figure 3.

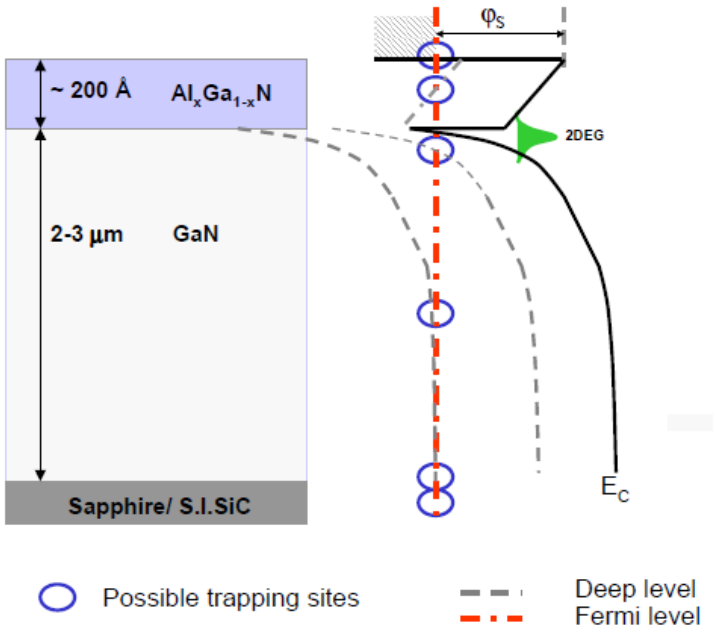

Figure 3. Possible trapping sites in AlGaN/GaN –on-Sapphire. After [16].

Trapping becomes a major issue that limits GaN HEMTs performance. A trap-related phenomenon in GaN HEMT devices is current collapse which limits the output power of the device, a critical parameter for satellite communications [16]. Hot carriers are trapped outside the conduction band. This results in a depletion layer, leading to lower drain current characteristics. Another phenomenon that occurs is the kink voltage effect. This is due to electron trapping and field-assisted de-trapping from donor-like traps in the GaN buffer layer [17]. The effect is an increase of output-conductance, transconductance compression, and dispersion between DC and RF characteristics [19].

C. DEPLETION REGION

The foundations of semiconductor physics are p-n junctions. In this and later sections, p-n junctions are

discussed with respect to the depletion width and its relationship to capacitance and voltage.

A p-n junction is the junction of two separate types of semiconductor materials: a p-type material and n-type material. Both materials can be described as having a majority of one type of carriers and a minority of the other type. Both substrates can be characterized as having majority carriers and minority carriers. For p-type substrates, holes are the majority carrier, and electrons are the minority carrier. It is vice versa for n-type substrates. When these two materials are combined to form one continuous material, the holes from the p-type material diffuse into the n-type region, leaving behind negatively ionized donors N_d, and electrons from the N-type material diffuse into the P-type material leaving behind positively ionized acceptors N_a. This forms an abrupt junction. The region composed of the ionized donors and acceptors is called the depletion region W.

The diffusion of the holes and electrons create diffusive currents, and the ionized acceptors and donors set up an electric field that induces a drift current opposite to that of the diffusive currents. The negation of the diffusive current and the drift current cancels the total hole and electron density currents. In this condition, the Fermi level is constant throughout the material.

The dipole region around the junction must have equal charges on both sides; that is, in the depletion region the total positive ionized donors must equal the total negative ionized acceptors per unit area; i.e.,

$$N_A W_p = N_D W_n \tag{1}$$

where W_p and W_n are the depletion width in the p-type material and n-type material, respectively. The depletion regions W_p, W_n, and the total depletion region W are depicted in Figure 4.

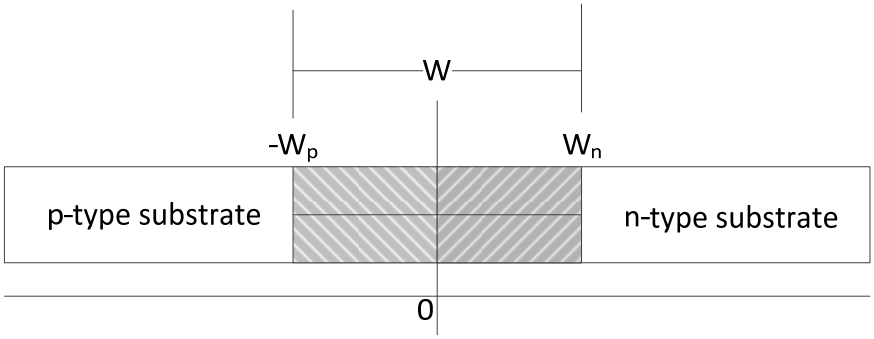

Figure 4. The depletion region within p-type substrate W_p, n-type substrate W_n, and total depletion region W.

The gradient of the electric field is related to the local space charge depletion region with Poisson's equation:

$$-\frac{d^2\psi_i}{dx^2} = \frac{dE_{field}(x)}{dx} = \frac{q}{\varepsilon_s}\left[N_D^+(x) - n(x) - N_A^- + p(x)\right] \tag{2}$$

where ψ_i is the potential distribution, E_{field} is the electric field, q is the charge of an electron, x is any point within the depletion region, $n(x)$ is the total electrons at point x, $p(x)$ is the total holes at point x, and ε_s is the dielectric constant of the substrate. Under the assumption that there are no holes or electrons within the depletion region and only ionized donor and acceptors, (2) can be simplified as

$$\frac{d^2\psi_i}{dx^2} \approx \frac{qN_A}{\varepsilon_s} \text{ for } -W_p \le x \le 0 \tag{3}$$

and

$$\frac{d^2\psi_i}{dx^2} \approx \frac{qN_D}{\varepsilon_s} \text{ for } 0 \le x \le W_n \text{ .} \tag{4}$$

Integrating (3) and (4), we obtain the built-in potential ψ_i for the regions in the p-type substrate and n-type substrate, respectively

$$\psi_i(x) = \frac{qN_A}{2\varepsilon_s}(x + W_p)^2 \text{ for } -W_p \le x \le 0 \tag{5}$$

and

$$\psi_i(x) = \psi_i(0) + \frac{qN_D}{\varepsilon_s}(W_n - \frac{x}{2})x \text{ for } 0 \le x \le W_n \text{ .} \tag{6}$$

The bulk built-in potential ψ_{bi} is the built-in potential from $-W_p$ to W_n; therefore, combining (5) and (6) we get

$$\psi_{bi} = \frac{qN_A W_p^2}{2\varepsilon_s} + \frac{qN_D W_n^2}{2\varepsilon_s} = \frac{|E_m|}{2}(W_p + W_n) \tag{7}$$

where E_m is the maximum electric field intensity. From Figure 4, the total depletion width is the joint depletion regions within the p-type substrate and n-type substrate; therefore,

$$W = W_p + W_n = \sqrt{\frac{2\varepsilon_s \psi_{bi}}{qN}} \tag{8}$$

where N is N_D or N_A depending on the doping concentration on the lightly doped side. If a voltage V is applied to the material, (8) can be modified to account for the potential across the junction

$$W = \sqrt{\frac{2\varepsilon_s}{qN}\left((\psi_{bi} - V) - \frac{2k_b T}{q}\right)} \tag{9}$$

where k_b is Boltzmann's constant and T is temperature in Kelvin. A correction factor of $2kT/q$ is needed to

account for majority carrier distribution tails for both p-type and n-type substrates. When a positive voltage bias is applied, the depletion width decreases; when a negative voltage bias is applied, the depletion width increases.

D. DEPLETION REGION CAPACITANCE

The depletion region that forms at the p-n junction can be considered the dielectric of a parallel capacitor where the plates are the neutral regions. The p-n junction can be related to parallel capacitances as

$$C = \frac{dQ}{dV} = \frac{\varepsilon_s}{W} = \sqrt{\frac{q\varepsilon_s N}{2}}\left(\psi_{bi} - V - \frac{2k_b T}{q}\right)^{-1/2} \tag{10}$$

where Q is the stored charge. As voltage increases, charge in the depletion region Q increases. From (10), the capacitance of the p-n junction is a function of the depletion width, which is a function of voltage. Applying a positive bias, we see that the capacitance increases and vice versa with negative bias applied.

A HEMT is a variant of a metal semiconductor field-effect transistor (MESFET); however, there is a wide band gap semiconductor between the channel and gate for a HEMT. The depletion width and depletion capacitance for a metal-semiconductor contact can be calculated from

$$W = \sqrt{\frac{2\varepsilon_s}{qN}\left(\psi_{bi} - V - \frac{kT}{q}\right)} \tag{11}$$

and

$$C = \frac{\varepsilon_s}{W} = \sqrt{\frac{q\varepsilon_s N}{2\left[\psi_{bi} - V - \left(kT/q\right)\right]}}\,, \tag{12}$$

respectively, utilizing the same assumptions to calculate the depletion width for p-n junction with an additional

boundary condition added to the Poisson's equation to account for the metal.

E. CAPACITANCE-VOLTAGE MEASUREMENT

Traps can be quantified by various testing procedure. A known method for traps characterization for semiconductors is capacitance-voltage measurements. The capacitance model for GaN HEMT is not the same for a MOSFET; however, the same principles can be applied to extract the interfacial trap densities.

The general capacitance definition of a metal-oxide-semiconductor (MOS) capacitor is defined as

$$C = \frac{C_{ox}(C_p + C_b + C_n + C_{it})}{C_{ox} + C_p + C_b + C_n + C_{it}} \tag{13}$$

where C_{ox} is the oxide capacitance which occurs at zero bias, C_P is the capacitance due to hole carriers, C_b is the bulk capacitance, C_n is capacitance due to electron carriers, C_{it} is the capacitance due to interface traps.

Depicted in Figure 5 are the capacitances for a MOS capacitor on a p-substrate at various bias regimes. All capacitances inherent to a MOSFET are depicted in Figure 5(a). In accumulation, the total capacitance is largely due to C_{ox} as depicted in Figure 5(b). In depletion the total capacitance is the sum of C_{ox} with C_b and C_{it} in series as seen in Figure 5(c). For inversion the capacitance is dependent on the frequency the AC signal. For low frequency, approximately 1-10 kHz [14], the equivalent capacitance is C_{ox} as shown in Figure 5.

At high frequencies ranging from 15 kHz to 1 MHz, the capacitance is the series capacitance of C_{ox} and C_b as shown in Figure 5(e) [14].

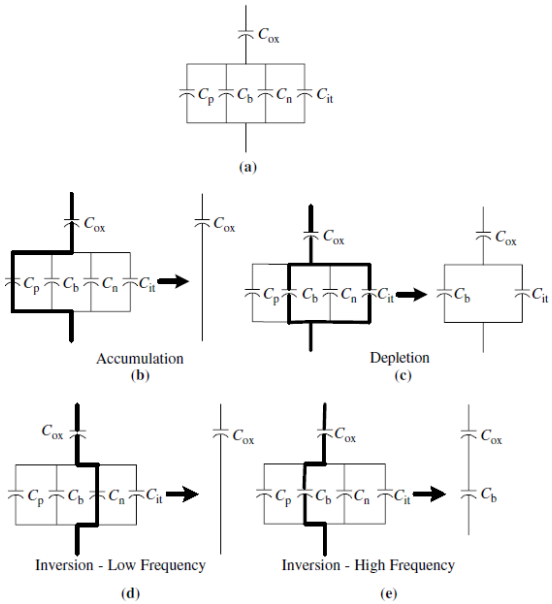

Figure 5. Capacitance of an MOS capacitor at various bias regimes and frequencies. From [15].

Castagne and Vapaille proposed a method to extract interface trapped charge density that utilizes both the low frequency and high frequency C-V measurements for MOSFETs [19]. The method exploits the interface traps' ability to respond to low frequency signals but not to high frequency signals; therefore, D_{it} can be quantified through measured low frequency capacitance C_{lf} and high frequency capacitance C_{hf} to yield

$$D_{it} = \frac{C_{ox}}{q^2}\left(\frac{C_{lf}/C_{ox}}{1-C_{lf}/C_{ox}} - \frac{C_{hf}/C_{ox}}{1-C_{hf}/C_{ox}}\right). \quad (14)$$

The value for C_{lf} is extracted from the minimum point as shown in Figure 6, and the value for C_{hf} is the capacitance at the equivalent point. This method for characterizing trap density for MOS structure can be used for AlGaN/GaN HEMTs [14].

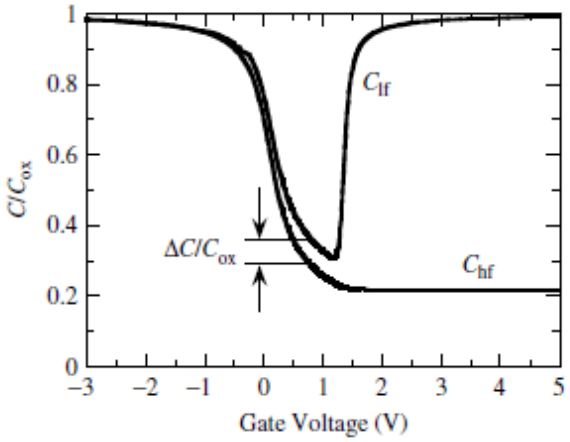

Figure 6. Low and high C-V curves showing the offset of $\Delta C/C_{ox}$ due to interface traps. After [14].

F. PRIOR RESEARCH

In 2006, frequency dependent C-V measurements were conducted by W. L. Liu et al. at the Nano-Device Laboratory at University of California Riverside and at the Device Research Laboratory at University of California Los Angeles [22]. The purpose of this research was to profile traps on AlGaN/GaN on SiC Schottky diodes and heterostructure field effect transistors (HFETs). The devices under test were an $Al_{0.2}Ga_{0.8}N$/GaN heterostructure grown on SiC substrate. The structure of the device had a thin Aluminum Nitride (AlN) nucleation layer followed with a 1.2 µm undoped GaN, 50 nm GaN channel, 3 nm undoped $Al_{0.2}Ga_{0.8}N$ spacer and 15 nm Si doped $Al_{0.2}Ga_{0.8}N$ barrier layers that produced a V_T of -3.8 V.

Liu et al. performed C-V profiling measurements on the large Schottky diode and the AlGaN/GaN HFETs at various frequencies to identify the interface traps near the channel and surface traps across region between the gate and drain.

The frequency dependent C-V measurements on the AlGaN/GaN-on-SiC Schottky diode at 50 kHz and 1 MHz are shown in Figure 7. The results were compared to a one dimensional Poisson-Schrodinger model with the same parameters of the fabricated device. The largest dispersion occurred before threshold. The shape of the dispersion and the bias potential suggested that traps were possibly located in the barrier layer near the AlGaN/GaN interface or in the 2DEG channel [22].

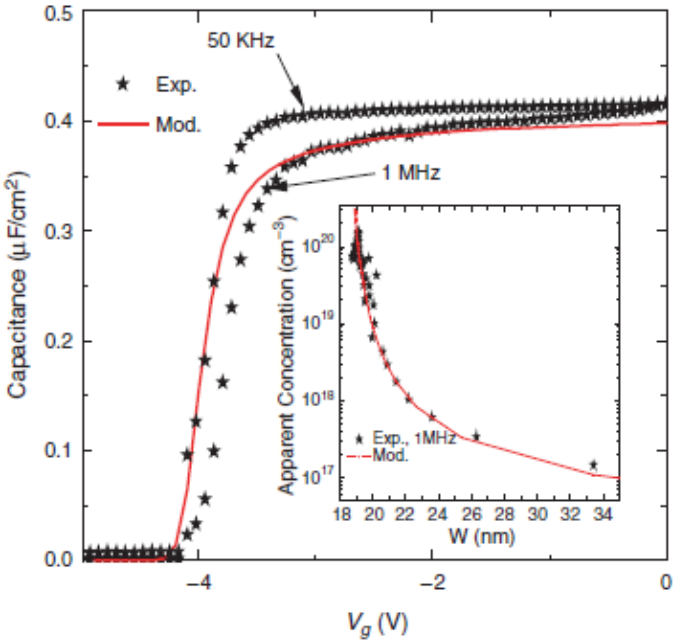

Figure 7. 50 kHz and 1 MHz C-V measurements (points) compared to simulated results (line). From [22].

Liu et al. estimated the trap density and carrier lifetime using

$$D_{it} = \frac{C_{AlGaN}}{q}\left(\frac{C_{it}/C_{AlGaN}}{1-C_{lf}/C_{AlGaN}} - \frac{C_{hf}/C_{AlGaN}}{1-C_{hf}/C_{AlGaN}}\right) \quad (15)$$

where C_{AlGaN} is the capacitance of the AlGaN barrier, f is the frequency, and τ is carrier lifetime. Extracting C_{lf}, C_{hf}, and C_b from plots, Liu et al. identified a trap density to be approximately 10^{11} $cm^{-2}eV^{-1}$ to 5 times 10^{12} $cm^{-2}eV^{-1}$.

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III. EXPERIMENTAL SETUP

A. EXPERIMENTAL SETUP

1. DC Source and Stress Source/Monitor:

The Agilent B1500A equipment was utilized to monitor the current as the gate voltage is being swept. The B1500A is considered a one box solution to DC/AC parametric measurements with software equipped to run and display results for predefined tests or user-defined tests [23]. The B1500A is capable of providing 200 V DC voltage and 1 A DC current output, DC voltage/current measurement capability, and AC signal output and impedance measurement [23]. The current setup for the B1500A contains a high power source/monitor unit (HPSMU) module, a medium power source/monitor unit (MPSMU) module, and a high resolution source monitor unit (HRSMU) module. The SMU module uses two triaxial connectors for force and sense connections and for Kelvin measurements. The B1500A is also equipped with a ground unit (GNDU) to provide a common ground reference for high resolution measurements.

2. QuadTech 7600

The QuadTech 7600 meter was used to perform the C-V measurements. The 7600 has three measurement speeds: slow, medium, and fast. The QuadTech 7600 is capable of measuring inductance, resistance and capacitance (LRC). Accuracy depends on the speed of the measurements as is depicted in Table 1.

Table 1. Measured parameters and basic measurement accuracy. From [24].

Parameter	Measurement Range	Fast	Medium	Slow
Cs, Cp	00000 .01 fF to 9.999999 F	±0.5%	±0.25%	±0.05%
Ls, Lp	0000.001 nH to 99.99999 H	±0.5%	±0.25%	±0.05%
D	.0000001 to 99 .99999	±0.005	±0.0025	±0.0005
Q	.0000001 to 999999.9	±0.005	±0.0025	±0.0005
Z. Rs, Rp, ESR,Xs	000.0001 mΩ to 99 .99999 MΩ	±0.5%	±0.25%	±0.05%
Y, Gp, Bp	00000 .01 µS to 9.999999 MS	±0.5%	±0.25%	±0.05%
Phase Angle	-180.0000° to +179.9999°	±1.8°	±0.9°	±0.18°

The Quadtech 7600 can generate an AC signal that ranges from 10 Hz to 2 MHz with 20 mV to 5.0 V peak [24].

3. Agilent E3631A Programmable DC Power Supply

The Agilent DC supply provided an external DC voltage bias for the Quadtech 7600 to apply to the device under test (DUT). The E3631A is capable of providing a range 80 W to 200 W of power with low noise [25]. The E3631A has built-in GPIB and RS-232 interfaces that allow for remote interfacing to a PC.

4. Micromanipulator Model 4460 Probe Station with heat exchanger

The apparatus that was used to set the die for measurement was the Micromanipulator 4460. The 4460 was modeled after the Micromanipulator Model 8860 probe station. The 4460 can be equipped with either a 6” or 8” ambient gold-plated, stainless steel, thermal chuck with full plumbing. The thermal chuck is connected to the Micromanipulator C1000 Heat Exchanger which has the ability to heat the chuck up to 400 C [26]. This provides the

ability to heat the device in order to characterize performance as the temperature varies. A light tight enclosure was utilized to block RF interference that could have affected the measurements.

5. Silvaco UTMOST™ 4

UTMOST™ 4, a software suite package from Silvaco, was utilized to interface with the Quadtech 7600 and Agilent power supply. UTMOST™ 4 is capable running multiple test setups and plotting the results. The test setups can be saved and reused for repeatable testing. The acquisition is autonomous, and UTMOST™ 4 can save the data in comma-separated value (CSV) format for post testing analysis.

B. DEVICE UTILIZED

The devices investigated were NPTB0004 5 W GaN RF HEMT devices fabricated by Nitronex Corporation. These devices are similar to the devices used in another investigation [14]; however, the NPTB0004 is a single AlGaN/GaN HEMT device that produces lower output power. The devices in this investigation are not packaged but are die transistors, nor do they contain vias at the source contacts. This left the body of the device to float. Die devices allowed for accurate measurements utilizing probes rather than soldering leads to packaged device that would add large series resistance to the gate. The device is laid out with source-ground-source contacts on one side and a drain contact opposing the source and ground contacts as seen in Figure 8.

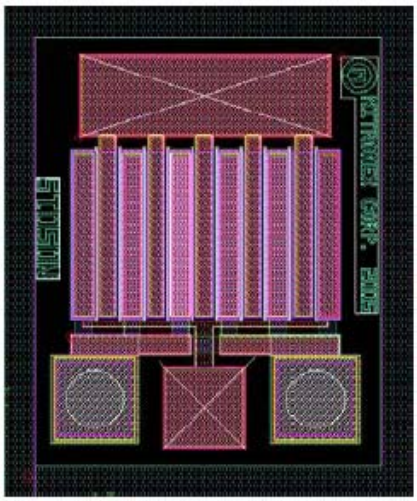

Figure 8. Microscopic layout of a 2mm die placed in NPTB0004. From [28].

The structure of the device has a Si substrate with thin layer of AlN followed by a GaN buffer and then an AlGaN barrier. The contacts for the source and drain are Ti/Al/Ni/Au alloys, and the gate contact is Ni/Au. Next, a layer of SiN passivation layer is placed on the contacts followed by an Au source-connected field plate over the gate [29]. The source-connected field plate reduces the high stress induced by the electric field on the drain side of the gate when biased. A cross-section scanning electron microscope (SEM) image of a Nitronex AlGaN/HEMT is shown in Figure 9.

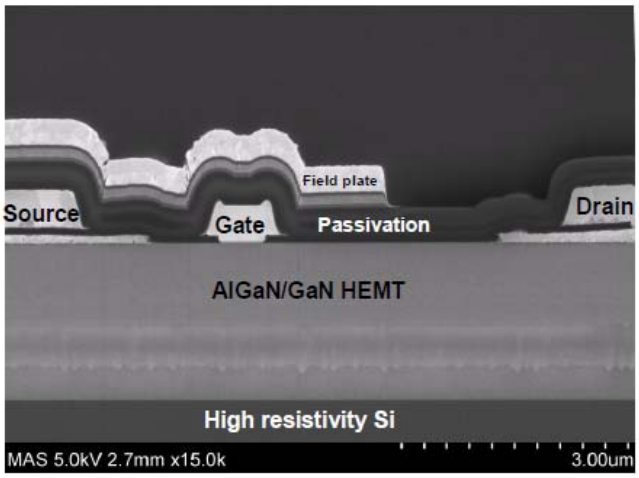

Figure 9. Cross-section SEM of 0.5µm AlGaN/GaN HEMT. From [28].

C. EXPERIMENTAL APPROACH

1. Device Setup

The die HEMTs were epoxied with conductive silver epoxy on a 10 mm by 10 mm by 0.5 mm Si substrates. This allowed for the device to be placed on the heat chuck of the probe station. Micromanipulator and Signatone probe holders with Signatone probe tips were used to make contact with the gate, source, and drain of the HEMT.

The connections for the C-V characterization tied the source and drain together. The low potential and low current leads from the Quadtech 7600 were connected with a T-BNC connector and then connected to the probes in contact with the drain and source of the HEMT. The high potential and high current leads from the Quadtech 7600 were connected together with a "T" BNC connector and then connected to the probe in contact with gate of the HEMT.

Depicted in Figure 10 is the set up for the I-V characterization.

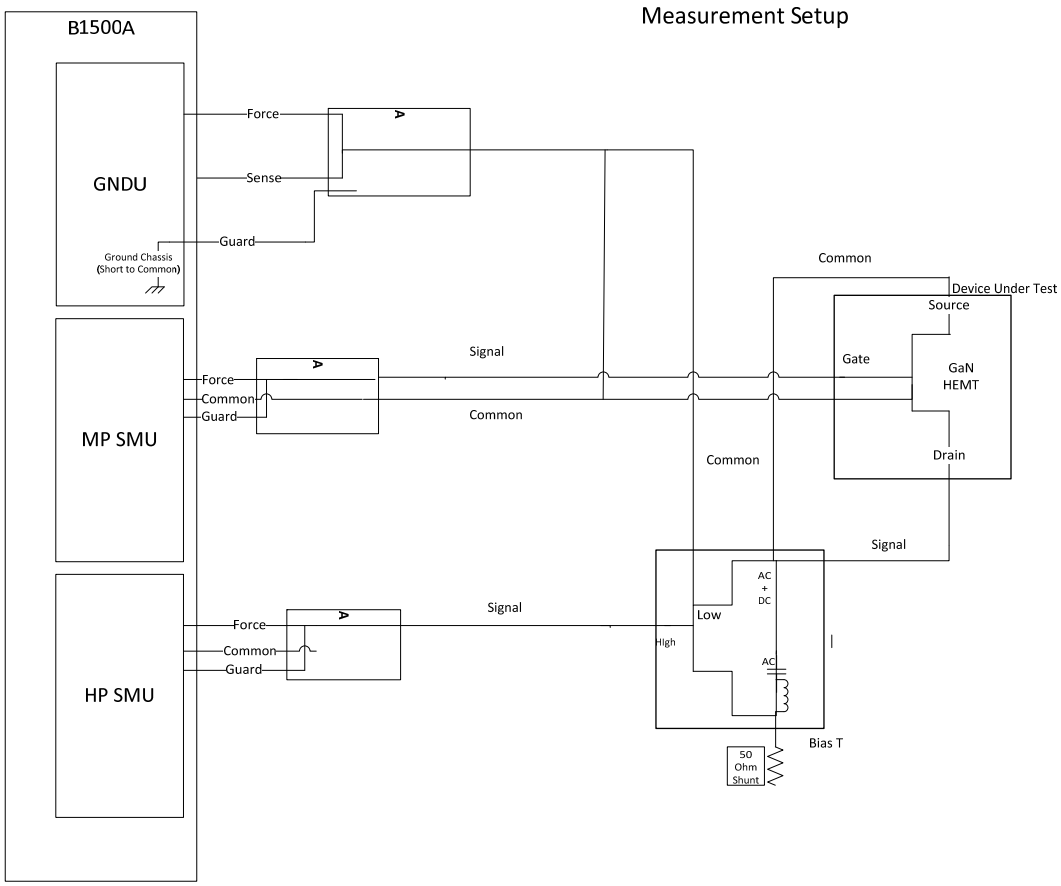

Figure 10. B1500a current-voltage connection.

D. TESTING PROCEDURES

Initial characterizations were performed at the temperature specified to track the performance prior to stressing. These characterizations involve the C-V trace, the I_{gs}-V_{gs} trace and the I_{ds}-V_{gs} trace.

The C-V trace swept the gate voltage from 0 V to -4 V in 0.5 V steps. The QuadTech 7600 was set to record 100 averages at each voltage step under the fast measurement setting. The magnitude of the AC oscillation applied was

300 mV at 10 kHz and 50 kHz. For the I_{ds}-V_{gs} trace, the gate was biased at a range of -2 V to -1 V in 25 mV steps. The drain was biased from 0 to 15 V in 153 mV steps. The source of the DUT was grounded.

The eight GaN HEMTs were tested with two sets of GaN HEMTs tested at four different temperatures. The temperature ranged from 300 K to 375 K in 25 K steps. The DUT was step stressed 200 s with a recovery period of 200 s. Depicted in Figure 11 is the experimental flow chart.

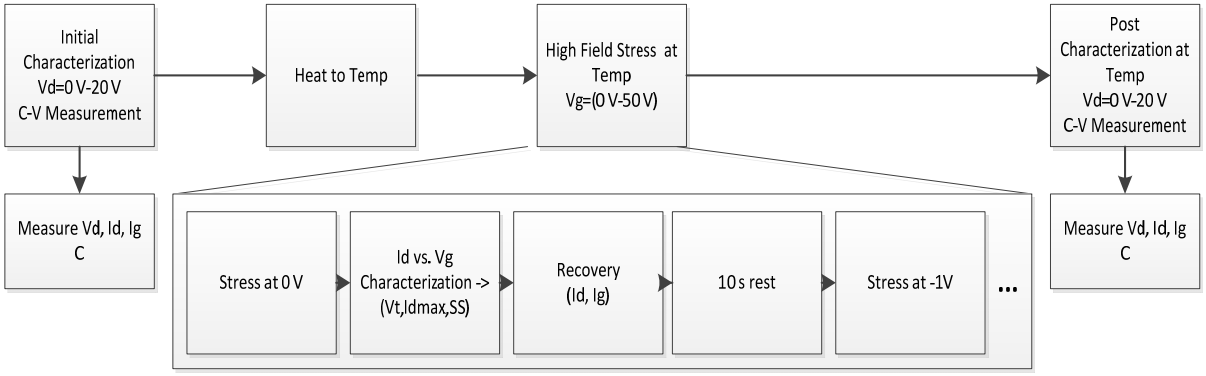

Figure 11. Step-stress experimental flowchart.

The voltage applied on the gate of the DUT went from 0 V to -50 V in -1 V steps. During the stressing period and recovery period, we monitored the gate current and the drain current. To record the currents during the recovery period, the gate was biased at -1 V, and the source and drain were grounded. Between the recovery period and stressing, the threshold voltage was monitored. After stressing, the temperature was held on the device and post characterizations were performed. The device was rested for 3600 seconds and characterized again. After 24 hours of

recovery, a final characterization at the temperature the device was stressed at was performed so that overall we captured the DUT for pre-stress, stressed, and post-stress, and recovery conditions.

IV. EXPERIMENTAL RESULTS

A. DRAIN CURRENT VERSUS TIME: STRESS MEASUREMENT

The drain and gate currents were monitored during the step stress test. The trapping transients were observed at each voltage step until break down. Depicted in Figure 10 are the drain currents versus applied voltages for each device at the various temperatures.

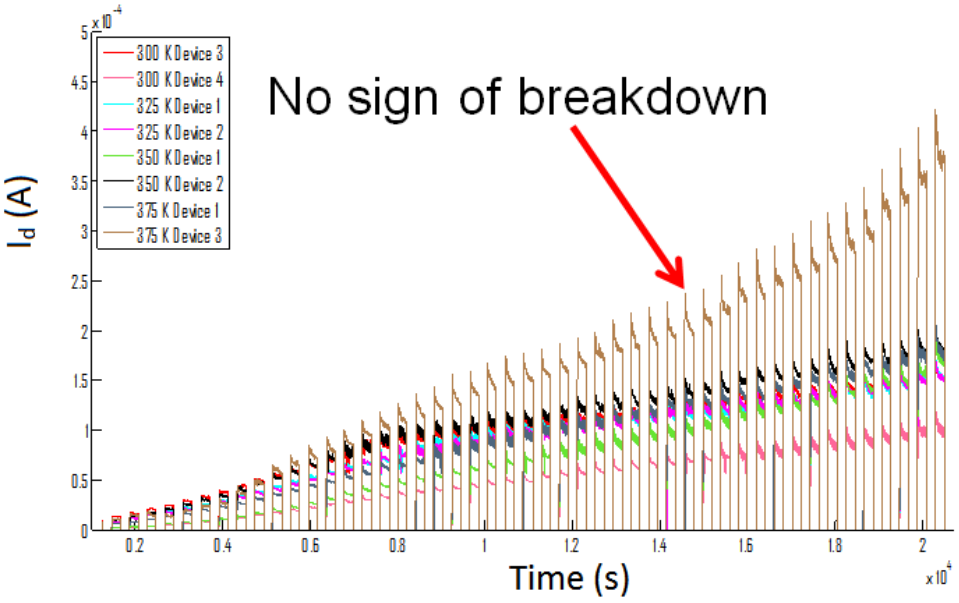

Figure 12. The drain current versus time.

It can be seen from Figure 12 that these devices exhibit an overall linear increase in drain current at low reverse bias. This is consistent with prior work [14]. Devices tested at higher temperatures had higher drain currents. This was to be expected due to additional thermal energy exciting trapped carriers. Unexpectedly, the devices did not show signs of breakdown. This could be due to

probing the contacts rather than the setup used in [14]. Probing the contacts reduced the series resistance at the gate and effectively increased the voltage on the gate.

B. DRAIN AND GATE CURRENT VERSUS TIME: RELAXATION MEASUREMENTS

A relaxation period was followed after each step stress. It was observed that the drain current dropped dramatically at higher temperatures, while the gate current remained steady. The results for 300 K, 325 K, 350 K, and 375 K are shown in Figures 13 to 16.

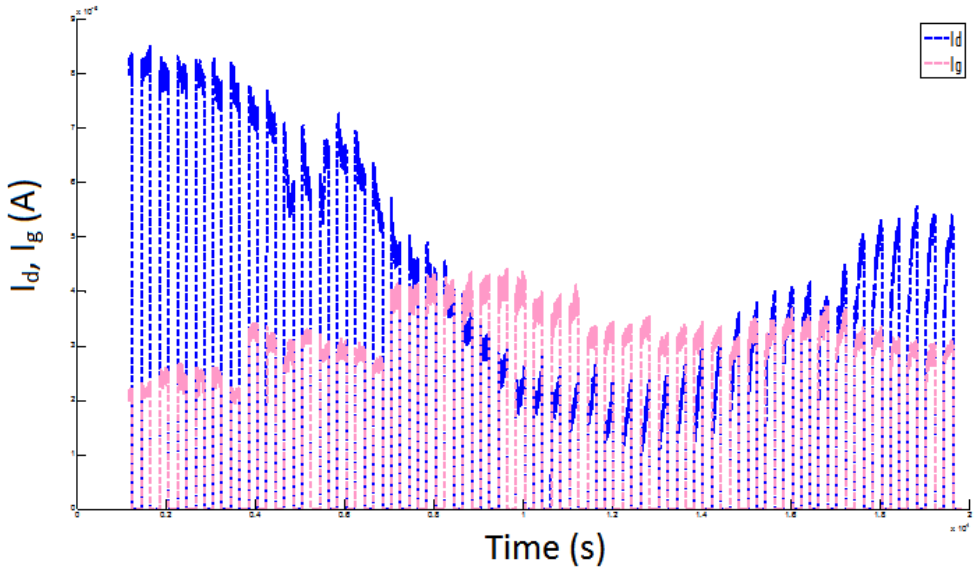

Figure 13. Drain and gate currents during the relaxation period at 300 K.

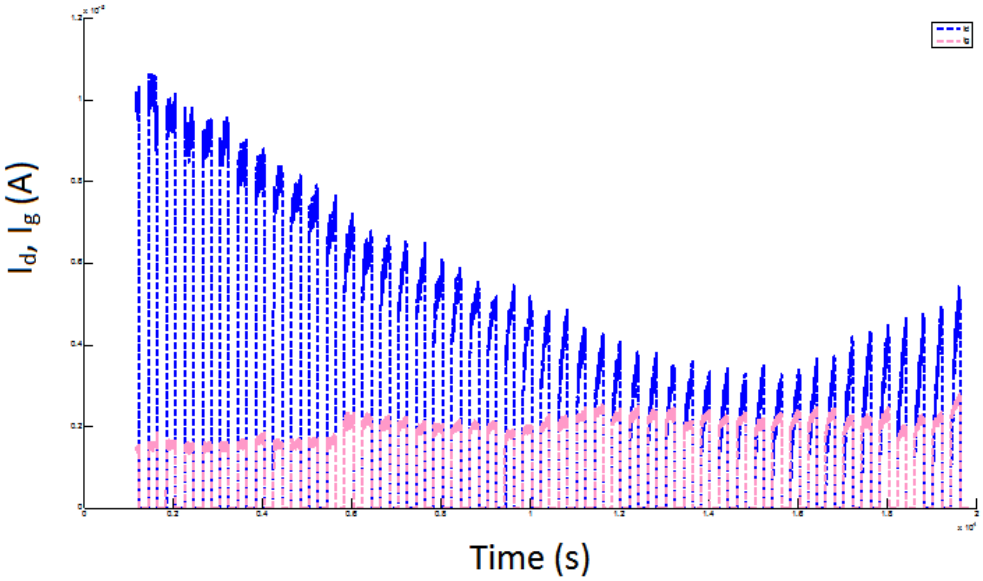

Figure 14. Drain and gate currents during the relaxation period at 325 K.

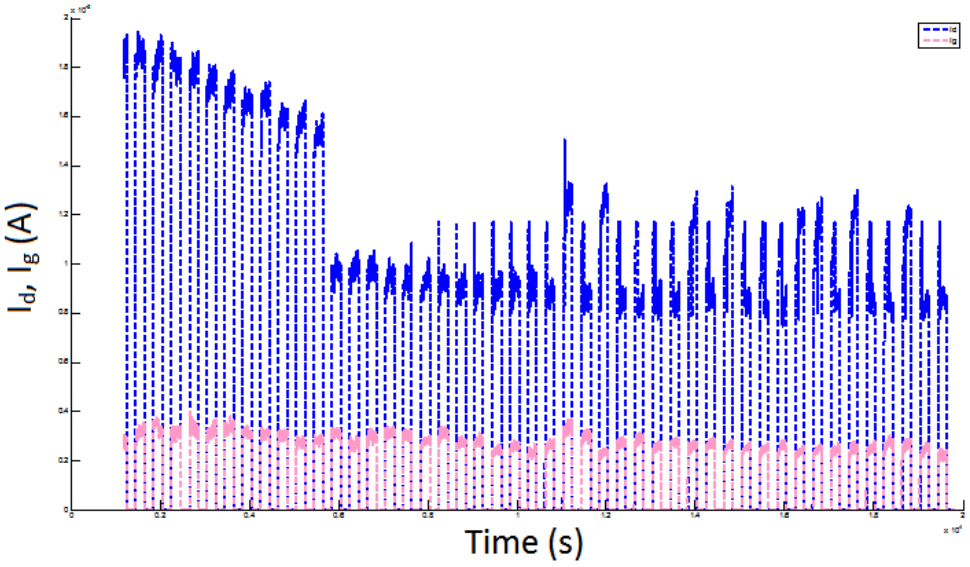

Figure 15. Drain and gate currents during relaxation period at 350 K.

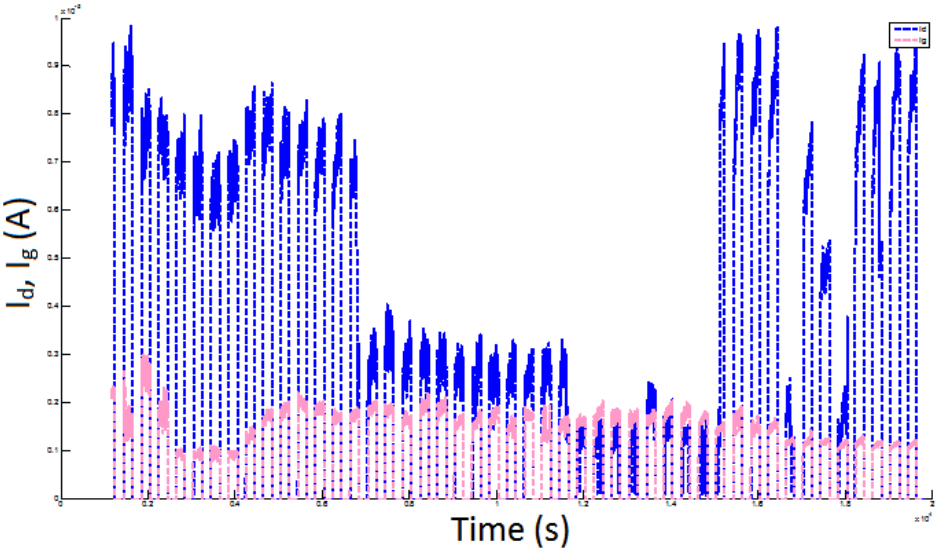

Figure 16. Drain and gate currents during relaxation period at 375 K.

C. GATE CURRENT LEAKAGE

Shown in Figure 17 is the gate leakage for device 1 tested at 300 K. Similar gate leakage is seen throughout the devices under test. The gate leakages in past studies show an increase in gate leakage after stressing. The DUT in this experiment showed a decrease in gate leakage after stressing that remained one hour after the stress test. It seems that the step stress annealed the device.

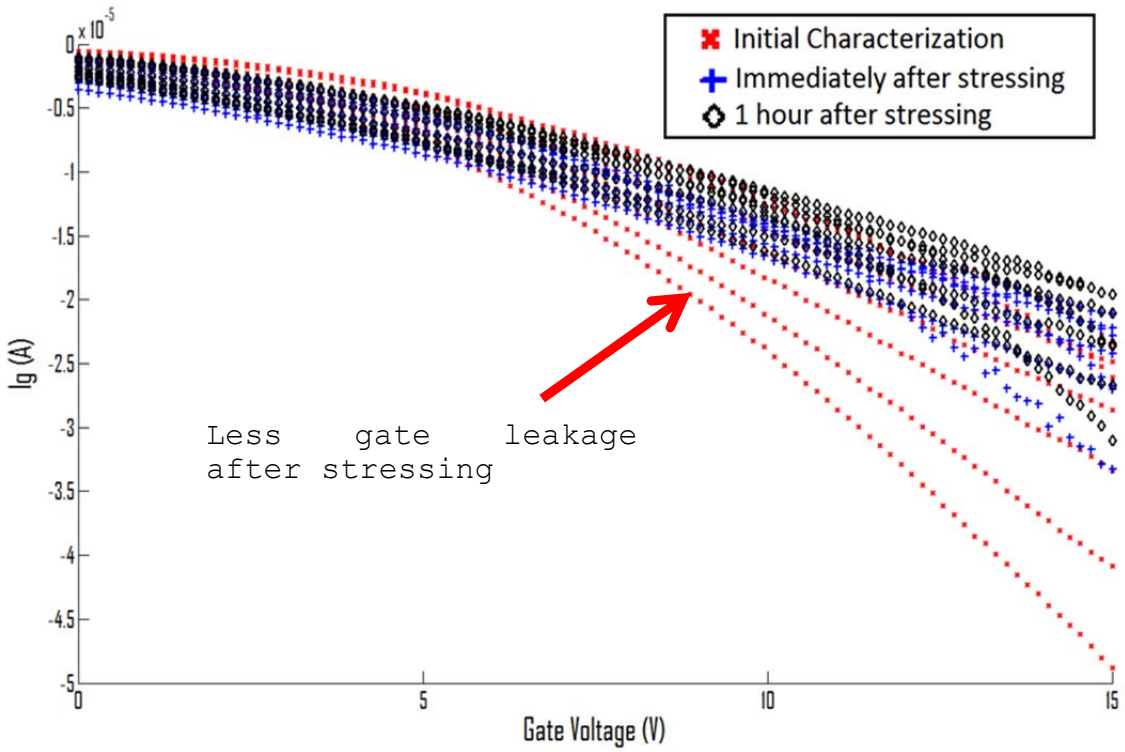

Figure 17. Drain current versus gate voltage at various stages during the test.

D. ACTIVATION ENERGY LEVEL

The energy that is required for a carrier to move from the E_T to E_C or E_V is the activation energy E_a. The activation energy can be described with the Arrhenius equation;

$$\tau = AT^2 \exp\left(\frac{E_a}{k_b T}\right) \tag{16}$$

where τ is the time constant and A is a constant prefactor [28]. The time constant is related to the transient response of the detrapping of electrons seen in the drain and gate currents during the step stress. The transient response is inversely proportional to the time constant. Depicted in Figure 18 are the activation energies

calculated. It can be seen from Figure 18 that the activation energy shows a field dependency. The activation energies at lower field strengths have higher activation energies compared to higher field strengths.

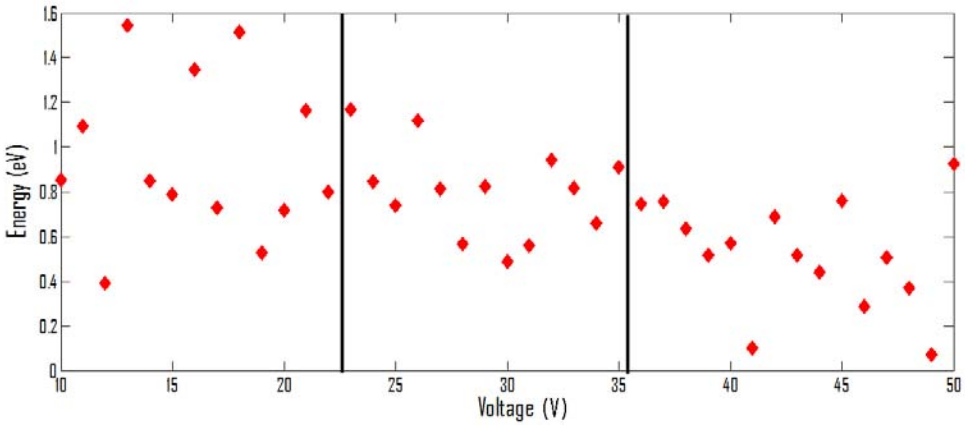

Figure 18. Activation energies for the devices under test.

E. SIMULATION

Courtesy of Matthew Porter, a simple model of the Nitronex NPTB0004 was created in Silvaco ATLAS. The regions the simple model replicated are highlighted in the TEM cross-section of the DUT shown in Figure 19. Depicted in Figure 20 is the ATLAS model.

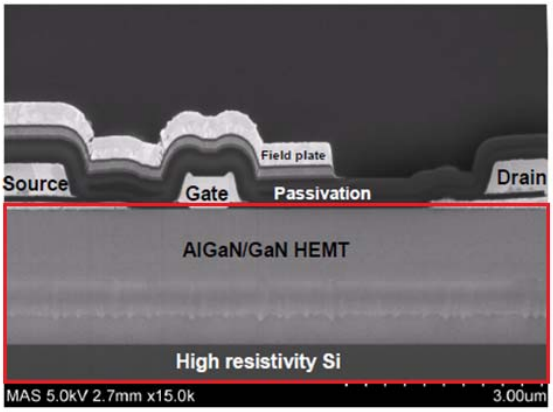

Figure 19. The cross-section of the Nitronex NPTB0004. Highlighted is the simulated region. After [29]

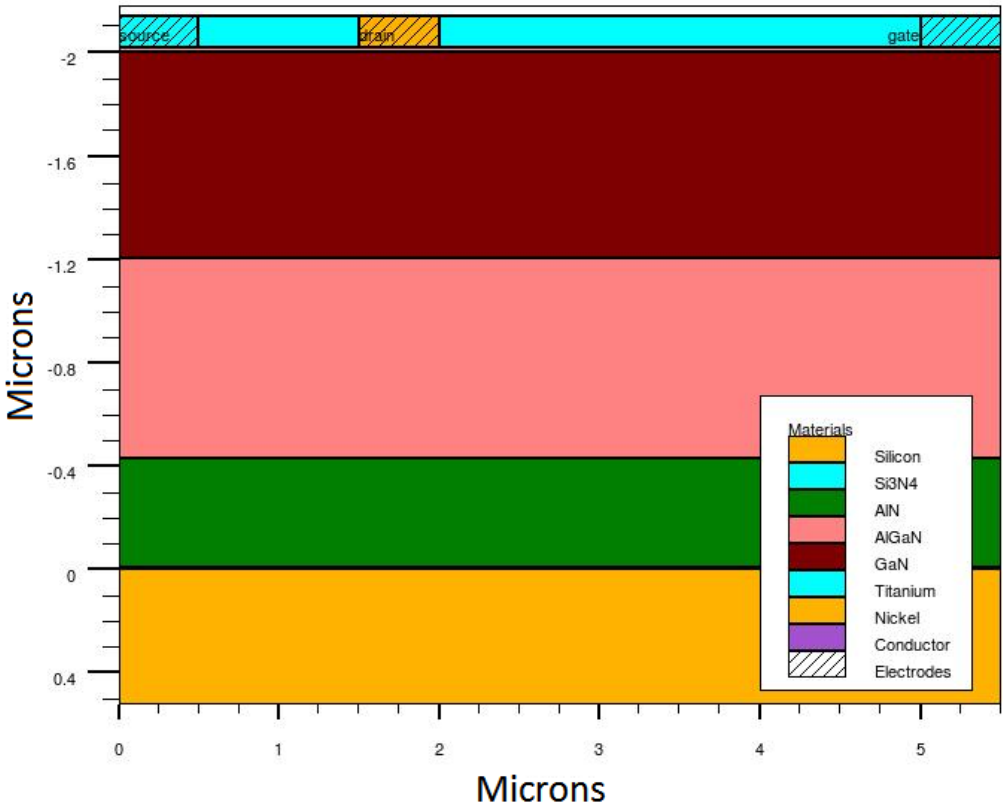

Figure 20. The structure of the simulated AlGaN/GaN HEMT.

The purpose of modeling the device represented in Figure 19 was to determine the parasitic capacitance caused

by the source-connected field plate. The model and equations used to calculate D_{it} neglected parasitic capacitances such as the gate-to-drain capacitance and the gate-to-source capacitance since these regions contribute negligible values of capacitance. The source-connected field plate could be considered as a capacitance with an area approximately that of the gate contact with a thickness of 0.3 µS and with a dielectric of the passivation material.

Shown in Figure 21 are the simulated results with and without traps. At accumulation, all charges are depleted within the barrier and in the bulk; therefore, in this regime the total capacitance is the source-connected field plate.

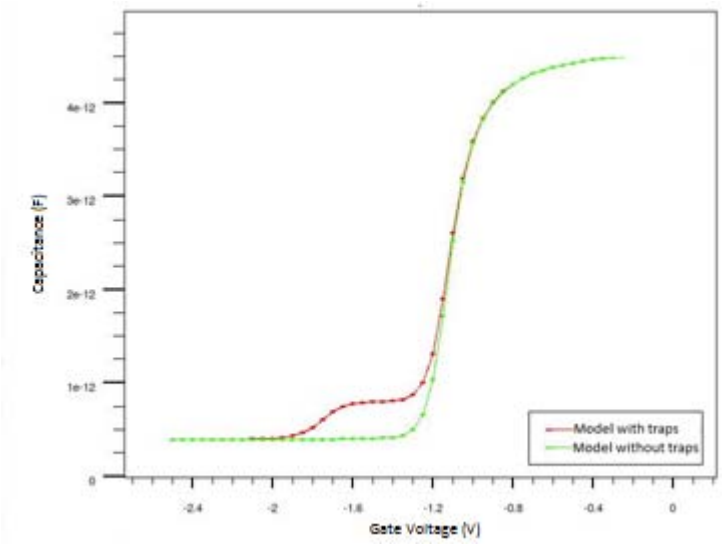

Figure 21. Simulated C-V measurement with traps and without simulated at 50 kHz.

F. DENSITY OF TRAP

Utilizing the Quadtech 7600, we measured the capacitance of the AlGaN/GaN die devices both pre-stressed and post-stressed. Shown in Figures 22 and 23 are the C-V curves for pre-stressed devices at 10 kHz and 50 kHz, respectively.

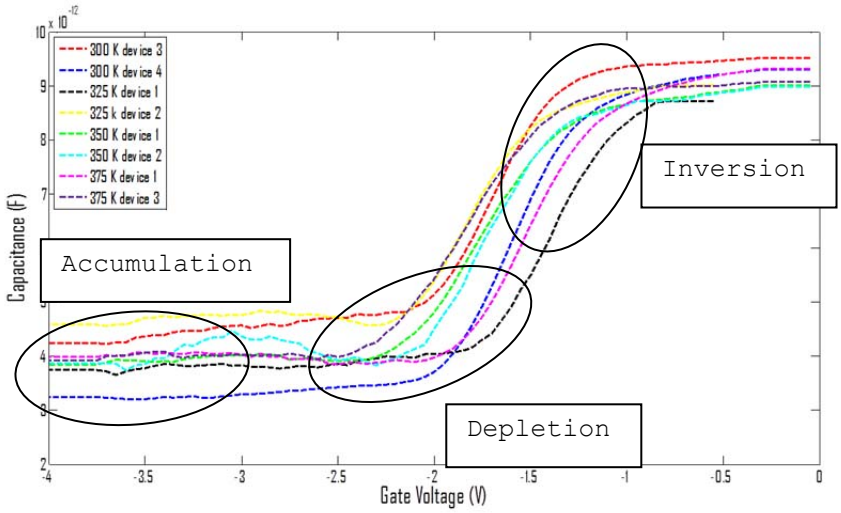

Figure 22. Capacitance versus voltage measurement at 10 kHz.

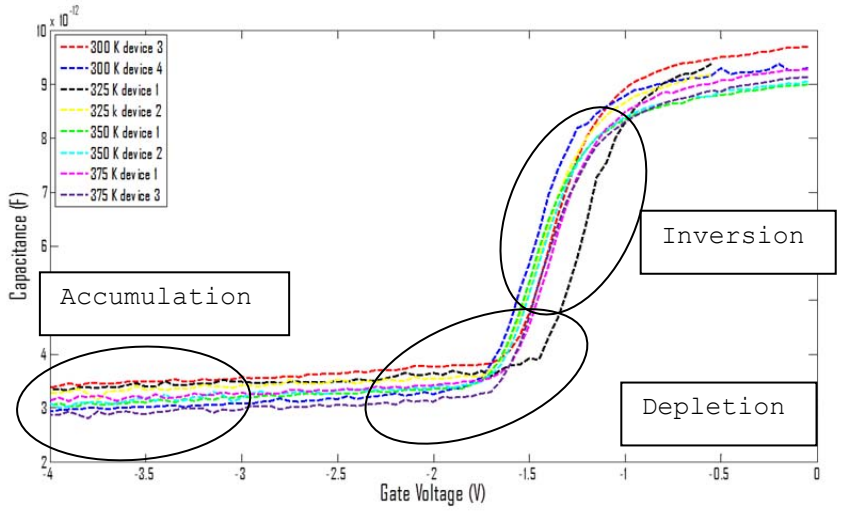

Figure 23. Capacitance versus voltage measurement at 50 kHz.

Highlighted in both figures are the inversion, depletion and accumulation regimes. The differences in capacitances in the accumulation regime for some of the devices suggest the traps are located in the GaN buffer. A simplified model is shown in Figure 24.

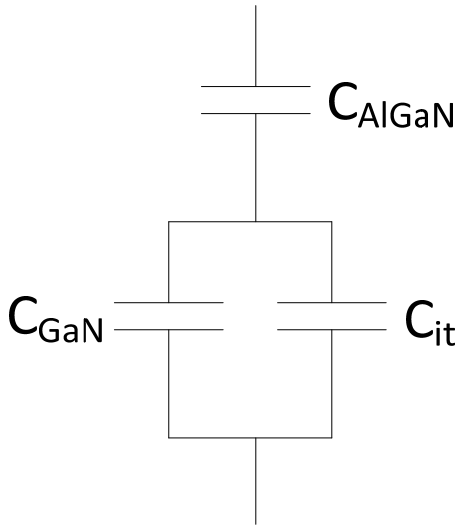

Figure 24. Simplified capacitances model for AlGaN/GaN HEMTs.

The interface trap densities for the DUT were calculated using the method proposed by Castagne and Vapaille. The method was used to calculate the interface trap density from the onset of inversion to accumulation. The interface trap densities were plotted versus the surface potential to depict the interface trap densities within the energy band of the GaN buffer. Shown in Figures 25 and 26 are the interface trap densities for each device pre-stressed and post-stressed, respectively.

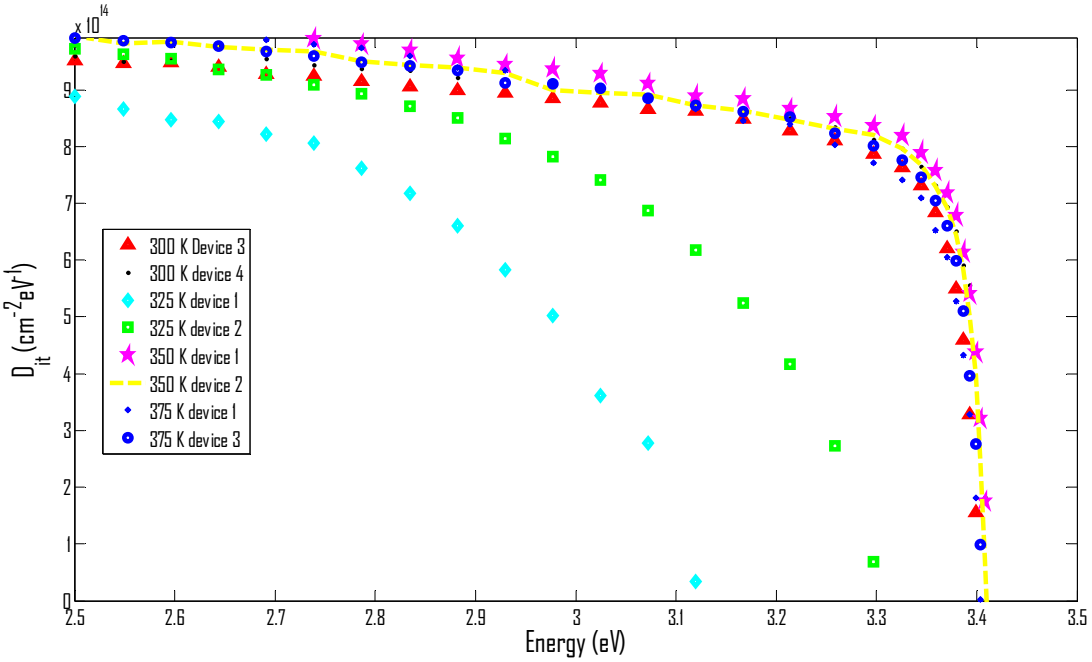

Figure 25. Interface trap densities versus energy (eV) for the DUT at pre-stressed.

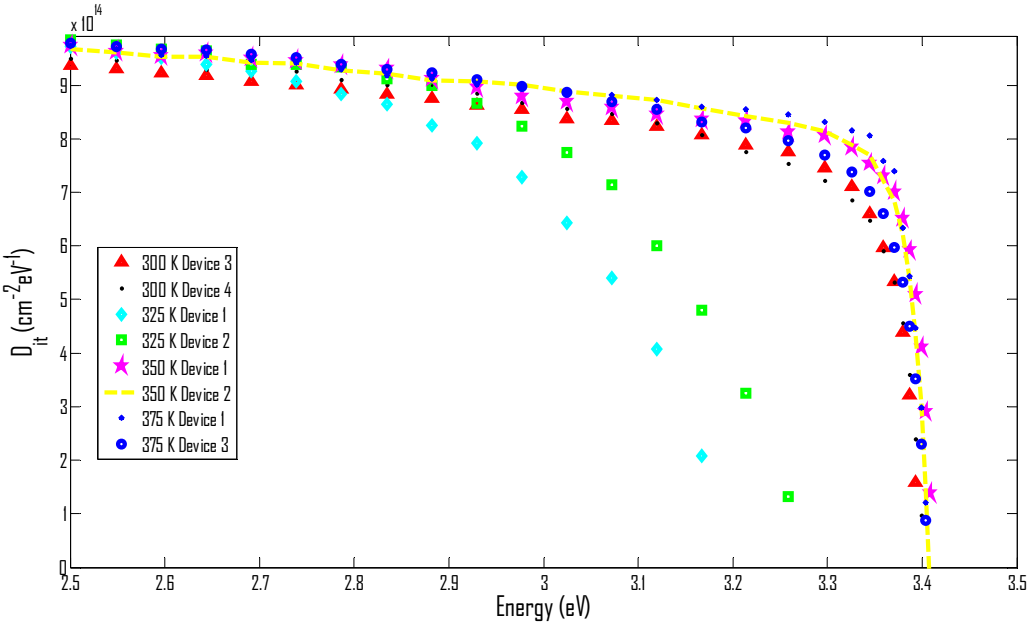

Figure 26. Interface trap densities versus energy (eV) for the DUT at post-stressed.

The interface trap densities for the DUT were on the magnitude of 10^{14} $cm^{-2}eV^{-1}$ both pre- and post-stressed. The interface trap densities varied pre- and post-stressed. The interface trap densities for devices tested at 300 K decreased after stressing, while the interface trap densities tested at 325 K increased after stressing.

G. DAY RECOVERY MEASUREMENTS

Another C-V measurement was recorded after the DUT was placed back into their respective container to recover for 24 hours. Unfortunately, the recovery measurement for device 3 at 300 K was not recorded due to poor handling of the device. Depicted in Figure 25 are the C-V measurements at 50 kHz.

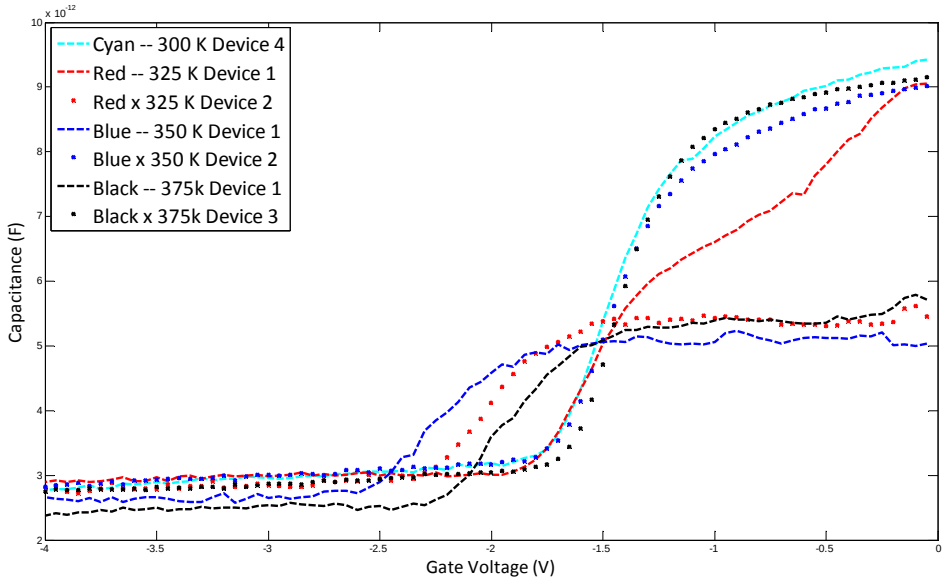

Figure 27. 50 kHz C-V measurements after a day of recovery.

From Figure 25 it can be seen that the AlGaN barrier capacitance for device 2 at 325 K and device 1 at 350 K

lowered after a day of recovery. Researchers at the University of Florida discovered the formation of dislocations from the gate to the AlGaN barrier. The dislocation allows for impurities within AlGaN barrier to bond with gate metal forming an additional oxide layer as shown in the TEM image in Figure 26 [30]. This additional oxide layer could increase the AlGaN barrier thickness which lowers the barrier capacitance.

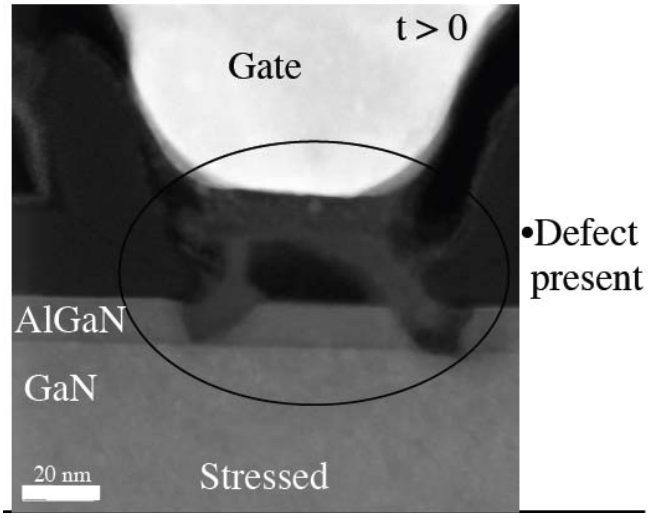

Figure 28. TEM cross section of an AlGaN/GaN HEMT with defect present. From [30].

The trap densities increased by an order of magnitude for some DUTs after the day of recovery. The results are shown in Figure 29. Highlighted in Figure 29 are two distinct trap locations at 2.5 eV and 2.7 eV for device 2 at 325 K.

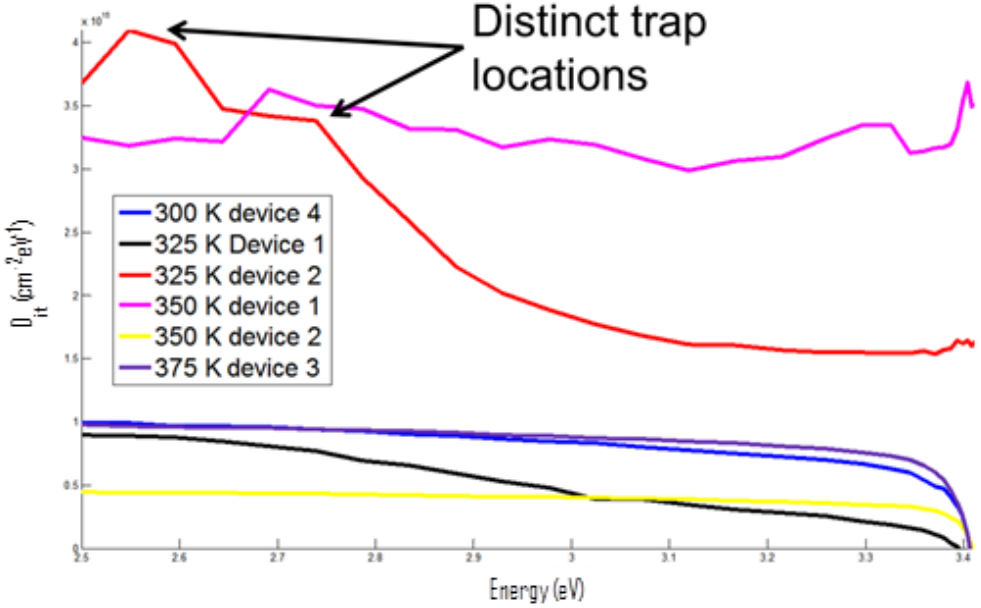

Figure 29. D_{it} versus energy after a day of recovery. Highlighted are distinct trap locations.

V. CONCLUSIONS AND FUTURE WORK

A. CONCLUSION

From the results, we found that the devices tested did not have the same degradation characteristics as seen in prior work [14]. The DUT in this thesis had a decrease in gate leakage after stressing. The DUTs also had three regions for activation energies that were voltage dependent. At lower voltages, the activation energies were higher but lowered as the voltage increased. The threshold shift for the DUT showed no dependency on voltage or temperature.

Devices tested at 300 K, 350 K, and 375 K had similar interface trap densities, while the interface trap densities were less for devices that were tested at 325 K. Some post-stressed devices showed an increase in interface trap densities while others showed a decrease.

Forty percent of DUTs had a lower barrier capacitance after a 24 hour recovery period. This could be evidence that an oxide layer is forming under the gate in the AlGaN barrier, effectively increasing the width and lowering the barrier capacitance. The interface trap densities increased by an order of magnitude after a day of recovery with a device that had two distinct trap locations.

B. FUTURE WORK

Different methods of stressing will provide further information as to whether AlGaN/GaN HEMTs degradation have a stronger dependency on temperature or field. Stressing the device at constant field strength with no recovery

period will determine the effects the recovery periods on the device. Transmission electron microscopy can determine the cause of the lower barrier capacitance.

The interface trap densities and location extracted from this thesis can be utilized for accurate simulation prediction. Simulating the results to match the findings in this thesis can validate the claims made in this thesis.

The devices under test had a source-connected field plate that reduced the stress caused by the electric field but also provided additional parasitic capacitance. Future testing on devices that lack the source-connected field plate would be beneficial to determine if the device will perform better with or without it.

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