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High-output-power densities from MBE-grown *n*- and *p*-type PbTeSe-based thermoelectrics via improved contact metallization[†]

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ABSTRACT

Electrical power densities of up to 33 W/cm^2 and up to 12 W/cm^2 were obtained for *n*- type and *p*-type PbTeSe-based stand-alone thermoelectric devices, respectively, at modest temperature gradients of ~200 °C (T_{cold}=25 °C). These large power densities were enabled by greatly improving electrical contact resistivities in the thermoelectric devices. Robust electrical contacts with contact resistivities as low as 3.9x10^{-6} Ω-cm^2 and 4.0 x10^{-6} Ω-cm^2 for *n*- and *p*-type telluride-based- materials, respectively, were developed by investigating several metallization schemes and contact layer doping/alloy combinations, in conjunction with a novel contact application process. This process exposes heated semiconductor surfaces to an atomic hydrogen flux under high vacuum for

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surface cleaning (oxide and carbon removal), followed immediately by an *in-situ* electron-beam evaporation of the metal layers.

Introduction

Thermoelectric materials provide direct solid-state conversion between thermal and electrical energy. They are of interest for both electrical power generation and solid-state cooling applications, where their small size, scalability, lack of moving parts and lack of pollutant emissions may be an advantage over other competing technologies. The well-known thermoelectric figure of merit for these materials, ZT, is given by $S^2\sigma T/\kappa$, where S is the Seebeck coefficient, σ is the electrical conductivity, T is the temperature, and κ is the total thermal conductivity (usually comprised mainly of lattice phonon and electronic contributions). Thermoelectric conversion efficiency is not limited only by Carnot efficiency ($=\Delta T/T_{hot}$) and ZT, but also by electrical and thermal parasitics, such as electrical contact resistivity.

For maximum electrical power output from a thermoelectric generator, the load resistance should be matched to the thermoelectric generator resistance, including all parasitics. Under these conditions, the load voltage will be equal to half of the thermoelectric open-circuit voltage, given by $V_{O.C.}=(|S_p|+|S_n|)\Delta T$, where $S_{p,n}$ are the Seebeck coefficients for the p- and n-type materials in the thermocouple pair. The total power output of a single thermocouple (one n-type leg and one p-type leg connected electrically in series and thermally in parallel) is given by Eq. (1),

$$P=\frac{V^2}{R}=\frac{\left(|S_p|+|S_n|\right)^2\Delta T^2 A}{4\left(\rho_p+\rho_n\right)L+16\rho_c}. \qquad (1)$$

In Eq. (1), A is the cross-sectional area of a single thermoelement, L is the length of a single thermoelement, ρ_p and ρ_n are the intrinsic resistivities of the p- and n-type legs,

respectively, and ρ_c is the contact resistivity. It is assumed in this equation that the *n*- and *p*-type legs have the same cross-sectional areas, lengths, and contact resistivities. The importance of minimizing the contact resistivity is apparent from Eq. (1). A typical guideline is that the contact resistance should be less than 10% of the intrinsic thermoelectric resistance. For our thermoelement geometries with 1 mm^2 areas and 100 μm lengths, this implies a required contact resistivity of low 10^{-6} Ω-cm^2 since the typical intrinsic PbTeSe-based thermoelement resistivity is on the order of 1-5x10^{-3} Ω-cm. Figure 1 shows the effect that contact resistances can have on the performance of a p-n thermoelectric power couple. While extremely low contact resistivities are readily achieved in more mature semiconductor material systems such as Si and InP/InGaAs, this is a significant challenge for relatively less-investigated systems such as PbTe.

In this paper we report a technique that has achieved contact resistivities as low as 3.9x10^{-6} Ω-cm^2 and 4.0 x10^{-6} Ω-cm^2 for our *n*- and *p*-type PbTe-based materials, respectively using Ti/Ni/Au (n-type) and Ni/Au (p-type) contacts . The Ti/Ni/Au metallization scheme was also found to work nearly as well as Ni/Au on p-type PbTeSe material. This has enabled us to achieve electrical power densities as high as 33 W/cm^2 at a relatively modest temperature gradient of 200 °C (T_{cold}=25 °C) from *n*- type PbTeSe stand-alone thermoelectric elements and power densities up to 12 W/cm^2 from *p*-type PbTeSe material using the same Ti/Ni/Au metal scheme. Furthermore, the Ti/Ni/Au metallization scheme was found superior to all the other metallization schemes investigated at ΔTs from 200 °C to 300 °C. The Ti/Ni/Au metal scheme, along with silicon nitride device wall passivation, appears to also significantly improve the robustness of the n-type devices when they were operated at a ΔT of 220° C in an initial life test (life tests on the p-type material were not yet performed).

Experiment

Growth

PbTeSe samples were grown by molecular beam epitaxy (MBE) in a commercial 2" growth system on (111) BaF_2 or CaF_2 substrates using PbTe, PbSe, SnTe, and Te sources, along with Bi_2Te_3 and Na_2Te for *n*- and *p*-type doping, respectively. PbSe layers were alternated with PbTe layers with typical periods ranging from 14-20 nm with ~13% PbSe by volume fraction.

In initial studies, stop growth experiments indicated Stranski-Krastanov self-assembled PbSe nanodot formation was present during the first few layers of growth after growth initiation. These studies were performed using atomic force microscopy on the nanodot stop growth top layer and cross-sectional transmission electron microscopy (X-TEM) on the composite 4-5 layer structure. Subsequent X-TEM of 90 to 110-um-thick samples, however, show no such nanodot structures present. High fidelity scanning electron (SEM) micrographs of the cross-sections of the thick samples show an initial thick defect entangled layer, followed by the formation of columnar growth. The high solubilities of the constituent materials, along with the 30 to 40 h of growth at 300 to 325° C required to produce the thick material, appears to likely produce a non- homogeneous alloy of PbTeSe rather than a purely nanodot superlattice sample. Here the designation PbTeSe is used for the designation of the overall material grown by the layered growth process.

The structures of the samples used in this study are given in Table I (n-type samples) and Table II (p-type samples). Contact study samples were typically 5-6 μm thick. The contact resistivities of the various metal recipes applied were obtained using the transfer length method (TLM) [1] with the top side contacted. The power generation

samples were approximately 100 μm thick with both sides contacted. The *n*-type samples utilized 2 x 10^{18} to 6 x 10^{19} Bi doped ~100 nm-thick PbTe contact layers while the *p*-type samples utilized 2 x 10^{20} Na doped ~100 nm-thick PbSe contact layers; 1 x 10^{19} not intentionally doped (nid) ~100 nm-thick SnTe contact layers; or 2 x 10^{20} Na doped ~100 nm-thick SnTe contact layers.

Surface Cleaning and Contact Formation

This work utilized three separate chambers of a vacuum cluster tool that also allowed ultra-high vacuum sample transfers between chambers. The chambers consisted of an introduction chamber, X-ray photoelectron spectrometry chamber and custom electron evaporation chamber. The custom evaporation chamber contained a heated substrate stage, a commercial atomic hydrogen cleaning gun and a three pocket electron beam evaporator with the usual shutters and crystal thickness monitor.

Surface cleaning before metallization was typically performed using a 40 min to 60 min atomic hydrogen cleaning step, keeping the atomic hydrogen gun filament at 9.5 A and the hydrogen flow rate at a level so that the chamber ion gauge read a constant 1- 2 x 10^{-6} Torr. The samples were kept at a thermocouple temperature of either 140 °C or 200 °C (heater located behind the molybdenum sample holder), followed immediately by electron-beam metal evaporation. Three samples were used for the thermoelectric power measurements. Sample G-580-C (*n*-type) was initially metalized using *in-situ* Sn in the MBE growth chamber immediately after sample growth without any surface cleaning. After substrate removal, G-580-C's back side was metalized using atomic hydrogen cleaning and a Sn/Ni/Au contact scheme. Samples G-676 (*n*-type) and G658, (*p*-type) had both sides metalized using in situ hydrogen cleaning and the Ti/Ni/Au contact metallization scheme.

BaF_2 substrate removal for backside metallization was performed in a solution of DI water, nitric acid, and boron oxide for several hours. The CaF_2 substrates (used to grow materials only for the contact studies) were not removed for TLM processing and measurements. For TLM contact resistivity characterization, four-wire resistance measurements between each pair of contact pads were typically repeated a few times to confirm stability and repeatability of the measurement, while precision resistors were used to confirm measurement accuracy to better than 1%.

It is important to note that due to step-height issues and intrinsic defects in the films caused by step edges in the surfaces of the cleaved BaF_2 substrates and polishing/surface damage issues in the polished BaF_2 and CaF_2 substrates used in this work, that smaller TLM pads, with smaller geometric spacings, produced significantly more usable contact resistance measurements. In all cases, except for the measurement on G-539-*p*, stainless steel stencil masks with TLM pad dimensions of 0.3 x 3 mms and pad spacings of 1, 1.5, 2, 2.5, and 3 mm were used. Sample G-539-*p* is further described in Table II. Since the goal is to completely cover the device material with low resistance contact metals, avoiding lithography is not an issue. The TLM structures were electrically isolated by saw cutting. Due to variations in the masks, mask height differences to the samples, and the placement of the saw cut streets, all TLM metal patterns were measured using optical microscopy. Very small TLM patterns were also laser cut into tantalum foils for use as stencil masks in shadow evaporation. These masks designs had pad dimensions 100 x 200 μm with pad spacings of 60, 65, 71, 78, 86, and 95 μm. These masks were used to compare contact results with the standard mask on wafer G-623 piece D.

The stencil masks allowed the pad openings to the sample to be hydrogen cleaned at temperature without worrying about processing residue before the *in-situ* application of the metal stacks. The relationship of the pad orientation to the deposition hearth position was also fixed in order to produce sharp pad edges in the TLM pattern between pads.

In order to obtain a good ohmic contact and the lowest possible contact resistivity removal of surface oxides is critical. In the late 1990's V.A. Kagadei *et al.* [2] and Vishnayakov *et al.* [3] developed an atomic hydrogen source and applied it to the surface cleaning of GaAs and AlGaAs. More recently Alcorn [4] developed high quality GaSb contacts by using the atomic hydrogen process to clean GaSb surfaces just prior to *in-situ* metallization. In this work, the Alcorn process has been applied to the tellurides.

The ability of atomic hydrogen to successfully clean the PbTe-based and SnTe-based sample surfaces is shown by the X-ray photoelectron spectroscopy (XPS) results in Figs. 2 and 3 respectively. The pre-cleaned *n*-PbTe and *p*-SnTe surface responses at O, C, Pb and Te peak energies are shown in green in Figs 2 a-d and 3 a-d, along with the post-atomic-hydrogen treatment responses shown in red. To the detection limit of the system, the figures show that the surface oxides and carbon have been removed. (Note that the transfer between the XPS system and deposition chambers occurred at a background pressure of $\leq 2 \times 10^{-10}$ Torr.) It is apparent in these figures that not only was the non-bonded surface oxygen successfully removed, but the oxidized Pb, Sn, and Te were also chemically cleaned to remove oxygen. Furthermore, other cleaning experiments showed that maintaining a TC substrate temperature of 140° C for 40 min while exposing the sample surface to the atomic hydrogen flux was sufficient to clean the surface.

Various metals have been investigated in the literature for use as electrical contacts with Pb-based devices such as lasers, detectors, and thermoelectrics, including Pt,

Au, Sn, Zn, Pb, In, Ag, Ti, Cr, Sb, W, Ni, Fe, Cu, Al, and Ge [5-15]. In most cases the contact resistivity values were worse (higher) than $1x10^{-5}$ Ω-cm^2, although in one case [15] values as low as $2.3x10^{-8}$ Ω-cm^2 were reported for *n*-type samples; however, this exceptionally low value was not directly measured using the standard transfer length method (TLM) [1] but rather was inferred based on transient *ZT* measurements so the accuracy is uncertain. The results of these various studies seem consistent that the Fermi level at the surface of PbTe or $Pb_{1-x}Sn_xTe$ is not inherently pinned, but the results are inconsistent as to whether the metal-semiconductor interface behaves as an ideal Schottky barrier or exhibits deviations. However, since widely different metal deposition techniques (e.g., plating, evaporation, and sputtering) and varying surface preparation techniques were utilized in the above references, it is likely that the observed variation in results (specifically measured Schottky barrier height) could be attributed to the impact of different processing techniques on the electronic properties of the metal-oxide-semiconductor interface. In nearly all cases, the measured Schottky barrier height was less than that calculated [16] using the standard equation of the difference between the metal work function and electron affinity of PbTe (~4.6 eV [7,17]). (Note that image force barrier lowering [16] is typically ignored for PbTe because its impact is negligible: even for intrinsic electric fields as high as $1x10^6$ V/cm at the metal-semiconductor interface, the image force lowering is calculated to be less than 20 mV due to the extremely large static dielectric constant of PbTe, ~400 [18-20].)

Here, in concert with in situ atomic hydrogen cleaning, In, Ni/Au, Sn/Ni/Au, and Ti/NiAu metallization schemes were investigated with *n*-type materials (Table I) while Sn, Ni/Au, Pt/Au, and Ti/Ni/Au metallizations were investigated with *p*-type materials (Table II). Besides having low contact resistances, the metallization schemes also needed

to be robust at the nominal operating temperatures. The contacts were required to be robust in the sense that the contacts did not electrically degrade with time, were able to withstand ΔT's up to 300° C, bonded well to the material, and did not significantly diffuse into the thermoelectric material.

Contact Measurements

Tables I and II list the contact resistivities measured using the various metallization stack schemes applied to the atomic-hydrogen-cleaned *n* and *p*-type wafers respectively. The tables also include information on the layer structures of each of the thermoelectric materials used in this study, information on the atomic hydrogen cleaning process used in each case and comments about the stability and reproducibility of the contact resistance measurements.

The problem of producing *n*-type low resistance contacts on either 2×10^{18} or $4\text{-}6 \times 10^{19}$ cm^{-3} doped *n*-type PbTe contact layers was solved using either Sn/Ni/Au or Ti/Ni/Au contacts in conjunction with atomic hydrogen cleaning. In and Ni/Au contacts were found to be inferior in terms of resistivity and/or stability and/or temperature performance. Two *n*-type results using Sn/Ni/Au metallization are listed in Table 1 with *n*-PbTe contact layers doped to $n \sim 5 \times 10^{19}$ and 2×10^{18} cm^{-3}, respectively, and contact resistivity values of $\rho_c = 9.8 \times 10^{-6}$ and 6.3×10^{-6} $\Omega\text{-cm}^2$, respectively. It is not believed that the difference in contact resistivities was a result of the different doping levels, but rather simply due to process variability. However, the results do demonstrate that even with a lower-doped contact layer good contact resistivity can still be obtained with proper surface cleaning and metallization. The two *n*-type results using Ti/Ni/Au contacts on $4 - 6 \times 10^{19}$ cm^{-3} doped *n*-type PbTe after hydrogen cleaning proved to be stable, with 3.9 x

10^{-6} and 4.7 x 10^{-6} Ω-cm^2 contact resistivities respectively. Furthermore, the Ti/Ni/Au contacts worked consistently with ΔT's up to 400° C.

The results using the various metal schemes for forming low contact resistance contacts to the *p*-type materials are more interesting as compared to the *n*-type contact schemes. Ni/Au contacts after atomic hydrogen cleaning worked with mixed results on SnTe not intentionally doped (nid) contact layers (*p*-type, 1 x 10^{19} cm^{-3}) and SnTe:Na doped contact layers (*p*-type, 2 x 10^{20} cm^{-3}.) With the standard TLM masks, the contact resistances ranged from 4 x 10^{-6} to 4.9 x 10^{-4} Ω-cm^2. When the very small TLM mask was used with G-623-D, the 4 point probe contact resistances dropped to 1.6 to 3 x 10^{-6} Ω-cm^2. Within the confines of the limited data it appears that highly doped SnTe layers may produce better contacts with Ni/Au. On the other hand substrate and growth issues may also affect the results when comparing metallizations with the two differently scaled TLM masks. When one examines the series G-636-D-F one sees that the Ti/Ni/Au scheme out performs both the Ni/Au and Pt/Au schemes. Using the higher-temperature-compatible Ti/Ni/Au scheme on both *n* and *p*-type materials simplifies processing and potentially reduces device cost.

Proper passivation of the edge -sawed surfaces of the samples became an issue in the work. Without proper passivation, devices would run for only hours or several days before their output powers would begin to decrease. After observing the decreasing power for a period of time the devices would then fail. To alleviate this problem a plasma-deposited SiN_x coating was applied to the sidewalls of the devices.

Power Measurements

In order to measure the electrical power output of individual 100-μm-thick thermoelements, samples were metallized on both sides as discussed above, saw-cut to 1

mm^2 area, and placed between a Cu heater probe and Cu heat sink. A GaSn alloy liquid metal was used to coat both metallized surfaces to promote better thermal and electrical contact between the Cu surfaces and the metallized thermoelement surfaces. The Cu heater probe, thermoelement, and Cu heat sink were connected electrically in series to a load resistance (length of Ag coated Cu wire), and the power output was obtained as the square of the voltage across the load resistance divided by the load resistance. It is important to note that one of the two thermocouples used to establish ΔT were embedded in the copper rod just above the sample that produced T_{hot} and the second thermocouple was embedded in the T_{cold} heat sink just below the sample. The ΔTs recorded here are from the thermocouple measurements and the actual temperature difference across the sample is expected to be at least 8% lower than the ΔTs quoted due to additional temperature drops across interfaces. A more detailed description of the test apparatus is given in [21].

Unicouple devices were measured from wafers *n*-type G-580-C, *n*-type G676 and *p*-type G658 and plots of typical output powers vs. ΔT are shown in Figure 4. In the test of G-580-C Fig. 4(a) the load resistance was measured to be 3.2 mΩ and the resistance of the thermal element with contacts was expected to be 3.4 m Ω. V_{oc} was consistently slightly less than $2V_L$ for this device. This means that either the mobility of the sample is better than expected or that the contacts are better than expected from the TLM measurements. Optimized load matching continued to decrease during testing. This was probably due to the resistance of the actual thermal element increasing with temperature while the largest part of the load resistance remained cool. As shown in Fig. 4 (a) a power density of 11 W/cm^2 was obtained at a ΔT of 200° C. Note that in this sample the

carrier concentrations on each side of the wafer and the metallizations used were different (Table I).

Samples G-676 and 658 were tested without disconnecting the load to measure the open circuit voltages. It was difficult to not disturb the liquid metal contacts during the disconnect and reconnect procedures. Sample G-676 (Fig. 4 b) was measured in the test setup to have a resistance of 3 mΩ (including contacts) and an estimated load resistance of 4.4 mΩ. These values account for V_{oc} , as compared to V_L for this series of devices. Device outputs varied from 16 W/cm^2 to 33 W/cm^2 (3 samples) at thermocouple ΔT of 200 °C. Sample G658 (Fig. 4 c, *p*-type) was measured in the test setup to have a device resistance of 8 mΩ with a measured load resistance of 3 mΩ minus the contact resistance. This sample had one contact with poor adhesion and the adhesion problem most likely contributed to the higher device resistance. Even so, G 658 produced a power density of 12 W/cm^2 at a ΔT of 200° C.

Data from a preliminary test of the passivation coating, performed using G 676 devices with- and without the SiN_x coating is shown in Fig. 5. Each device was run for 18 days. As shown in the plot, the passivated device continued to perform well while the unpassivated device degraded. Although the passivated device appears to improve with time, the reason the output power increased was due to the ΔT drifting to a higher value over the course of the test. The data is encouraging, especially when coupled to the fact that the Ti/Ni/Au metal system continued to perform well with G676 devices run using ΔTs as high as 300°C (Fig. 4).

Discussion

The power densities reported here are approximately 5 X higher than our previous best results [21]. We attribute the improvement solely to improved contact resistivities, because the power factors ($=S^2\sigma$) of the samples reported in this report are not better than those in the previous work. We also note that the since the matched load resistance is so low for individual thermoelements (3-4 mΩ), accurate measurement of the load resistance is thus critical for accurate power determination. The problem is that even with our commercial micro-Ohm meter, the load resistance (which includes the contacts, connections and load wire) is difficult to separate fully from the intrinsic sample resistance. On the other hand, better load matching is expected to further improve device performance.

Ti/Ni/Au contacts applied in situ just after atomic hydrogen cleaning performed well with low contact resistances on *n*-type samples. Ni/Au contacts applied with the same cleaning procedure worked well from a resistivity standpoint on Na doped (*p*+) SnTe contact layers but not as well on nid (*p*+) SnTe contact layers. Ti/Ni/Au contacts out performed Ni/Au on nid (*p*+) SnTe contact layers and were demonstrated to produce a p-type device with reasonable power output. Furthermore, there was one experiment performed that indicated that Ni/Au with the small TLM mask produced much better resistivity results than the same metals on the same material (*p*+) with the large TLM mask. Although this preliminary study shows significant power improvements from individual devices as compared to past results, it also raises more materials questions than it answers. Theoretical work on the intermixing (thermodynamics) of the materials at the contact/semiconductor interface should be performed to further understand stability and

contact resistivity issues over long periods of time. An improved test apparatus should also be developed to more easily measure both load and open circuit voltages.

Summary

Significant electrical output powers have been achieved using both n- and p-type PbTeSe thermoelectric devices with Ti/Ni/Au contacts applied using a combination of *in-situ* atomic hydrogen cleaning and *in-situ* metallization. These contacts appear stable at ΔTs as high as 300° C and, using n-type material have been run as high as 400° C. The low contact resistance procedures developed here are expected to be applicable to other thermoelectric materials, thereby reducing the total amount of material required to produce devices with high power outputs. Furthermore, since no masking is required, the contacting process is scalable for high throughput.

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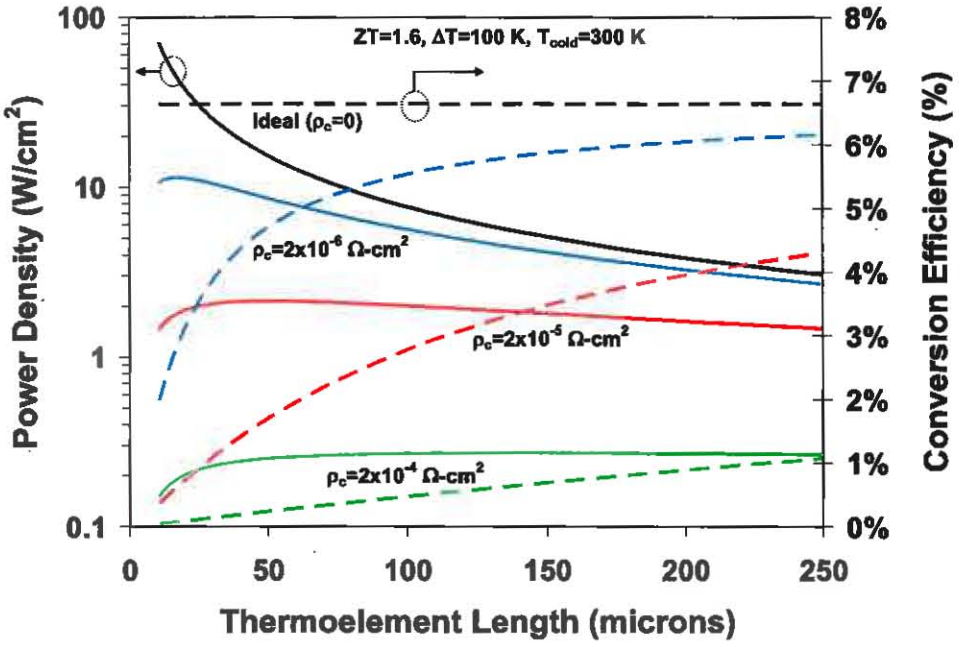

Figure 1 Calculated curves illustrating deleterious impact of contact resistivity on thermoelectric module performance. In order to take advantage of high-*ZT*, Pb-salt-based thermoelectric materials with very low contact resistivity values are required. Solid curves are electrical power density, dashed curves are total system conversion efficiency (including Carnot).

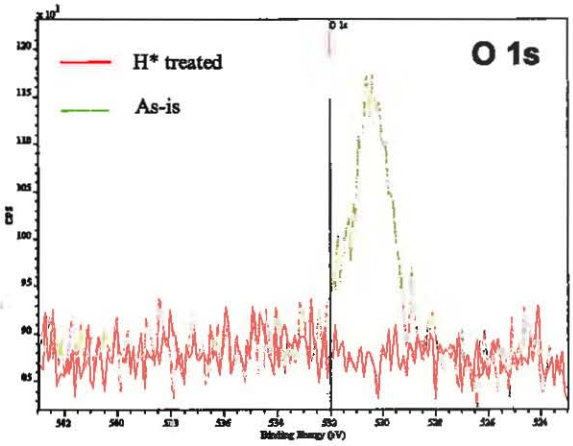

Figure 2(a)

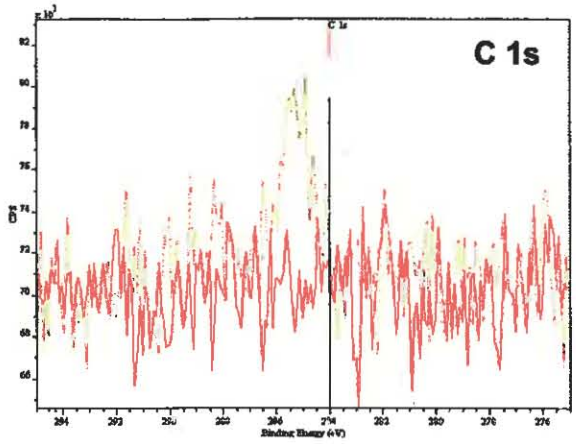

Figure 2(b)

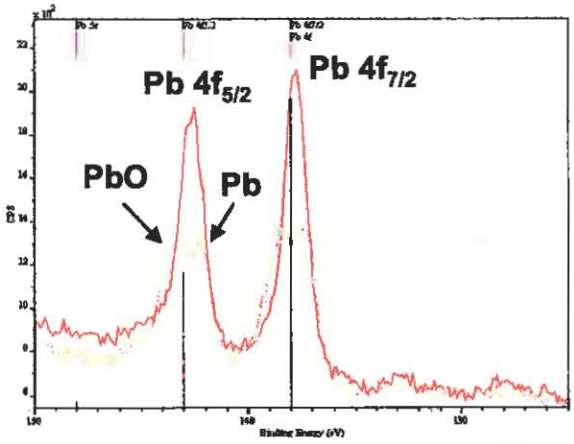

Figure 2©

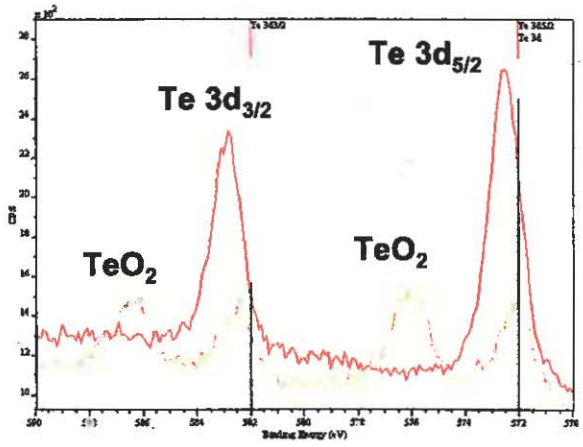

Figure 2(d)

Figure 2: XPS spectra of as-received (green) and atomic-hydrogen-treated (red) PbTe surfaces, illustrating the impact of atomic hydrogen cleaning on: (a) adsorbed oxygen, (b) adsorbed carbon, (c) Pb and PbO, and (d) Te and TeO_2. Atomic hydrogen cleaning in vacuum of a sample at 200 °C (as well as 140 °C, not shown) successfully removed deleterious oxides and carbon.

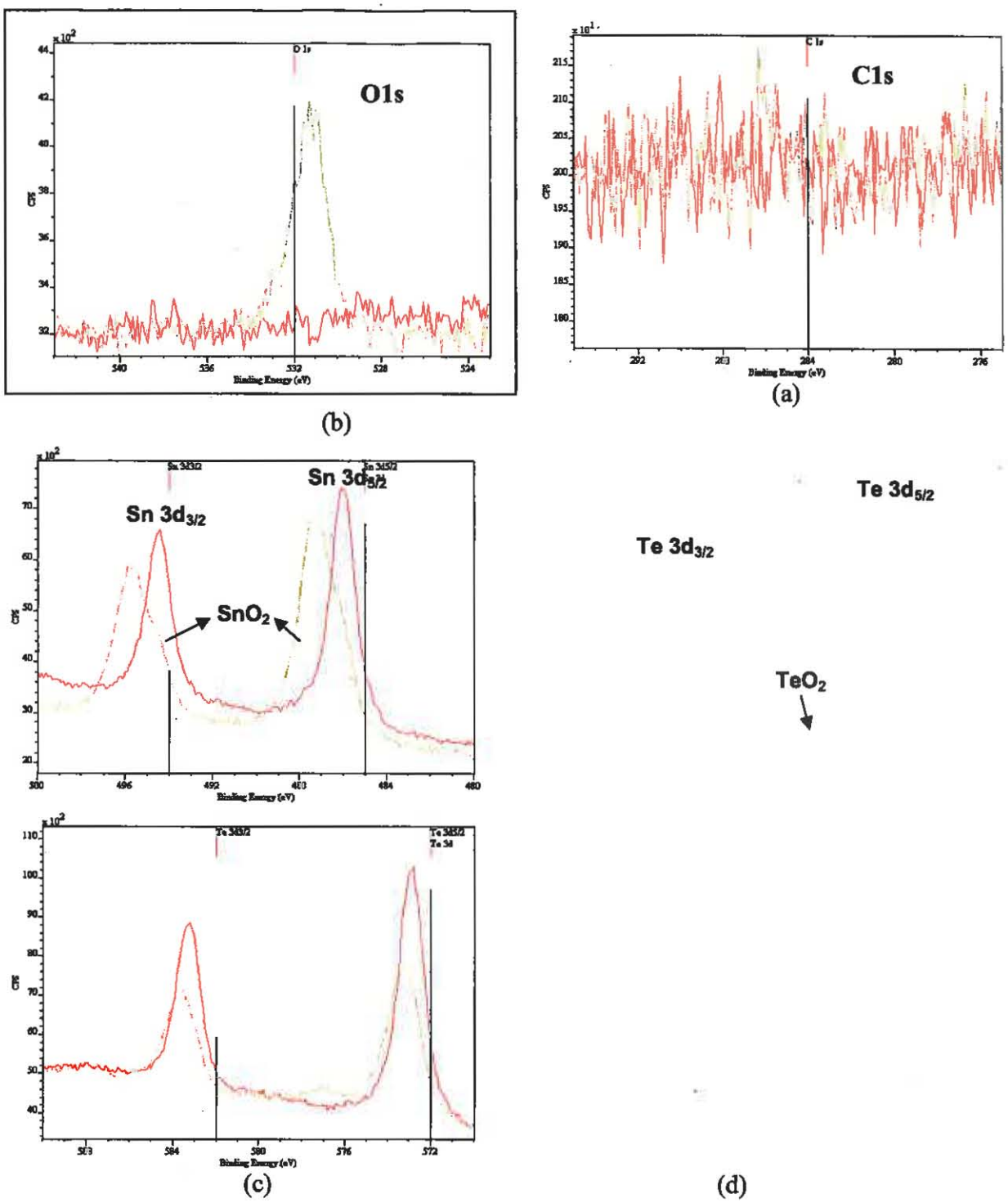

Figure 3: XPS spectra of as-received (green) and atomic-hydrogen-treated (red) SnTe surfaces, illustrating the impact of atomic hydrogen cleaning on: (a) adsorbed oxygen, (b) adsorbed carbon, (c) Sn and SnO, and (d) Te and TeO_2. Atomic hydrogen cleaned at a substrate temperature of approximately140 °C.

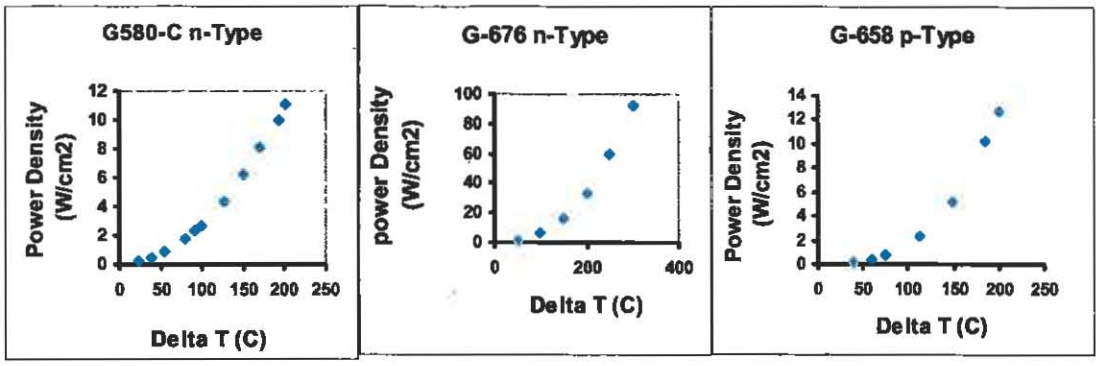

Figure 4: Power densities measured from 1 mm x 1mm devices in cross-plane configuration. Load resistance values taken to be 3.15 mΩ, 5.8 mΩ and 5.8 mΩ for G580, G676 and G658 respectively.

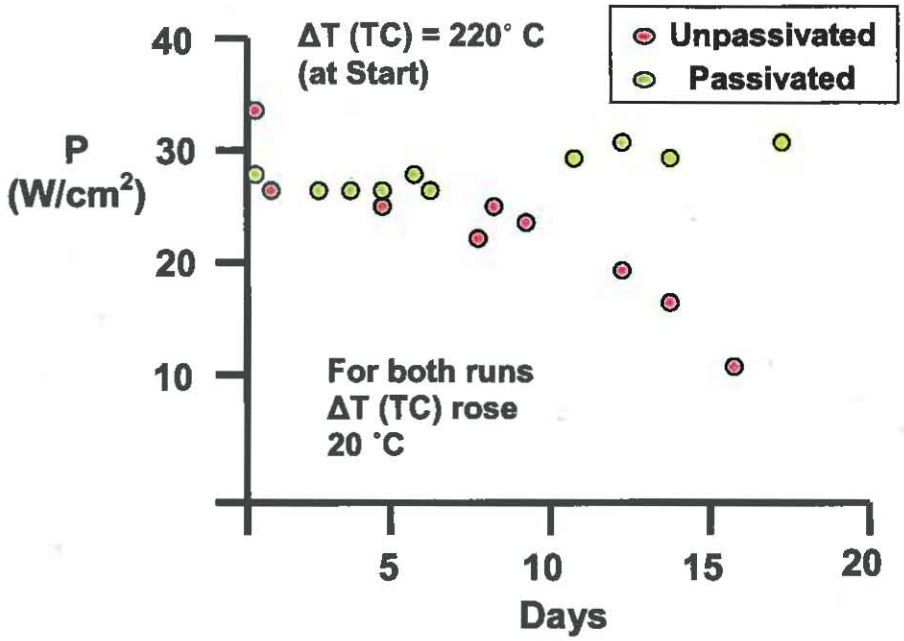

Figure 5: Power data from SiO_x passivated and unpassivated G-676 devices (n-type, 100-μm-thick). A value of 4.4 mΩ was used for the load resistor in the power calculations. The heater was not PID controlled and ΔT varied up to 10° C from data point to data point.

Table I. Summary of various metal stacks and atomic hydrogen cleaning procedures studied to improve n-type contact resistivity.

Sample	Cleaning Technique and Structure	Metal stack	ρ_c (Ω-cm^2)	Notes
G-551-A n-type	40 min atomic H, 140 °C 100 nm PbTe:Bi 6E+19 n++ 6μm PbTe:Bi 1E+19 n+ 100 nm PbTe:Bi 6E+19 n++ Polished BaF2 substrate	1 μm In	1.6×10^{-2} 4 pt method	In too soft, poor mechanically
G-561-A n-type	40 min atomic H, 140 °C 100 nm PbTe:Bi 6E+19 n++ 6μm PbTe:Bi 1E+19 n+ 100 nm PbTe:Bi 6E+19 n++ Polished BaF2 substrate	200 nm Ni /100 nm Au	$\sim1\times10^{-4}$ 4 pt method	Scatter in TLM data, poor measurement repeatability
G-561-B n-type	60 min atomic H, 200 °C Structure – see G-551-A	200 nm Ni / 100 nm Au	1.5×10^{-4} 4 pt method	Some scatter in TLM data, poor measurement repeatability, better adhesion than 561-A
G-561-C n-type	60 min atomic H, 140 °C Structure – see G-551-A	500 nm Sn /2 μm Ni / 100 nm Au	9.8×10^{-6} 4 pt method	Very linear data, excellent measurement repeatability
G-561-D n-type	40 min atomic H, 140 °C Structure – see G-551-A	200 nm Ti/ 100 nm Ni/ 200 nm Au	3.9×10^{-6} 4 pt method	Excellent repeatability
G-580-C n-type NDSL	In-Situ Sn/ 60 min 140°C 100 nm PbTe:Bi 6E+19 n++ 100 μm PbTeSe 2E+18 n+ 100 nm PbTe:Bi 2E+18 n+ Polished BaF2 substrate	**Side A:** 5 μm Sn **Side B:** 500 nm Sn /1.5 μm Ni /100 nm Au	Device Wafer	$\Delta T = 220°C$ $P = 10$ W/cm^2
G-581 n-type	60 min atomic H, 140 °C 6μm PbTe:Bi 2E+18 n+ Polished BaF2 substrate	500 nm Sn /2 μm Ni / 100 nm Au	6.3×10^{-6} 4 pt method	Excellent measurement repeatability and stability
G-613-A n-type	40 min atomic H, 140 °C? 100 nm PbTe:Bi 4E+19 n++ 5μm PbTe:Bi 4E+18 n+ 500 nm PbSe:Bi nid Polished CaF2 substrate	200 nm Ti/ 200 nm Ni/ 200 nm Au	4.7×10^{-6} 4 pt method	Good adhesion and Resitivity. Works up to 400° C
G-676 n-type NDLS	40 min atomic H, 140 °C-both sides 150 nm PbTe:Bi 5E+19 n++ 100μm PbTeSe 3.5E+18 n+ 150 nm PbTe:Bi 5E+19 n++ Polished BaF2 substrate	**Both sides:** 200 nm Ti/ 200 nm Ni/ 200 nm Au	Device Wafer	$\Delta T = 220°C$ $P = 30$ W/cm^2

Table II. Summary of various metal stacks and atomic hydrogen cleaning procedures studied to improve p-type contact resistivity.

Sample	Cleaning Technique and Structure	Metal stack	ρ_c (Ω-cm^2)	Notes
G-531 p++ surface	40 min atomic H, 140 °C 100 nm SnTe:Na 2E+20 p++ 5-6 µm PbTe:Na 1E+19 p+ 100 nm SnTe:Na 2E+20 p++ 0.8-1.5 nm Te:Na > 1E+19 wetting layer Polished BaF_2 substrate	50 nm Ni/ 150 nm Au	4×10^{-6} 4pt method	100-nm-thick SnTe layer P= 3×10^{20} cm^{-3}
G-539 p+	MBE in situ Sn 0.5 µm Sn Monolayer Te cap 100 nm PbSe:Na 2E+20 p++ 5-6µm PbSe:Na 1E+19 p+ 100 nm PbSe:Na 2E+20 p++ 0.8-1.5 nm Te:Na >1E+19 wet layer Polished BaF_2 substrate	Thick Sn	2.0-8.0 $\times 10^{-5}$ **Etched large TLM Ladders** 4 pt method	100-nm-thick PbSe contact layer 2×10^{20} cm^{-3} ???
G-623-D	40 min atomic H, 140 °C 200 nm SnTe nid 5µm PbSe:Na 1E+19 200 nm SnTe 1E+19 nid p++ 500 nm p-PbSe:Na 2E+19 Polished CaF_2 (111)substrate	50 nm Ni/ 150 nm Au	4.9×10^{-4} 4pt method Small TLM ladders: $1.6\text{-}3 \times 10^{-6}$ 4pt method	Stable and reproducible contacts
G-623-F	60 min atomic H, 140 °C Structure – see G-623-D	500 nm Ni/ 100 nm Au	9.3×10^{-5} 4pt method	Stable and reproducible contacts
G-636-C p+	40 min atomic H, 140 °C 100 nm SnTe nid 6µm PbSe:Na 1E+19 p+ 100 nm SnTe nid 500 nm p-PbSe 2E+19 Polished CaF_2 (111)substrate	100 nm Ni/ 150 nm Au	5.4×10^{-5} 4pt method	Stable and reproducible contacts
G-636-D p+	40 min atomic H, 140 °C Structure – seeG-636- C above	100 nm Pt/ 100 nm Au	7.7×10^{-5} 4pt method	Stable and reproducible contacts
G-636-F p+	40 min atomic H, 140 °C Structure – see G-636-C above	200 nm Ti/ 100 nmNi/ 200 nm Au	2.3×10^{-5} 4pt method	Stable and reproducible contacts
G-658 p-type NDSL	40 min atomic H, 140 °C-both sides 100 nm SnTe nid 1E+19 p++ 80µm PbTeSe 1E+19 p+ 100 nm SnTe nid p++ Polished BaF_2 substrate	**Both sides:** 200 nm Ti/ 100 nm Ni/ 200 nm Au	Device Wafer	$\Delta T = 220$°C P = 10 W/cm^2