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Pascale M. Gouker, Brian Tyrrell, Matthew Renzi, Chenson Chen, Peter Wyatt, Jonathan R. Ahlbin, Stephanie Weeden-Wright, Nick M. Atkinson, Nelson J. Gaspard, Bharat L. Bhuva, Lloyd W. Massengill, Enxia Zhang, R. Schrimpf, and Matthew J. Gadlage

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MIT Lincoln Laboratory
244 Wood Street
Lexington, MA 02420

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SET Characterization in Logic Gates Circuits Fabricated in a 3DIC Technology

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***Abstract* – Single event transients are characterized for the first time in logic gate circuits fabricated in a novel 3DIC technology where SET test circuits are vertically integrated on three tiers in a 20-µm-thick layer. This 3D technology is extremely well suited for high-density circuit integration because of the small dimension the tier-to-tier circuit interconnects, which are 1.25-µm-wide through-oxide-vias. Transients pulse width distributions were characterized simultaneously on each tier during exposure to krypton heavy ions. The difference in SET pulse width and cross-section between the three tiers is discussed. Experimental test results are explained by considering the electrical characteristics of the FETs on the 2D wafers before 3D integration, and by considering the energy deposited by the Kr ions passing through the various material layers of the 3DIC stack. We also show that the back metal layer available on the upper tiers can be used to tune independently the nFET and pFET current drive, and change the SET pulse width and cross-section. This 3DIC technology appears to be a good candidate for space applications.**

***Index Terms*—single event transient, SOI, fully depleted, 3D technology, heavy ions, single event effects**

I. Introduction

New technologies exploiting the three-dimensional stacking of integrated circuits are actively explored in R&D laboratories and the industry as a way to increase circuit density and improve system performance. Figure 1 shows the cross-section of MITLL 3DIC circuits where three FDSOI CMOS circuit tiers are integrated [1]. Tier-to-tier interconnection is achieved with 1.25-µm-diameter 3D vias. The vertical integration of 3DIC is accomplished entirely using wafer-based CMOS fabrication techniques. This approach is attractive because short electrical interconnects improve speed and bandwidth; and 3DIC approaches can integrate circuits fabricated with heterogeneous materials and processes as previously demonstrated [2,3,4,5]. For those 3DIC, an energetic particle can easily pass through the transistors in all three tiers because the total three tier thickness is 20 µm. As shown in Figure 1, the particle will travel through multiple layers including aluminum-copper, silicon dioxide, polysilicon, tungsten (contact, vias) and silicon, before reaching the bottom tier. As a result, the ion energy and the amount of energy deposited are expected to be different for each tier. We have shown previously that the 3D integration process did not affect the characteristics of the devices and circuits fabricated on the individual 2D circuit wafers [5]. Single event effects in such 3DIC are yet to be reported.

In this work, we report on the characterization of single-event effects induced by heavy ions in 3DIC logic gate circuits fabricated in MITLL 3DIC technology. To the authors knowledge, this is the first time that single event transient pulse widths are measured independently on circuits fabricated on three tiers. We show how the back gate metal layer, available on tiers 2 and 3, can be used to characterize SETs and control the SET pulse width. Implication for the design of SET-free circuits is discussed. Monte Carlo simulations were performed to analyze the effects tungsten contacts and vias had on tier-to-tier energy deposition.

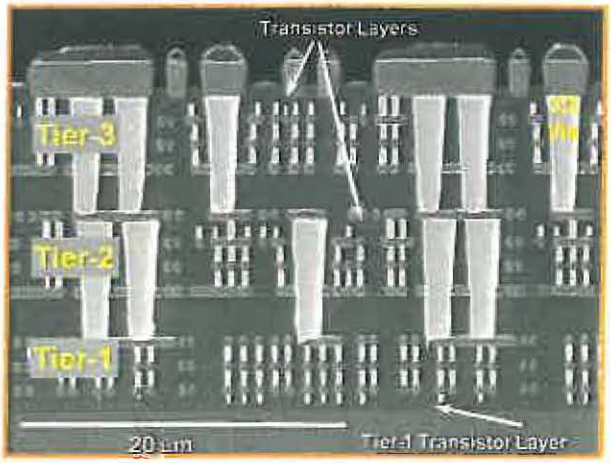

Figure 1: Scanning Electron Micrographs of a 3DIC wafer with three FDSOI CMOS tiers, eleven metal interconnect layers, and 3D vias interconnecting tiers 1. 2 and 3.

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Pascale Gouker, , MIT Lincoln Laboratory, Advanced Silicon Technology Group, L-304, 244 Wood Street, Lexington, MA 02420, USA. Phone:781-981-0460,fax:781-981-7889, email:pgouker@ll.mit.edu
Brian Tyrrell, Matt Renzi, Chenson Chen, and P. Wyatt, are with MIT Lincoln Laboratory, Lexington, MA 02420, USA
Jonathan R. Ahlbin, Stephanie Weeden-Wright,, Nick M. Atkinson, Nelson J. Gaspard, Bharat L. Bhuva, Lloyd W. Massengill, R. Schrimpf, and Enxia Zhang are with Vanderbilt University, Nashville, TN, 37235 USA
Matthew J. Gadlage, NAVSEA Crane, IN, 47522, USA

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II. 3DIC Fabrication Process

The three-tier integrated circuits characterized in this work were fabricated at MIT Lincoln Laboratory in the third DARPA-sponsored 3D multi-project run (3DM3). The 3D process begins with fabricating three individual fully depleted SOI (FDSOI) CMOS wafers, and with a 150-nm FET gate length, 40-nm-thick SOI active layer, a 400-nm buried oxide (BOX), a dual threshold CMOS, Co-silicided poly gate and a silicide block layer, and three metal interconnect layers. The circuits were designed using standard logic design rules. Specific alignment structures were added to the lithographic masks to enable accurate tier-to-tier alignment (<+/- 0.75 μm). 3D integration follows, beginning with oxide-oxide bonding of tier 1 and tier 2 wafers. Tier 2 substrate is then removed by grinding and wet chemical etching, stopping on the tier 2 BOX layer. Electrical interconnection is formed by back vias to tier 2, 3D vias from tier-1 to tier 2, and a tier 2 back metal layer. The process is then repeated, bonding and interconnecting a tier 3 wafer to a tier 1, 2 stack to form a three-tier stack [1]. Figure 2 shows an illustration of a 2D and 3D integrated circuit cross-section. Figure 3 shows a photograph of a 150-mm wafer after the 3D integration is complete.

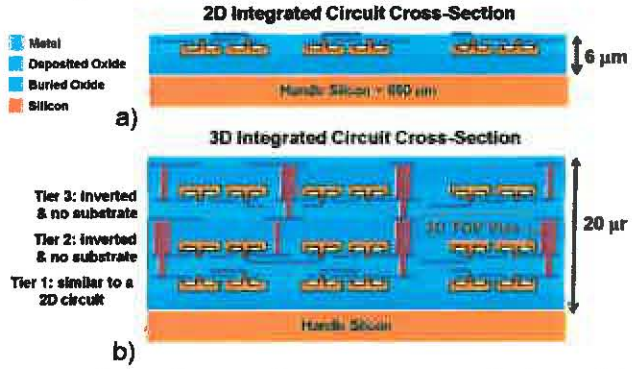

Figure 2: Illustrated cross-section of a) a 2D integrated circuit and b) a 3DIC wafer with three FDSOI CMOS tiers, eleven metal interconnect layers, and 3D Though Oxide Vias (TOV) interconnecting tiers 1, 2 and 3.

The 3DIC technology includes three FDSOI circuit tiers, eleven interconnect-metal layers, and dense unrestricted 1.25-μm diameter 3D vias to interconnect stacked circuit layers. Upon completion of single tier fabrication and again after 3D integration, an extensive series of tests is performed to characterize transistor and circuit performance to monitor the effect of wafer integration. Figure 4 shows $I_{drain}(V_{gate})$ curves at V_{drain} = 1.5 V for W=8 μm, L=0.15 □m transistors on tiers 1, 2, & 3 after 2D fabrication and after 3D integration. The transistor $I_{drain}(V_{gate})$ characteristics for tiers 1, 2, & 3 were shown to be essentially unchanged by the 3D integration process.

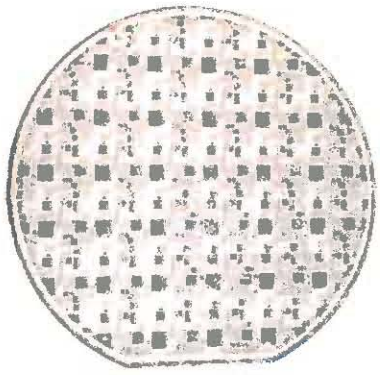

Figure 3: Photograph of a 150-mm wafer after 3D integration is completed.

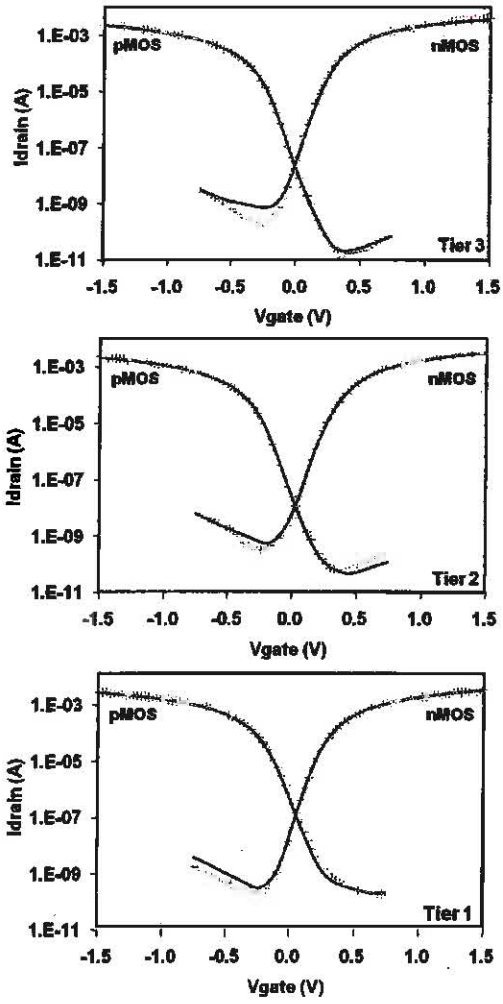

Figure 4: $I_{drain}(V_{gate})$ curves at V_{drain} = 1.5 V for W=8 μm, L=0.15 μm FETs on tiers 1, 2, & 3 before (symbols) and after (solid line) 3D integration.

III. 3D SET Test Circuit Design and Testing

A 3D IC was fabricated with an SET characterization testchip on each tier. An illustrated cross-section of the 3DIC is shown in Figure 5. The SET test circuits on tier 3, tier 2 and tier 1 are located 2,600 nm, 9,900 nm and 20,350 nm below the passivation surface. The testchip design was based on the autonomous pulse-width measurement technique described in [7]. The ion collector or target circuit consists of chain of minimum sized inverters with 4 blocks of 200 inverters each connected with OR gates with no body ties. SETs generated in the inverter chain then propagate through a series of latches where the SET width is measured in terms of latch delays. In the 3D SOI design, one measurement circuit and corresponding target circuit were instantiated on each tier. With an individual latch stage delay of about 120 ps and 25 latch stages, this circuit allows measurement of SET pulses ranging from 120 ps to 3 ns with a 60-ps measurement resolution. The test structure is designed such that only SETs created in the target inverter circuit are measured, and ion hits in any other part of the circuit are not measured. Additionally, for the testchip on tier 2, a back metal layer (see Figure 1) was designed on the back of nFET and the pFET in the target inverter circuit. This back metal layer is separated from the active body of the FET by 600 nm of oxide. It is used as a secondary gate to control independently the threshold voltage of the nFETs and pFETs. 3D tungsten-filled vias are used to interconnect the bottom tiers, *i.e.,* tiers 1 and 2, to the pads on the top level, and they are all more than 200 μm away from the active circuitry.

Heavy-ion broadbeam testing of the fabricated 3D SOI SET test circuits was performed at Lawrence Berkeley National Laboratory with the 16 MeV ion cocktail using krypton (Kr) at normal incidence and in air. The LET of the incident particle was 25 MeV-cm^2/mg. For all results presented in this paper, the angle of incidence and particle energy were kept constant. Note that the penetration depth of Kr is much deeper than 20 μm, which is the total thickness of the 3D stack [8]. SET data were collected at incremental fluences of 1x10^8 cm^{-2} simultaneously on all three tiers.

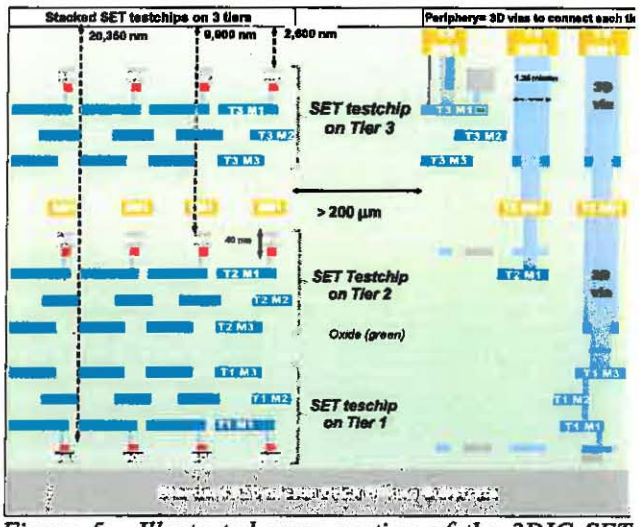

Figure 5: Illustrated cross-section of the 3DIC SET test circuit. There are three independent SET test circuits on each tier capable of collecting SETs and measuring their width. There is also a back-metal layer on the back of the nFET and pFET in the inverter chain collecting SETs on tier 2 and tier 3 (a separate back-metal layer for each FET type).

IV. Experimental Results and Discussion

SET cross-sections: Figure 6 shows the distribution of SET pulse widths measured on the testchips on tiers 1, 2 and 3. For tiers 2 and 3, the median SET pulse width is ~ 7 latches (or ~ 840 ps). It is ~ 5 latches (or ~ 600 ps) for the bottom tier 1. For all three tiers, the SET width has a broad distribution. We know from previous work [9,10,11] that transient signals generated in 180-nm FDSOI FETs can be very narrow (< 200 ps). However, these transient signals broaden as they propagate through a chain of inverters, and the transient widths measured at the output of the chain have a broad distribution.

The SET widths measured for the 3DIC testchips are consistent with earlier results published for single tier circuits for the 180-nm FDSOI technology (in this work the gate length is 150 nm) [12]. In this earlier work, we have shown that, if the inverter chains have floating body FETs, almost all of the measured SETs are broadened from their initial width. As a result, the average measured SET width for floating-body circuits is not an average of the generated SET width, but rather an average of the generated plus broadened SET width. In other words, the average SET width has been skewed by the broadening. Figure 6 shows that the SET pulse width distribution is similar on tier 2 and 3, but skewed toward narrower SETs on tier 1. Also, while the SET cross-section is comparable on tier 1 and 2, it is 60% higher on tier 1. These results are discussed in Section V.

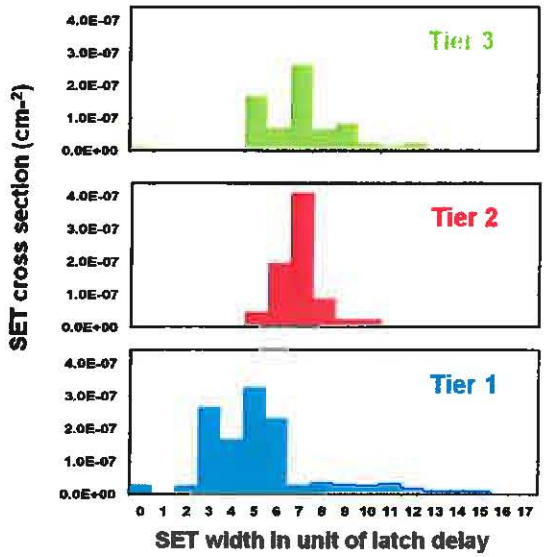

Figure 6: Distribution of the SET pulse widths in units of latch delay measured at normal incidence in air with a 25 MeV-cm^2/mg ion. Data shown for each tier of the 3D stack [tier 1 (bottom), tier 2 (middle) and tier 3 (top) for a ion fluence of 1x10^8 /cm^2. Upset cross-section is 1.22x10^{-6}, 7.74x10^{-7} and 7.31x10^{-7} cm^2 for the circuits on tier 1, 2 and 3, respectively.

Back metal gate effect: One of the key features of the 3D SOI process is that a back metal layer can be added on the backside of the n and pFETs, behind the body region, on tier 2 and 3. This is because both tier 2 and tier 3 are inverted during 3D integration, and the Si substrate is removed from both tiers. In contrast, tier 1, which is not inverted, has a silicon substrate below the BOX. There is a 600-nm thick oxide between the back metal layer and the active SOI on tier 2 and 3, therefore applying a bias voltage on the back metal gate changes the threshold voltage of the SOI FET located below it. We designed two separate back metal gates so that one would bias all the nFETs and the other would bias all the pFETs in the inverter chain of the SET collecting circuit. Figure 5 shows an illustration of the back metal lines over the nFETs and pFETs on tier 2. During heavy ion testing, the back metal bias voltage, V_{BG}, of the pFETs and nFETs transistors was changed independently. V_{BG} was set to 0. -15 V, and – 20 V for the pFETs. V_{BG} was set to 0. +15 V, and + 20 V for the nFETs.

Figure 7 shows the SET pulse widths in units of latch delay for different V_{BG} voltages applied to the FETs on tier 2. The data corresponding to V_{BG} = 0 V for the pFET and nFET on Figure 7a and Figure 7b (*i.e.*, pFET 0 / nFET 0) are the same data as those shown in Figure 6 for tier 2. When a negative bias voltage is applied to the back of the pFET, or a positive bias voltage is applied to the nFET, or a bias voltage is applied to both FET types at the same time, the SET distribution changes significantly. Note that the latch delay remains constant when V_{BG} is changed because V_{BG} affects only the nFETs and pFETs in the SET collecting circuit, not in the latch circuit. These results indicate that the back metal gates can be used to characterize SETs as discussed in the next section V.

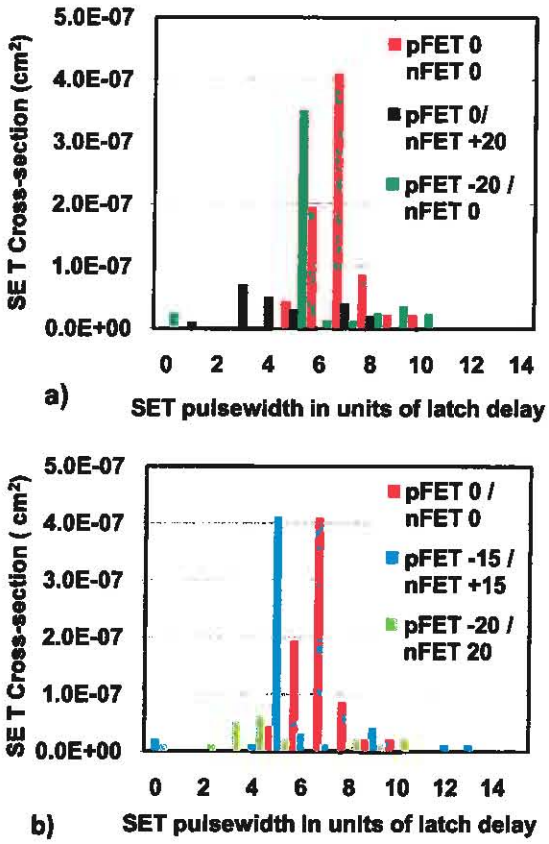

Figure 7: Experimental results at normal incidence in air with a 25 MeV-cm^2/mg ion showing the SET pulse widths measured on tier 2, for different back gate bias voltages, V_{BG}, for the nFETs and pFETs in the inverter chain collecting SETs. "pFET 0 / nFET 0" refers to V_{BG} =0 V for both the nFETs and pFETs. The ion fluence was 1x10^8 /cm^2. In a) V_{BG} is applied to the pFETs or the nFETs, the other voltage remaining at 0 V. In b) V_{BG} is applied simultaneously to the nFET and pFETs .

V. Discussion

SET cross-sections: The heavy ion test data shown in Figure 6 revealed that the SET pulse width distribution on tier 1 is skewed compared to that on tier 2 and 3. In addition, the SET cross–section is higher on tier 1 than on the two upper tiers. To explain these results, we first compared the electrical characteristics of the transistors on each tier; then we performed

simulations to characterize the energy deposited by the Kr ions travelling through the 3DIC layers.

The same process flow was used to fabricate the three 2D FDSOI CMOS wafers used for the 3D integration, however the three wafers were not fabricated in the same lot, and the SOI wafer used on tier 1 was different from the one used on tier 2 and 3. The substrate on tier 1 was fabricated at MITLL, and had buried oxide engineered for radiation tolerance. Lot-to-lot process variations and differences in the starting SOI substrate will yield wafers where the nFETs and pFETs have slightly different characteristics. Figure 8 shows the $I_{drain}(V_{gate})$ of nFET and pFET on tier 1, 2 and 3. These are the same curves shown in Figure 4, which we superimposed on the same plot. The I(V) curves are similar for the FETs on tier 2 and 3, but different on tier 1. As shown in Figure 4, this is not attributed to the 3D integration process. The difference in the characteristics for the pFETs, and to a lesser extend the nFET, on tier 1 compared to tier 2 and 3 are attributed to the difference in the starting SOI wafer used for the 2D circuit fabrication and variations in Critical Dimension (CD) during circuit fabrication. Different FET electrical characteristics (drive current, threshold voltage, parasitic bipolar gain, etc…) will yield different inverter response, consequently the SET pulse broadening rate is expected to be different on tier 1 compared to tier 2 and 3 [13,14,15]. The pFETs have a lower threshold voltage, and a larger drive current on tier 1 compared to that on tier 2 and 3. This is consistent with narrower SET pulse width and lower broadening rate on tier 1 compared to those on tier 2 and 3 as reported in Figure 6. The heavy ion test is not sufficient to confirm whether the initial pulse width is narrower or whether the broadening rate is smaller.

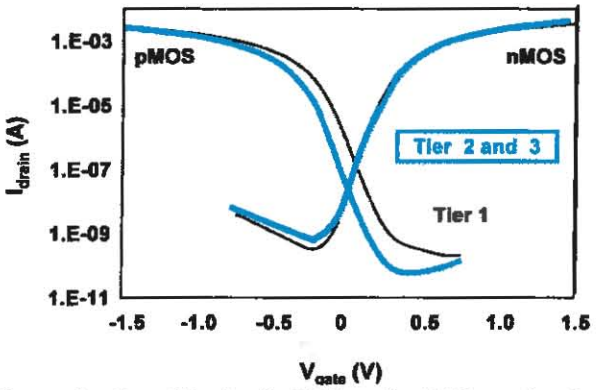

Figure 8: $I_{drain}(V_{gate})$ of nFET and pFET on tier 1, 2 and 3. The difference in the characteristics for the pFETs are attributed to the difference in the starting SOI wafer used for the 2D circuit fabrication and CD variations during fabrication.

The difference in pulse width distribution between tier 1 and 2 and tier 3 could also be due to a difference in the energy deposited by the Kr ions as they go through the 3D layer stack. Simulations were performed using the Monte Carlo Radiative Energy Deposition (MRED) code [16]. MRED is a simulation tool that calculates the energy deposited by radiation in microelectronic devices based on the Geant4 libraries [17]. Howe et al [18] successfully used MRED simulations to show that CMOS circuits can have different SEU error rates if the circuit layers contain high Z materials compared with direct ionization by the primary ion alone. 16-MeV/amu Kr ions were randomized over a plane normal to target. Simulations were run to compare the energy deposited by the Kr ions in the sensitive volume of the FET on tier 1, 2 and 3. Figure 9 gives a description of the layers (material and depth) that matched the 3DIC process and that were used for the simulations. The thickness of tungsten layer was calculated by looking at the fractional area of the contact and via by the depth with respect to the sensitive area.

	Layer Name	MRED Material	Depth (nm)
Tier 3	Al-Cu (Cu < 0.5%)	Aluminum	2000
	SiO_2	SiO_2	600
	Sensitive Detector	Silicon	40
	M1-Active Contact	Tungsten	19.23
	Co-silicided Poly	Silicon	150
	M1-Poly Contact	Tungsten	10.42
	SiO_2	SiO_2	800
	Metal 1 (M1)	Aluminum	630
	M1-M2 Via	Tungsten	16.03
	SiO_2	SiO_2	1000
	Metal 2 (M2)	Aluminum	630
	SiO_2	SiO_2	1000
	Metal 3 (M3)	Aluminum	630
	SiO_2	SiO_2	2100
Tier2	Back Gate Metal	Aluminum	630
	SiO_2	SiO_2	600
	Sensitive Detector	Silicon	40
	M1-Active Contact	Tungsten	19.23
	Co-silicide Poly	Silicon	150
	M1-Poly Contact	Tungsten	10.42
	SiO_2	SiO_2	800
	Metal 1 (M1)	Aluminum	630
	M1-M2 Via	Tungsten	16.03
	SiO_2	SiO_2	1000
	Metal 2 (M2)	Aluminum	630
	SiO_2	SiO_2	1000
	Metal 3 (M3)	Aluminum	630
	SiO_2	SiO_2	2100
Tier 1	Metal 3 (M3)	Aluminum	630
	SiO_2	SiO_2	1000
	Metal 2 (M2)	Aluminum	630
	SiO_2	SiO_2	1000
	M1-M2 Via	Tungsten	16.03
	Metal 1 (M1)	Aluminum	630
	SiO_2	SiO_2	800
	M1-Poly Contact	Tungsten	10.42
	Co-silicide Poly	Silicon	150
	M1-Active Contact	Tungsten	19.23
	Sensitive Detector	Silicon	40
	SiO_2	SiO_2	400
	Substrate	Silicon	10 um

Figure 9: Description of the layers used to simulate the energy deposited by 16-MeV/amu Kr ions with MRED. The layers match the materials and thickness of the SET collecting circuit.

To evaluate the effects of having tungsten (high Z material) in the contacts and vias, another simulation was run as a control case replacing contacts and vias with oxide.

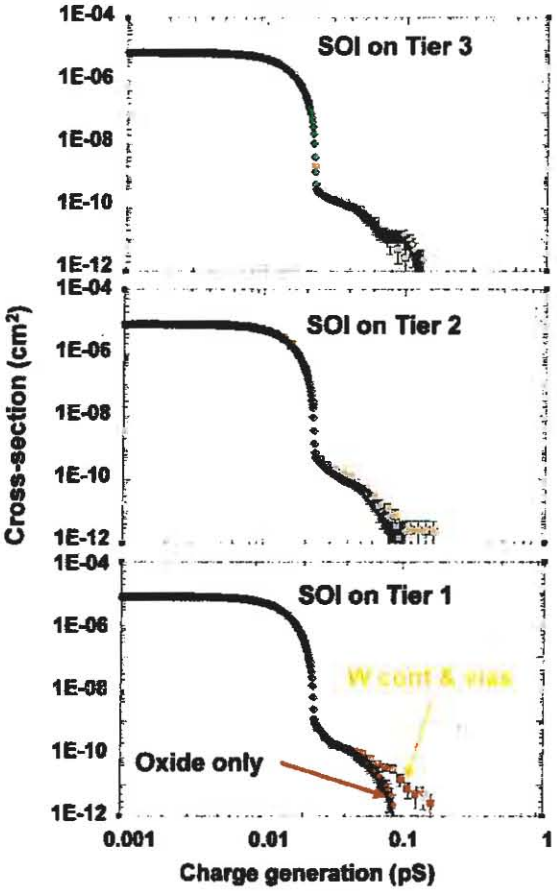

Figure 10: Results from MRED simulations showing the cross-sections versus the charge generated by 16 MeV Kr ions in the sensitive SOI device layer of an inverter in tier 1, 2 and 3 of the 3DIC SET test circuit. Results are also shown for a control case where the tungsten (W) contact and vias were replaced by SiO_2.

Comparing the oxide-only and the W contact and vias simulations indicate that the presence of the tungsten layers increased the amount of energy deposited in the sensitive devices on tier 1 only. The bottom tier is the only tier where the tungsten contacts and vias are immediately located *above* the sensitive SOI volume. As illustrated in Figure 5, the tungsten is located *below* the sensitive SOI volume on tier 2 and 3. These results indicate that circuits on tier 1 may be more sensitive to transients because of the close proximity of the contacts and vias above the sensitive device volume. This is maybe why the experimental data in Figure 6 show a higher SET cross-section for the test circuit on tier 1 compared to tier 2 and 3.

Back metal gate effect: Figure 11 shows $I_{drain}(V_{gate})$ curves for L=150-nm FDSOI pFETs and nFET, and the effect of varying the back metal gate voltage, V_{BG}. To understand the experimental results, one should consider three cases. In the first case, V_{BG} for the pFET transistors was varied from 0 V to -20 V, which has the effect of decreasing the threshold voltage, thereby increasing the drive current of all the pFETs in the inverter chain. As a result of the increased pFET restoring current, SETs generated in nFETs are expected to become narrower. In the second case, V_{BG} for the nFET transistors was varied from 0 V to +20 V, which has the effect of decreasing the threshold voltage of the nFET, thereby increasing the drive current of all the nFETs in the inverter chain. As a result of the increased nFET restoring current, SETs generated in pFETs are expected to become narrower. In the third case, increasing the drive currents of both the nFET and pFET at the same time increases the restoring current for transients generated in nFETs and pFETs, which should result in a narrower FET width. In all three cases, applying V_{BG} will change the inverter response, which will change the broadening rate.

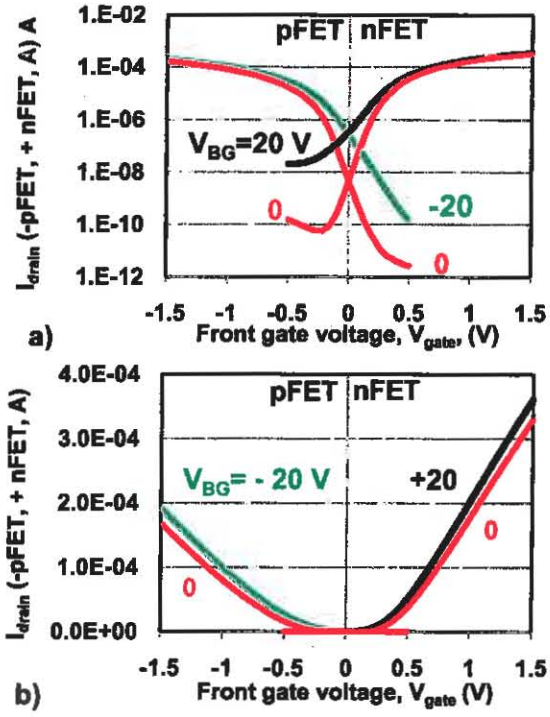

Figure 11: Effect of the back metal bias voltage (V_{BG}) on the $I_{drain}(V_{gate})$ of nFET and pFET. The effect is similar to applying a bias voltage to the substrate of FDSOI FETs. V_{BG} is 0 or -20 V for pFET, 0 or +20 V for nFET.(a) subthreshold and (b) linear regions.

Figure 12 shows the average pulse width and the SET cross-section measured experimentally as a

function of V_{BG} applied to the back of nFET and/or pFET for the SET test circuit on tier 2. The SET distributions were shown previously in Figure 7.

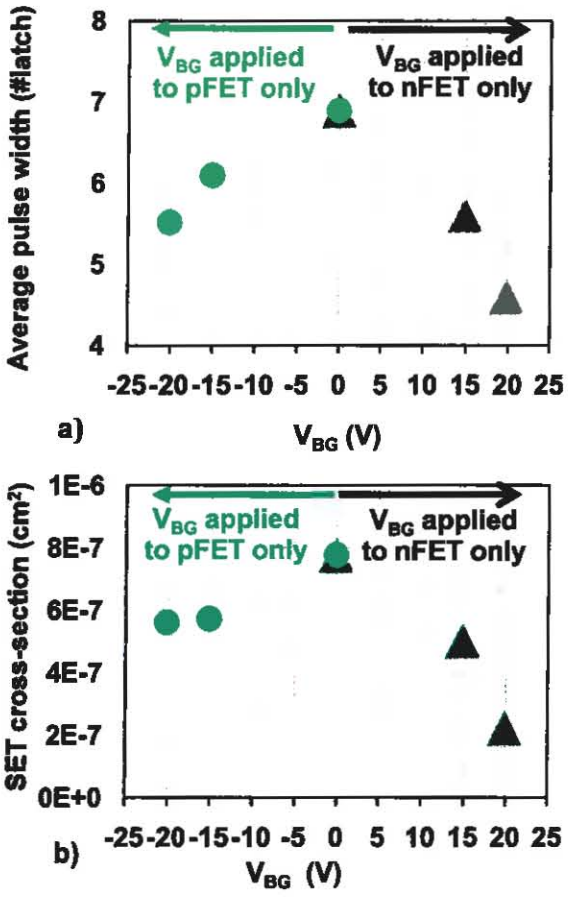

Figure 12: a) Average SET pulse width and b) SET cross-section as a function of V_{BG} applied to the back

A negative V_{BG} on the pFET (V_{BG} =0 for the nFET) reduces the total number of SETs by ~ 28% at V_{BG} = -20 V. It also reduces the average SET width by ~ 20% at V_{BG} = -20 V compared to that the baseline conditions where V_{BG} = 0 for the nFET and pFET. This is because V_{BG} increases the pFET drive current, which will reduce the pulse width of SETs induced in nFETs. Figure 7 shows that the maximum SET pulse width is still ~ 10 latches wide; indicating that the widest SETs could be associated with SETs generated in the pFETs. Laser testing would be needed to characterize the SET broadening rate as a function of V_{BG} . A positive V_{BG} on the nFET (V_{BG} =0 for the pFET) also reduces the total number of SETs by ~ 72% at V_{BG} = 20 V. It also reduces the average SET width by ~ 33% at V_{BG} = -20 V as well as the maximum SET widths as shown in Figure 7.

The experimental SET distributions are consistent with what we predicted based on the change in electrical I(V) of the nFETs and pFETs as a function of V_{BG} shown in Figure 11. Applying V_{BG} on the pFET or the nFET will result in both cases in a reduction of the SET pulse width. The largest effect is for V_{BG} applied on the back of the nFETs because, for an equal $|V_{BG}|$ value, the change in the nFET drive current is larger than for pFET. This result is consistent with earlier work [9], where we showed that the SET cross-section was larger for nFET than pFET for this design.

All our experimental results were explained. The back metal gate can be used to change the SETs generated in an inverter chain of a 3DIC.

VI. Conclusion

We present the first experimental results on single event transients induced by heavy ions in 3DIC logic gate circuits fabricated in a novel 3D technology. The 3D technology integrates three fully-fabricated 2D circuit wafers that are interconnected with 1.25-µm through-oxide vias.

SETs were collected in an inverter chain and measure using an on-chip circuit. SET test circuits were stacked on three different tiers within a 20-µm-thick layer. We show that the Kr ion-induced SET distribution is comparable on the two upper tiers, but it is different on the bottom tier where the median SET pulse width is narrower and the SET cross-section is larger than on the upper tiers. MRED simulations showed that the circuit on the bottom tier might be more sensitive to SETs due to the presence of tungsten and vias and contacts above the sensitive device areas. Due to the 3D process integration, the vias and contacts are located below the sensitive device area for the circuits on tier 2 and 3. Most importantly, the SET distribution will be a function of the inverter response, which will be different if the transistor electrical characteristics are different on each tier.

We also show that the back metal layer, available for circuits on tier 2 and 3, can be used to reduce the SET pulse width and cross-section. This is because the back metal layer can be used to change the drive current of nFET and pFET devices of local sub-circuits independently. Changing the back metal gate voltage has allowed us to discriminate SETs induced in nFET from those induced in pFETs.

Overall, the 3DIC technology offers several unique design features to allow designers to experimentally isolate SET contributions and to build SEE tolerant circuits. For example, if there is a concern with SET effects on a recombinant clock tree causing a false clock edge, one could place a different set of back gates at

each branch level of the clock tree to quantify the percentage contribution of each branch to the SEE effects.

VII. References

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