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# LOW HOMOLOGOUS TEMPERATURE (<0.2) SPUTTERING OF INDIUM FILMS ON SILICON (POSTPRINT)

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Substrate temperature is used to control the film morphology and packing of indium metal deposited by DC sputtering. Indium is sputtered on silicon at room- and liquid nitrogen cryogenic-temperatures resulting in very different homologous temperatures of 0.7 and 0.17. The deposition of the indium film at <0.2 homologous temperature results in increased film packing density, reduced voids, and a near specular indium surface which is very different from the extremely rough room temperature sample. The samples are characterized using atomic force microscope, scanning electron microscopy, transmission electron microscopy, and selective area electron diffraction. This technique for achieving low surface roughness indium has many potential uses for microelectronic packaging.

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# Low homologous temperature (<0.2) sputtering of indium films on silicon

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Substrate temperature is used to control the film morphology and packing of indium metal deposited by DC sputtering. Indium is sputtered on silicon at room- and liquid nitrogen cryogenic-temperatures resulting in very different homologous temperatures of 0.7 and 0.17. The deposition of the indium film at <0.2 homologous temperature results in increased film packing density, reduced voids, and a near specular indium surface which is very different from the extremely rough room temperature sample. The samples are characterized using atomic force microscope, scanning electron microscopy, transmission electron microscopy, and selective area electron diffraction. This technique for achieving low surface roughness indium has many potential uses for microelectronic packaging. © *2012 American Vacuum Society*. [http://dx.doi.org/10.1116/1.4753818]

## I. INTRODUCTION

The manufacturing of electronic and optoelectronic devices has improved dramatically over the last decades. Packaging, however, still contributes significantly to reduced yields because high performing materials such as submounts and solders often have nonideal mechanical characteristics making them difficult, if not impossible to use.[1] Solders are often critical, due to their close proximity to heat producing devices as well as their critical location in the electrical circuit. While lead-based solders such as PbSn have performed extremely well,[2] environment hazards and subsequent legislation have phased these materials out due to the difficulty in recycling lead-containing products.[3] Hard solders such as AuSn perform well in lifetime tests,[4] but their thermal conductivity is low compared to indium, and their lack of mechanical compliance makes them better suited for small component soldering, as opposed to large area or wafer-level bonding.[5]

Indium is a key metal for making electrical as well as thermal contact to a wide variety of semiconductors. Despite some disadvantages such as whisker formation and migration under lifetime test,[6] key characteristics such as its mechanical compliance and softness, combined with extremely high thermal- and electrical-conductivity make it a preferred contact metal for applications where the solder is sandwiched with some force between a device and carrier. For instance, indium solder technology is critical for bonding detector arrays to readout integrated circuits (ROIC) to form focal plane arrays (FPAs)[7] as well as some high power devices such as power amplifiers or large area lasers with heat spreaders.[8] In order to achieve such a layer of indium, several different techniques have been employed including—electroplating,[9] vacuum deposition by sputtering,[10] and evaporation.[11] The deposition techniques have offered better control over the thickness of the indium film and are currently employed extensively in the semiconductor processing industry. Several significant challenges posed by deposited indium on various substrates include void formation, which can be highly detrimental to thermal transport,[12] as well as the presence of extensive crystalline columns on the film surface which can complicate bonding to the indium surface. It must also be pointed out that the softness of indium which makes it such a desirable solder prevents the use of any mechanical or chemical polishing techniques from improving the surface.

To overcome these indium thin film voids and improve surfaces more amenable to uniform bonding, in this manuscript we explore DC sputtering of indium onto silicon substrates by using the substrate temperature as a key parameter in achieving closely packed and highly planar films. The planar surface morphology of a sputtered metal is highly dependent upon the homologous temperature at which the process takes place. The homologous temperature of the sample is defined as the ratio of the substrate temperature during sputtering to the melting point of the metal. It has been shown by Grovenor *et al.*[13] and by Thornton[14] in their structure zone models that the deposition of sputtered metal films at homologous temperatures of <0.2 results in very small equiaxial grains and a planar surface morphology, whereas at a much higher homologous temperature of >0.7, the growth would be dominated by very large columnar structures. The presence of these large columnar structures is considered to be the dominant source of surface roughness when sputtered indium is used as a solder.[15] In most metals, the melting point is very high compared to ambient room temperature, and therefore, the grain structure corresponding to zone I or zone T is naturally produced with a room-temperature platen as the homologous temperature remains

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<0.2. In the case of indium, the low melting point of 429.76 K results in a substrate temperature of ~86 K necessary to achieve a homologous temperature of 0.2 and this can be achieved by cooling the substrate with liquid nitrogen during indium sputtering. This study involves comparing two scenarios. The first scenario represents indium deposition with the substrate kept at room temperature (no active temperature control), where the homologous temperature is ~0.70. The second scenario involves depositing indium with a homologous temperature of about 0.17 and is achieved using liquid nitrogen to cool the substrate to a nominal temperature of 77 K. Correspondingly, the grain structures fall within the zone T and zone III regions.[13] The objective of the study is therefore to deposit and characterize sputtered indium on silicon at cryogenic temperatures to achieve a highly planar and closely packed indium layer thus drastically improving the quality of indium solder for electronic and optoelectronic devices.

## II. EXPERIMENT

For this experiment, sputtering of the indium is done in an AJA ORION©, sputtering system, with modifications to allow for the cooling of the platen using liquid nitrogen. The target was a disk of 99.99% pure indium with a 2-in. diameter and 0.25-in. thick. Prior to sputtering, the silicon substrate was cleaned with acetone and isopropanol and subsequently blow dried with nitrogen before it was placed in the substrate holder. The vacuum chamber was pumped down to a base pressure of 3.2 $\mu$Torr before deposition. Argon plasma was used to sputter the indium onto the silicon substrate. These processing parameters were optimized at room temperature to yield relatively fast growths with the smoothest surface morphology. We found that indium sputtered at room temperature tended to result in smoother surfaces with greater large-scale uniformity than that of evaporated films.

In the case of cryogenic samples, the substrate was cooled using liquid nitrogen fed into the substrate holder after the chamber reached the base pressure. After the substrate reached ~77 K, the deposition process was started with a deposition rate of 0.6 $\mu$m/h. The argon plasma pressure was recorded at 2.2 mTorr with the flow rate of 11.96 sccm. The post deposition characterization of the sample included atomic force microscopy (AFM) to characterize surface roughness followed by the use of a scanning electron microscopy (SEM) with a focused ion beam (FIB). The SEM is used to characterize surface roughness followed by the creation of sections in the material using FIB for cross-section analysis. A section of the samples were also thinned to conduct transmission electron microscopy (TEM) and selective area diffraction (SAED) studies.

Using the above system, 8-h depositions were used to demonstrate films with a relevant thickness for solder bonding purposes. The slow deposition rate we use is unrelated to the inclusion of liquid nitrogen cooling; therefore, we expect a faster production sputtering system would significantly reduce the processing time. At room temperature, films were typically 8.6 $\mu$m thick, while low temperature sputtering resulted in 4.8 $\mu$m thick indium films. The main difference was due to indium packing density. The room temperature samples had a very rough morphology, while the cryogenic samples were near specular. The reason for such an improvement in the quality of the samples can be seen in Figs. 1(b) and 1(c), which show plan-view SEM images of the two samples [Fig. 1(b) at 77 K, Fig. 1(c) at 300 K]. The sample kept at 77 K during the sputtering process shows the presence of some large surface features, which are crystalline indium grains, with large areas of planar surfaces. The AFM image in Fig. 1(a) shows a profile of the flatter surface and this measurement registers a root mean square roughness of ~20 nm. In contrast, the silicon substrate that was kept at room temperature during the sputtering shows a much higher density of indium grains, with some features as long as 50 $\mu$m and having facet formation. There is no presence of any area that is free from such formations. For 8-h depositions, the 300 K deposited indium resulted in rough surfaces outside the vertical range of our AFM (5 $\mu$m), although we approximate this roughness to be about 630 nm, based on shorter depositions, where the film thickness is consistently ~7.3% that of the mean thickness for films >1 $\mu$m in thickness. Thus, the growth of the sample at cryogenic temperatures has moved the growth mode into a much more planar regime compared to the room temperature sample. This effect is consistent with other metallic films structure zone model.[13] However, the issue of the residual crystalline structures in the cryogenic sample needs to be understood. This can be explained through the more involved model by Thornton,[14] where the observed surface is termed a "transitional surface" laying between a completely planar zone and a columnar growth mode zone. This issue may be resolved in the future by further reducing the homologous temperature by making use of a helium based cryogenic system or by modifying the argon plasma pressure both of which have been effective in other metal systems.[15]

## III. RESULTS AND DISCUSSION

The mechanism for the surface morphology difference in the two samples is attributed to the complete lack of indium ad-atom mobility on the surface at lower temperatures, leading to fewer crystalline grains nucleating during the sputtering process. To confirm this effect, we investigate the evolution of the indium film growth from the silicon–indium interface to the final surface using cross-section microscopy. Figure 2 shows the cross-section SEM image of the two samples, with the cryogenic sample shown in Fig. 2(a), while the room temperature deposition shown in Fig. 2(b). The sectioning of the film is done with a FIB. The packing of the indium film is extremely close in the cryogenic sample and the indium seems to have a regular consistency from the interface to the top. An interesting observation in this sample is the porous nature of the first 500 nm of deposited indium, where small voids can be seen across the indium/silicon interface [Fig. 2(a)]. This effect is well explained by a coalescence mechanism for sputtered film growth at low temperatures where the small islands on the silicon wafer merge to form a planar film. The pore size is very indicative

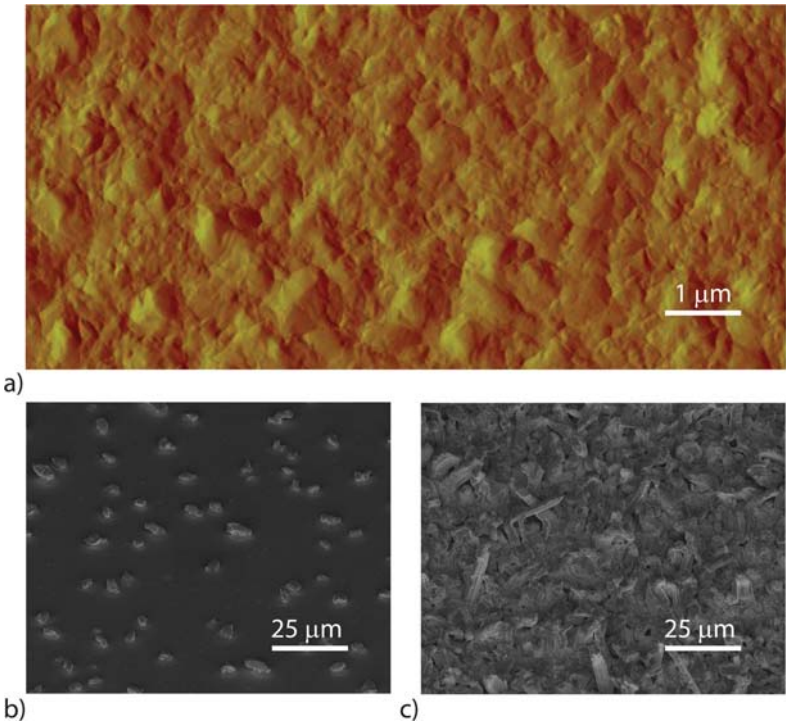


FIG. 1. (Color online) SEM image of the samples with indium sputtered on a silicon samples at 77 K substrate temperature (b) and at room temperature (c). The cryogenic sample in (b) clearly shows significant reduction in the presence of crystalline indium grains compared to the room temperature sample in (c). (a) AFM profile of the planar region in the cryogenic sample.

of the nucleating island size. In this particular sample, we have thinned an adjacent region to the point where we can perform transmission electron microscopy. The room temperature sample shows a significant deviation in indium packing from the cryogenic sample. The indium in the room temperature sample is in the form of large columns that are approximately 3–5 $\mu$m wide and several tens of microns long. One such column is dissected in Fig. 2(b). The structure shows the column bifurcating with the bottom section having a rather uniform consistency while the upper column has continued to grow through the addition of multiple layers one on top of the other. This layer by layer growth could be absent in the lower column after larger grains inhibit material from reaching lower crystals. These large indium grains have preferential growth directions and hence the coalescence between them is limited. These combined effects can lead to the formation of very large voids in the material.

In Fig. 3, we have selected a region in the upper column of the room temperature sputtered sample to analyze with transmission electron microscopy. Figure 3(a) shows a cross-sectional SEM of room temperature deposited indium grain of nominally 2 $\mu$m. The first test involves using SAED to investigate the crystal structure. Figure 3(b) shows the presence of a distinct cubic lattice for indium deposited at

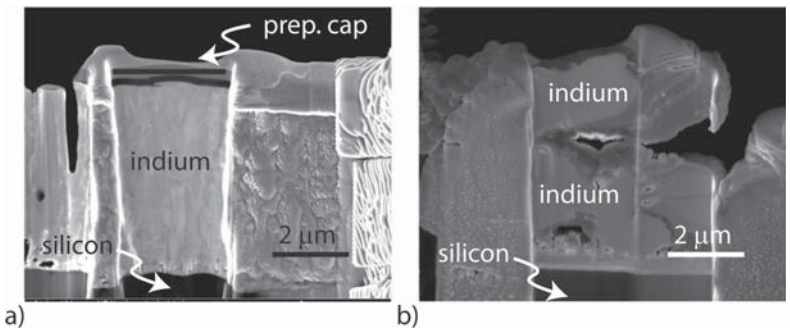


FIG. 2. Cross-section SEM images of the sample at 77 K (a) and the sample at room temperature (b). Both samples have been processed for imaging using a FIB.

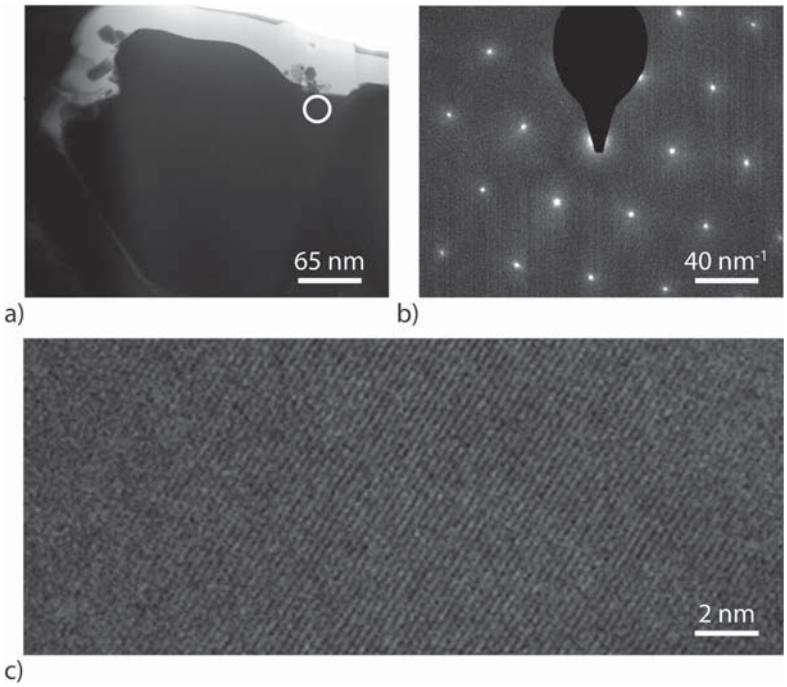


FIG. 3. X-TEM images of the room temperature indium film. (a) A low-resolution image with the circle showing the region being analyzed. (b) SAED image of the region showing the clear presence of a cubic lattice in the crystal. (c) TEM image of the region showing the atomic ordering of indium atoms.

room temperature. The orientation of the indium crystal has no discernible bearing to the underlying silicon crystal orientation. Finally, the high resolution image of the area in Fig. 3(c) shows a very clean crystal ordering in the grain.

In contrast to the room temperature growth of the indium sample, the SAED analysis of the cryogenic sample leads to very different results. The sample SAED consistently shows concentric circles indicative of an amorphous material, and in some regions as shown in Fig. 4, there are some signs of polycrystallinity with very small grain sizes. The SAED analysis of the samples is consistent with the structure zone models for the sputtering conditions used. Furthermore, it also confirms the need for a more amorphous indium phase to achieve the required close packing and planar morphology of the indium which is only achieved by reduced homologous temperature sputtering of the indium.

## IV. SUMMARY AND CONCLUSIONS

In conclusion, we have deposited indium on silicon substrates using DC magnetron sputtering comparing samples at liquid nitrogen cryogenic temperature to those deposited at room temperature. The sputtered indium films are then characterized using AFM, SEM, TEM, and SAED for morphology and material phase information. The results are consistent with structured zone models for metal sputtering with the lower homologous temperature which leads to a highly planar indium film with a near specular surface, while the higher

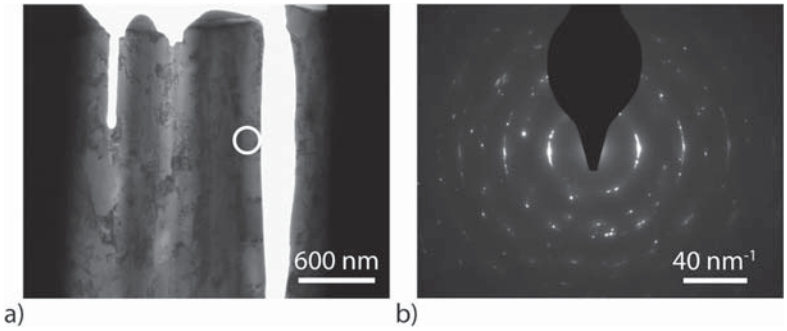


FIG. 4. (a) Low resolution transmission electron microscopy analysis of the cryogenic indium sample and (b) a diffraction pattern from the circled area in TEM image indicating a polycrystalline material with very small grain sizes.

homologous temperature results in very rough morphology dominated by micron size crystalline grains. The indium film on the cryogenic sample still has some remaining crystalline features which puts the deposition process in a transitional zone, between completely planar and completely rough morphologies, in structure zone model of Thornton *et al*. However, the large planar regions have a very low RMS roughness of ~20 nm. By operating in a different zone region, it is worth noting that processing parameters such as pressure and plasma power may be revisited to achieve faster film depositions. Furthermore, we expect that this technique may be used to create smaller grain indium films with other deposition techniques such as evaporation.

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