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14. ABSTRACT

This project was focused on key fundamental issues of future hybrid CMOS/nanodevice circuits:
(i) optimization of metal-oxide devices with resistive bistability, and
(ii) design and simulation of single-electron molecular latching switches.
The report describes the significant progress made in both directions, including
- fabrication of bistable TiO_x devices with yield up to 70% and endurance up to 10^3 cycles,
- design and characterization of single-electron molecular latching switches, and
- design and fabrication of a CMOS subsystem for hybrid integration.

15. SUBJECT TERMS hybrid circuits, nanoelectronics, molecular electronics, CMOS, CMOL, bistability, memory effect, metal oxides, switching

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Fundamental Problems of Hybrid CMOS/Nanodevice Circuits

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1. Objectives:

This project was focused on two key issues of future hybrid CMOS/nanodevice circuits:

(i) fabrication and characterization of reliable two-terminal bistable nanodevices ("latching switches"), and

(ii) development of area-distributed interfaces between the nanowire crossbar and the underlying semiconductor transistor circuit.

The success of work in these directions should enable fabrication and testing of prototype hybrid CMOS/nanodevice circuits and evaluation of their performance. We believe such a demo may change the industrial perception of nanoelectronics and speed up the practical introduction of this technology.

2. Major Accomplishments:

(ia) Fabrication and characterization of metal-oxide bistable devices

We have fabricated and characterized numerous devices from more than 30 wafers with M-Ox-M junctions based on the three metal oxides (which looked most promising from literature data): CuO_x, NbO_x and TiO_x. Metallic base films have been deposited by e-beam evaporation, and then transferred in the sputtering system for cleaning, oxidation and counter-electrode and contact metal deposition. The oxide layer have been formed either "thermally" (by exposure the base electrode to dry oxygen at certain pressure, at room temperature), or by its oxidation in rf plasma discharge. The oxide layer has been encapsulated in-situ using Nb counter-electrode. The subsequent patterning of the junctions (with areas ranging from 3×3 to 300×300 μm^2) has been performed with UV lithography and reactive ion etching.

After the fabrication, samples have been electrically characterized both "as is" and after an additional rapid thermal annealing (RTA) at various temperatures and time intervals. The characterization has been performed mostly at room temperature; however, in order to explore certain fine features of the bistability, some testing was done at 4.2 K.

The results of device property measurements may be briefly summarized as follows:

1. In order to observe the desired bistability effect, junction "formation" process with current "compliance" (restriction) is necessary.

2. Using that formation procedure, the bistability effect may be obtained in junctions based on all studied oxides, with plasma oxidation provides much higher yield of bistable devices than thermal oxidation.

3. After moderate RTA, some plasma-oxide wafers have up to 70% of junctions which showing repeatable switching between two stable states, with endurance ranging from 5 to 1000 cycles.

4. Best results have been achieved with multilayer TiO_x junctions, fabricated by the deposition of several thin (~1.5 nm) Ti layers, interrupted for with their plasma oxidation.

Our best devices are already suitable for CMOS/nanodevice integration studies, though they still need optimization for VLSI circuit applications.

(ib) Design and simulation of molecular single-electron bistable devices

For sub-10-nm scaling of bistable devices, the variability of metal-oxide junctions may prove to be too high, and more reproducible devices necessary. With this motivation, we have carried out design and simulation of single-electron latching switches based on a system of two linear, parallel, electrostatically-coupled molecules: one implementing a single-electron transistor and another serving as a single-electron trap. Both molecules consist of carefully chosen, chemically-synthesizable groups: a phenyl-benzobisoxazole donor group and a naphthalenediimide acceptor group, playing the role of single-electron islands, and alkane chains which work simultaneously as tunnel junctions and intermediate islands of the trap. To verify our design, we have carried out transport calculations based on the combination of two techniques: an *ab-initio* (density-functional-theory) calculation of molecules' electronic structure, and the general theory of single-electron tunneling in systems with discrete energy spectrum.

Our results show that properly designed molecular assemblies with a length below 10 nm and a footprint area of the order of 5 nm^2 can combine sub-microsecond switching times with multi-year retention times as well as high (> 10^3) ON/OFF current ratios, at room temperature. Moreover, Monte Carlo simulations of self-assembled-monolayers (SAM) based on such assemblies have shown that such monolayers may be also used as latching switches, with comparable characteristics.

Our design still needs to be improved by adding neural groups (such as side alkane chains) which would provide proper spacing and transversal rigidity of the active molecules. Nevertheless, we believe that the design is already sufficiently convincing to justify an experimental effort toward fabrication and testing of such molecular devices.

(ii) Development of an area-distributed CMOS/nanodevice interface

We have carried out the first design of CMOS chips for the CMOS/nanodevice integration, and got them fabricated in IBM' 180-nm 7RF process (via MOSIS, Inc. silicon foundry). Each 4×4 mm^2 chip assembly of the design consists of 4 component chips, merged together for processing convenience. Each 2×2 mm^2 component chip features two interface arrays, with 10×10 vias each, with chip's MOSFETs allowing individual access to each via from the peripheral contact pads. Such layout is sufficient for a broad range of experiments with CMOS/nanodevice integration.

The Si_3N_4/SiO_2 passivation layer (common for industrial production of integrated circuits) has been removed using chemical-mechanical polishing (CMP). For that, we have modified a commercial, 2-inch CMP tool for individual chip processing. Inspection and testing of the polished samples has confirmed the suitability of most aspects of our design, but the oxide used in MOSFET design has turned out to be too thin to support voltages necessary for metal-oxide device formation. The IBM design rules allow for a correction of this deficiency; we plan to carry out such modification within the framework of our parallel STTR Phase 2 project (performed in collaboration with Sensor Electronic Technology, Inc. and Rensselaer Polytechnic Institute teams).

In addition, after a detailed discussion with coauthors of our new proposal to 2011 FY MURI (which was submitted to AFOSR in November 2010), we believe that our design may be an excellent starting point for the 3D hybrid integrated circuit work planned in the proposed project.

3. Publications:

1. K. K. Likharev, "Hybrid Semiconductor/Nanoelectronic Circuits: Freeing Advanced Lithography from the Alignment Accuracy Burden". *J. Vac. Sci. Technol. B* **25**, No. 6, pp. 2531-2536 (2007).
2. K. K. Likharev, "Single- and Few-Electron Memories". In: J. E. Brewer and M. Gill (eds.), *Nonvolatile Memory Technologies with Emphasis on Flash*, Wiley, Hoboken, NJ, pp. 689-696 (2008).
3. K. K. Likharev , "Resistive and Hybrid CMOS/Nanodevice Memories". In: J. E. Brewer and M. Gill (eds.), *Nonvolatile Memory Technologies with Emphasis on Flash*, Wiley, Hoboken, NJ, pp. 696-703 (2008).
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5. K. K. Likharev , "Integrated Circuits Beyond CMOS". In: A. Korkin and F. Rosei (eds.), *Nanoelectronics and Photonics*, Springer, Berlin, 2008, pp. 5-7.
6. X. S. Hu, A. Khitun, K. K. Likharev, M. T. Niemeyer, M. Bao, and K. L. Wang, "Design and Defect Tolerance Beyond CMOS". In: *Proc. CODES-ISSS*'08, ACM, 2008, pp. 223-229.
7. K. K. Likharev, "Hybrid CMOS/Nanoelectronic Circuits: Opportunities and Challenges". *J. Nanoelectronics and Optoelectronics* **3**, No. 3, pp. 203-230 (2008).
8. Z. Tan, V. Patel, K. K. Likharev, D. Su, and Y. Zhu, "Experimental Study of Resistive Bistability in Metal Oxide Junctions", *Appl. Phys*. *A* (published online Oct. 25, 2010).
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11. K. K. Likharev, "CrossNets: Neuromorphic Hybrid CMOS/Nanoelectronic Networks". Submitted for publication in *Proc. IEEE* (2010).