



## **Nanowire Photonic Systems**

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## **I. Executive Summary**

The overall objectives of our AFOSR funded research program was to develop semiconductor nanowires as building blocks for nanoscale photonic devices, and to exploit these new photonic devices in fundamental studies relevant to the AFOSR and DoD. To achieve these objectives we pursued a research path defined by the bottom-up paradigm for systems development, which focuses on (i) controlled synthesis of nanoscale building blocks, (ii) characterization of fundamental physical properties of the building blocks, and (iii) assembly of building blocks into functional devices and systems. First, we developed methods for the controlled and predictable synthesis of nanowires and nanowire heterostructures that served as the basic nanoscale building blocks for photonic devices. Nanocluster catalyzed growth was used to develop the synthesis of silicon and gallium-indium nitride alloy nanowire heterostructures to provide building blocks for photonic devices that can span the ultraviolet through visible regions of the electromagnetic spectrum. We also used nanocluster catalyzed growth to investigate the synthesis of axial nanowire heterostructures in which the composition and/or doping was modulated along the axis of a nanowire in a controlled manner, and we explored the growth of an array of core-shell, core-multi-shell, and core-multi-quantum well nanowire heterostructures in which the composition and/or doping were modulated radially in a controlled manner. Second, we elucidated the fundamental optical and electrical properties of these new nanowire and nanowire heterostructure building blocks to define their unique characteristics and potential photonic applications. Our optical and electrical studies focused on measurements at the single nanowire level to provide information about intrinsic properties without ensemble broadening. Last, directed assembly and nanofabrication methods were used to prepare nanowire-based photonic structures. Crossed nanowire junctions and axial-modulated structures were used to demonstrate the first nanoscale avalanche photodiodes. Core-shell or coaxial and axial dopant modulated p-i-n nanowires were also used to elucidate fundamental photovoltaic properties of single nanostructures for the first time, and moreover, to demonstrate the capability of these nanoscale sources to power nanosensors and nanoscale logic circuits. Multi-quantum well nanowire heterostructures were also used to demonstrate the highest performance nanoscale lasers, and to show the capability of broad wavelength tenability in these novel photonic sources.

**REPORT DOCUMENTATION PAGE**

Form Approved  
OMB No. 0704-0188

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<b>1. REPORT DATE (DD-MM-YYYY)</b> 22-12-2009		<b>2. REPORT TYPE</b> Final Technical		<b>3. DATES COVERED (From - To)</b> 09/01/2006-09/30/2009	
<b>4. TITLE AND SUBTITLE</b> Nanowire Photonic Systems				<b>5a. CONTRACT NUMBER</b>	
				<b>5b. GRANT NUMBER</b> FA9550-06-1-0541	
				<b>5c. PROGRAM ELEMENT NUMBER</b>	
<b>6. AUTHOR(S)</b> Charles M. Lieber				<b>5d. PROJECT NUMBER</b>	
				<b>5e. TASK NUMBER</b>	
				<b>5f. WORK UNIT NUMBER</b>	
<b>7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)</b> President and Fellows of Harvard College, Office for Sponsored Programs 1350 Massachusetts Avenue Cambridge, MA 02138				<b>8. PERFORMING ORGANIZATION REPORT NUMBER</b>	
<b>9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)</b> AF Office of Scientific Research AFOSR/PKC 875 N. Randolph St. Room 3112 Arlington, VA 22203				<b>10. SPONSOR/MONITOR'S ACRONYM(S)</b> AFOSR	
				<b>11. SPONSOR/MONITOR'S REPORT NUMBER(S)</b>	
<b>12. DISTRIBUTION/AVAILABILITY STATEMENT</b>					
<b>13. SUPPLEMENTARY NOTES</b>					
<b>14. ABSTRACT</b> Advances in materials and the understanding of the behavior of materials are critical to future Air Force and DoD technologies, ranging from sensing, imaging and threat detection to information processing and storage. In each of these critical areas, there is the potential to make quantum jumps forward in capabilities by developing and exploiting the broad area of science and technology known as 'nanotechnology'. Hence, the development of new nanoscale structures with the unique properties and fabrication of hybrid structures and systems that exploit these unique capabilities and those of conventional technology could lead to systems that are essential to and create powerful new technology. This project has addressed key scientific issues underlying the development of nanowire building blocks and their development in a variety nanophotonic devices, including nanoscale detectors with ultra-high sensitivity and subwavelength spatial resolution, novel nanoscale photovoltaic devices with high efficiencies and capability of powering nanoelectronic devices, and nanoscale light sources, including nanolasers.					
<b>15. SUBJECT TERMS</b> nanowires, nanophotonics, avalanche detectors, nanoLEDs, nanolasers, photovoltaics					
<b>16. SECURITY CLASSIFICATION OF:</b>			<b>17. LIMITATION OF ABSTRACT</b>	<b>18. NUMBER OF PAGES</b>	<b>19a. NAME OF RESPONSIBLE PERSON</b> Webb Brightwell
<b>a. REPORT</b>	<b>b. ABSTRACT</b>	<b>c. THIS PAGE</b>			<b>19b. TELEPHONE NUMBER (Include area code)</b> 617-384-7673

Final Technical Report for  
GRANT NUMBER FA9550-06-1-0541  
1 September 2006 – 30 September 2009

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## IV. Technical Report

### A. Scientific Results

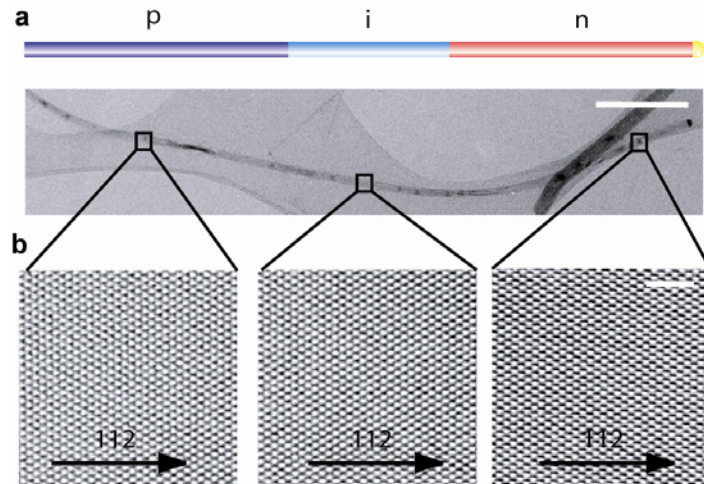
During this project we pursued a research path defined by the bottom-up paradigm for systems development, which focused on controlled synthesis of nanoscale building blocks, characterization of fundamental physical properties of the building blocks, and assembly of building blocks into functional devices and systems. Substantial progress and accomplishments were made in all areas of the project and will be summarized below. First, we developed methods for the controlled and predictable synthesis of nanowires and nanowire heterostructures that served as the basic nanoscale building blocks for photonic devices. Nanocluster catalyzed growth was used to develop the synthesis of silicon and gallium-indium nitride alloy nanowire heterostructures to provide building blocks for photonic devices that can span the ultraviolet through visible regions of the electromagnetic spectrum. We also used nanocluster catalyzed growth to investigate the synthesis of axial nanowire heterostructures in which the composition and/or doping was modulated along the axis of a nanowire in a controlled manner, and we explored the growth of an array of core-shell, core-multi-shell, and core-multi-quantum well nanowire heterostructures in which the composition and/or doping were modulated radially in a controlled manner. Second, we elucidated the fundamental optical and electrical properties of these new nanowire and nanowire heterostructure building blocks to define their unique characteristics and potential photonic applications. Our optical and electrical studies focused on measurements at the single nanowire level to provide information about intrinsic properties without ensemble broadening. Last, directed assembly and nanofabrication methods were used to prepare nanowire-based photonic structures. Crossed nanowire junctions and axial-modulated structures were used to demonstrate the first nanoscale avalanche photodiodes. Core-shell or coaxial and axial dopant modulated p-i-n nanowires were also used to elucidate fundamental photovoltaic properties of single nanostructures for the first time, and moreover, to demonstrate the capability of these nanoscale sources to power nanosensors and nanoscale logic circuits. Multi-quantum well nanowire heterostructures were also used to demonstrate the highest performance nanoscale lasers, and to show the capability of broad wavelength tenability in these novel photonic sources. Below further details of the project studies organized around the major accomplishments in (1) nanoscale detectors and (2) nanoscale photovoltaics will be summarized.

**IV.A.1. Nanoscale avalanche photodiodes.** We have developed the controlled synthesis of axial modulation-doped p-type/intrinsic/n-type (*p-i-n*) silicon nanowires (SiNWs) with uniform diameters and single crystal structures. The *p-i-n* nanowires were grown in three sequential steps: in the presence of diborane for the p-type region, in the absence of chemical dopant sources for the middle segment and in the presence of phosphine for the n-type region. The *p-i-n* nanowires were structurally characterized by transmission electron microscopy, and the spatially-resolved electrical properties of individual nanowires were determined by electrostatic force and scanning gate microscopies. Temperature-dependent current-voltage measurements recorded from individual *p-i-n* devices show an increase in the breakdown voltage with temperature, characteristic of band-to-band impact ionization or avalanche breakdown. Spatially-resolved photocurrent measurements show that the largest photocurrent is generated at the intrinsic region located between the electrode contacts, with multiplication factors in excess of ca. 30, and demonstrates that single *p-i-n* nanowires function as avalanche

photodiodes. Electron- and hole-initiated avalanche gain measurements performed by localized photoexcitation of the *p*-type and *n*-type regions yield multiplication factors of ca. 100 and 20, respectively. These results demonstrate the significant potential of single *p-i-n* nanowires as nanoscale avalanche photodetectors, and open possible opportunities for studying impact ionization of electrons and holes within quasi-one-dimensional semiconductor systems.

The *p-i-n* SiNWs were synthesized by the nanocluster-catalyzed chemical vapor deposition methods approach described previously. The dopant concentration was varied by controlling the feed-in ratio between silane and phosphine (diborane), and the effective dopant concentrations in the *p*-type and *n*-type regions were estimated to be ca.  $8 \times 10^{19}/\text{cm}^3$  and ca.  $5 \times 10^{19}/\text{cm}^3$ , respectively. Synthesis of the undoped region between the *p* and *n*-type regions was achieved by switching off the dopant flow while maintaining axial growth. The effective carrier density of the undoped region, ca.  $10^{16}/\text{cm}^3$ , is  $10^3$ - $10^4$  lower than the effective concentration in the *p*- and *n*-type regions, and hence we term this section intrinsic. Although the exact dopant number is not known in the SiNWs, it is worth recognizing that a concentration of  $10^{16}/\text{cm}^3$  corresponds to only ca. 3 dopants in a 1 micron long 20 nm diameter Si crystal, which is consistent with the assignment of this region as intrinsic.

Low- and high-resolution transmission electron microscopy (TEM) studies of *p-i-n* SiNWs (e.g., Figure 1) show that NW diameters are very uniform over the lengths of the structures with no observable end-to-end change. These results show that simultaneous radial growth, which would obscure modulation of electronic properties along the nanowire axis,<sup>18</sup> has been effectively eliminated in the growth of the *p-i-n* SiNWs. The low-resolution TEM and SEM (not shown) data also show that the average *p-i-n* SiNW length, ca. 6.5  $\mu\text{m}$ , is consistent with the 6.84  $\mu\text{m}$  length expected based on the growth rates/times.<sup>18</sup> In addition, high-resolution TEM images recorded from the *p*-, *i* and *n*- regions (Figure 1b) demonstrate that these SiNWs have uniform single-crystalline structures, despite the changes in chemical dopant sources during synthesis, with a  $\langle 112 \rangle$  lattice direction along the NW axis. The demonstration of single crystal structures with uniform growth direction is important for studies of APDs, because the multiplication factors may vary for different crystallographic directions.

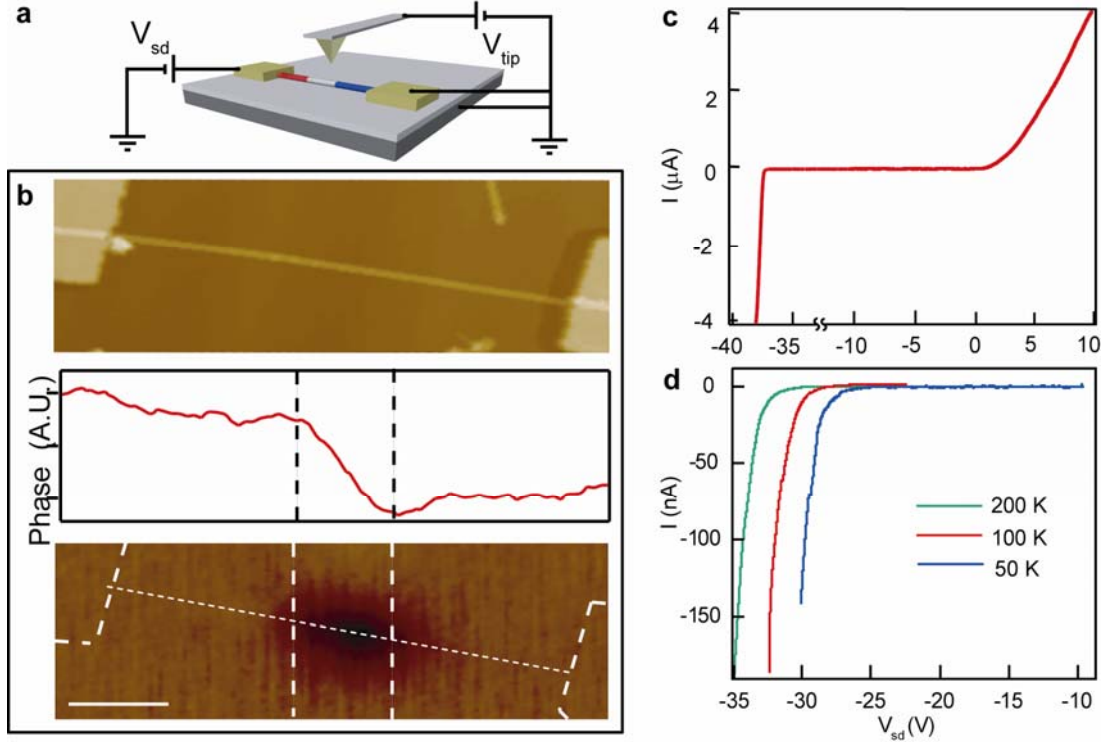




**Figure 1.** TEM characterization of *p-i-n* SiNWs. (a) Schematic of a *p-i-n* NW, where the yellow hemisphere (right end) corresponds to the Au-nanocluster catalyst used in the sequential growth of the *p*-type (purple), *i* (pale blue) and *n*-type (red) regions. Low-resolution TEM image of a representative 20 nm diameter *p-i-n* SiNW; scale bar is 500 nm. (b) High-resolution TEM images from the *p-i-n* segments – left, middle and right, respectively – recorded along the [1,1,-1] zone axis; the images were taken from the central regions indicated by the boxes along the low-resolution SiNW in (a); scale bar is 2 nm.

To confirm that SiNWs exhibit expected variations in the electronic properties associated with *p-i-n* dopant modulation, we used electrostatic force microscopy (EFM) and scanning gate microscopy (SGM). In these measurements (Figure 2a, top), a conducting tip with applied voltage  $V_{tip}$  was scanned at a fixed height over a *p-i-n* SiNW device with bias  $V_{sd}$  applied through contacts to the *p*- and *n*-type ends of the NW. We can glean several important points from the resulting data. First, the AFM topography image shows a well-defined single NW device ca. 4.7  $\mu\text{m}$  in length between the contact electrodes. Inclusion of the 1  $\mu\text{m}$  NW lengths under each electrode contact yields a total NW length, ca. 6.7  $\mu\text{m}$ , consistent with the estimated value of 6.8 based on growth. Second, the line-profile of EFM phase-shift signal measured along the *p-i-n* SiNW axis exhibits a pronounced change only across the middle region of the device, and thus shows that voltage drop occurs primarily across this ca. 1.0  $\mu\text{m}$  long middle region. Third, the SGM image of the same device further demonstrates a substantial change (decrease) in conductance only in this same 1.0  $\mu\text{m}$  long middle region of the *p-i-n* SiNW device. The SGM results are consistent with heavily doped end-regions, which do not undergo substantial depletion or accumulation in presence of local tip gate, and a lightly *p*-type central region, which we refer to as “*i*” due to the low effective dopant concentration determined from resistivity measurements (see above). Taken together, these results indicate that the *i* region our *p-i-n* SiNWs has a length of  $1.0 \pm 0.2 \mu\text{m}$ , which is consistent with the length estimated from the growth rate and growth time, and that the voltage drops primarily across this region as expected for a well-defined *p-i-n* structure.





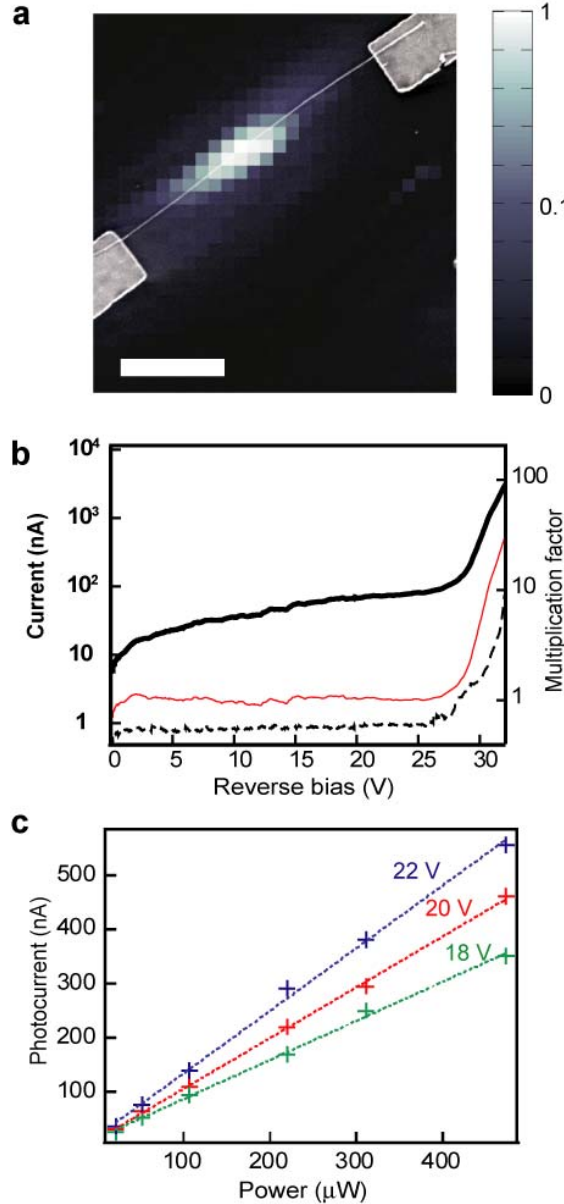
**Figure 2.** Probe microscopy and transport characteristic of  $p-i-n$  SiNW devices. (a) Schematic of the measurement setup. (b) From top to bottom, (i) AFM topograph of the  $p-i-n$  SiNW, (ii) plot of EFM phase-shift vs. position recorded along the nanowire axis and (iii) SGM image taken on the same device. The dark region corresponds to a decrease in current, white dash lines in the SGM image indicate the  $p-i-n$  SiNW between contacts and electrodes. The vertical dash lines mark the intrinsic regions. Scale bar shown in SGM image, 1  $\mu\text{m}$ , is same for EFM and AFM images. (c) Current vs. applied voltage curve for a typical SiNW  $p-i-n$  junction at room temperature. (d) Current vs. applied reverse voltage data of a  $p-i-n$  SiNW recorded at temperature of 200 K (green line), 100K (red line) and 50K (blue line).

The electrical properties of  $p-i-n$  junctions within nanowires were also probed by the current ( $I$ ) versus bias voltage ( $V$ ) measurements. Representative data recorded from a  $p-i-n$  SiNW device at room temperature (Figure 2c) show current rectification with significant current flowing at a forward bias  $> 1$  V. The reverse bias results further show a sharp increase at a much larger voltage, 38 V, that we associate with breakdown voltage ( $V_B$ ). This sharp increase in current at  $V_B$  is suggestive of an avalanche breakdown mechanism. The corresponding breakdown field, assuming the voltage drop occurs across the  $i$ -region is ca.  $4 \times 10^5$  V/cm. In addition, we have characterized the temperature of the reverse-bias breakdown behavior (Figure 2d). Significantly, these  $I-V$  data show a positive shift in the onset of breakdown with increasing temperature, corresponding to a temperature coefficient of ca. 30 mV/K. The measured positive temperature coefficient confirms that the breakdown mechanism is based on band-to-band impact ionization rather than on band-to-band tunneling; that is, avalanche breakdown.

To characterize the optoelectronic properties of the SiNW *p-i-n* junctions and evaluate their potential as nanoscale APDs, we have combined a scanning optical microscope with transport measurements. A representative photocurrent map measured from a *p-i-n* SiNW (Figure 3a) shows a large photocurrent in the middle region of the device, where the position of the SiNW devices is highlighted by registered SEM image overlaid on the photocurrent data. Analysis of the photocurrent peaks yield a full-width-half-maximum (FWHM) of ca. 500 nm perpendicular to the nanowire axis, which corresponds to the upper bound on the spatial resolution of our measurements. The FWHM along the SiNW axis, ca. 1.5  $\mu\text{m}$ , is consistent with the length of the *i*-region characterized independently by SGM and EFM. The photocurrent in the middle region of our *p-i-n* SiNW devices has a peak value typically  $10^2 - 10^3$  times (500 in Figure 3a) larger than the photocurrents measured on the *p*- and *n*-regions. This observation is consistent with the large potential drop and corresponding strong electric-field in the *i*-region, which can efficiently separate photo-generated electron-hole pairs to create a photocurrent. In addition negligible photocurrent response is observed at the SiNW-metal contacts, which is distinct from previous studies where Schottky barriers dominate the response. These results demonstrate clearly that the active detecting region is localized at the *i*-region of the *p-i-n* SiNWs.

To determine the avalanche multiplication in the *i*-region, we measured the dark current ( $I_{dark}$ ) and the photocurrent ( $I_{ph}$ ) from the center of the *i* region of *p-i-n* SiNW devices as a function of reverse bias voltage as shown in Figure 3b. At the levels of illumination used in our experiments the  $I_{ph}$  is up to  $10^3$  larger than the  $I_{dark}$ , and increases with increasing reverse bias. Avalanche gain is quantified by calculating the avalanche multiplication factor,  $M$ , defined as  $M = I_{ph}/I_{ph0}$ , where  $I_{ph0}$  is the primary unmultiplied photocurrent at the bias voltage at which the  $I_{ph}$  is measured. The value of  $I_{ph0}$  is obtained from a linear extrapolation of the  $I_{ph}$  in the bias region of from 20 to 25 V where the curve is nearly flat. The plot of  $M$  versus reverse bias voltage (red curve, Figure 3b) shows that this device exhibits a multiplication factor of ca. 30 for sub-breakdown biases. Similar values of  $M$  have been reproducibly observed in a number of *p-i-n* SiNW devices, and moreover, we note that these values are comparable to multiplication factors for planar Si APDs.

In addition, the responsivity of the *p-i-n* SiNW photodectors was measured as a function of the incident laser power.  $I_{ph}$  vs. laser power (Figure 3c) measured at 22, 20 and 18 V show linear dependences with slopes of 1.16, 0.94 and 0.72 nA/ $\mu\text{W}$ , respectively. As expected, larger  $I_{ph}$  are observed for larger reverse bias voltages at the same incident laser power. The responsivity of SiNW devices is limited by optical absorption and geometric effects; for example, only ca. 0.02% of the incident light is absorbed by a 20 nm SiNW photoexcited with a 500 nm FWHM beam with 0.9  $\mu\text{m}$  absorption length. If we correct for these limitations on absorption in *p-i-n* SiNW photodectors the responsivity is comparable to values for planar Si APD devices. By operating the device in the Geiger mode the sensitivity could be substantially increased to overcome intrinsic geometric and absorption limitations.



**Figure 3.** Photocurrents from *p-i-n* SiNW avalanche photodiodes. (a) Normalized photocurrent map with superimposed SEM image of a 20 nm *p-i-n* SiNW. The length of the intrinsic region was determined by EFM and SGM is 1.5  $\mu\text{m}$ . The bias voltage and the scanning step size were -28 V and 250 nm (in x and y), respectively. Scale bar, 2  $\mu\text{m}$ . (b) Photocurrent (black solid line), dark current (dashed line)  $I$ - $V$  data, and corresponding multiplication factor (red line). (c) Photocurrent vs. optical power at 488 nm for reverse bias values of 22 V (blue line), 20V (red line) and 18 V (green line). (b) and (c) were measured with the laser focused onto the center of the intrinsic region.

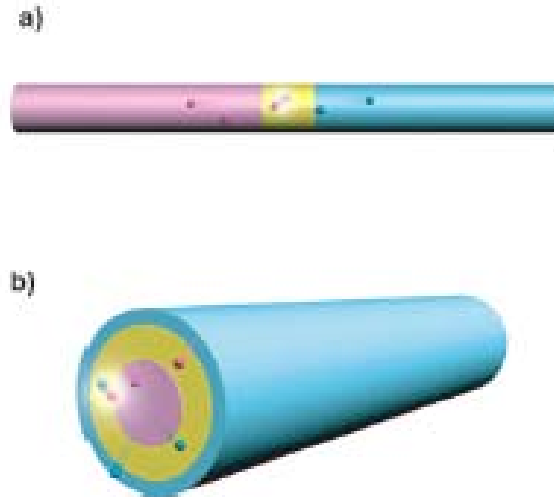
In summary, we have described a general and controlled approach for synthesizing single-crystal *p-i-n* SiNW structures. High-resolution TEM, EFM and SGM were used to spatially define the structure and electrical characterize of the three regions along the SiNW *p-i-n* structures. Temperature-dependent transport measurements were

used to characterize the diode behavior and demonstrated an avalanche breakdown mechanism at large reverse bias. In addition, photocurrent measurements show that *p-i-n* SiNW devices act as nanoscale APDs with a spatial resolution defined by the physical dimension of the *i* region encoded during growth. Photomultiplication as well as pure multiplication factors for electrons and holes were determined and found to be comparable to published results for planar Si APDs. These *p-i-n* SiNW APDs should make possible integrated nanophotonic systems by providing direct polarization sensitivity, high-spatial resolution and high-sensitivity not achievable with conventional planar photodetectors, and moreover, the capability of being readily assembled with other distinct photonic elements in a bottom-up approach. In addition, the nanowire APDs will enable access to new and interesting physics associated with confined 1-dimensional or quasi-1-dimensional semiconducting systems, such as investigations of impact ionization rates as carrier-phonon interactions change due to confinement. Last, while our studies have focused on characterizing the fundamental properties of individual *p-i-n* SiNW devices, emerging assembly techniques could be used to fabricate large arrays of addressable *p-i-n* SiNW APDs over flexible or rigid substrates thus enable a variety of additional applications.

**IV.A.2. Nanoscale photovoltaics.** Semiconductor nanowires are a broad class of materials which, through controlled growth and organization, have led to a number of novel nanoscale photonic and electronic devices. Given the need to elucidate the intrinsic characteristics and limits of nano-enabled solar cells in order to evaluate their potential for next generation, large-scale, high-efficiency and low-cost solar cells, as well as integrated power solutions for emerging nanoelectronic devices, we have carried out studies exploiting single nanowire heterostructures as stand-alone and active photovoltaic elements. The use of single nanowires as photovoltaic elements presents several key advantages which may be leveraged to produce high-efficiency, robust, integrated nanoscale PV power sources. First, the principle of bottom-up design allows the rational control of key nanomaterial parameters, which will determine PV performance, including chemical/dopant composition, diode junction structure, size, and morphology. Importantly, this principle has been demonstrated previously in a wide variety of nanoscale structures and devices. Second, single or interconnected nanowire PV elements could be seamlessly integrated with conventional electronics and/or future nanoscale electronics to provide energy for low-power applications. Third, studies of PV properties at the single nanowire level will permit determination of the intrinsic limits, areas of improvement, and potential benefits of nano-enabled PV.

Two unique structural motifs that can yield functional PV devices at the single nanowire level include *p*-type/intrinsic/*n*-type (*p-i-n*) dopant modulation in axial and radial geometries. A prototypical single *p-i-n* axially-modulated nanowire diode is shown in Figure 4a. The pink, yellow, and blue regions denote the *p*-type, intrinsic, and *n*-type diode segments, respectively. In this structure, electron-hole pairs are generated throughout the device upon absorption of photons whose energies are equal to or greater than the band-gap of silicon ( $E_g = 1.12$  eV for single-crystal silicon). Carrier generation and separation are most efficient within the depletion region due to the built-in field established across the *p-i-n* junction. Once swept in the direction of the electric field, the

photogenerated holes (electrons) traverse through the  $p$ -type ( $n$ -type) regions and are collected as a photocurrent by ohmic metal contacts. In this axial configuration, the  $p$ -type and  $n$ -type regions can be made arbitrarily short since their main purpose is to provide contact to the junction embedded within the nanowire. Therefore, the active device area can be kept very small so as to enhance integration.



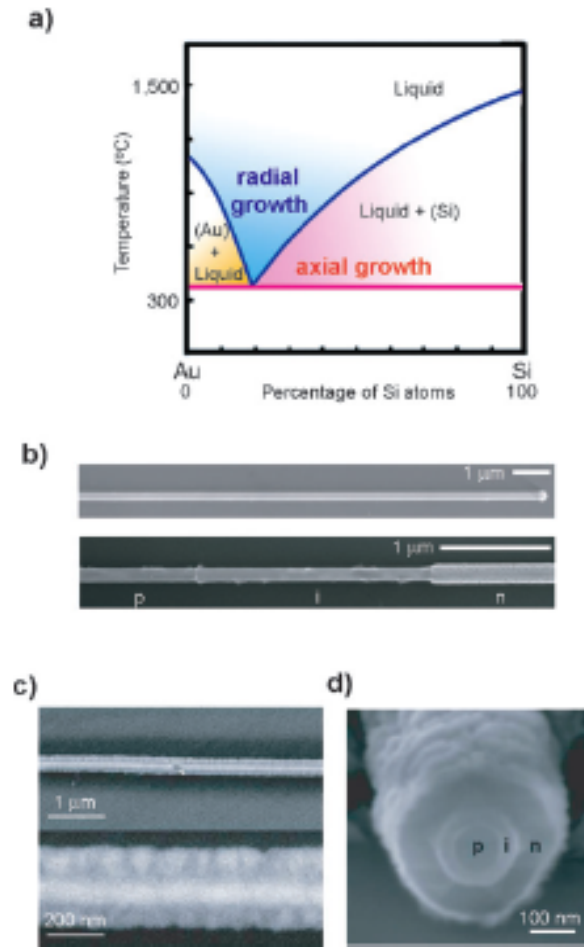
**Figure 4.** Schematic of carrier generation and separation in **a)** axial and **b)** radial  $p$ - $i$ - $n$  nanowires. The pink, yellow, and blue regions denote the  $p$ -type,  $i$ -, and  $n$ -type diode segments, respectively. The pink and blue spheres denote the holes and electrons, respectively.

A closely related structure is the  $p$ - $i$ - $n$  radially-modulated nanowire diode (Figure 4b). The overall device physics is identical to that of the axially-modulated motif, with the key added benefits being that the  $p$ - $i$ - $n$  interface extends along the length of the nanowire and that carrier separation takes place in the radial versus the longer axial direction. Since the latter yields a carrier collection distance smaller or comparable to the minority carrier diffusion length, photogenerated carriers can reach the  $p$ - $i$ - $n$  junction with high efficiency without substantial bulk recombination. Indeed, recent theoretical studies have suggested that coaxial nanowire structures could improve carrier collection and overall efficiency with respect to comparable single-crystal bulk semiconductors, and especially when relatively low quality materials are used as absorber materials. Large-scale vertically aligned arrays of coaxial nanowires would enable substantial light absorption along the long-axis of the nanowires, and also afford the benefit of short-range and efficient radial carrier separation. Together, these advantages would orthogonalize the pathways for light absorption and carrier collection, thereby eliminating a key limitation of conventional planar solar cells, and reduce device surface reflectance, which is not the focus of our work and the current tutorial review.

Both axial and radial  $p$ - $i$ - $n$  Si-nanowires are synthesized via the gold-nanoparticle catalyzed VLS growth method, using silane ( $\text{SiH}_4$ ), diborane ( $\text{B}_2\text{H}_6$ ) and phosphine ( $\text{PH}_3$ ) as silicon source, and  $p$ -type and  $n$ -type dopants, respectively, and guided by the Au-Si

phase diagram (Figure 5a). A typical VLS process (pink region) starts with the dissolution and saturation of gaseous reactants into nanosized liquid droplets of a catalyst metal (*e.g.* Au), followed by nucleation and growth of single-crystalline nanowires. The phase diagram shows that silicon nanowire axial growth (pink region) is preferred at lower temperatures ( $\sim 400\text{-}500\text{ }^{\circ}\text{C}$ ) and higher  $\text{SiH}_4$  partial pressures, while radial growth (blue region) occurs preferentially at higher temperatures ( $\sim 600\text{-}800\text{ }^{\circ}\text{C}$ ) and lower  $\text{SiH}_4$  partial pressures.

For axial *p-i-n* silicon nanowires, dopant modulation is achieved by switching dopant precursor gases at appropriate times during nanowire elongation. Field-emission scanning electron microscopy (SEM) images indicate that the as-grown axial *p-i-n* Si-nanowires are straight, have smooth surfaces, and a uniform diameter with  $< 1\%$  deviation along the typical  $25\text{ }\mu\text{m}$  length (Figure 5b, top). Independently calibrated growth rates for each segment of Si-nanowire growth obtained on homogeneous *p*-, *i*-, and *n*-type Si-nanowires prepared under similar conditions have shown that the lengths of the Si-nanowires are consistent with overall growth times. In addition, the uniform diameters demonstrate that axial growth is the predominant process under these experimental conditions. In order to verify successful encoding of designed *p-i-n* structures, the Si-nanowires were selectively-etched in potassium hydroxide solution, where the single-crystal Si-nanowire radial etching rate,  $R$ , goes as  $R_i > R_p > R_n$ . SEM images of etched *p-i-n* Si-nanowire structures (Figure 5b bottom) show clear delineation of the individual regions of the diode structure, which can be referenced to the Au nanocluster catalyst at the end of the last (*n*-type) segment. Finally, the Si-nanowire etching profile follows the order in which dopants were introduced during synthesis: First boron for *p*-type, no dopant for *i*-type, and then phosphorous for *n*-type.



**Figure 5.** a) Binary phase diagram for Au and Si illustrating the thermodynamics of axial and radial nanowire growth. b) SEM images of *p-i-n* axial Si-nanowire before (upper panel) and after (lower panel) wet-chemical etching. c) SEM images of the *p-i-n* coaxial Si-nanowire at two different magnifications. d) Cross-section SEM image of coaxial Si-nanowire after wet-chemical etching from cleaved end.

For the radial structure, *p*-core growth proceeds as for the axial case and is followed by deposition of *i*- and *n*- shells at higher temperature and lower pressure to inhibit axial elongation of the Si-nanowire core during the radial growth. SEM images of a typical *p-i-n* coaxial Si-nanowire recorded in the back scattered electron imaging mode (Figure 5c) highlight several key features. First, the uniform contrast of the nanowire core is consistent with a single-crystalline structure expected for Si-nanowires obtained by the VLS method. Second, contrast variation observed in the shells is indicative of a polycrystalline structure with grain size on the order of 30-80 nm. HRTEM images confirm that the nanowire shells are indeed polycrystalline. We note here and later comment in greater detail, that this nanocrystalline shell structure may enhance light absorption by the nanowires. In analogy with the etching technique used to delineate the axial *p-i-n* diode regions, an SEM image of the cross-section of a radial *p-i-n* Si-nanowire (Figure 5d) clearly reveals the distinct *p*-core and *i*- and *n*-shell portions of the structure.

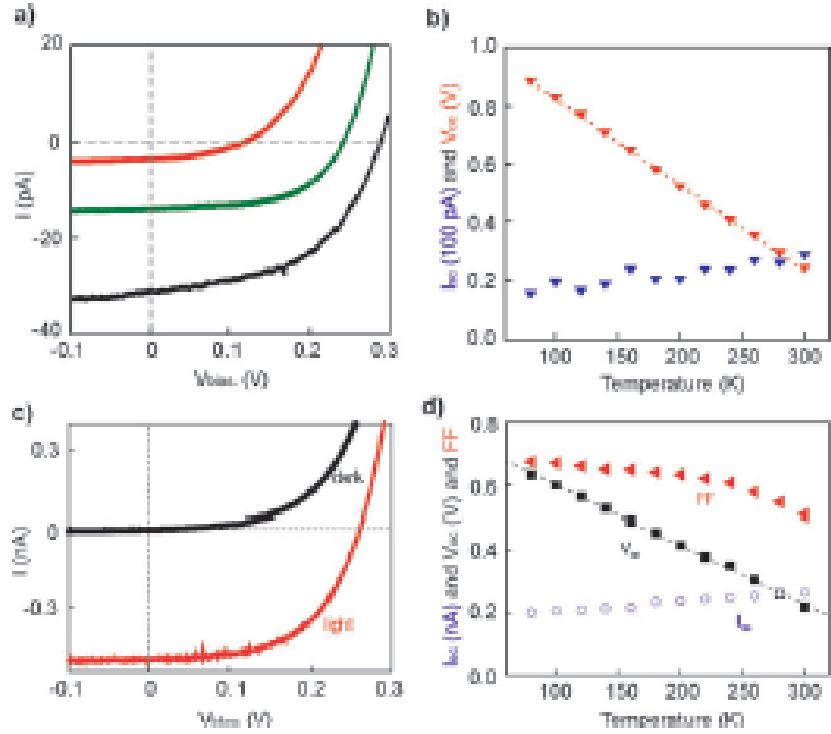


Together, these observations show that our designed synthesis can reliably yield axial and radial *p-i-n* Si-nanowires with controlled encoding of the length (thickness), dopant profile, and material morphology within different regions. Control of these parameters is, of course, the prerequisite for producing well-defined diode structures necessary for investigating PV devices.

The electrical transport properties of the axial and radial *p-i-n* Si-nanowire devices have also been characterized by current-voltage (*I-V*) measurements under dark conditions at room temperature. Dark *I-V* characteristics recorded from axial *p-i-n* devices with *i*-region lengths of 0, 2 and 4  $\mu\text{m}$ . Overall, these data show well-defined current rectification, which is characteristic of the diode structure, and a current onset in forward bias at ca. 0.6 V. The onset value is typical for a *p-n* silicon diode with the built-in potential being established as the difference between the Fermi energies in the *p*- and *n*-type regions. *I-V* curves recorded across the *p*- or *n*- segments alone in *p-i-n* Si-nanowire devices containing multiple contacts showed linear behavior, thus confirming that the contacts are ohmic to the *p*- and *n*-type segments, and that current rectification is due solely to the built-in electric field across the *p-n* or *p-i-n* junction. We also note that the reverse bias leakage current ( $V < -1$  V) is largest for the *p-n* Si-nanowire diodes. This leakage can be attributed to larger interfacial recombination in the *p-n* diodes that is reduced with inclusion of an *i*-region in the *p-i-n* Si-nanowires. Dark *I-V* curves obtained from radial *p-i-n* devices likewise exhibit characteristics indicative of formation of good diodes. Linear *I-V* curves from core-core (p1-p2) and shell-shell (n1-n2) configurations demonstrate that ohmic contacts are made to both core and shell portions of the nanowires, with the latter showing higher conductance versus the core. Significantly, the highly conductive *n*-shell will reduce or eliminate potential drop along the shell, thereby enabling uniform radial carrier separation and collection when illuminated. *I-V* curves recorded from different core-shell contact geometries show rectifying behavior, and demonstrate that the *p-i-n* radial Si-nanowires behave as well-defined diodes.

The photovoltaic properties of the axial and radial *p-i-n* Si-nanowire diodes were characterized under standard conditions of 1-sun ( $100 \text{ mW/cm}^2$ ) AM 1.5G illumination. Representative light *I-V* data for *p-n*, *p-i-n*  $i = 2 \mu\text{m}$ , and *p-i-n*  $i = 4 \mu\text{m}$  devices (Figure 6a) yield open-circuit voltage,  $V_{oc}$ , and short-circuit current,  $I_{sc}$ , values of 0.12 V and 3.5 pA, 0.24 V and 14.0 pA, and 0.29 V and 31.1 pA, respectively. The results reveal a systematic improvement in both  $V_{oc}$  and  $I_{sc}$  with increasing *i*-segment length with the largest increase in  $V_{oc}$  observed in moving from the *p-n* to *p-i-n* structural motif. Qualitatively, the improvement of  $V_{oc}$  is consistent with the reduction of leakage currents upon inclusion of the *i*-segment. Likewise, the systematic increase in  $I_{sc}$  as a function of increasing *i*-segment length is consistent with previous studies of Si-nanowire avalanche photodiodes which identified the intrinsic region as the most optically sensitive device region. The fill-factor,  $FF$ , for the  $i = 4 \mu\text{m}$  device is 51% and yields a maximum power output per nanowire of 4.6 pW. This value is approximately 15 times smaller than that achievable at 1-sun illumination using radial *p-i-n* Si-nanowire devices, (see below) but is still ca. 1000 times larger than that achieved with single piezoelectric nanowires. In addition, estimated the AM 1.5G efficiency,  $\eta$ , based on the projected active area of the  $i = 4 \mu\text{m}$  device is 0.5%, which is similar to the 0.46% value reported for single Si-nanowires with metal/semiconductor junctions, but considerably smaller than the 3.4% achieved in radial Si-nanowire devices. The apparent short circuit current density ( $J_{sc}$ ) calculated based on the projected active area<sup>12</sup> is  $\sim 3.5 \text{ mA/cm}^2$  (Figure 6a), slightly

smaller than that reported for rectifying single metal/Si-nanowire photovoltaic devices ( $\sim 5.0 \text{ mA/cm}^2$ ), although the nanowire diameter in the latter was 4x larger,  $\sim 1 \mu\text{m}$ .



**Figure 6.** **a)** Light  $I$ - $V$  curves recorded from axial  $p$ - $i$ - $n$  Si-nanowire,  $i$ -length = 0 (red), 2 (green), and 4 ( $\mu\text{m}$ ) (black) devices with illumination intensity of  $100 \text{ mW/cm}^2$ , AM 1.5G. **b)** Plots of  $V_{oc}$  (red) and  $I_{sc}$  (blue) vs. temperature for a  $p$ - $i$ - $n$  ( $i = 4 \mu\text{m}$ ) device. **c)** Dark and light  $I$ - $V$  curves of coaxial Si-nanowire device. **d)** Temperature-dependent data from a coaxial device, where the red triangle, black square and blue circle correspond to  $FF$ ,  $V_{oc}$  and  $I_{sc}$ , respectively.

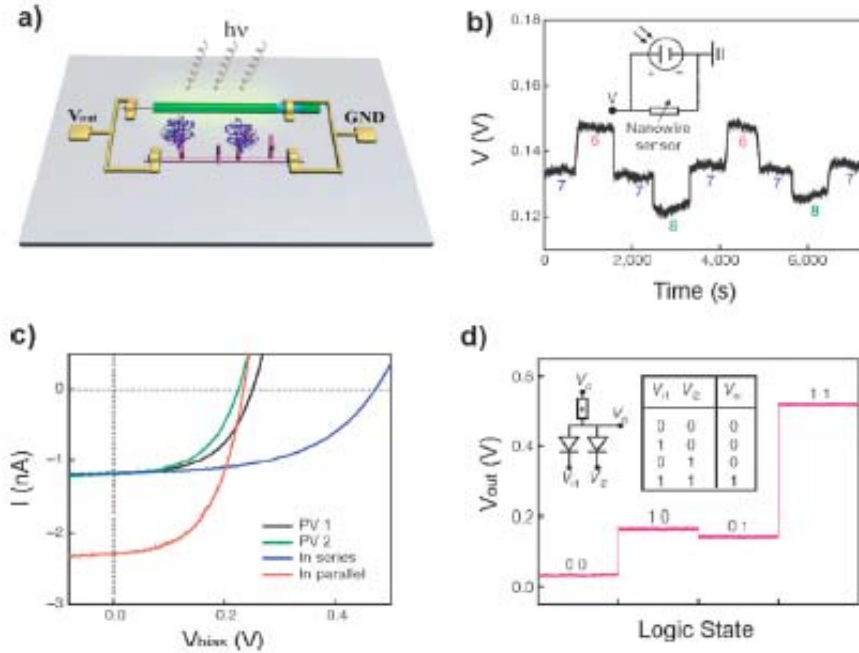
The axial  $p$ - $i$ - $n$  Si-nanowire photovoltaic devices we further characterized by measurement of temperature dependent device photovoltaic characteristics.  $V_{oc}$  and  $I_{sc}$  data for a  $p$ - $i$ - $n$  ( $i = 4 \mu\text{m}$ ) Si-nanowire device are shown in Figure 6b.  $V_{oc}$  exhibited a well-defined linear dependence on temperature with a slope of  $-2.97 \text{ mV/K}$ . Extrapolation of  $V_{oc}$  to the 0 K limit yielded a value of 1.12 V that is in agreement with the band-gap of single crystalline silicon. In addition,  $I_{sc}$  was found to increase weakly with temperature due to a decrease in band-gap with increasing temperature. These low temperature data further confirm that insertion of the  $i$ -segment is critical to improving the junction quality. Further insight into the role that junctions and interfaces play in controlling device performance was obtained through  $I_{sc}$  and  $V_{oc}$  data for  $p$ - $n$  and  $p$ - $i$ - $n$  axial devices recorded with illumination intensities from  $\sim 0.1$  to 6 suns. Significantly, analyses of these data yielded ideality factors  $n = 1.78$  and  $1.28$ , and saturation currents,  $I_0 = 102$  and  $6.14 \text{ fA}$ , for the  $p$ - $n$  and  $p$ - $i$ - $n$  Si-nanowire diodes respectively. These results show that introduction of the  $i$ -region dramatically reduces the saturation current, and

thus a large component of the leakage current in the diode. Lower leakage current improves the quality of the diode, which is reflected in the lower value of  $n$ , and leads to the observed larger  $V_{oc}$  due to reduced shunt losses (large parallel resistances) at the junction.

The PV properties of the  $p-i-n$  radial Si-nanowire diodes were characterized under identical conditions.  $I-V$  data recorded from one of the better devices (Figure 6c) yielded a  $V_{oc}$  of 0.260 V,  $I_{sc}$  of 0.503 nA, and  $FF$  of 55.0 %. The maximum power output ( $P_{max}$ ) for the Si-nanowire device at 1-sun is  $\sim 72$  pW, approximately 15 times larger than for the axial  $p-i-n$  structure. Notably,  $I-V$  data recorded on a single Si-nanowire from two devices with  $p$ -core to  $n$ -shell contact distances of 5.9 and 13.3 mm exhibited the same PV response, indicating that the  $n$ -shell is equipotential with radial carrier separation occurring uniformly along the entire length of the radial Si-nanowire. The apparent  $J_{sc}$  calculated using the projected area of the radial nanowire structure is  $23.9 \pm 1.2$  mA/cm<sup>2</sup>. The large  $J_{sc}$  in the radial nanowire device implies substantial absorption across the solar spectrum and efficient carrier collection. Such absorption is consistent with the nanocrystalline shell structure of the nanowires and previous studies of polycrystalline thin films, although the detailed nature of absorption will require further investigation. Finally, the apparent PV  $\eta$  of this device was  $3.4 \pm 0.2$  %.

In addition, the temperature dependence of  $I_{sc}$ ,  $V_{oc}$  and  $FF$  were characterized to understand better the behavior of the radial Si-nanowire PV devices (Figure 6d). Consistent with the observations in the axial structure,  $I_{sc}$  increases slightly with increasing temperature, as expected for increased light absorption due to decreasing band-gap with elevated temperature. Second,  $V_{oc}$  exhibits a substantial linear increase with decreasing temperature, where the slope ( $dV_{oc}/dT$ ) of -1.9 mV/K is close to the value (-1.7 mV/K) calculated in single crystalline Si solar cells. Interestingly,  $V_{oc}$  does not extrapolate to the single-crystal Si band gap as expected for a structure consisting of single-crystal core and polycrystalline shells. The observed increase in  $V_{oc}$  can be attributed to a reduced recombination rate at lower temperature, implies that Si-nanowire photovoltaic performance could be substantially improved at room temperature by reducing recombination processes.

Finally, we have demonstrated that our novel Si-nanowire PV elements can be readily interfaced with and provide power for nanoelectronics which consume power at the nano-watt scale. Figure 7a shows schematically a Si-nanowire radial PV element connected in parallel with a homogenous nanowire field effect transistor (FET) functioning as a nanowire protein sensor. The binding of charged proteins gate the channel of a nanowire FET leading to a change in nanowire resistance and a concomitant change in voltage drop across the nanowire sensor. Therefore, time dependent change in voltage output of the circuit can be used to monitor the binding/unbinding of analytes. For example, a single Si-nanowire PV device, operating under 8-sun illumination was used to drive a Si-nanowire pH sensor without additional power sources (Figure 7b). Measurements of the voltage drop across the  $p$ -Si-nanowire sensor (connected in parallel with the Si-nanowire PV power source) as a function of time showed reversible increase (decrease) in voltage as the solution pH was decreased (increased). Such changes are consistent with expected changes in resistance of the Si-nanowire with surface charge.



**Figure 7.** Integrated and self-powered nanosystems. **a)** Schematic of self-powered nanowire biosensor. **b)** Real-time detection of the voltage drop across a modified silicon nanowire at different pH values. The silicon nanowire pH sensor is powered by a single silicon nanowire photovoltaic device. **c)** Light I–V curves (1-sun, AM1.5G) of two silicon nanowire photovoltaic devices (PV 1 and PV 2) individually and connected in series and in parallel. **d)** Nanowire AND logic gate powered by two silicon nanowire photovoltaic devices in series.

Lastly, we demonstrated that multiple integrated Si-nanowire PV elements can drive larger loads, such as nanowire logic gates. Two radial Si-nanowire PV devices (black, green) interconnected in series (blue) and in parallel (red) yield  $V_{oc}$  and  $I_{sc}$  values, respectively, that are nearly the sum of the two constituent devices, as expected (Figure 7c). Notably, we have used two series interconnected Si-nanowire PV elements as the sole power supply to drive a nanowire-based AND logic gate (Figure 7d). Measured voltage output levels and a tabulated summary of input/output logic states demonstrated correct AND logic. Notably, such results highlight that even without full optimization, Si-nanowire PV elements can function effectively as integrated power sources in practical nanoelectronic device applications. With proper on-chip scale-up techniques, involving vertical and horizontal in-plane integration *via* epitaxial growth and high density printing, respectively, one could realize a nanowire PV enabled solar cell with much larger power output.

## B. Publications Stemming from Research Effort

1. C.J. Barrelet, J. Bao, M. Loncar, H.-G. Park, F. Capasso and C.M. Lieber, "Hybrid Single-Nanowire Photonic Crystal and Microresonator Structures," *Nano Lett.* **6**, 11-15 (2006).
2. O. Hayden, R. Agarwal and C.M. Lieber, "Nanoscale avalanche photodiodes for highly-sensitive and spatially-resolved photon detection," *Nature Mater.* **5**, 352-356 (2006).
3. W. Lu and C.M. Lieber, "Semiconductor nanowires," *J. Phys. D: Appl. Phys.* **39**, R387-R406 (2006).
4. R. Agarwal and C.M. Lieber, "Semiconductor nanowires: optics and optoelectronics," *Appl. Phys. A: Mater. Sci. Proc.* **85**, 209-215 (2006).
5. C. Yang, C.J. Barrelet, F. Capasso and C.M. Lieber, "Single p-Type/Intrinsic/n-Type Silicon Nanowires as Nanoscale Avalanche Photodetectors," *Nano Lett.* **6**, 2929-2934 (2006).
6. C.M. Lieber and Z.L. Wang, "Functional Nanowires," *MRS Bull.* **32**, 99-104 (2007).
7. Z. Zhong, C. Yang and C.M. Lieber, "Silicon Nanowires and Nanowire Heterostructures," *Nanosilicon* 176-216 (Ed. V. Kumar, Elsevier, 2007).
8. B. Tian, X. Zheng, T.J. Kempa, Y. Fang, N. Yu, G. Yu, J. Huang and C.M. Lieber, "Coaxial silicon nanowires as solar cells and nanoelectronic power sources," *Nature* **449**, 885-890 (2007).
9. W. Lu and C.M. Lieber, "Nanoelectronics from the bottom up," *Nature Mater.* **6**, 841-850 (2007).
10. O. Hayden, G. Zheng, P. Agarwal and C.M. Lieber, "Visualization of Carrier Depletion in Semiconducting Nanowires," *Small* **3**, 2048-2052 (2007).
11. Z. Zhong, C. Yang and C.M. Lieber, "Silicon Nanowires and Nanowire Heterostructures," *Nanosilicon* 176-216 (ed. V. Kumar, Elsevier, 2008).
12. F. Qian, Y. Li, S. Gradečak, H.-G. Park, Y. Dong, Y. Ding, Z.L. Wang and C.M. Lieber, "Multi-quantum-well nanowire heterostructures for wavelength-controlled lasers," *Nature Mater.* **7**, 701-706 (2008).
13. H.-G. Park, C.J. Barrelet, Y. Wu, B. Tian, F. Qian and C.M. Lieber, "A wavelength-selective photonic-crystal waveguide coupled to a nanowire light source," *Nature Photon.*, **2**, 622-626 (2008).

14. T.J. Kempa, B. Tian, D. R. Kim, J. Hu, X. Zheng and C.M. Lieber, "Single and Tandem Axial p-i-n Nanowire Photovoltaic Devices," *Nano Lett.* **8**, 3456-3460 (2008).
15. B. Tian, T.J. Kempa and C.M. Lieber, "Single Nanowire Photovoltaics," *Chem. Soc. Rev.* **38**, 16-24 (2009).
16. P. Xie, Y. Hu, Y. Fang, J.Huang and C.M. Lieber, "Diameter-dependent dopant location in silicon and germanium nanowires," *Proc. Natl. Acad. Sci. USA* **106**, 15254-15258 (2009).

### **C. Presentations of Research STEMMING FROM RESEARCH EFFORT**

#### **Invited Lectures**

**8 May 2007** – George C. Pimentel Memorial Lecture, University of California, Berkeley  
Invited talk: "Nanowire, Nanoscience and Emerging Nanotechnologies"

**24 May 2007** – Lund University Department of Physics Colloquium, Lund, Sweden  
Invited talk: "Nanowires, Nanoscience and Emerging Technologies"

**18 June 2007** – MITRE Corporation JASON Program Nanotechnology Study, San Diego CA  
Invited talk: "Nanowire and Nanotube Electronics"

**17 July 2007** – NSLS-II User Workshop, Brookhaven National Laboratory, Upton NY  
Invited talk: "Nanowires, Nanoscience & Emerging Technologies"

**21 August 2007** – 234<sup>th</sup> ACS National Meeting, Boston MA  
Langmuir Lecture: "Nanowires, nanoscience and nanotechnologies"

**28 September 2007** – James W. Neckers Memorial Lecture, Southern Illinois University, Carbondale IL  
Invited talk: "Nanowires, Nanoscience and Emerging Nanotechnologies"

**26 October 2007** – E. Roger Washburn Memorial Lecture, University of Nebraska-Lincoln  
Invited talk: "Nanowires, Nanoscience & Emerging Nanotechnologies"

**6 November 2007** – Cheng Tsang Man Professorship, Nanyang Technological University, Singapore  
Invited talk: "Nanowire Electronics: From Fundamental Device Properties to Three-Dimensional Integrated Circuits"

**8 November 2007** – Rohm and Haas Student Hosted Colloquium, Stanford University  
Invited talk: "Nanowires, Nanoscience, and Emerging Nanotechnologies"

**14 November 2007** – Beijing University of Technology International Exchange Symposium, Beijing China

Keynote: “Nanowires, Nanoscience and Emerging Nanotechnologies”

**15 November 2007** – 6<sup>th</sup> Chinese Conference for Advanced Functional Materials, Wuhan China

Keynote: “Nanowires, Nanoscience and Emerging Nanotechnologies”

**26 November 2007** – MRS Fall Meeting, Boston MA

Invited talk: “Nanowires: From Functional Building Blocks to Integrated Nanoelectronics”

**6 May 2008** - Institute for Molecular and Nanoscale Innovation Nanoscience Forum, Brown University, Providence, RI

Invited talk: “Nanowires, Nanoscience and Emerging Nanotechnologies”

**20 May 2008** - Institute for Molecules and Materials Symposium, Radboud University, Netherlands

Keynote Lecture: “Nanowires, Nanoscience and Emerging Nanotechnologies”

**10 June 2008** - Peking University, China

Invited talk: “Nanowires: A Platform for Nanoscience and Nanotechnology”

**11 June 2008** - Chinese Academy of Science, China

Einstein Lecture: “Nanowires, Nanoscience and Emerging Nanotechnologies”

**21 July 2008** - International Conference on Nanoscience and Technology 2008, Keystone CO

Plenary Talk: “Nanowires: A Platform for Nanoscience and Nanotechnology”

**12 August 2008** - Samsung Semiconductor Technical Advisory Committee Forum 2008: Silicon Technology for the Next Ten Years, Samsung Electronics

Main Presentation: “Nanowires: A Platform for Nanoscience and Nanotechnology”

**19 August 2008** - ExxonMobil Solid State Chemistry Faculty Fellow Award Symposium, American Chemical Society National Meeting, Division of Inorganic Chemistry

Invited talk: “Nanowires, NanoScience and Future Opportunities”

**27 September 2008** - Julius Springer Forum on Applied Physics 2008, Harvard University

Invited talk: “Nanowires: A Platform for Nanoscience and Nanotechnology”

**2 December 2008** - Materials Research Society Fall Meeting 2008

Session Chair and Invited Talk: “Nanowires: A Platform for Nanoscience and Nanotechnology”



**3 December 2008** - NSF Nanoscale Science and Engineering Grantees' Conference 2008, National Science Foundation

Keynote Talk: "Nanowires: A Platform for Nanoscience and Nanotechnology"

**9 March 2009** - Scientific Inauguration of the Centre for Research on Adaptive Nanostructures and Nanodevices (CRANN), Dublin, Ireland

Plenary Address: "The Opportunities & Challenges Facing Nanotechnology"

**7 April 2009** – University of Pittsburgh Department of Chemistry

Invited lecture: "Nanowires: A Platform for Nanoscience & Nanotechnology"

**18 April 2009** – 73<sup>rd</sup> Annual Intercollegiate Student Chemists Convention, Franklin & Marshall College

Keynote Talk: "Nanowires as a Platform for Nanoscience and Nanotechnology"

**29 April 2009** - Scientific Symposium: Material Challenges for Clean Energy in the New Millennium, Northeastern University

Invited talk: "Nanowires as solar cells and nanoelectronic power sources"

**20 May 2009** – Central Regional Meeting of the American Chemical Society, Cleveland, OH

Plenary talk: "Nanowires: A Platform for Nanoscience and Nanotechnology"

**18 August 2009** – 238<sup>th</sup> National American Chemical Society Meeting, Washington, D.C.

Inorganic Nanoscience Award Lecture: "Nanowires as a Platform for Nanoscience and Nanotechnology"

### **C. M. Lieber Group , Harvard University**

#### **Invited or Contributed Talks/Posters**

**24 January 2007** – SPIE Photonics West 2007, San Jose CA

"Nanowire photonic crystal waveguide and active diode"

**Hong-Gyu Park – contributed talk**

**24-25 January 2007** – GRC Renewable Energy: Solar Fuels, Ventura CA

"Single core/shells Si nanowire photovoltaic devices"

**Bozhi Tian – contributed poster**

**9 April 2007** – MRS Spring Meeting, San Francisco CA

"Multicolor Nanolasers from Individual Multi-quantum Well Nanowire Heterostructures"

**Fang Qian – contributed talk**

**10 April 2007** – MRS Spring Meeting, San Francisco CA

"Nanowire Heterostructures for Nanophotonics"

**Fang Qian – award talk**

**12 April 2007** – MRS Spring Meeting, San Francisco CA  
“Advances in Nanowire Photonics”

**Fang Qian – invited talk**

**25 October 2007** – 20<sup>th</sup> Annual IEEE Lasers and Electro Optics Society Meeting, Lake Buena Vista FL

“Semiconductor Nanowire Lasers”

**Fang Qian – invited talk**

**25 March 2008** – 2008 Spring Materials Research Society Meeting

“Single Silicon Nanowires as Solar Cells and Nanoelectronic Power Sources”

**Bozhi Tian, contributed talk**

**25 March 2008** – 2008 Spring Materials Research Society Meeting

“Single and Tandem Axial p-i-n Nanowire Photovoltaic Devices”

**Thomas Kempa, contributed Poster**

**26 March 2008** – 2008 Spring Materials Research Society Meeting

“Vertically- Integrated Three-Dimensional Nanowire CMOS Circuits”

**SungWoo Nam, contributed Talk**

**16 June 2008** – European Science Foundation’s Meeting on Nanotechnology for Renewable Energy, Obergurgl, Austria

“Nanowire Structures as Novel Photovoltaic Elements”

**Thomas Kempa, Invited Talk**

**27 September 2008** – Julius Springer Forum on Applied Physics 2008, Harvard University

“Modulation- doped Nanostructures as Fully-integrated Photovoltaic Elements”

**Bozhi Tian, Invited Poster**

**10 November 2008** – 2008 Annual IEEE-LEOS Meeting, Newport Beach, CA

“Silicon Nanowire Heterostructures as Solar Cells and Nanoelectronic Power Sources”

**Thomas Kempa, Invited Talk**

**2 December 2008** – 2008 Fall Materials Research Society Meeting

“Silicon Nanowire Heterostructures as Solar Cells and Nanoelectronic Power Sources”

**Bozhi Tian, Invited Talk (Graduate Student Award Talk)**

**3 December 2008** – 2008 Fall Materials Research Society Meeting

“Single and Tandem Axial Nanowire Solar Cells”

**Thomas Kempa, Contributed Talk**

**20 March 2009** – CCB Student/Postdoc Seminar Series, Harvard University

“Silicon nanowire heterostructures for photovoltaic applications”

**Bozhi Tian, Invited Talk**

**5 June 2009** – IEEE/LEOS International Semiconductor Laser Workshop 2009  
“Coaxial III-nitride Nanowire Optoelectronics”

**Yajie Dong, Invited Talk**

**24 June 2009** - MIT/Optical Society of America Meeting on Optics and Photonics for  
Advanced Energy Technology, MIT  
“Nanowires as Solar Cells and Nanoelectronic Power Sources”

**Tom Kempa, Invited talk**

**16 August 2009** – 238th ACS National Meeting & Exposition  
“Single Nanowire Photovoltaics”

**Bozhi Tian, Contributed talk**