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TOWARDS A NARROWBAND PHOTONIC SIGMA-DELTA DIGITAL ANTENNA

by

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14. ABSTRACT

A narrow-band photonic sigma-delta digital antenna is described as a system intended to provide a proof of concept for the use of photonics technology in the sampling of wide-band radio frequency (RF) signals.

The ability to sample wide-band RF signals is an important requirement in modern electronic warfare (EW) systems where a determination of the existence of complex and often difficult to detect signals is sought. As an example, the class of signals referred to as low probability of intercept (LPI) is becoming increasingly common-place with the evolution of modern radar and communication systems. The emergence of this class has led to a concomitant demand for receivers that can provide the necessarily high sensitivity to detect these signals thereby enabling their classification in an electronic intelligence (ELINT) database or jamming using electronic attack (EA).

The described system is designed to oversample the analog RF signal exciting an antenna at a rate at least 10 times higher than the Nyquist rate relative to the RF signal frequency (that is, twice the RF signal frequency).

Numerous aspects of the development of the described concept demonstrator are presented and extended to outline the requirements for progressing the technology to wide-band capability.

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TABLE OF CONTENTS

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GLOSSARY

ADC	Analog-to-Digital Conversion/Converter
AM	Amplitude Modulation
APC	Physical Contact, Angle Polished Convex In Fiber Connectors
BW	Bandwidth
CAVF	Constant-Amplitude, Variable-Frequency
CJSEW	Center for Joint Services Electronic Warfare
COTS	Commercial-Off-The-Shelf
CP	Circular Polarized
CW	Continuous Wave
DAC	Digital To Analog Conversion/Converter
DC	Direct Current
DFB	Distributed Feedback
DPO	Digital Phosphor Oscilloscope
DSF	Defense Science Fellowship
DSHI	Delayed Self Heterodyning (*Homodyning*) Interferometer
DSTO	Defense Science and Technology Organization
EA	Electronic Attack
ELINT	Electronic Intelligence
EM	Electro-Magnetic
EP	Elliptically Polarized
ES	Electronic Support
ESEP	Engineer and Scientist Exchange Program (also SEEP)
EW	Electronic Warfare
EWRD	Electronic Warfare and Radar Division
FC	Mechanical Description of Fiber Connector – Screw Type with Key Alignment
FM	Frequency Modulation
FMCW	Frequency Modulated Continuous Wave
FWHM	Full-Width at Half-Maximum

GaAIAs	Gallium Aluminum Arsenide
GPIB	General Purpose Interface Bus
HL	Horizontal Linear (Polarization)
IC	Integrated Circuit
IF	Intermediate Frequency
IIR	Infinite Impulse Response
kTB	Thermal Receiver
LD	Laser Diode
LH	Left-Hand (Polarization)
$LiNBO_3$	Lithium Niobate
LO	Local Oscillator
LP	Linear Polarization
LPI	Low Probability of Intercept
LSB	Least Significant Bit
LTA	Long-Term Attachment
MMF	Multi-Mode Fiber
MOU	Memorandum Of Understanding
MS/s	MSamples/s
MZI, MZM	Mach-zehnder Interferometer, Modulator
NIPO	Navy International Program Office
NPS	Naval Postgraduate School
ONR	Office of Naval Research
OOAM	On-Off Amplitude Modulated/modulation
OSA	Optical Spectrum Analyzer
OSR	Over-Sampling Ratio
PC	Physical Contact, Polished Convex in Fiber Connectors
PCM	Pulse Code Modulated/Modulation
PD	Photodetector, Photodiode
PDM	Pulse Density Modulated/modulation
PDS	Product Datasheet
PM	Phase Modulator

PM	Polarization Maintaining
PMF	Polarization Maintaining Fiber
PRF	Pulse Repetition Frequency
PSD	Power Spectral Density
RF	Radio Frequency(ies)
RFSA	RF Spectrum Analyzer
RH	Right-Hand (Polarization)
RMS	Root Mean Square
RSNS	Robust Symmetrical Number Systems
RSD	Relative Standard Deviation
SEEP	Scientist and Engineer Exchange Program (also ESEP)
SHR	Super Heterodyne Receiver
SM	Single Mode
SMF	Single Mode Fiber
SOA	Semi-Conductor Optical Amplifier
SOI	Signal of Interest
SPL	Spurious Peak Level
SQNR	Signal to Quantization Noise Ratio
ST	Mechanical Description of Fiber Connector - bayonet type
Sync	Synchronization
TE	Transverse Electric
TE	Thermo Electric
TH	Thermistor
TM	Transverse Magnetic
UCSB	University Of California, Santa Barbara
USB	Universal Serial Bus
VACF	Variable-Amplitude, Constant-Frequency
VAVF	Variable-Amplitude, Variable-Frequency
VL	Vertical-Linear (Polarization)
VRC	Variable Ratio Couplers
ΣΔ	Sigma Delta

EXECUTIVE SUMMARY

In October 2007, funding was approved by the United States Office of Naval Research for a three year New Start research project titled "Cueing Receivers for Fast Jammer Response Management".

The research is a collaborative project between the **Naval Postgraduate School's (NPS) Center for Joint Services Electronic Warfare (CJSEW)**, the **Electronic Warfare and Radar Division (EWRD)** of the Australian **Defence Science and Technology Organisation (DSTO),** and the **University of California Santa Barbara (UCSB)**, **Department of Electrical and Computer Engineering (ECE)**.

The international collaboration with DSTO was conducted over a 12 month term under the **Engineer and Scientist Exchange Program (ESEP)** in accordance with a **Memorandum of Understanding (MOU)** between the respective Departments of Defence of the USA and Australia. This program was conducted with the oversight of the **United States Navy International Programs Office (NIPO)**.

The collaboration with UCSB is for three years.

The principal objective of the project is to develop an experimental prototype of a photonic sigma-delta wide-band cueing receiver. The prototype is intended to digitally sample a **radio frequency (RF)** signal typical of **low probability of intercept (LPI)** emitters directly from an antenna source. The expected advantage of this approach is the elimination of signal down-conversion to intermediate and base-band frequencies, and its associated noise contribution. Other advantages include the reduced quantization noise through the use of over-sampling and the dispersion of the noise power spectral density beyond the signal band.

The DSTO contribution to this collaborative project is described in this report in the context of a proof of concept demonstrator for a narrow-band photonic sigma-delta digital antenna. This demonstrator is a scaled version of the wide-band receiver which utilizes many of the same components while allowing the relaxation of band width requirements of the necessary measurement and test equipment. Some components from

the wide-band receiver were substituted, such as the resonator which is a precision device not compatible with a narrow-band application.

The approach presented here for the narrow band receiver provides insight into many of the integration issues of its individual components that have yet to be explored with the wide-band receiver system architecture.

The research performed with this demonstrator allowed the work to be accommodated within a budgetary constraint of $40k USD, which was the **Office of Naval Research** (**ONR)** funding allocated to NPS for the first year of the project.

A summary of progress made under this project is presented, emphasizing DSTO's contribution towards the research and development of the prototype, from individual component specification to the design and conduct of experimental measurements. This has led to the rationalization of the original design of the wide-band receiver, which is presented here, as well as a better understanding of the requirements for components and sub-systems of the design.

An outline is submitted for the future developmental work, with a description of potential issues that may arise with the wide-band receiver.

LIST OF FIGURES

LIST OF TABLES

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I. INTRODUCTION

Radar jamming is commonly defined as the denial of access to all or part of the electromagnetic spectrum (in the **radio frequency (RF)** domain). During military operations, jamming can be used to protect assets and personnel from hostile threat systems, thereby enabling successful mission completion. There are a number of ways jamming can be applied to achieve these objectives, but such discussion is beyond the scope of this report.

The successful jamming of threat radars is predicated by the timely detection of the electromagnetic (RF) signals they emit. The evolution of radar technology has naturally progressed to counter the adverse effects of jamming which seek to degrade radar functionality. The development of modern and future digital radar systems has led to wide-band RF waveforms that are difficult to detect and classify. This technology is commonly referred to as **Low Probability of Intercept (LPI)**.

The ability to sample wide-band RF signals is an important requirement in modern **electronic warfare (EW)** systems where a determination of the existence of complex and often difficult to detect signals is sought. The emergence of the LPI class of signals has led to a concomitant demand for receivers that can provide the necessarily high sensitivity to detect these signals thereby enabling their classification in an **electronic intelligence (ELINT)** database or jamming using **electronic attack (EA)**.

The detection of LPI signals is a significant challenge to the design of receivers whose function is to classify radars or emitters and cue a jammer or some other system towards that threat. An LPI signal may consist of a low power **frequency modulated continuous wave (FMCW)** signal. At long ranges and wide bandwidths, a typical **electronic support (ES)** receiver may have difficulty detecting this signal if it is indistinguishable from the noise background.

Sources of noise can include environmental clutter, however, a major issue is overcoming the receiver noise which, in many existing receivers results in insufficient sensitivity to detect LPI signals. **Thermal receiver or kTB** noise describes the power spectral density of the receiver noise as a function of the receiver's operating temperature and bandwidth.

An additional significant source of noise is the result of mixing and sampling, wherein the RF analog signal is first down-converted to **intermediate frequency (IF)** and baseband. The down-conversion is achieved by mixing the RF with a **local oscillator (LO)** signal, which is the basis of a **super-heterodyning receiver (SHR)**. This is necessary for conditioning the signal of interest before it is sampled and digitized using an **analog-to-digital converter (ADC)**, but it can introduce a significant amount of noise. Additional noise is introduced in the form of quantization noise during the ADC stage. Existing receivers typically perform sampling at the Nyquist rate (equivalent to twice the maximum bandwidth of the RF signal of interest).

This description of a conventional digital receiver is indicative of the challenges faced in detecting wide-band LPI signals. In order to sample a wide-band signal at its Nyquist rate at the ADC stage, a much higher bandwidth is required from the down-conversion stage. However, in order to provide this bandwidth, the SHR would introduce even greater harmonic noise reducing the sensitivity of the receiver. There is also an issue of timing jitter from clock signals operating at the 10-100 GHz range. While this can be addressed somewhat by a channelized receiver design, this adds to the complexity of the receiver and does not address the quantization noise from the ADC stage.

An alternative approach to wide-band Nyquist sampling involves the application of photonics to *oversample* wide-band signals. This would require much higher frequency pulses, which can be produced with the requisite stability using a mode-locked laser. These pulses can be amplitude modulated with the amplitude of the signal of interest using RF electro-optic modulators.

The expected advantages of the use of photonics in this application include the elimination of a down-conversion stage and its associated noise, the reduction of quantization noise in the ADC due to spectral shaping of that noise outside the signal band, and the ability to digitize signals at much faster rates than possible with electronics. A photonic receiver architecture, such as the one described in this report, also lends itself to integration onto a substrate, allowing direct conversion to be performed at the receiver antenna. Indeed, such an arrangement can be referred to as a digital antenna.

In this report, a narrow-band photonic sigma-delta digital antenna is described as a system intended to provide a proof of concept for the use of photonics technology in the sampling of wide-band **radio frequency (RF)** signals.

While the described system and its potential broader application to wide-band signals offer some exciting possibilities for the future, it is an objective of this report to provide a balanced assessment of the viability of photonic ADC technology.

A. REPORT OUTLINE

In **Chapter** I, the relevance and importance of this research is briefly described. This is followed by a brief outline of the challenges of using conventional receivers to sample wide-band LPI signals and how these challenges can be addressed using photonics. An outline of the report content is also given.

In **Chapter II**, photonic analog to digital conversion is introduced as part of a review of the literature. This is followed by a summary of previous research efforts at NPS.

In **Chapter III**, a comparison of generic conventional (Nyquist sampling) ADCs with some oversampling ADC architectures is presented highlighting their differences with respect to **Signal to Quantization Noise Ratio (SQNR)**.

In **Chapter IV**, the discussion of **Chapter III** is extended to photonic sigma-delta ADC, with a presentation of the design considerations for both wide-band and narrow-band applications. The reasons for considering this photonic approach in preference to other approaches (including electronic) are also reiterated. A brief description of the original proposed architecture is provided and revisions to this original NPS design are also presented with justification.

In **Chapter** V, the experimental and developmental effort undertaken to build the narrow-band photonic sigma-delta is presented. A description of the methods and results of the various characterization studies performed on the components and sub-systems comprising the narrow-band photonic sigma-delta digital antenna is included in this discussion.

Finally, this work is summarized in **Chapter VI** where recommendations are also made for the ongoing development of the wide-band receiver.

II. PHOTONIC ANALOG TO DIGITAL CONVERSION TECHNOLOGIES

For most applications involving analog to digital conversion the requirements are high speed (sampling rate), high dynamic range and low quantization noise. Photonics technology has shown great potential to achieve these hitherto conflicting requirements through the ongoing collective efforts of many researchers over the last 40 years. Indeed, many of the limitations of photonic ADC that have been identified throughout this period have been continuously improved through advancements in the fields of lasers and electro-optics, as well as solid state electronics.

Valley **[1]** has made a comprehensive review of photonic ADC with a compilation of works dating back to 1970. With a deliberate emphasis towards systems with RF input in the electronic domain and digitized output in the electronic domain, he excluded applications in image digitization and optical communications. Valley categorized various systems in terms of their degree of photonic integration. The four categories were **(1)** photonic assisted electronic ADC for performance improvement; **(2)** photonic sampling and electronic quantizing ADC; **(3)** electronic sampling and photonic quantizing ADC; and, **(4)** photonic sampling and quantizing ADC. It should be reiterated that all 4 categories invariably require some form of electronic sampling and quantization.

The wide-band photonic sigma-delta ADC system described in this report belongs to the 2nd category. Sampling is achieved through the amplitude modulation of the RF input onto a pulsed photonic carrier. High-speed photo-detectors are then used to convert the optical pulses to electronic pulses and the output is input to high-speed electronic comparators where the signal is quantized according to some threshold test. These electronic signals are used, in one case, to send accumulate up or down commands, and in the other case to feedback a signal to be added/or subtracted from the antenna fed input signal. The achievable sampling rate is therefore constrained by the bandwidth of these comparators and the feedback circuit.

A. NPS CONTRIBUTIONS TO PHOTONIC ADC RESEARCH

Many of the innovations made in photonic ADC within NPS are described in the book entitled “Advanced Techniques for Digital Receivers” by Pace **[2]**.

Some of the key innovations are listed as follows:

- Photonic ADC using **Robust Symmetrical Number Systems (RSNS) [3,4]**
- Femto-second Erbium-doped GaAs fiber sigma laser **[5]**
- Oversampling sigma-delta photonic ADC with a bulk fiber-lattice accumulator **[6]**

In addition to these references, there are a number of NPS Master’s theses which describe various aspects of the photonic sigma-delta ADC dating back to the early 1990s **[**6**,7,8,9]**. These works are focus mainly on modeling and simulation using MATLAB and SIMULINK.

The RSNS and fiber laser works are not directly relevant to the work presented here and will not be discussed further.

In 2000, Gillespie **[**9**]** presented a thesis entitled “*The Design and Experimental Evaluation of an Electro-Optical Sigma-Delta Modulator for Wideband Digital Antennas*”. Gillespie focused his dissertation on the design considerations, construction process and experimental evaluation of the electro-optical sigma-delta ADC. He also compared his results with various computer models. Gillespie’s approach was similar to the one presented in this report, where he focused on the construction of a low bandwidth prototype. While Gillespie did not achieve a functional ADC prototype system, he outlined a number of issues which were contributory factors to this lack of success. Many of these issues are addressed in the new research presented in this report along with additional issues, which had not been considered until now.

With the exception of Gillespie’s work and the unpublished and incomplete work of Schroder and Alves (NPS students) in 2005 **[10]**, there has been little other hardware development of the architecture. In 2005, Pace, Schroder and Alves attempted to reimplement the photonic ADC design using a bulk fiber lattice accumulator (also see Moslehi *et al.* **[11, 12]**) in the place of the electro-optic resonator featured in **Figure IV.1**. This work was intended as a follow-up on the recommendations resulting from Gillespie's work. Pace *et al.* found the accumulator device was still very sensitive to fluctuations in the phase coherence of the laser pulses, despite the use of a narrower line-width laser source. This finding was the basis of their conclusion that the electro-optic resonator should be a very high precision device with a delay path matching the photonic PRF and a waveguide structure that provides a high degree of phase and polarization control. This requirement is intended to be met in the design of the ring resonator being conducted by UCSB as their contribution to the wide-band ADC architecture. Both the lattice accumulator and the resonator concepts will be discussed in more detail in **Chapters IV and** V.

The work presented here addresses the challenges involved with developing the photonic sigma-delta ADC from a concept to experimental demonstration. Of particular concern is the fact that no proof of concept has so far been achieved to verify the validity of the proposed architecture. Given the significant cost of developing a wide-band receiver, including the necessary test and measurement instrumentation, experimental development of a narrow-band photonic sigma-delta ADC using existing infrastructure and equipment is a prudent risk mitigation strategy.

B. UTILIZATION OF INTEGRATED PHOTONIC DEVICES

This research utilizes a range of integrated photonic devices, for a variety of reasons. In the developmental environment of the laboratory, the use of integrated photonics avoids such complications as misalignment, which is typically encountered in free air systems. However, the primary reason is that once developed, the wide-band digital antenna system can be fabricated onto a substrate. This would mean a fully contained and miniaturized system with minimized internal losses and maximized versatility in installation.

In the laboratory environment, the use of integrated devices interconnected with optical fiber allows experiments to be conducted while minimizing the ocular hazard. Moreover, the interconnection allows for the optimal alignment of components to be maintained and the ability to accurately quantify the insertion loss of each component in the system.

Among the integrated photonic devices used are **Mach Zehnder modulator (MZM)** interferometers, a **phase modulator (PM)**, a **continuous-wave (CW) laser diode (LD)** source **distributed feedback (DFB)** and, in some implementations, a **semi-conductor optical amplifier (SOA)** or similar.

The MZM interferometers and PM comprise electro-optic lithium niobate crystals containing electrodes which, when stimulated by an electric current supplied via the modulator's RF inputs, undergo a change in refractive index. The amplitude of an optical pulse passed through such devices can be modulated with the instantaneous amplitude of the RF input voltage. Moreover, the modulation can be used to switch the pulse off or on if these devices are biased to act as switches.

As lithium niobate crystals are also birefringent, they are polarization sensitive with respect to the input laser radiation. The laser diode source is similarly configured for a single output polarization mode. For these reasons, polarization maintaining fiber is used to minimize losses due to torsional stresses applied to the optical fibers.

The specific features and relevant issues of the equipment set-up are discussed in **Chapters IV and** V.

III. ELECTRONIC AND PHOTONIC RECEIVERS: A COMPARATIVE ANALYSIS

In this Chapter, a comparison of a generic electronic (conventional) receiver with a photonic sigma-delta ADC receiver is presented highlighting their respective performance capabilities in the presence of basic LPI radar signals.

The discussion on conventional electronic ADC receivers will focus on Nyquist sampling.

Analog-to-Digital Conversion (ADC) is an important area of signal processing wherein real-world continuous time-varying analog signals are converted into the discrete-time digital domain.

The digital representation of an analog signal enables many other signal processing operations to be performed, and makes for easier data transmission and storage.

ADC is typically a two-step process: the temporal discretization of the signal and the amplitude quantization of the signal. Temporal discretization is sampling the signal periodically at a rate called the sampling frequency, f_S. Amplitude quantization is the conversion of the instantaneous signal amplitude (corresponding to a given sample) from an analog value to a digital or binary number representation. The assignment of a discrete value to a continuous variable means that it is not possible to perform this conversion without error and this error is known as the quantization error.

Quantization error can be minimized by increasing the resolution of the quantizer. The method used to achieve this depends on the method used to sample the analog signal and, hence, this will be discussed in the appropriate sections that follow.

A. CONVENTIONAL (NYQUIST) SAMPLING

The conventional approach to sampling analog signals is to select a sampling frequency which is at least twice the highest frequency contained in the **signal of interest**

(SOI) – the Nyquist sampling rate, f_{NS}. This rate is the minimum condition specified in the Nyquist-Shannon sampling theorem for the lossless digitization of a band-limited continuous time signal.

The term 'lossless' is a theoretical idealization which is unachievable in practice as pure band-limiting cannot be implemented with physical filters. The digital realization of the sampled signal is therefore mathematically represented as an infinite series where the higher frequency components converge to zero. The realistic interpretation of the Nyquist-Shannon sampling theorem is that the digitization loss or *aliasing*, is minimized when the band-limited signal is sampled at the Nyquist rate.

When the highest frequency contained in a signal, that is its bandwidth, is known the Nyquist rate is readily deduced. However, such information is not always known, at least with absolute certainty. Moreover, the design of the receiver typically dictates the maximum frequency which can be used to sample signals, based on both the expectation of the largest frequency signal that the receiver would encounter, as well as the limitations of receiver sub-systems such as ADC speed. This maximum frequency is the Nyquist frequency of the receiver.

In order for a receiver to be able to avoid the aliasing of signals with bandwidths above its Nyquist frequency, a low-pass filter is introduced with a cut-off frequency at half the Nyquist frequency. A consequence of this design feature is that wide-band signals with bandwidths larger than that of the receiver will not be fully sampled. Hence, conventional receivers employing Nyquist sampling may have severely limited capability to adapt to the sampling of wide-band emitters which may emerge once they have been deployed into service.

1. Conventional ADC Techniques

Conventional ADC techniques include successive approximation registers, dual slope integrating, sub-ranging and flash converters.

A successive approximation converter provides a fast conversion of a momentary value of the input signal. It works by first comparing the input with a voltage which is half the full scale input range. If the input exceeds this threshold level, the ADC compares it with three-quarters of the range, and so on. Twelve such steps give 12-bit resolution. While these comparisons are taking place the signal is frozen in a *sample and hold* circuit. After A-D conversion the resulting bytes are placed into either a pipeline or buffer store. A pipeline store enables the ADC to do another conversion while the previous data is transferred to the computer. Buffered ADCs place the data into a queue held in buffer memory. The computer can read the converted value immediately, or can allow values to accumulate in the buffer and read them when it is convenient. This frees the computer from having to deal with the samples in real time, allowing them to be processed in convenient batches without losing any data.

The dual slope integrating converter reduces noise but is slower than the successive approximation type. It lets the input signal charge a capacitor for a fixed period and then measures the time for the capacitor to fully discharge at a fixed rate. This time is a measure of the integrated input voltage, which reduces the effects of noise.

Sub-ranging or pipelined ADCs are high speed converters capable of digitizing at 100 MSamples/s at 8-bit resolution. In an 8-bit implementation, a sub-ranging ADC will use two 4-bit stages to convert the upper and lower 4 bits, respectively. The upper stage ADC digitizes a sample and sends its output to a buffer as well as to a 4-bit **digital-to-analog converter (DAC)**. The output of the DAC is subtracted from the sampled input voltage and the resulting analog voltage is input to the lower stage ADC.

Flash ADCs, particularly of the parallel type, are the fastest conventional ADC type with **commercial-off-the-shelf (COTS)** models able to sample at rates ranging from tens of **MSamples/s (MS/s)** up to 5 GS/s. Some proprietary designs have reportedly achieved sample rates up to 20 GS/s **[13]**. The typical resolution for flash ADCs is 8-bit, although 10-bit resolution is achievable.

Parallel flash converters use a bank of comparators that compare an input voltage against a set of reference voltages across a resistor network. The reference voltages start at a value equivalent to one-half the **least significant bit (LSB)** and increase in voltage increments equivalent to one LSB for each comparator. Hence, each comparator's output represents one LSB. For an 8-bit flash converter, 255 comparators are required (2^8-1).

The common feature of all these ADC techniques is that they all sample an analog signal at, or slightly above, its Nyquist rate. Without any further reference to their specific architectures, we illustrate in **Figure III.1** a basic signal model of a conventional ADC **[**9**]**.

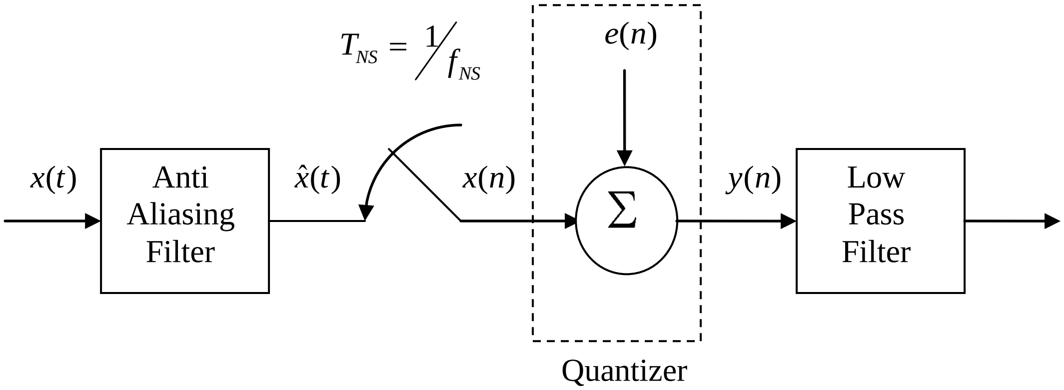

Figure III.1 Signal model of a conventional Nyquist-sampling analog-to-digital converter.

The input analog signal $x(t)$ is passed through an anti-aliasing filter to avoid ambiguous reconstruction of the signal from its samples. The resulting Nyquist band-limited output signal $\hat{x}(t)$, is then sampled once every T_{NS} seconds, creating the discrete-time sampled signal $x(n)$. The sampled values of amplitude are assigned discrete values by the quantizer, a process which introduces an inherent error in the form of quantization noise $e(n)$. The result is represented in the digital signal $y(n)$. A low pass filter is included at the output to reject high frequency components introduced by the sampling and quantization processes.

2. Digital Modulation [14]

Amplitude quantization and sampling in time are the basis of all digital modulation techniques. Quantization is a common source of error which must be taken into account when designing modulators.

Consider a uniform quantization process that rounds off a continuous amplitude signal $x(t)$ to odd integers in the range $-5 \le x\ \ t\ \ \le 5$ volts. For convenient illustration, assume a quantization level spacing of $q = 2$. The quantized signal $y(n)$ can be represented as a linear function $Gx(n)$ with an error $e(n)$, according to **Equation (III-1)**.

$$y(n) = Gx(n) + e(n)$$

(III-1)

The slope G is a gain term passing through the centre of the quantization characteristic such that for non-saturating signals input to the quantizer (i.e., $-6 \le x \le 6$), the error is bounded by $\pm q/2$.

The error is completely defined by the input. If the input changes randomly between samples[1] with amplitude comparable to, or greater than the level spacing, and without causing saturation, then the error is uncorrelated from sample to sample and has equal probability of taking any value in the range $\pm q/2$. If it is further assumed that the error is statistically independent of the signal, then it can be considered as noise, allowing some important properties of the modulator to be deduced.

In many cases, experimental measurements have confirmed these properties, but there are two important possible exceptions: constant input, and regularly changing input based on multiples and factors of the step size between sample times as can happen in feedback circuits.

For a uniformly distributed quantization error e having equal probability of taking any value in the range $\pm q/2$, its mean square value (variance) is described by **Equation (III-2)**:

---

[1] - This randomization can be the result of timing jitter in the sampling process and other sources, which will be explained in **Sub-Section 3**.

$$e_{RMS}^2 = \frac{1}{q}\int_{-q/2}^{+q/2} e^2 de = \frac{q^2}{12}$$

(III-2)

When a quantized signal is sampled at a frequency, $f_{NS} = 1/T_{NS}$, all of its power folds into the frequency band $0 \le f \le f_{NS}/2$ (assuming the one-sided power spectral density representation where all the power is in the positive range of frequencies).

For white quantization noise, the power spectral density (PSD) of the sampled noise is described in **Equation (III-3)**:

$$E(f) = e_{RMS}\sqrt{\frac{2}{f_{NS}}} = e_{RMS}\sqrt{2T_{NS}}$$

(III-3)

This power spectral density of Nyquist sampled noise will be discussed further in **Section III.B** where it will be compared with the PSD of oversampled noise.

3. Sources of Noise Randomizing the Quantization Error

There are numerous other sources of noise in the ADC system featured in **Figure III.1.** The input analog signal will have some electronic thermal noise associated with it, especially if some pre-amplification signal conditioning is applied. This would be additional to the jitter introduced by the clock reference used in the sampling process.

These noise sources will combine to induce fluctuations in the instantaneous value of amplitude of the input signal. The difference between the quantized value of the signal and its actual value is the quantization error or rounding error. For a rounding quantizer, the discussion from the previous section explained that between two adjacent half-quantization levels (or bits of the ADC), the instantaneous value of quantization error is a uniformly distributed random variable. This is illustrated in **Figure III.2**.

In some cases, such as in ADC systems with large quantization levels (low resolution) and very stable clocks producing low jitter; and where input signals have low noise levels, there may be insufficient noise to achieve a uniform distribution of the quantization error across the range of adjacent half-quantization levels. This will result in distortion of the output as the ADC will tend to favor one quantization level over another when the sample amplitude falls between adjacent quantization levels. This is particularly problematic in cases of very low input signal level. This problem is addressed by the addition of a dither signal to the quantization stage to randomize the quantization error. The effect is an increased effective dynamic range for a small noise penalty. This additional dither signal can be easily removed using a suitable filter at the output of the ADC.

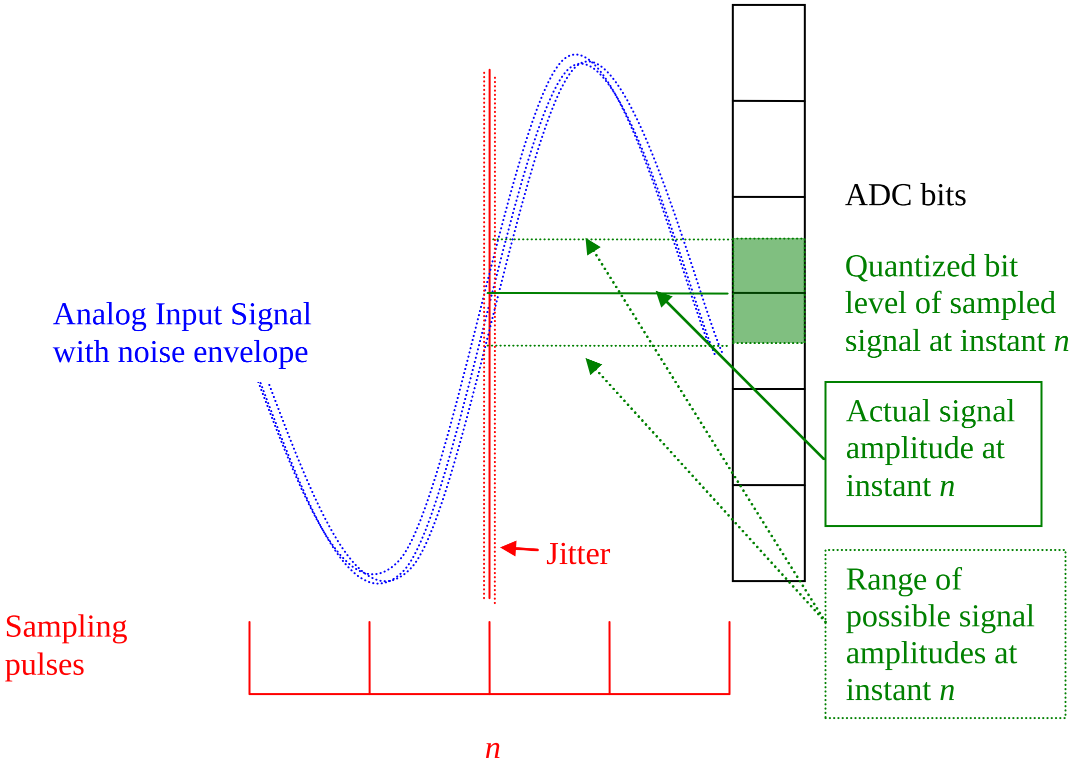

Figure III.2 **The effects of signal thermal noise and sample timing jitter on the quantization process of conventional ADC techniques.**

4. Signal to Quantization Noise Ratio

In the previous sections, the effect of various sources of noise on the quantization error illustrated how quantization error could be considered a random process. It should be noted that the quantization error is assumed to be statistically independent of the input signal. In the absence of any applied dither, it is assumed that the ADC resolution is more than 5 bits to ensure the input signal and quantization error are uncorrelated.

Therefore, the variance of uniformly distributed quantization error is from **Equation (III-2)**:

$$\sigma_{RMS}^2 = \frac{q^2}{12}$$

For a Q-bit ADC, the peak-to-peak voltage of the largest signal applied to the input of the ADC without saturation is described by **Equation (III-4)**:

$$V_{PPK} = 2^Q q$$

(III-4)

For a sinusoidal input signal, the corresponding root mean square (RMS) voltage is described by **Equation (III-5)**:

$$V_{RMS} = \frac{V_{PPK}}{2\sqrt{2}}$$

(III-5)

The signal to quantization noise ratio (SQNR) is written down in **Equation (III-6)**:

$$SQNR = \frac{V_{RMS}^2}{\sigma_{RMS}^2}$$

(III-6)

This, after substitution of the various preceding terms becomes **Equation III-7**:

$$SQNR = 6.02Q + 1.76\,\mathrm{dB}$$

(III-7)

Hence, the SQNR will increase by approximately 6 dB for each unit increase in bit resolution, Q, for the ADC. Unfortunately, the number of bits cannot be increased without bound, as fabrication issues affect the maximum achievable resolution. For large resolutions, the tolerance specification of components can become prohibitively narrow.

B. OVERSAMPLING

The limitations of Nyquist sampling ADCs can be addressed using an over-sampling approach, which samples a signal well above its Nyquist sampling rate. The extent of oversampling is represented by the **Over-Sampling Ratio (OSR)**, k, which is that multiple relative to the Nyquist sampling rate, f_{NS}. By selecting a suitably large oversampling frequency, f_{OS}, a broader spectrum of signals can be sampled: with narrow-band signals at high OSRs and wide-band signals at lower OSRs. The choice of OSR is not an arbitrary one, however, as subsequent filter stages will be optimized for a specific range of OSR.

1. Pulse Code Modulation

The description of PSD in **Equation (III-3)** and the subsequent analysis of Nyquist-sampled SQNR can be applied to analyze examples of oversampling modulators. For example, consider the pulse code modulation (PCM) architecture described in **Figure III.3**.

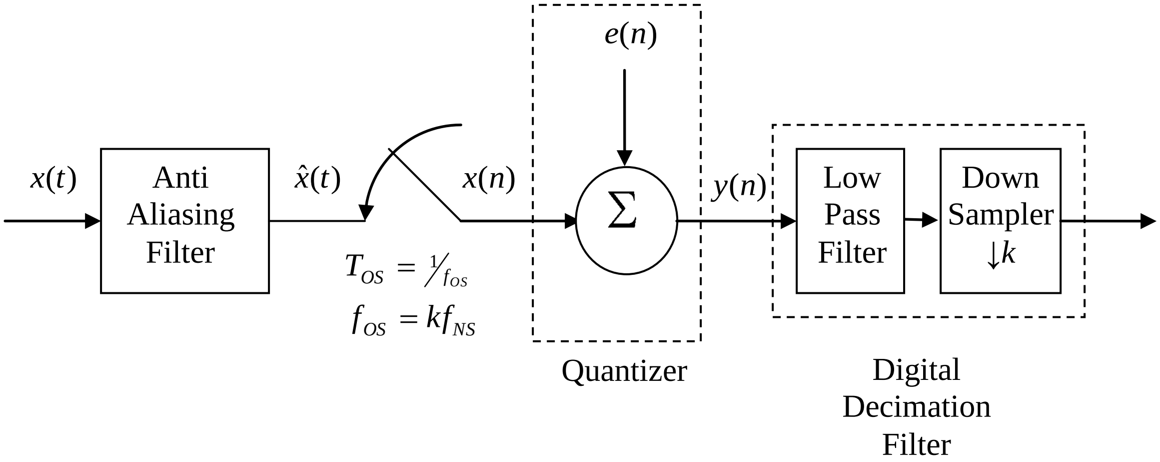

Figure III.3 Signal model of an oversampling ADC architecture employing pulse code modulation (PCM).

A signal extant in the frequency band $0 \leq f_0 < f_{NS}/2$ to which a dither signal contained within the band $f_{NS}/2 \leq f < f_{OS}/2$ is added, is pulse code modulated at f_{OS}.

The oversampling ratio, k, is the integer ratio of the oversampling frequency f_{OS} to the Nyquist frequency f_{NS}, defined in **Equation (III-8)**:

$$\mathrm{OSR} = k = \left\lfloor \frac{f_{OS}}{f_{NS}} \right\rfloor = \left\lfloor \frac{1}{f_{NS} T_{OS}} \right\rfloor$$

(III-8)

If the dither signal is sufficiently large and variable to whiten and decorrelate the quantization error, the noise power that falls into the signal band will be given by **Equation (**(III-9)**)**:

$$n_0^2 = \int_0^{f_0} e(f)\,df = e_{RMS}^2 (f_{NS} T_{OS}) = \frac{e_{RMS}^2}{k}$$

(III-9)

Hence, oversampling reduces the in-band RMS noise from ordinary quantization by the square root of the oversampling ratio. A comparison of the respective power spectral densities $N(f)$ of quantization noise for Nyquist and oversampling is illustrated in **Figure III.4**.

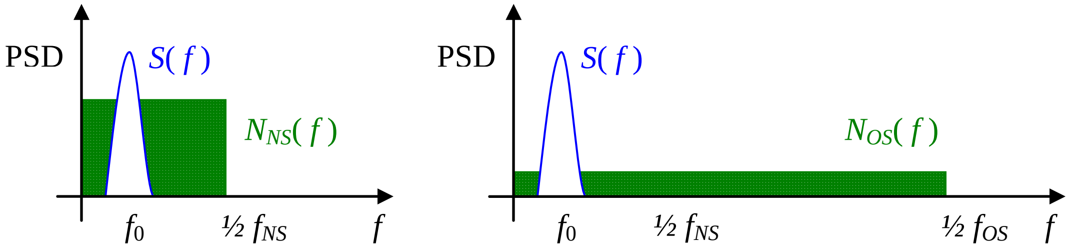

Figure III.4 Comparison of the one-sided power spectral density (PSD) of quantization noise $N(f)$ for Nyquist sampling ADCs (left) and oversampling ADCs (right). $S(f)$ is the PSD of the signal of interest (SOI).

The effect of oversampling is to redistribute the total quantization noise power from the signal band to the oversampling band. The quantization noise contained in the signal band is subsequently reduced, and the out of band noise is easily rejected by subsequent low-pass filter stages.

Using the same procedure to derive **Equation (III-7)**, the oversampling SQNR is described in **Equation (III-10)**:

$$SQNR = 6.02Q + 1.76 + 10\log_{10} k \ \text{dB}$$

(III-10)

Hence, each doubling of the sampling frequency increases the SQNR by decreasing the in-band noise by 3 dB. An alternate perspective is that an oversampling ADC can achieve a one-half bit increase in resolution for each octave of oversampling **[2]**.

The digital decimation filter lowers the word rate (and, hence, the net bit rate) of the digitally output encoded signal by increasing the length of the words, thus improving the efficiency of the encoding **[15]**.

2. Sigma-Delta Modulation

Pulse code modulation is an oversampling technique commonly used in ADC applications, such as digital telephony, where specific amplitude information is encoded into each pulse. Other oversampling techniques exist, which can further improve the SQNR. **Pulse density modulation (PDM)** is one such technique, which has particular significance to oversampling ADC applications. PDM is a technique where high resolution signals are represented as low resolution signals, with the amplitude information encoded into the relative density of pulses. PDM is the basis of sigma-delta modulation.

A **sigma-delta ($\Sigma\Delta$)** modulator employing first-order feedback is a more efficient oversampling quantizer than PCM **[14]**. The $\Sigma\Delta$ modulator has the topology of nested **infinite impulse response (IIR)** filters with the inner feedback loop representing a first order integration operator and the outer feedback loop representing a first order differentiation operator. The effect this process has on the quantization noise is that this noise is shaped to be the dominant signal at higher frequencies outside of the band of the signal of interest. The result is a 1-bit ADC that can achieve remarkably high dynamic range. Consider the sigma-delta modulator illustrated in **Figure III.5**.

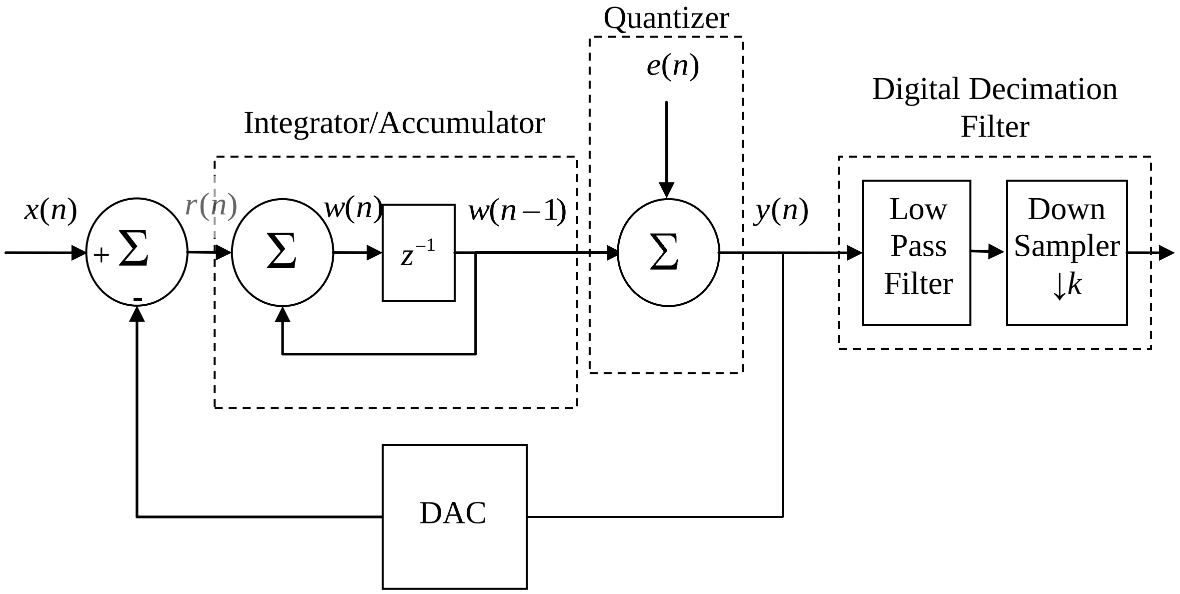

Figure III.5 Signal model of a sigma-delta modulator employing first order feedback.

Assume a uniform quantizer with unity gain *G*. The input signal is subject to feed-forward delay[2] for discrete time integration prior to quantization where the output is fed back through a digital-to-analog converter (or the output signal is preconditioned as required) to be subtracted from the input signal. The feedback forces the average value of the quantized signal to track the average input. Any persistent difference between them accumulates in the integrator and eventually corrects itself. A time-varying input signal, such as a ramp will be quantized over number of levels. The quantized signal oscillates between two adjacent quantization levels that are adjacent to the input value in such a way that the local quantized average equals the average input value **[16]**.

Using the nomenclature of **Equation (III-1)** with unity quantization gain *G* and quantization error *e*, the ΣΔ modulator can be analyzed **[17]**. In a sampled-data circuit, integration by accumulation in a ΣΔ modulator has unit gain. The output of the quantizer, $y(n)$, is the output of the integrator, $w(n-1)$, plus the quantization error, $e(n)$, as described in **Equation (III-11)**:

---

[2] For an oversampling architecture, which implicitly involves a small step-size and minimal aliasing, there is very little difference between employing a feed-forward delay integrator (Tustin's or Trapezoidal Method) or a feed-back delay integrator (Euler's or Rectangular Method).

$$y(n) = w(n-1) + e(n)$$

(III-11)

The output of integrator, $w(n-1)$, is the unit-delayed input, $w(n)$, which comprises $w(n-1)$ as feedback in addition to $r(n)$, as described in **Equation (III-12)**:

$$w(n) = r(n) + w(n-1)$$

(III-12)

The signal, r(n), is the output at the junction of the outer feedback loop and is the difference between the input signal, x(n), and the output y(n), as described in **Equation (III-13):**

$$r(n) = x(n) - y(n)$$

(III-13)

Equations (III-11), **(III-12)** and **(III-13)** can be combined to perform the following simplification:

$$w(n) = x(n) - y(n) + w(n-1)$$

$$w(n) = x(n) - w(n-1) + e(n) + w(n-1)$$

Thus, resulting in **Equation (III-14)**:

$$w(n) = x(n) - e(n)$$

(III-14)

Equation (III-14) can be time-shifted by unit delay to yield:

$$w(n-1) = x(n-1) - e(n-1)$$

After substitution into **Equation (III-11)**, an expression for the output signal is described **in Equation (III-15)**:

$$y(n) = x(n-1) + e(n) - e(n-1)$$

(III-15)

From these expressions, it is apparent that the ΣΔ modulator differentiates the quantization error, making the modulation error the first difference of the quantization error while leaving the signal unchanged, except for delay.

The output of a ΣΔ modulator is illustrated in **Figure III.6** as the red pulse train of varying density or duty cycle. The input waveform is the blue sinusoid which has been sampled 200 times over its period. This is equivalent to an OSR of 100. The output pulses have been chosen to swing between two states: +1 and –1, and the input signal has been conditioned for matching peak-to-peak amplitude. That is, the output signal that is fed-back to the subtracted from the input signal has the same dynamic range as the input.

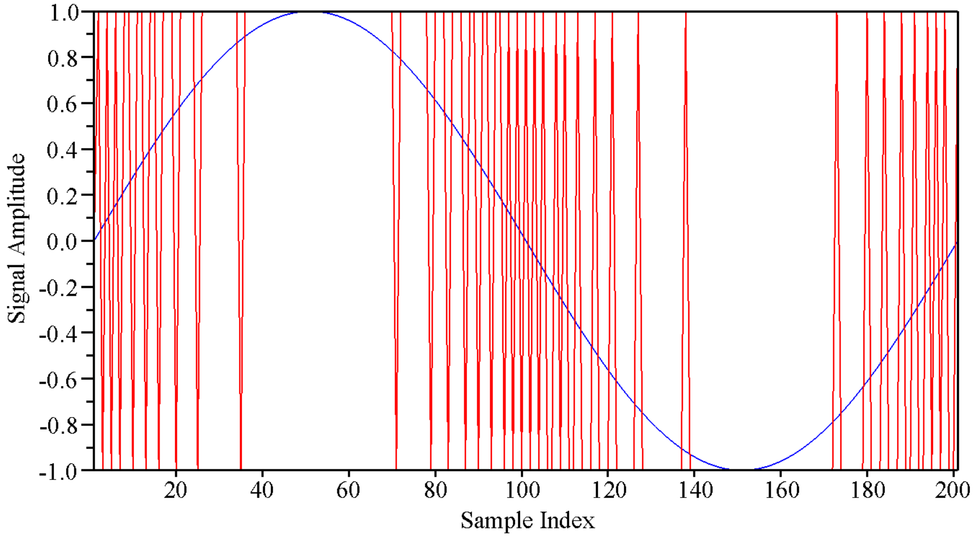

Figure III.6 Exemplar output of a ΣΔ modulator (red) for an input sinusoid waveform (blue) oversampled 100 times.

At input signal amplitudes near zero, the PDM output has a 50% duty cycle. As the input increases, the duty cycle increases in a positive sense. That is, the pulses remain at state +1 for longer, with excursions to state –1 becoming less frequent. At maximum input, the pulse output corresponds to state +1. As the input decreases, the duty cycle decreases in a positive sense with pulses remaining at state –1 for longer. Note that, the PDM output lags the input by one sample, due to the unit delay.

The effective resolution of the modulator requires a sufficiently variable input signal such that the error, *e*, behaves as uncorrelated white noise. The spectral density of the modulation noise, $\eta(n) = e(n) - e(n-1)$, may then be expressed as **Equation (III-16)** where $\omega = 2\pi f$:

$$N(f) = E(f)\left|1 - \varepsilon^{-j\omega T_{OS}}\right| = 2e_{RMS}\sqrt{2T_{OS}}\,\sin\left(\frac{\omega T_{OS}}{2}\right)$$

(III-16)

The total noise power, $\eta_0{}^2$, in the signal band, $0 \le f_0 < f_{NS}/2$, is described in **Equation (III-17)**:

$$\eta_0^2 = \int_0^{f_0} \left|N(f)\right|^2 df \approx e_{RMS}^2\,\frac{\pi^2}{3}(f_{NS}T_{OS})^3,\; f_{OS}^2 >> \;{}^{f_{NS}}\!/_{2}\;{}^{2}$$

(III-17)

The RMS value of noise power is described in **Equation (III-18)**:

$$\eta_0 \approx e_{RMS}\,\frac{\pi}{\sqrt{3}}\;\; f_{NS}T_{OS}\;\;{}^{3/2} = e_{RMS}\,\frac{\pi}{\sqrt{3}}\;\; k\;\;{}^{-3/2}$$

(III-18)

That is for each doubling of the oversampling ratio in the $\Sigma\Delta$ modulator, the quantization noise is reduced by 9 dB or the resolution is increased by 1.5 bits, according to **Equation (III-19)**:

$$SQNR = 6.02Q - 3.41 + 30 \log_{10} k \text{ dB}$$

(III-19)

From comparison with **Equation (III-10)**, the SQNR for the $\Sigma\Delta$ modulator is better than that for PCM for all meaningful integer values of *k* (i.e. greater than 1).

The improvement in resolution requires that the modulated signal is decimated to the Nyquist rate with a precisely tuned digital filter. Without decimation, high frequency components of the noise will corrupt the achievable resolution when the noise is sampled at the Nyquist rate. There are various schemes for achieving decimation filtering where the achievable noise rejection generally varies inversely with ease of implementation.

3. Decimation

The output of the modulator represents the input signal together with it’s out of band components, modulation noise, circuit noise and interference. These components dominate at different frequency bands such that no one filter can account for them all. A practical solution to this is to perform decimation in more than one stage.

The first stage is designed to remove modulation noise, which dominates at higher frequencies. A convenient filter for this stage has a frequency response based on $\mathrm{sinc}^k(f)$ functions. The word rate is lowered from the sampling frequency to an intermediate decimation frequency which is four times the Nyquist rate **[15]**. This factor gives the best compromise between reducing the noise penalty due to decimation and avoiding the drop-off in frequency response of the filter at the edge of the signal band.

In addition to attenuating the modulation noise, the filter should also provide sufficient attenuation of the high frequency components of the signal that alias into the signal when re-sampled at the intermediate frequency. The attenuation should meet the anti-aliasing requirement of the application.

An intermediate oversampling ratio of around 4 and sinc decimation is favorable in many sigma-delta applications. Smaller ratios lead to rapidly deteriorating characteristics, whereas higher ratios introduce less favorable design requirements for the low-pass filter in the subsequent decimation stage.

IV. PHOTONIC SIGMA-DELTA ADC

The NPS photonic sigma-delta ADC system represents an architecture which can be scaled in frequency subject to the fulfillment of certain hardware requirements. The system is designed to oversample the analog RF signal exciting an antenna at a rate at least 10 times higher than the Nyquist rate relative to the RF signal frequency (that is, twice the RF signal frequency). The original proposed system design is illustrated in **Figure IV.1**.

The oversampling is achieved by electro-optic modulation of the RF onto an on-off amplitude modulated (OOAM) optical carrier using **Mach-Zehnder modulator (MZM)** interferometers. After first order integration (sigma-stage) is applied, the resulting optical signal is converted back to the electronic domain using a photodetector and quantized using a comparator into a single-bit binary stream. This stream is fed back to be subtracted (delta-stage) from the antenna signal. The system therefore represents a photonic version of a first order single-bit sigma-delta **analog to digital converter (ADC).**

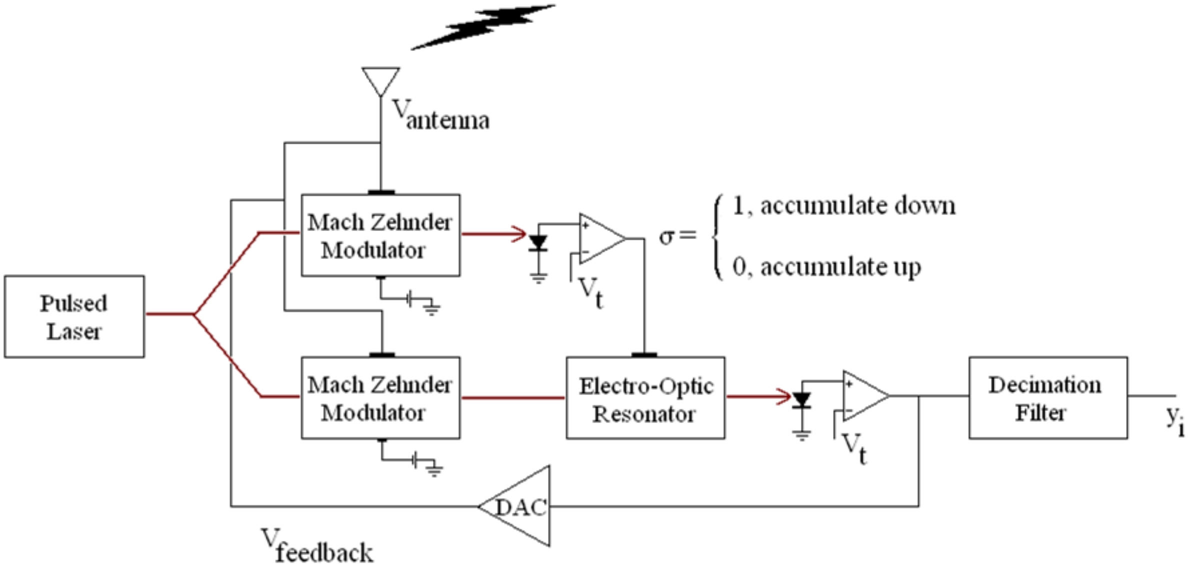

Figure IV.1 The original design for the integrated optical first-order single-bit sigma delta analog to digital converter.

The oversampling removes the traditional requirement for mixing the RF down to **intermediate frequency (IF)** and base-band and eliminating local oscillator noise which is a significant source of interference. The oversampling rate is determined by the pulse repetition rate of the OOAM photonic carrier. As described in Chapter III, oversampling reduces the quantization noise inherent to all ADCs and is a decreasing function of the **oversampling ratio (OSR)**. Thus, a receiver with a very high sensitivity for LPI applications could be implemented with this architecture.

The MZM pair is used to de-couple the magnitude and sign information from the RF antenna signal. The sign information, from the upper MZM, is processed by a comparator before recombination in a first-order single-bit integrator (electro-optic total internal reflection mirror ring resonator[3]) or 'sigma' stage.

The output of this sign-comparator is used to bias a phase modulator in the EO integrator to control the coherent integration or accumulation of an optical pulse with the previous delayed pulse. The resultant optical output is converted back to an electronic signal via a photo-detector before being processed by a high speed electronic comparator.

The output of the comparator represents a single-bit binary word, with a maximum bit rate corresponding to the oversampling rate. This output is divided for further processing and feedback. The further processing involves decimation and low pass filtering to convert the high-bit rate binary words to the final digital representation of the RF signal. The feedback takes the binary output of the comparator and (after signal conditioning) subtracts it from the RF signal at the antenna. This feedback loop or delta-stage allows the quantized output to track the input RF signal and spectrally shapes the quantization noise outside the bandwidth of the RF input signal. After decimation and low pass filtering of the output, the higher frequency quantization noise is removed and an increased sensitivity of the receiver in the input signal band is achieved.

The electronic sigma-delta ADC architecture is well known for its high dynamic range and robust spurious (noise) signal rejection. However, it is not possible

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[3] The resonator, which is intended to act as a coherent single-bit integrator, is being developed by UCSB.

electronically to sample microwave frequencies using this architecture, as the higher frequencies require timing clocks that do not offer the requisite stability in the electronic domain. In the photonic architecture presented here, the timing is referenced to the oversampling rate from the delivered OOAM laser pulses. In a wide-band implementation, this can be achieved with high precision using a mode-locked fiber laser with stable femto-second pulses, although, as will be discussed in this report, there are many challenges to overcome.

In this **Chapter**, a review of the original NPS photonic ADC system design is presented. This was the result of months of laboratory experimentation presented in **Chapter** V, which contributed to developing an understanding of the many issues that would need to be addressed before bringing this design to a functional prototype stage. This review is followed by the specification of a revised design of the photonic ADC system. Finally, the construction of the narrow-band prototype is presented.

In the narrow-band implementation, a mode-locked laser cannot produce pulses with sufficiently low **pulse repetition frequency (PRF)**. Thus, the use of an externally modulated laser source is required. This will be discussed in depth later in this Chapter.

A. WIDEBAND PHOTONIC ADC DESIGN REVIEW

The design illustrated in **Figure IV.1** described a system intended to be capable of sampling a wideband RF signal. The current specification for the UCSB electro-optic ring resonator sub-system design is driving factor in the system design specification. NPS has specified that the ring resonator should be capable of coherently integrating one delayed 10 ps-wide pulse with a subsequent pulse received 100 ps later. That is, the supported PRF of the laser pulse traveling through the ring resonator should be of the order of 10 GHz with a 10% duty cycle. Therefore the bandwidth of the ring resonator should be of the order of 100 GHz.

The specification of such a pulse characteristic is critical to the whole of system design. Every component of the system must support this very high bandwidth, from the laser source to the decimation filter. Moreover, the individual test and evaluation of system components must be performed using instrumentation possessing similarly high bandwidth for direct measurements. As will be demonstrated later this **Chapter**, these requirements are difficult to achieve with current technology and may require the development of new measurement techniques, instrumentation and hardware.

Assuming the bandwidth specification can be met for all components of the systems, the resulting ADC system should be capable of sampling an RF signal bandwidth of 500 MHz at 10 times oversampling ratio (i.e. 10 times the Nyquist rate of 1 GHz). The significance of this assumption is that the achievable bandwidth of the ADC system is constrained by that component having the lowest maximum bandwidth. This unavoidable limitation is due to the need for electronic components within the ADC system. These components include the photodetector, comparator, summing amplifiers, DAC and decimation filter.

Components that have insufficient bandwidth in **commercial-off-the-shelf (COTS)** packages will need to be sourced from other research labs or specially constructed. At some point there will be an upper-limit of bandwidth imposed because the required technology either does not exist or is beyond the budgetary resources of the project. Moreover, any development of the required technology may well constitute a project in its own right.

From **Figure IV.1**, the 10 ps-wide (100 GHz bandwidth) pulses output from the pulsed laser source are input to the Mach Zehnder Modulators to be ‘encoded’ with the sign and magnitude information relating to the 1 GHz RF input. Therefore, MZMs with 100 GHz bandwidth are required. Similarly, the photodetectors and comparators should bear similar specification, as should the summing amplifier between the antenna and RF inputs to the MZM. The output signal will be a high bit-rate single-bit word and, hence, the decimation and low pass filter stage should also bear a 100 GHz bandwidth.

Table IV-1 describes the availability/existence of components that could meet two different bandwidth specifications of the NPS photonic sigma-delta ADC system. Information is presented for the same mode-locked laser source with a 50% duty cycle (20 GHz) and a 10% duty cycle (100 GHz). The maximum bandwidth is also described.

Table IV-1 Availability of components meeting bandwidth requirements for the NPS photonic sigma-delta ADC system.

Device	20 GHz	100 GHz	Max Bandwidth
Mode-Locked Laser	Y	Y	>100 GHz dependent on pulse-width
Summing Amplifier[4]	Y	N	22-26 GHz (InP DHBT)
Mach Zehnder Modulator	Y	N	40 GHz
Photodiode	Y	Y	100 GHz
Comparator	Y	N	26 GHz (SiGe)
Ring Resonator	Y	Y	made to order
Decimation Filter	N	N	Use high speed DSO

The fastest COTS comparators currently available (in SiGe technology) have a bandwidth of 26 GHz **[18]**. If this is assumed to be the maximum bandwidth constraint of the system, then the minimum pulse width is specified as 38.5 ps for a 10% duty cycle to achieve an oversampling rate of 2.6 GHz. Thus, for a 10 times OSR the maximum bandwidth for the signal of interest is 130 MHz. For a 50% duty cycle, the corresponding oversampling rate would be 13 GHz, enabling ten times oversampling of a 650 MHz bandwidth signal. Current technology electronic receivers have COTS bandwidth specifications up to 1.2 GHz.

The requirements for the decimation filter are not considered in this report since, in the laboratory environment; the resulting bit-stream would be passed to a data-storage oscilloscope or similar device to allow decimation and other analysis to be performed

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[4] Pace **[2]** proposed a push-pull electrode configuration in the MZM pair to perform the subtraction of the RF antenna and feedback signals. This requires very strict phase control over the bandwidth of the modulator, which is difficult to achieve in standard push-pull MZM applications that power splits an input RF signal to achieve a reduced $V\pi$.

using software. It has been envisaged that for a high bandwidth application, the decimation filtering would be achieved with filters using high temperature superconductors **[**2**]**.

In the NPS design there is no identified requirement for a DAC since the output of the comparator is a binary output that spans the dynamic range of the system. That is, the peak-to-peak amplitude of the comparator output matches that of the RF input voltage (which is itself conditioned to correspond with the characteristic voltage range of the MZM). Instead of the DAC, signal conditioning was proposed to modify the comparator output from (0, +15V) across 1 MΩ to ± $V_{antenna}$ across 50 Ω. In any case, the signal conditioner is constrained to the same high bandwidth requirement.

It was found during the course of the experiments presented here that the original design and previous experimental efforts did not account for impedance matching of the feedback signal. Moreover, neither design work nor experiments had considered the actual requirements for a summing amplifier, which also has to be impedance matched with the antenna-MZM circuit. The RF-inputs of the Mach-Zehnder and Phase modulators have an input impedance of 50 Ω.

The issue of impedance matching is also relevant to the UCSB ring resonator. This device will comprise an integrated electro-optic phase modulator, which would have an input impedance of 50 Ω. Thus, the output of the direction comparator will also need to be impedance matched. Experiments are yet to be conducted with the UCSB electro-optic ring resonator. Earlier experiments performed with its predecessor version, the fiber-lattice accumulator, demonstrated that coherent integration could not be achieved, which is one of the motivations behind the resonator’s development.

In previous experimental efforts involving the fiber-lattice accumulator sub-system, a 50 Ω phase modulator was utilized. These efforts did not recognize the impedance matching requirements between the direction comparator and the phase modulator in the system set-up. However, most experimentation with the fiber-lattice sub-system involved the excitation of the phase modulator with an RF test source, which was impedance matched. Hence, while impedance matching was not explicitly accounted for in the system design, it is not considered to be the issue responsible for the lack of results achieved with the fiber-lattice accumulator.

Figure IV.1 shows that the direction and magnitude paths of the ADC system follow different path lengths prior to recombination in the electro-optic resonator stage. For 10 ps wide pulses, separated in time by 100 ps the corresponding spatial pulse density is one 3 mm pulse every 3 cm. This suggests a requirement for high precision optical fiber lengths, in addition to taking into account the finite integration time of the photodetector as well as delays associated with the subsequent electrical circuit, including the comparator and ring-resonator. Ultimately, the ADC system may require the addition of electronic time delay to achieve the necessary synchronization between magnitude and sign data output by the MZMs. This synchronization requirement is one of the reasons for choosing a low duty cycle optical pulse, however, precise control may be affected by thermal noise. Naturally, any additional components will also require high bandwidth.

A more rational implementation of de-coupling the sign of the RF input from the magnitude is presented here. Instead of using photonics, the sign information can be obtained by passing a suitably buffered version of the RF signal directly to a high-speed comparator. This would eliminate the unnecessary complexity of using a MZM, photodetector and optical fiber. It would also reduce the amount of optical insertion loss in the system, thereby improving the optical SNR in the remaining photonic circuit. Moreover, the delay in the direction circuit can be managed electronically to ensure synchronicity between magnitude and direction of the RF input.

The revisions and rationalizations proposed in the preceding paragraphs are incorporated into a revised design of the ADC system illustrated in **Figure IV.2**.

A further rationalization of the design may be to replace the ring resonator with an electronic accumulator device. The advantage of this would be a system design not constrained to an oversampling frequency fixed by the geometry of the ring resonator. However, such devices are currently limited to maximum bandwidths of 1.25 GHz. Nevertheless, this option may be worth considering in the development of the narrow-band prototype.

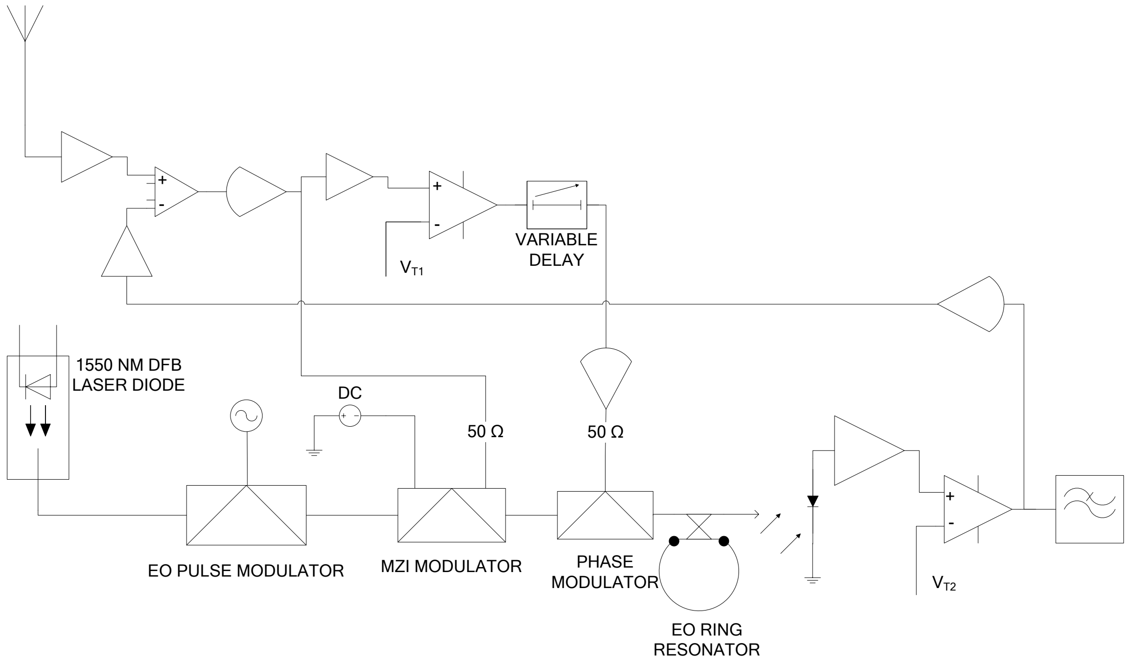

Figure IV.2 Revised design of the NPS photonic sigma-delta ADC system.

The revised design illustrates that all inputs to the comparators and the summing amplifier are buffered with high input impedance (in the case of an RF summing amplifier buffering at the input may not be required, or may be integrated within the amplifier). The outputs of these components are subject to power amplification so that they can provide sufficient power to drive the 50 Ω MZI and phase modulators. In the feedback path, signal conditioning to convert the low current output of the comparator to a signal with sufficient power to match the antenna input is achieved using a similar power amplifier.

Many of these electronic components would have insufficient bandwidth to satisfy the wide-band application, beyond the 26 GHz described in **Table IV-1**. However, this limitation would also exist in the original design which also requires signal conditioning in the feedback loop, the summing amplifier and two comparators as well as the decimation and low pass filter. Hence the revised design illustrated in **Figure IV.2** is proposed as both a simplification of the original design and as a means of better illustrating the assembly and construction requirements for the system.

The representation of the pulsed laser system is expanded to illustrate separately the 1550 nm CW laser source and the pulse modulation stage. The pulse modulation shall be tuned with respect to the PRI to match the fixed delay within the EO ring resonator. The direction and magnitude signals, which are ‘recombined’ in the phase modulator at the input of the ring resonator, shall be synchronized using the variable delay at the output of the direction comparator, V_{T1}.

In a wide-band application, the appropriate choice of pulsed laser is the mode-locked laser for low duty cycle, high PRF stable pulses. For narrow-band applications, a different electro-optic pulse generation technique is described in the following section.

B. CONSTRUCTION OF A NARROW-BAND PHOTONIC ADC

The narrow-band photonic ADC prototype was constructed based on the revised wide-band design described in the previous section. A high bandwidth specification was determined to warrant a significant capital investment in laboratory infrastructure, including test and measurement instrumentation. The requisite funding and purchases could not be achieved within the 12 month *in situ* term of the international collaboration. Moreover, there had been no hitherto proof of concept hardware development of this photonic ADC architecture. Consequently, the specification of the narrow-band ADC system was proposed as a low cost, low risk development that would avoid the constraints of the available budget, equipment and components.

The components that could be sourced and utilized for the narrow band system are listed in **Table IV-2**. The connection of these components is illustrated in **Figure IV.3.** Some of the components are constituted as sub-systems, the characterization of which will be discussed in more detail in the following chapter. The specific sub-systems that will be addressed in detail include the laser diode, the electro-optic pulse generator and the fiber-lattice accumulator.

Table IV-2 Component list for the narrow band photonic ADC. See Figure IV.3 for the component schematic.

Part No	Description/ Function	Maximum Bandwidth (Hz)	Input Impedance (Ω)	Comments
LM319M	Comparator	6.25 M	3 M	80 ns response time
LM318N	Buffer/ Difference Amplifier	15.0 M	3 M	
2N2222	Relay/Current Buffer	100 M	60 (Real Part)	
JDSU MZ150-000560	MZI Modulator S/N: 148163D/E 443383C	10 G	50	1550 nm
JDSU	EO Phase Modulator	10 G	50	1550 nm
New Focus Model 1024	High Speed Photodiode/Amplifier	26 G no amplifier 50 k transimpedance amplifier	N/A	12 ps rise time 50 Ω output impedance
HP 8447A	Amplifier	100 k - 400 M	50	Amplify photodiode output, if required
EM4 EM253-080-053	DFB Laser Diode (LD) 1550nm 80mW	N/A	N/A	Polarization Maintained Output
Tektronix DSO4104	Digital Phosphor Storage Oscilloscope	1 G	50 / 100 M user selectable	5 GS/s across 4 channels
Thorlabs ITC510-IEEE488	Laser Diode Combi Controller	N/A	N/A	Current and Temperature Control
Newport 744	Laser Diode Butterfly Mount	N/A	N/A	Interfaces LD with ITC510
Agilent 33220A	Function / Arbitrary Waveform Generator	N/A	50 (typical) user programmable	Sinusoids up to 20 MHz
Various Unspecified	Regulated DC power supply (mains and battery powered)	N/A	N/A	Up to ±30 V DC
Custom	Fiber Lattice Accumulator with Semiconductor Optical Amplifier (SOA)	N/A	N/A	SOA is a JDSU CQF781/0 Multiple Quantum Well booster amplifier

The system schematic illustrated in **Figure IV.3** represents an RF field incident on an antenna, which creates an excitation voltage, $V_{antenna}$, that is input to a high impedance unity gain voltage buffer amplifier followed by a difference amplifier which subtracts the input feedback voltage, $V_{feedback}$ from $V_{antenna}$. The difference signal output is input to a low output impedance (50 Ω) current buffer (or relay) and divided to provide the drive voltage at the 50-ohm RF input of the MZI modulator (for unipolar amplitude modulation of the optical carrier). The output of this relay is also input to a high impedance unity gain voltage buffer amplifier, before passing through an analog low pass filter (designed with a cut-off frequency corresponding to the oversampling frequency) and then input to a high speed comparator. This comparator is tuned with a zero voltage threshold to provide an output that is sensitive to the sign of the input voltage. A positive voltage is assigned an output value of 0 V and a negative voltage an output value of +15 V.

The output of the sign comparator is input to a low output impedance (50 Ω) current buffer (or relay). The output of this relay is scaled to the half-wave voltage of an EO phase modulator (for phase modulation of the optical carrier), such that when 0 V is applied no phase change is applied to the input optical signal from the MZI modulator. When the half-wave voltage or V_π is applied, however, the input optical signal from the MZI modulator is phase shifted by π radians. There is no delay element included in this design as the narrow-bandwidths to be investigated are not considered to warrant such precise control.

The optical carrier is generated using a **continuous wave (CW) distributed feedback (DFB)** laser diode. The laser diode output is controlled both thermally and electronically to maintain a regulated output and prevent damage to the laser.

The CW output of the laser is externally modulated using an electro-optic pulse generator. The output is a low duty cycle optical pulse train with pulse shapes that closely resemble those of solitons (hyperbolic secant squares).

Preliminary efforts to produce optical pulse trains for this work used a square wave generator to produce on-off amplitude modulated optical pulses. These pulses could

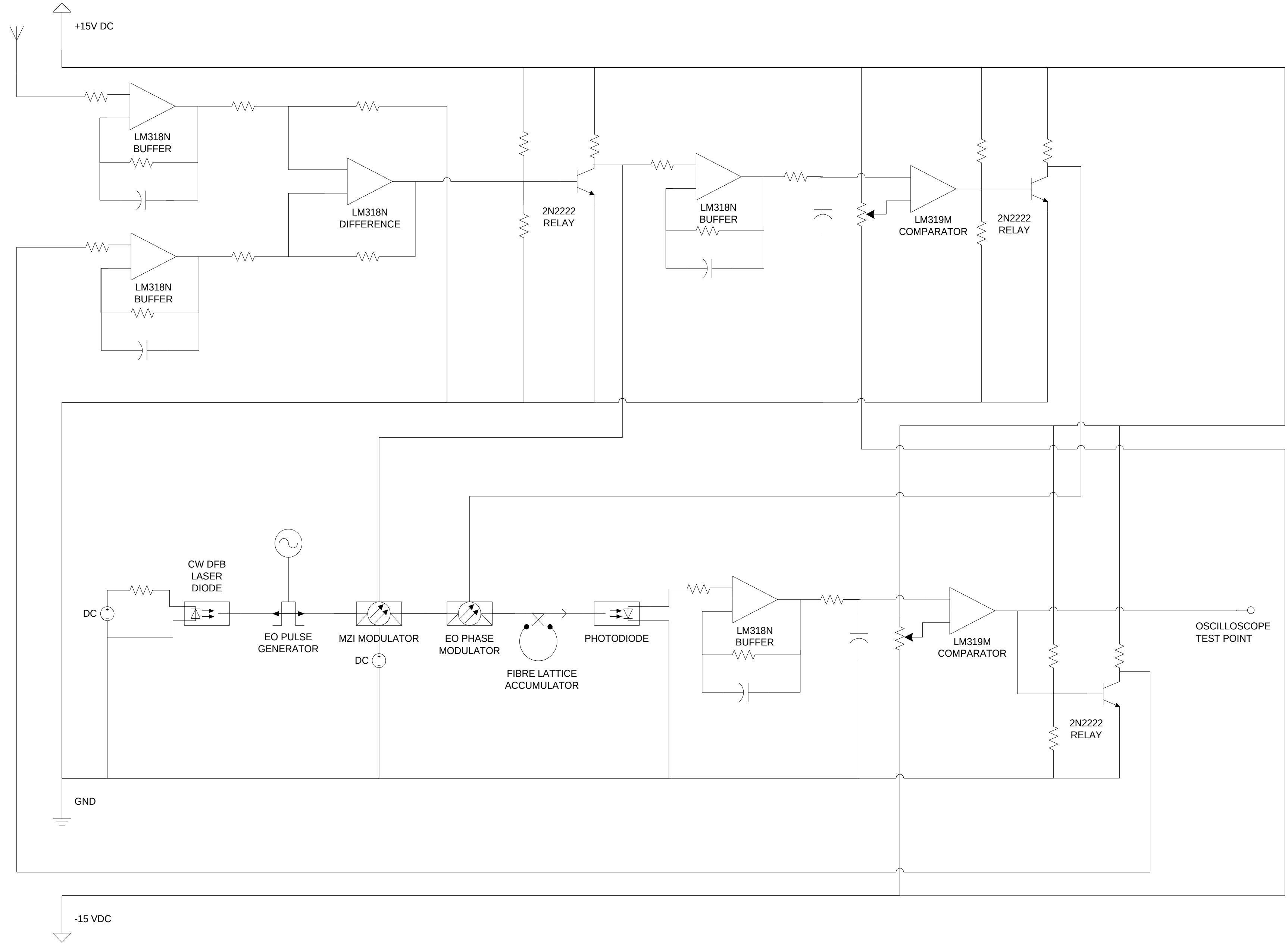

Figure IV.3. Component schematic of the narrow band photonic sigma-delta ADC used in laboratory development at NPS.

not be produced at sufficiently high frequency (PRF), with sufficiently low duty cycle and were prone to high frequency switching noise.

The EO pulse generator **[19]** uses a cascade of MZI modulators stimulated with phase-locked sinusoidal voltage waveforms with peak amplitudes corresponding to increasing multiples of V_π across the cascade to achieve a pulse train whose parameters can be flexibly configured. The EO pulse generator is described in greater detail in Chapter V.A.2.

The resulting EO generated pulses are transmitted via optical fiber to the MZI modulator, where they are amplitude modulated (unipolar) with the RF input signal to that modulator, i.e. $V_{antenna}$ - $V_{feedback}$.

The output of the MZI modulator is then transmitted via optical fiber to the EO phase modulator. As described earlier, the RF input signal to the phase modulator is a power amplified version of the output of the sign comparator. This input signal is used to control the optical pulse input to the fiber lattice accumulator to achieve optical integration with another optical pulse that has been delayed in the accumulator circuit by one pulse period (if feedback delay has been used). For a zero voltage input to the phase modulator (from the sign comparator), the optical pulse is not phase shifted as it passes through the phase modulator. Optical pulses will continue to experience integration gain in the fiber lattice accumulator. For a half-wave voltage input to the phase modulator (6 V across 50 Ω) a π radians phase change in the optical pulse traveling through the phase modulator is produced, which when combined with the optical pulse delayed in the accumulator will produce an attenuated output from the accumulator due to destructive interference. (As mentioned earlier in this **Chapter**, the coherent optical integration/accumulation function could not be demonstrated.)

The fiber-lattice accumulator is a 4-port device that applies the input optical pulse to a 3 dB splitter and applies a delay to one path (either feed forward or feedback) followed by some optical gain. The delay corresponds to one pulse repetition interval. The accumulator is an implementation of the integrator featured in **Figure III.5** and is described in greater detail in **Chapter V.A.3**.

The output of the fiber lattice accumulator is detected by a photodiode and the resultant electronic signal is buffered and input to a magnitude comparator. The threshold of this signal is tuned at half the dynamic range of this buffered input signal, with signals below the threshold assigned zero voltage and signals above the threshold assigned +15 V.

The output of the magnitude comparator is fed back to a voltage buffer where it is scaled to the dynamic range of the antenna signal (defined by the maximum antenna voltage peak-to-peak amplitude) and subsequently subtracted from the antenna signal at the difference amplifier. That is, the zero output of this comparator is scaled to $-\boldsymbol{max}(V_{antenna})$ and the +15V output is scaled to $\boldsymbol{max}(V_{antenna})$. The output of magnitude comparator is also sampled with an oscilloscope, to capture the resulting pulse density modulated signal.

V. SYSTEM CHARACTERIZATION

In **Chapter V**, the methods and results of various characterization studies performed on the sub-systems and components comprising the narrow-band photonic sigma-delta digital antenna are described.

The studies were motivated by a number of factors, such as the need to verify the performance of components that had either just been purchased or had not been used since previous research efforts in 2005. Moreover, experimental investigation into some parts of the sigma-delta system had never been attempted; for instance, the delta stage.

A. SUB-SYSTEM CHARACTERIZATION

The sub-system studies encompassed the following electro-optic sub-systems:

- The laser diode source;
- The electro-optic pulse generator; and
- The fiber lattice accumulator.

Before discussing these sub-systems individually, it is appropriate to discuss those issues that were common to all.

The EO sub-systems all utilized optical fiber, most of which was of the **single mode (SM)** type and was observed to be sensitive to contact, vibrational and torsional stresses. The associated random phase and polarization changes that manifested as amplitude fluctuations in the photo-detected output were considered to have an adverse effect on system performance. The importance of stability arises from the need to have very precise phase control in the optical pulses for coherent integration and to minimize noise in the entire system. False alarms due to any photo-detected amplitude fluctuations exceeding the magnitude comparator threshold would reduce the achievable signal to quantization noise ratio in the ADC. Some fiber was of the **polarization maintaining (PM)** type, which was found to provide much greater stability.

A number of steps were taken to mitigate the observed sensitivity of the optical fiber:

- Where possible, PM fiber was used;
- New components were ordered with PM fiber connectivity;
- EO sub-systems were enclosed in boxes with optical fibers appropriately secured within.
- The boxes were mounted on pneumatic support to isolate them from external vibrations[5] and mechanical stresses;
- All fiber connectors[6] were replaced with rotatable key FC connectors to facilitate manual alignment of the PM fiber with the SM fiber.
- All fiber connectors were checked using a fiber-scope to determine the physical condition of their apertures. Defective connectors were repolished or replaced as required.

1. Laser Diode

An unused **distributed feedback (DFB) laser diode (LD)** had been held in storage since it was purchased in 2005. This **continuous wave (CW)** laser, with a wavelength of 1550nm, had a maximum output optical power of 63mW. The LD is housed within an **integrated circuit (IC)** of the butterfly configuration which also contains a monitor **photodiode (PD)**, **thermistor (TH)** and inputs for a **thermo-electric (TE)** cooler. The IC was mounted on a Newport 744 butterfly mount. Prior to connecting the mount to a Newport laser diode current driver (via 9-sub-D) and ILX temperature controller (via 15-sub-D) the pinouts of the butterfly mount were modified to ensure the correct connection of the IC.

An 80mW replacement for the 63mW laser was purchased to provide additional power to ensure sufficient signal at the output of the system. The replaced laser would

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[5] Building renovations in adjacent laboratories were underway during this work.

[6] Except PM fibers already supplied with connectors and factory aligned.

then serve as a spare. The connection set-up of both laser diodes were equivalent.

The laser diode driver and temperature controller pair was replaced with a Thor Labs ITC-510 Combi Controller, which housed the laser diode driver and temperature controller in the one chassis. A connection diagram is illustrated in **Figure V.1**.

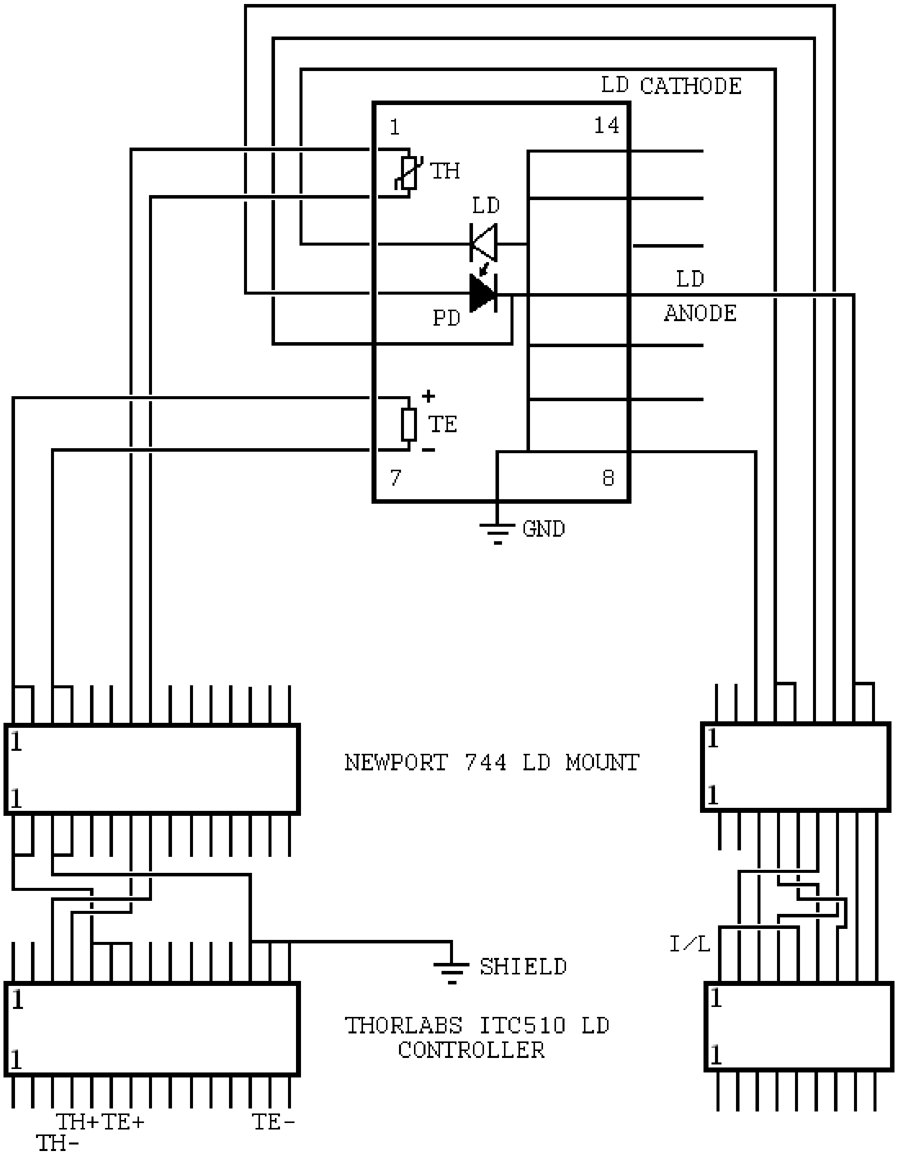
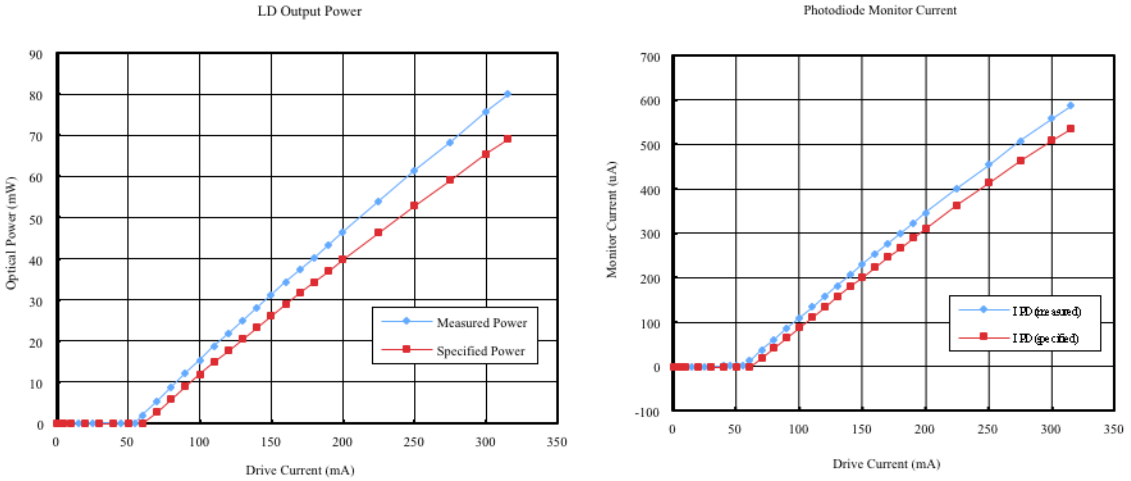


Figure V.1 Connection diagram of the EM4 EM253-80-053 DFB CW Diode Laser to the Thor Labs ITC-510 LD Controller via a Newport 744 LD mount.

Characterization of the laser source was required to determine the output power, monitor photodiode response and coherence length of the laser. The output power and monitor photo-diode response was measured and compared against the specification provided in the **product data sheet (PDS)**. The results are illustrated in **Figure V.2**.

The optical output power was measured using a Thor Labs PM300 Optical Power Meter. As these measurements were performed for CW illumination, a high-speed photodetector was not required. The photodiode monitor current was measured using the built in sensor of the ITC-510 Controller.



(a) (b)

Figure V.2 Laser diode output characteristic of the EM4 EM253-080-053 DFB CW Diode Laser. The measured data is plotted on the same axes as the data specified in the supplier's PDS. (a) Optical power response; (b) Monitor photo-diode current.

Figure V.2 shows that the measured data is consistent with the specification with equally linear responses observed over the range of drive current for both optical power and monitor current. In both cases, the measured data exceeds the specified data once the drive current is increased beyond the onset of stimulated emission in the laser. The reason for this was not investigated, although the higher measured monitor current is consistent with the laser producing the observed greater optical power than specified for a given drive current.

The laser wavelength and spectral width was measured using a Hewlett-Packard HP70951B optical spectrum analyzer, with respective values of 1550 nm and 0.1 nm obtained. The direct optical measurement of the laser's line-width was limited by the available resolution of the optical spectrum analyzer. Consequently, the measured value of 0.1 nm was neither accurate nor typical of diode lasers. The corresponding coherence length for this spectral width, $\Delta\lambda$, is calculated from the following approximation:

$$l_c = \frac{\lambda^2}{n\Delta\lambda}$$

(V-1)

Where $n = 1.47$ is the refractive index of the SM fiber at wavelength, $\lambda = 1550$ nm. Substitution of these values into **Equation (V-1)** yielded the grossly insufficient coherence length of 0.016 m.

A narrow line-width laser was selected for this work due to a requirement for a long coherence length. The reasoning behind this requirement was to ensure that delayed laser pulses would maintain optical phase coherence with subsequent incoming pulses, provided the length of the delay line in the fiber-lattice accumulator was less than the coherence length. This is discussed in more detail in **Chapter VI.**

DFB laser diodes are well known for their long coherence lengths, however, product data sheets tend to underestimate the actual value of this parameter on the basis of optical spectral measurements. For example, the laser used here was quoted a spectral width of less than 1 MHz, which corresponds to a coherence length of greater than 64 m.

The line-width of a DFB diode laser is generally too narrow to be measured directly using a typical optical spectrum analyser. Instead this parameter is measured indirectly using an RF spectrum analyser.

The CW output of the laser is input to 3 dB splitter with one path fed through a long fiber delay (4000m) and the other fed through a lithium niobate ($LiNbO_3$) electro-optic travelling wave phase modulator. A fiber delay line was constructed using existing spools of single mode fiber. The two paths are recombined (50/50) and the output is input to a high-speed photo-detector. The electronic output of the photo-detector is input to an RF spectrum analyser which displays a power spectrum of the interfering waves. The **full width half maximum (FWHM)** of this power spectrum is equivalent to twice the spectral line-width of the laser. The power spectrum represents a Lorentzian distribution of the photons undergoing spontaneous emission inside the laser, which is the principle cause of line-width broadening in a laser.

This technique is known as a delayed **self heterodyning interferometer (DSHI)** after Yariv and Yeh **[20]** and an experimental measurement was conducted using the set-up illustrated in **Figure V.3**. Numerous other examples of this measurement technique may be found in the scientific literature **[21,22]**. A comprehensive derivation may be found in Yariv's text; however, a summary of the method is included here.

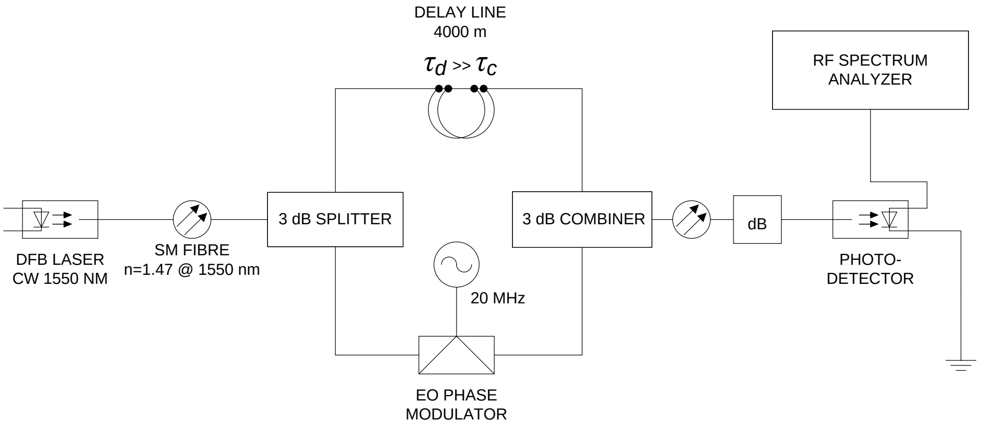


Figure V.3 Experimental set-up of the line-width measurement using the delayed self-heterodyning method to measure the line-width of the EM253-80-053 DFB Laser.

The delayed self heterodyning method utilizes the fact that the main source of fluctuations in laser fields is phase and not amplitude. By mixing an optical field with a delayed version of itself (where the delay exceeds the coherence time), the field at the detector can be approximated in complex phasor form as the vector sum of the field and its delayed version. The photo-detector output current is therefore proportional to the time average of the square of the total optical field incident on the detector, i.e. the product of the complex amplitude of this field and its complex conjugate. The power spectrum of this current is obtained from application of the Weiner-Khintchine theorem.

The resultant spectrum contains a DC component and the Lorentzian term referred to previously. The width of the measured spectrum of the photo-detector current is twice the laser spectral linewidth.

The phase modulator was used to inject a high frequency component onto the optical carrier to enable the power spectrum to be shifted away from DC, enabling the FWHM to be accurately measured. In the measurements described here, the phase modulator was supplied with a 20 MHz sinusoid waveform. The long delay (~4000 m) was chosen to be larger than the expected value of coherence length (~1000-2000 m). This ensured the delayed waves at the input of the combiner were uncorrelated with the direct waves.

Some measurements were corrupted with a 20MHz frequency component which persisted after the laser was switched off. This was traced to a poorly isolated function generator and the issue was resolved by its replacement.

A line-width measurement result is illustrated in **Figure V.4**. The measured half-width half maximum of 17 kHz corresponded to a full-width half maximum of 34 kHz. The resulting spectral linewidth was 68 kHz with a coherence length of approximately 1910 m for 1550 nm wavelength in single mode fiber with refractive index 1.47. This result was calculated from **Equation (V-2)**.

$$l_c = \frac{c}{n}\tau_c = \frac{c}{n\pi\Delta f} \tag{V-2}$$

The video trace of the spectrum analyser was averaged over 999 samples and applied over a span of 5 MHz. Resolution and video bandwidth were both automatically configured at 30 kHz, along with the sweep time of 50 ms.

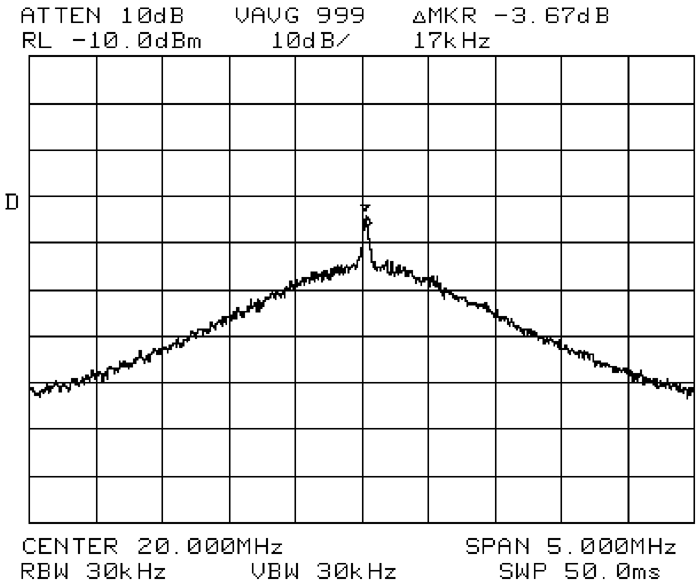


Figure V.4 Linewidth measurement using the delayed self heterodyning interferometer technique as displayed on an Agilent 8564E RF Spectrum Analyzer.

2. Electro-Optic Pulse Generator

A photonic oversampling ADC system requires the generation of short duration optical pulses with high PRF. The resulting low duty-cycle pulse train can then be transmitted via optical fiber to a MZI modulator where it is coupled with the much lower frequency signal of interest. The output of this modulator is an oversampled, discretized version of the signal of interest. Where, as is the case here, the laser source used in such a system is continuous wave, an electro-optic pulse generator is required to generate the sampling pulses.

Many laser diode power supplies include a built in pulse-modulation function; however, these are generally limited to a maximum PRF of 100 kHz with duty cycles of 50%.

Higher PRFs can be achieved by passing the laser output through an EO pulse modulator, such as an MZI modulator. In its simplest form, such a modulator can be stimulated by a square wave RF signal with amplitude corresponding to V_π. The modulator acts as a switch with the resulting optical output undergoing successive constructive and destructive interference to produce an optical square wave. The quality of the generated optical square wave is very dependent on the quality of the RF signal source used to ‘drive’ the MZI modulator. The available RF square wave or pulse generator (i.e. the Agilent 33220A) had limited capability and could not generate the required pulse characteristics of low duty cycle and high PRF. The maximum PRF that could be generated was 5 MHz with a minimum duty cycle of 10%. Moreover, the switching between the on and off states in this pulse generation technique was observed to be associated with the existence of excessive amplitude distortion and jitter at the output of the fiber-lattice accumulator for the higher PRF values tested.

For wide-band photonic applications, the oversampling pulses are best achieved with mode-locked lasers delivering stable femto-second pulses at repetition rates of the order of 10-100 GHz. These lasers are readily available “commercial-off-the-shelf”; however, such a significant investment in laboratory infrastructure could not be achieved within the time-frame and budget of the project.

Since no other electronic or RF pulse generator was available, or could be sourced from a supplier within the available time and budget, a study was commenced to investigate electro-optic pulse generation using cascaded MZI modulators. Parts of this study were published and presented at an international conference in 2008 **[19]**. A detailed description of the study is presented here.

Techniques for generating optical pulse trains include mode-locked lasers of many types, the use of arrayed waveguide gratings **[23]** and the use of fiber lattice structures **[24]** and optical modulators. Overdriven directional coupler modulators can generate very short pulse trains with high repetition frequency, but spurious pulse suppression is low **[25]**. It is possible to drive **Mach-Zehnder interferometer (MZI)** modulators to full V_π and get pulses of 33.3% duty cycle with very high spurious pulse suppression **[26]**. Haus *et al.* **[27]** suggested the use of a cascade of MZI modulators, driven by a succession of sine-wave voltages with constant amplitudes and different harmonic frequencies to achieve narrower pulses. In this report, a simpler configuration using sine-wave drive voltages with differing amplitudes, but a common frequency is demonstrated. The advantages of this new technique include the use of a single source (without the use of frequency multipliers) and that it can be readily fabricated with integrated optics. In addition, an analysis of two and three-modulator cascades is presented for a variety of configurations and techniques. For the narrow-band photonic ADC application, these techniques also offer a programmable, lower frequency range without the complexity and cost associated with a cavity dumped mode locked laser **[28].** The following discussion describes the theory of the techniques and compares simulation and experimental results.

The CW output of the laser is externally modulated using an electro-optic pulse generator. The EO pulse generator uses a cascade of MZI modulators stimulated with phase-locked sinusoidal voltage waveforms with peak amplitudes corresponding to increasing multiples of V_π across the cascade to achieve a pulse train whose parameters can be flexibly configured.

Overdriving a modulator with voltage amplitudes larger than its half-wave voltage generates short pulses, but spurious pulses also appear. Cascading several modulators in series suppresses these spurious pulses and further reduces the pulse width. The output is a product of cosine-squares manifested as a low duty cycle optical pulse train with pulse shapes that resemble those of solitons (hyperbolic secant squares).

The transmissivity T_i of the i-th MZI modulator in a cascade is given by **Equation (V-3).**

$$T_i(V_i) = \cos^2\left(\frac{\pi V_i}{2V_\pi}\right)$$

Equation (V-3)

Where V_i is the i-th modulator's drive voltage and V_π is the modulator's half-wave voltage. In the theoretical model, it is assumed that the modulators are identical and lossless. A cascade is established when two or more modulators are connected optically in series. A general expression for the transmissivity of a three-modulator cascade is described in **Equation (V-4)**.

$$T_{123} = \prod_{i=1}^{3} \cos^2\left(\frac{\pi}{2}\frac{V_i(A_i, f_i)}{V_{\pi_i}}\right)$$

Equation (V-4)

The voltage applied to each of the modulators is a function of variable amplitude or frequency or both, depending on the configuration tested. The number of modulators in the cascade and their configuration is represented by the numerical sub-subscripts. The subscripts for V_{π_i} refer to the specific half-wave voltages of the modulators in the cascade, which is relevant to the comparative analysis of the modeled devices and those employed in the experimental set-up.

Three configurations of the modulator cascade were studied, with variable-amplitude of the drive voltage waveform, variable-frequency and both variable-amplitude and frequency. These can be implemented according to the schematic of **Figure V.5**.

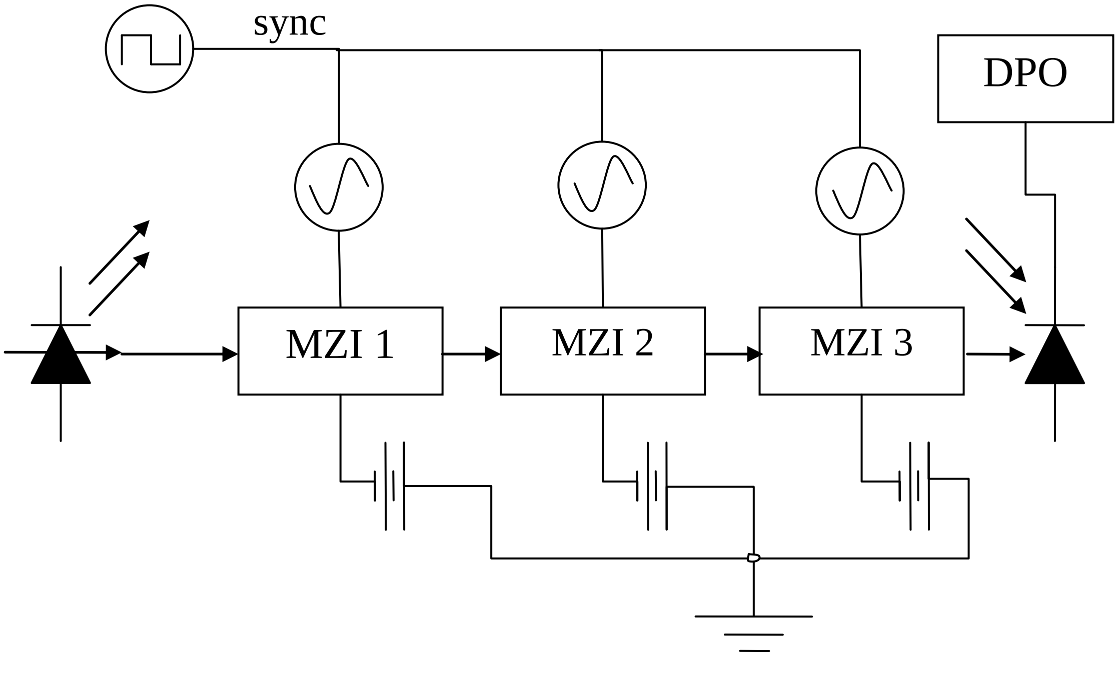


Figure V.5 General schematic of the three modulator cascade that can be used to implement the three configurations of variable amplitude, variable-frequency or variable-amplitude and frequency.

The resultant set-up is flexible and programmable, permitting a convenient transition between the three different cascade configurations.

Simulation results of this study are presented in the following three sub-sections V.A.2.*a)*, *b)* and *c)* and summarized in the analysis of **sub-section *e)*** alongside the experimental results. In the experimental implementation, which is described in detail in **sub-section V.A.2.*d)*,** the three sinusoid waveform generators were externally triggered by a common pulse generator source to produce three synchronous sine waves of the required harmonic frequencies to drive the MZI modulators. The DC bias on these modulators enabled tuning for optimal response.

For the simulation, a frequency of 1 MHz was selected for the output optical waveform. This was achieved by selecting $f_0 = 500$ kHz as the fundamental frequency for the input sinusoid waveform. This choice enabled direct comparison to be made with the experimental results, which were obtained in accommodation of the limits of the available laboratory instrumentation.

The standard representation of ‘duty cycle’ as the percentage ratio of pulse-width to the inter-pulse period was assumed. The pulse-width is measured as **the full-width at the half-maximum (FWHM)** of the photo-detector output signal. The photo-detector is a square-law detector such that the measured voltage is proportional to the photocurrent which is proportional to the intensity of light incident on detector. Therefore the FWHM is also the 3 dB pulse-width.

The desirable properties of the transmissivity output of the cascade are a narrow pulse-width and, hence, low duty cycle, as well as a low **spurious peak level (SPL)**. Where optical pulse trains generated by single MZI modulators typically require a high extinction ratio (the relative output power between the modulator’s on state and off state), a cascade of over-driven MZI modulators can introduce spurious peaks between the main peaks leading to an analogous requirement for a low spurious peak level.

The SPL is defined here as the decibel fraction of the highest spurious peak obtained between adjacent main peaks divided by the maximum output transmissivity. It is most clearly illustrated using a normalized decibel scale relative to the maximum transmissivity. The most desirable property for a MZI modulator cascade is a transmissivity output where any spurious peaks would be indistinct from the noise floor.

a) Variable-Amplitude, Constant-Frequency (VACF) cascade

Figure V.6 illustrates an alternate cascade concept for the specific case of **variable-amplitude, constant-frequency (VACF)**. The MZI modulators are cascaded optically. Each modulator is driven by a sinusoidal voltage from a common source, but with differing amplitudes achieved by attenuators.

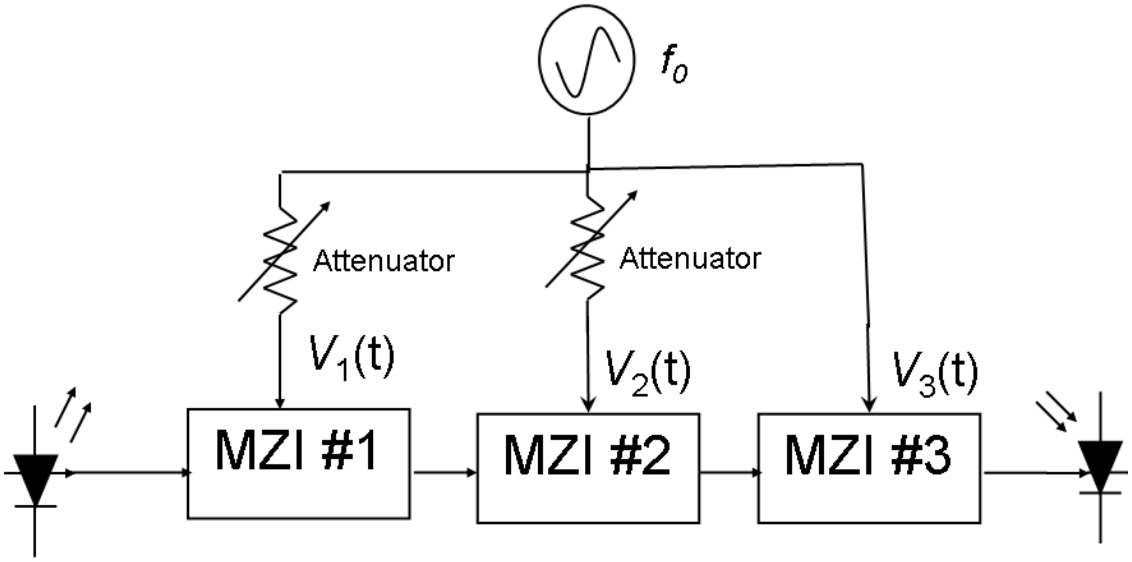


Figure V.6 Alternate concept for a three modulator VACF cascade. Applied voltage waveforms have the same frequency, but different peak-to-peak amplitudes.

In this VACF cascade, phase synchronization is not required as the applied waveforms are all of the same frequency. However, sufficient output power from the common source is required to drive all three modulators at their respective voltages.

The input drive voltage of the *i*-th modulator in the VACF cascade can be represented as shown in **Equation (V-5)**.

$$V_i(t) = A_i \sin(2\pi f_0 t)$$

Equation (V-5)

Where A_i is the peak-to-peak amplitude of the drive voltage waveform and f_0 is the common frequency of the drive voltage waveform.

The equation for the three-modulator VACF cascade was calculated using MATLAB. The drive voltage amplitudes were $A_1 = V_\pi$, $A_2 = 1.25V_\pi$, $A_3 = 1.375V_\pi$ with an assumed value of $V_\pi = 5$ volts. (The simulations assume equal half-wave voltages, but different values can be easily accommodated.) **Figure V.7** illustrates the predicted transmissivity (in dB) of the three-modulator cascade.

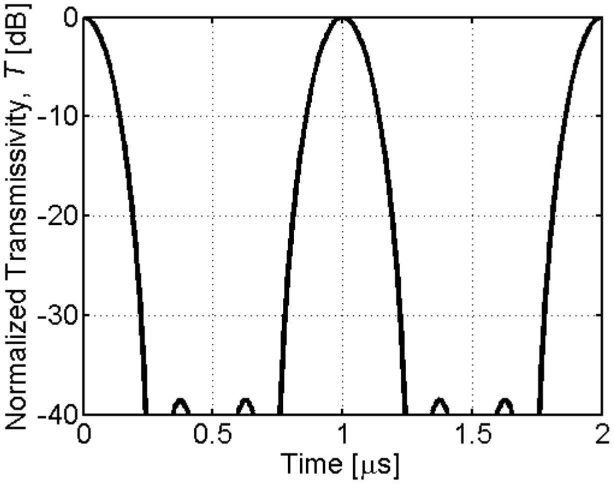


Figure V.7 The predicted optical pulse train generated by the VACF cascade model. The predicted response is shown in decibels highlighting the relative level of the spurious peaks.

The resultant pulse-train PRF is twice the applied voltage frequency and the calculated pulse width is 158.3 ns. The duty cycle is 15.83%. The SPL is –38.53 dB.

b) Constant-Amplitude, Variable-Frequency (CAVF) cascade

The CAVF cascade assumes the modulators are each excited by a sinusoid waveform with constant amplitudes, $V_1 = V_{\pi_1}$, $V_2 = V_{\pi_2}$, and $V_3 = V_{\pi_3}$ but with varying frequencies, such that $f_1 = f_0$, $f_2 = 2f_0$ and $f_3 = 4f_0$. For this cascade, the three function generators were phase-locked using an external trigger source, such that for every single cycle triggered of the fundamental frequency in the first modulator, 2 cycles are triggered in the second modulator and 4 cycles in the third. All frequencies applied in the cascade were even multiples of the fundamental frequency.

A cascade of three modulators established for this study is represented in **Equation (V-6)**.

$$V_1 = V_{\pi_1} \sin\ 2\pi f_0 t$$
$$V_2 = V_{\pi_2} \sin\ 4\pi f_0 t$$
$$V_3 = V_{\pi_3} \sin\ 8\pi f_0 t$$

Equation (V-6)

Figure V.8 illustrates the T_{123} transmissivity output of the CAVF cascade as having a lower duty cycle than VACF, but with a higher SPL and additional spurious peaks in the inter-pulse region. The calculated pulse-width is 74.1 ns for a 7.41% duty cycle and a SPS of −29.1 dB.

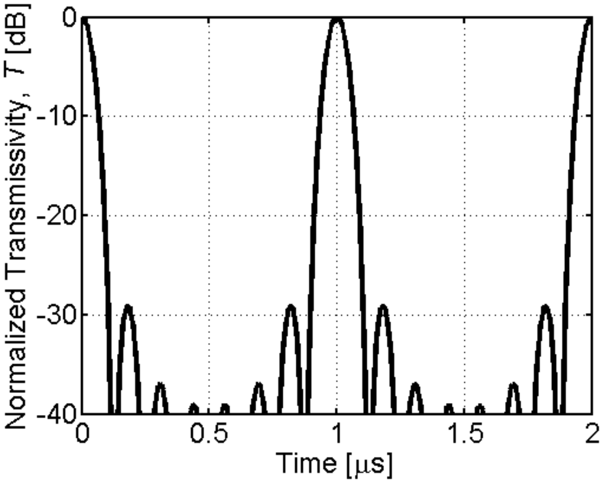


Figure V.8 The predicted optical pulse train generated by the CAVF cascade model represented by Equation (V-6).

c) Variable-amplitude, variable-frequency (VAVF) cascades.

This hybrid cascade combines the features of both VACF and CAVF, which are represented in **Equation (V-7).**

$$V_1 = V_{\pi_1} \sin\ 2\pi f_0 t$$
$$V_2 = 1.25 V_{\pi_2} \sin\ 4\pi f_0 t$$
$$V_3 = 1.375 V_{\pi_3} \sin\ 8\pi f_0 t$$

Equation (V-7)

Figure V.9 illustrates the T_{123} transmissivity output of the VAVF cascade as having the lowest duty cycle of all, but again with a higher SPL due to the presence of spurious peaks in the inter-pulse region. The calculated pulse-width is 54.1 ns for a 5.41% duty cycle and a SPL of –15.2 dB.

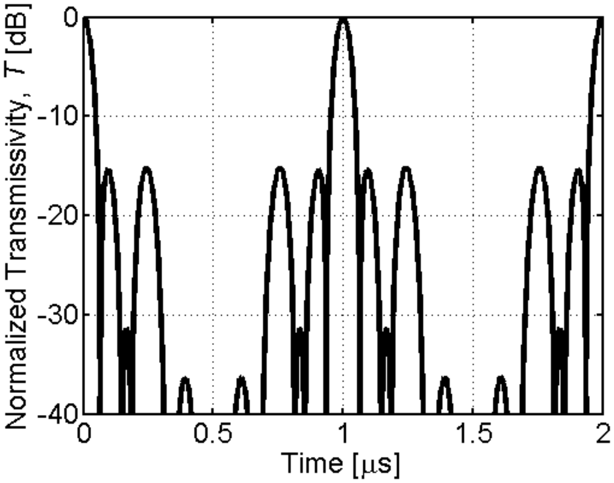


Figure V.9 The predicted optical pulse train generated by the VAVF cascade model represented by Equation (V-7).

d) Experimental Procedure

A schematic diagram of the experimental set-up was provided in **Figure V.5**. The schematic for **Figure V.6** could not be implemented due to the inability to produce sufficient output voltage using a single waveform generator. An attempt was made to address this limitation using available AC coupled RF amplifiers without success as the available devices had insufficient gain to generate the required output signal level from the maximum non-saturating input signal level.

The laser source was a 1550 nm **distributed feedback (DFB)** continuous wave semiconductor diode laser (EM4-080-253) capable of delivering an output power of up to 80 mW. The diode was mounted on a Newport 744 butterfly mount and connected to a Thor Labs ITC-510 combination controller (thermo-electric cooler and laser diode current driver). The output of the laser was delivered fiber-optically to the first MZI modulator via **polarization maintaining (PM)** fiber.

The MZI modulators were equivalent to JDS Uniphase APE AM-150 Analog Microwave Intensity Modulators capable of broadband operation from DC to 20 GHz at 1550 nm. They had PM fiber input and **single mode (SM)** fiber outputs.

The input connectors of the MZI modulators were replaced with rotatable FC connectors to achieve polarization control, thereby optimizing optical throughput. In this way, the stress rods of the PM input fiber were aligned as required to the resultant polarization axis of the SM output fiber from the preceding MZI modulator. All SM fibers were secured to minimize movement induced fluctuations in the polarization.

The first modulator had a maximum half-wave voltage of 6 V for its RF electrodes and 12 V for its DC bias electrodes. The second and third modulators were superseded versions of the AM-150 with maximum half-wave voltages of 3 V_{RF} and 6 V_{DC}. The input impedance of the modulators' RF electrodes was 50 Ω. These values of half-wave voltages could not be readily supplied from a single source. Typical arbitrary waveform generators have a maximum supply of 10 V_{ppk}, but the implemented cascade of three modulators required a supply of 24 to 28 V_{ppk}. While such requirements could have been achieved with RF and microwave power amplifier modules; the available time and budget did not support this approach.

Hence, the experiment utilized three function generators (Agilent 33220A[7], with $V_{max} = 10\ V_{ppk}$ for an output impedance of 50 Ω) to provide the required sinusoidal waveforms for the three cascaded modulators. The 6 V half-wave voltage of the first modulator meant that only 83% of the requisite peak-to-peak amplitude could be delivered to that modulator and this limitation is explored in more detail in the analysis of **sub-section *e)***.

To ensure the synchronization of these function generators, a fourth generator (also an Agilent 33220A) was configured as a pulse generator to externally trigger the sine-wave generators. This synchronization method was limited by the 100 ns latency of the available function generators and this necessitated the use of burst triggering for a number (4-8) of cycles. Too many cycles resulted in excessive synchronization error and too few resulted in periodic resets appearing in the resultant pulse train, which manifested as periodically wider pulses. It is expected that this limitation would be resolved with the use of higher-performance arbitrary waveform generators.

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[7] These function generators were sourced from various teaching laboratories in the ECE Department.

The optical output of the MZI cascade was converted to an electrical signal using a fast photo-detector, the output of which was measured using a 1 GHz sampling oscilloscope.

The choice of frequency for the synchronizing pulse generator and, hence the required sine-waves, was affected by synchronization error which was observed to increase exponentially with the **pulse repetition frequency (PRF)** of the cascade output.

Figure V.10 illustrates a measure of this synchronization error in terms of the **relative standard deviation (RSD)** of the measured frequencies of the cascade output, function generator output and the **synchronization (sync)** pulse generator output. In addition, the RSD of the measured duty cycle of the cascade output was also plotted against an increasing PRF of the photo-detected output of the cascade.

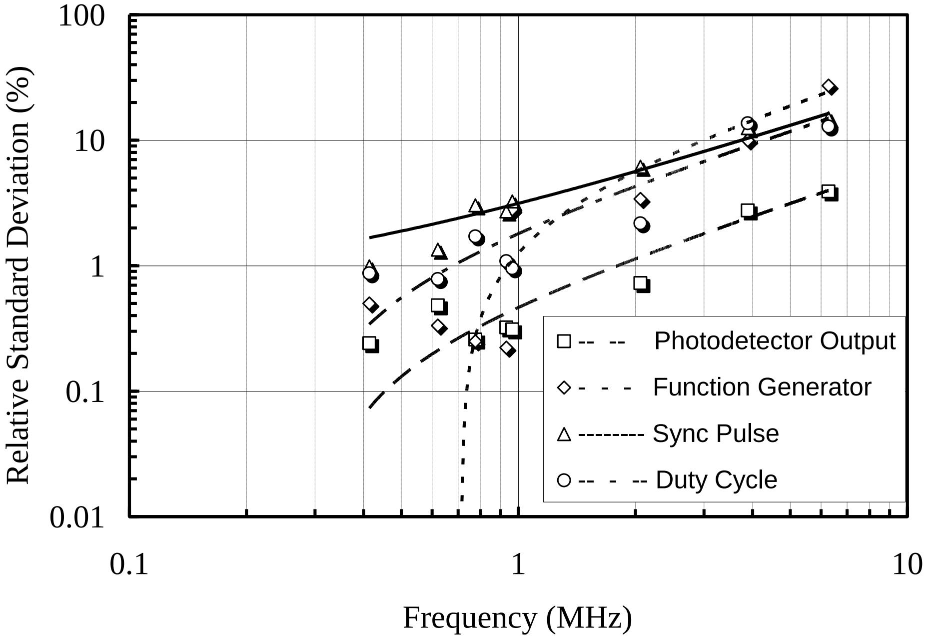


Figure V.10 Measured relative standard deviations (RSD) of the frequencies measured: for the photo-detector output (PRF) of the VACF cascade; the function generator; the sync pulse generator; and the duty cycle of the photo-detected output. Data is plotted against the measured PRF of the photo-detected output of the cascade.

Control of the PRF was achieved by adjusting the frequencies on the pulse and function generators. From **Figure V.10**, the **relative standard deviation (RSD)** is less than 5% for all measurements below a PRF of 2 MHz. The maximum RSD for the cascade output was approximately 3.5% at a PRF of 6 MHz. At this upper frequency, the RSD for the function generator, synchronization pulse generator and the cascade output pulse width all exceeded 10%. Although not measured explicitly, it was assumed the remaining function generators driving the other modulators in the cascade would exhibit similar properties to those measured for the function generator tested.

An upper-bound on the drive frequencies was set at 2 MHz to mitigate the effects of the synchronization error. This corresponded to a maximum 5% RSD for the function and pulse generators, with corresponding RSDs for the pulse width and PRF at 2% and 0.7%, respectively. Subsequent experimental measurements were performed for a cascade output PRF of 1 MHz. (Some results were obtained at 2 MHz, but these special cases are explained in the following sub-section's analysis.)

e) Results and Analysis

Experimental results were obtained for the three modulator configurations featured in the simulations illustrated in **sub-sections *a)-c)*.** For the sake of brevity, graphic illustration of the experimental results is also limited to the T_{123} cases for the VACF, CAVF and VAVF cascades featured in **Figure V.7** to **Figure V.9**. In addition, the simulated and measured waveform parameters for these and the other combinations comprising two modulators are summarized for comparison in **Table V-1**.

From **Table V-1**, it is apparent that the model predicts a three-modulator cascade to deliver a more desirable optical pulse train than any two-modulator cascade for all cascade types and this is supported by experimental measurement. The differences between simulation and experiment are described in more detail later in this sub-section.

Of the three-modulator cascades, our VACF model predicts the widest pulse, but lowest SPL. The CAVF model produces a narrower pulse, by a factor of 2 relative to VACF, but with one spurious peak which yields a SPL 9 dB higher than VACF. The VAVF model produces the narrowest, by a factor of 3 relative to VACF, but with the most spurious peaks and the highest SPL at −15.2 dB.

Of the two-modulator cascades, similar trends were predicted to those of the three-modulator cascades.

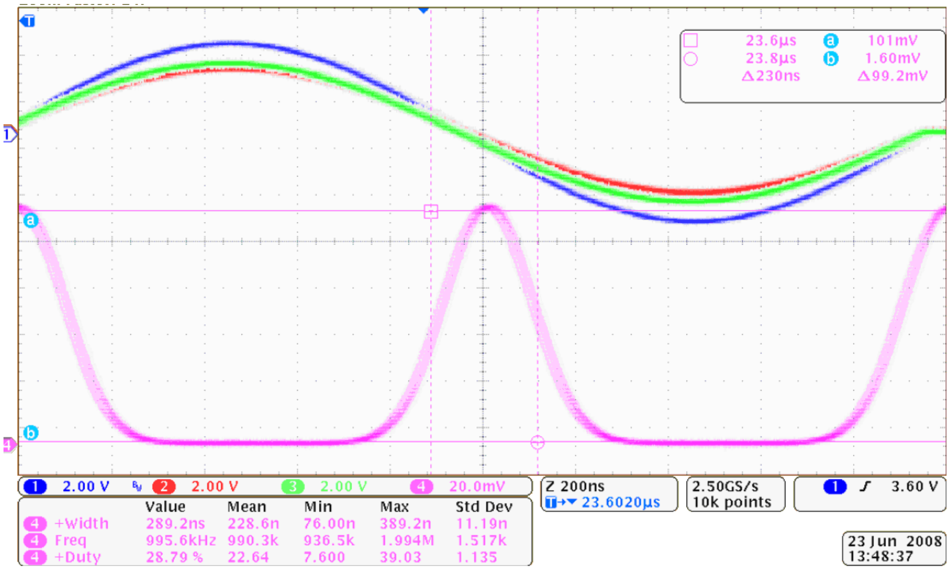
Table V-1 Simulation and experimental results for various configurations and combinations of two and three Mach-Zehnder Interferometer modulators. The asterisk '*' denotes a configuration where the output frequency is 2 MHz for a 1 MHz input which is realized by the removal of the 1st modulator.

Cascade Configuration	Pulse-width (ns)		Duty Cycle (%)		Spurious Peak Level (dB)	
	Sim.	Exp.	Sim.	Exp.	Sim.	Exp.
VACF						
T_{12}	208.2	286±4	20.82	28.8±0.4	−30.3	−15.6
T_{23}	178.2	272±2	17.82	26.9±0.2	−13.5	−15.6
T_{13}	194.2	272±2	19.42	27.0±0.2	−24.2	−15.6
T_{123}	158.2	229±11	15.82	22.6±1.1	−38.5	−15.6
CAVF						
T_{12}	150.2	214±3	15.02	21.6±0.3	−25.5	−10.3
T_{23}	74.1*	112±8*	14.82*	22.2±1.6*	−25.5	−11.3
T_{13}	82.1	150±3	8.21	N/A	−6.6	−2.2
T_{123}	74.1	110±3	7.41	11.0±0.3	−29.1	−7.3
VAVF						
T_{12}	122.1	181±6	12.21	18.0±0.6	−14.5	−11.5
T_{23}	54.1*	84±3*	10.82*	16.8±0.6*	−8.4	−11.4
T_{13}	58.1	98±6	5.81	N/A	−6.7	−2.9
T_{123}	54.1	81±2	5.41	8.1±0.2	−15.2	−10.7

The VACF model produces the widest pulses but with the lowest SPL. The CAVF model predicts narrower pulses with a higher SPL. The VAVF model predicts the narrowest pulses with the highest SPL. There was also some variation attributed to the choice of modulators in the dual-cascade. For VACF, the predicted duty cycle (and, hence, pulse width) decreased through 20.82%, 19.42% and 17.82% for T_{12}, T_{13} and T_{23}, respectively. However, this was accompanied by a concomitant increase in SPL, from –30.3 to –13.5 dB. For CAVF, a similar trend of decreasing pulse width was apparent, but a dissimilar trend for SPL where SPL was the same for T_{12} and T_{23}, but much higher for T_{13}. In the case of duty cycle, however, the pulse train due to T_{23} was twice the frequency of that due to T_{12} or T_{13}. This is because the frequency applied to the first modulator in the cascade determines the resultant output frequency of the optical pulse train. Subsequent modulators in the cascade contribute to further narrowing of the pulse. Hence, in the case of T_{23}, the frequency applied to the first modulator is 1 MHz, instead of 500 kHz for T_{12} and T_{13}, resulting in a 2 MHz optical pulse train. For VAVF, the trend in pulse width, duty cycle (that is, the frequency doubling of T_{23}) and SPL is the same as for CAVF, with the only exception being the predicted SPL for T_{23} increasing significantly to be approximately 1.5 dB below T_{13}.

While the VACF model is the easiest to implement experimentally and produces the greatest SPL, the much narrower pulses predicted by the variable-frequency models could make such implementations attractive for certain applications despite the less desirable SPL, particularly where thresholding could be applied to reject pulses at the spurious peak level.

Figure V.11 features an image of the oscilloscope display with the three synchronously applied sinusoidal waveforms and the photo-detected optical pulse train of the VACF cascade. The latter exhibits no discernable spurious peaks, however, the resolution of the display is not sufficient to provide an accurate determination of the SPL. Hence the data was captured via the oscilloscope's **universal serial bus (USB)** interface before being re-scaled and normalized for representation in the format of **Figure V.12**, which is also consistent with **Figure V.7** to **Figure V.9**.



	Value	Mean	Min	Max	Std Dev
④ +Width	289.2ns	228.6n	76.00n	389.2n	11.19n
④ Freq	995.6kHz	990.3k	936.5k	1.994M	1.517k
④ +Duty	28.79 %	22.64	7.600	39.03	1.135

Figure V.11 **Real-time representation of the three synchronously applied sinusoidal waveforms (upper) and the photo-detected optical pulse train of the VACF cascade (lower).**

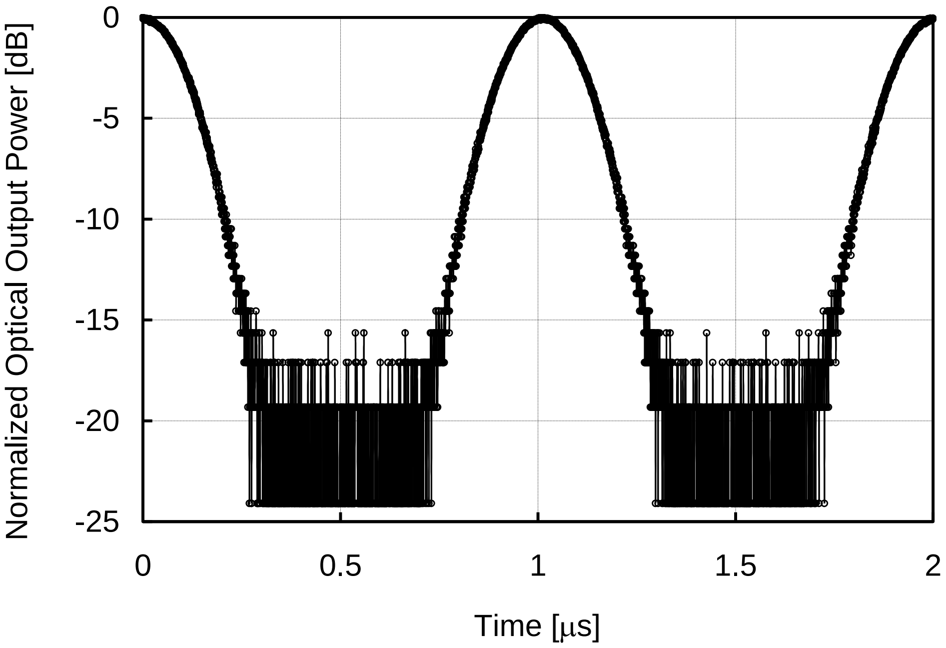


Figure V.12 Representation of the photo-detected optical pulse train of the VACF cascade. The data points were captured using a digital sampling oscilloscope (Tektronix DP4104) and normalized with respect to the maximum.

From the format of **Figure V.12**, the SPL is readily deducible at –15.6 dB. From **Table V-1**, it is apparent that this value represents the lowest achievable SPL for all of the experimental measurements. This is due to a number of factors such as the finite extinction ratio of the individual modulators (specified at 27 dB), the inability to fully overdrive the first modulator (which reduces the achievable extinction ratio for the first modulator) and the finite insertion loss (3 dB) of the modulators in the cascade reducing the achievable signal-to-noise ratio (SNR) of the optical pulse. The noise floor is due to the photo-detector's dark current and the sampling error of the oscilloscope.

From **Table V-1**, it is evident that the same measured SPL value applies to all variants of the VACF cascade regardless of whether or not the first modulator is present. A similar observation can be made with respect to the pulse width and duty cycle for which the experimental measurement of T_{23} and T_{13} is equivalent within experimental error. Hence it is not immediately apparent that the inability to supply the required voltage to the first modulator is of any consequence. For this reason the effect of the inability to fully overdrive the first modulator is investigated in greater depth in this subsection.

Another likely contributing factor to the broader pulse width is the noise due to synchronization error related to the external triggering. This was quantified in **Figure V.10** as a 3% standard deviation about the mean frequency output by the sync generator, which translates from **Table V-1** to a standard deviation about the mean pulse width of up to 5%. The standard deviation and mean statistics were measured using a digital oscilloscope sampling 10000 points per second for two minutes.

The trend in duty cycle measured for the four cascade configurations is consistent with that predicted by the VACF model.

Figure V.13 depicts the CAVF cascade of Haus *et al.* **[27]**, which shows a narrower pulse width, but a significantly higher SPL. It is also immediately apparent that significant asymmetry exists in the location of the spurious peaks. The asymmetry was also apparent, although less obvious, on the real-time linear display. However, the linear scale meant that this asymmetry could not be balanced by adjusting the MZI modulators' DC bias controls. The measured optical pulses were broader than those predicted for this cascade as a result of the synchronization error.

From **Table V-1**, the narrowest pulses were obtained for T_{23} and T_{123} with the output frequency for T_{23} at 2 MHz due to the removal of the first modulator. A similar trend was observed between simulated and experimental pulse-widths across the four configurations (within experimental error). There was also some agreement in the trend for SPL, except the experimental values were higher and the value of SPL for T_{123} was much higher than predicted. The duty cycle for the T_{13} pulse train was not included as its SPL was too high.

For the VAVF cascade in **Figure V.14** the narrowest pulses were obtained with a SPL higher than the VACF cascade, but lower than the CAVF. There was still a degree of asymmetry in the spurious peaks, which could not be balanced by adjusting the DC bias setting. The measured optical pulses were broader than those predicted for this cascade as a result of the synchronization error.

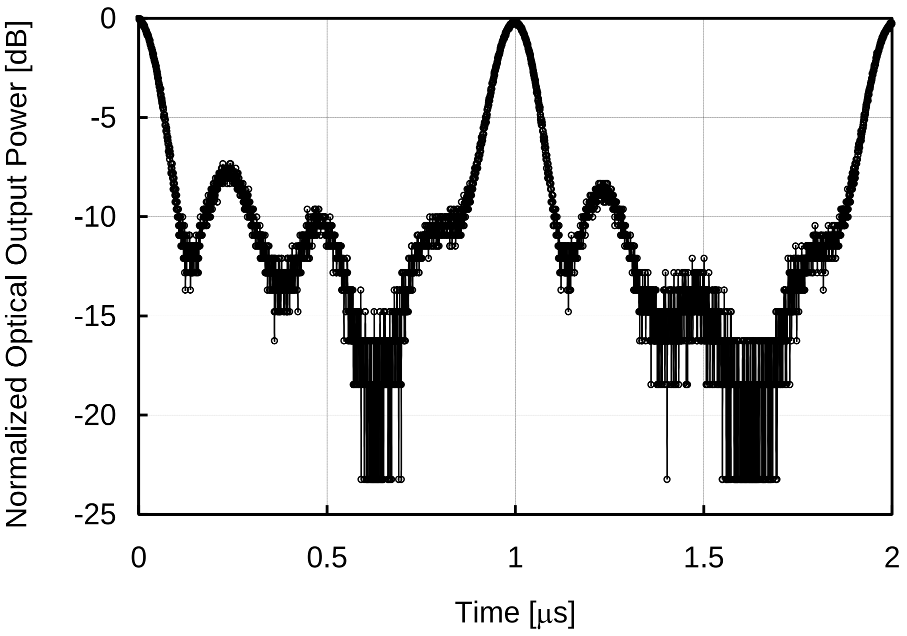


Figure V.13 Representation of the photo-detected optical pulse train of the CAVF cascade. The data points were captured using a digital sampling oscilloscope (Tektronix DP4104) and normalized with respect to the maximum.

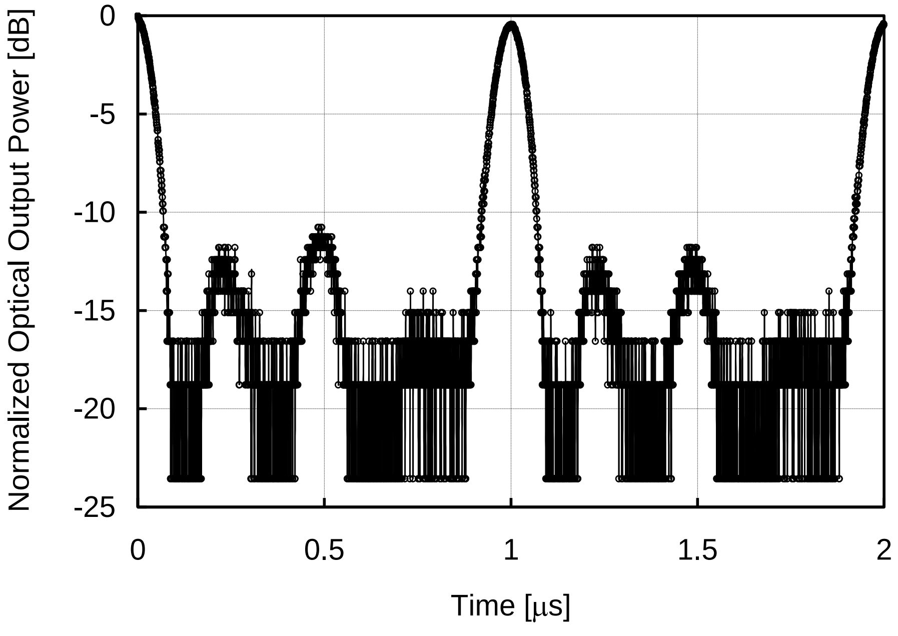


Figure V.14 Representation of the photo-detected optical pulse train of the VAVF cascade. The data points were captured using a digital sampling oscilloscope (Tektronix DP4104) and normalized with respect to the maximum.

The data of **Table V-1** shows similar trends in pulse-width, duty cycle and SPL across the four VAVF cascade configurations compared to the CAVF cascades.

The remainder of this sub-section is focused on the analysis of the experimental results with respect to the inability to supply the required voltage to the first MZI modulator.

The pertinent question is: Does this limitation contribute to a broadening of the pulse and, or a higher SPL?

To address these questions, the simulations were repeated with the limitation applied to the first modulator. The idealized model data from **Table V-1** is re-listed in parentheses in **Table V-2** alongside the limited model data.

One source of broadening has been identified as synchronization error in the experimental set-up. By comparing the experimental data of **Table V-1** with both sets of modeled results, neither of which were affected by this synchronization error, the contribution to broadening of the modulator under-voltage can be inferred.

From **Table V-2**, the effect of the first modulator is most readily discernible by removing it. It can be seen that consideration of only the T_{23} cascade configuration across all three models, predicts pulse parameters that are invariant with the respect to the voltage applied to the first modulator. In all other cases where the first modulator is present, the undersupplied modulator leads to an increase in the predicted SPL. Of these other non-ideal cases, the VACF model features broader pulses and larger duty cycles and this is apparent to a lesser extent for T_{12} in the CAVF and VAVF models.

The similarity between ideal and non-ideal pulse parameters for non-T_{12} CAVF and VAVF is due to the pulse narrowing being a result of the frequency multiplication. However, the increased SPL associated with T_{13} and T_{123} indicates that the under-voltage of the first modulator resulted in a reduction of the achievable extinction of light output by the modulator. This is illustrated graphically in **Figure V.15** in a plot of the output of the first modulator for both ideal (full-voltage) and non-ideal (under-voltage) cases.

Table V-2 Simulation results for modulator cascades where the first modulator is supply limited to 83% of the required voltage. The asterisk '*' denotes a configuration where the output frequency is 2 MHz for a 1 MHz input which is realized by the removal of the 1st modulator. The ideal data from Table V-1 is included in parentheses wherever there is a difference.

Cascade Configuration	Pulse-width (ns)	Duty Cycle (%)	Spurious Peak Level (dB)
VACF			
T_{12}	222.2 (208.2)	22.22 (20.82)	−20.1 (−30.3)
T_{23}	178.2	17.82	−13.5
T_{13}	206.2 (194.2)	20.62 (19.42)	−16.5 (−24.2)
T_{123}	164.2 (158.2)	16.42 (15.82)	−25.2 (−38.5)
CAVF			
T_{12}	154.2 (150.2)	15.42 (15.02)	−11.7 (−25.5)
T_{23}	74.1*	14.82*	−25.5
T_{13}	82.1	8.21	−4.3 (−6.6)
T_{123}	74.1	7.41	−11.7 (−29.1)
VAVF			
T_{12}	126.1 (122.1)	12.61 (12.21)	−11.8 (−14.5)
T_{23}	54.1*	10.82*	−8.4
T_{13}	58.1	5.81	−4.5 (−6.7)
T_{123}	54.1	5.41	−11.8 (−15.2)

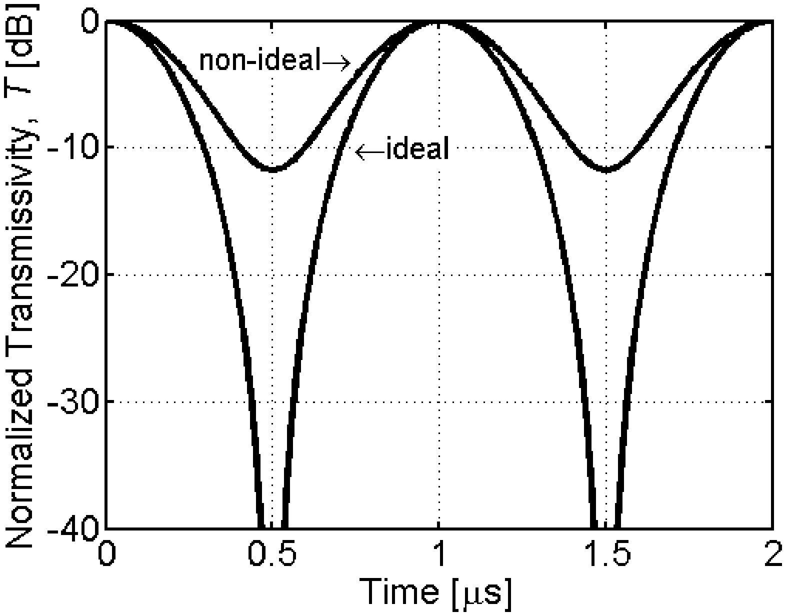


Figure V.15 Comparison plot of the modeled optical output of the first modulator for the ideal (full-voltage) and non-ideal (under-voltage) cases. This graph applies to all three-modulator cascade models.

Figure V.15 illustrates that in the resultant pulse, the increase in the width is less of a problem than the increased SPL. Both transmissivity waveforms have similar 3 dB widths, but in the ideal case the transmissivity decreases dramatically. In fact, for almost 50% of the pulse period the ideal transmissivity is more than 10 dB below maximum.

The predominant mechanism for pulse broadening is the synchronization error of the experimental setup. However, there is also a lesser contribution to broadening from the under-voltage constraint on the first modulator. The simulation analysis indicates this contribution is minimal for the CAVF model and maximal for the VACF model. This is consistent with their respective mechanisms' pulse-narrowing effect.

3. Fiber-Lattice Accumulator

The availability of high pulse repetition frequency mode-locked lasers **[29]** and wide bandwidth optical modulators **[30]** has lead to the emergence of high speed optical signal processing. Moslehi *et al* **[11, 12]** proposed the implementation of fiber-optic lattice structures to perform various high-speed time domain and frequency domain functions. Optical integration, in particular, has become an enabling technology for high-speed applications such as optical filtering **[31]** and analog-to-digital conversion. The latter having received special attention in the last few years with a number of configurations investigated **[32, 33, 34, 35]**.

The operation of integration or accumulation is an important concept in sampling and the availability of a photonic sampled-data accumulator can benefit many schemes for direct analog-to-digital conversion. For example, by embedding an accumulator within a feedback loop around a quantizer, such as is done in Σ-Δ modulation to force the average value of the quantized signal to track the average of the input signal **[14],** higher oversampling ratios can be achieved. High oversampling ratios directly lead to a higher achievable dynamic range as the resultant quantization noise can be spectrally shaped to a band outside the signal band of interest and removed by subsequent decimation filtering **[14, 36]** as was described in **Figure III.4**.

Photonic accumulation ultimately has the potential advantage of extending the performance of the Σ-Δ modulation technique into the very high frequency range and beyond. Optical lattice filter architectures have been proposed for performing accumulation since they can be designed to operate at very high bandwidths with repetition rates in the THz range **[**2**,** 6**,** 8**, 36]**.

Optical accumulation using lattice filters has been published by other workers *[31]*. Their design was composed of a stack of partially reflective mirrors where the filter design parameters were specified by the mirror reflectivities.

In this section, a uni-directional accumulator based on a coherent four-port fiber lattice filter is investigated. The accumulator has two directional couplers, an embedded optical amplifier and a delay line. The function of this device relies on the fact that since light intensity is always positive, the interference between the input optical wave and the recirculating optical wave results in the wave amplitudes being added constructively, if they are in phase within the combining directional coupler, leading to accumulation. Where the input wave is π radians out of phase with the recirculating wave, destructive interference occurs, leading to leakage. Therefore, accurate phase control is essential for the intended function of this device.

This section begins with an examination of two different architectures for sampled-data accumulation, which have been considered for the NPS design. This is followed by a description of experiments that were attempted in order to quantitatively evaluate the device performance and demonstrate its function.

a) Sampled-Data Accumulation

In this sub-section, a brief description of the sampled-data accumulator transfer function is presented. To begin, note that discrete-time integration is a numerical approximation to continuous integration, for which the transfer function is $H(s) = 1/s$. Various numerical approximations to the integration operator are available, such as Euler's backward, Euler's forward and Tustin's (bilinear transformation or trapezoidal rule) methods. While Tustin's is the most accurate (and stable), it is generally not much different than Euler's methods when the step size is kept sufficiently small and aliasing is minimal. Euler's forward method is the least accurate and least stable, with a tendency to map poles in the left-half of the *s*-domain to poles outside the unit circle on the *z*-domain **[37]**, however, it does have the advantage of expressing the output variable as an explicit function of the input variable.

This discussion of first-order sampled-data accumulators is confined to those employing Euler's methods. This is justified on the basis of an interest in applications involving a high oversampling ratio which provide both sufficiently small sampling intervals and sufficiently good signal approximations. Moreover, constraints are employed in the selection of the accumulator's tunable parameters to ensure poles are contained within the unit circle in the *z*-domain.

To assist with the discussion a unit normalization of the sampling interval is employed. **Figure V.16 (a)** illustrates the block diagram of a sampled-data accumulator employing feed-back delay (Euler's backward method), with the well known transfer function **[37, 38]**:

$$H(z) = \frac{A}{1 - Bz^{-1}}$$

Equation (V-8)

where A is a multiplying factor, B is the accumulator leakage coefficient and z^{-1} is the delay operator τ. If the accumulator is ideal, then $B = 1$ (no leakage), however, this is not the case in practice once equipment limitations are taken into account.

Figure V.16 (b) features the feed-forward delay sampled-data accumulator (Euler's forward method). It has the well-known transfer function:

$$H(z) = \frac{Az^{-1}}{1 - Bz^{-1}}$$

Equation (V-9)

It is also important to note that in both sampled-data accumulators, the sign of the sample being fed back to the adder is accounted for in the addition.

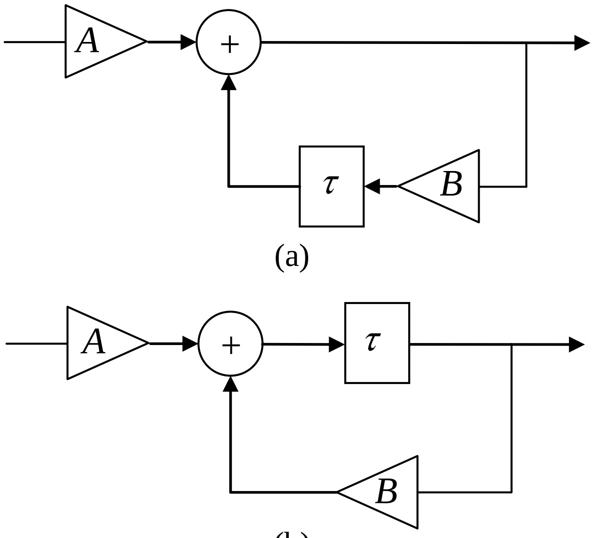


Figure V.16 Sampled-data accumulator block diagrams showing (a) feed-back delayed and (b) feed-forward delayed methods.

b) Accumulator Description

A schematic diagram of the NPS four-port fiber lattice accumulator is shown in **Figure V.17.**

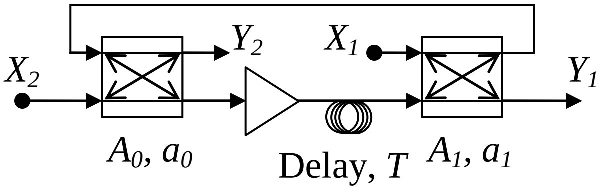


Figure V.17 One-directional four-port fiber lattice accumulator configurations: (i) selection of X_2 and Y_1 (terminating X_1 and Y_2) gives the feed-forward delay path; and (ii) selection of X_1, Y_2 gives the feedback delay path.

The fiber lattice contains two four-port directional couplers A_0 and A_1, with respective power coupling ratios a_0 and a_1. Also X_1 and X_2 are the input ports, Y_1 and Y_2 are the output ports and the delay is described by the transit time, T, of an optical pulse through a fiber spool of known length. An optical power amplifier (Semiconductor Optical Amplifier - SOA) with gain G is included. The gain contributes to the stability of the fiber lattice filter.

By choosing different combinations of directional coupler input and output ports in the fiber lattice structure, a variety of known transfer functions (transmissivities) can be selected **[11,39]**. With input X_1 and output Y_2 selected and X_2 and Y_1 optically terminated, the expression for the transmissivity of the feedback delay (2 coupler recirculating delay line) accumulator is as follows:

$$H_{21}(z) = \frac{1-a_0 \quad 1-a_1}{1-a_0 a_1 G T z^{-1}}$$

Equation (V-10)

Here, a_0 and a_1 are the directional coupler *cross* ratios and (1 - a_0) and (1 - a_1) are the *bar* ratios. Note that this transmissivity has the same form as **Equation (V-8)** where the delay is in the feedback path and T is normalized with respect to the sampling time such that the multiplying factor, $A = \ 1-a_0 \quad 1-a_1$ and the leakage coefficient, $B = a_0 a_1 G$.

The transmissivity for the feed-forward delay (2 coupler non-recirculating delay line) path, which comes from the selection of input X_2 and output Y_1, with X_1 and Y_2 optically terminated, is given by:

$$H_{12}(z) = \frac{1-a_0 \quad 1-a_1 \quad GTz^{-1}}{1-a_0 a_1 G T z^{-1}}$$

Equation (V-11)

The transmissivity in **Equation (V-11)** has the same form as Equation (V-9) where the delay is in the feed-forward path and T is normalized with respect to the sampling time such that the multiplying factor, $A = \ 1-a_0 \quad 1-a_1 \quad G$ and the leakage coefficient, $B = a_0 a_1 G$.

The correct (stable) operation of the fiber-lattice accumulator requires that the power coupling coefficients for the directional couplers (a_0, a_1) and the optical gain G must be matched such that the leakage coefficient B is approximately equal to 1. This ensures both a linear response for a DC input and the existence of a pole of the transfer function within the unit circle. Previous workers have analyzed the effects of integrator leakage **[40,41]** and others have demonstrated that the vector-couple ($\boldsymbol{a_0}$, $\boldsymbol{a_1}$) maps the values of G to a Toeplitz matrix $\boldsymbol{G}$ subject to the constraint $1 < G < (a_0 a_1)^{-1}$ **[**6**,** 8**].** For example, a linear monotonically increasing accumulator output is obtained with a_0=0.4, a_1=0.6, and G=4.166 (B=0.9998) **[**6**]**. When any of these parameters deviate from their matched values such that the leakage coefficient no longer approximates unity, the accumulator output dramatically becomes non-linear. For $B > 1$, the pole of the transfer function is outside the unit circle.

c) Experimental Results

The experimental set-up is illustrated in **Figure V.18**. The optical source used was the narrow linewidth **distributed feedback (DFB)** continuous wave laser diode (EM4-253) with a wavelength of 1550 nm described in **Section V.A.1**. The laser diode was pigtailed with **polarization maintaining (PM)** fiber. Pulse modulated operation was achieved externally using an appropriately biased Mach-Zehnder modulator (JDS Uniphase) with PM fiber input and **single mode (SM)** fiber output. The couplers were mechanical **variable ratio couplers (VRC)** with PM fiber where the coupling ratios were adjusted using Vernier micrometers. The optical amplifier was a multiple quantum well SOA (JDS Uniphase CQF871/0) with a wavelength of 1550 nm and this was connected using SM fiber. The manufacturer quoted gain of this SOA was 16 dB with a saturated output power of 10 dBm (10 mW). The delay line was a spool of SM fiber with a loss factor of 0.22 dB/km. A number of calibration measurements were performed to determine the properties of the various fiber-lattice components.

Calibration measurements were performed using the set-up illustrated in **Figure V.19** to determine the achieved coupling ratios (cross and bar) from the Vernier setting and the results of these measurements are illustrated in **Figure V.20**.

Electro-optically pulse modulated laser light was input to one of the inputs of the couplers. The unused input was isolated using a low reflection coefficient (-55 dB) optical attenuator. For each Vernier setting, the peak-to-peak output voltage and its associated measurement error was measured using an oscilloscope.

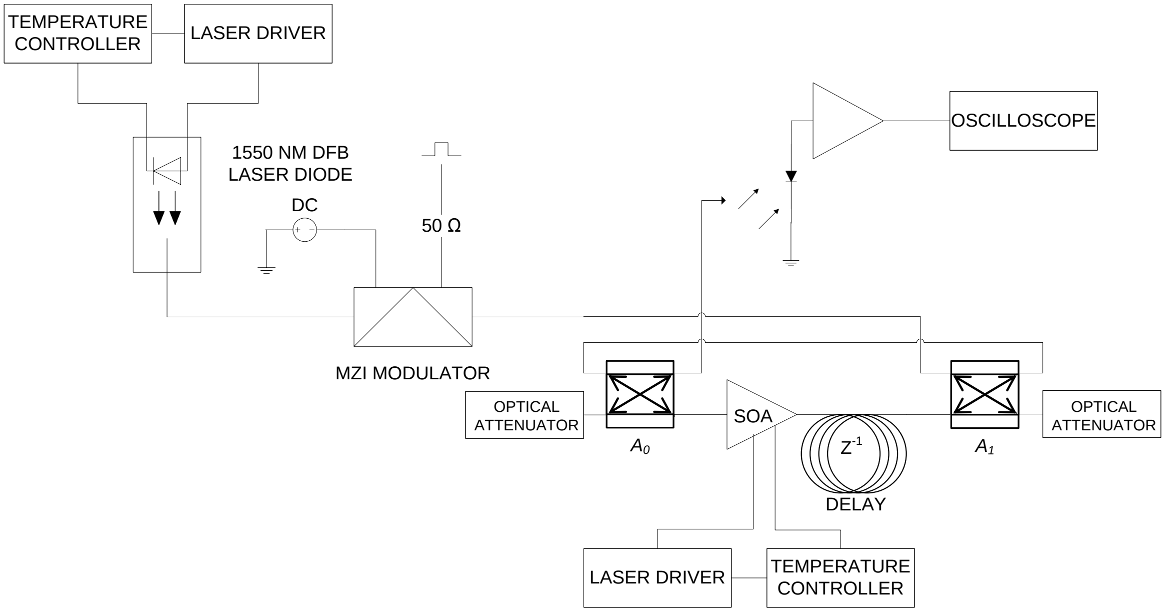


Figure V.18 **Set-up of the fiber-lattice accumulator experiment featuring feedback delay.**

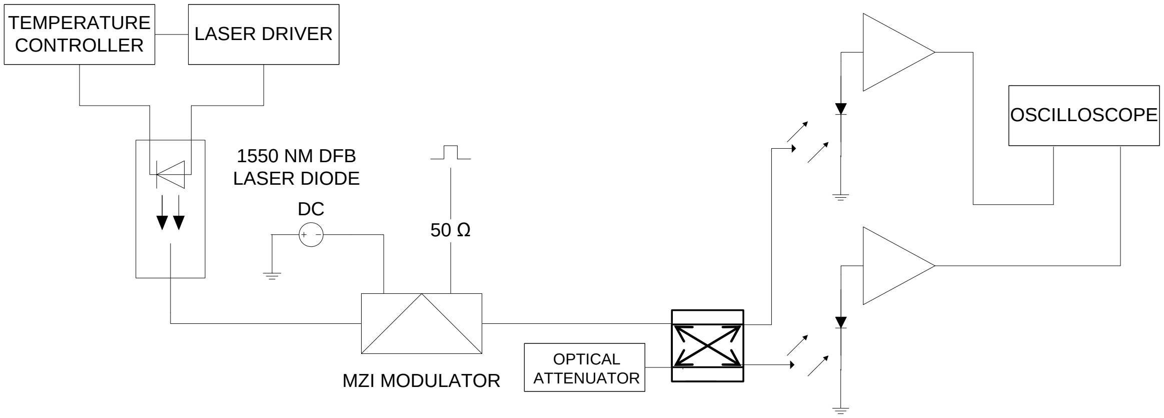
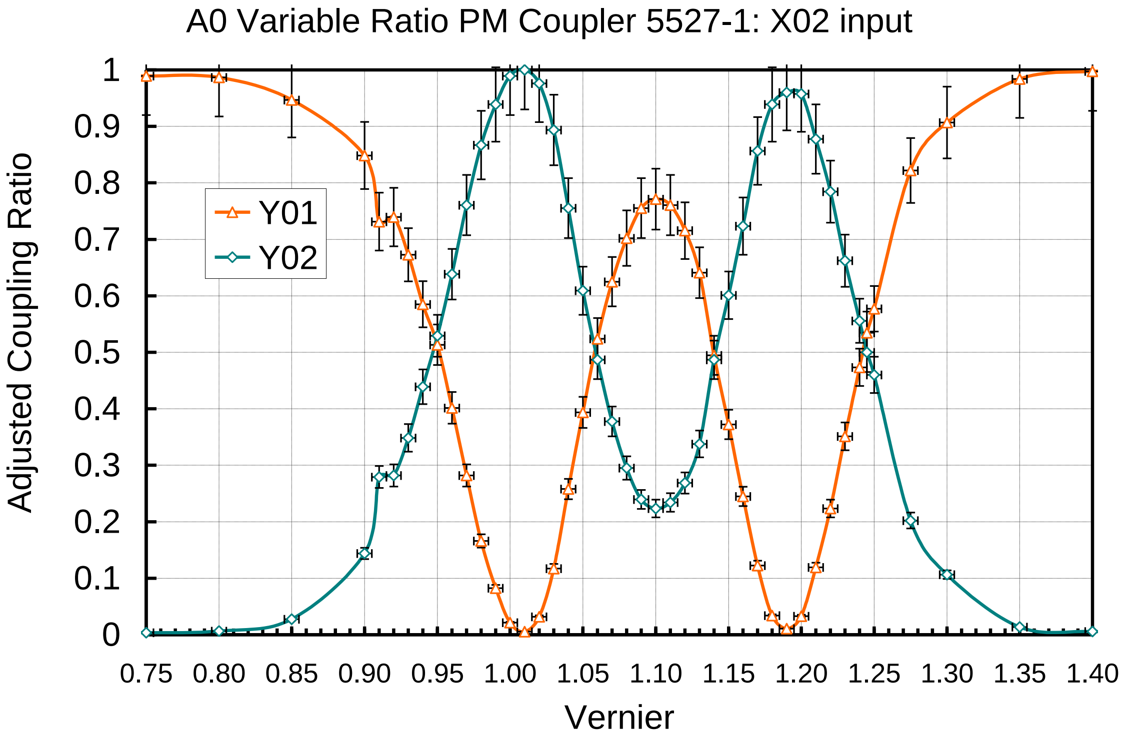


Figure V.19 **Set-up for the measurement of the coupling ratios plotted in Figure V.20.**

The measurements were normalized with respect to the measured maximum peak-to-peak photo-detected input voltage as featured in **Figure V.20**. The normalized relative measurement error of the optical output (the Y-axis error) was calculated to be ±7% and the X-axis error was determined to be half the smallest division of the scale of the Vernier, i.e. 0.005. Thus for the two couplers, the cross ratios corresponded to $a_0 = Y_{01} / X_{02}$ and $a_1 = Y_{12} / X_{11}$, respectively. Conversely, the bar ratios corresponded to $1 - a_0 = Y_{02} / X_{02}$ and $1 - a_1 = Y_{11} / X_{11}$, respectively.



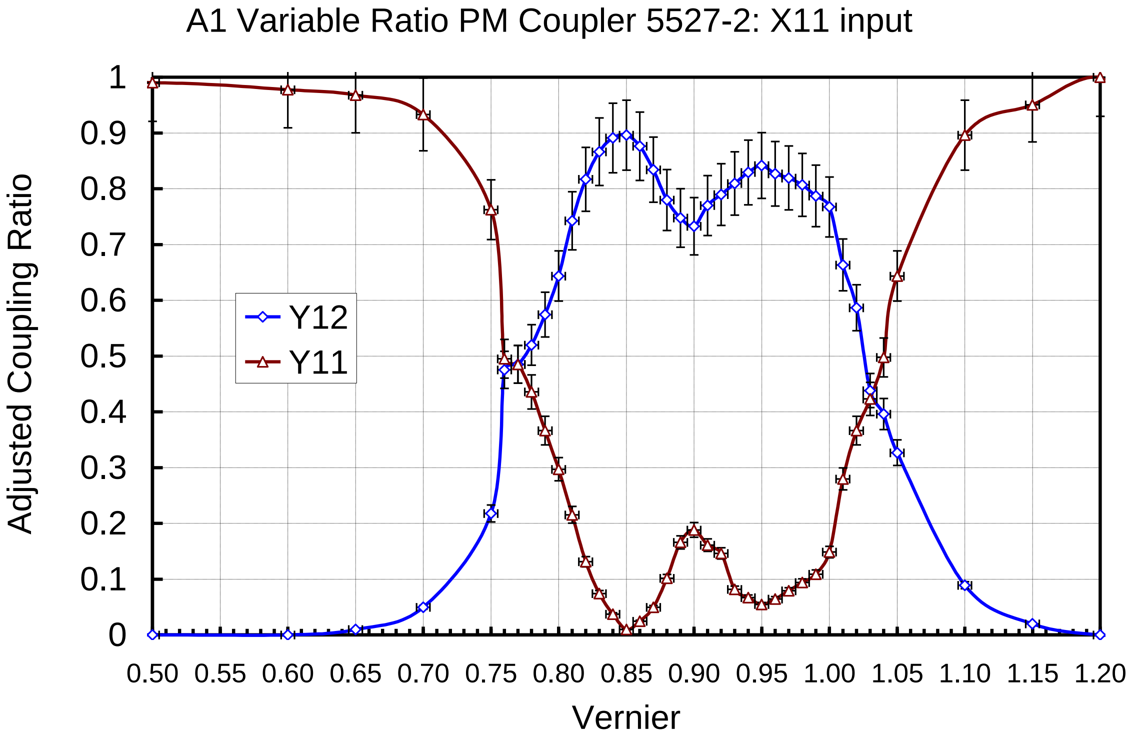


Figure V.20 Coupling characteristics of the *A_0* and *A_1* variable ratio couplers.

Calibration was also required for the optical amplifier to determine its optical gain response as a function of the drive current. The measured gain response is plotted in **Figure V.21**.

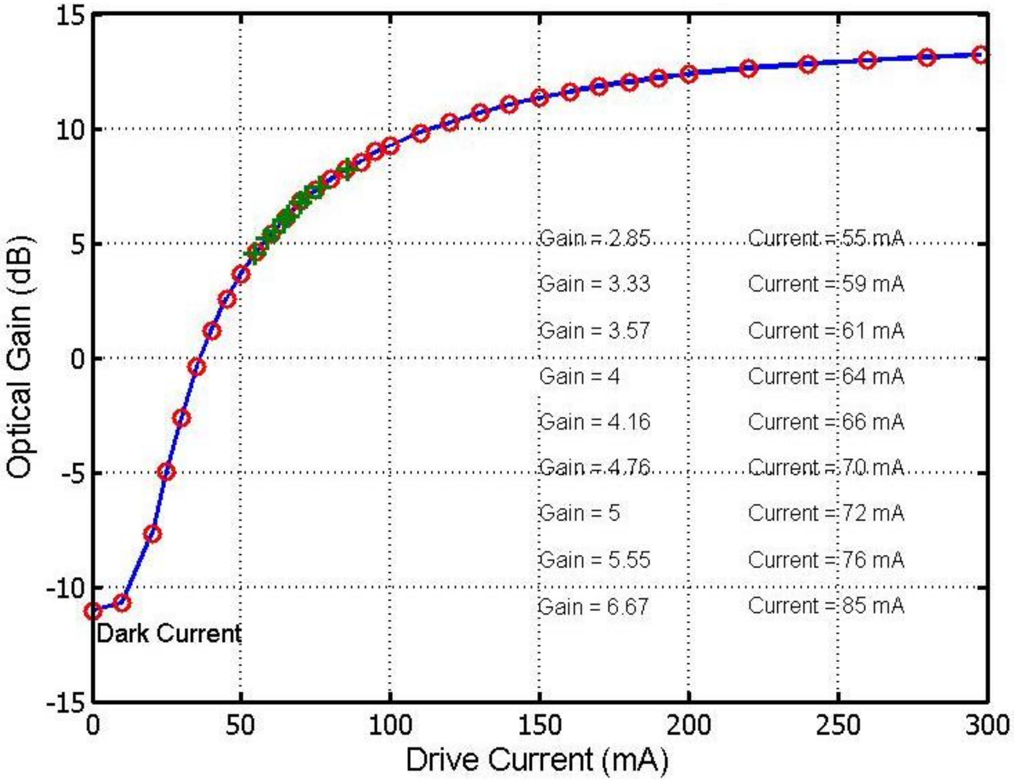
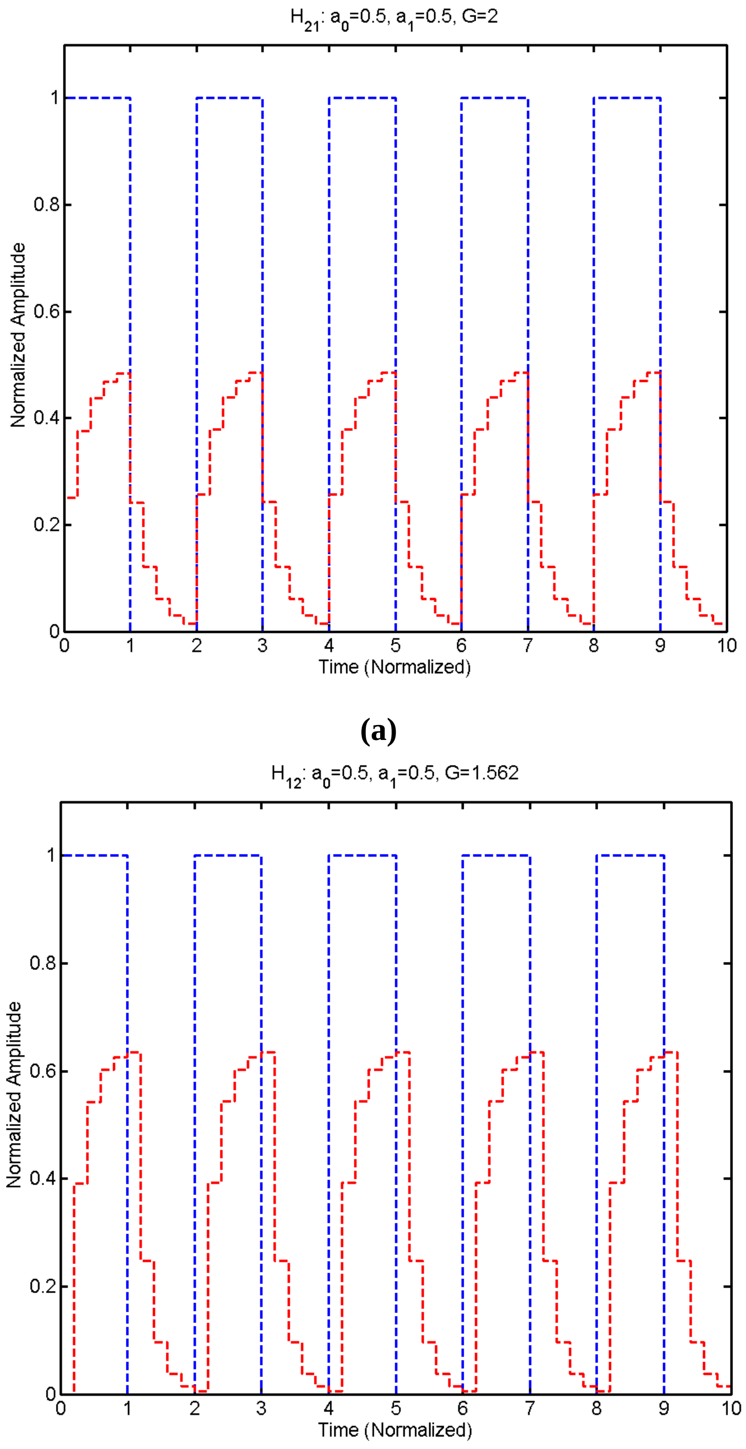


Figure V.21 Optical Gain Response for the CQF871/0 multiple quantum well semiconductor optical amplifier as a function of input drive current. The red circles represent the various drive current settings from which the gain was measured. The green plus-signs represent the interpolated values of drive current necessary to achieve various values of gain within the range useful for optical accumulation.

The maximum achievable optical gain was measured to be 13 dB, for a saturating output power of 12.6 mW (11 dBm). With the gain response of the optical amplifier and the coupling ratios of the couplers characterized, the experiments proceeded in an attempt to achieve optical integration. To verify the experiments, calculations were performed to simulate the optical integration processes that were investigated, i.e. feed-back and feed-forward delay. Simulations of continuous accumulation of a 50% duty cycle pulsed input signal are illustrated in **Figure V.22**, for both delay configurations. The accumulator output correctly represents a sawtooth waveform as the numerical integral of the pulsed input.



(a)

(b)

Figure V.22 Simulated optical integrator (red) output for (a) feed-back delay and, (b) feed-forward delay fiber-lattice accumulator performing continuous accumulation of a 50% duty cycle pulsed input (blue). G-values were chosen for steady state response [6].

Increasing the optical gain from the steady state values applied in these simulations, to the critical value (*G* = 4) and beyond, results in an accumulator output that increases from asymptotically bounded above (quasi-concave) (*G* < 4) to linear monotonically increasing (*G* = 4) to exponentially unbounded (*G* > 4).

Figure V.23 illustrates the simulation of sampled accumulation of a 50% duty cycle pulsed input with additive thermal noise. The input is sampled with a 50% duty cycle with a sampling PRF that is 10× the input PRF.

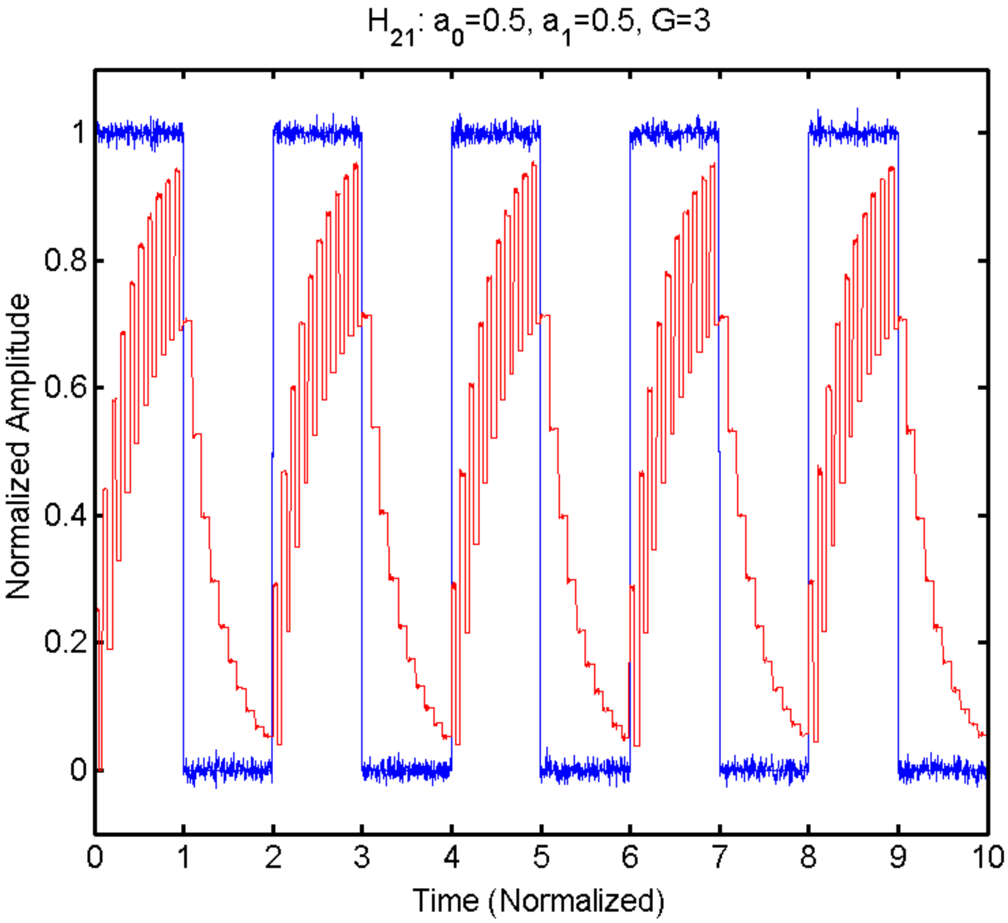


Figure V.23 Simulated optical integrator output (red) output for a feed-back delay fiber-lattice accumulator performing sampled accumulation at a 5× oversampling rate of a 50% duty cycle pulsed input (blue) with additive thermal noise.

The accumulator employs feed-back delay with coupling coefficients of 0.5 and an SOA gain of 3. **Figure V.23** is qualitatively similar to the accumulator output obtained in laboratory experiments with the fiber-lattice accumulator. However, the fiber-lattice accumulator could only be implemented experimentally as a leaky accumulator, due to the limitations of the SOA. For optical signals input to the SOA approaching the measured saturated output power limit of 11 mW, the maximum achievable gain decreases leading to a decrease in the leakage coefficient. Thus, this limiting factor prevents the accumulator from achieving even a near linear monotonically increasing response.

B. COMPONENT CHARACTERIZATION

The functionality of all components was verified by measurements that were compared against their respective specifications and product data sheets. In some cases complete verification was not achievable due to limitations in the available laboratory test equipment. Where this was the case is made clear in this report.

For the Mach Zehnder modulators this required confirming correct V_π (bias voltage) and insertion loss values. The Mach Zehnder modulators with their **polarization maintaining (PM)** fiber pigtails were originally fusion spliced to **single-mode (SM)** fiber. These splices were replaced with adjustable key polarization maintaining FC connectors between PM and SM fibers. Polarization alignment was achieved using these in-line polarization controllers. Once set-up, chassis mounted and correctly aligned, the modulator and polarization controller combination were observed to be less sensitive to vibrations and other mechanical stresses.

The photodetector was a New Focus Instruments, Model 1024 high speed photodetector with a rise time of 12ps and a bandwidth of 26GHz. This high-speed photodetector was powered by a 9V DC alkaline battery source which quickly discharged after regular use. A DC-DC regulated power supply was constructed from available parts to take a 12V DC sealed lead-acid battery (SLAB) source and convert the 12V to regulated 9V DC via two outputs. The easily rechargeable 12V SLAB maintained its charge for much longer periods. AC power was not used to avoid mains interference.

The photodetector's full bandwidth could only be utilized without gain, via the SMA connector mounted on the device's backplane, the signal output of which typically requires some amplification. The SMA connector on the front plane is limited to frequencies up to 50 kHz. The limit is imposed by the frequency response characteristic of the device's built-in trans-impedance amplifier. The front plane connector is otherwise only used for bias port monitoring, that is, checking the battery supply is satisfactory. For applications above 50 kHz that require amplification, the electronic output of the photodetector should be input to a bandwidth matched low noise amplifier. The photo-detector manufacturer supplies travelling wave amplifiers, however at $3k USD, this was cost prohibitive.

The maximum CW input power of the photodetector was 1 mW. A 10 mW pulsed input power was specified as acceptable, but no duty cycle was specified. For this reason, the input optical power to the photo-detector was limited to an arbitrarily selected maximum of 1.0 mW in pulsed mode.

To overcome insertion and connector losses in the set up between the laser source and the photodetector, the laser was driven at its maximum laser diode forward current, which corresponded to its maximum output optical power. The average maximum power was measured using an optical multimeter to determine the requirements for the insertion of an optical attenuator at the input of the photodetector. The optical attenuator was a fixed value attenuator. Variable fine tuning of the optical power can be achieved through adjustable key polarization maintaining FC connectors, fitted to single mode fiber input to the photodetector. This acts as a fiber analyzer on polarized light emerging from a polarization maintaining fiber.

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VI. SUMMARY

A narrow band photonic sigma-delta ADC was constructed with a maximum oversampling frequency of 2 MHz delivered using a cascade of three MZMs to ensure a CW optical carrier signal. Assuming a 10× OSR, the resultant maximum allowable bandwidth of the signal of interest is 100 kHz for 50% duty cycle oversampling pulses.

Stable optical pulse trains extending across more than three pulses could not be achieved due to the inadequate synchronization that was experienced with the waveform generators. The associated pulse broadening also contributed to inconsistent pulse width of the optical pulses. These issues could be addressed by replacing the waveform generators with versions having greater output voltages or replacing the MZMs with versions having smaller V_π-values. Higher gain amplifiers could also be employed. In a wide-band photonic sigma-delta ADC application, stable optical pulses would be achieved with a mode-locked laser.

Experiments were performed with the phase modulator to measure the linewidth of the laser source using the delayed self-heterodyning interferometer technique. However, when the phase modulator which was used in this linewidth measurement was incorporated into the narrowband photonic sigma-delta ADC at the input of the fiber-lattice accumulator, it was not possible to verify its function against the numerous simulations presented by previous workers. The phase modulator was intended to provide coherent addition of light pulses modulated with positive RF voltage through constructive interference, and subtraction of light pulses modulated with negative RF voltage through destructive interference. Previous work **[**9**,10]** had not been able to provide experimental verification of the phase modulator function and a lack of phase coherence had been cited as a reason for not achieving coherent integration in the fiber-lattice accumulator. This lack of coherence was attributed to an insufficiently narrow linewidth (i.e. insufficient coherence length) of the laser source used in this work. However, it should be noted that in this previous work, the requirement for impedance matching between the comparator output and the phase modulator RF input had been overlooked, which lead to insufficient current stimulating the modulator’s electro-optic crystal. The recent experiments presented in this report demonstrated that the coherence length of the new laser was sufficient to ensure phase coherence in the fiber-lattice accumulator. That is, the delay path of the accumulator was less than the laser's coherence length. Despite the implementation of a narrow linewidth laser and impedance matching it was not possible to verify the integration function of the fiber-lattice accumulator, except for a leaky integrator. The fiber-lattice accumulator was not able to produce sufficient gain to achieve the required linear monotonic output thereby preventing the ADC from tracking the amplitude of the input signal of interest and producing the necessary accumulate up and accumulate down signals as the sign and magnitude of the input signal + feedback (sigma stage) changes. This was caused by the saturating output power level (measured at 11 dBm) of the SOA, which reduced the achievable gain as the power of the optical pulses input to the SOA increased. This limitation would be addressed by replacing the SOA with a version that specifies a sufficiently large saturation output power level.

In the wide-band photonic sigma-delta ADC architecture, the maximum allowable bandwidth of the signal of interest is limited by the bandwidth of the electronic components such as comparators, photodetectors, signal conditioning and summing amplifiers. This is consistent with published findings **[42].** If a push-pull MZM setup is used **[**2**]**, a summing amplifier is not required. However, the MZM bandwidth is required to match the oversampling pulse bandwidth. Current technology COTS comparators (e.g. SiGe) have maximum operating frequencies of the order of 26 GHz. For a 10× OSR, the maximum allowable bandwidth of the signal of interest is 130 MHz for 10% duty cycle oversampling pulses.

Replacing the fiber-lattice accumulator with the UCSB developed EO resonator (total internal reflection mirror ring resonator) will constrain the oversampling bandwidth of the wide-band ADC according to the resonator's dimensions. Its design should therefore reflect the bandwidth limitations imposed upon current technology components. It is a recommendation of this report that the current NPS specification of 10 GHz PRF and 10 ps pulse-width for the UCSB resonator should be relaxed by at least one order of magnitude. Maintaining the existing specification requires electronics technology that currently does not exist thereby warranting additional effort to research, develop or acquire such technology, which would cause unknown delays to the current project. Moreover, the higher bandwidths require very expensive or non-existent laboratory instrumentation to test and evaluate the performance of the wide-band ADC system.

A successful implementation of wide-band photonic ADC in the laboratory is likely to be achieved in the near future, given sufficient resources and technological advances. However, transferring this technology to the military environment will inevitably raise more practical and systems issues that will need to be addressed. For example:

- Ruggedization of a wide-band photonic sigma-delta digital antenna system to operate robustly in air, marine and land environments.
- Climate control and conditioning to maintain the system in some desired operating range of temperature and humidity.
- Power requirements such as consumption, control and stability.
- Integration of the system into an existing sensor network, combat system, etc.
- The enhanced ability to detect LPI signals will logically mean that many more signals will be detected. Additional resources will be required to process and handle these detections.

All of these issues will likely warrant trade-offs between the degree of capability which can be delivered and the platform(s) on which the system can be installed. It may well be the case that only larger platforms such as ships and large aircraft (C2 platforms) can meet the system requirements necessary to achieve the desired capability.

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