Hindawi Publishing Corporation
International Journal of Microwave Science and Technology
Volume 2011, Article ID 945189, 4 pages
doi:10.1155/2011/945189

Research Article

Temperature Dependence of GaN HEMT Small Signal Parameters

Ali M. Darwish,[1,2] Amr A. Ibrahim,[1] and H. Alfred Hung[2]

[1] *Electronics Engineering Department, The American University in Cairo, AUC Avenue, New Cairo 11835, Egypt*
[2] *RF Electronics Branch, US Army Research Laboratory, 2800 Powder Mill Road., Adelphi, MD 20783, USA*

Correspondence should be addressed to Ali M. Darwish, darwish@alum.mit.edu

Received 12 August 2011; Revised 30 November 2011; Accepted 9 December 2011

Academic Editor: Ichihiko Toyoda

This study presents the temperature dependence of small signal parameters of GaN/SiC HEMTs across the 0–150°C range. The changes with temperature for transconductance (g_m), output impedance (C_{ds} and R_{ds}), feedback capacitance (C_{dg}), input capacitance (C_{gs}), and gate resistance (R_g) are measured. The variations with temperature are established for g_m, C_{ds}, R_{ds}, C_{dg}, C_{gs}, and R_g in the GaN technology. This information is useful for MMIC designs.

1. Introduction

Devices based on wide bandgap materials (such as GaN, SiC) promise much higher power densities and potential for higher temperature operation than GaAs, Si, and SiGe devices [1–3]. The reliability and performance of HEMTs and MMICs depend critically on the device operating channel temperature [4, 5]. Previous studies [6–11] have focused on various effects with temperature. However, the referenced temperature was the chuck (or base plate) temperature. This study presents characterization and comparison of two current GaN/SiC devices from different foundries across temperature where the temperature is reference to the channel reference.

2. Measured Results

To quantize the effect of temperature on the performance of GaN/SiC device, two state-of-the-art AlGaN/GaN HEMT devices were characterized at −25, 25, 75, and 125°C base plate (on-wafer chuck). At each temperature, *S*-parameters are measured at V_d = 20 V and a fixed drain current (equal to 25% of the room temperature I_{dss}) and the small signal extracted. The dissipated DC power is fixed, and hence the channel temperature to the chuck temperature is constant. For example, in the first device the temperature difference between the channel and the chuck was 26°C (calculated from finite element simulation of the structure), temperature contours shown in Figure 1. In both devices, the gate length (L_g) for the HEMT was about 0.25 μm and the gate width was 2 × 100 μm. A standard equivalent circuit is used to match the measurements, see Figure 2. The model used includes a source inductance L_s and resistance R_s to model the via holes to ground. In the current case, a via hole structure was measured independently in order to find L_s and R_s. Additionally, the input and output feeding structures (Figure 3), were constructed on full wave analysis simulator (EM Sight from Microwave Office Suite) and simulated. The structures were used to de-embed the *S*-parameters. This is a critical step to separate the intrinsic device behavior from the extrinsic-layout-dependent behavior. In the optimization, the *S*-parameters are normalized to give equal-weight real and imaginary parts as well to all the parameters (S_{11}, S_{21}, S_{12}, and S_{22}). Upon de-embedding and optimization of the S parameters against the layout circuit, several important points are noted for both devices. First, the optimization is very robust and always arrives at the same values for various R_s and L_s. Second, the match between the measurement and model is very close, at all frequencies and temperatures, see Figure 4. Third, the optimized values for the parasitic components L_g, L_d, C_{ds}, and R_d are zero, indicating that the feeding structures account for them completely. The only exception is R_g where the gate resistance was not fully included in the input matching structure because the

Report Documentation Page

Form Approved
OMB No. 0704-0188

1. REPORT DATE	2. REPORT TYPE	3. DATES COVERED
NOV 2011		**00-00-2011 to 00-00-2011**

4. TITLE AND SUBTITLE	5a. CONTRACT NUMBER
Temperature Dependence of GaN HEMT Small Signal Parameters	5b. GRANT NUMBER
	5c. PROGRAM ELEMENT NUMBER
6. AUTHOR(S)	5d. PROJECT NUMBER
	5e. TASK NUMBER
	5f. WORK UNIT NUMBER
7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES) **US Army Research Laboratory,RF Electronics Branch,2800 Powder Mill Road,Adelphi,MD,20783**	8. PERFORMING ORGANIZATION REPORT NUMBER
9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)	10. SPONSOR/MONITOR'S ACRONYM(S)
	11. SPONSOR/MONITOR'S REPORT NUMBER(S)

12. DISTRIBUTION/AVAILABILITY STATEMENT
Approved for public release; distribution unlimited

13. SUPPLEMENTARY NOTES

14. ABSTRACT

15. SUBJECT TERMS

16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT	18. NUMBER OF PAGES	19a. NAME OF RESPONSIBLE PERSON
a. REPORT	b. ABSTRACT	c. THIS PAGE			
unclassified	**unclassified**	**unclassified**	**Same as Report (SAR)**	**4**	

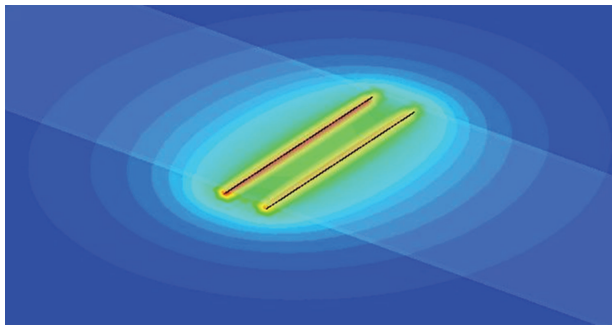

Figure 1: Temperature contours of $2 \times 100\,\mu$m device based on finite element simulation.

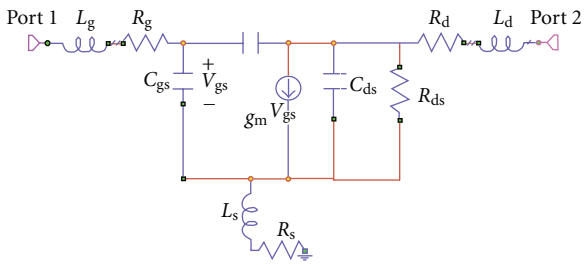

Figure 2: Equivalent circuit used to extract small signal parameters. The ground vias are modeled as a series inductor and resistance.

resistance is sensitive to the exact gate dimension and shape (T-gate, Mushroom gate, etc.) information which was not available.

For each device type, two identical transistors were measured to check for consistency of the results. Figures 5, 6, 7, 8, and 9 show the temperature dependence of C_{gs}, C_{dg}, R_g, R_{ds}, and g_m, respectively. In all cases, the values are normalized to 1 mm gate periphery. For example, in Figure 4, a C_{gs} value of 1 pF corresponds to 1 pF/mm, and, for a $2 \times 100\,\mu$m device, C_{gs} would be 0.2 pF. Figure 10 shows the saturation current (I_{dss}).

3. Discussion and Analysis

The measured results contain a number of findings. In particular, the following may be noted.

(1) The transconductance g_m decreases with temperature, as expected. The mean square slope of g_m versus T is $-0.16\%/^\circ$C and $-0.25\%/^\circ$C for the two devices.

(2) The gate resistance R_g with temperature, as expected, is at a slope of $0.27\%/^\circ$C and $0.22\%/^\circ$C for the two devices.

(3) The change in input capacitance C_{gs} with temperature is $-0.12\%/^\circ$C and $-0.34\%/^\circ$C for the two devices. The decrease in capacitance with temperature could be due to decrease in sheet charge or charge confinement with temperature. It merits further investigation.

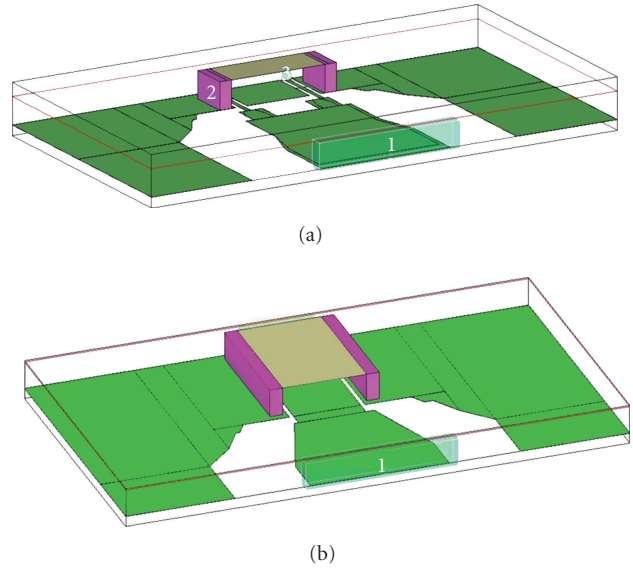

Figure 3: (a) Input feeding and (b) output feeding structure simulated with full wave analysis and used for de-embedding the S-parameters.

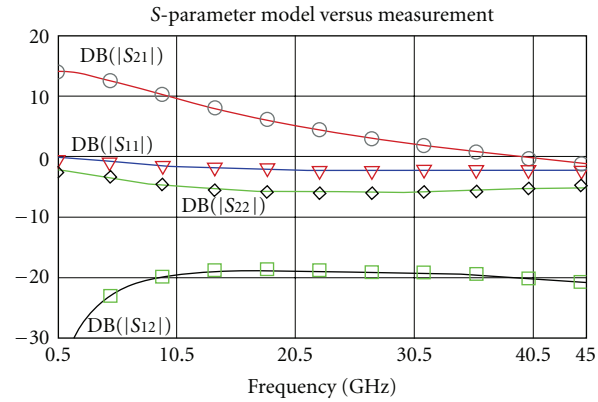

Figure 4: The model equivalent circuit versus the measured S-parameters at 25°C.

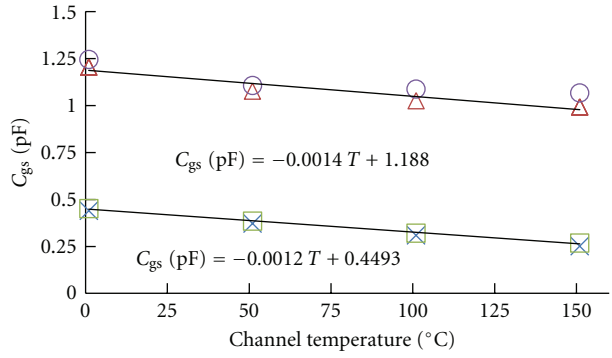

Figure 5: Variation of input capacitance (C_{gs}) with temperature.

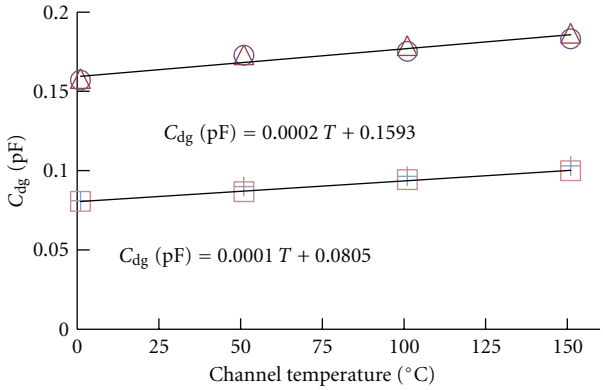

FIGURE 6: Variation of feedback capacitance (C_{dg}) with temperature.

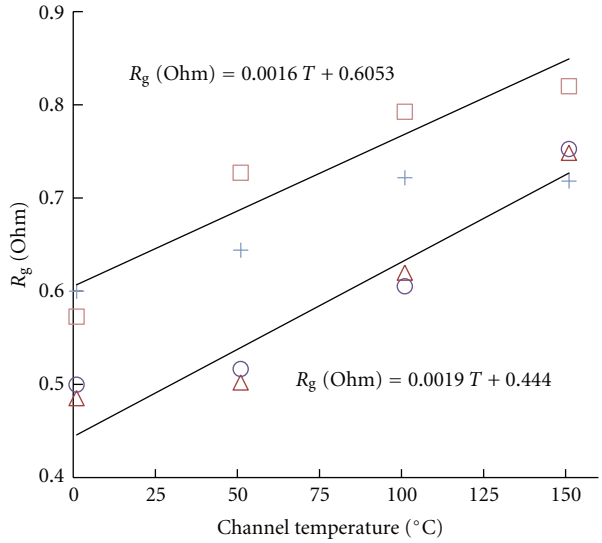

FIGURE 7: Variation of gate resistance (R_g) with temperature.

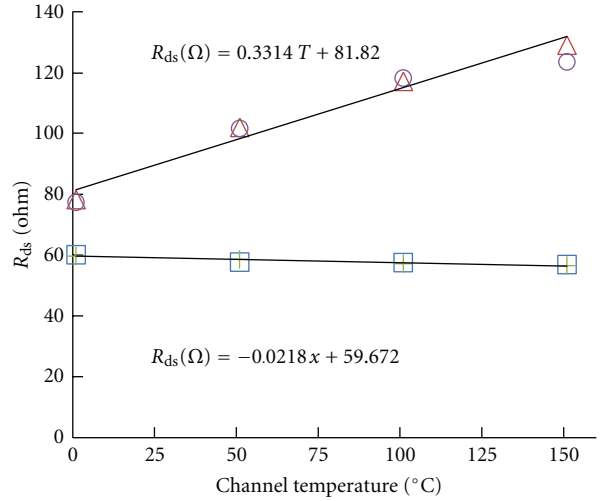

FIGURE 8: Variation of output resistance (R_{ds}) with temperature.

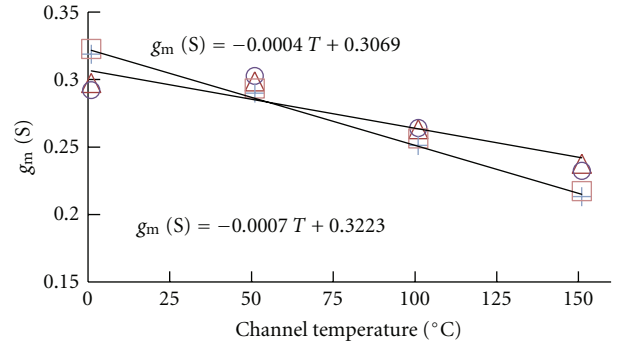

FIGURE 9: Variation of transconductance (g_m) with temperature.

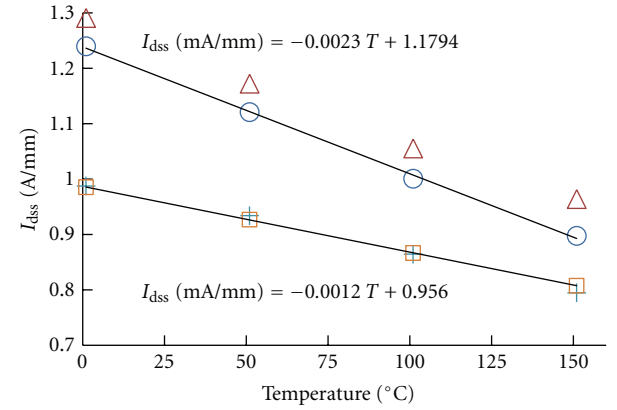

FIGURE 10: Saturated current (I_{dss}) versus temperature.

(4) The change in feedback capacitance C_{dg} with temperature is 0.11%/°C and 0.14%/°C for the two devices. An increase in C_{dg} is generally detrimental to achieving high performance as it decreases gain and efficiency. Reduced charge confinement is expected to increase the feedback capacitance, which may indicate a link between the feedback capacitance C_{dg} increase and the input capacitance C_{gs} decrease. Further studies are required.

(5) The output resistance R_{ds} is a very critical parameter as it directly influences power added efficiency, and output power. A small R_{ds} results in more RF power dissipation inside the transistor. Hence, the increase in R_{ds} with temperature should reduce the decline of efficiency and P_{out} with temperature. It increases with T at 0.3%/°C and almost 0%/°C for the two devices.

(6) In each case, a linear fit (using least square error) is shown. This should prove valuable in device modeling as most models (Angelov, EEHEMT, Curtice, etc.) allow temperature coefficients of various components and there is a general lack of experimental values.

4. Conclusion

From the preceding measurements, one may conclude that GaN HEMT devices experience higher parasitic, greater feedback capacitance, and lower gains with temperature. However, the degradation observed is less than (or equal to) GaAs degradation with temperature. Additionally, if the input matching network (which compensates for C_{gs}) and the output matching network (which compensates for C_{ds} and C_{dg}) can tolerate 10–15% variation in the reactance value, then they will work over 100°C range.

References

[1] Y.-F. Wu, A. Saxler, M. Moore et al., "30-W/mm GaN HEMTs by field plate optimization," *IEEE Electron Device Letters*, vol. 25, no. 3, pp. 117–119, 2004.

[2] Y. Pei, R. Chu, N. A. Fichtenbaum et al., "Recessed slant gate AlGaN/GaN high electron mobility transistors with 20.9 W/mm at 10 GHz," *Japanese Journal of Applied Physics*, vol. 46, no. 45, pp. L1087–L1089, 2007.

[3] J. S. Moon, D. Wong, M. Hu et al., "55% PAE and high power Ka-band GaN HEMTs with linearized transconductance via n+ GaN source contact ledge," *IEEE Electron Device Letters*, vol. 29, no. 8, pp. 834–837, 2008.

[4] A. Darwish, A. Bayba, and H. A. Hung, "Thermal resistance calculation of AlGaN-GaN devices," *IEEE Transactions on Microwave Theory and Techniques*, vol. 52, no. 11, pp. 2611–2620, 2004.

[5] A. M. Darwish, A. Bayba, and H. A. Hung, "FET gate length impact on reliability," in *Proceedings of the IEEE MTT-S International Microwave Symposium, (IMS '07)*, pp. 311–314, Honolulu, Hawaii, USA, June 2007.

[6] T. Palacios, S. Rajan, A. Chakraborty et al., "Influence of the dynamic access resistance in the gm and f T linearity of AlGaN/GaN HEMTs," *IEEE Transactions on Electron Devices*, vol. 52, no. 10, pp. 2117–2122, 2005.

[7] D. W. DiSanto and C. R. Bolognesi, "At-bias extraction of access parasitic resistances in AlGaN/GaN HEMTs: impact on device linearity and channel electron velocity," *IEEE Transactions on Electron Devices*, vol. 53, no. 12, pp. 2914–2919, 2006.

[8] C. F. Campbell and S. A. Brown, "An analytic method to determine GaAs FET parasitic inductances and drain resistance under active bias conditions," *IEEE Transactions on Microwave Theory and Techniques*, vol. 49, no. 7, pp. 1241–1247, 2001.

[9] C. L. Lou, W. K. Chim, D. S. H. Chan, and Y. Pan, "A novel single-device DC method for extraction of the effective mobility and source-drain resistances of fresh and hot-carrier degraded drain-engineered MOSFET's," *IEEE Transactions on Electron Devices*, vol. 45, no. 6, pp. 1317–1323, 1998.

[10] S. Manohar, A. Pham, and N. Evers, "Direct determination of the bias-dependent series parasitic elements in SiC MESFETs," *IEEE Transactions on Microwave Theory and Techniques*, vol. 51, no. 2 I, pp. 597–600, 2003.

[11] M. Thorsell, K. Andersson, M. Fagerlind, M. Südow, P. A. Nilsson, and N. Rorsman, "Thermal study of the high-frequency noise in GaN HEMTs," *IEEE Transactions on Microwave Theory and Techniques*, vol. 57, no. 1, Article ID 4717215, pp. 19–26, 2009.