

# 11.72-cm<sup>2</sup> Active-area Wafer Interconnected PiN Diode pulsed at 64 kA dissipates 382 J and exhibits an action of 1.7 MA<sup>2</sup>-s

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**Abstract**— SiC device area is presently limited by material and processing defects. To meet the large current handling requirements of modern power conditioning systems, paralleling of a large number of devices is required. This can increase cost and complexity through dicing, soldering, inclusion of ballast resistors, and forming multiple wire bonds. Furthermore, paralleling numerous discrete devices increases package volume/weight and reduces power density. To overcome these complexities, PiN diodes were designed, fabricated at 83% yield, tested, and interconnected on a three-inch 4H-SiC wafer to form an 11.72-cm<sup>2</sup> active-area full wafer diode. The full wafer diode exhibited a breakdown voltage of 1790 V at an extremely low leakage current density of less than 0.002 mA/cm<sup>2</sup>. At a pulsed current density of 5.5 kA/cm<sup>2</sup> and a rise time of di/dt = 1.1 kA/μs, the peak current through the wafer interconnected diode was 64.3 kA with a forward voltage drop of 10.3 V. The dissipated energy was 382 J and the calculated action exceeded 1.7 MA<sup>2</sup>-s. Preliminary efforts on high voltage diode interconnection have produced quarter wafer interconnected PiN diodes with breakdown voltages of 4 kV and 4.5 kV and active areas of and 3.1 cm<sup>2</sup> and 2.2 cm<sup>2</sup>, respectively.

**Index Terms**— 4H-SiC, PiN diode, wafer interconnection, full wafer diode, pulsed power, high voltage, action, di/dt

## I. INTRODUCTION

Although significant progress has been made in optimizing SiC material quality and fabrication, material and processing defects presently set an upper limit on SiC device

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area that can be fabricated at good yields. Micropipe defects, which render a device inoperable [1], have recently been eliminated with material growth improvements [2]. However, other material defects, including screw dislocations, are inevitably present in larger area SiC devices and can impact device performance and reliability [3, 4].

While a GTO thyristor of 1 cm<sup>2</sup> has recently been reported [5], high yielding SiC chip sizes are still limited to 0.1-0.5 cm<sup>2</sup> and high power applications necessitate a large number of discrete devices connected in parallel [6]. This can increase cost and complexity through wafer dicing, device soldering, and forming multiple wire bonds. The latter introduce stray inductance, while high-voltage operation dictates large “keep-out” distances between devices that increase package volume/weight and reduce power density. In addition, discrete device current sharing concerns typically necessitate ballast resistors which further increase package volume/weight and overall complexity.

To overcome the complexities associated with paralleling discrete devices, PiN diodes were fabricated on a three-inch SiC wafer at 83% yields and interconnected to form a full wafer PiN diode. The full wafer diode was packaged in a “hockey-puck” configuration and pulsed to 64 kA, dissipating 382 J with a calculated action exceeding 1.7 MA<sup>2</sup>-s.

## II. FULL WAFER INTERCONNECTION

To realize the high power potential of a SiC wafer, the active area of the wafer interconnected diode is maximized by optimally selecting the area of discrete PiN diodes. A smaller than optimal discrete diode area provides excellent wafer yield, however, a significant portion of the diode area is consumed by inactive regions such as edge termination. Conversely, a discrete diode area that is larger than optimal results in low wafer yield due to the inclusion of material and process defects. Thus, the optimal diode area must be carefully established. Based on defect distribution calculations [7], a discrete diode active area of 0.09 cm<sup>2</sup> (0.17 cm<sup>2</sup> total area) was chosen as optimal for maximizing wafer interconnected diode area. Subsequently, PiN diodes were designed and fabricated on three-inch 4H-SiC n<sup>+</sup> substrates with an epitaxial n- drift layer 20 μm in thickness that is doped to 5 x 10<sup>14</sup> cm<sup>-3</sup>. As bipolar devices, PiN diodes are better suited for +3.5 kV applications where thick drift epitaxial layers are utilized.

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14. ABSTRACT <b>SiC device area is presently limited by material and processing defects. To meet the large current handling requirements of modern power conditioning systems, paralleling of a large number of devices is required. This can increase cost and complexity through dicing, soldering, inclusion of ballast resistors, and forming multiple wire bonds. Furthermore, paralleling numerous discrete devices increases package volume/weight and reduces power density. To overcome these complexities, PiN diodes were designed, fabricated at 83% yield, tested, and interconnected on a three-inch 4H-SiC wafer to form an 11.72-cm<sup>2</sup> active-area full wafer diode. The full wafer diode exhibited a breakdown voltage of 1790 V at an extremely low leakage current density of less than 0.002 mA/cm<sup>2</sup>. At a pulsed current density of 5.5 kA/cm<sup>2</sup> and a rise time of di/dt = 1.1 kA/&amp;#956;s, the peak current through the wafer interconnected diode was 64.3 kA with a forward voltage drop of 10.3 V. The dissipated energy was 382 J and the calculated action exceeded 1.7 MA<sup>2</sup>-s. Preliminary efforts on high voltage diode interconnection have produced quarter wafer interconnected PiN diodes with breakdown voltages of 4 kV and 4.5 kV and active areas of and 3.1 cm<sup>2</sup> and 2.2 cm<sup>2</sup>, respectively.</b>			
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However, initial interconnection development targeted lower voltages to minimize material costs. A single-implant junction termination extension (JTE) in the periphery of each diode mesa provided edge termination. The diode anode and cathode regions were metallized with Ni, which was sintered at 900-1000°C to form nickel silicide ohmic contacts.

Following anode metallization, initial breakdown voltage measurements were performed. Diodes were selected for interconnection based on limits set for threshold voltage at a leakage current density of 0.2 mA/cm<sup>2</sup>. An overall breakdown voltage yield of 83% was achieved. The diodes selected demonstrated low leakage currents with sharp onset of breakdown voltage as illustrated in Fig. 1. Diodes with higher pre-breakdown leakage currents and softer breakdown knees were excluded due to defect related long term reliability concerns [4]. Also excluded were diodes located at the wafer edges due to the higher defect densities in these areas.

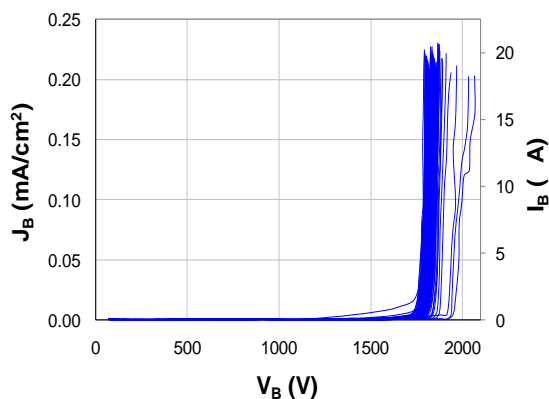


Fig. 1. PiN diodes selected for full wafer interconnection demonstrated low leakage currents and sharp onsets of voltage breakdown.

Full wafer diode interconnection was accomplished by first depositing a thick dielectric film designed to withstand high-voltage operation. Anode windows were subsequently reactive-ion etched to remove dielectric and expose diodes that qualified for interconnection (diodes passing breakdown voltage testing) as shown in the cross-sectional schematic in Fig. 2. Diodes that failed breakdown voltage testing were not interconnected and remain inactive under the dielectric. With a final metallization step, the anodes of the qualified diodes were interconnected to form a large area full wafer PiN diode [8].

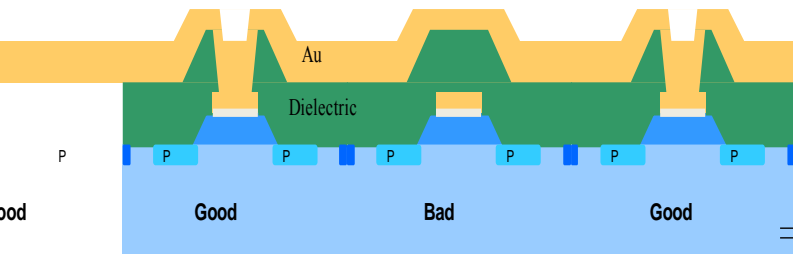


Fig. 2. Exemplary cross-sectional schematic of full wafer diode interconnection. Anodes of PiN diodes passing breakdown voltage testing were interconnected across the wafer. Diodes that failed breakdown voltage testing were not interconnected and remain inactive under the dielectric.

### III. RESULTS AND DISCUSSION

A wafer interconnected diode is shown in the inset of Fig. 3 (a). The diode has an active area of 11.72 cm<sup>2</sup> and consists of 135 discrete interconnected diodes. The interconnected wafer diode exhibited reverse voltage breakdown of 1790 V at an extremely low leakage current density of less than 0.002 mA/cm<sup>2</sup>, Fig. 3 (a), confirming successful full wafer interconnection. A schematic of a “hockey puck” package used in forward pulsed interconnected diode testing is shown in Fig. 3 (b). Once assembled, the package was potted and pressurized with SF<sub>6</sub> to 30 psi for high-voltage insulation. Centering rings are used to ensure even pressure. Voltage probe contacts extending radially through the package are used to measure voltage drops. This minimizes the package inductance contribution to the voltage measurements. The wafer’s center of mass is on the package axis to minimize

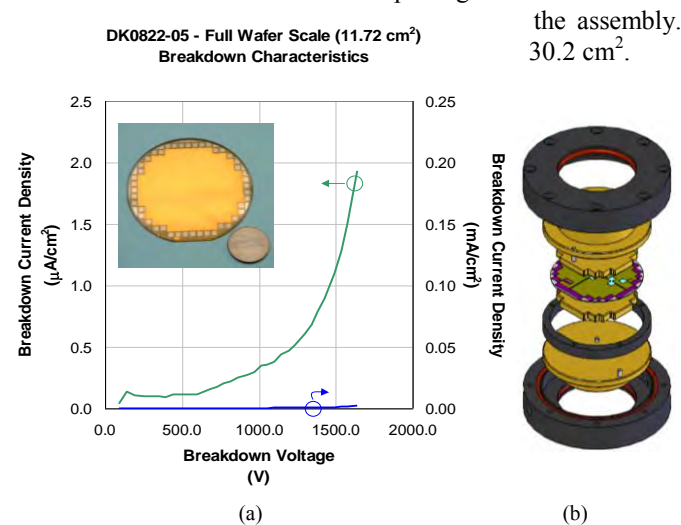


Fig. 3. (a) The fully interconnected wafer diode exhibited a breakdown voltage of 1790 V at an extremely low leakage current density of less than 0.002 mA/cm<sup>2</sup>. The inset is a photograph of the interconnected wafer diode. (b) Schematic of a “hockey puck” package for interconnected wafer testing.

The packaged wafer interconnected diode was subjected to high power pulsed testing. A 3.1 mF capacitor bank Pulsed-Forming-Network (PFN) was used for pulsing. The PFN is capable of producing a peak current of approximately 96 kA (~6 kA/kV of charge voltage) with a rise time of 33 μs for a 500 μs FWHM pulse width. It is switched by a light activated semiconductor switch for charge voltages below ~5 kV. Beyond 5 kV, triggering is achieved by releasing the pressurized gas in a spark gap pneumatic circuit [9]. When the PFN is switched, initial energy stored in the capacitor bank discharges through the wafer interconnected diode into a resistive load.

The wafer interconnected diode was subjected to fourteen high current pulses with PFN charge voltages ranging from 1 kV to 11 kV. The reverse leakage current was measured before and after each high current shot. Failure of the spark gap triggering mechanism terminated testing. At the end of the fourteenth shot, the leakage breakdown voltage density was 1.3 μA/cm<sup>2</sup> at the 1400 V measuring point. Under the 11 kV PFN charge pulse, the wafer interconnected diode conducted a peak current of 64.3 kA with an on-state voltage drop of 10.3

V (at  $di/dt = 0$ ) as shown in Fig. 4. This corresponds to a peak current density of  $5.5 \text{ kA/cm}^2$  and a diode on-state resistance of  $0.13 \text{ m}\Omega$ . The current rise time was  $di/dt = 1.1 \text{ kA}/\mu\text{s}$  and the FWHM pulse width was  $470 \mu\text{s}$ . The accumulated energy dissipated by the wafer interconnected diode during the  $11 \text{ kV}$  switching transient was  $382 \text{ J}$ . The calculated action (surge current integral), a key reliability parameter, exceeded  $1.7 \text{ MA}^2\text{-s}$ . Neglecting thermal diffusion during the short  $470 \mu\text{s}$  pulse duration, the temperature of the wafer interconnected diode rose by  $296 \text{ }^\circ\text{C}$ .

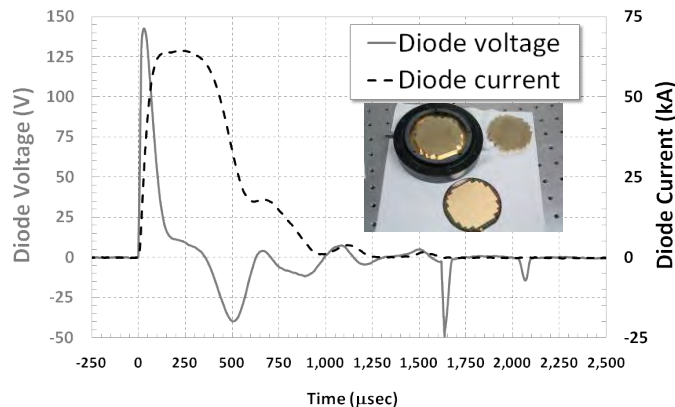


Fig. 4. The  $1790 \text{ V}$  interconnected PiN diode was pulsed at a peak current of  $64.3 \text{ kA}$  ( $5.5 \text{ kA/cm}^2$ ) with an on-state voltage drop of  $10.3 \text{ V}$ . The current rise time was  $di/dt = 1.1 \text{ kA}/\mu\text{s}$ . The energy dissipated by the interconnected diode was  $382 \text{ J}$  with a calculated action exceeding  $1.7 \text{ MA}^2\text{-s}$ .

Having successfully demonstrated a  $1.8 \text{ kV}$  wafer interconnected diode, work on higher voltage interconnection was initiated. To withstand higher voltages, thicker dielectrics were deposited, which increased interconnection complexity. Twenty-four discrete PiN diodes were interconnected to form a  $2.2 \text{ cm}^2$  active-area quarter-wafer interconnected diode, which exhibited a breakdown voltage of  $4.5 \text{ kV}$  at a leakage current density of  $0.03 \text{ mA/cm}^2$ , Fig. 5. In addition, thirty-six discrete PiN diodes were interconnected to form a  $3.1 \text{ cm}^2$  active-area quarter-wafer interconnected diode with a breakdown voltage of  $4 \text{ kV}$  at  $0.05 \text{ mA/cm}^2$ . On-state current interconnection

FA0840-05 - Top Interconnected WaSMI Diode  
(24 Interconnected Diodes,  $2.08 \text{ cm}^2$ )

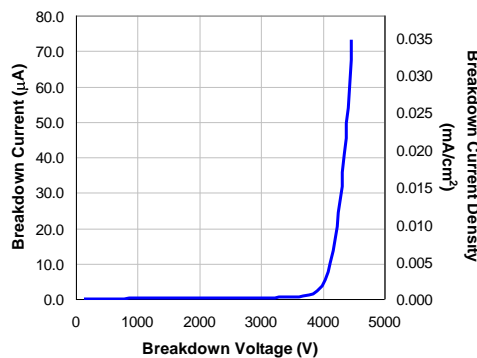


Fig. 5. The quarter wafer interconnected diode exhibited a breakdown voltage of  $4.5 \text{ kV}$  at an extremely low leakage current density of  $0.03 \text{ mA/cm}^2$ .

#### IV. CONCLUSION

PiN diodes were designed, fabricated at high yields, and interconnected on a three-inch 4H-SiC wafer to form an  $11.72 \text{ cm}^2$  active-area wafer interconnected diode. The wafer interconnected diode exhibited a breakdown voltage of  $1790 \text{ V}$  at an extremely low leakage current density of less than  $0.002 \text{ mA/cm}^2$ . The wafer interconnected diode was mounted in a “hockey puck” package and subjected to high power pulsed testing. It conducted a peak current of  $64.3 \text{ kA}$ , which corresponds to a peak current density of  $5.5 \text{ kA/cm}^2$ . The accumulated energy dissipated by the wafer interconnected diode was  $382 \text{ J}$  and the calculated action exceeded  $1.7 \text{ MA}^2\text{-s}$ . Discrete PiN diodes were interconnected to form quarter wafer diodes with breakdown voltages of  $4 \text{ kV}$  and  $4.5 \text{ kV}$ . High-voltage full wafer diode interconnection will be the focus of future work.

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