Compound Semiconductors for Low-Power *p*-Channel Field-Effect Transistors

Brian R. Bennett, Mario G. Ancona, and J. Brad Boos

Abstract

Research in *n*-channel field-effect transistors based upon III–V compound semiconductors has been very productive over the last 30 years, with successful applications in a variety of high-speed analog circuits. For digital applications, complementary circuits are desirable to minimize static power consumption. Hence, *p*-channel transistors are also needed. Unfortunately, hole mobilities are generally much lower than electron mobilities for III–V compounds. This article reviews the recent work to enhance hole mobilities in antimonide-based quantum wells. Epitaxial heterostructures have been grown with the channel material in 1–2% compressive strain. The strain modifies the valence band structure, resulting in hole mobilities as high as 1500 cm^2/Vs. The next steps toward an ultra-low-power complementary metal oxide semiconductor technology will include development of a compatible insulator technology and integration of *n*- and *p*-channel transistors.

Introduction

While silicon has long dominated electronics, compound semiconductors that are formed from combinations of Group III and Group V elements (e.g., GaAs) have nevertheless remained of interest because their higher electron mobilities and velocities allow for faster devices of a given size and power. Over the last three decades, the advantages of III–V semiconductor field-effect transistors (FETs) have been exploited in a variety of high-performance, front-end analog applications (e.g., radar systems, cell phones). For digital applications, however, high-performance III–V FET technology analogous to Si complementary metal oxide semiconductor (CMOS) has been difficult to achieve due to the lack of a suitable insulator, higher levels of defects, and the fact that the hole mobilities are generally much lower than the electron mobilities. In this article, we review recent efforts aimed at raising the mobility of holes in III–V materials in the hopes of making a III–V CMOS technology viable.

Because III–V semiconductors lack a good insulator, the standard approach for making III–V FETs has been different than for silicon FETs. Growth techniques such as molecular beam epitaxy (MBE) are used to create heterostructures in which the electron transport is restricted to a channel layer by cladding it with wider energy-gap barrier layers. The first such devices employed GaAs channels and AlGaAs barriers,[1] and in the years since, the primary method for enhancing performance has been simply to choose channel materials with better electron transport properties. The spectrum of possibilities open to such III–V heterostructure design is best revealed by the plot of the energy bandgap of various semiconductors versus their lattice constant shown in Figure 1. In general, the history of *n*-channel III–V transistors has progressed to the right in this diagram because the narrower bandgaps and smaller electron effective masses of those semiconductors offer higher speed and lower power. The initial GaAs/AlGaAs FETs were succeeded by structures having $In_{0.2}Ga_{0.8}As$ channels pseudomorphically strained to the GaAs lattice constant. Later, performance was further improved by increasing the In fraction in the channel, changing the barrier material to InAlAs, and accommodating the larger lattice constants by using InP substrates. In the last decade, several groups have reported additional progress with semiconductors (Figure 1)—namely InAs and InSb—whose smaller bandgaps and higher electron mobilities offer even further improved low-power performance. For example, low-noise amplifiers using InAs channels and antimonide barriers operating at frequencies of 10–100 GHz consume 3–10 times less power than comparable InP- or GaAs-based circuits.[2]

The extremely high electron mobilities of III–V semiconductors have naturally made them an attractive target for device researchers and have led to the history just recounted. The corresponding hole mobilities are much lower, as shown in Table I, and so the analogous *p*-channel devices show much poorer performance and have received far less attention. The earliest work was by groups at Bell Laboratories and IBM that in 1984 independently reported the first *p*-channel III–V FETs.[3,4] A subsequent investigation with GaAs channels and a gate length of 0.25 μm obtained a cutoff frequency (f_T), defined as the frequency at which the current gain of the transistor is unity, of 11 GHz and an estimated hole velocity of 1.7×10^6 cm/s.[5] Table I suggests that the strategy of moving to the right in Figure 1 that has been so effective in improving *n*-channel devices also should improve the performance for *p*-channel devices. Indeed, later *p*-channel work employed $In_xGa_{1-x}As$ channels, with either AlGaAs barriers and GaAs substrates for $x < 0.25$ or InAlAs barriers and InP substrates for $0.5 < x < 0.8$. For example, one study with strained AlGaAs/$In_{0.2}Ga_{0.8}As$ *p*-channel FETs fabricated using self-aligned Be ion implantation obtained maximum transconductances of 113 mS/mm and 175 mS/mm at room temperature and 77 K, respectively.[6] Similar devices fabricated using a self-aligned Mg implant yielded a maximum transconductance of 68 mS/mm at 300 K and an f_T of 11 GHz for a 0.3-μm gate length.[7] Another investigation involving an InGaP/$In_{0.15}Ga_{0.85}As$ *p*-channel FET

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14. ABSTRACT

Research in n-channel field-effect transistors based upon III?V compound semiconductors has been very productive over the last 30 years, with successful appli - cations in a variety of high-speed analog circuits. For digital applications, complementary circuits are desirable to minimize static power consumption. Hence, p-channel transistors are also needed. Unfortunately, hole mobilities are generally much lower than electron mobi - lities for III?V compounds. This article reviews the recent work to enhance hole mobilities in antimonide-based quantum wells. Epitaxial heterostructures have been grown with the channel material in 1?2% compressive strain. The strain modifies the valence band structure, resulting in hole mobilities as high as 1500 cm2/Vs. The next steps toward an ultra-low-power complementary metal oxide semiconductor technology will include deve - lopment of a compatible insulator technology and integration of n- and p-channel transistors.

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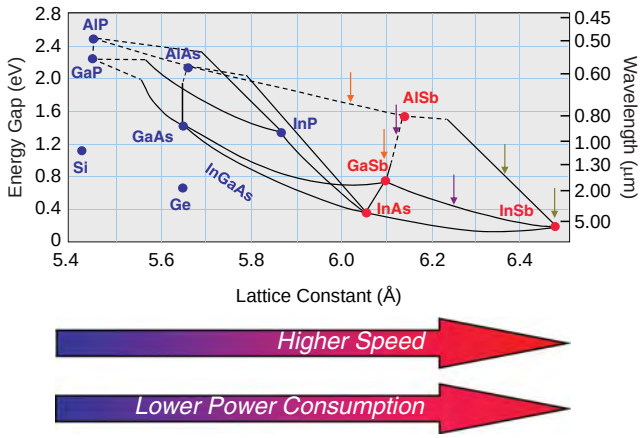

Figure 1. Energy gap versus lattice constant for selected semiconductors. The antimonide-based materials generally have the smallest energy gaps and the largest electron and hole mobilities and velocities, resulting in higher speed and lower power consumption. The arrows indicate the channel and barrier materials for antimonide-based quantum wells: orange, GaSb/AlAsSb; magenta, InGaSb/AlGaSb; and green, InSb/InAlSb.

with a 1-μm gate length demonstrated a transconductance of 63 mS/mm, a turn-on voltage greater than 2 V, a broad 4 V gate voltage swing, and an f_T of 3.1 GHz.[8] With respect to the InP-based material system, both lattice matched and strained $In_{0.52}Al_{0.48}As/In_xGa_{1-x}As$ *p*-channel FETs were investigated. A comparison between a dual channel design with low doping and a single channel design with high doping found that the latter exhibited the best direct-current and radio-frequency performance due to preferential low-effective-mass band occupation.[9] The role of strain was also investigated in $InP/In_xGa_{1-x}As/InP$ *p*-channel FETs for the range of $x = 0.64$ to 0.82.[10] In this study, FETs with an $x = 0.77$ channel composition and a 1.0-μm gate length exhibited a transconductance at 300 K of 19 mS/mm and an f_T of 2.9 GHz.

Almost all of the work done with GaAs and InGaAs channels obtained room-temperature hole mobilities of only 200–400 cm²/Vs (see Figure 2).[6,9–13] Only one more recent paper described an InGaAs alloy and an InGaP barrier with a hole mobility as high as 875 cm²/Vs.[8] For further progress, the recent *n*-channel work and information in Table I suggest moving further to the right in Figure 1 and using GaSb, InSb, or their alloys ($In_xGa_{1-x}Sb$). Although early work in this direction with GaSb channels and AlGaSb barriers achieved room-temperature hole mobilities of only 180–270 cm²/Vs,[14,15] the last two years have seen important progress (see Figure 2) by our group at the Naval Research Laboratory (NRL)[16–18] and by a collaboration between Intel and QinetiQ Corporations.[19] These recent advances with the Sb-containing III–V-s form the main focus of this review. Our coverage begins in the next section with a discussion of the various strategies being used to enhance the hole mobility. The following three sections then detail the progress that has been made with GaSb-, InGaSb-, and InSb-channel heterostructures, respectively. In the final section, we discuss the remaining challenges and outlook for *p*-channel III–V FETs.

Table I: Electron and Hole Mobilities of Selected Semiconductors.

Semiconductor	Electron Mobility at 300 K (cm²/Vs)	Hole Mobility at 300 K (cm²/Vs)
GaN	400	10
SiC	400	50
GaP	110	75
InP	4600	150
GaAs	8000	400
InAs	33000	460
Si	1450	500
GaSb	5000	850
InSb	80000	1250
Ge	3900	1900

Strategies for Enhancing Hole Mobility

Besides the basic choice of the channel material itself, it is well-known that the design of the III–V heterostructure affords many opportunities for improving the performance of both *n*-channel and *p*-channel FETs. Most important is the need to choose a compatible barrier material (if it exists) with a large enough band offset to confine the electrons or holes and to keep the gate leakage current low. Beyond this, the heterostructure design can enhance mobility in at least three different ways. First is modulation doping in which one situates the dopant atoms in the cladding layers

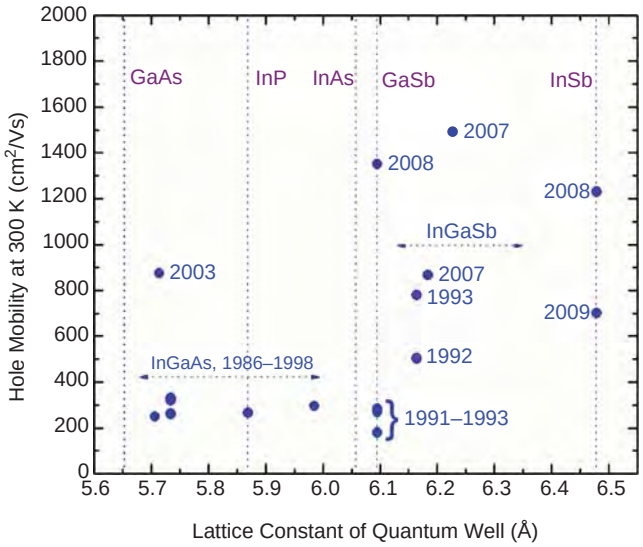

Figure 2. Room-temperature hole mobility versus lattice constant for quantum wells formed by III–V compound semiconductors. Note that the quantum well strain and sheet carrier density vary considerably among the samples. Data are from the following references: InGaAs,[6,8–13] GaSb,[14–16] InGaSb,[17,23] and InSb.[19,26]

rather than in the channel, thereby minimizing the scattering effect of the ionized impurities.[1] FETs that utilize this common technique are referred to as modulation-doped field-effect transistors (MODFETs) or high-electron-mobility transistors (HEMTs). A second way that the heterostructure design can benefit mobility is by making the transport layer very narrow (on the order of 10 nm) so that the quantum mechanics of the confinement strongly perturbs the band structure and can thereby enhance transport properties by reducing either the average effective electron mass (and so raising their velocity) and/or the scattering (by decreasing the number of available final states). The third benefit of a heterostructure design is that, through proper choice of the channel and barrier materials, it is possible to introduce large biaxial strains of as much as 1–2% into the channel layer, and these strains modify the band structure and can benefit transport. All of these methods presume that one is able to grow the requisite heterostructures with minimal defects, interface roughness, or other irregularities that would degrade mobility.

In contrast to the conduction bands, the valence bands of III–V semiconductors are very much like those of the Group IV semiconductors (Si, Ge, and the SiGe alloys). In particular, they consist of a so-called heavy-hole (HH) band, a light-hole (LH) band, and a split-off band. In the III–Vs, the split-off band is generally shifted far enough away in energy that it can be ignored. In bulk material, the HH and LH bands are degenerate, meaning that their energy maxima are equal, and so both bands will be significantly occupied. In a *p*-channel FET with the usual crystal orientation, epilayer growth on a (001) surface, the channel layer is oriented so that the band names correspond to the masses (heavy and light) in the channel width direction, while the masses in the in-plane direction are reversed (i.e., the HH band has a light in-plane mass). These differences mean that the quantum confinement imposed by the narrow channel will split the degenerate HH and LH bands, with the HH band being at higher energy. Hence, at low densities, only the HH band will be occupied (by holes), and this increases the hole mobility because the in-plane mass of the HH band is smaller. As a result, the hole velocity will be higher, and the scattering will be reduced because of a lower density of final states. As the hole density increases, the LH band also will become occupied, and the mobility benefit will be reduced. Making the channel narrower strengthens the confinement, increases the splitting, and raises the mobility further. At a certain point, however, forcing the holes into more intimate contact with the interfaces becomes counterproductive due to increased interface scattering.

Strain in the channel layer also can have mobility benefits. A common way of introducing strain into the channel is by growing heterostructures with an intentional mismatch in lattice constant between the channel and barrier materials. These strains, which are biaxial in nature, cause relative shifts of the HH and LH valence bands, and in this way act just like confinement to influence the hole mobility. It turns out that compressive strain in the channel (induced when the lattice constant in the channel is larger than in the barrier) is preferred because its band shifts *add* to those of confinement and so further augment the mobility. Conversely, tensile strains offset the confinement shifts and the attendant mobility benefits. The splittings associated with compressive strain are illustrated in Figure 3, where the results of electronic structure calculations (performed using the nextnano simulator[20]) are shown. The figure shows the highest energy LH1 (dotted lines) and HH1 (solid lines) bands for unstrained (bulk) GaSb and a 7.5-nm quantum well with 1% strain. As seen, compressive strain splits the HH and LH bands, with the HH band being higher in energy, hence having greater occupancy. Lastly, another ingenious use of strain that has been applied to SiGe FETs (but not yet to the III–Vs) is to introduce uniaxial strains by appropriate fabrication steps and, through the induced warping of valence bands, obtain even further increases in the mobility.[21]

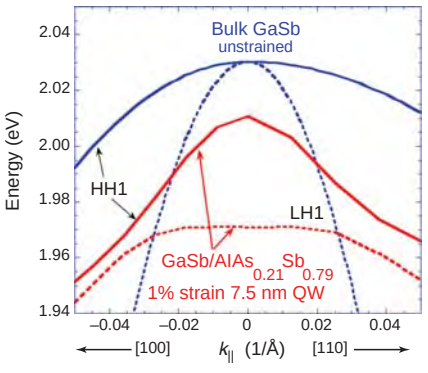

Figure 3. Calculated dispersion curves for strained GaSb quantum well (QW) and unstrained GaSb.[22] HH1, highest energy heavy-hole band; LH1; highest energy light-hold band; $k_{||}$, wave number.

GaSb *p*-Channel FETs

In work at NRL, the transport properties of GaSb quantum wells with varying strain, well thickness, buffer layer thickness, growth temperature, and doping were investigated.[16] A typical cross section of the MBE-grown FET layer structure is shown in Figure 4a.[22] Alloys of $AlAs_xSb_{1-x}$ were chosen as the buffer and barrier layers because they have a significant valence band offset (~0.6 eV) with respect to GaSb, allowing for good confinement of the holes, as shown by the energy band diagram in Figure 4b. The alloy composition of the $AlAs_xSb_{1-x}$ can be varied, resulting in different levels of strain in the GaSb channel. The buffer layers are almost fully relaxed and accommodate the ~7% lattice mismatch with the semi-insulating GaAs substrates. The doping is located below the channel to allow smaller gate-to-channel separations and better aspect ratios.

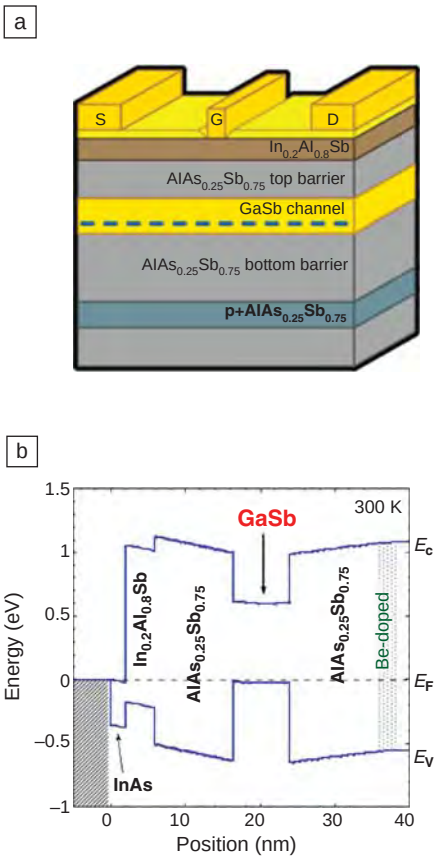

Figure 4. (a) Heterostructure cross section, GaAs substrate and AlAsSb buffer layer not shown and (b) energy band diagram for *p*-channel field-effect transistor with a strained GaSb channel.[22] S, source; G, gate; D, drain; E_C, conduction band energy; E_F, Fermi energy level; E_V, valence band energy.

The heterostructures were characterized using high-resolution x-ray diffraction. Figure 5 shows the x-ray scan for a sample that has the nominal structure shown in Figure 4 with an AlAsSb buffer thickness of 1.0 μm and a GaSb thickness of 10 nm. The buffer layer consisted of 666 periods of (3.9 sec AlSb/1.1 sec AlAs). Peaks are visible for the GaAs substrate, the 100-nm AlSb buffer layer, and the digital superlattice (n = –1, 0, and +1 satellites, where n is the order of the superlattice diffraction peaks). The expected result based on dynamical diffraction theory assuming superlattices with 1.083-nm AlSb and 0.337-nm AlAs is also shown. The measured epilayer peaks were all broadened, compared to the simulation, as a result of a high density of misfit dislocations required to relax the lattice mismatch. Using the superlattice layer thicknesses and Vegard's law (a linear interpolation of lattice constants from the binary endpoints), the effective ternary composition was calculated to be $AlAs_{0.238}Sb_{0.762}$, corresponding to a compressive biaxial strain in the GaSb of 1.21%.[16]

Most of the parameters that were varied did not have a major impact on mobility over the range investigated. The parameter that had the largest impact was quantum well strain. In Figure 6, the room-temperature Hall mobility is plotted as a function of quantum well strain for samples with quantum well thicknesses varying from 7.5 to 12.5 nm. The upper axis shows the AlAs mole fraction in the buffer layer. Most of this work focused on samples with compressive strain in the GaSb quantum well. As expected (see previous section), there is a strain-induced enhancement of mobility, with 11 samples exceeding 1000 cm²/Vs.

A GaSb-channel pFET with a 0.3-μm gate length was fabricated using material with a Hall mobility of 780 cm²/Vs and a hole sheet density of 2.6×10^{12} cm^{-2}. A maximum transconductance of 80 mS/mm is observed at a gate-source voltage V_{GS} = 0.4 V. A maximum cutoff frequency, f_T, of 6 GHz and a maximum oscillation frequency, f_{max}, of 18 GHz were obtained.[22]

InGaSb *p*-Channel FETs

As shown in Figure 1, if In is added to GaSb to create alloys of $In_xGa_{1-x}Sb$, the energy gap decreases. This could lead to FETs with lower power consumption. In addition, bulk InSb has a hole mobility of 1250 cm²/Vs, the highest of any III–V compound (see Table I). For these reasons, quantum wells of $In_xGa_{1-x}Sb$ have been investigated. The barrier material was AlGaSb. By changing the composition of the $In_xGa_{1-x}Sb$, one can modify the compressive strain in the quantum well. Cyclotron resonance measurements on samples with $In_{0.23}Ga_{0.77}Sb$ and $In_{0.41}Ga_{0.59}Sb$ quantum wells showed the hole effective mass (m_0) was reduced to approximately $0.10m_0$, approaching the values for *electrons* in InP and GaAs.[17] For comparison, the hole effective mass of bulk (unstrained) GaSb or InSb is $0.40m_0$. Figure 7 plots room-temperature hole mobilities as a function of channel composition for 12.5 nm quantum wells (circles).[17,23] Increasing strain (and confinement) also should reduce the effective mass and enhance the mobility. A peak in mobility occurred near 1000 cm²/Vs for x ~ 0.36–0.41. For larger x, the mobility dropped, which is consistent with x-ray results that showed lattice relaxation.

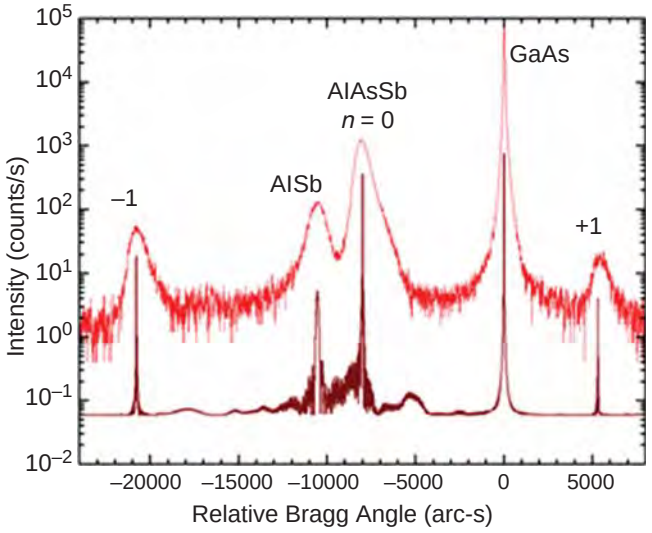

Figure 5. Double crystal x-ray diffraction data for GaSb/AlAsSb quantum well (upper curve) and simulation (lower curve); n is the order of the superlattice diffraction peaks.[16] These results allow the determination of strain in the GaSb quantum well.

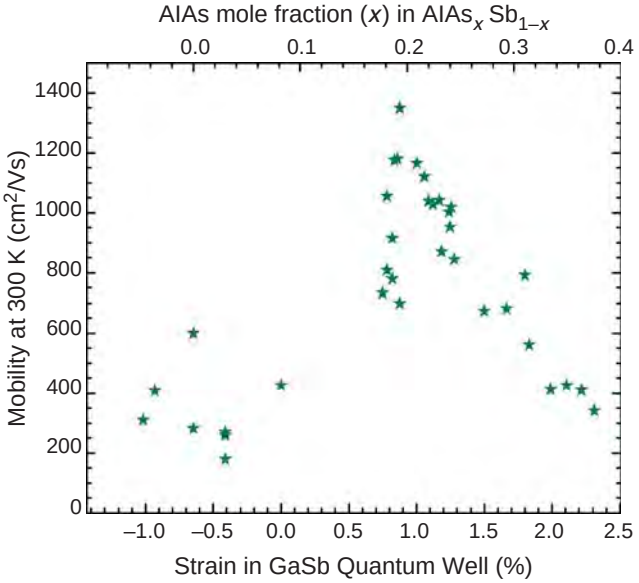

Figure 6. Room-temperature hole mobility versus strain (or buffer layer composition) for GaSb/AlAsSb quantum wells. Quantum well thicknesses were between 7.5 and 12.5 nm.[14–16]

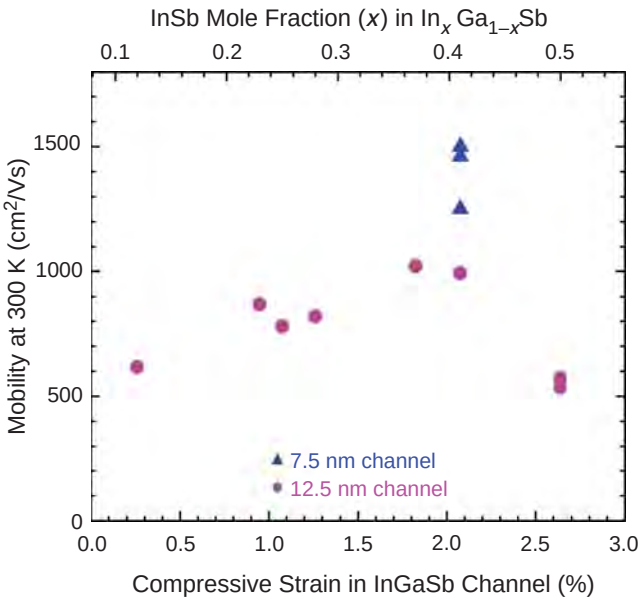

Figure 7. Room-temperature hole mobility versus strain (or channel composition) for InGaSb/AlGaSb quantum wells.[17,23] With the appropriate quantum well strain and thickness, mobilities can reach 1500 cm^2/Vs.

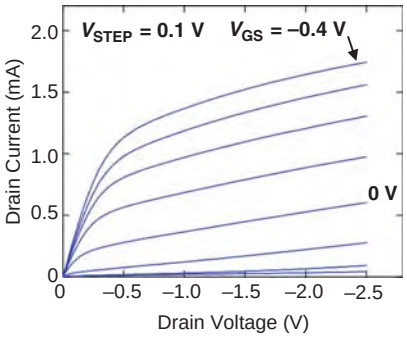

Figure 8. InGaSb-channel *p*-field-effect transistor drain characteristics.[18] The device had a 0.25-µm gate length, 1.0-µm source-to-drain spacing, and a 28-µm gate width. Each curve represents a different gate-source voltage (V_{GS}), with a 0.1 V/step increment (V_{STEP}). These results demonstrate well-behaved transistor performance.

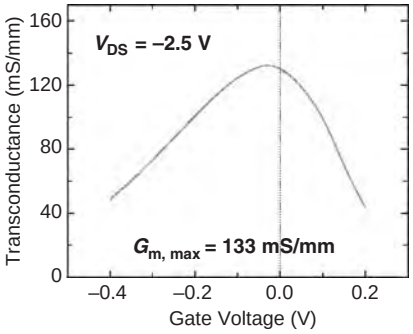

Figure 9. InGaSb-channel *p*-field-effect transistor transconductance versus gate voltage for a source drain voltage (V_{DS}) of –2.5 V.[18] $G_{m,max}$, maximum transconductance. These results demonstrate well-behaved transistor performance.

Investigations on an $In_{0.40}Ga_{0.60}Sb$ alloy gave further insights. By decreasing the quantum well thickness to 7.5 nm and modifying the growth procedures, room-temperature mobilities as high as 1500 cm^2/Vs were reached (triangles in Figure 7).[17]

The fabrication and characterization of InGaSb-channel pFETs[18,24] as well as the low-frequency noise characteristics of the devices[25] were recently reported. The drain characteristics obtained for a pFET with a 0.25-µm gate length are shown in Figure 8.[18] The dependence of the transconductance on the gate voltage is shown in Figure 9. At a drain-source voltage V_{DS} = –2.5 V, a maximum transconductance of 133 mS/mm is observed at V_{GS} = –0.05 V. An f_T of 15 GHz and an f_{max} of 27 GHz were measured. Devices on a similar heterostructure with a 0.2-µm gate length yielded values of 19 and 34 GHz, respectively.[24] Further improvements in high-speed, low-voltage performance should be possible with a decrease in gate length and a reduction of the contact and access resistances.

InSb *p*-Channel FETs

The final Sb-containing III–V *p*-channel FET to be discussed is that with InSb channels. Figure 1 and Table I suggest that such a device could have very attractive properties, although the narrowness of the bandgap (0.17 eV) and the lower band offset (0.3 eV) could present problems. The first work on InSb *p*-channel quantum wells and FETs was recently reported. Edirisooriva et al. achieved mobilities of 700 cm^2/Vs at 300 K and 55,600 cm^2/Vs at 77 K.[26,27] A joint effort between QinetiQ and Intel fabricated the first InSb-channel pFETs.[19] The devices were grown by MBE on a GaAs substrate, with a thick InAlSb buffer layer and a 5-nm InSb channel (1.9% compressive strain). A cross section is shown in Figure 10. The hole mobility at room temperature was as high as 1230 cm^2/Vs (see Figure 2). Figure 11 shows f_T as a function of direct-current power dissipation with a peak of 140 GHz for a FET with a gate length of 40 nm. Compared to Si, the InSb device exhibits an order of magnitude lower power at the same speed or a factor of two higher speeds at matched power. The peak transconductance for this device was 510 mS/mm. The estimated effective hole velocity was as high as 7×10^6 cm/s, a factor of four improvement over GaAs. These results provide additional evidence that strained antimonide channels are viable candidates for pFETs.

Conclusions and Outlook

The three antimonide-based *p*-channel field-effect transistor (FET) technologies surveyed in this article utilize mechanical strain and quantum confinement in appropriate heterostructures in order to achieve higher hole mobilities. Interestingly, at present, all three yield similar levels of

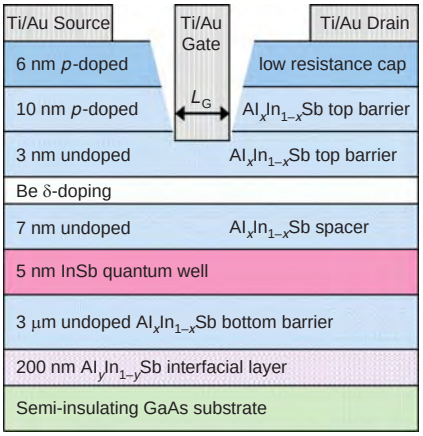

Figure 10. Schematic of InSb *p*-channel field-effect transistor structure on GaAs.[19] L_g, gate length.

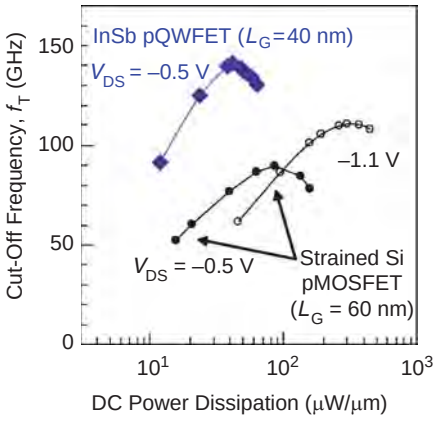

Figure 11. Cut-off frequency, f_T, as a function of direct-current (DC) power dissipation for a InSb-channel *p*-quantum well field-effect transistor (QWFET) with a 40-nm gate length (L_G) and drain-source voltage V_{DS} = –0.5 V. For comparison, data from a standard strained Si *p*-channel metal oxide semiconductor field-effect transistor (MOSFET) is included.[19] These results indicate that antimonide-based pFETs can operate at high frequency with very low power consumption.

enhancement with maximum hole mobilities approaching 1500 cm²/Vs. These values are competitive with those of the Si/SiGe alternatives,[28] especially given the added potential of the antimonides for low-voltage operation[29] as well as their superb electron transport properties. However, whether these promising results will lead to viable III–V complementary metal oxide semiconductor (CMOS) technology remains speculative and is contingent on important progress being made in a number of areas, as discussed briefly in this final section.

A first issue regarding progress is how much further the hole mobilities of the Sb-based III–V heterostructures can be enhanced. The main strategies would seem to be through improvements in crystal quality (e.g., via better buffer design) and additional exploitation of strain. With respect to strain, it is difficult to achieve strains higher than about 2% in two-dimensional epitaxial growth, and so it would seem that only GaSb has significant room for improvement in this area, since its best mobilities to date were achieved at strains of only about 1%. As mentioned earlier, one other possible route for progress in all systems is the SiGe strategy of introducing uniaxial strains to produce a favorable warping of the valence bands.[21]

Mobility is but one measure of device performance; the Sb-based pFETs also must be judged by a number of other criteria, including cutoff frequency, power dissipation, contact resistance, leakage currents, integration with oxides, integration with *n*-channel FETs, enhancement-mode capability, and scalability. Currently, the InSb pFETs exhibit the lowest contact/access resistance (probably due to the lower barrier presented by $In_{0.65}Al_{0.35}Sb$), and their transconductances are consequently about a factor of four higher than the best InGaSb pFETs. With respect to leakage current for a pFET design, GaSb would seem to be favored, as its valence band offset is largest (~0.6 eV as compared with ~0.45 eV for InGaSb and ~0.3 eV for InSb). However, this is not an overriding concern in that any future *p*-channel technology will likely incorporate a high-quality insulator in the gate stack. Integration with a compatible *n*-channel FET technology is also required. It is not essential that the same material be used for both the *n*- and *p*-channel, but it is desirable that the channels have similar lattice constants so that they can be grown in a single heterostructure. The *p*-channel antimonides discussed here could potentially be mated with *n*-channel InSb, InGaSb,[30] GaSb, InAs, or InAsSb. Also, *n*-channel technology based upon InGaAs channels and InAlAs[31,32] or InGaP[33] barriers is more advanced and might be used instead of antimonide-based nFETs. Composite InAs/InGaAs *n*-channel FETs are also under investigation for logic applications.[34]

Substantial research efforts on both *p*-channel and *n*-channel antimonide-based FETs continue in our group, in the Intel/QinetiQ collaboration, and elsewhere. The progress of these efforts in the areas outlined here will determine the future practicality of the antimonides for III–V CMOS devices and also will dictate which of the three antimonide-based technologies discussed herein will be favored. To impact mainstream ultra-scaled digital electronics in the coming decade, antimonides must also face the stiff competition presented by Si/SiGe, InGaAs, carbon nanotubes, and other more exotic possibilities.

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Women and MRS Prizes/Awards

A Letter from Julia Weertman, MRS Awards Committee Chair

The Materials Research Society sponsors a number of prestigious prizes, but very, very few have been awarded to women. Only once has a woman been honored with either the Von Hippel Award or Turnbull Lectureship, and the MRS Medal has never been awarded to a woman. While it is recognized that the pool of senior women materials researchers eligible for the Von Hippel and Turnbull is relatively small, that is not the case for awards that recognize outstanding contributions during the earlier stages of one's career.

It is estimated that 20% of materials researchers are women, a great many of whom have the qualifications to be nominated for MRS awards. If you know, or know of, a woman whose contributions to materials science/engineering merit competing for one of these honors, or for the new Innovation in Materials Characterization Award, consider nominating her. **Information about these awards, as well as for the MRS Fellow, is available on the inside back cover of this issue and on the MRS Web site, at www.mrs.org/awards.** Note that, with the exception of the MRS Fellow, membership is not a criterion for nomination for MRS awards.

By increasing the percentage of qualified women nominated for awards, we can make progress toward ensuring that women materials researchers are appropriately represented and recognized. Nomination is the essential first step toward honoring more women!

If you have any questions about the nomination process, please feel free to contact me at **jrweertman@northwestern.edu**.

Julia Weertman
Walter P. Murphy Professor Emerita, Northwestern University