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Anomalous Drain Voltage Dependence in Bias Temperature Instability Measurements on High-κ Field Effect Transistors

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ABSTRACT

We find that changes in threshold voltage induced by negative bias temperature stressing of p-channel field effect transistors with HfSiON gate dielectrics are modulated by the drain voltage, in measurements wherein the drain current is measured during stressing. This effect is not observed in SiO_2 gate devices. Short channel effects are excluded as explanations, leading us to conclude that positive charge in the dielectric stack is laterally mobile and is conducted out of the insulator via the drain. Further, a simple qualitative model of charging kinetics allows us to extract the density of interface states as a function of time, and shows that these defect densities of the order of 10^{11} cm^{-2} after hundreds of seconds. These values are consistent with observations on pure SiO_2 gate insulator devices.

1. Introduction

Accurate determination of the susceptibility of metal oxide semiconductor field effect transistors (MOSFETs) to degradation via the Negative Bias-Temperature Instability (NBTI) is of crucial importance for future generations of Si based devices, since this has been recognized as one of the critical reliability issues in advanced CMOS devices [1]. Complicating this task is the fact that there appears to be no established generic measurement protocol; indeed, they vary considerably from one research group to another, making cross-referencing of research results difficult. In our own recent investigations [2], to minimize errors resulting from trapped charge relaxation during the MOSFET characteristic acquisition sequence, we have adopted the practice of measuring changes in the drain current I_{ds} whilst maintaining a constant bias stress level V_{gs} on the gate electrode. The device threshold voltage shift ΔV_{th} under this NBTI stress can then be determined from the fractional current variation $\Delta I_{ds}/I_{ds}^{o}$ $\frac{\Delta I_{ds}}{I_{ds}^{o}}$ given certain approximations which we have discussed at some length [2].

Under usual conditions, I_{ds} can be determined in either the linear or saturation modes of operation [3] of the MOSFET. Following reference [3], I_{ds} can be approximated by

$$I_{ds} = (W/L)\mu_{eff}C_{ox}\left[(V_{gs} - V_{th})V_{ds} - \frac{1}{2}V_{ds}^2\right], \qquad I_{ds} = \left(\frac{W}{L}\right)\mu_{eff}C$$

where W and L are the device inversion channel width and length, μ_{eff} is the effective inversion channel carrier mobility, and C_{ox} the gate insulator capacitance. The drain-source voltage V_{ds} biases the device in the linear regime when $V_{ds} \gg (V_{gs} - V_{th})$ $|V_{gs} - V_{th}|$ and in the saturation regime when $|V_{ds} \leq (V_{gs} - V_{th})|V_{gs} - V_{th}|$. Assuming that some physical phenomenon (such as NBTI) induces a given ΔV_{th} and an associated ΔI_{ds}, then from Eq. (1) it is easy to show that

$$2\left(\frac{\Delta I_{ds}}{I_{ds}^{o}}\right)_{lin} = \left(\frac{\Delta I_{ds}}{I_{ds}^{o}}\right)_{sat}, \quad (2)$$

so that for a maximum measurable effect it is more sensible to measure in the saturation regime. However in practice, measurements are usually made in the linear regime where V_{ds} is small. Logic for the latter may be the possibility of non-uniform charge generation or trapping in the gate dielectric or at the Si/dielectric interface resulting from a non-uniform vertical (z direction) electric field $E_z(y)$, when V_{ds} is not small and so the semiconductor surface potential becomes a function of distance along the inversion channel (y direction).

In the work reported here we have performed NBTI measurements on SiO_2 and HfSiON gate dielectric p-channel MOSFETs while stressing in either the linear or saturation drain current regime. We have observed what appears to be an important measurement protocol issue, at least in the HfSiON devices we have studied: an unexpected dependence of the NBTI-induced threshold voltage shift on the drain voltage applied during stress. We argue that this is not due to lateral non-uniformities. That different V_{ds} could affect NBTI stress measurements is important to note both from the point of view of physical understanding of the effect and from the point of view of deriving predictive formulae for reliability lifetimes. Furthermore, based upon our observations of the effect of V_{ds}, we propose a simple qualitative model of charging kinetics that, while approximate, allows us to also extract the NBTI-induced interface state density as a function of time.

2. Experimental Procedure

The high-k samples used in this investigation were pMOSFETs in which the dielectric stack consisted of a nominal 1 nm of SiO_2 onto which was deposited 2 nm of HfSiO using atomic layer deposition. The stack was subsequently nitrided and the resultant atomic

composition estimated to be SiO_2 (70%), HfO_2 (30%) and N (15%) with respect to the concentration of starting HfSiO material. The effective dielectric constant for the stack was approximately 13. A detailed description of the gate dielectric manufacturing process is provided in reference [4]. Devices with gate lengths of 1.0 μm and 0.7 μm, both with 0.5 μm gate widths, were measured; the two gate length sets gave similar results. At least 20 HfSiON FETs were used in our studies to ensure reproducibility of the observed phenomena. Additionally, p-channel devices with 2.6 nm thick SiO_2 gate dielectric were fabricated on silicon-on-insulator substrates as described elsewhere [5]. The measured devices had typical channel lengths ~ 0.5 μm and widths ≤ 2 μm.

Drain current measurements were made using a Keithley 4200 SCS measurement system in "continuous" mode [2] at a gate voltage of -2 V, and an arbitrarily chosen temperature of 175 °C . Because the NBTI is generally observed to be smaller in pure SiO_2 gate dielectric devices, these were measured at 195 °C to enhance the effect. The drain voltage V_{ds} was varied over the range -0.1 V to -2.0 V, but was constant during measurement on a particular device. Source, substrate and body were grounded. In the continuous mode, the drain current $I_{ds}(t)$ was measured periodically (approximately every 0.75 s) without interrupting the stress. This nominally avoids the likelihood of trapped charge relaxation [6] which is commonly observed in experiments where the stressing voltage is removed in order to perform an I_{ds} versus V_{gs} measurement. From the drain current data, the threshold voltage shift $\Delta V_{th}(t)$ was extracted using the simple square law model (Eq. 1) , which yields

$$\Delta V_{th}(t) = \left(1 - \frac{I_{ds}}{I_{ds}^{o}}\right)\left(V_{gs} - V_{th}^{o} - \frac{V_{ds}}{2}\right) \qquad (3)$$

where V_{th}^{o} is the threshold voltage prior to NBTI stress (~ -0.5 V at 175 °C for the HfSiON devices and +1.3 V at 195 °C for the SiO_2 devices), I_{ds}^{o} is the drain current at t = 0, and V_{gs} and

V_{ds} are the gate and drain voltages. Eq. (3) holds provided $V_{ds} \gg (V_{gs} - V_{th})$ $|V_{gs} - V_{th}|V_{ds} > V_{gs} - V_{tho}$; for more negative V_{ds}, $(V_{gs} - V_{th})V_{gs} - V_{tho}$ must be substituted for V_{ds}. Note that for the measurements on the SiO_2 with large, positive V_{th}, $V_{ds} = V_{gs} = -2$ V does not strictly meet the saturation definition condition. However, we performed $I_{ds}(V_{ds})$ measurements for $V_{gs} = -2$ V and observed that the current was within 4% of the saturation value.

The protocol described here is designed to minimize charge loss during measurement. The largest uncertainty in these measurements is in determining the initial source-drain current (I_{ds}^{o}) since the system takes 1 - 2 seconds to generate the first data point. We estimate the uncertainty in I_{ds}^{o} to be of the order of 0.1%, causing errors of a few percent in the extracted ΔV_{th}. We also ignore any changes in mobility, which we have previously argued to be a reasonable approximation for these samples [2].

3. Results and Discussion

Normalized change in drain current $\frac{\Delta I_{ds}(t)^{o}}{I_{ds}\,\Delta I_{ds}(t)/I_{ds}^{o}}$ measured during stressing, and the resultant threshold voltage shifts, are shown for HfSiON gate devices in Fig. 1. All samples were stressed at 175 °C and $V_{gs} = -2.0$ V, and at varying V_{ds}. As indicated in Eq. (2), the square law model predicts that for a given ΔV_{th}, the normalized change in drain current $\Delta I_{ds}/ I_{ds}^{o}$ measured in the saturation region $V_{ds} < V_{gs} - V_{tho})$ should be twice as big as in the linear region ($V_{ds} \sim 0$). In any event, ΔV_{th} should not depend on V_{ds}. What we observe, however, is that in saturation ($V_{ds} < -1.5$ V) the change in drain current is in fact *much less* than in the linear

region (V_{ds} = -0.1 V). As a result, ΔV_{th} is found to be smaller by a factor of more than 4 when NBTI stress is performed in saturation as compared with the value estimated from the linear region data (Fig. 1b). Intermediate values of V_{ds} have a corresponding effect on ΔV_{th}.

We have also performed NBTI measurements at 195°C on p-channel MOSFETs constructed on silicon-on-insulator substrates. $I_{ds}(t)$ measurements were made with the source-drain voltage biased in the linear regime (-0.2 V) and in the saturation regime (- 2V). The results for $\Delta I_{ds}/I_{ds}^{o}$ are shown in Fig. 2a. and after conversion to $\Delta V_{th}(t)$, in Fig. 2b. As argued above, we observe that $\Delta I_{ds}/ I_{ds}^{o}$ in the saturation regime is ~ 2 x the variation in the linear regime. This result is in agreement with what is anticipated in a p-channel MOSFET but is in complete contrast with what we have observed for HfSiON gate devices. This conclusion for SiO_2 based devices is further supported in other published data [6,7].

3.1. Short channel effects

The first explanation of the drain voltage dependence of ΔV_{th} which comes to mind is a short-channel effect in which charge is created non-uniformly at higher drain voltages. If that were the case, one would expect to observe it in SiO_2 devices as well, but we do not. There are other reasons why non-uniform charging is not likely to explain the observations. We have performed measurements of I_{ds} as a function of V_{gs} in the sub-threshold regime for our devices. Sub-threshold current plots of our 1 μm devices measured with V_{ds} varying from -0.1 to -2.0 V show no measureable shift in V_{th}^{o}. This is in fact to be expected since the doping density in the devices was ~10^{18} cm^{-3} and the equivalent oxide thickness was approximately 2 nm. Thus the devices are very "long channel-like", so drain voltage effects are confined to a region very close

to the drain. Furthermore, we note that there is a sizeable change (Fig. 1b) in ΔV_{th} even for lower drain voltage (-0.1 V > V_{ds} > -1.0 V), i.e., well before saturation.

We can place the "long channel-like" argument on more sound physical footing using a quasi-two-dimensional model [8]. The model allows calculation of the surface potential along the channel in the Si substrate V_s while accounting for 2D effects present near the source/drain contacts in small devices. Specifically, we have [8]

$$\varepsilon_{Si}\frac{d_{max}}{\eta}\frac{dE_x(y)}{dy}+\varepsilon_{ox}\frac{V_{gs}-V_{FB}-V_s(y)}{t_{ox}}=qN_B d_{max} \quad (4)$$

The z- and y-directions here correspond to the vertical and lateral directions, so that $E_z(y)$ is the vertical oxide field, which is a function of distance along the channel. The dielectric permittivity in the silicon and in the oxide are ε_{Si} and ε_{ox}, V_{gs} and V_{FB} are the applied gate voltage and flatband voltage [3], N_B and t_{ox} are the substrate doping density and oxide thickness, d_{max} is the maximum depletion depth in the substrate due to the drain voltage (and is given by the depletion approximation), and η is a fitting parameter, which we set to 1. The solution for the surface potential, with boundary conditions $V_s(0) = V_{bi}$ and $V_s(L) = V_{ds} + V_{bi}$ is

$$V_s(y)=V_{sL}+(V_{bi}+V_{ds}-V_{sL})\frac{\sinh\left(\frac{y}{l}\right)}{\sinh\left(\frac{L}{l}\right)}+(V_{bi}-V_{sL})\frac{\sinh\left(\frac{L-y}{l}\right)}{\sinh\left(\frac{L}{l}\right)} \quad (5)$$

Here, $V_{sL}=V_{gs}-V_{tho}+\varphi_s V_{sL}=V_{gs}-V_{th}^{o}-2\varphi_B$ where V_{th}^{o} is the long-channel threshold voltage, φ_B is the Fermi potential in the silicon bulk, and V_{gs} and V_{bi} are the applied gate voltage and built-in potential. The length parameter l is given by $l=\sqrt{\frac{\varepsilon_{Si}t_{ox}d_{max}}{\varepsilon_{ox}\eta}}$. $l=\sqrt{\frac{\varepsilon_{Si}t_{ox}d_{max}}{\varepsilon_{ox}\eta}}$,

We have applied the model to the geometry of our devices, using V_{bi} = 1 V, V_{FB} = 0, and V_{th}^{o} = -0.5 V, the oxide permittivity appropriate to SiO_2 with an oxide thickness t_{ox} of 2 nm, and

semiconductor parameters at 175 °C. From the surface potential we have calculated the oxide field as a function of distance along the channel as $E_z(y) = \frac{V_{gs} - V_s(y)}{t_{ox}}$. A plot of $E_z(y)$ is shown in Fig. 3a for the case of V_{ds} = -0.1 V and -2 V. We observe that $E_z(y)$ is very uniform along the channel for both cases and that for the -2V case significant variation occurs only in the last 0.05 μm. Therefore, whether in the linear regime or the saturation regime, our devices should have experienced a uniform $E_z(y)$ profile over nearly the entire channel.

3.2. Non-uniform trapped charge generation

The previous estimates reveal that the vertical electric field is essentially uniform along the channel length in both linear and saturation cases. However, we cannot a priori reject the idea that the trapped charge generation mechanism itself in some way "amplifies" the non-uniformity of the electric field and thereby gives rise to substantially less charge in one case as opposed to the other. Various authors have endeavored to estimate the vertical electric field dependence of the NBTI charge generation rate $G(E_z)$ resulting from the NBTI phenomenon. We arbitrarily chose one which has the form [9] $G(E_z) \sim E_z e^{\gamma E_z}$ where γ has a value of 0.6. We show in Fig. 3b a plot of the generation rate as a function of distance along the device channel assuming the $E_z(y)$ variation also shown in Fig. 3a – the calculation assumed V_{ds} = - 2V. The generation rate of trapped charge due to NBTI is again found to be relatively uniform along the channel. We are therefore led to conclude that short channel effects in general, and non-uniform charging in particular, cannot give rise to a level of trapped charge generation substantially different from that one would anticipate if $E_z(y)$ were entirely uniform as in the case of linear regime device operation (low V_{ds}).

3.3. An alternative explanation

To recap the situation, we have performed NBTI measurements on devices operated in the linear and saturation regimes. Surprisingly, the experimental data on high-k based devices gives evidence that charge trapping is substantially larger in the former operational mode than in the latter. Having eliminated short channel and non-uniform charging effects, we look for an explanation in the nature of the dielectric itself. Noting that high-κ dielectrics tend to trap charge more readily than SiO_2, we postulate the following: NBTI induces a high density of positive charge in the dielectric near the interface with the Si substrate, perhaps in the thin "SiO_2" layer itself below the HfSiON, or at the interface between the SiO_2 and high-κ layer. We further stipulate that the positive charge in that region is highly mobile in the lateral sense. This hypothesis is not inconsistent with lateral charge redistribution effects observed in other dielectric system such as in the SONOS memory cell [10, 11]. The mobile charge may be due to holes, or perhaps protons; we will assume here that the charge is due to holes. We suggest that the drain voltage produces a lateral field in both the semiconductor and in the dielectric layers that removes the holes by conducting them out via the drain, thus reducing the hole population in the dielectric stack by an amount that increases with increasing V_{ds}. Because the drain voltage is not "felt" far from the drain, the mechanism must involve removal of holes near the drain, followed by transport of holes toward the drain from farther inside the channel, much as charge is conducted out of the drain from the Si inversion layer during normal device operation.

3.4. Estimation of the magnitude of different contributions to ΔV_{th}

The simplest approximation to model the NBTI induced charging is to assume two distinct "species", interface states and charges trapped in the gate dielectric [8]. With this assumption we propose a simple qualitative model of NBTI charging kinetics for the devices we have studied that actually allows us to extract the time dependent variation of the two components of ΔV_{th}(NBTI). We begin by noting that if we take the data of Fig. 1 and plot ΔV_{th} at fixed time as a function of V_{ds}, we can generate a series of curves as shown in Fig. 4a, which emphasize the variation of ΔV_{th}(NBTI) with V_{ds}. One observes that the curves are in fact not parallel, but tend to diverge at lower V_{ds}. We now assume that (i) holes are trapped rapidly in comparison with the generation of interface states, so that for early times the interface state component is negligible, and (ii) that interface state generation is roughly independent of drain voltage. One can now write the trapped hole and interface state contribution to the total threshold voltage shift as

$$\Delta V_{th}(t) = \Delta V_{th}^{h}(t) + \Delta V_{th}^{is}(t) . \quad (6)$$

It is reasonable also to suggest that for times t_1, t_2 ($t_2 > t_1$) not too different from one another, hole trapping increases proportionally with time so that

$$\Delta V_{th}(t_2) = a(t)\Delta V_{th}^{h}(t_1) + \Delta V_{th}^{is}(t_2) . \quad (7)$$

This equation models the divergence of the curves at lower V_{ds}: for longer times, more interface states are generated. In Eq. (7), $\Delta V_{th}^{is}(t_2)\,\Delta V_{th}^{is}(t_2)$ is the shift due to interface states generated between times t_2 and t_1. Finally, if we take the curve in Fig. 4a corresponding to a time of 20 s as one for which $\Delta V_{th}^{is} \sim 0$ (an arbitrary choice, provided t is short), we can construct the interface state density as a function of time. Plots of $\Delta V_{th}(t_2)\Delta V_{th}(t_2)$ as a function of $\Delta V_{th}^{h}(t_1)\Delta V_{th}(t_1)$ for two choices of t_2 and t_1 yield straight lines, as shown in Fig. 4b, with slope a(t) and intercept $\Delta V_{th}^{is}(t_2)\Delta V_{t2}^{is}(t)$. The density of interface states determined from the intercepts is plotted as a

function of time in Fig. 5. As mentioned previously, implicit in this calculation is that interface state generation is independent of V_{ds}, which is reasonable given that the field (and G(E) from B. above) is uniform across the large fraction of the channel. In choosing t_1 and t_2 values, we found that a difference of no more than 100 s gives reasonably straight line plots such as those in Fig. 4b; accordingly we chose t = 20s, 50s, 100 s, 200 s…600 s. Given the level of approximation adopted here, we feel that the results are reasonable and that the model, although qualitative, is justified.

In developing the plot of interface states shown in Fig. 5 we have assumed certain things about NBTI charging: that it comprises separate hole and interface state generation in HfSiON, and that the interface states are generated relatively slowly, and after holes are trapped. The first of these implications is consistent with the literature, although in fact it is more likely that a wide range of interface and near-interface defects, with widely varying response times, exists. In that case, what we (and others who write equations similar to Eq. (6)) have done is to probe two broad classes of defect: one that is relatively slow (ΔV_{th}^{h}) and one that is relatively fast (ΔV_{th}^{is}). The latter assumption we cannot prove, but we note that it is consistent with interface state generation models in which H_2 diffusing through the oxide "cracks" on a positively charged center and de-passivates a silicon dangling bond [12]. That model has been developed to explain interface state generation in radiation damaged oxides, and we suggest that it may be appropriate here as well.

4. Conclusion

We have performed NBTI measurements in high-k gate stack devices, and these reveal an anomalous dependence of the threshold voltage shift on V_{ds} as one changes the stress conditions

from the linear to the saturation mode.This effect was not observed in devices with pure SiO_2 gate dielectrics. Customarily, NBTI in MOSFETs is studied either with the source, body and drain contacts shorted or with a small potential (~ 0.1 V or less) between the source and drain contacts. We are presently unable to say, on the basis of our measurements and of published data, whether or not the observed effect is particular to our devices or generic to other devices or dielectric gate stacks. If, for example, the effect is generic to high-k gate stacks involving complex oxides, our data has important implications for estimates of the reliability lifetime due to NBTI in p channel MOSFETs. We provide evidence that this effect is consistent with removal of holes/protons at the drain contact by conduction along the dielectric stack, i.e. lateral charge transport.

A simple two-species model that assumes interface state buildup is slow compared to hole trapping allows us to extract values for the interface state density component of ΔV_{th}(NBTI) in the HfSiON based devices. The interface state density tends to saturation at times greater than 500 s, at which time it is found to be on the order of 10^{11} cm^{-2}. These values are consistent with published data on interface state generation by NBTI in devices having a variety of dielectric gate stacks [9, 13, 14]. Furthermore, they are consistent with the values one can deduce from the data in Fig. 2 for pure SiO_2 gate devices where we expect interface state generation by NBTI to dominate charge trapping in the "bulk" of the dielectric.

Further studies are clearly relevant to ascertain how widespread the phenomena is that we have observed in our devices

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Figure Captions

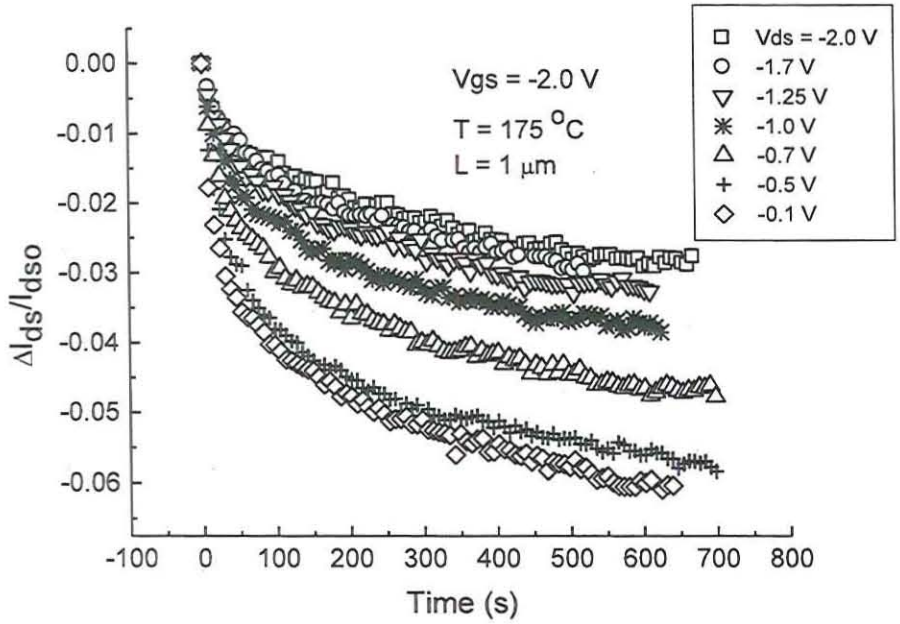
Fig 1. a) Normalized change in drain current in HfSiON based devices measured for NBTI stress at V_{gs} = -2.0 V, T = 175 °C, and varying V_{ds} as indicated. Data was taken approximately every 0.75 s but for clarity only every 10^{th} point is displayed. Measurements were made at V_{ds} = -1.5 V as well but for clarity are not shown. b) Threshold voltage shifts determined from the data of Figure 1a using Eq. (3).

Fig. 2. a) $\Delta I_{ds}(t) / I_{ds}^{o}$ for SiO_2 gate p-channel MOSFETs at 195 °C. Measurements were made in the linear regime (□) and saturation regime (○) b) Data converted to $\Delta V_{th}(t)$ using Eq. 3. In both cases the gate-source voltage was maintained at -2V.

Fig. 3. a) Vertical electric field $E_z(y)$ in the oxide as a function of distance along the channel obtained from a quasi-2D model of the surface potential. Solid line: V_{ds} = - 0.1 V; dashed line: V_{ds} = - 2.0 V. b) Generation rate $G(E_z) \sim E_z e^{\gamma E_z}$ $G(E) \sim E e^{\gamma E}$ in arbitrary units for V_{ds} = - 2.0 V.

Fig. 4. a) ΔV_{th} in HfSiON devices plotted at selected times, as indicated, and as a function of the drain voltage V_{ds} applied during stress. The lines are guides for the eye. (b) $\Delta V_{th}(t_2)$ as a function of $\Delta V_{th}(t_1)$, for three sets of t_2, t_1. The intercept along the $\Delta V_{th}(t_2)$ axis in each case is due to interface states generated between times t_1 and t_2. At time t_1 = 20s, interface state density is assumed to be 0.

Fig.5. Density of interface states determined from the intercepts of curves such as those in Figure 4b.


Vds = -2.0 V
-1.7 V
-1.25 V
-1.0 V
-0.7 V
-0.5 V
-0.1 V
Vgs = -2.0 V
T = 175 °C
L = 1 μm
0.00
-0.01
-0.02
-0.03
-0.04
-0.05
-0.06
ΔIds/Idso
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Time (s)

Fig 1a

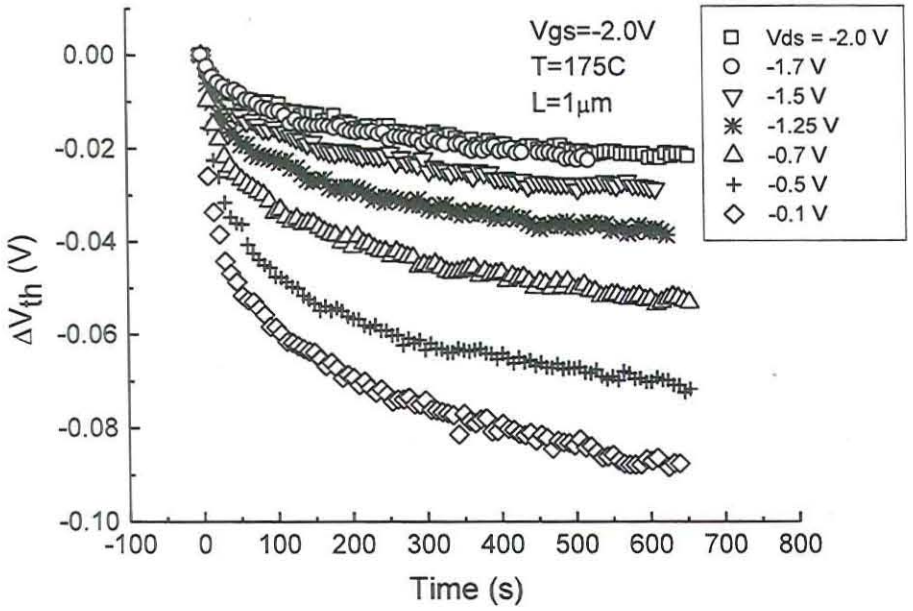
Vgs=-2.0V
T=175C
L=1μm
Vds = -2.0 V
-1.7 V
-1.5 V
-1.25 V
-0.7 V
-0.5 V
-0.1 V
0.00
-0.02
-0.04
-0.06
-0.08
-0.10
ΔVth (V)
-100
0
100
200
300
400
500
600
700
800
Time (s)

Fig 1b

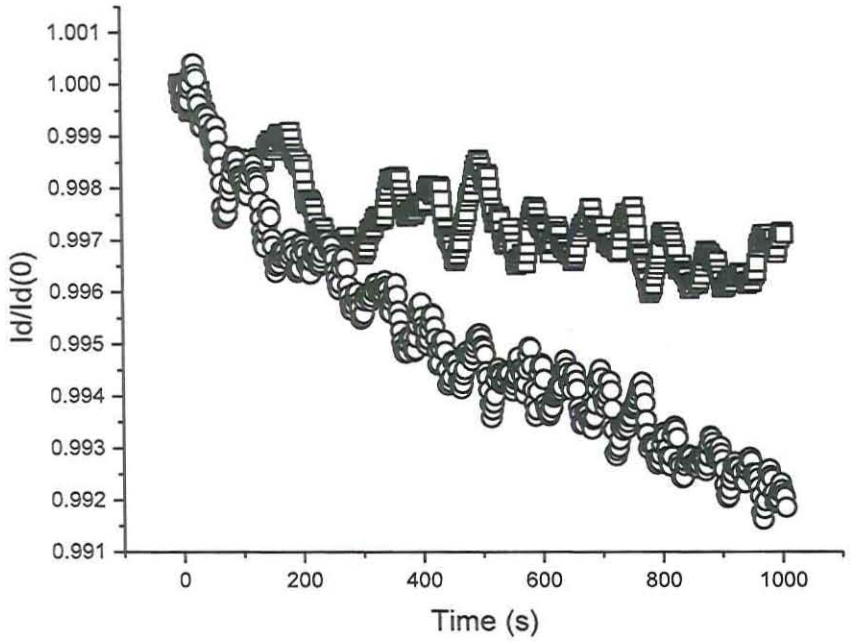
1.001
1.000
0.999
0.998
0.997
0.996
0.995
0.994
0.993
0.992
0.991
Id/Id(0)
0
200
400
600
800
1000
Time (s)

Fig 2a

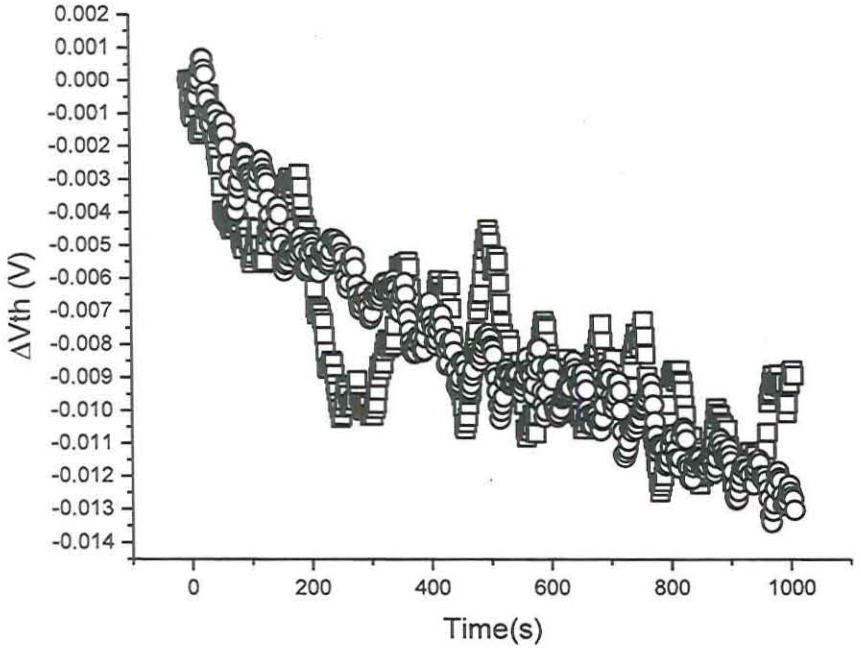
0.002
0.001
0.000
-0.001
-0.002
-0.003
-0.004
-0.005
-0.006
-0.007
-0.008
-0.009
-0.010
-0.011
-0.012
-0.013
-0.014
ΔVth (V)
0
200
400
600
800
1000
Time(s)

Fig 2b

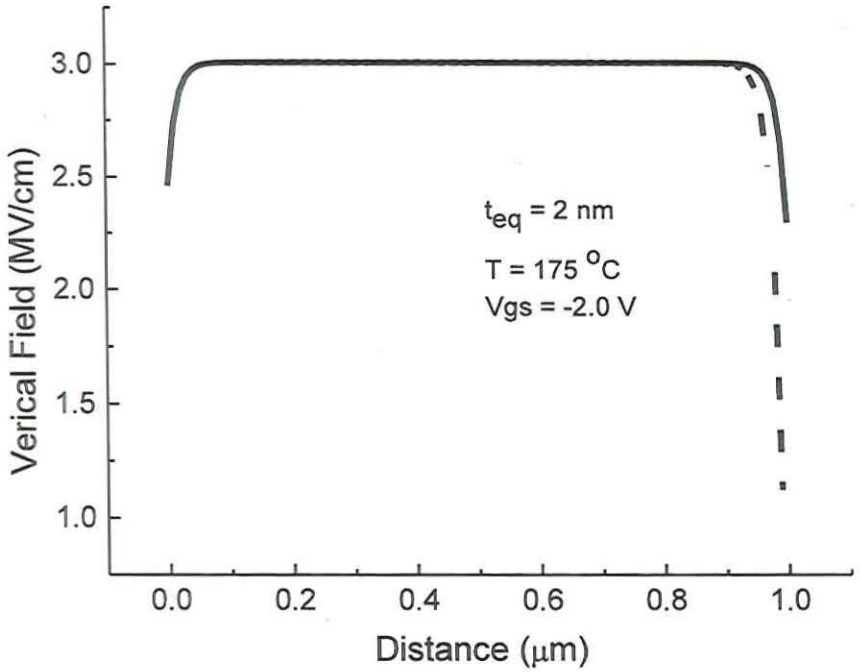
3.0
2.5
2.0
1.5
1.0
Verical Field (MV/cm)
t_{eq} = 2 nm
T = 175 °C
Vgs = -2.0 V
0.0
0.2
0.4
0.6
0.8
1.0
Distance (μm)

Fig3a

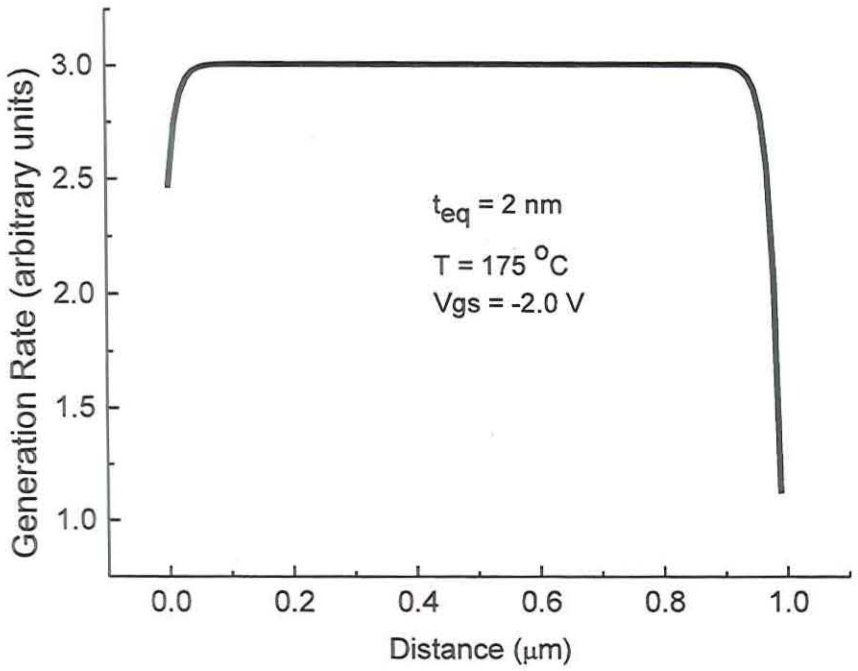
Generation Rate (arbitrary units)
3.0
2.5
2.0
1.5
1.0
0.0
0.2
0.4
0.6
0.8
1.0
Distance (μm)
t_{eq} = 2 nm
T = 175 °C
Vgs = -2.0 V

Fig3b

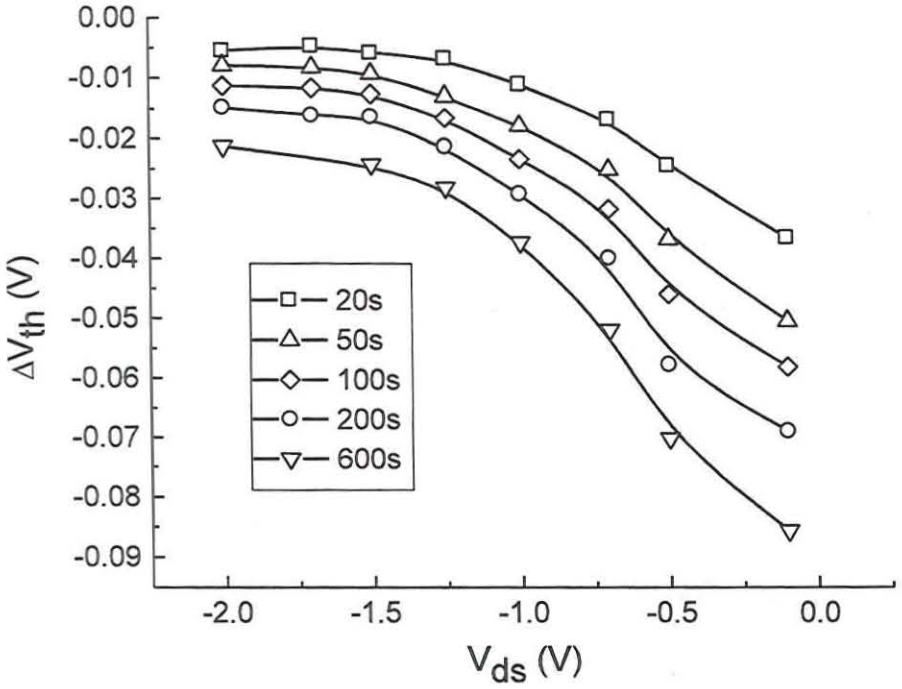
0.00
-0.01
-0.02
-0.03
-0.04
-0.05
-0.06
-0.07
-0.08
-0.09
ΔVth (V)
-2.0
-1.5
-1.0
-0.5
0.0
Vds (V)
20s
50s
100s
200s
600s

Fig 4a

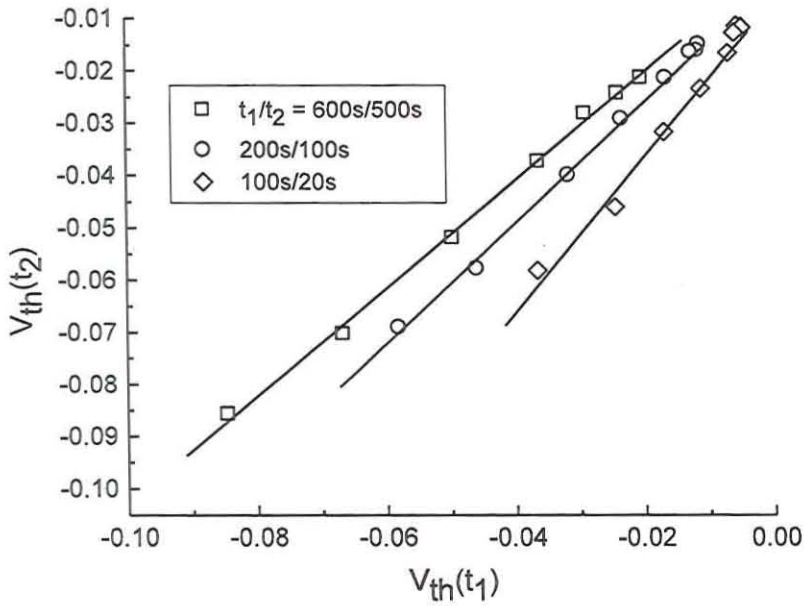
-0.01
-0.02
-0.03
-0.04
-0.05
-0.06
-0.07
-0.08
-0.09
-0.10
$V_{th}(t_2)$
t_1/t_2 = 600s/500s
200s/100s
100s/20s
-0.10
-0.08
-0.06
-0.04
-0.02
0.00
$V_{th}(t_1)$

Fig 4b

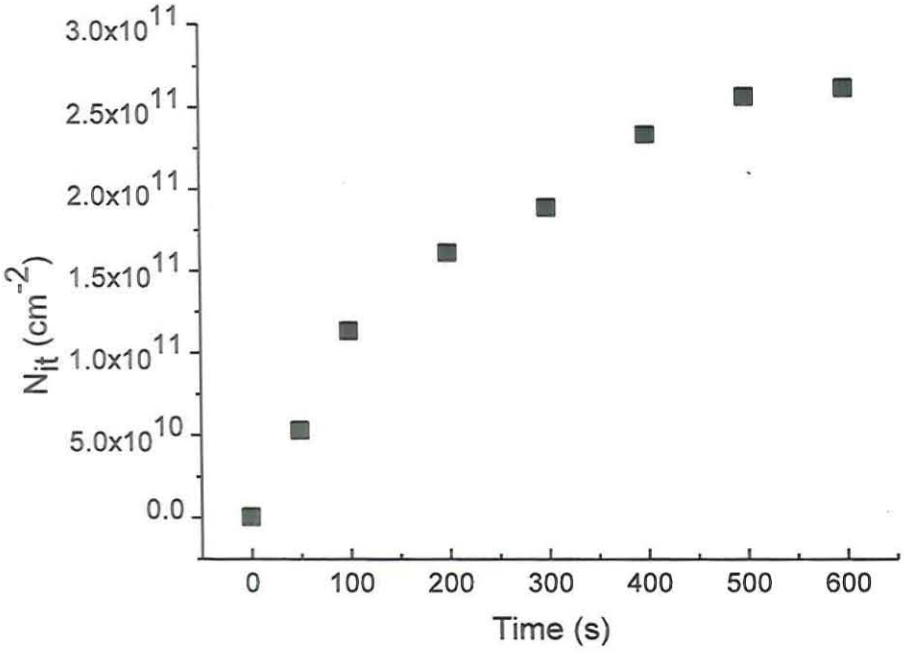
3.0x10^11
2.5x10^11
2.0x10^11
1.5x10^11
1.0x10^11
5.0x10^10
0.0
N_it (cm^-2)
0
100
200
300
400
500
600
Time (s)

Fig 5