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14. ABSTRACT
We demonstrate the feasibility of fabricating heterojunctions of semiconductors with high mismatches in lattice constant and coefficient of thermal expansion by employing nanomembrane bonding. We investigate the structure of and electrical transport across the interface of a Si/Ge bilayer formed by direct, low-temperature hydrophobic bonding of a 200 nm thick monocrystalline Si(001) membrane to a bulk Ge(001) wafer. The membrane bond has an extremely high quality, with an interfacial region of ~1 nm. No fracture or delamination is observed for temperature changes greater than 350 _C, despite the approximately 2:1 ratio of thermal-expansion coefficients. Both the Si and the Ge maintain a high degree of crystallinity. The junction is highly conductive. The nonlinear transport behavior is fit with a tunneling model, and the bonding behavior is explained with nanomembrane mechanics. :

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Si/Ge Junctions Formed by Nanomembrane Bonding

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ABSTRACT We demonstrate the feasibility of fabricating heterojunctions of semiconductors with high mismatches in lattice constant and coefficient of thermal expansion by employing nanomembrane bonding. We investigate the structure of and electrical transport across the interface of a Si/Ge bilayer formed by direct, low-temperature hydrophobic bonding of a 200 nm thick monocrystalline Si(001) membrane to a bulk Ge(001) wafer. The membrane bond has an extremely high quality, with an interfacial region of ~1 nm. No fracture or delamination is observed for temperature changes greater than 350 °C, despite the approximately 2:1 ratio of thermal-expansion coefficients. Both the Si and the Ge maintain a high degree of crystallinity. The junction is highly conductive. The nonlinear transport behavior is fit with a tunneling model, and the bonding behavior is explained with nanomembrane mechanics.

KEYWORDS: nanomembrane · heterojunction · bonding · semiconductor · silicon · germanium

The direct bonding of dissimilar semiconductors provides many opportunities for the design of novel hybrid optoelectronic devices[1−3] and micro- and nanoelectromechanical systems (MEMS and NEMS).[4] The formation of high-quality interfaces and electronic junctions directly between dissimilar materials is, however, significantly constrained by materials properties. In one limit, heteroepitaxy provides the best achievable structural interfaces, but heteroepitaxy can be accomplished only for materials with small differences in lattice constants (and thus in composition), before dislocation formation or total loss of crystalline order results. Only device structures for which such small compositional differences are acceptable are possible, and their properties, in turn, are degraded by dislocation formation.[5−7] In the alternative, formation of a heterojunction by wafer bonding, thermal-expansion mismatch during bonding or thermal cycling frequently leads to either complete or local bond failure and the generation of massive numbers of dislocations, depending on the materials and the process.[8]

In particular, the formation of a heterojunction between Si and Ge by growth or wafer bonding has been generally unsuccessful. Such a structure is constrained by a 4.2% mismatch in lattice parameter and a ratio of thermal expansion coefficients of about 2:1 (Ge:Si).[9] Yet, there are many reasons why such junctions would be useful, for example, photovoltaics,[10,11] photodetectors,[12,13] light emitters,[14] and radio frequency MEMS[15] compatible with Si device fabrication technology.

In efforts to circumvent the problems inherent in heteroepitaxy or bulk wafer bonding, we consider here a different approach, the bonding of a free-standing, monocrystalline semiconductor nanomembrane [Si] to a bulk substrate of a dissimilar material [Ge] (or more generally, the bonding of two dissimilar nanomembranes to each other). This approach is made possible by the development of methods to release very thin single-crystal sheets (10−500 nm) by etching away a buried layer of different composition using a highly selective chemical etchant and to transfer these sheets to an arbitrary new host substrate (for a review, see ref 16). The ability to bond thin, single-crystal membranes to rigid substrates or to each other at low temperatures provides increased flexibility in the fabrication of hybrid electronic, optoelectronic, and thermoelectric-device structures.

Two important questions immediately arise: (1) How well can one bond dissimilar materials if one or both are nanomembranes? (2) How does the interface between such a bonded pair influence electronic transport across the interface? To address these questions, we bond a very thin (200 nm) sheet of single-crystal Si to a bulk Ge substrate and measure charge transport across the bonded interface.

We find exceedingly good bonding of membranes to a host substrate, with a narrow, well-defined interface. We explain the bonding behavior in terms of elastic properties of thin membranes and strain

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sharing between thick and thin materials. We demonstrate that the interface is likely due only to twist boundaries. Cross-membrane electrical transport is nonlinear, with a quite high minimum conductance, sufficiently high for practical applications. We fit the interfacial charge transport using a tunneling model.

RESULTS AND DISCUSSION

Nanomembrane Transfer and Bonding. Semiconductor nanomembranes (NMs) are rapidly emerging as a new platform technology. The interest has focused on both the fabrication of novel structures[17−19] and the transfer and bonding of membranes to new hosts.[20−22] In these efforts, for a variety of reasons, the detailed structural and electrical quality of the bond interface is not of concern in the science or technology being explored. Here, we are specifically interested in those aspects, as our goal is to investigate the extent to which a semiconductor NM bond interface can produce high cross-interface electrical conductance.

We fabricate silicon nanomembranes from commercially available Soitec Smart Cut silicon-on-insulator (SOI) substrates. The silicon template layer is patterned using standard optical lithography to define membranes and to create access channels to the buried oxide layer. The patterned SOI is submerged in a solution of hydrofluoric acid to etch away the buried oxide layer and release the membrane from the thick handle substrate. We form bonded junctions between Si and Ge by transferring an ∼200 nm thick Si(001) NM to a bulk Ge(001) substrate by either a wet- or a dry-transfer technique and annealing the composite system at a temperature of 400 °C with no applied external pressure. Both the Si NM and the Ge surfaces are chemically etched prior to bonding.

In a wet-transfer process, the NM is always kept in water or dilute HF etching solution. Because its surface is hydrophobic under these conditions, the NM floats on the solution surface. Surface tension keeps the NM flat but applies negligible stress that, if it were large, could damage extremely thin (<100 nm) membranes during manipulation. The membrane is moved to the host substrate in liquid or the host substrate is dipped into the liquid containing the membrane to initiate contact and bonding.

Alternatively, for relatively thick NMs (>100 nm), a temporary adhesive stamp may be used for simultaneous dry transfer of large areas or patterns of membranes. We use thermal-release tape in this transfer method. After the membranes are released by etching away the oxide, they are allowed to settle back onto the original substrate (the handle wafer in SOI). The NMs, which are now only weakly bonded to the substrate by van der Waals forces, are simply picked up using the thermal-release tape and transferred to the new host substrate. Heating the substrate and tape together causes the tape adhesive to foam, reducing the contact area and adhesion with the membrane. The tape is lifted off, leaving the membranes on the new substrate. Residual adhesive is chemically removed. An example of a transferred NM is shown in Figure 1.

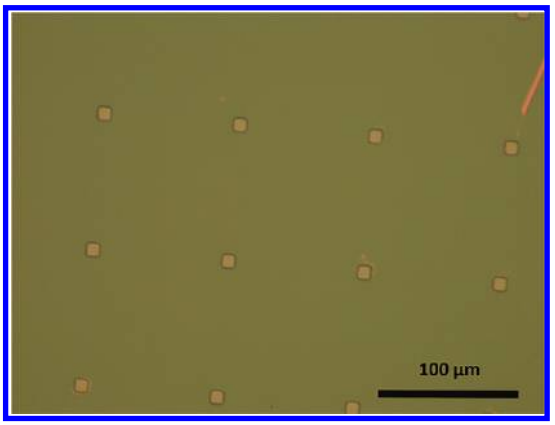

Figure 1. Optical micrograph of a 220 nm thick Si NM bonded to a bulk Ge substrate and annealed at 400 °C. The membrane was transferred using thermal-release tape. The lighter areas are holes in the NM for etchant access to the originally underlying silicon dioxide.

To increase adhesion and promote covalent bonding between the membrane and the new host material, the Si NM−Ge pair is heated slowly from 100 to 400 °C at a rate of 5 °C/min, held at 400 °C for 30 min, and ramped down to 50 °C at the same rate. Using optical microscopy, we observe no fracture, buckling, or delamination of the Si NM throughout the annealing process. Widely separated bubbles occasionally form, presumably due to trapped gases or particle contamination. These areas do not affect the overall membrane bonding quality and cause no extended-defect formation.

Figure 2 demonstrates some of the features of a transferred and annealed Si/Ge bonded pair. Si NMs, each 1.32 mm square, are prepared from SOI *via* lithographic patterning and released. Several such NMs were transferred simultaneously in registry to a Ge wafer using thermal-release tape. Figure 2 shows one complete checkerboard and part of an adjacent one. In the right checkerboard in the image, particles contaminating the Ge surface before bonding allow us to show how limited their effect is. The exceptionally low bending stiffness of NMs means that they are so compliant that they simply wrap around these very occasionally occurring particles. Although particles at the interface are clearly not desirable, their presence is not catastrophic and their impact is localized. For wafer bonding or Smart Cut transfer, these particles would have created very large unbonded areas.[8]

The success of nanomembrane bonding, relative to bulk wafer bonding, is explained as follows. First, the thinness of the membrane results in an extremely conformal film on the microscale, increasing the initial contact area and, therefore, total adhesion energy. Second, for a thin film on a relatively thick, rigid substrate,

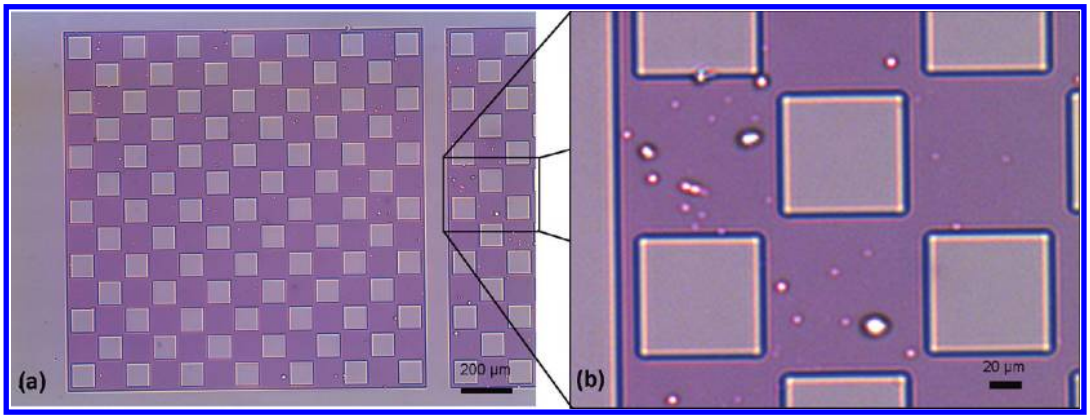

Figure 2. Optical micrographs of Si NM/Ge bonded pairs. (a) 220 nm thick Si(001) NMs prepared with large square holes in a checkerboard pattern are transferred to a Ge(001) substrate using thermal-release tape and bonded at 400 °C. Si is dark, and the Ge is seen through the holes as light areas. The holes are 80 μm × 80 μm. The size of a complete membrane is 1.32 mm × 1.32 mm. One complete membrane and part of another are shown. (b) A magnified view of the outlined area on the left shows particles trapped at the interface with the Si NM tightly enclosing them.

essentially all of the thermal-mismatch strain energy resides in the thin film.[23] The amount of strain energy stored in the film is directly proportional to its thickness. When very thin compared to the substrate, the bonded membrane contains insufficient strain energy to drive separation or cause fracture. The calculated maximum in-plane strain in a 220 nm Si NM bonded to Ge for annealing to 400 °C is only 0.12%, with a corresponding in-plane stress of 0.22 MPa. The film simply stretches in plane with the Ge substrate, and negligible bending of the substrate occurs.

We contrast this result to typical wafer bonding of smooth wafers of thermally mismatched materials, where each wafer is of the order of a few hundred micrometers thick.[24] In such a configuration, the out-of-plane bending stress caused by unequal expansion is borne by both wafers. This stress drives crack propagation from the edges of the wafer either through the bulk of a wafer or at the bonding interface. Under conditions of initially strong interfacial adhesion or externally applied pressure, some of the strain may be relaxed by microcracks, dislocations, or phase transformations at the interface. These defects are avoided in nanomembrane bonding by remaining below the critical stress—or equivalently, the critical thickness—of the membrane for the onset of these failure mechanisms.[23]

The transfer of free-standing nanomembranes is qualitatively different from the Smart Cut (*i.e.*, ion-cutting) process of transferring thin layers to a new host substrate on the wafer scale.[25] In the Smart Cut process, the transferred layer is rigidly affixed to either the source wafer or the new host wafer at all times. The bonding surfaces must be extremely flat and smooth on all length scales and particle-free to ensure good initial adhesion, because of the rigidness of the wafers. Otherwise, large areas remain unbonded with significant residual stress near encapsulated particles or surface asperities. In contrast, a free-standing membrane is able to stretch and bend. Membranes can conform more readily to surface asperities and may be bonded to nonplanar surfaces. Furthermore, membrane transfer and bonding avoids the polishing and etching needed in Smart Cut transfers to remove damage from the thin-film exfoliation process. The additional polishing step usually requires thicker films to be transferred, thus limiting the transferred film's compliancy during the bonding step.

Interface Quality. The above optical-microscopy results suggest excellent interface quality after bonding the Si NM to the bulk Ge. We investigate the interfaces and the crystallographic integrity of the bond in greater detail with cross-sectional transmission electron microscopy (XTEM). Figure 3 shows a high-resolution XTEM micrograph of the interface of a Si(001) NM/Ge(001) bonded pair fabricated by dry transfer. The lower-magnification image (Figure 3a) shows that the Si NM/Ge bond interface has no inhomogeneities: extended defects, inhomogeneous strain fields, precipitates, and inclusions are absent from the bond interface and in the crystalline material near the interfacial region. Figure 3b is a high-resolution image of the interfacial region between the Si and Ge. The XTEM samples were fabricated such that the [110] direction of the Si NM is perpendicular to the face of the cross-section. When bonding the Si NM to the Ge, there is typically a twist angle (θ) between similar in-plane directions of the NM and the substrate. We determine this twist angle to be ~22° by measuring the tilt angle between the [110] directions in the Si NM and the Ge substrate with transmission electron diffraction (see the Materials and Methods section). Lattice fringes are visible in the Si NM, indicating that the NM remains crystalline throughout the bonding process. The high twist bond angle, between the Si NM and the Ge substrate, prevents the appearance of high-resolution fringes from the Ge substrate in the same image as the Si. Nevertheless, electron diffraction patterns of the Ge very near the interfacial region indicate that the Ge is

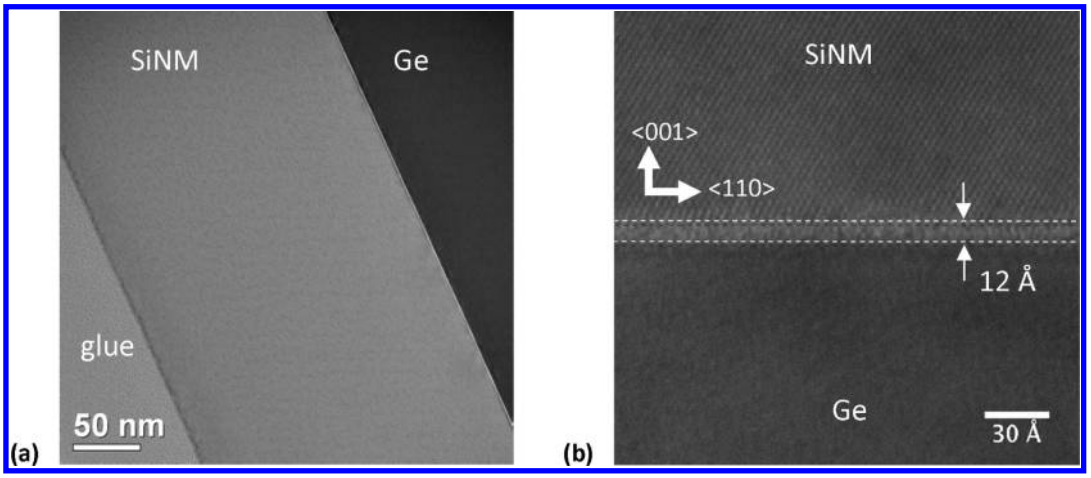

Figure 3. Transmission electron microscopy images of the interface region between a Si(001) NM bonded to a Ge(001) substrate by dry transfer and annealed at 400 °C. (a) XTEM image showing the entire thickness of the Si NM with no strain variations or extended defects near the interface. (b) A high-resolution image oriented along the Si(110) zone axis. The crystalline orientation of the Si NM is as shown. The interfacial region is ~1.2 nm thick.

monocrystalline. The interfacial region appears to be amorphous and approximately 1.2 nm thick.

To place our results in context, we summarize here the experimental evidence and simulation of interfaces of bonded bicrystals that has emerged in recent years. Several experimental studies of single-element hydrophobic (*i.e.*, hydrogen-terminated) bonding of Si(001)/Si(001) wafers indicate that the interfacial structures fall into three categories with respect to twist angle (θ).[26] If $\theta < 5°$, the interface is crystalline with a network of dislocations at the interface; for $5° < \theta < 10°$, the interface is partly crystalline with amorphous regions forming at the interface; and for $\theta > 10°$, the interface is entirely amorphous. No lattice constant mismatch (only orientation changes) is involved.

In general, a crystalline interface can be described within the standard framework of bicrystallography.[27] At low twist angles, the underlying symmetry of the crystal structure is preserved at the interface because of the high density of coincident-lattice sites of the joined crystals. It is energetically favorable to form patches of a continuous crystal across the interface with an array of screw dislocations bounding the crystalline regions to produce the lowest interfacial energy. The distance between dislocations (S_d) for these particular crystal structures is given by[28]

$$S_d = \frac{a_1 a_2}{[2(a_1^2 + a_2^2 - 2a_1 a_2 \cos\theta)]^{1/2}} \quad (1)$$

where a_1 and a_2 are lattice constants of the two crystals and θ is the twist angle between the lattice vectors within the interfacial plane. A plot of the dislocation spacing as a function of twist angle is shown in Figure 4. For simplicity, we ignore the slight tilt misorientation from the ideal (001) surface planes, which also produces interfacial defects.

For the Si(001)/Ge(001) interface, the dislocations require an edge component to account for the 4.2% lattice mismatch. The dislocation spacing with no twist is 10 nm and is completely edge-type in character. With an increase in twist angle, the dislocations have both screw and edge components. As can be seen from Figure 4, the dislocation spacing at the Si/Ge interface converges to that of the Si/Si interface for $\theta > 5°$. Because of their similar crystal structures and sp^3 bonding nature, we assume that Si/Ge high-angle twist boundaries will be similar in character to Si/Si high-angle twist boundaries. For high twist angles, the density of coincident-lattice sites is very low, resulting in a very small spacing between screw dislocations. Organization of the interface into crystalline regions is no longer energetically favorable. The interfacial atoms instead rearrange into an amorphous layer to bond the two surfaces covalently while maintaining the highly directional sp^3 bonds.

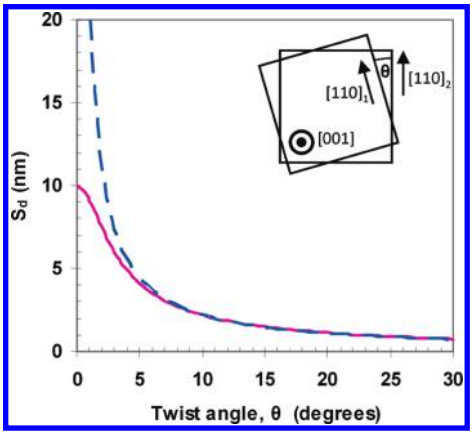

Figure 4. Plot of eq 1 showing the dislocation spacing (S_d) as a function of twist angle using parameters for a Si(001)/Si(001) interface (dashed line) and a Si(001)/Ge(001) interface (solid line). There is little difference above 5°. For Si/Si, S_d asymptotically approaches infinity as θ approaches 0.

Molecular dynamics simulations of high-angle twist boundaries formed between grains of nanocrystalline Si show that an amorphous interlayer exists between

grains.[29] The calculated radial density function for these interlayers is practically identical to that of bulk amorphous Si. The principal conclusion of these simulations is that the amorphous interlayer is energetically lower than alternative interfaces, making it the thermodynamically preferred state for twist angles greater than 10°. Otsuki measured the interfacial energy between Si(001) twist boundaries from 0° to 45° and found that the interfacial energy for twist angles >10° was nearly constant, in agreement with the simulations.[30] The simulations also predict that the interlayer tends to be between 4 and 8 ML (monolayers) thick, independent of twist angle. The vast majority of Si atoms within the amorphous layer is 4-fold coordinated with less than 10% of them either 3- or 5-fold coordinated, indicating that the density of dangling bonds near the interface is less extensive than one may initially expect. The low stiffness of NMs makes it likely that the interface region is as least as small, and possibly smaller, than for bulk crystals.

Thus far, we have only considered geometrical relationships for predicting the structure of the interface. Si and Ge constitute a fully miscible binary alloy system, and interdiffusion could, in principle, drive morphological changes of the interface. Interdiffusion is, however, unlikely to be significant at the temperatures and times used in our experiments. As an example, the diffusivity of Si in Ge is on the order of 10^{19} cm^2/s at 550 °C.[31] Assuming the same diffusivity at a much lower 400 °C, the diffusion length is on the order of 1 Å in 30 min. Although the more open structure of the interface may enhance diffusion, diffusion beyond the interfacial layer is negligible.

Additionally, interfacial contamination could, in principle, play a role. Because our surfaces are hydrophobic, we can rule out most contamination possibilities, even though the initial contact between our bonded surfaces occurs in an ambient atmosphere. Hydrophobic bonding generally produces thinner interfacial layers or crystalline interfaces with minimal extrinsic defects.[32] However, hydrophobic surfaces in bulk wafer bonding generally produce interfaces with low adhesive energy and require higher annealing temperatures to create strong interfacial bonding. For full-wafer bonding, thermal-expansion mismatch limits annealing temperatures to values below those necessary to form sufficiently strong interfaces. In contrast, NMs are ultracompliant and are able to maximize the contact area with the host substrate and to stretch without creation of defects at higher thermal-mismatch strain. Consequently, the benefits of hydrophobic bonding are available to NM bonding. Any low-temperature bonding scheme employing hydrophilic or plasma treated surfaces will likely produce wider interfaces, due to incorporation of other elements.[33,34] The measured interfacial conductivity of bonded hydrophobic Si/Si wafers is clearly superior to hydrophilic bonding for this reason.[32] If electrical conduction across the interface is desired, hydrophilic bonding, even though it is much easier in bulk materials, is counterproductive. As we demonstrate here with NMs, hydrophobic bonding produces excellent interfaces.

We conclude that the bonded Si/Ge interface structure is a thin amorphous layer created by twist boundaries. This interfacial region is thermodynamically stable and only a few lattice constants wide, owing to the strong sp^3 bonding, which drives atomic reorganization at the interface. Interdiffusion will be insignificant for the range of temperatures and times under consideration. Because our Ge and Si NMs are hydrogen-terminated, contamination is minimal and does not likely contribute to the interface width.

Electrical Characterization. Membrane bonding in the manner described above creates a narrow interfacial region with a high density of atomic defects. Simplistically, any interface creates a barrier to charge transport. In principle, the interface can always be made more resistive by deliberately adding an interfacial dielectric layer. We attempt to minimize the dielectric layer to make the cross-barrier conductivity high, and our narrower interface, relative to conventional wafer bonding of Si and Ge, presents that opportunity.[33,34]

To investigate cross-interface conduction, we use a 200 nm n^+−Si NM ($4 \times 10^{20}/cm^3$) bonded to a p^+−Ge wafer ($>1 \times 10^{20}/cm^3$) and annealed at 400 °C for 30 min (see the Materials and Methods section). High doping reduces depletion regions, thus better defining the interface electrically, and ensures a high density of mobile carriers for enhanced charge transport.

After transferring the Si NM, we create 100 μm × 100 μm mesas of Ge and Si/Ge and deposit metal contacts, as depicted in Figure 5. Current−voltage ($I-V$) characteristics are then measured from mesa to mesa. Positive bias is defined with respect to the Si contact as ground. Typical results of dc $I-V$ measurements are shown in Figure 6a. The maximum relative errors were 0.3% for current and 0.01% for voltage at zero applied bias with no dependence on the polarity of the swept voltage. There was no appreciable difference in curves from pads measured at adjacent sites.

We confirmed that Si contacts were Ohmic on separate control devices formed using the same SOI substrate from which the Si NMs were fabricated. dc current−voltage measurements of bonded Si/Ge interfaces are shown in Figure 6a for three different current paths defined in the inset. Path 1 is from a bottom contact on the Ge bulk substrate to a Ge mesa contact on the top; the curve confirms Ohmic conduction through the bulk Ge wafer and Ge contacts. Path 2 is from the bottom Ge contact to a Si/Ge mesa contact on the top; at high biases, the current parallels path 1, indicating that conduction has become limited by the series resistance of the bulk substrate. Path 3 is from the top Ge mesa contact to the Si/Ge mesa contact; the

current increases much more rapidly with applied bias as compared to path 2 through the bulk. It is, therefore, clear that series resistance influences the $I-V$ characteristics of the bonded Si/Ge mesa, and we consider the extracted conductance to be a lower limit of the actual conductance of the interface.

We have calculated the conductance from Ge-to-Si/Ge mesa charge transport measurements by taking the derivative of the $I-V$ curve of path 3 in Figure 6a and compared it to the measured conductance of the same device path using an ac impedance meter (Figure 6b). The ac conductance measured at different junction biases and fixed frequency (10 kHz) matches the conductance calculated from the dc $I-V$ measurements (see the Materials and Methods section). The minimum specific conductance, defined as the conductance normalized by the total interface area (1.0×10^{-4} cm^2), is 6 S/cm^2 at a bias of approximately -70 meV.

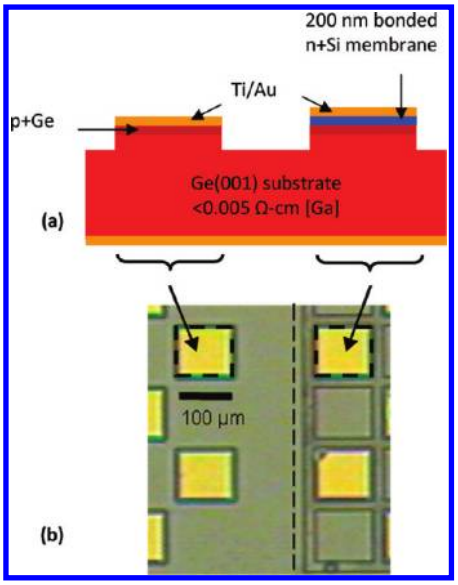

Figure 5. Device structures for cross-interface charge transport measurements. (a) A schematic diagram of a cross section of a mesa-type Si/Ge diode (right mesa). The mesas are etched ~2.4 μm below the original Ge surface prior to evaporation of Ti/Au contacts. (b) An optical micrograph of Ge mesas (left) and Si/Ge mesas (right) used for charge transport measurements.

On the basis of structural and electrical observations, we suggest a tunneling model to explain interfacial conductance.[35] The amorphous interfacial layer observed with TEM, even though extremely thin, creates a potential barrier to electronic transport, which may exist in addition to or in place of an interfacial dipole or potential barrier caused by differences in electron affinities and band gaps of the Si and Ge. The barrier must be narrow because we observe high conductance even at low bias.

The device resembles a typical tunneling diode (Figure 7).[36] Both the Si and the Ge are degenerately doped. Degenerate doping creates impurity energy bands within the Si and Ge band gaps that merge with the respective conduction and valence bands. The presence of filled and empty electronic states immediately adjacent to the barrier allows tunneling to occur. However, unlike a tunneling diode, there is no observed negative differential resistance at forward bias when the Fermi level of Si passes through the energy gap of Ge at forward bias. Conduction at this condition is most likely due to the numerous interface states and traps expected to be within the barrier. They provide states within the forbidden band gap by which carriers can tunnel. In addition to trap states, impurity bands can be broad in energy and may provide sufficient overlap of empty and filled states throughout the bandgap region to allow tunneling.

We observe an offset of the conductance minimum to a small negative bias of -70 meV. Such an offset can be explained by a charge imbalance at the interface. The trap states on the silicon (germanium) interface are filled (empty) as a result of the position of the Fermi level at equilibrium (Figure 7a). Accumulation of negative (positive) charge at the Si

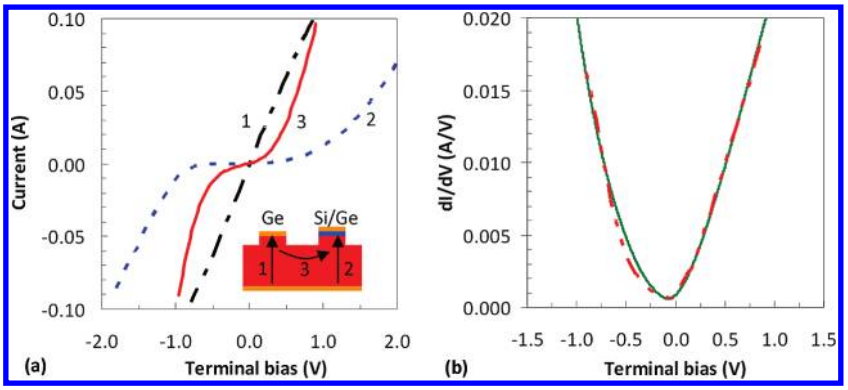

Figure 6. Charge transport measurements across bonded NM interfaces of an area of 100 μm $\times$ 100 μm. (a) Direct-current $I-V$ measurement made for different current paths: path 1 (black dotted-dashed line), Ge mesa to Ge back contact showing Ohmic behavior; path 2 (blue dashed line), Ge back contact to Si/Ge mesa; and path 3 (red solid line), Ge mesa to Si/Ge mesa. (b) Differential conductance measured with an ac impedance meter (green solid line) is compared to the calculated differential conductance (red dashed-dotted line) from the dc $I-V$ data points measured from path 3 of the Ge mesa to Si/Ge mesa shown in (a).

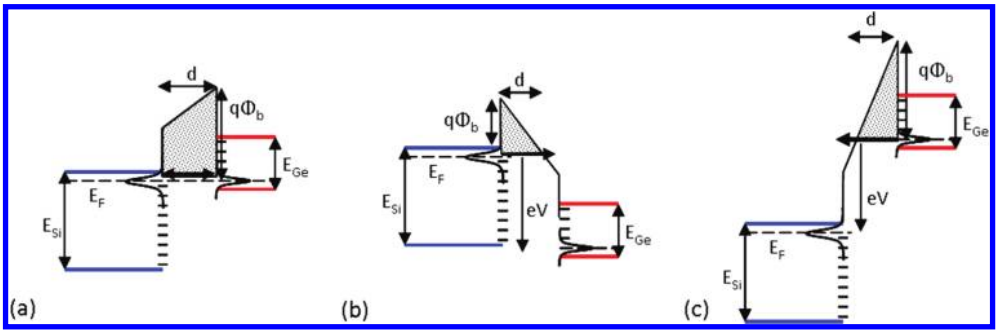

Figure 7. Proposed band diagrams for a Si−barrier−Ge tunneling model. The shaded area in each panel represents the effective tunneling barrier, with a width *d* and height $q\Phi_b$. The intrinsic band gaps of Si and Ge are shown, but the Fermi energy, E_F, passes through the impurity bands. The impurity bands and interface states are represented by curves and dashes, respectively. Tunneling is denoted by a heavy arrow. For clarity, not all tunneling possibilities are shown. At equilibrium (a), tunneling occurs in both directions and no net current is measured (even though the conductance is high). At high forward bias (b), tunneling occurs primarily from the Si conduction band/impurity levels to the Ge conduction band. At high reverse bias (c), tunneling occurs primarily from the Ge valence band/impurity levels to the Si conduction band.

(Ge) interface creates an electric field that has the effect of a positive bias. A negative bias is required to compensate this field.

Having assumed a potential barrier at the interface, we can semiquantitatively predict the conductance or *I*−*V* characteristics of the junction. Elastic tunneling occurs in both directions simultaneously, producing a net current. The current density *J* for the arbitrary case is given by[36]

$$J = \frac{q}{4\pi^2\hbar}\int\int T[F_1(E) - F_2(E)]\mathrm{d}\,k_\perp^2\,\mathrm{d}\,E \qquad (2)$$

where *T* is the 1-D barrier transmission probability and the *F*'s are the distributions of occupied states on either side of the barrier. The integrals are evaluated over the range of kinetic energies for which the electron's transverse momentum, $k_\perp$, is the same on both sides of the barrier. Implicit in this formulation is the energy−momentum relationship, which must be specified.

The barrier transmission probability is approximated using the Wentzel−Kramers−Brillouin (WKB) approximation

$$T \cong \exp\left(-\frac{2}{\hbar}\int_0^d |k(x)|\mathrm{d}\,x\right) \qquad (3)$$

where *k* is the wave vector of the electron within the barrier and the integration limits are the classical turning points at the barrier's edges. For a rectangular barrier of height $q\Phi_b$ and width *d*, the transmission probability is approximately

$$T \cong \exp(-\alpha d\sqrt{\Phi_b}) \qquad (4)$$

where $\alpha = 2(2qm^*)^{1/2}/\hbar$ and m^* is the effective mass within the barrier. It is clear from this expression that a change in barrier width has a greater influence on the transmission probability than a change in barrier height.

The minimum transmission probability occurs when the product $d(\Phi_b)^{1/2}$ is greatest; that is, the barrier is approximately rectangular. An applied voltage distorts the barrier and changes its transmission probability. At low biases, the barrier is trapezoidal. The width remains essentially constant, and the barrier height effectively changes. At high biases, the barrier becomes triangular and the tunneling distance changes linearly with the applied voltage. This is the classical Fowler−Nordheim (FN) tunneling regime often observed in metal−insulator−metal or metal−insulator−semiconductor devices. The current density is given by the expression[36]

$$J = \frac{q^2V^2}{16\pi^2\hbar d^2\Phi_b}\exp\left(\frac{-4\sqrt{2qm^*}d\Phi_b^{3/2}}{3\hbar V}\right) \qquad (5)$$

At high applied bias, the current density increases approximately as the square of the voltage drop and not exponentially as for a typical p−n junction. The change in conductance is then approximately linear with increasing voltage. Figure 8 is a plot of conductance measured with an impedance meter from −10 to +10 V of terminal bias. The conductance follows the functional form of a Fowler−Nordheim tunneling model for both forward and reverse biases. The deviation from linearity results from a constant series resistance (0.73 Ω) that was included in the calculation. For low biases ($|V| < 1$ V), the measured conductance deviates slightly from the FN model because the barrier width is essentially fixed and direct tunneling through a trapezoidal barrier occurs.

The observed asymmetry of the conductance results from an asymmetric energy barrier with respect to Si and Ge. The height of the barrier on the incident (transmitted) side is determined by the energy of the filled (empty) state. An applied bias not only distorts the barrier (Figure 7b, c) but also changes the state to which the carrier tunnels. For example, in reverse bias, the Fermi level of Si moves below that of Ge, bringing an empty state higher in the Si conduction band to the same energy as the filled state in the Ge valence band. Thus, reverse bias reduces the effective barrier height,

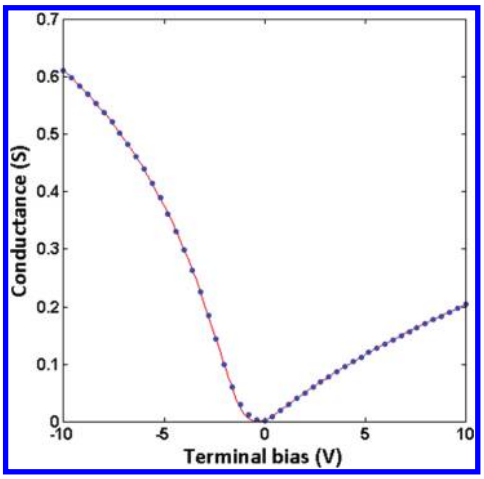

Figure 8. ac conductance as a function of terminal bias. The data (blue dots) are fit applying only a Fowler−Nordheim tunneling model (red solid line) assuming a barrier width of 1.2 nm and a series resistance of 0.73 Ω. In forward bias, $\Phi_b = 1.27$ eV and $m^* = 0.0170\ m_e$; in reverse bias, $\Phi_b = 1.94$ eV and $m^* = 0.8354\ m_e$.

increasing the tunneling probability. Other factors that may affect asymmetry in conductance include the effective masses of carriers, the dielectric constants, and the density of states of the Si, Ge, and interfacial layer.

A tunneling model can explain the trends in interfacial conductance by correlating current with barrier transmission probability, and a numerical fit can yield physically reasonable parameters. However, the fit is not unique based solely on these data because of the mathematical interdependencies of the parameters within the model. A precise, quantitative extraction of interfacial properties from modeling requires extreme caution for several reasons: (1) Our simplified model does not explicitly address the different band structures of Si and Ge. As both are indirect-gap semiconductors, inelastic processes are required to conserve momentum during tunneling. This added constraint should dramatically reduce the tunneling current. (2) Knowledge of the distribution of the interface states, both spatially and energetically, is presently inadequate to estimate their role quantitatively in conduction. We expect $\sim 10^{13}/cm^2$ unsatisfied or strained Si bonds at the interface because Si has a higher planar density of atoms than Ge. This high number of states in combination with the high degree of atomic disorder within the barrier makes it unlikely that a single, uniform barrier potential will apply across the entire interface. A small fractional change in barrier width locally can cause dramatic changes in current density, making homogeneous current flow across the interface unlikely. (3) The effective mass of carriers within the barrier is unknown. It has been shown that energy−momentum dispersion relations of a disordered barrier cannot be accurately determined solely by analysis of conductance curves.[37]

Because of the general overwhelming difficulty in forming bonded Si/Ge structures, measurements of electrical transport across bonded Si/Ge interfaces to compare to ours are scarce. The difference in interface structural and chemical quality makes a quantitative comparison futile in any case. However, as an example, Zahler *et al.* employed a p^+−Ge layer bonded to a p^+−Si substrate and report an interfacial resistance of 400 Ω cm^2.[11] By comparison, the resistance of our bonded n^+−Si NM/p^+−Ge junction is significantly less, < 1 Ω cm^2, of considerable value for high-current-density applications, such as photovoltaics, where high interfacial conductance is crucially important to reduce resistive losses.[10] In general, we can state that our membrane bonded junction conducts very well, well enough, even without optimization, for many applications that require electronic transport across a bonded heterojunction. Thus, nanomembrane bonding can serve as the basis of optoelectronic devices, such as a Si/Ge tandem solar cell, a Si/Ge/Si PIN photodetector, or Si/Ge light emitters.

We have not so far attempted to optimize interfacial conductance. We expect that even higher conductance can be achieved by appropriate surface preparation prior to bonding and by optimizing thermal treatments. Furthermore, postbonding interface modification, such as annealing in forming gas, may lead to a modification of the barrier and thus different *I*−*V* characteristics with presumably higher currents.

CONCLUSIONS

We show successful bonding of a 200 nm thick crystalline Si sheet to a bulk Ge substrate using hydrophobic bonding, characterize the bonding interface, and fabricate diode device structures on this bonded pair to explore cross-interface electrical transport. No indication of separation, fracture, or strain inhomogeneity is observed, demonstrating that NM bonding is an effective and viable method to join highly lattice mismatched materials. XTEM measurements show a very well defined, extremely narrow interface region, controlled by structure rather than interface chemistry, because NM bonding is successful even if hydrophobic surfaces are bonded. Hydrophobic bonding of nanomembranes thus offers a new direction for integration of materials for novel hybrid electronic devices that circumvents the serious problems associated with bulk wafer bonding. Our nanomembrane bonded devices are nonlinear and give a minimum specific conductance of 6 S/cm^2 without any effort at optimization.

Our structural and electronic study of bonded Si/Ge nanomembranes, a material combination that has resisted conventional approaches, makes novel Si/Ge devices that require cross-interface conduction a realistic possibility. More generally, one can expect to extend nanomembrane bonding to other material

combinations, with similar beneficial outcomes. With the current rapid progress in the manipulation, transfer, and stacking of nanomembranes,[38] the high-quality interfaces obtained in nanomembrane bonding make it likely that a new generation of flexible, high-performance semiconductor devices will be enabled.

MATERIALS AND METHODS

Membrane Fabrication. Silicon nanomembranes are fabricated from commercially available Soitec Smart Cut silicon-on-insulator (SOI) substrates with a 220 nm Si(001) template layer on 3 μm of buried silicon dioxide. Thinner buried oxides may be used. Prior to fabrication, the membranes are ion-implanted and annealed (see below). Annealing reduces the membrane thickness ~20 nm by oxidation. Standard optical lithography is used to define membranes of various lateral sizes and shapes, as well as etchant access holes. Reactive-ion etching using SF_6 or $CF_4 + O_2$ removes exposed silicon. The photoresist is removed by soaking in acetone for 10 min using ultrasonication or by pressurized spray. The patterned SOI pieces are cleaned using H_2SO_4/H_2O_2 (1:1) solution in a quartz beaker for 5 min and rinsed in flowing deionized water for 5 min. Particles and residual organic contamination are removed by soaking in a mixture of $NH_4OH/H_2O_2/H_2O$ (1:1:5) for 10 min at 80 ± 5 °C and again rinsed in flowing deionized water for 5 min. The pieces are then placed in concentrated HF (49%) in a Teflon beaker to sit undisturbed to release the Si template layer by differential etching of the buried oxide layer. Etching time varies depending on the thickness of the buried oxide and the required etch distance. Typical etching times are 45 ± 10 min for concentrated HF.

Wet-Transfer Technique. Soon after the complete dissolution of the buried oxide layer, Si membranes may float off the substrate and onto the surface of the liquid solution due to their hydrophobic (H-terminated) surfaces. Frequently, they collapse back onto the original handle substrate during the underetching process and remain weakly bonded. Slight agitation may release them into the liquid. The membranes are then picked out of the water either with Teflon tweezers by electrostatic attraction or by use of a small loop of plastic-coated wire (28 gauge). A water film across the loop provides a surface on which the membrane lies. The membrane is then brought into contact with the new host substrate. Alternatively, the new substrate may be dipped into the beaker with the membrane and pulled out, thus drawing the membrane to the surface by capillary forces. The substrate with membrane is then set on a hot plate at ~110 °C for at least 10 min to allow evaporation of water and to increase initial bonding strength. Usually, any wrinkles in the membrane will smooth out as the shifting interface dries. The final placement and orientation of the membrane is difficult to control using this technique.

Dry-Transfer Technique. Nitto Denko Revalpha Thermal Release Tape (No. 3198LS) may be used to transfer nanomembranes of reasonable thickness (~200 nm) and lateral dimensions on the order of millimeters. The membranes are underetched in HF solution and allowed to collapse onto the original handle substrate. The handle with membranes is then removed from the HF solution and slowly dipped into deionized water to remove residual HF. The substrate with membranes is removed from the water. The thermal-release tape is placed directly on top of the membranes without pressing. An adhesion front starting at the point of first contact spontaneously spreads across the tape/substrate interface. When the membranes are fully adhered, the tape is carefully peeled with minimum bending, to prevent membrane fracture. Frequently, membranes near the initial peeling edge will crack. The tape with membranes is immediately placed on the new substrate without pressing. A slight bending of the tape will usually ensure only one point or line of contact. The adhesion front is allowed to progress spontaneously and often occurs in <10 min for a 1 cm^2 area. The substrate with tape is then placed on a preheated hot plate just above the tape's release temperature (~100 °C). After the tape debonds, the tape is lifted off the substrate. Removal of residual adhesive using photoresist stripper (*e.g.,* AZ 300T from AZ Electronic Materials) for Ge substrates is possible, and is done before high-temperature annealing. Very thin membranes cannot be transferred using this technique as the membranes conform to the foaming adhesive layer of the tape rather than adhering to the new substrate.

Ion Implantation. Before membrane fabrication, the Si template layer of the SOI is ion-implanted (Core Systems, California) with P (dose is $1 \times 10^{16}/cm^2$ at an energy of 12 keV with a 7° tilt) and annealed in N_2 at 950 °C for 45 min to achieve a uniform dopant concentration of $4 \times 10^{20}/cm^3$ throughout the template layer thickness, as measured by secondary-ion mass spectroscopy (Evans Analytical Group, NJ). Sheet resistance measurements by transfer length and Greek cross methods confirm the expected carrier concentration.[39] The as-received Ge wafers were p-type (Ga) with a resistivity of 0.005 Ω·cm. We additionally doped the top 50 nm degenerately to $>1 \times 10^{20}/cm^3$ with Ga by ion implantation (dose is $3 \times 10^{15}/cm^2$ at 40 keV with a 7° tilt). The dopant concentration was also measured by secondary-ion mass spectroscopy. Prior to implantation, 10 nm of PECVD SiO_2 is deposited on the Ge surface to ensure shallow implantation. The implanted Ge is annealed in a rapid thermal annealing tool at 600 °C for 1 min.[40]

Germanium Preparation. It is essential that the Ge substrate remain particle-free to avoid trapping particles at the interface. Once diced or cleaved, the brittle edges of germanium become a persistent source of particle contamination, so whole 2 in. wafers are used whenever possible. Just prior to transfer of the nanomembrane, the deposited and native oxides on the Ge are removed in a mixture of $HF/HCl/H_2O$ (1:1:10).[41,42]

Thermal Annealing. Bonded pairs are heated directly on a programmable hot plate or in a convection oven in nitrogen ambient. The temperature is ramped from 100 to 400 °C at a rate of 5 °C/min, held at 400 °C for 30 min, and ramped down to 50 °C at the same rate. No pressure is applied to the sample during the annealing step.

Mesa Device Fabrication. We define 100 μm × 100 μm mesas of Ge and Si with optical lithography and reactive-ion etching using $CF_4 + O_2$. We then deposit 90 μm × 90 μm metal contacts pads of 500 Å/5000 Å Ti/Au by evaporation onto the mesas and use a standard lift-off technique. No contact annealing was performed.

All fabrication processes are carried out in a Class 100 clean room to avoid particulate contamination.

Electrical Measurements. *I*−*V* measurements were performed on a probe station using a Keithley 2400 Source Metering Unit. The current range of the measurement was −100 to +100 mA, limited by the compliancy of the instrument. To establish precision, the bias was swept back-and-forth 10 consecutive times with alternating polarity. The relative error was determined by dividing the standard deviation by the average of the measurements at a given point. ac conductance measurements were made using an Agilent 4284A Precision LCR Meter. The ac signal amplitude was 10 mV, and a dc bias across the device was swept from −10 to +10 V. The ac frequency was varied from 100 Hz to 1 MHz but held constant during each voltage sweep. The measured admittance was decomposed into conductance and susceptance. The conductance was essentially independent of frequency; however, the measurements are typically made at 10 kHz to reduce coupling with parasitic impedance.

The series resistance of a test device is estimated by measuring the slope of the dc *I*−*V* curve at high bias or by measurement using the ac impedance meter. The measured

complex impedance is decomposed into resistance and reactance components. The series resistance depends on the measurement instrument, method of connection, and current path, as this is a two-terminal measurement.

Cross-Sectional Transmission Electron Microscopy (XTEM). The XTEM samples were prepared by mechanical polishing and ion milling. The samples were initially thinned to 8−10 μm *via* mechanical polishing and dimpling with diamond lapping films. The samples were further thinned with Ar^+ ion milling to make them electron transparent. The ion milling energies were progressively reduced (from 4 to 1 keV) to minimize the depth of the amorphous layer on the surface of the sample. The samples were characterized on a Philips CM200 TEM with a 200 keV operating voltage.

The twist angle between the Si NM and the Ge substrate was obtained by measuring the tilt angle between the (110) zone axis of the Si NM and the (130) zone axis of the Ge substrate. The twist angle was then extrapolated from knowledge of the actual angle between the (110) and (130) zone axes. Any miscut from the [001] direction of the surface of the Si NM or the Ge substrate was not accounted for in determining the approximate twist angle.

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