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Simulation based performance comparison of transistors designed using standard photolithographic and coarse printing design specifications

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ABSTRACT

In this work a simulation based comparative study of organic field effect transistors designed using standard lithographic and printing designs is presented. The device simulations were performed using two-dimensional drift-diffusion equations with a Poole–Frenkel field dependent mobility model. Both photolithographic and coarse printing transistor designs employed common materials such as 150 nm thick pentacene, 150 nm thick parylene gate insulator, gold source-drain electrodes and aluminum gate electrodes. The major differences between the two fabrication specifications are the minimum source/drain line width and the transistor channel length. The typical specifications for the minimum line width and channel length were 2 μm and 5 μm for photolithography and 25 μm and 20 μm for coarse printing techniques, respectively. The gate, source, and drain capacitances and channel on-resistances at various channel lengths and gate overlaps have been extracted and presented specifically for both process schemes. Due to increased channel length and gate-source/drain overlap of printed electrodes relative to lithographic design, the resulting on-resistance and capacitances for coarse printing are significantly higher. These results demonstrate a substantial operating frequency reduction for printing design relative to photolithographic design. For the tested materials and designs it is shown that the cut-off frequency for the photolithographic process was 400 kHz but decreased to a much lower 26 kHz for the coarse printing process. Since printing technology uses various other materials, which typically have less performance than the ones used for this simulation, the actual printed device might have even lower performance than predicted here.

1. Introduction

Currently, a variety of fabricating techniques have been used by different research groups to fabricate organic field effect transistors. Some of the most common methods are spin coating, lithography, thermal evaporation, and direct printing [1–3]. Each technique has different advantages and disadvantages in regard to resolution, registration, process temperature, and device performance. For example, the use of conventional lithography is advantageous to get a non-destructive, high-throughput, minimum registration, and high-resolution patterning. However photolithography, when compared with printing, exhibits higher production costs and process time [4]. On the other hand the development of a solution-based process on a flexible substrate would allow roll-to-roll fabrication [5]. Since it eliminates complex substrate processing procedures, such as vapor phase deposition and etching, printing process is an inexpensive option for mass production of circuits.

Photolithography has been the widely adopted technology used to fabricate electrode/contact materials in both top-contact and bottom-contact organic thin film transistors (OTFT) [6]. It is a process in which the patterns are transferred onto a substrate with the help of optical sources similar to the processes involved in lithographic printing. In a top-contact, the source/drain electrodes are usually deposited on the top of the semiconductor and then the photoresist is applied prior to the consequent processes of exposure, development, etching and resist removal. On the other hand in the bottom-contact OTFT, the source/drain electrode materials are deposited on the insulator layer, due to which the semiconductor layer has to be deposited on both the insulator and the electrode materials after the photolithographic process [7].

Photolithographic process for deposition of organic semiconductors has noted problems because of the damage and degradation done to the semiconductor due to the chemicals involved in the etching and developing steps [7]. Hence the deposition process used in majority of

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14. ABSTRACT

In this work a simulation based comparative study of organic field effect transistors designed using standard lithographic and printing designs is presented. The device simulations were performed using twodimensional drift-diffusion equations with a Poole?Frenkel field dependent mobility model. Both photolithographic and coarse printing transistor designs employed common materials such as 150 nm thick pentacene, 150 nm thick parylene gate insulator, gold source-drain electrodes and aluminum gate electrodes. The major differences between the two fabrication specifications are the minimum source/ drain line width and the transistor channel length. The typical specifications for the minimum line width and channel length were 2 μm and 5 μm for photolithography and 25 μm and 20 μm for coarse printing techniques, respectively. The gate, source, and drain capacitances and channel on-resistances at various channel lengths and gate overlaps have been extracted and presented specifically for both process schemes. Due to increased channel length and gate-source/drain overlap of printed electrodes relative to lithographic design, the resulting on-resistance and capacitances for coarse printing are significantly higher. These results demonstrate a substantial operating frequency reduction for printing design relative to photolithographic design. For the tested materials and designs it is shown that the cut-off frequency for the photolithographic process was 400 kHz but decreased to a much lower 26 kHz for the coarse printing process. Since printing technology uses various othermaterials,which typically have less performance than the ones used for this simulation, the actual printed device might have even lower performance than predicted here.

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the organic devices has been limited only for fabrication for electrode regions. OTFTs fabricated through photolithography process attained resolutions as low as 5 μm [8]. Although photolithographic processing of electrodes was proven to produce high quality OTFT devices with field effect mobilities as high as 1 cm^2/Vs, the technique is comparatively expensive due to the extensive and time-consuming processing steps involved. These constraints lead to the investigation of many low cost techniques to fabricate electrodes in OTFTs out of which printing was found to be a promising one.

The increasing interest in organic devices fabricated via printing techniques is due to the low cost involved in realizing flexible electronics. The use of printing techniques in OTFT fabrication eliminated many expensive procedures involved in lithography, PVD, CVD, plasma etching etc. Many researchers reported the use of printed electrodes as gate electrodes or source/drain electrodes in bottom-contact and top-contact OTFT architectures [9,10]. Many printing techniques have been used to develop OTFT electrode regions and each one varied in the overall resolution and channel length. Table 1 depicts the typical ranges of layer thickness, line width and channel length for various printing techniques.

Among the well developed printing techniques shown in Table 1, inkjet printing has emerged as an attractive direct patterning technique. This is mainly because fully data driven and maskless drop-on-demand inkjet processing is more versatile than other direct printing methods [3]. Despite all its advantages, the resolution of the inkjet process is limited to the order of 20–100 μm [10,13]. Another drawback for the inkjet printing process is that the material employed for electrodes and interconnects is typically a conducting polymer that has intrinsically higher resistivity than metals [10,13,14]. High-resolution and low-temperature metal deposition methods that do not require photolithography or vacuum processes are not yet well developed. Secondary techniques like laser ablation can also be used along with printing techniques to fabricate very high-resolution (~5 μm) OTFT electrodes. Table 2 summarizes the common electrode materials that were reported to be printed using inkjet technology. While it is obviously possible to use different techniques for different layers of the device, the use of a single printing technique for whole arrays should minimize the cost of fabrication and reduce the complexity of device processing.

One of the main requirements of inkjet printing process is the availability of solution processable materials [22]. The solubility is an important organic material property for solution based processes. However charge carrier mobility in organic material tends to decrease as solubility increases [23]. Mobilities recorded for high soluble organic materials were lower than 0.1 cm^2/Vs [24]. Recently newer processing schemes are being employed using organic material precursors with low mobilities but have excellent solubility. When, after a solution inkjet process, they are annealed slightly 100 °C to 200 °C it is found that the precursor will have converted through chemical reaction to a derivative that has significantly higher mobility (nominally on the order of 0.1 cm^2/Vs). This concept was first introduced by the Subramanian Group in 2003 [25] with pentacene and a pentacene precursor. Notwithstanding the significant improvements in mobility from this relatively new approach there are doubts that such a process will be able to surpass in performance the bulk vacuum deposited material. This is because the anneal process required for conversion of the precursor tends to introduce intramolecular disorder which lowers mobility.

Table 1
Typical ranges for device resolution in various printing techniques.

Printing technique	Layer thickness (μm)	Line width (μm)	Channel length (μm)
Inkjet	0.1–20 [11]	20–100 [7]	40–400 [7]
Screen	1–15 [11]	100 [7]	100–200 [7]
Flexography	0.2–2.5 [11]	50–100 [12]	–
Pad	1–2 [7]	>100 [7]	20–60 [7]
Offset	0.5–1.5 [7]	100–200 [7]	30–200 [7]

Table 2
List of various materials for inkjet printing techniques.

Device	Material printed	Type of printing	Reference
TFT	PEDOT:PSS (gate, S/D)	Inkjet	[10,15]
TFT	Ag (S/D)	Inkjet	[16]
TFT	Ag (Gate)	Inkjet	[17]
TFT	Ag nanoparticles	Inkjet	[18]
TFT	Au nano particles	Inkjet	[3]
TFT	Cu nanoparticles	Inkjet	[19]
Semiconductor materials			
TFT	TIPS-pentacene	Inkjet	[16,20]
TFT	P3HT	Inkjet	[3]
Dielectric materials			
	PVP	Inkjet	[21]
	Organic–inorganic hybrid dielectric	Inkjet	[17]

As discussed above, significant research has been done mostly devoted to developing and optimizing the process flow of both printing and photolithographic fabrication technologies and selecting materials compatible to the processes. Transistors fabricated with those technologies have also been tested for various circuits and applications [25–33]. However, there is only limited research performed on a direct comparison of device performances with a focus on the differences between layout design rules of the two technologies using same materials. Didane et al. [34] reported performance variations of thin film transistors based on fabrication methods as well as device configuration. Critical transistor parameters such as the charge mobility and the threshold voltage have exhibited significant variability between vapor deposition, spin coating, drop casting, and inkjet printing fabrication techniques as well as between top-contact and bottom-contact device configuration. But photolithographic fabrication technique was not included in their study. In this work we focused on a comparison of two major fabrication techniques (inkjet printing and photolithography) and followed a different approach of performance analysis. Bottom-contact organic field effect transistors designed based on standard photolithographic and inkjet printing design rules have been simulated and compared. Design rules have been taken from the literature. The work is intended to study how the performances of the transistors differ from each other because of the change in the design rules only. In this regard, the reported materials such as pentacene, parylene, gold, and aluminum have been used. Also presented is the parallel study on the impacts of layer registration, channel length, and source/drain width on device performance.

2. Simulation details

Specific design rules and device structures adapted from our process flow for photolithographic design have been used for the simulation. The design specifications for inkjet printing process are taken from literature [7]. Table 3 summarizes the design specifications of both technologies that are used in this work. The cross-sectional view of the transistor is shown in Fig. 1. The material and model parameters used in the simulation are listed in Table 4. The simulation

Table 3
Design specifications of lithographic and printing techniques.

Technology	Channel length (μm)	Source, drain length (μm)	Maximum gate length (μm)	Channel width (μm)
Photolithography	5	2	75	200
Inkjet printing	20	25	90	200

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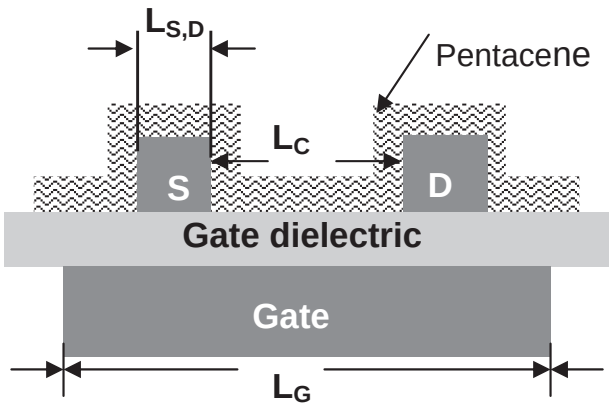

Fig. 1. Cross-sectional view of device structure. Figure is not drawn to scale.

was performed using the standard Poisson, continuity, and drift-diffusion equations as implemented in ATLAS device simulator [35]. Most organic semiconductors have a disordered structure in both position and energy. The experimentally observed linear relation between *log(μ)* and $\sqrt{E}$ in disordered organic systems is modeled by the Poole–Frenkel transport model (1) [35–37].

$$\mu(E) = \mu(0)\ exp\left(\frac{\beta\sqrt{E}}{kT}\right) \quad and \quad \mu(0) = \mu_i\ exp\left(-\frac{\Delta}{kT}\right) \tag{1}$$

where $\mu(E)$ is the field dependent mobility, E is the electric field, β is the Poole–Frenkel factor, μ_i is the intrinsic mobility, and Δ is the zero field thermal activation energy. This Poole–Frenkel mobility model was employed for pentacene active material. Parylene gate insulator, gold source-drain electrode and aluminum gate electrode have been used. A fixed interface charge density of $3\times10^{11}\ cm^{-2}$ between pentacene and parylene was considered for the simulation. The interface charges are supposed to be formed during the fabrication process of the device. Since the charges are fixed at the interface they are gate voltage independent.

3. Results and discussion

3.1. Impact of gate electrode length on performance of the devices

Field effect transistors are formed by depositing successive layers of materials on top of one another to form the complete device. These successive layers should be aligned only within some corresponding tolerance. The semiconductor industry refers to such layer alignment tolerance as layer-to-layer registration. In the case of a transistor, the channel typically needs to be aligned over a gate electrode such that no part of the channel resides unaligned with the gate electrode. Traditional silicon wafer fabrication techniques often employ a self-aligning gate technique to effectively reduce such non-alignment to zero. Masks are used to implement this technique; however, these are not useful in a printing context. To meet this requirement, typical printing techniques would suggest increasing the size of the gate region to ensure a result consistent with expected registration tolerances. Unfortunately this also requires overlap between the gate electrode and the other electrodes of the transistor (such as the drain electrode and the source electrode). And this, in turn, gives rise to undesirable parasitic capacitances that slow down the switching speed of the transistor itself.

To study the effect of the gate electrode length and its overlap with the channel and source-drain contacts, transistors have been simulated at different gate lengths. For cases (A), (B) and (C) below, the gate electrode length is systematically selected according to guidelines defined in terms of the channel length and the source-drain electrode lengths. For case (D) the electrode gate length is set to the maximum device length as defined in Table 3.

A) $L_G = L_C$: length of gate electrode is exactly equal to channel length.
B) $L_G = L_C + L_{S,D}$: gate electrode extends half way from the source to half way the drain.
C) $L_G = L_C + 2L_{S,D}$: gate electrode extends from outside edge of the source to outside edge of the drain.
D) L_G = maximum gate length: gate electrode covers the entire device size as mentioned in Table 3.

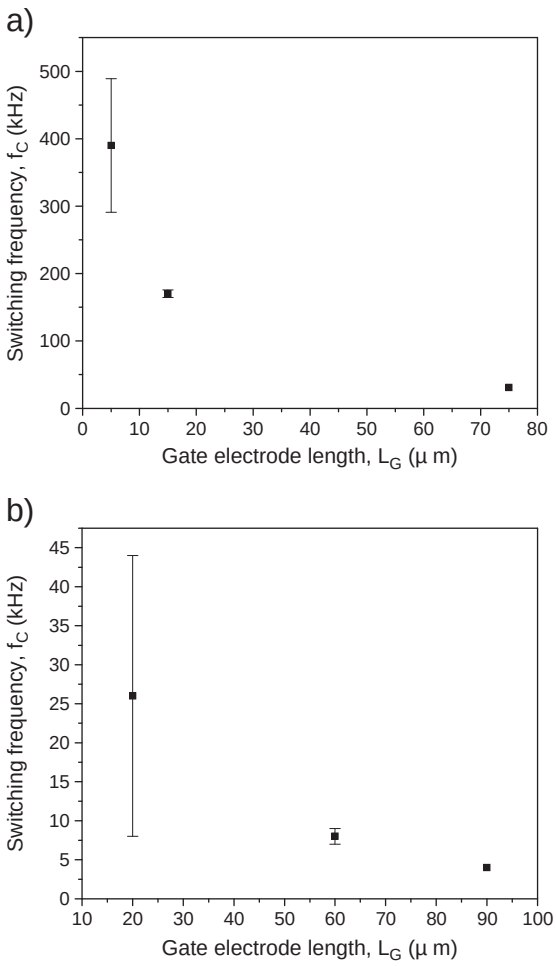

Fig. 2. Switching frequency of the transistors at different gate electrode lengths for a) lithographic and b) printing designs.

Table 4
Material and model parameters used in the simulations performed at T = 300°K.

Pentacene	Band gap	2.2 eV
	Thickness	150 nm
	Affinity	2.7 eV
	Permittivity	3.0
	Nc, Nv	$2.4\times10^{21}\ cm^{-3}$
	Acceptor trap	$2.4\times10^{17}\ cm^{-3}$
	μ_i	$0.1\ cm^2/Vs$
	Δ	0.16 eV
	β	$4.37\times10^{-5}\ eV(cm/V)^{1/2}$
Parylene	Thickness	150 nm
	Permittivity	3.0
Gold	Work function	5.1 eV

Table 5
Simulated and extracted transistor parameters of lithographic and printing techniques for different gate electrode lengths (A: $L_G = L_C$; B: $L_G = L_C + L_{S,D}$; C: $L_G = L_C + 2L_{S,D}$; D: L_G = maximum gate length).

Parameters	A			B			C			D		
	C_G (pF)	I_{DS} (μA)	f_C (kHz)	C_G (pF)	I_{DS} (μA)	f_C (kHz)	C_G (pF)	I_{DS} (μA)	f_C (kHz)	C_G (pF)	I_{DS} (μA)	f_C (kHz)
Photolithography	0.11	33	390	0.19	33	240	0.27	33	170	1.4	33	31
Inkjet printing	0.43	6	26	1.3	6	8	2.24	6	5	2.44	6	4

The summary of simulated values of the gate capacitance, the drain current, and the switching frequency for different gate electrode lengths for both design rules is provided in Table 5. From the table we can observe that as the length of the gate electrode increases from Lc (the size of the channel) to the full length of the device, the gate capacitance increases from 0.11 pF to 1.4 pF for lithographic design and from 0.43 pF to 2.44 pF for printing design. This increase in capacitance decreases the operating frequency of the devices dramatically. The switching frequency was calculated from Eq. (2) [38]

$$f_C = \frac{1}{2\pi C_G R_{ON}} \tag{2}$$

where C_G is the total gate capacitance extracted from the simulation and R_{ON}, as discussed later in Section 3.2, is the channel on-resistance of the device. When comparing the switching speed of the transistors from the two designs at a gate electrode length equal to the length of the respective channel, the transistor for photolithographic design was found to be 15 times faster than the printing design. In both design methodologies, variation in the gate length does not show significant impact on the drain current. This implies that the channel on-resistance is insensitive to the variations in gate length. As shown in Table 5, the saturation drain current for photolithographic design is increased by a factor of 5.5 relative to the saturation current for the printed transistor design. However, under the ideal long channel (metal-insulator-semiconductor field effect transistor) MISFET saturation model the current ratio would only be a factor of 4 as per square law rule given by

$$I'_{DS(SAT)} = \frac{W}{2L_c} C_i \mu (V_G - V_T)^2 \tag{3}$$

where $I'_{DS(SAT)}$ is the ideal long channel model saturation drain current, W is the channel width, $L_c$is the channel length, C_i is oxide

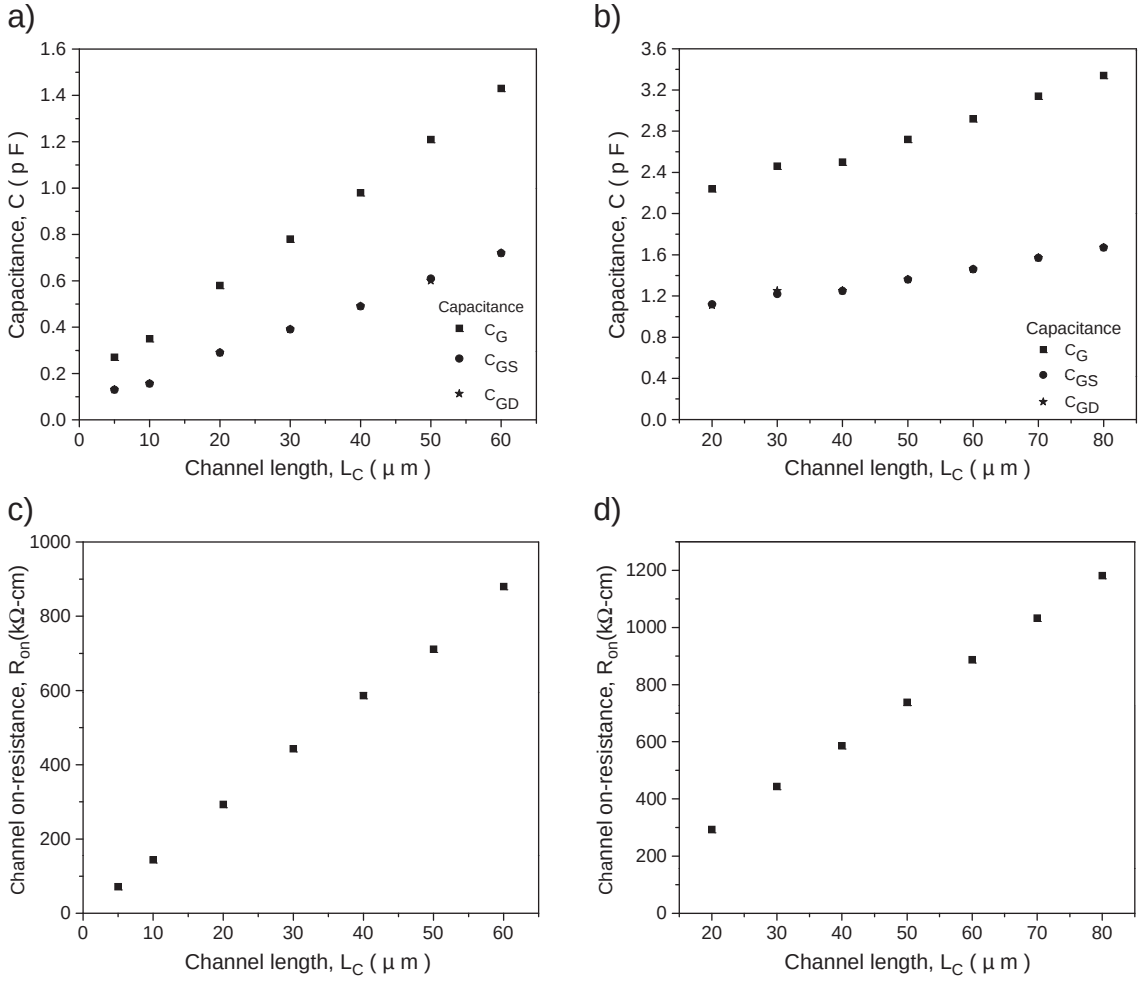

Fig. 3. Gate, source, and drain capacitances of (a) lithographic design and (b) printing design; channel on-resistances of transistors (c) lithographic design and (d) printing design.

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capacitance per unit area, μ is the constant channel mobility, V_G is the gate voltage, and V_T is the threshold voltage. In practice OTFT parameters are frequently extracted using this equation by fitting with experimental data.

On the other hand Eq. (3) will not account for the deviation from ideal MISFET behavior that is often observed in the current-voltage characteristics of organic thin film transistors [39]. It should be noted that Eq. (3) is derived based on two major assumptions. The first assumption is that the charge mobility is assumed to be constant in the channel. The second assumption is that the device is a long channel transistor so that the gradual channel approximation is applicable.

In regard to the first assumption two physical processes can be important for the invalidation of the constant mobility assumption. For organic materials the Poole–Frenkel transport model leads to an increase in the mobility, and corresponding increase in current with the electric field created by the applied drain-source voltage. A second less pronounced impact is created by the phenomena known as velocity saturation which occurs for both organic and inorganic transport. This would lead to a reduction in the transport mobility and corresponding reduction in current. Velocity saturation effect is typically considered second order in organic materials, relative to the previously mentioned Poole Frenkle effect. Physical arguments supporting this conclusion are related to the low-field mobility values symptomatic of organic transport. There is however significant evidence [39–41] that the velocity saturation effect should not be completely ignored in OTFTs for purposes of obtaining a close agreement between predicted and experimental transistor characteristics. The dominant Poole–Frenkel effect explains in part the elevated current ratio 5.5 previously noted.

The second assumption is that Eq. (3) assumes the validity of the gradual channel approximation (GCA) for which the gate voltage induced (transverse) field is required to be high compared with the drain-source voltage induced (longitudinal) field

$$\frac{V_{GS}}{t_i} >> \frac{V_{DS}}{L_c} \tag{4}$$

where t_i is the insulator thickness. The GCA is expected to be closer to being invalid in the photolithographic design, than printing process design, due to the shorter photolithographic channel length $L_c = 5.0\,\mu m$. Using in addition $Vg = -30\,V$, $Vds = -35\,V$, and $t_i = 150\,\mu m$ confirms that GCA is not violated for the photolithographic transistor design and therefore also not violated in the printed transistor design. In practice, it has been reported that short channel effects have been observed in conditions where the gradual channel approximation should be valid [42], which is true in our case too. One of the short channel effects is a slow increase of the drain current in the saturation regime. This short channel effect is often modeled according to the semi-empirical rule [42] given by

$$I_{DS(SAT)} = I'_{DS(SAT)}(1 + \lambda V_{DS}) \tag{5}$$

where λ is known as the channel length modulation parameter, V_{DS} is the drain-source voltage, V_G is the gate voltage and V_T is the threshold voltage.

The results of the switching frequency analysis indicate that the best speed performance is attained if the gate electrode is limited between the source and drain. However this requires the precise control of the gate electrode width to avoid undesired performance variations between transistors fabricated with the same process. Performance variations between similar transistors are undesirable phenomenon particularly for analog circuit applications. This will be more challenging for printing fabrication, which has less control of thicknesses and widths of the different layers. Even though sub-micron level layer-to-layer registration can be achieved in photolithographic design [43], the registration in printing design is in the order of 5 μm [43,44]. To compare the performance variability of the two design rules, which comes from the gate width variability, we have simulated the transistors by introducing a ±5 μm and ±0.5 μm variation of the gate electrode length for printing and lithographic design rules respectively. The simulations have been performed for three cases: 1) when the gate electrode is limited between the inside edges of the S/D electrodes (case A in Table 5); 2) when the gate electrode is limited between the outside edges of the S/D electrodes (case C in Table 5); and 3) when the gate electrode extends to the full size of the device (case D in Table 5). The first observation from simulations is that the highest percentage variability in gate capacitance, drain current and switching frequency resulted when the gate electrode is limited between the inside edges of the S/D electrodes and the variability diminishes as the gate length increases beyond the channel. The second observation is that photolithographic design has shown less percentage variability than printing design in all device parameters we have studied such as gate capacitance, drain current, and switching frequency. Particularly the change in the drive current for the printed transistor is significant when the gate electrode does not fully cover the channel length. When the gate electrode uncovers 5 μm of the channel on the source side and 5 μm of the channel on the drain side, the current drops to nano-amps. The current is normally in micro-amps when gate electrode length exactly matches the channel length. Plots of switching frequencies which summarize the above mentioned observations are given in

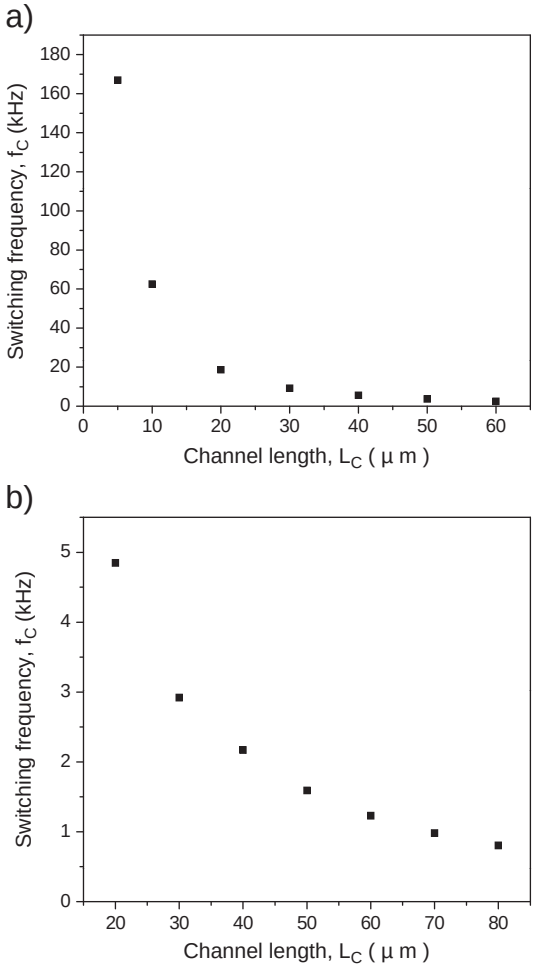

Fig. 4. Switching frequency of transistors at different channel lengths (a) lithographic design, (b) printing design.

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Fig. 2. The variations in switching speed correspond to variations in electrode length.

3.2. Impact of channel length on performance of the devices

The ability to define high-resolution gaps helps to design short channel length transistors which have low capacitances and low channel on-resistances. Not only the resolution but the precise control of the channel length is also an important criterion to fabricate transistors for intended circuit functionality.

The length of the channel is critical since it is directly related to the speed and the drive current of the device. The maximum on-current scales linearly with 1/L for a given transistor [45]. The response speed of the transistor is also affected by gate capacitance and channel on-resistance [39]. A slight error in registration of the channel masks results in additional gate capacitance and channel on-resistance which diminish the response speed of the transistor.

To predict the impact of channel length on transistor performance we have simulated transistors at different channel lengths. The source/drain length ($L_{S,D}$ in Fig. 1) was kept at 2 μm and 25 μm for the photolithographic and printing designs respectively. The gate length was kept between the outside edges of the source and drain electrodes, i.e. $L_G = L_C + 2L_{S,D}$ for both designs. The gate, source, and drain capacitances of the transistors as a function of channel length are given in Fig. 3a) for lithographic design and b) for printing design. The channel on-resistance (R_{on}), which is the sum of the channel resistance (R_{ch}) and the source-drain contact resistance (R_c), was calculated from the slope of the transfer characteristics of the transistors in the linear region [46,47] (Eq. (6)).

$$R_{on} = \left.\frac{\partial V_{ds}}{\partial I_{ds}}\right|_{\left(V_{gs}, V_{ds\to 0}\right)} = R_{ch} + R_c \tag{6}$$

Fig. 3c) and d) shows the channel on-resistances at different channel lengths for lithographic and printing designs respectively. As expected the capacitances and resistances show a linear relation with the channel length [7]. But those capacitances and resistances of printing design are significantly higher than those of the photolithographic technique. This results in a significant difference in switching frequency between the two designs. Fig. 4a) and b) presents the switching frequency at different channel lengths for lithographic and printing designs respectively. As shown in the figures, the maximum operational frequency of printing design is 2 orders of magnitude less than that of the photolithographic design. This maximum switching frequency corresponds to the minimum channel length in each design. For both designs the speed drops significantly as the channel length increases.

3.3. Impact of source-drain (S/D) electrode length on device performance

Performance of organic thin film transistors is controlled by electrodes and device structures. A high-resolution gate or source/drain electrode does require precise control of length, width and thickness

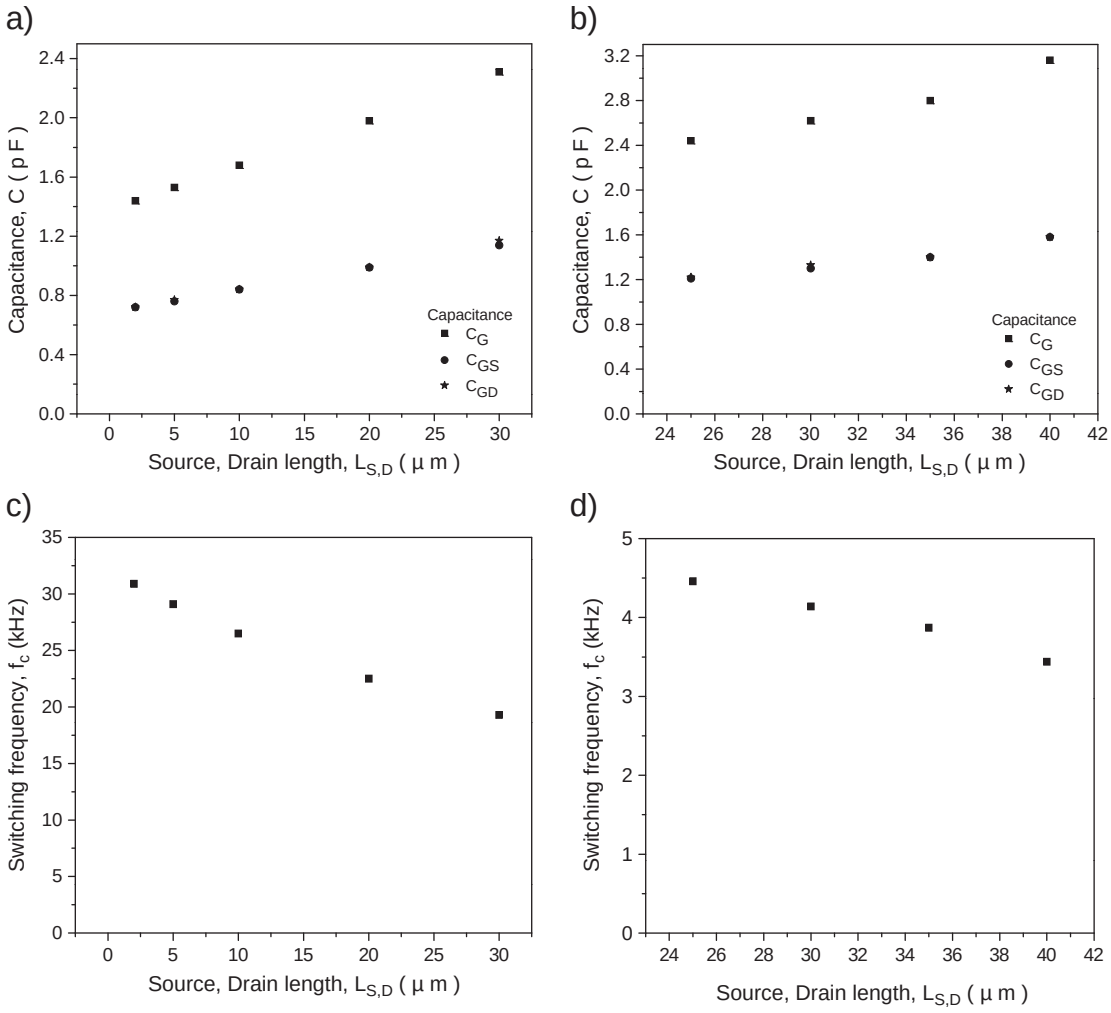

Fig. 5. Gate, source, and drain capacitances of (a) lithographic design and (b) printing design; switching frequency of transistors (c) lithographic design, (d) printing design.

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of these electrodes for performance optimization. To predict the impact of S/D electrode length ($L_{S,D}$) on transistor performance, transistors with various $L_{S,D}$ for both design rules were simulated. During the simulation, $L_C = 5\ \mu m$, $L_G = 75\ \mu m$ for photolithography and $L_C = 20\ \mu m$, $L_G = 90\ \mu m$ for printing design.

The gate, source, and drain capacitances of the transistors as a function of channel length are given in Fig. 5a) for lithographic design and b) for printing design. The capacitances show a linear relation with S/D length. This linear relation between the capacitance and the S/D length results an inverse relation between the switching frequency and the S/D length. Fig. 5c) and d) shows the switching frequencies of the transistors at different S/D lengths for lithographic and printing designs respectively. The switching frequency decreases as $L_{S,D}$ increases. The channel on-resistance was insensitive to the S/D length variation. As a result the simulation did not show an impact of S/D length on drain current.

4. Conclusion

The printed transistors were designed with higher channel lengths and higher gate-source and gate-drain overlaps relative to the corresponding photo lithographically designed transistors. As a consequence the printed transistors had higher gate-source and gate-drain capacitances as well as higher channel on-resistances. The channel on-resistance was 72 kΩ cm for photolithography and 292 kΩ cm for printing designs. For the gate length kept at the size of the channel, the gate capacitance increased from 0.11 pF for lithography to 0.43 pF for printing designs. This significant difference in capacitances and resistances results in a substantial difference in switching frequency. The cut-off frequency decreased from 400 kHz for lithographic transistor to 26 kHz for printed transistor. In addition, performance differences of transistors from the two fabrication techniques might also come from material differences as well. In order to put the focus for performance differences on the design rules the photolithographic compatible materials were also used in the printed transistor design. This is notwithstanding that compatible actual materials used for printing would typically have less desirable material properties in terms of electrical performance.

The results on the impact of gate electrode variability on transistor performances indicated highest performance variability for short gate electrode lengths i.e. when the gate electrode is limited to the size of the channel. The impact is higher for printed transistors since printing has higher layer-to-layer registration and thickness variability. The impact of the electrode width variability decreases as the gate electrode extends beyond the size of the channel.

In general the simulation studies presented here show a clear difference in performance between the transistors designed using lithographic and printing designs. Due to material differences between the two fabrication techniques, the actual printed device might even have lower performance than predicted here. Although the photolithographic approach is more costly than printing with the typical design rules it should have a significantly better performance. This indicates that in choosing between the two fabrication techniques, printing versus lithography, one has to compromise between cost and performance.

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