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Intelligent Automation Incorporated

Coherent distributed radar for high-resolution through-wall imaging

SBIR Phase I Final Technical Report

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Summary

This report details progress in the FY10 period of performance on development, implementation and testing of hardware and algorithms for highly accurate wireless synchronization.

1.0 INTRODUCTION

In this report we discuss progress accomplished in FY10 period of performance in hardware design, synchronization algorithm, and definition of the final demonstration. FY10 work has largely focused on 1) redesigning the hardware to achieve higher synchronization resolution and accuracy, increase the operational distance between synchronization transceivers, and increase robustness to interference, and 2) Complete Matlab simulations of the entire synchronization algorithm, for cases where the synchronization transceivers are moving, and significant multipath reflections are present in the channel.

1.1 Hardware design

RF front-end

Part of the hardware design and implementation was supported by other efforts at IAI using the same hardware design. During FY10, we initiated and completed the design, schematics, and layout of entire new RF front-end for the synchronization receiver. While we have not characterized the receiver yet, the goal of its design is, compared to the first prototype developed for ONR, to reduce noise in the receiver, increase the transmit power, allow for half-duplex operation, allow flexibility in the operating frequency (by changing filters) without the need for a change in layout, and minimize distortion of signal phase on both transmit and receive. In addition, hardware designs that allow real-time measurement of hardware delays were implemented; specifically grounding practices that increase isolation between transmit and receive circuits. The RF layout was sent out for manufacture, and will be tested in October, 2010. We show a picture of the RF front-end PCB

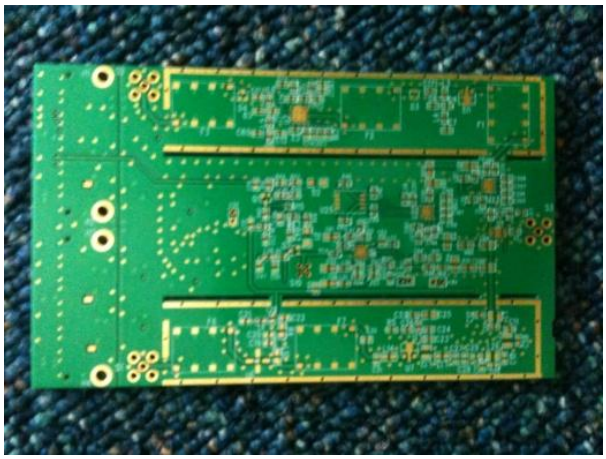

Figure 1. RF front-end for Synchronization receiver. The board is unpopulated.

Digital Transceiver

We started FY10 period of performance with a prior digital board design developed under an effort for the Air Force. This plug and play transceiver consists of a large FPGA, a high precision and flexible clock distribution circuit, and is capable of Direct Digital Synthesis up to L-band. In FY10, we selected, acquired, and tested a more accurate reference clock to interface to this design. We also designed a new ADC board with higher resolution, and higher clocking rates. We designed a frequency plan for the clocking rates of FPGA, D/As, and ADCs. The ADC board was manufactured and tested. The ADC board testing was completed, and has prompted a redesign to address problems with the analog input circuit, specifically level shifters. The redesign has been sent out for manufacture and the redesigned hardware testing will be completed in October, 2010. We show a picture of the digital receiver in Figure 2.

Figure 2. Digital transceiver

We have extensively tested the stability and tenability of the reference clocks used for the synchronization transceivers. We have developed an automated (using LabView) test set-up to accurately measure the frequency offset between two clocks, and used it to characterize the stability of the clocks over time scales varying from 0.05s to several hours. We have also studied the effect of power supply stability and accuracy on clock frequency accuracy and stability. We are using these results to select proper power supplies and tuning circuits to tune the clocks in the field. We show a picture of the LabView application, and two reference clock signals in Figure 3.

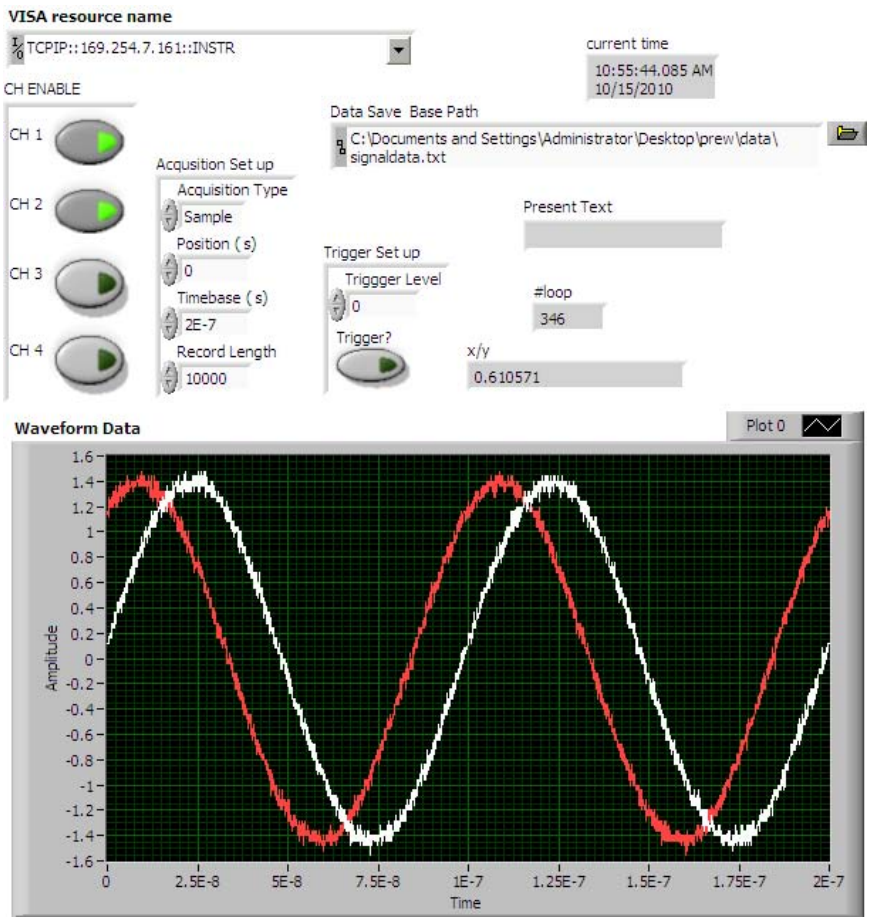

Figure 3. Screenshot of LabView application used to measure and correct frequency offset between two reference clocks

1.2 Synchronization algorithm

We have completed Matlab simulations of the estimated the performance of frequency estimation algorithm under varying SNR through simulations. We have also tested this algorithm using data collected on the digital transceiver in a loopback test, i.e. the transceiver transmits a tone and receives it simultaneously. For relevant achievable SNR values, and mobility consistent with hand-held radars, the accuracy of the frequency estimation algorithm is comparable to the tenability and stability of the reference clocks. This means that frequency estimation may not be needed during operation in the field more than once a day. To reduce the effort in implementing the frequency synchronization algorithm, we have decided to implement it outside the FPGA, in an external processor in floating point precision.

For time synchronization, we are now completing Matlab simulations of our synchronization of multiple moving nodes, in a multi-tap multipath channel. We have also started implementation of the time offset estimation algorithm in the digital hardware.

1.3 Preparation for final demonstration

We have accelerated the preparation of the final demonstration. We are redesigning a previously developed through-wall radar to be interfaced to our synchronization hardware. We are also planning

for manufacture of a second unit of this radar, so that we can demonstrate the improved cross range resolution afforded by using two separated, tightly synchronized radars.

3.0 CONCLUSIONS AND WORK PLANNED FOR NEXT REPORTING PERIOD

The next reporting period will focus on implementation of the time offset estimation algorithm in the digital hardware, characterization and testing of the RF hardware, specifically the achieved noise figure, and ability to accurately measure hardware delays. We will complete the definition of the final demonstration and present a schedule of activities remaining in preparation for the demonstration.

3.0 REFERENCES

None.

4.0 LIST OF SYMBOLS, ABBREVIATIONS, AND ACRONYMS