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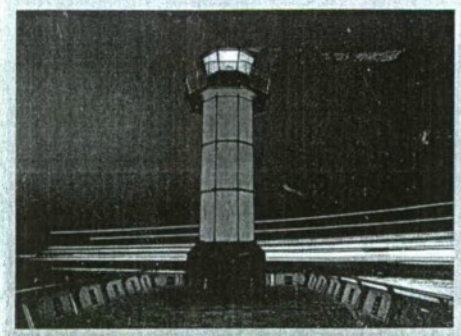

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CONVERGENCE OF III-V COMPOUND AND Si TECHNOLOGIES : PHOTONIC-ELECTRONIC CONVERGENCE

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Abstract

The convergence of III-V compound and Si technologies has been advanced toward the integration of photonics and electronics. III-V-on-Si epitaxy is overviewed from the viewpoint of defect control and device technologies for monolithic integration and future preospects are discussed.

I. Introduction

Photonic devices and LSIs have achieved revolution in information-communication and computing systems. However, it would be hard to expect the marked progress of both devices individually in the near future since their technologies have been matured. Photonic systems have the specific features of high-speed and high-capacity processing. The LSI is highly adaptive to various electronic systems and forms the core of computing systems. Thus, highly functional systems are expected when the photonic systems and the LSIs are implemented to a Si platform.

Various Si optical components , such as waveguides, ring resonators, couplers and others, have been developed with the fine processing technologies of the Si LSI. However, reliable light emitting devices such as semiconductor lasers have not been realized by utilizing GaAs and InP layers grown on a Si substrate. The convergence of III-V compounds and Si has been proposed even in the Si LSIs, in which a III-V compound and Ge are embedded as channel materials for electron and holes in CMOS LSIs, respectively [1].

Thus, the key technology of the conversion of photonics and electronics is the technology for the conversion of III-V compounds and Si including Ge. The epitaxial growth of III-V compounds on a Si substrate (III-V-on-Si) had been energetically studied over the world in the '80s. However, the prospect for growing dislocation-free III-V compound layers was hardly obtained. Around the start of 21 century, heteroepitaxial technologies for a dislocation-free III-V-on-Si were developed [2, 3]. On the other hand, technologies for wafer bonding and chip bonding have been developed for practical use, which keep defect-free III-V compounds [4].

In this plenary talk, we clarify firstly the main causes of problems and their countermeasures in the III-V-on-Si heteroepitaxy. Then, heteroepitaxy for dislocation-free III-V-on-Si and optoelectronic-device applications are overviewed. Finally, future prospects are discussed.

II. III-V-on-Si heteroepitaxy

A. Fundamental problems

The III-V-on-Si heteroepitaxy has the three following problems, as seen in Table 1:

(1) the difference in crystalline structures and the number of valence electrons;
(2) the difference in lattice parameters;
(3) the difference in thermal expansion coefficients.

Table 1. Material parameters of III-V compounds, Ge and Si

	Si	Ge	GaP	GaAs	InP	InAs
Lattice parameter (nm)	.54307	.56579	.54512	.56533	.58687	.60583
Thermal expansion coefficient ($\times 10^{-6}K^{-1}$)	2.56	5.90	4.60	6.86	4.75	4.52
Energy bandgap (eV)	1.12	0.66	2.26	1.42	1.34	0.36

As a result, the following structural defects are generated [5], as shown in Fig. 1(a):

(1) anti-phase domains (APDs) and stacking faults (SFs);
(2) misfit dislocations (MDs) and threading dislocations (TDs);
(3) glide dislocations

The generation of the APDs are due to single atomic steps on a Si (100) surface. The SFs are generated at the coalescence of growing islands which are formed on a chemically stabilized Si surface adsorbing As or P atoms. Pits are generated at an initial growth stage when Ga atoms react with a Si surface.

The MDs are generated in principle when the thickness of a growing III-V compound layer is over a critical thickness. In the growth of GaP-on-Si, the critical thickness is about 50 nm. The density of the MDs increases with the increase in

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the thickness of the GaP layer. The TDs are formed by the reaction of the MDs.

The glide dislocations could be introduced from a growing surface in a cooling process after the growth. This is due to a large tensile strain in III-V compound layers caused by large differences in thermal expansion coefficients.

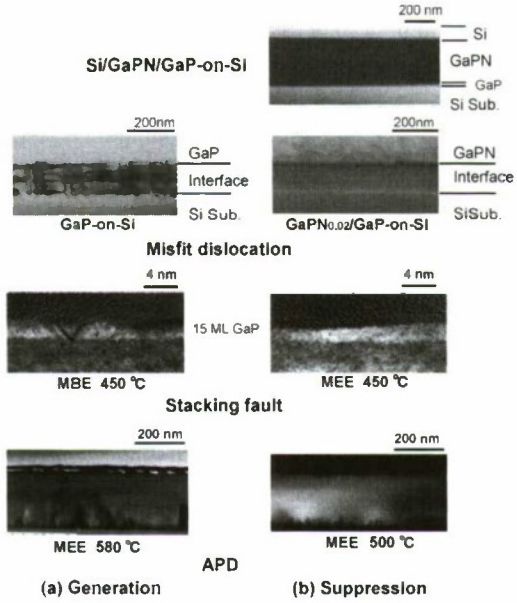

Fig. 1. Generation and suppression of structural defects in GaP-on-Si heteroepitaxy

B. Reduction in structural-defect density

The APDs are self-annihilated during the growth on Si (100) substrates misoriented toward the <110> directions [6, 7]. The density of the SFs can be decreased by enhancing two-dimensional growth. This was achieved by migration-enhanced epitaxy (MEE) in the growth of GaAs and GaP layers on a Si substrate [8]. The low-temperature (LT) MEE is more effective for suppressing the growth of the APDs. The generation of the pits was suppressed by decreasing the quantity of Ga atoms at the initial growth stage [9]. These countermeasures were applied to the growth of a GaP initial layer on a Si substrate in our lattice-matched dislocation-free growth mentioned below. The results are shown in Fig. 1(b). Similar results were obtained recently by alternately supplying TEGa and PH_3 in MOVPE [10].

Methods for the reduction in TD densities are classified into the three following methods. The TDs are mostly originated in the MDs generated on account of a lattice-mismatch.

(1) Suppression of generation and propagation

A buffer layer is grown before the growth of III-V compound layers. The lattice parameters are increased gradually or stepwise according to the growth by varying alloy compositions. For the stepwise buffer layer, the difference in lattice parameters is reduced [11]. Thus, the MD density is low compared with that in the growth without the buffer layer. As a result, the low TD density is realized. It should be noted that a TD-free III-V compound layer is hardly obtained.

(2) Threading dislocation bending

Dislocations tend to be moved and bent under mechanical stress at high temperature. For temperature cycling (TC), mechanical stress is induced by the large difference in thermal expansion coefficients between the III-V compound and Si. The dislocations are moved even in high-temperature (HT) annealing. The TD density decreased to around 1×10^6 cm^{-2} by applying the TC after growth in the growth of GaAs-on-Si [12].

(3) Dislocation-free growth

Lattice-matching is ideal for the dislocation-free growth. III-V-N alloys called dilute nitrides can be lattice-matched to Si since lattice-parameters decreased with the increase of N compositions [13]. We have grown a $GaPN_{0.02}$ layer on a Si substrate. A 20 nm thick GaP initial layer was grown on the Si substrate before the growth of the $GaPN_{0.02}$ for preventing the reaction of N atoms with a Si surface. The grown $GaPN_{0.02}$ layer was dislocation-free in principle. A Si capping layer can be grown on the $GaPN_{0.02}$ layer. Thus, the edge dislocation on a glide plane is prevented from being introduced from a Si surface since the tensile strain of the Si capping layer is negligibly small [3]. These results are shown in Fig. 1(b).

It was reported that the TDs disappeared after TC in GaAs and Ge layers grown selectively in a small area of around 10 μm squares on a Si substrate [14, 15]. A small number of TDs moved out of a grown area.

Lateral growth is also effective for the reduction in the TD density in liquid phase epitaxy (LPE), MBE and MOVPE. Laterally grown III-V compound (GaAs and GaN) layers contain a few dislocations since the TDs propagate upward from a selective area on a Si substrate [16, 17]. The surface of the Si substrate is covered with laterally grown layers when stripe areas are opened periodically through a SiO_2 layer on

Table 2. Defect generation and countermeasures

Difference between III-V compounds and Si	Structural defects	Countermeasures
Crystalline structure Number of valence electrons	APD SF (and Pit)	Misoriented Si (100) sub. LT-MEE (Initially less Ga supply) Alternately supply MOVPE
Lattice parameter	MD and TD	Buffer layer (Graded, Stepwise) Dislocation bending (TC, HT-annealing)
Thermal expansion coefficient	Glide dislocation	Si capping layer

the Si substrate. It should be noticed that areas at which the laterally grown layers coalesce contain highly dense dislocations. This technology has been practically applied to the growth of GaN layers on a sapphire substrate for the fabrication of reliable laser diodes [18]. The lateral growth of an InGaAs layer was reported, in which an InAs pillar was grown on a small area with a diameter of 2 μm on a Si substrate [19]. These results are summarized in Table 2.

In order to avoid the difficulties in the III-V-on-Si heteroepitaxy, wafer bonding has been developed. GaAs and InP wafers were bonded to a Si substrate with a SiO_2 layer in H_2 atmosphere at relatively low temperature. Ge wafers were also bonded to the Si substrate.

III. Device application

Laser diodes (LDs) are typical discrete optoelectronic devices. They were fabricated with a III-V compound epilayers grown on a Si substrate. For monolithic optoelectronic integrated circuits (OEICs), optoelectronic devices are formed in a III-V compound layers and electronic circuits are in a Si substrate or a Si epilayer.

A. Discrete devices

AlGaAs double heterostructure (DH) lasers and InGaAsP DH lasers were fabricated with III-V compound layers grown on a Si substrate. AlGaAs DH lasers showed marked degradation during operation since the III-V compound layers contained a high TD density around $10^6 - 10^8\,cm^{-2}$. InGaAsP DH lasers showed relatively stable operation at room temperature [20]. The lasers are less sensitive to the TDs in operation at room temperature. For a GaAsPN MQW laser, lasing was reported under optical pumping at low temperature [21]. The epilayers of the laser were lattice-matched to a Si substrate.

For photodetectors, Ge photodiodes (PDs) were fabricated on a Si substrate. An edge detection type is effective in coupling a waveguide on the Si substrate. For multi-junction solar cells, an InGaP/InGaAs/Ge structure achieved a high efficiency of around 40 % [22].

B. Optoelectronic integrated circuit (OEIC)

A monolithic OEIC was tried to be fabricated by using the GaAs-on-Si, in which an GaAs LED was driven by a MOSFET driver circuit implemented to the Si substrate [23]. It was not practical since highly dense TDs were contained in the GaAs epilayer.

We showed that monolithic OEICs can be implemented to dislocation-free epilayers of a Si/InGaPN/GaPN DH on a Si substrate covered with the 20 nm thick GaP initial layer [24, 25]. A process flow was basically the same as that for LSIs although process conditions were optimized for both III-V compounds and Si. InGaPN/GaPN DH LEDs and MOSFETs were fabricated anywhere in a chip. A monolithic OEIC was fabricated recently, in which a MOS counter circuit drove the LED, as shown in Fig. 2 [26]. The light emission with a peak wavelength of about 650 nm was observed according to counting results.

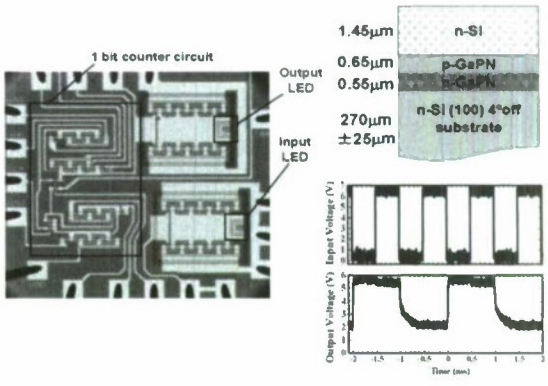

Fig. 2. A monolithic OEIC with GaPN LED and Si MOS counter circuit

Hybrid OEICs have been developed with the wafer bonding and the chip bonding. The silicon laser was fabricated by bonding an AlGaInAs MQW wafer to a Si waveguide wafer [27]. The MQW and the waveguide were coupled optically and an optical cavity was constructed by setting reflectors at both ends of the waveguide. Then 1.5 μm wavelength light emitted in the MQW is amplified in the Si waveguide by stimulated Raman scattering and lasing occurs. In high-speed LAN systems, various device chips, such as 1.5 μm InGaAsP LDs, Ge PDs and LSIs were bonded to a Si substrate with waveguides and electric wires.

IV. Conclusion

The conversion of photonics and electronics is based on the conversion of III-V compounds and Si. The causes of the fundamental problems of the III-V-on-Si heteroepitaxy have been clarified and the problems overcome. Defect-free heteroepitaxy has been under development. For lattice-matched heteroepitaxy, the increase in light emission efficiency of III-V-N alloys is a key issue since N atoms generate point defects. Small-area selective growth and quantum dot growth might be practical in lattice-mismatched N-free heteroepitaxy. Band edges are shifted by introducing N atoms with high electron affinity and by strain caused by a lattice-mismatch. These effects should be taken into account for the design of LDs [28].

Optical wiring in a LSI chip has been argued [29]. Parallel optical wiring between LSI chips could be realized by using monolithic OEIC technology. The wiring leads to massively parallel information processing for high performances. Photonic-electronic conversion systems would be constructed with monolithic OEICs , LSIs and optical systems bonded to a Si platform for ultimately high performance and low energy consumption.

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THE DARPA COSMOS PROGRAM: THE CONVERGENCE OF InP AND SILICON CMOS TECHNOLOGIES FOR HIGH-PERFORMANCE MIXED-SIGNAL

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ABSTRACT

The COmpound Semiconductor Materials On Silicon (COSMOS) program of the U.S. Defense Advanced Research Projects Agency (DARPA) focuses on developing transistor-scale heterogeneous integration processes to intimately combine advanced compound semiconductor (CS) devices with high-density silicon circuits. The technical approaches being explored in this program include high-density micro assembly, monolithic epitaxial growth, and epitaxial layer printing processes. In Phase I of the program, performers successfully demonstrated world-record differential amplifiers through heterogeneous integration of InP HBTs with commercially fabricated CMOS circuits. In the current Phase II, complex wideband, large dynamic range, high-speed digital-to-analog convertors (DACs) are under development based on the above heterogeneous integration approaches. These DAC designs will utilize InP HBTs in the critical high-speed, high-voltage swing circuit blocks and will employ sophisticated in situ digital correction techniques enabled by CMOS transistors. This paper will also discuss the Phase III program plan as well as future directions for heterogeneous integration technology that will benefit mixed signal circuit applications.

Index Terms — Si CMOS, InP HBT, heterogeneous integration, compound semiconductor, mixed signal circuit, ADC, DAC.

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I. INTRODUCTION

The development of compound semiconductor (CS) electronics has been motivated by their many superior materials properties relative to silicon. For example, high electron mobility and peak velocity of InP-based material systems have resulted in transistors with f_{max} above 1THz [1] as well as a 32 GHz direct digital synthesizer [2]. Wide energy bandgap GaN has enabled large voltage swing as well as high breakdown voltage power devices [3]. Excellent thermal conductivity of SiC also makes tens of kilowatt-level power switches possible [4]. Nonetheless, CS technologies have failed to displace Si in all but the most specialized electronic applications. This fact can be attributed to the aggressive device scaling and the extremely high levels of integration driven by Moore's Law over the past 50 years. Even for RF applications, where compound semiconductors are most commonly found, the advantages of compound semiconductors have been eroded by advances in silicon CMOS and SiGe heterojunction bipolar transistors. Recent RF CMOS [5] and SiGe HBT results [6] have driven the RF performance of silicon-based electronics well beyond what was previously thought realizable. Given these trends, it has been increasingly clear that the future of III-V electronics depends not on displacing Si, but rather on heterogeneous integration of compound semiconductors with silicon technology.

Heterogeneous integration of compound semiconductors with silicon has been explored in past decades [7], [8], but its main practical implementation today is through the use of multi-chip modules or similar assembly techniques. Multi-chip module techniques have been prevalent in various microwave/millimeter-wave RF systems, but performance for high-speed/bandwidth mixed-signal systems has been limited

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by I/O parasitic effects between chips in such modules and by device and interconnect variability issues.

The U.S. Defense Advanced Research Projects Agency (DARPA) COmpound Semiconductor Materials On Silicon (COSMOS) program focuses on developing *transistor-level* heterogeneous integration technologies which will overcome technical challenges such as accurate device-level placement, robust heterogeneous interfaces, dense heterogeneous interconnects (HIC), and high yield processes to enable heterogeneous integration at micrometer distance scales. If this vision can be achieved with high yield and at low cost, this revolutionary technology will allow circuits in which the optimum device is chosen for each specific function within an integrated mixed-signal microsystem. This capability will not only have significant impacts on the performance of both military and commercial circuits, but it also represents a new paradigm for the compound semiconductor community.

II. PROGRAM OBJECTIVES AND CHALLENGES

The objective of the COSMOS program is to develop a viable high-yield process for the transistor-scale heterogeneous integration of compound semiconductor devices with standard Si CMOS, thereby enabling superior performance in specific mixed-signal circuit demonstrators not possible in either device technology by itself. To this end, the COSMOS program seeks to integrate transistors from at least one CS technology, CMOS transistors, and back-end interconnect technologies on wafers fabricated using a standard Si CMOS foundry process. This must be achieved without any extraordinary modifications of the Si CMOS process.

The COSMOS program is exploring three different integration strategies in order to realize the program objectives. One approach, pursued by a team led by Northrop Grumman Aerospace Systems, involves sub-circuit integration in which III-V device "chiplets" are assembled onto a processed CMOS wafer with high-density [9]. At the other end of the spectrum, in an approach being developed by a Raytheon-led team [10], monolithic integration methods are being explored to epitaxially grow III-Vs on CMOS-compatible substrates. An intermediate approach is being studied by a team led by HRL Laboratories [11]. In order to achieve the challenging demonstration circuit performance goals, all three teams chose to integrate state-of-the-art InP HBTs with silicon CMOS transistors. In order words, the COSMOS program is developing a novel InP-based BiCMOS integrated circuit technology for the first time.

There are major technical challenges of these three fabrication approaches which have been addressed in the early phases of the program:

(1) *Placement of CS Devices*: A central problem is the capability to manufacture, position, register, and align "chiplets" or "islands" (~several μm on a side) of CS on a Si substrate.

(2) *Heterogeneous Material Interfaces*: A successful COSMOS implementation must address the coefficient of thermal expansion (CTE) mismatch which is expected to occur at this interface and potentially degrade device performance.

(3) *Dense Heterogeneous Interconnects:* To enable fine-scale integration, interconnects and vias must be defined with very short (~several μm) pitch separations without excessive electrical losses while maintaining high electrical isolation.

(4) *Yield Enhancement:* A high yield COSMOS process will be critical to enable the routine fabrication of heterogeneous integrated circuits with high reliability and low cost. The ultimate yield goal of the COSMOS technology is to match that of commercial Si technologies.

III. PROGRAM PLAN

To realize the COSMOS vision for mixed-signal applications, the program has established aggressive technical milestones as shown in Table 1. In the first Phase, COSMOS proved the feasibility of micrometer-scale heterogeneous integration process by realizing a simple demonstration circuit with minimal performance degradation of the CS and Si-based devices as a result of the integration process, i.e., < 10% reduction in transconductance of both types of transistors after heterogeneous integration. In the second Phase, the program will further reduce the length and pitch of heterogeneous interconnects for increasing complexity of the demonstration circuits. Ultimately, high yield, robust transistor-level heterogeneous integration processes will be developed with record-breaking mixed signal demonstration circuits.

Table 1. Key COSMOS Program Technical Metrics

Metric	Unit	Phase I	Phase II	Phase III
HIC* Length	μm	≤ 5	≤ 5	≤ 5
HIC Pitch	μm	≤ 25	≤ 5	≤ 5
HIC Yield	%	≥ 99	≥ 99.9	≥ 99.99
Demonstration Circuit		Diff Amplifier • Slew rate ≥ 10^9 V/μsec • Voltage swing ≥ 3V • DC gain * Unity-gain BW ≥ 10^4 V/V- GHz • Power ≤ 100mW	D/A Converter • Resolution ≥ 13 bits • SFDR ≥ 78 dBc (@ f_{output} = 1 GHz) • Power ≤ 2.5 W	A/D Converter • 16 SNR bits • 500MHz BW • SFDR ≥ 90 dBc • Power ≤ 4W
Circuit Robustness**	%	≥ 50	≥ 95	≥ 95

* HIC = Heterogeneous Interconnect
** Fraction of yielded circuits which remain yielded after 100 temperature cycles over a baseplate temperature range from –55 C to 85 C with dwell-time at each temperature extreme of at least ten minutes

In the first Phase of this program, the performers focused on transistor-scale integration technology, integrating CS and Si CMOS transistors within a small circuit on very short length scales (e.g. 5 μm HIC in length). The demonstration circuit was a heterogeneously integrated differential amplifier (DA), which provided both proof of the integration concepts, and world record characteristics compared to today's state of the art.

Phase II foeuses on yield enhaneement and eireuit integration. The objeetives of this phase are to signifieantly improve both the yield and the density of the heterogeneous intereonneet proeess. The speeifie eireuit demonstrator to validate performanee builds on the simple differential amplifier eoneept in Phase I but at a mueh higher level of eireuit eomplexity: a heterogeneously-integrated 13-bit digital-to-analog eonverter (DAC).

Finally, in Phase III the performers will demonstrate advaneed heterogeneous eireuits. The objeetive of this phase is to seale the COSMOS proeess to an even more eomplex mixed-signal eireuit, eonelusively demonstrating that fine-seale heterogeneous integration ean be realized on a large seale with high yield. The speeifie eireuit demonstrator to validate performanee will be a heterogeneously-integrated 16-bit analog-to-digital eonverter (ADC).

IV. PROGRAM ACHIEVEMENTS

As previously mentioned, three innovative heterogeneous integration proeesses are eurrently being developed in COSMOS program: mierometer seale assembly [9], monolithie epitaxial growth [10], and epitaxial layer printing [11] approaehes as illustrated in Fig. 1 (a)-(e). All integration processes successfully demonstrated intimate integration of InP and silieon transistors, and all teehnieal goals of the first Phase of the program were aehieved.

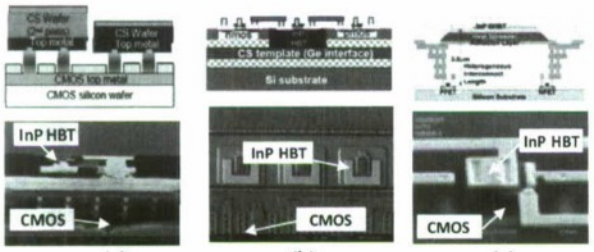

Figure 1. Hetcrogeneous integration proeesses: (a) mierometer seale assembly, (b) epitaxial layer printing, and (e) monolithie epitaxial growth.

A mierometer-seale assembly proeess is being developed by the team led by Northrop Grumman Aerospaee Systems. By first separately fabrieating small InP HBT "ehiplets" and silieon CMOS wafers, COSMOS eireuits are assembled and eonnected by heterogeneous interconnects (HIC) whieh are enabled by low temperature metallie bonding interfaees. The major advantage of this method is the flexibility to choose any CS deviees for integration with minimal proeess modifieation. However, the fabrieation of small "ehiplets," the aeeuraey of the deviee plaeement, and the fabrieation yield of the HICs are key teehnieal eoncerns. At the end of the Phase I, the NGAS researchers sueeessfully integrated 0.18 µm CMOS with advaneed 0.25 µm InP HBT as seen in Fig. 1(a).

In eontrast, the monolithie integration of III-V deviees and Si CMOS on a silieon substrate is revolutionary but extremely ehallenging (Fig. 1(b)). The approaeh developed by the Raytheon team starts by fabrieating CMOS eireuits on silieon template wafers, also known as SOLES (Silieon on Lattiees Engineered Substrates) wafers [12]. After eteling windows to expose the Ge template layer underneath the buried oxide layer, lattice-matehed buffer layers as well as metamorphie InP HBT epitaxial struetures are subsequently grown with appropriate thiekness. InP HBT deviees are then fabrieated and a BCB-based multilayer intereonneet proeess is used to intereonneet the InP HBT and previously fabrieated Si CMOS deviees. Sinee the SOLES wafers are eurrently not widely used in silieon foundries, the proof-of-eoneept demonstration in this program is eritieal for future teehnology adoption to industry partners. In Phase I, the epitaxial teehnique to grow deviee-quality struetures within the window was sueeessfully demonstrated for the first time. The eutoff frequeney of 0.5 µm-emitter-width InP HBTs fabrieated within the re-growth windows is higher than 200 GHz, and integration of higher frequeney geometries is possible. Furthermore, the fabrieation yield of this unique monolithie integration process is high, and there is no performance degradation evident for either silieon or InP transistors.

To offset the technical risks of growing high-quality epitaxial layers in situ (Raytheon approaeh) and aeeurate device plaeement (NGAS approaeh), an "epitaxial layer printing" proeess has also been explored by researchers at HRL Laboratories. Starting from transferring high quality epitaxial layers for InP HBT to a earrier wafer and then removing the original InP substrate, the epitaxial deviee layer ean be segregated and bonded on top of a pre-fabrieated planarized CMOS wafer. Subsequently, the InP deviee mesa and HBT strueture are defined. Finally, the InP and silieon intereonnect systems are interfaeed together. As shown in Fig. 1(e), the state-of-the-art 0.13 µm foundry CMOS wafers are integrated with 0.25 µm InP HBTs. These InP transistors can aehieve a eutoff frequency of more than 400 GHz.

The Phase I COSMOS demonstration eireuit, shown in Figure 2(a), is a simple differential amplifier (DA), whieh is a fundamental eireuit building bloek in digital-to-analog and analog-to-digital eonverters. To improve the resolution and signal bandwidth of mixed signal eireuits, a high speed DA with high low-frequeney voltage gain is usually desired. As has been established in silieon-based BiCMOS eireuit designs, employing high speed bipolar transistors, (e.g., SiGe HBTs), for the differential pair and using PMOS transistors as the aetive loads will signifieantly improve the DA performanee [13]. The COSMOS program leverages this eireuit eoneept by heterogeneously integrating InP HBTs, silieon NMOS and PMOS together as shown in Fig 2(a). All three teams in the program sueeessfully demonstrated reeording-breaking DAs based on their heterogeneous integration approaehes. For example, a COSMOS amplifier with > 50 dB low-frequeney voltage gain as well as 95 GHz unity gain bandwidth has been demonstrated [11]. It is worth noting that sueh reeord

performance is impossible to achieve with either CS or CMOS technology alone.

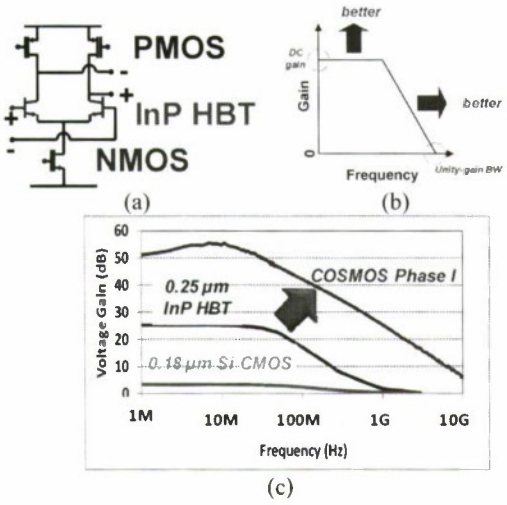

Figure 2. (a) Circuit diagram of a COSMOS differential amplifier, (b) a frequency response curve to illustrate the potential performance improvement, and (c) COSMOS Phase I DA measured result.

While continuously enhancing the heterogeneous integration processes, the teams are currently designing COSMOS-based DACs. Low power silicon CMOS technology provides the capability to calibrate and correct the static as well as dynamic errors in the data convertors in situ. Additionally, InP HBT technology intrinsically provides better transistor matching as well as much higher transistor speed and breakdown voltage than CMOS technology. However, even in this case, digitally assisted correction techniques are required to achieve the highest speed and dynamic range performance. Thus, aggressive DAC goals were intentionally defined (Table 1) to demonstrate the world's fastest, high dynamic range DAC. Several novel design techniques are now being utilized in COSMOS DACs, including dynamic element matching, digital dithers, tunable current sources, and output deglitcher circuits to reduce conversion errors. These DACs are currently in fabrication and will soon be evaluated. Based on design simulations, it is expected that these DACs will demonstrate record performance.

Although great progress has been made to date in the COSMOS program, there are further technical challenges that must be addressed. For example, the thermal conduction path (through thermal via) to efficiently transport heat away from the high-current density InP HBTs can be further optimized to fully exploit the performance of the InP technology. A comprehensive and fully integrated computer-aided-design (CAD) environment is still needed to facilitate and optimize the COSMOS circuit designs based on "the best junction of the function" concept. In addition, the heterogeneous integration processes are continually being optimized under the program and the yield and reliability of the processes will certainly be further enhanced. The ultimate goal is to establish low-cost COSMOS technology to benefit not only defense but also commercial applications.

V. OUTLOOK

The InP-silicon COSMOS technology has demonstrated record performing differential amplifiers and will soon enable ultra high performance mixed signal circuits. However, the current COSMOS technology will also allow designers to create other classes of circuits that further push the state of the art. For example, DARPA's Feedback Linearized Amplifier for RF Electronics (FLARE) program has demonstrated ultra wideband, ultra linear microwave operational amplifiers with >50 dBm of output-referred third-order intermodulation distortion intercept (OIP3) [14] by trading the excess bandwidth of 300 GHz InP HBT technology for linearity with negative feedback techniques. By applying COSMOS technology to further increase the open-loop gain of the amplifiers, even higher linearity amplifiers without power consumption penalty will be attainable.

Furthermore, it is logical to envision intimately integrating other advanced CS material systems with silicon as well. Figure 3 shows a collection of silicon-based ADC data published in literature in the past decade. The performance of these silicon ADCs are clearly bounded by the estimated 0.1 THz•V Johnson Figure of Merit (JFoM), which is defined as the product of the maximum breakdown voltage of the transistor and the unity gain cutoff frequency (f_T). While the current COSMOS program is focusing on pushing the ADC performance towards the InP 2.5 THz•V limit, we can envision the integration of GaN devices with silicon as well [15]. With digital calibration, linearization, and self-healing techniques developed in other DARPA programs, one can envision creating next-generation high power transmitters by combining GaN technology with silicon. Beyond electronics, the potential impact of monolithically integrating high-performance CS-based photonics with silicon in a chip can also be realized in the near future.

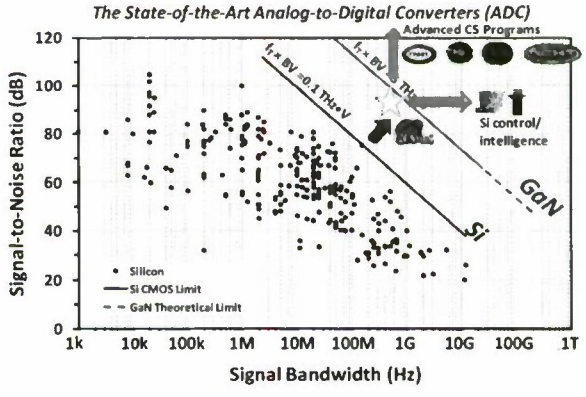

Figure 3. Published ADC data with estimated Johnson Figure of Merits of Silicon and GaN material systems.

VI. CONCLUSION

Heterogeneous integration at transistor scale has been successfully demonstrated. It provides unparalleled flexibility in circuit design for the implementation of increasingly demanding and complex mixed signal analog to digital converters and other circuit applications. The COSMOS program is developing fabrication capabilities to combine the functionality provided by state-of-the-art CS and silicon devices. The success of the COSMOS technologies will enable tremendous savings of size, weight, power, cost, and fabrication cycle time of RF and mixed-signal microsystems.

VII. ACKNOWLEDGEMENTS

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Nanowires for Quantum Optics

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We present optical measurements on nanowire heterostructured quantum dot devices. Quantum dots defined with hetero-material structures are presented as well as a novel type of quantum dot defined by the crystal phase of the semiconductor. We demonstrate the possibility of electrically addressing a single quantum dot with photocurrent and perform electroluminescence measurements on a single nanowire light emitting diode. The applicability of our devices to advanced quantum optics and quantum plasmonics measurements is discussed.

Nanowire quantum dots offer a range of advantages over the well established self-assembled quantum dots. The light extraction efficiency can be far higher because the dot is not fully embedded in a high refractive index material and the nanowire, given the right diameter, can act as a waveguide for the quantum dot emission. The position of the nanowire can be controlled by simply positioning the gold seed particles that are used as catalysts to grow the nanowire heterostructure. The lateral size of the quantum dot can be controlled at will with the nanowire diameter from a few to tens of nanometers and the height of the quantum dot is simply set by the growth time. Stacking two quantum dots in a nanowire is straightforward, making quantum dot molecules easily realized. The possibility to grow a shell around the nanowire enables surface passivation as well as strain engineering. Because of the very small diameters of nanowires, strain at heteroepitaxial boundaries is easily accommodated by lattice deformation instead of defect formation as is the case for two-dimensional growth. This versatility enables the combination of a vast range of materials, even including the combination of silicon and III-V materials. Last but not least, a single nanowire can be electrically contacted and al the current flowing through the device will then flow through the quantum dot.

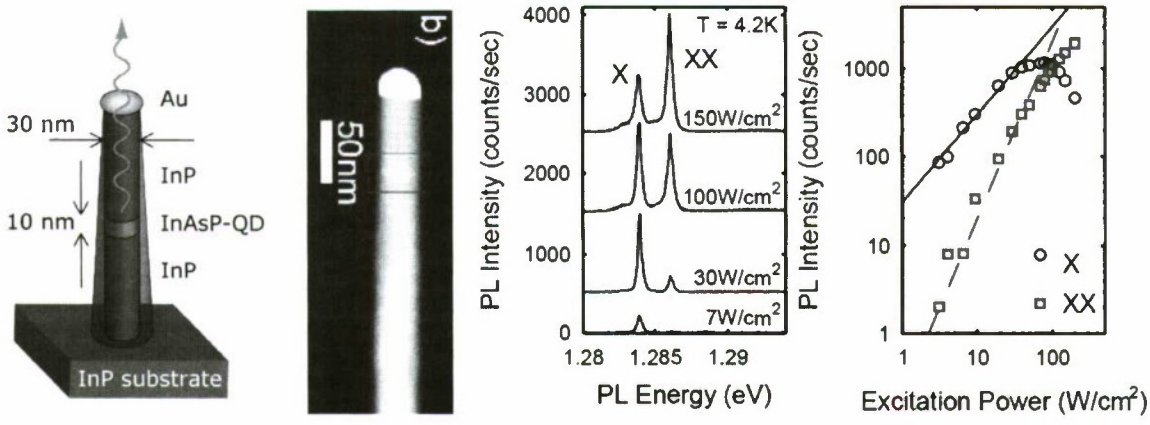

Fig 1. Left: structure of an InAsP/InP nanowire quantum dot, a transmission electron microscope image of a nanowire quantum dot is shown, the quantum dot is highlighted by the red rectangle. Photoluminescence spectra taken under increasing laser power showing the exciton (X) and biexciton (XX) emission. Right: Integrated power dependence for the exciton and biexciton.

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Our first goal was to define a high quality nanowire quantum dot heterostructure, where the emission linewidth would be narrow enough to enable quantum optics experiments. We obtained high quality quantum dots made of InAsP in an InP nanowire with a thin InP shell acting as a surface passivation for the nanowire. A schematic of the structure is shown in fig 1a. A transmission electron microscope image confirms the presence of the quantum dot, as shown in fig 1b.

Optical measurements were performed at the single quantum dot level at cryogenic temperatures using a micro-photoluminescence setup with a high numerical aperture objective (0.85 NA), sensitive CCD and spectrometer with a resolution of 25 μeV. Spectra taken under increasing laser excitation power density are shown in fig 1c where the exciton and biexciton emission lines are observed. The identification of the exciton and biexciton lines is confirmed by a power dependence shown in fig 1d where the exciton shows a linear power dependence while the biexciton shows a quadratic power dependence. This behavior is very much reminiscent of the usual self-assembled quantum dot behavior.

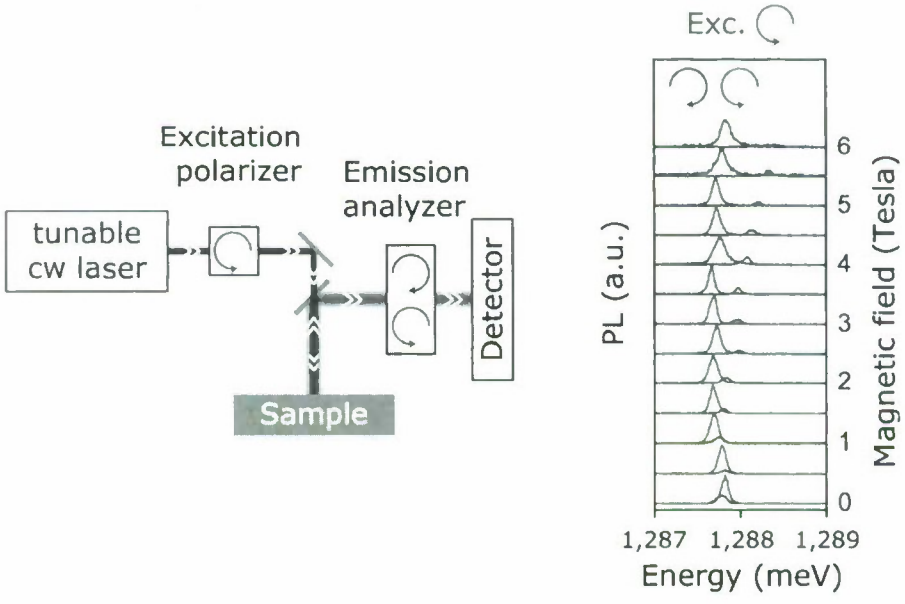

Fig 2 Left: Schematic of the single spin memory experiment: a circularly polarized laser pulse creates an exciton. The photoluminescence polarization is then analyzed. Right: Photoluminescence spectra under right circularly polarized excitation measured under increasing magnetic field from 0 to 6 T. The photoluminescence is always right circularly polarized.

The narrow linewidth of the exciton emission (typically of the order of 100 μeV) enables the observation of a Zeeman splitting at easily accessible magnetic fields. We tuned the excitation laser to the p-shell of the quantum dot for quasi-resonant excitation and set its polarization to right circular polarization. This then creates a given spin orientation of the electron and hole. No spin flip is to be expected from the p to s shell relaxation and the luminescence should therefore retain the same polarization than the incoming excitation laser pulse. This experiment was performed with the setup schematically shown in fig 2a, where the laser and photoluminescence polarization is precisely measured. The measured exciton photoluminescence is shown in fig 2b as a function of magnetic field intensity for right circular excitation. The photoluminescence is dominantly right circular polarized, demonstrating that the exciton spin is conserved during relaxation. Our nanowire quantum dots can therefore act as spin memories for time scales in excess of their radiative lifetimes (of about 1 ns). The same experiment was performed with left circularly polarized light and demonstrated left circularly polarized photoluminescence. **[1]**

Quantum dots are usually defined with material heterostructures such as InAs in GaAs. This material combination has been a very successful and thoroughly studied quantum dot system. Nanowires offer a new route to charge confinement at the nanometer scale: the crystal phase is an additional degree of freedom: both zincblende and wurtzite crystal structures are stable at the nanometer scale. While both crystal structures have the exact same chemical compositions, their band structure differ in bandgap as well as in band alignment. A zincblende InP region in a wurtzite InP nanowire confines electrons in the conduction band. We show InP nanowire in fig 3a, transmission electron microscopy i9mages are shown in fig 3b. The red arrows indicate zincblende regions. While the zincblende segments are not yet fully controlled in terms of position and width during growth, the density is low enough to study a very small number of such structures optically. In fig 3c, we show an atomic resolution image, where the narrow zincblende region that can confine electrons is visible.

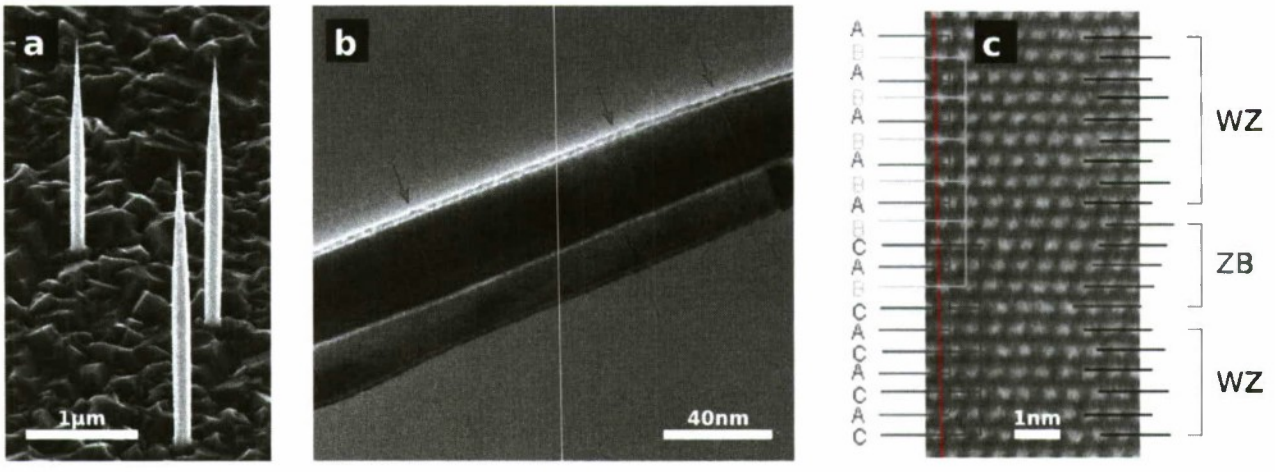

Fig Fig 3 (a) Scanning electron microscope image of an InP nanowire. (b) Transmission electron microscope image of two InP nanowires. The red arrows indicate zincblende segments. (c) atomic resolution image showing a zincblende segment.

A photoluminescence spectrum taken on a single InP nanowires containing zincblende segments is shown in fig. 4. The emission linewidth is very narrow (24 µeV, limited by our spectrometer resolution) and very intense with an integrated intensity above 10^4 detections/s. This demonstrates the great value of this novel type of quantum dots where only the crystal phase is used to define the confinement potential. We have demonstrated that these crystal phase quantum dots act as single photon sources, and that the radiative lifetimes are very long, as expected from the type II recombination in this system [2].

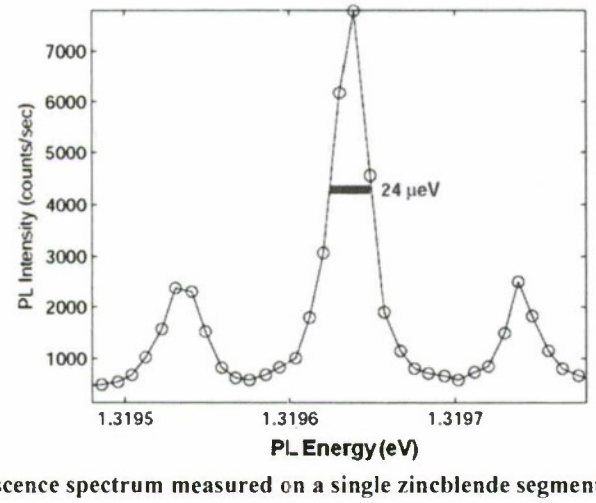

Fig 4 Photoluminescence spectrum measured on a single zincblende segment in a wurzite InP nanowire.

The high quality InAsP quantum dots in InP nanowires were then positioned in nanowires with a p doped extremity on one side and n doping on the other to define a pin structure. This structure can be used both as a detector by reverse biasing the pn junction or as a light emitting diode under forward bias. A schematic view of the band structure of the device is shown in the top of fig 5. A photocurrent image was obtained by applying a constant reverse bias on the nanowire structure and measuring the current while a laser spot was scanned across the device. The resulting image is shown at the bottom of fig 5 where the surface reflection was also added to make the contacts visible. An intense photocurrent spot is clearly visible in the middle of the nanowire, exactly where the quantum dot is expected. This demonstrates that absorption takes place in the quantum dot and that under reverse bias the photogenerated electron-hole pairs tunnel out and contribute to a current.

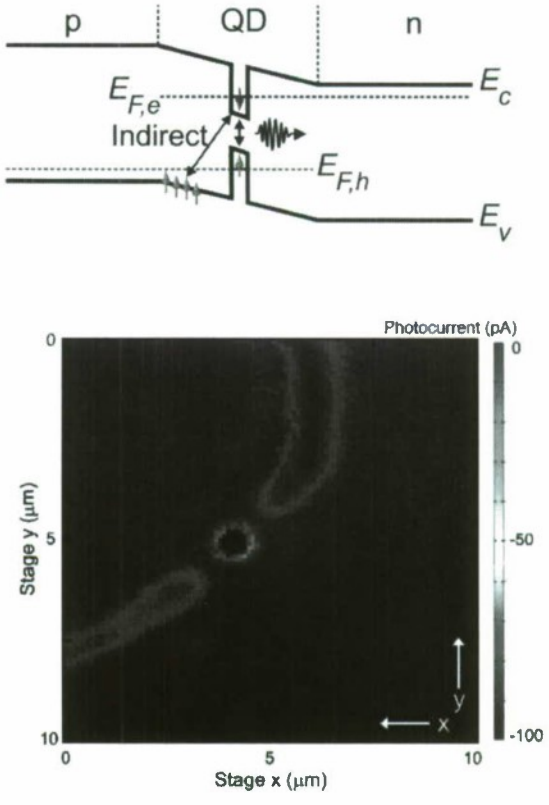

Fig 5 Top: band structure of a nanowire quantum dot light emitting diode. Bottom: photocurrent image of a nanowire device under reverse bias. A reflection image was superimposed with the photocurrent to make the electrical contacts visible.

The very same device that was used for photocurrent measurements can also be used for electroluminescence experiments. Here a single quantum dot embedded in a nanowire is electrically excited; this represents an important step towards the realization of a practical single photon turnstile device where single photons would be generated on demand under the injection of single electrons. In fig 6 (left), we present a schematic of the device we have realized where ohmic electrical contacts are made to both the p and n doped regions and electroluminescence occurs at the pn junction under forward bias. A microscope image of the real device under white light illumination and zero bias is shown in fig 6 (center), here the device is held at liquid helium temperature. Fig 6 (right) shows the device under a forward bias of 2 V. Electroluminescence is clearly observed from the center of the nanowire where the pn junction is expected. This constitutes the operation of the smallest light emitting diode reported so far where the active region is only one single quantum dot.

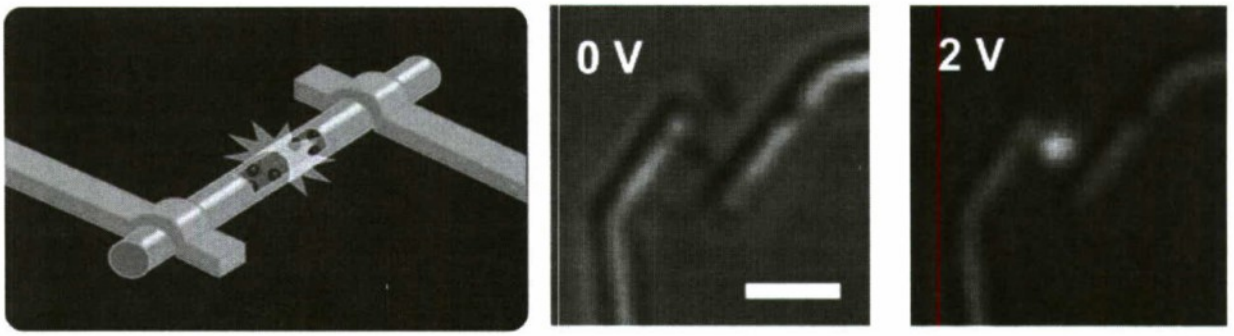

Fig 6. Left: schematic of a single nanowire light emitting diode. Center and right: microscope image of a nanowire light emitting diode, from ref [3].

Our single quantum dot nanowire offers great application perspectives in the field of integrated quantum optics. We show in fig 7a a schematic representation of an all on-chip quantum plasmonics device where a single nanowire light emitting diode is used as a source and is coupled to a plasmon waveguide. A superconducting nanowire is then used to detect single plasmons in the near field. A plasmonic waveguide coupled to a single plasmon detector was fabricated and successfully operated in our group [4]. Fig 7b shows an integrated plasmonic Hanbury-Brown Twiss interferometer where two plasmonic waveguides are couple over 5 microns to obtain a 50-50 coupling according to simulations. Here, both output arms are coupled to superconducting nanowire single plasmon detectors. Merging optically active nanowire structures with plasmonic structures offers a very strong potential for on chip-quantum optics experiments.

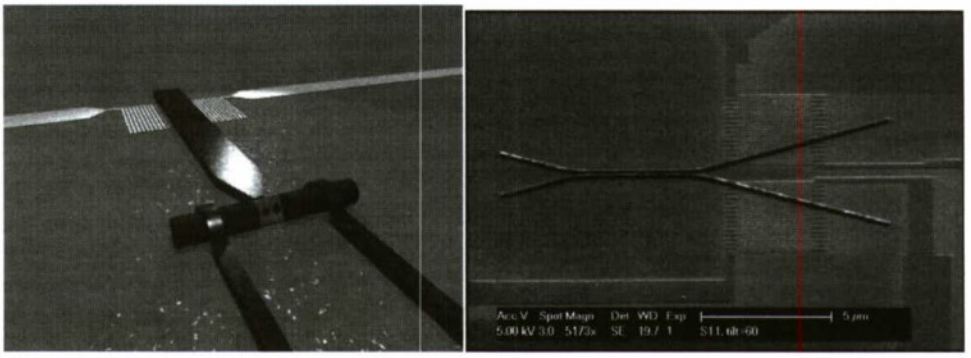

Fig 7. Left: Integrated quantum plasmonics concept. A nanowire light emitting diode is coupled to a plasmonic waveguide. Single plasmons are detected with a meandering superconducting nanowire. Right: A plasmonic beam splitter (coupled waveguide) coupled to two independent single plasmon detectors.

In conclusion, we have demonstrated that optically active quantum dots in nanowires are very good nano-optical systems with properties and functionalities that offer advantages over more conventional self-assembled quantum dots. In particular, the possibility of merging nanowire quantum dot light emitting diodes with plasmonics circuits offers a wide field of applications and experiments.

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Selective-area MOVPE growth and optical properties of single InAsP quantum dots embedded in InP NWs

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***Abstract*—We grew InAsP and InP/InAsP/InP heterostructure NWs (NWs) by selective-area MOVPE and carried out micro-photoluminescence (μ-PL) measurement. We investigated growth conditions for InAsP NWs and that embedded in InP NWs, and obtained exciton and biexciton emissions from InAsP QDs at optimized growth conditions. Negative binding energy of biexciton was observed due to the strong Coulomb interaction between the holes in the QDs.**

I. Introduction

Recently, semiconductor NWs (NWs), which are one of the one-dimensional nanostructures with thin diameter of hundreds of nanometer or less, are attracting great deal of interest as new building blocks for nano-photonic and nano-electronic devices. One of the interest in such one-dimensional semiconductor nanostructure is in a possibility to realize various kind of heterostructures, including quantum wells (QWs) or quantum dots (QDs) [1], [2], by utilizing growth control in the axial or radial directions [3], [4]. In addition, because of their small lateral size, it is expected to realize heterostructures free from constraints originating from lattice mismatching issues. Therefore, it is possible to realize high-quality heterostructures going beyond a conventional limit of strained-layer systems, for example, based on InP [5], [6].

Combination of NWs and QDs by embedding QDs inside NWs is particularly promising for single photon sources [7] used in quantum information and quantum cryptography application. The reasons are as follows. Firstly, it is possible to put one single QD in NWs by appropriate control of the growth. Secondly, geometry of NWs makes the formation of electrical contact easy, and it is advantageous in achieving high light extraction efficiency. Furthermore, QDs in NWs have an advantage that vanishing fine structure splitting of excitons is expected [8], which is necessary to realize entangled single photon sources. This is because III-V semiconductor based NWs are, in general, grown in the $\langle 111 \rangle$-direction of zincblende crystal, and the $\{111\}$ surface has three-fold symmetry. Consequently, there are no intrinsic anisotropy for vertical and parallel polarizations. Such symmetry also leads to an expectation that the shape anisotropy of QDs on $\{111\}$ surfaces is much smaller than those on (001) surfaces.

Here, we report on the growth of InP/InAsP/InP heterostructure NWs by selective-area MOVPE to realized InAsP QDs inside of InP NWs. We first describe the growth of InAsP NWs on InP substrates to investigate the growth conditions for InAsP. Next, InP/InAsP/InP heterostructure NWs were grown. By optimizing the growth conditions for InAsP, QDs are formed in InP NWs. Formation of QDs were confirmed by micro-photoluminescence (μ-PL) measurement.

II. Experimental Details

InP-based NWs were grown on InP(111)A or (111)B substrates partially covered with SiO_2 mask. First, 20 nm-thick SiO_2 film was deposited by RF-sputtering, and periodic array of circular mask openings was defined by electron beam lithography and by wet chemical etching. Obtained mask opening diameters d_0 was around 100 nm and distances between the openings (pitch a) were 600 nm, 800 nm, 1000 nm, 1500 nm and 3000 nm. Selective-area MOVPE growth was carried out on these substrates using trimethylindium (TMIn), terthiryhutilphoshine (TBP) and arsine (AsH_3) for precursors of In, P, and As, respectively. Two types of samples, namely, sample A and B, were grown to study the growth of InAsP NWs and to form QDs, respectively. For sample A, InAsP NWs were grown on InP (111)A and B substrates while changing the supply ratio R_V of group V precursors to investigate its impact on the composition of grown InAsP. Here, R_V is defined by the ratio of partial pressures of TBP and AsH_3, that is, $R_V = [\mathrm{TBP}]/[\mathrm{AsH_3}]$, and was set at 1.3, 20, and 50. Growth temperature T_g was 580°C and growth time was 20 min. For sample B, InP/InAsP/InP heterostructure NWs were grown as follows. First, InP NWs were grown at $T_g = 660$°C for 15 min, followed by the growth of InAsP at $T_g = 580$°C with various growth time t_g and R_V. In the present study, t_g was 1, 3, 10 and 30 sec, and R_V was 1.3,

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20 and 50. Finally, InP capping were formed with two steps, namely, at the same temperature for 1 min growth without interruption and at 660°C for 10 min.

Optical properties of the samples were studied by μ-PL at 4K. He-Ne laser was used for an excitation light source and was focused on the sample by $\times 50$ microscope objective lens with spot size of about 2 μm. PL from the sample were collected through the same objective lens and analyzed by a spectrometer equipped with liquid-nitrogen-cooled Si charged coupled device (CCD) or InGaAs photodiode (PD) array.

III. Results and Discussions

A. Growth of InAsP NWs

Figure 1 shows a typical scanning electron microscope (SEM) image of InAsP NWs (sample A) grown on InP (111)B substrate. Here, R_V is 20 and similar SEM images were obtained for different R_V. One can see uniform array of InAsP NWs are formed. NWs had hexagonal cross section and their sidewall facets were $\{\bar{1}10\}$, similar to the case of InAs [9]. On the other hand, NWs on (111)A substrates did not grow vertically; instead, we obtained tripod structures in the part of the mask opening, as typically shown in the inset of Fig. 1. We have reported that the growth direction of InAs NWs are in the $\langle 111\rangle$B direction [9], while it is in the $\langle 111\rangle$A direction [10], [11] for InP in selective-area MOVPE. This suggest that the InAsP growth direction is related to the composition of InAsP. That is, P rich InAsP NWs would grow in the $\langle 111\rangle$A direction but As rich ones in the $\langle 111\rangle$B direction. Since the present results show that the growth direction of InAsP NWs is in the $\langle 111\rangle$B direction, we think As-rich InAsP NWs are formed. For tripod structure on (111)A, we think the direction of the tripod is in the $\langle 111\rangle$B direction and As-rich InAsP is also formed.

We also carried out low-temperature PL measurement of InAsP NWs with various R_V using an InGaAs PD array detector. However, we were not able to any detect PL signal from InAsP NWs grown grown for R_V=1.3, 20 and 50. Instead, we obtained PL peak at 0.78 eV from reference planar region for R_V=20 and 50. We believe these results show the emission energy of InAsP NWs are beyond the detection limit (down to 0.73 eV) of our PL setup, and that the ratio of P to As incorporated into NWs and planar layers is much fewer than the supply ratio of TBP to AsH_3 (=R_V) during the growth. From the emission energy, the composition of P in InAsP NWs is estimated to be 0.42 for $R_V = 50$, and the amount of P is much fewer in NWs or planar regions for lower R_V. Such few incorporation of P in InAsP is also reported for planar growth in MOVPE [12].

B. Growth and characterization of heterostructure NWs

As mentioned in the previous section, InP NWs grown in the $\langle 111\rangle$A direction, while InAsP grows in the $\langle 111\rangle$B direction in our present conditions. It also should be noted that the present growth condition for InP NW results in the formation of wurtzite InP with $\{\bar{2}11\}$ sidewall facets [13]. With all these complications, we chose the the growth of

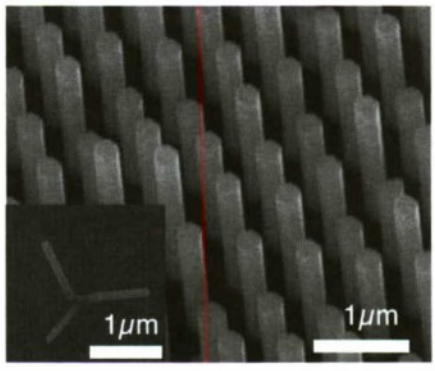

Fig. 1. SEM images of (a) InAsP NWs (sample A) on (111)B InP substrate. Inset shows InAsP grown on (111)A InP substrate.

InP/InAsP heterostructure (sample B) on (111)A substrate, since the required thickness for InAsP QDs and QWs are much thinner than InP NWs. Figure 2(a) shows a typical SEM image of InP/InAsP/InP NWs. R_V is 20 and t_g is 10 sec. It was found that the diameter of NW became enlarged from its middle. Such enlargement of the top was not observed for InP NWs. Furthermore, the diameter of InP NW prior to the growth of capping InP was the same as the mask opening. This is shown in SEM images of Fig. 2(b) and (c), where InAsP was grown for 1 min with R_V=20. We can clearly see NWs with uniform thickness and edges of the SiO_2mask. Thus, the enlarged top was formed after the growth of capping InP. There are some bent NWs in Fig. 2(b), which are resulted from non-uniform sidewall growth of a strained layer [14]. However, such bent NWs were formed only for the growth time of 1 min. Therefore, we conclude that side wall growth of InAsP layers was negligible, especially for short t_g, InAsP was grown on the top of InAsP, and the cross section of NWs is as shown in Fig. 2(d).

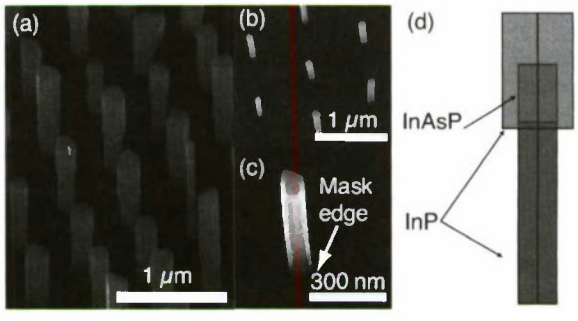

Fig. 2. (a) SEM image of InP/InAsP/InP NWs (sample B). (b) and (c) show InAsP/InP NWs without InP capping. (d) Schematic cross section of an InP/InAsP/InP NW.

Next, we carried out PL measurement of sample B grown with various group-V supply ratio (R_V) and growth time t_g of InAsP. Firstly, we show typical PL spectra with different R_V in Fig. 3(a) (R_V=20) and (b) (R_V=50), with t_g = 3 sec. In these figures, spectra of NW array width different pitch a

are also shown. In addition to the PL from InP NW at 1.51 eV (which has wurtzite crystal structure [11], [13]) and InP substrate at 1.43 eV, we observed PL emission around 1.2 eV or 1.4 eV in sample B for R_V=20 and 50, respectively. These are attributable to the emissions from InAsP layer. This means that the emission from InAsP layer embedded in InP shows considerable blueshift as compared to InAsP in sample A. Large R_V, that is, high TBP supply ratio, resulted in the blueshift of PL emission energy, as expected from the increase of P incorporation in InAsP layer. However, decrease of R_V down to 1.3 resulted in much broader emission band, particularly for long t_g (=10 sec) (not shown here). Therefore, it is considered that larger R_V and short growth time is important to obtain uniform InAsP layer.

We also can see that the emission energy is also different with a. Difference of alloy composition with different a is reported for group-III alloy, for instance, InGaAs [15]. However, it is not expected for group-V alloys, because incorporation of group-V materials are thought to mainly be determined by their precursor concentration in the gas phase, and their concentration gradient in the vapor phase is uniform in the region far smaller than their diffusion length ($\sim 100\mu$m). Since clear tendency for a is not observed in the emission energy, further investigation is necessary for precise control of InAsP composition.

To further confirm the origin of blueshift in sample B, we compared the PL spectra of different t_g, as in Fig.4(a). R_V is 20. We can confirm the lowest energy emission from InAsP layers changed with t_g, indicating the origin of blueshift is quantum confinement effect due to the reduction of the thickness of InAsP layer.

We estimated the thickness of InAsP layer assuming the InAsP layer forms unstrained QW in InP, and the results are summarized in Fig. 4(b). Here, the lowest energy of the emission peak is used to estimate the well width of InAsP, and P composition y of 0.6 is assumed, based on the experimental results for sample A described in the previous section. The increase of InAsP thickness with growth time t_g is evident. It is, however, noted that the thickness is lower than that estimated from growth rate of InAsP NW (dotted line) and shows sublinear increase with t_g. These errors would be caused by the negligence of strain effect, and non-constant growth rate, or change of P incorporation during growth.

C. Optical properties of QDs in NWs

Finally, we carried out detailed PL measurement on NWs grown for R_V=20 and t_g = 3 sec. Because the excitation spot size for PL is about 2 μm, single NWs can be measured if the pitch a of NW array is 3 μm. Figure 5 (a) shows PL spectra from a single NW and its dependence on excitation intensity. We got very sharp emissions of X and XX at 1.227 eV and 1.232 eV, respectively. The full width of half maximum of X was 400μeV at the excitation power density of 1 W/cm^2, as shown in Fig. 5(b). Figure 5 (c) represents excitation power dependence of X and XX. The peak X increases linearly as excitation power density, and XX shows squared dependence.

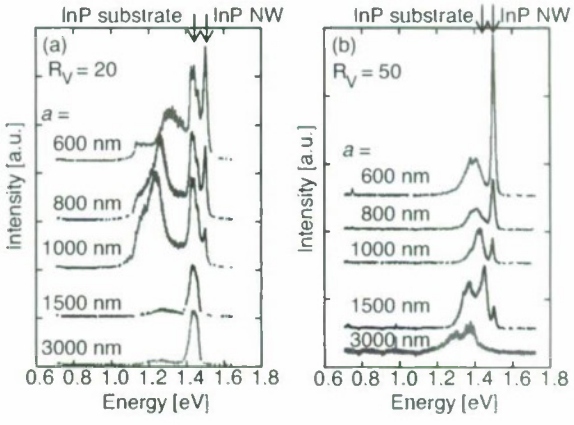

Fig. 3. PL spectra of sample B for different NW pitch a for R_V=20 (a) and 50.

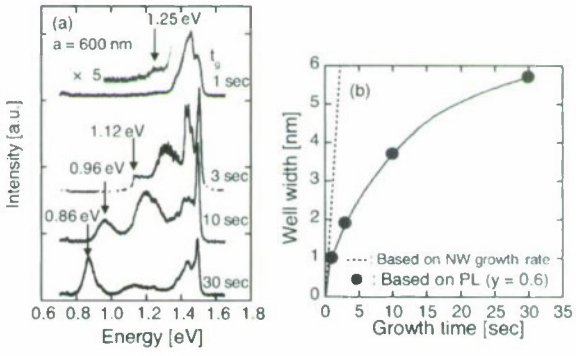

Fig. 4. Growth time t_g dependence of PL emission in sample B for R_V=20.

Therefore, we conclude X and XX are emissions from exciton and biexcitons in a single InAsP QD embedded in NWs, respectively. It is noted that binding energy of biexciton is negative ($E_X - E_{XX} = -4.5$meV), This is presumably due to the strong Coulomb interaction between the holes of biexciton. Such negative binding of biexcitons are reported in Stranski-Krastanow InAs QDs, and indication of the formation of very small QDs [16].

Sharp emissions originating from QDs are observed in some other NWs of sample B grown for R_V=20 and 50, and t_g less than 3 sec. In addition, both excitonic and biexcitonic emission were observed in most of the QDs. The emission peak energy, intensity, and linewidth differs NW to NWs, and some NWs seem to contain multiple QDs. Nevertheless, the emission energy is reasonably controlled by R_V, and larger R_V resulted in the emission at the higher energy level. Excitonic and biexcitonic from QDs have been confirmed between 1.02 eV [17] from 1.45 eV at present. Binding energy of biexciton is both positive and negative, which seems to be correlated with emission energy; it is positive for smaller emission energy, and large and negative for higher energy. Therefore, our InAsP QDs embedded in InP offers a wide tunability of emission

energy and possibility for single photon emission to cover whole optical fiber communication band, as well as to study the optical properties of QDs.

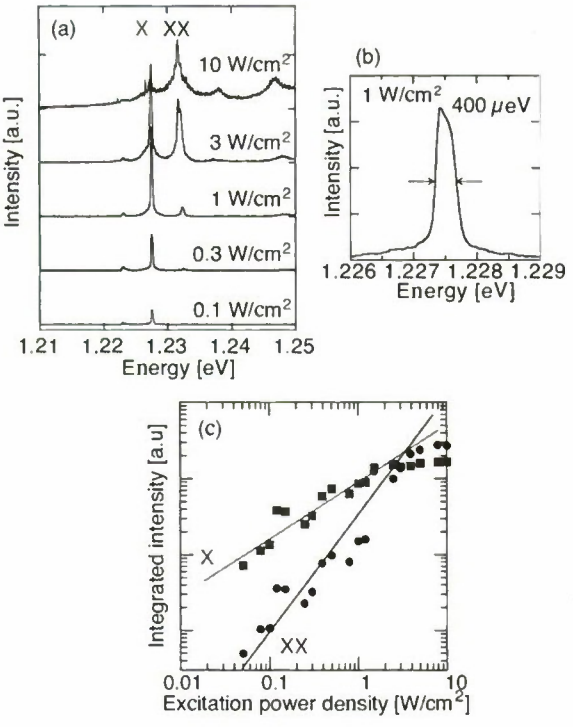

Fig. 5. (a) PL spectra of an InAsP QD. X and XX were considered to be exciton and biexciton, respectively. (b) Blow-up of a spectrum for excitation power density of 1 W/cm^2. (c) Excitation power dependence of integrated peak intensity for X and XX.

IV. Conclusion

We grew InAsP NWs and InP/InAsP/InP vertical heterostructure NWs by selective-area MOVPE to form a single QD in NWs. InAsP NWs vertical to the substrate were grown on (111)B InP substrate, indicating that the growth direction of NWs is in the ⟨111⟩B in the present growth conditions. Alloy composition of P and As in InAsP can be controlled by changing the supply ratio of their precursors. Incorporation of P is smaller than As, resulting in As-rich InAsP NWs. PL measurement of heterostructure NWs confirmed the composition and thickness of InAsP layer can be controlled by growth conditions. Emissions of exciton and biexciton in QD were confirmed by μ-PL measurement and their excitation intensity dependence. Negative binding energy of biexciton was found, suggesting strong Coulomb interaction between holes confined in small QDs.

Acknowledgment

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InAs/InP QDs broadband LED using selective MOVPE growth and double-cap procedure

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Abstract

InAs/InP QDs broadband LED more than 450 nm spectrum width was succcssfully demonstrated. The broadband spectrum was obtaincd from the height controlled double-cap procedure and strain controlled buffer layer fabricated by the selective MOVPE technique.

I. Introduction

Broadband emission deviees in long wavelength band are important for the optieal eommunication systems such as WDM light sources, infrared speetroseopy, and medical application sueh as optieal coherence tomography. To achieve broadband light emission, a scmiconductor material with a wideband energy distribution is neeessary. By using the quantum well structure, only one dimension of the height ean be controlled the quantum energy level. On the other hand, in the QDs strueture, the three-dimensional control of the energy level is possible, and we can expeet to obtain the widc energy lcvel eontrol in the QDs structure.

In a previous study, we obtained wideband electrolumineseenee (EL) from InAs/InP QDs by a double-eap procedure and selective MOVPE growth [1]. Using a narrow-stripe array mask with a wide mask at one side of the array, we controlled the emission wavelength in each array waveguide. We also attempted to control the vertieal height of the QDs by changing the eap layer thickness during the double-eap procedure [2]. To obtain broader band lumineseenee, we controlled the strain under the QDs by changing the Ga content of the $Ga_xIn_{1-x}As$ buffer layer [3].

In this paper, we explain the growth conditions of the InAs/InP QDs broadband LED using selective MOVPE growth and double-eap proeedure, and also show the speetrum width of QDs LED.

II. Selective MOVPE using a double-cap procedure

A QDs-array waveguide structure was grown by seleetive area growth by low-pressure MOVPE using a SiO_2 narrow-stripe mask array with a wide SiO_2 mask at one side of the array. A sehematie diagram of thc mask pattern is shown in Fig. 1. Since the supply material does not grow on SiO_2, the eoneentration of the material at the upper part of the SiO_2 mask becomes high, and lateral vapor diffusion oeeurs at the non-masked part of the mask pattern. The growth speed becomes large near the wide mask and small in the far side of wide mask. And at the same time, the eomposition of Ga and In of GaInAs layer ehanges in eaeh array waveguides due to the diffusion length difference between Ga and In. Hence the peak wavelength of the emission of light in eaeh array waveguide changes by the difference of QDs energy level.

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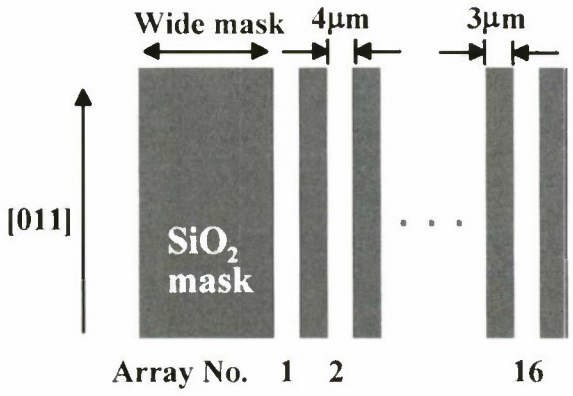

Fig. 1: Schematic diagram of the SiO_2 mask pattern.

The growth of QDs is Stranski–Krastanov (S–K) growth mode [4], and during the growth of QDs, we used double-cap procedure. The growth process of double-cap procedure is explained as follows. After the growth of InAs QDs, first-cap layer (FCL) was supplied thinner than the height of InAs QDs. Then the growth interruption performed under the supply of phosphide. During the As/P exchange occurs, the unprotected island are planned. After the growth interruption, InP second-cap layer (SCL) was grown. By using this double-cap procedure, the uniformity of QDs height improves in each array waveguides.

By using selective MOVPE growth and double-cap procedure, we can control the size and energy level of QDs for the lateral direction. In the previous experiment, we have tried to control the QDs vertically in each array waveguide [3]. If we change the FCL thickness during double-cap procedure, we can control the QDs height vertically. Furthermore, if we change the composition of GaInAs buffer layer under the QDs, we can control the QDs energy because of the strain energy difference between QDs and buffer layer. By using these lateral and vertical control of QDs size and energy, we have tried to obtain the broadband LED.

III. Results and Discussion

In the selective MOVPE growth, the wide mask width was 100-200 μm. The number of stripe was 16, and stripes were formed parallel to the [011] direction. The array waveguide was selectively grown with the width of 4 μm and the space between next array was 3 μm. We named the nearest waveguide array as no.1, and array no.16 was in the far side of wide mask. The precursors used in the MOVPE growth were TMI, TEG, TBP, TBA, and DEZn, DTBSi as a *p* and *n* dopant.

The dependency of PL peak wavelength and thickness of the FCL at the non-masked area was shown in Fig.2. From this figure, the peak wavelength was clearly blue-shifted as the thickness of FCL was decreased. The wavelength shift between 0.5 nm thickness FCL and 2.0 nm thickness FCL was 100 nm. From this result, if we grow the different thickness of FCL in the multiple stacked InAs QDs, we could expect the further wide emission wavelength LED. In our growth conditions, the height of the QDs in the non-masked area was approximately 5.5 nm. Therefore, we could control the height of QDs below this value.

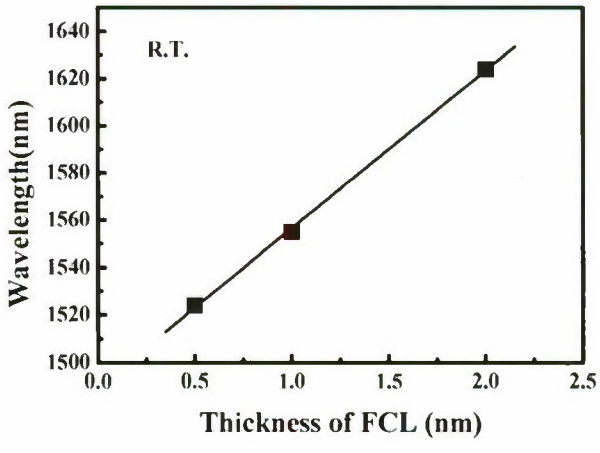

Fig. 2: PL peak wavelength of QDs versus FCL thickness.

Fig. 3 shows the PL peak wavelength from QDs when the composition of GaInAs buffer layer was changed. We can clearly observed if we increased the Ga composition of buffer layer, the PL wavelength

was blue shifted because of the strain between QDs and buffer layer was increased. And we obtained more than 500 nm PL wavelength change by changing the buffer layer.

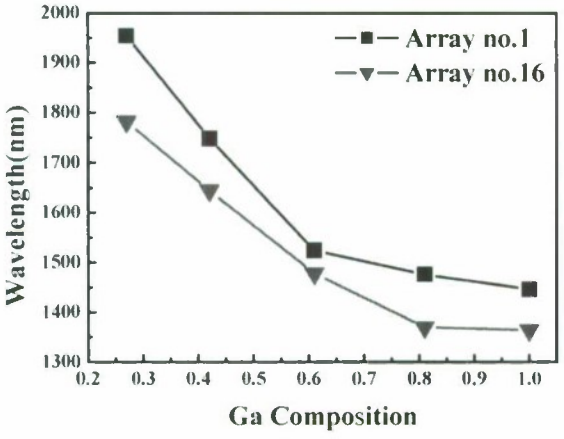

Fig. 3: PL peak wavelength of QDs versus Ga composition of the buffer layer.

By using these experimental results, we have fabricated 3 QDs layer LED by changing the FCL thickness and composition of GaInAs buffer layer. Fig. 4 shows the schematic layer structure of a three-layer InAs QDs LED with varying Ga content in the buffer layer and also an FCL thickness that varied layer by layer. The growth procedure is as follows. First, 110-nm-thick n-InP and 1.4-nm-thick $Ga_{0.47}In_{0.53}As$ layers were grown on (100)-oriented n-InP substrate at a temperature of 640 °C and a pressure of 100 Torr. InAs QDs were grown at a temperature of 540 °C and a pressure of 15 Torr. The growth rate of the QDs was 0.013 ML/s, and the source supply time was 35 sec. In addition, growth interruptions of 60 sec occurred during supply of TBA after QDs growth. The $Ga_{0.47}In_{0.53}As$ layer under the QDs was grown to prevent phosphorus desorption during these growth interruptions. We then used the double-cap procedure. After the growth of InAs QDs, 3-nm-thick $Ga_{0.75}In_{0.25}As$ layer, which were thinner than the height of the InAs QDs and are referred to as the FCL, were supplied. The $Ga_{0.75}In_{0.25}As$ as a FCL in place of InP was used to improve the PL intensity and the uniformity of QDs size after the ref. [5,6]. A growth interruption of 8 min was then applied under a supply of TBP, during which As/P exchange occurred, and unprotected islands are planned. After this growth interruption, the temperature and pressure were increased to 640 °C and 100 Torr, respectively. Then, a 22-nm-thick InP second cap layer (SCL) was grown. After the growth of 2nd and 3rd GaInAs layer and double-capped QDs layer, 55-nm-thick i-InP, 1.5 μm p-InP, and 10 nm p-$Ga_{0.47}In_{0.53}As$ layers were grown at a temperature of 640 °C and a pressure of 100 Torr. In this device, the Ga content (x) and FCL thickness were 0.47 and 3 nm in the first QDs layer, 0.27 and 1.5 nm in the second layer, and 0.75 and 4.5 nm in the third layer, respectively.

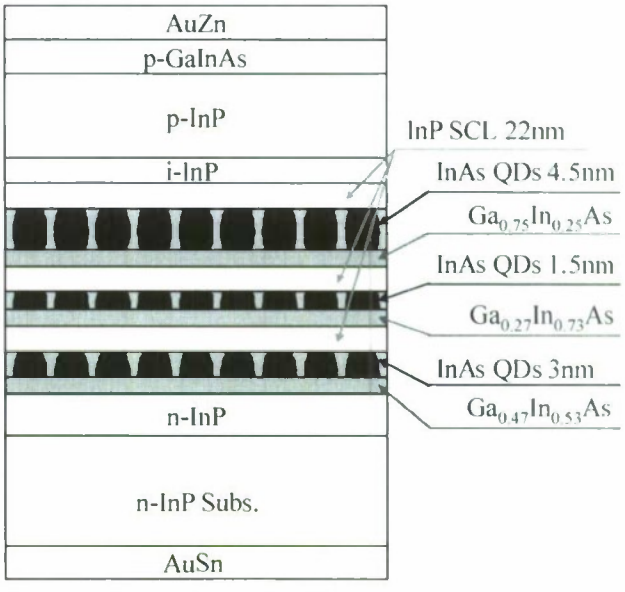

Fig. 4: Schematic layer structure of InAs QDs LED

Fig. 5 shows the EL spectrum of an InAs QDs array waveguide LED with various CW injection currents measured at room temperature where the device length was 218 μm. Table I summarizes the FWHM of spectrum with various injection current. By increasing the injection current, the spectrum width was gradually reduced, but we have obtained more than 450 nm FWHM of the spectrum, when the

injection current was less than 60 mA. This broadband spectrum width was obtained because of the lateral and vertical control of QDs size and energy level.

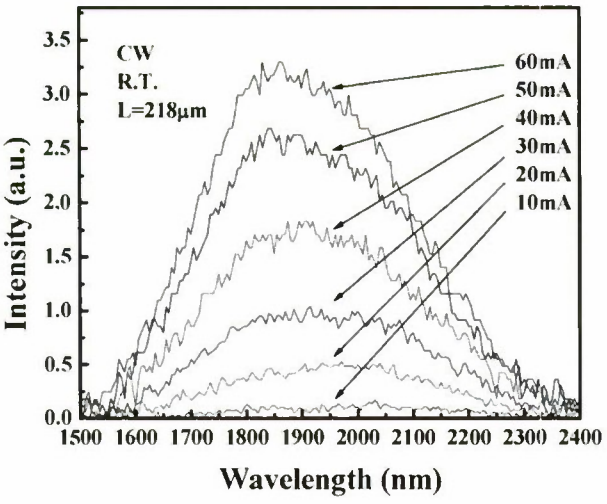

Fig.5: EL spectrum as a function of injection current.

TABLE I: FWHM of spectrum with various current

Current (mA)	10	20	30	40	50	60
FWHM (nm)	484	462	479	450	443	451

From the PL measurements, the peak wavelengths were 1800 nm, 1550 nm, and 2050 nm for the first, second, and third QDs layers, respectively. By comparing the EL spectrum, the emission from the second layer, where the Ga composition of the buffer layer was 0.70, was considered too weak. In the PL measurements, the PL intensity was reduced remarkably when the Ga composition of the buffer layer was high because of the large strain energy. To increase the intensity of QDs where the high Ga composition buffer layer, we have to optimize the growth conditions of buffer layer and QDs.

However, because we obtained an EL spectrum width more than 450 nm, the lateral and vertical controls of QDs energy are effective for a broadband LED.

IV. Conclusion

Broadband LED with a spectrum width of more than 450 nm was obtained in an InAs QDs array waveguide. In the three-layer QDs array waveguide, the height of the QDs was changed by changing the FCL thickness during the double-cap procedure. The strain of the QDs was controlled by changing the Ga composition in the $Ga_xIn_{1-x}As$ buffer layer using selective MOVPE growth.

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Temperature sensitivity of 1.5μm (100) InAs/InP-based Quantum Dot Lasers

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Semiconductor lasers with quantum dot (QD) based active regions have generated a huge amount of interest for applications including communications networks due to their anticipated superior physical properties due to three dimensional carrier confinement. For example, the threshold current of ideal quantum dots is predicted to be temperature insensitive [1]. We have investigated the operating characteristics of 1.5μm InAs/InP (100) quantum dot lasers focusing on their carrier recombination characteristics using a combination of low temperature and high pressure measurements. By measuring the intrinsic spontaneous emission from a window fabricated in the n-contact of the devices we have measured the radiative component of the threshold current density, J_{rad}. We find that J_{rad} is itself relatively temperature insensitive (Fig. 1). However, the total threshold current density, J_{th}, increases significantly with temperature leading to a characteristic temperature T_0~55K around RT. From this data it is clear that the devices are dominated by a non -radiative recombination process which accounts for up to 94% of the threshold current at room temperature (Fig. 1).

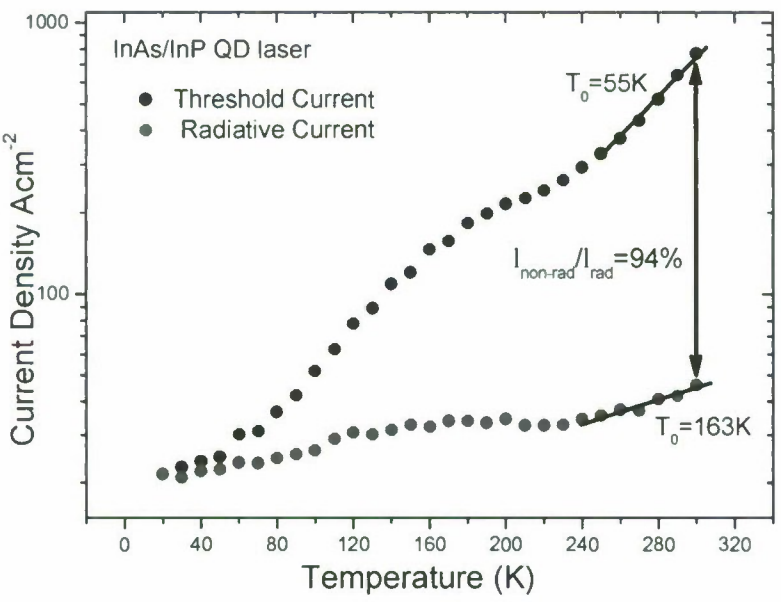

Fig. 1. J_{th} and J_{rad} as function of temperature

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Different carrier recombination processes have distinctive dependencies on the band gap, therefore hydrostatic pressure provides a robust tool to study the dominating proeesses since it allows one to reversibly vary the band gap of an operating device in the absence of other compositional changes [2, 3]. Fig. 2 shows that the lasing energy increases (reversibly) with pressure in the QD lasers with a pressure eoeffieient that is temperature insensitive, ~8meV/kbar.

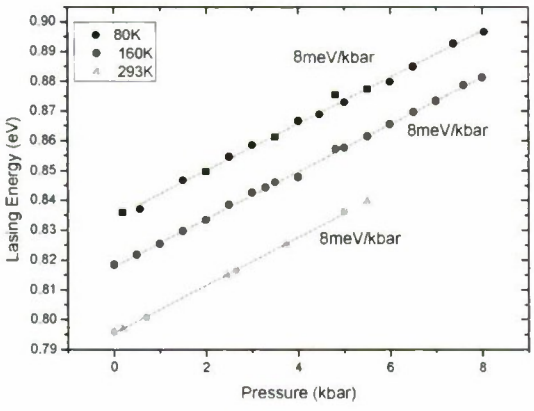

Fig. 2, Dependence of lasing energy on hydrostatie pressure and temperature for a quantum dot laser

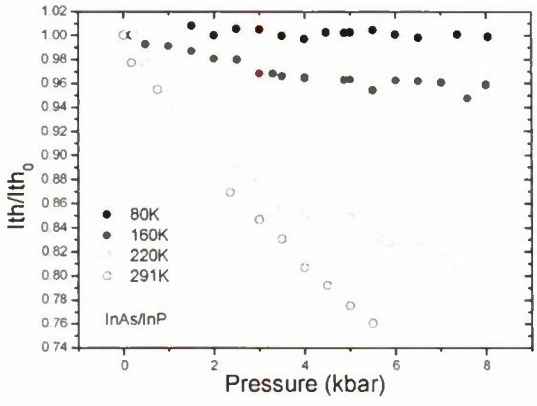

Fig. 3, Variation of threshold current with temperature and pressure for the QD lasers.

In Fig. 3, we plot the corresponding pressure and temperature dependence of the threshold current, normalised at atmospheric pressure. At room temperature, a strong decrease in threshold current is observed with increasing pressure, consistent with Auger recombination dominating as per previous findings on 1.5μm (311B) InAs/InP [2] and 1.3μm InAs/GaAs [3] QD lasers. With decreasing temperature, the rate of decrease in threshold eurrent with pressure reduces. This is exactly as one would expect due to the reduced importance of Auger recombination at lower temperature, as evidenced from the temperature dependenee data in Fig. 1. From these data it is clear that the thermal behaviour of these QD lasers is dominated under ambient conditions by Auger recombination.

In summary, we have investigated the temperature sensitivity of recombination processes in 1.5μm InAs/InP QD laser grown on (100) InP substrate using temperature dependent measurements on J_{th} and J_{rad} and hydrostatic pressure measurements of J_{th} and lasing wavelength to determine the dominant recombination processes. The temperature behaviour of J_{th} and J_{rad} and decrease in J_{th} with increasing pressure indicates that these devices are dominated by NR recombination processes which decrease strongly with increasing pressure and also decrease with decreasing temperature. The presence of NR recombination proeesses is consistent with the temperature dependence characteristics observed in Fig. 1 and Fig. 3. Therefore we conclude that Auger process is dominant NR recombination processes in these devices

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III-V MOSFETs: Scaling Laws, Scaling Limits, Fabrication Processes

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Abstract—III-V FETs are in development for both THz and VLSI applications. In VLSI, high drive currents are sought at low gate drive voltages, while in THz circuits, high cutoff frequencies are required. In both cases, source and drain access resistivities must be decreased, and transconductance and drain current per unit gate width must be increased by reducing the gate dielectric thickness, reducing the inversion layer depth, and increasing the channel 2-DEG density of states. We here describe both nm self-aligned fabrication processes and channel designs to address these scaling limits.

I. Introduction

III-V transistors of ~10 to 100 nm lithographic dimensions are being developed both for sub-mm-wave (0.3-3 THz) applications and for use in large-scale digital integrated circuits. Both applications demand improved transistor characteristics; both applications demand significant changes in the design and fabrication of the channel, of the source/drain access regions, and of the gate dielectric.

For application in VLSI, FET leakage currents must be low and drain drive current densities must be high despite low supply voltages. High intrinsic transconductance and low source / drain access resistivities are therefore required.

For application in THz ICs, high current-gain (f_t) and power-gain (f_{max}) cutoff frequencies are required. With present InGaAs HEMTs, f_t is limited by parasitic capacitance charging times which are only reduced by increasing the FET transconductance per unit gate width. As with the VLSI application, the drive current and transconductance must be increased and the source access resistance reduced.

THz InGaAs HEMTs and InGaAs MOSFETs thus face several similar design challenges. To increase the transconductance of both HEMTs and MOSFETs, the gate barrier must be thinned, which increases gate leakage. In VLSI application, gate leakage must be very small, and an MOS structure with a wide-gap (insulating) gate dielectric is required. Even for HEMTs used in THz ICs, the wide-gap gate barrier semiconductor layer has been thinned to the point where gate leakage reduces microwave power gain; better barriers are needed. In both devices high transconductance implies both high carrier velocities and high carrier densities in the 2-dimensional electron gas. Semiconductors with low carrier effective mass provide high carrier velocities yet low 2-D densities of states hence low carrier densities, high effective mass provides low velocities yet high carrier densities. [1] This limitation must somehow be addressed. Both devices need low access resistances. Both devices need thin channels both for high transconductance and for low output conductance.

Design challenges with THz InGaAs HEMTs and InGaAs MOSFETs also differ in key aspects. Unlike THz HEMTs, where overall device dimensions can be much larger than the gate length, in VLSI the device packing density must be high hence all device dimensions must be small. In particular, in VLSI the source/drain contacts must have dimensions comparable to the gate length, placing greater demands on low-resistivity source/drain contacts. Similarly, while in THz HEMTs the N+ drain can have a large offset from the gate to reduce drain electrostatic coupling and consequently output conductance, in MOSFETs for VLSI both density and logic design requirements force the N+ drain region to be placed adjacent to or under the gate. Electrostatic design and vertical scaling of the VLSI device is therefore more demanding.

We describe below our efforts to develop III-V MOSFETs for VLSI. Although III-V MOS gate dielectrics [2, 3] remain an area of intense development, we focus here on device design and on development of process flows for fabrication of nm devices. Since their low 2-dimensional density of states makes III-V channel materials uncompetitive for application in nm FETs, we also discuss modified III-V channel designs which address this limitation.

II. FET Scaling Laws

First consider FET scaling laws (Table 1) [4] . To increase bandwidth γ:1, capacitances and transit delays must be reduced γ:1 while maintaining constant voltages, currents, and resistances. In InGaAs FETs with L_g ~35 nm, the gate-source $C_{gs,f} \propto \varepsilon W_g$ and gate-drain $C_{gd} \propto \varepsilon W_g$ fringing capacitances are a *substantial* fraction of the total capacitance, and consequently limit

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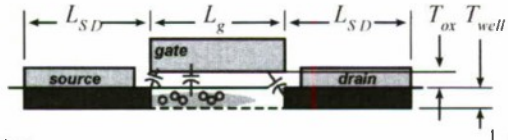
Table 1: Constant-voltage / constant-velocity FET scaling laws: changes required for γ:1 increased bandwidth in an arbitrary circuit



parameter	law	parameter	law
gate length L_g, source-drain contact lengths $L_{S/D}$ (nm)	γ^{-1}	electron density $n_s = (C_{g-ch}/L_gW_g)(V_{gs}-V_{th})/q$ (cm^{-2})	γ^{1}
gate width W_g (nm)	γ^{-1}	injection velocity (m/s) $v_{injection} = (4/3\pi)(2qC_{g-ch}(V_{gs}-V_{th})/m_{\parallel}C_{dos})^{1/2}$	γ^{0}
equivalent oxide thickness $T_{eq} = T_{ox}\varepsilon_{SiO_2}/\varepsilon_{oxide}$ (nm)	γ^{-1}	drain current $I_d = qn_s v_{injection}$ (mA)	γ^{0}
dielectric capacitance $C_{ox} = \varepsilon_{SiO_2}L_gW_g/T_{eq}$ (fF)	γ^{-1}	drain current density I_d/W_g (mA/μm)	γ^{1}
		transconductance $\partial I_d/\partial V_{gs}$ (mS)	γ^{0}
wavefunction mean depth T_{inv} (nm)	γ^{-1}	gate-source, gate-drain fringing capacitances $C_{gs,f} \propto \varepsilon W_g$, $C_{gd} \propto \varepsilon W_g$ (fF)	γ^{-1}
wavefunction depth capacitance $C_{depth} = \varepsilon_{semi}L_gW_g/T_{inv}$ (fF)	γ^{-1}	S/D access resistances R_s, R_d (Ω)	γ^{0}
DOS capacitance (ballistic case) $C_{dos} = q^2 g(m_{\parallel}^* m_{\perp}^*)^{1/2} L_gW_g/2\pi\hbar^2$ (fF)	γ^{-1}	S/D access resistivities R_sW_g, R_dW_g ($\Omega-\mu$m)	γ^{-1}
		S/D contact resistivities ρ_c ($\Omega-\mu m^2$)	γ^{-2}
gate-channel capacitance $C_{g-ch} = [1/C_{ox}+1/C_{depth}+1/C_{DOS}]^{-1}$ (fF)	γ^{-1}	temperature rise (one device, K)	$\sim W_g^{-1}$

f_τ. $C_{gs,f}$ and C_{gd} are only weakly dependent on lateral geometry, hence the $(C_{gs,f}+C_{gd})\Delta V/I_d$ delay is reduced γ:1 only if I_d/W_g is increased γ:1.

Consider drive current scaling in the ballistic limit. $I_d = qn_s v_{inj} W_g$ is determined by the carrier injection velocity v_{inj} and the sheet carrier concentration $n_s = (C_{g-ch}/L_gW_g)(V_{gs}-V_{th})/q$, where the gate-channel capacitance $C_{g-ch} = [1/C_{ox}+1/C_{depth}+1/C_{DOS}]^{-1}$ is the series combination of dielectric $C_{ox} = \varepsilon_{SiO_2}L_gW_g/T_{eq}$, wavefunction depth $C_{depth} = \varepsilon_{semi}L_gW_g/T_{inv}$ and density of states $C_{dos} = q^2 \cdot dn_s/dE_f$ capacitances. T_{inv} is here the wavefunction mean depth. In the ballistic case, $C_{dos} = q^2 g(m_{\parallel}m_{\perp})^{1/2} L_gW_g/2\pi\hbar^2$, where g is the # of populated valleys, and $m_{\parallel}$ and $m_{\perp}$ the effective masses parallel and perpendicular to transport; near equilibrium, C_{dos} is 2:1 larger. Given ballistic transport [5] and assuming degenerate carrier concentrations, $E_f - E_{well} >> kT$, $v_{inj} = (4/3\pi)(2(E_f-E_{well})/m_{\parallel})^{1/2} = (4/3\pi)(2qC_{g-ch}(V_{gs}-V_{th})/m_{\parallel}C_{dos})^{1/2}$. We scale by maintaining constant v_{inj} while reducing C_{ox}/L_gW_g, C_{depth}/L_gW_g, and C_{dos}/L_gW_g by γ:1 so as to increase n_s by γ:1. This requires fixed transport mass $m_{\parallel}$, T_{eq} and T_{inv} reduced γ:1, and C_{dos} increased γ:1 by increasing the # of valleys or the perpendicular mass.

The FET is scaled such that the on-state current density I_d/W_g (mA/μm) varies as γ^1 while the current per unit source and drain Ohmic contact area (mA/μm^2) varies as γ^2. It is well understood that difficulties in reducing T_{eq} (gate leakage by tunneling) will impede constant-voltage FET scaling; note also that T_{inv} must scale as γ^{-1}, requiring thinner wells or stronger confinement of the wavefunction in the well by strong vertical fields, and $(R_s+R_d)/W_g$ must scale as γ^{-1}, requiring a γ^2:1 reduction in contact resistivity ρ_c and increased carrier concentrations in the access regions. Design goals include low access resistance, high drive current density, thin wells, high sheet carrier density, and gate barriers that are both thin and high in energy.

To out-perform future scaled Si MOSFETs, drive currents must exceed 1-2 mA/μm at 300 mV gate overdrive $(V_{gs}-V_{th})$. We must develop Ohmic contacts of ~0.5 $\Omega-\mu m^2$ contact resistivity; this resistivity must not increase when operating ~150 mA/μm^2 current density, nor can the contact metals diffuse under such high current and thermal stress through device junctions only ~3-5 nm below the surface. T_{inv} must be at most 2-3 nm.

We describe our efforts to develop process to fabricate FETs having such parameters. We must also consider changes in the channel design necessary to enable the target high current densities.

III. Density-Of-States Limits And High Current Density Channels

We now examine the density-of-states limit to drive current and modified channel designs which address this limit.

Low transport mass produces high carrier velocities but low charge densities while high transport mass produces low carrier velocities but high charge densities. At a given dielectric thickness T_{equiv}, there is an optimum m^* maximizing I_d. We find

$$I_d/W_g = J_0 \cdot K_1 \cdot ((V_{gs}-V_{th})/1\text{V})^{3/2} \quad , \qquad (1)$$

where

$$J_0 = \left(\frac{4}{3\pi}\right)\left(\frac{2q}{m_0}\right)^{1/2}\left(\frac{q^2 m_0}{2\pi\hbar^2}\right)(1\text{ V})^{3/2} = 84 \text{ mA}/\mu\text{m} \qquad (2)$$

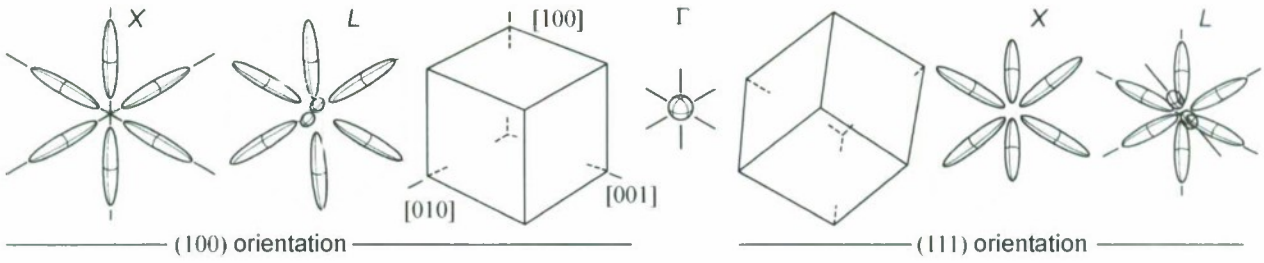


Figure 1: Γ, L, and X-valley orientations for (100)- and (111)-oriented wafers

Table 2 Parameters of Γ, L, and X-valleys for several suitable semiconductors

		Γ valley	X valleys*			L valleys		
material	substrate	m^*/m_0	m_l/m_0	m_t/m_0	$E_X - E_\Gamma$	m_l/m_0	m_t/m_0	$E_L - E_\Gamma$
$In_{0.5}Ga_{0.5}As$	InP	0.045	1.29	0.19	0.83 eV	1.23	0.062	0.47 eV
InAs	InP	0.026	1.13	0.16	0.87 eV	0.65	0.050	0.57 eV
GaAs	GaAs	0.067	1.3	0.22	0.47 eV	1.9	0.075	0.28 eV
GaSb	GaSb	0.039	1.51	0.22	0.30 eV	1.3	0.10	0.07 eV
Si	Si		0.92	0.19	(negative)	*Si minima at $\Delta \sim 0.85 \cdot \langle 100 \rangle$		

and

$$K_1 = \frac{n \cdot (m_\perp / m_0)^{1/2}}{(1 + (C_{dos,0}/C_{equiv}) \cdot g \cdot (m_\perp^{1/2} m_\parallel^{1/2} / m_0))^{3/2}} \qquad (3)$$

is the normalized current density. $C_{equiv} = [1/C_{ox} + 1/C_{inv}]^{-1}$ is C_{depth} and C_{ox} in series, while $C_{dos,0} = q^2 m_0 L_g W_g / 2\pi\hbar^2$. . Given one isotropic valley ($m_\perp = m_\parallel = m^*$, g=1) and 1 nm *total* equivalent dielectric thickness EOT (i.e. $C_{equiv} = \varepsilon_{r,SiO_2} L_g W_g / (1\,\text{nm})$), highest current is obtained for m^*/m_0=0.05, while for 0.3 nm EOT, peak I_d is obtained at m^*/m_0=0.2; given one isotropic valley, low m^* gives low I_d in nm FETs [6], though low m^* reduces transit time for any EOT. Note than for Si {100} FETs [6], m^*/m_0=0.19 and g=2.

Consider a 3 nm (100) GaAs well with strained AlSb barriers. The L bound states lie 177 meV above that of Γ. Equilibrium (not ballistic transport) analysis uses Schrödinger-Poisson, the effective mass approximation, and parabolic bands. 0.66 nm Al_2O_3 and 0.34 nm AlSb lie between the well and gate, giving T_{eq}=0.37 nm. Under strong inversion $C_{g-ch}/L_g W_g \cong 2.4$ μF/cm^2, far below $C_{ox}/L_g W_g$=9 μF/cm^2, and the high-mass L-valleys fill for $n_s > 2.4 \cdot 10^{12}$ cm^{-2}. Under ballistic transport, C_{dos} and the maximum n_s would both decrease 2:1.

Increased C_{dos} and low $m_\parallel$ can be obtained by using L valley minima alone or combined with the Γ valley. The InGaAs, GaAs, and GaSb L-valleys [7] have low m_t/m_0 (0.062-0.1) and high m_l/m_0 (1.23-1.9). The L-valleys have $\langle 111 \rangle$ orientations, and transport in a (100) channel includes contributions from the high m_l. Using instead a (111) wafer, the L[111] valley is oriented vertically, and shows low transport masses ($m_\parallel = m_\perp = m_t$) and high confinement mass ($m_q = m_l$). The L$[\bar{1}11]$,$[1\bar{1}1]$, and $[11\bar{1}]$ minima show high transport mass[6] $(m_t + 8m_l)/9$ in one in-plane direction, but low confinement mass [6] $m_q = 9m_t m_l/(m_t + 8m_l)$. The X valleys have $\langle 100 \rangle$ orientations, in bulk InGaAs, GaAs, and GaSb have minima well above Γ and L, and in a (111) well have low $m_q = 3m_t m_l/(m_t + 2m_l)$ quantization mass. In appropriate thin wells, the X and L$[\bar{1}11]$,$[1\bar{1}1]$, and $[11\bar{1}]$ quantized states are driven to high energies and depopulated. T_{well} can be selected to place Γ and L[111] at similar energies, doubling C_{dos}, or Γ driven in energy above L[111], and transport provided in multiple L[111] valleys.

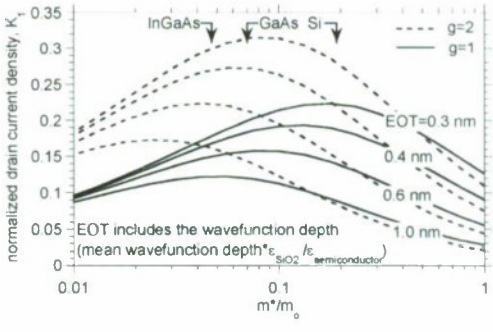


Figure 2: FET normalized drive current K_1 where $I_d/W_g = (84\,\text{mA}/\mu\text{m}) \cdot K_1 \cdot ((V_{gs} - V_{th})/1\text{V})^{3/2}$, and g is the # of valley minima.

Consider a 2.3 nm (111) GaAs well with strained AlSb barriers. m_q is large, thus the first two L[111] states are separated by only 84 meV. The Γ state lies 41 meV above the lower L[111] state; 3 valleys are populated over a 300mV range of V_{gs}. L$[\bar{1}11]$,$[1\bar{1}1]$, and $[11\bar{1}]$ and X lie 175 and 288 meV above the lower L[111] state. In equilibrium simulation n_s= $7 \cdot 10^{12}$ cm^{-2} with $V_{gs} - V_{th}$=300 mV, and moderately higher n_s does not populate heavy valleys. In inversion, $C_{g-ch}/L_g W_g \cong 4$ μF/cm^2. The benefit over the (100) design is larger in the ballistic case.

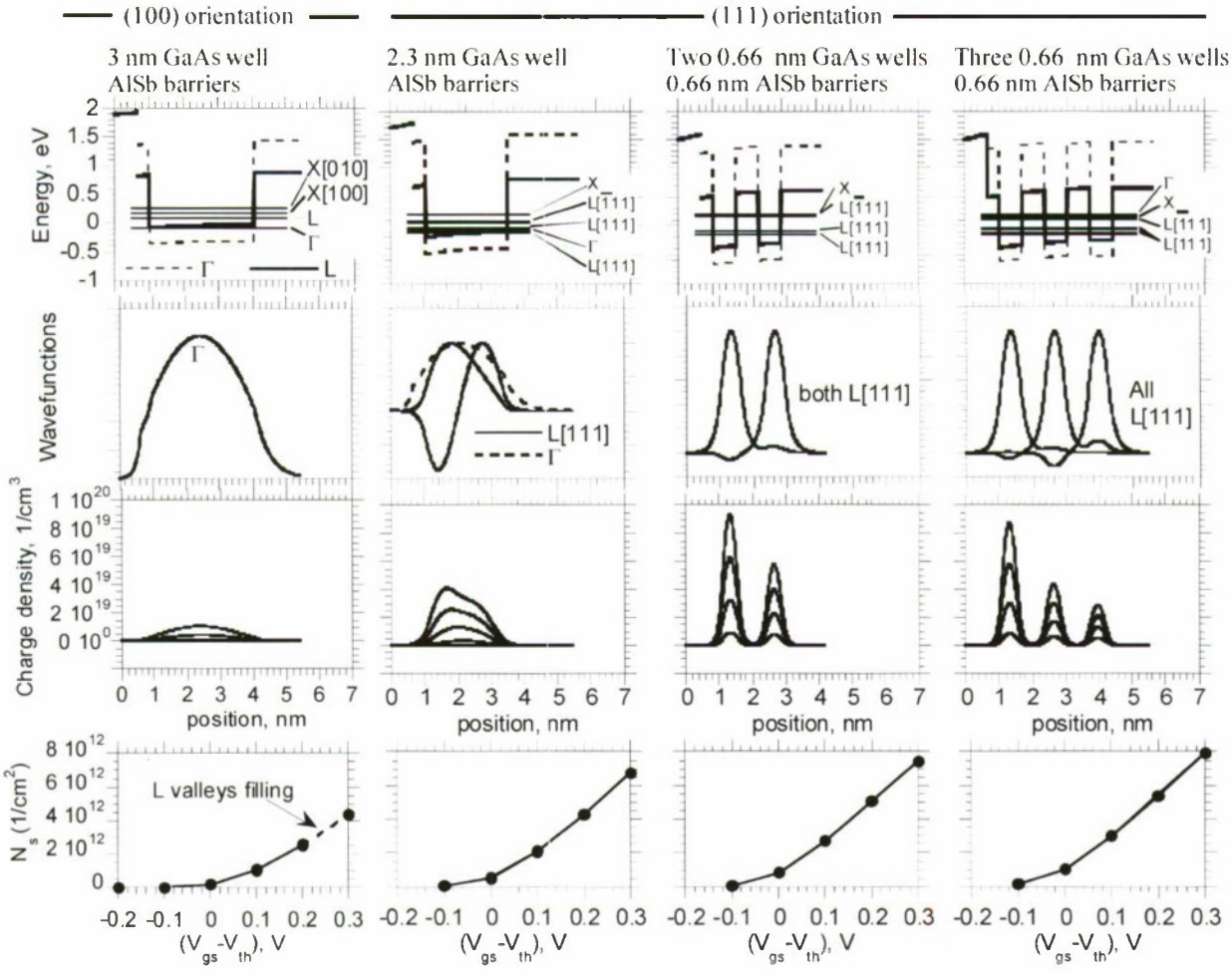


Figure 3: Simulation of Γ, Γ-L, and multiple-L valley FETs: quantized states, wavefunctions, charge density, and sheet carrier concentrations vs. bias. Well energies and charge densities calculated using the effective mass approximation and assuming parabolic bands. The gate dielectric is 0.3 nm Al_2O_3. Well charge densities are computed assuming thermal equilibrium; in the ballistic limit, C_{dos} is 2:1 smaller than in equilibrium, and multiple-valley FET channels provide a proportionally larger improvement in N_S. 0.66 nm is 2 monolayers.

In InGaAs, GaAs, and GaSb, the L-valley m_t is >25:1 larger than the Γ-valley mass, hence T_{well} can be made 5:1 smaller for a given quantization energy. m_q is high in the barriers, hence multiple wells can be placed between ~ 1 nm barriers without significant well coupling hence energy redistribution. Multiple L[111] quantum wells can stacked to increase g hence C_{dos}. Consider a FET with two 0.66 nm (2 ML) (100) GaAs wells separated by strained 0.66 nm AlSb barriers. Given zero field, the two L[111] states split in energy by < 40 meV; for $V_{gs} - V_{th}$ =300 mV the separation is 56 meV. L$[\bar{1}\,1\,1]$, L$[1\,\bar{1}\,1]$, and L$[1\,1\,\bar{1}]$ and X lie 322 and 346 meV above the lower L[111] state. The Γ state is driven to high energy. In equilibrium, n_s is driven to $7.8 \cdot 10^{12}$ cm^{-2} with $V_{gs} - V_{th}$~300 mV; moderately higher n_s does not populate heavy valleys. $C_{g-ch} / L_g W_g \cong 4\ \mu F/cm^2$. The advantage over Γ{100} is greater for ballistic transport. A triple- well L[111] design gives similar results. In these FETs, the upper wells charge most strongly because of charge division between the wells' C_{dos} and the well-well capacitance $C_{well} = \varepsilon L_g W_g / T_{pitch}$, where T_{pitch} is the well pitch. With thin wells, and low m_t, C_{dos} can be increased 1.5:1 to 2.2:1.

The designs above use very thin wells and barriers. It must be determined whether such layers can be grown and whether mobility is acceptable. The energy calculations must be refined. 2-4 ML GaSb and InAs wells [8,9] have been grown. Preliminary tightbinding calculations using an sp3d5s* basis [10] conducted for triple 1.1nm GaSb wells with 1.1nm AlSb barriers confirm the symmetry of the lowest state manifold and its expected transverse dispersion. Excited states are slightly lower than predicted by effective mass, but the design still appears viable. Experimental demonstration of such channel designs would enable III-V FETs to provide smaller carrier transit times and larger drive currents than Si MOSFETs even for gate dielectrics with equivalent thickness below 0.5 nm.

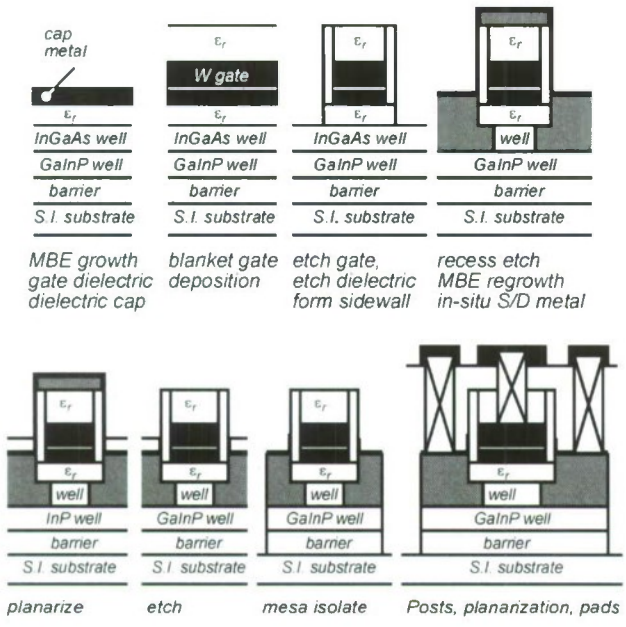


Figure 4: Process flow for III-V FETs with source/drain regrowth by MEE.

IV. Fabrication Processes For nm III-V MOSFETs

Established III-V HEMT structures do not well address scaling requirements of Section II. We have therefore developed a fully self-aligned InGaAs MOSFET process flow [11,12,13,14] (fig. 1). In this flow, 4.7 nm Al_2O_3 gate dielectric is deposited by ALD on a 5 nm $In_{0.53}Ga_{0.47}As$ channel, the gate is formed by blanket W/Cr/SiO_2 deposition and RIE etching, and thin ~25 nm Si_3N_4 gate sidewalls formed. After etching the Al_2O_3, self-aligned S/D InAs N+ regions (50 nm thick, 8×10^{19} cm^{-3}, 23 Ω sheet resistance) are formed by migration enhanced epitaxy, and self-aligned S/D contacts formed by in-situ blanket evaporation of Mo (1-3 $\Omega-\mu m^2$ contact resistance) and a subsequent height-selective etch [15]. Mesa isolation and back-end metal completes the process. Unlike HEMTs, no gate barrier is present in the S/D regions, the source and drain are fully self-aligned to the gate, and carrier densities in the S/D access regions are high ($\sim1.5\times10^{13}$cm^{-2}). Figure 3 shows measured I_D for a 200-nm-L_g device.

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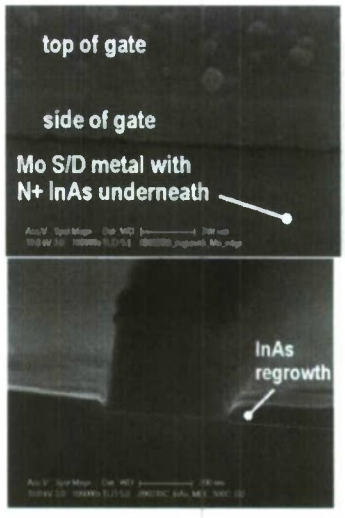

Figure 5: Regrown S/D InGaAs FET, oblique view & cross-section

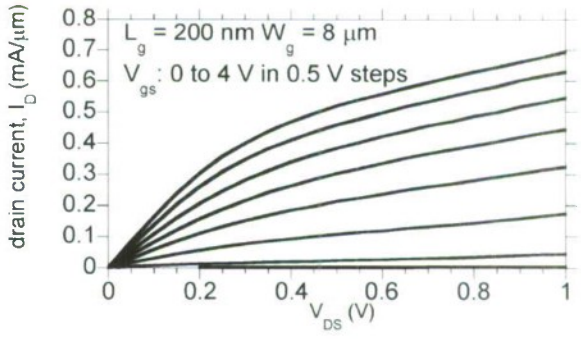

Figure 6: Common-source characteristics, 200 nm FET

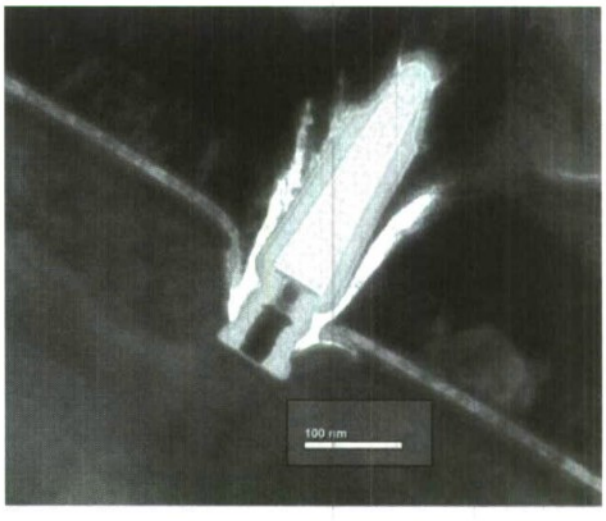

Figure 7: Cross-section of regrown S/D InGaAs FET with a 27 nm gate

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Scaling of InGaAs MOSFETs into deep-submicron regime (invited)

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We have demonstrated high-performance deep-submicron inversion-mode InGaAs MOSFETs with gate lengths down to 150 nm with record G_m exceeding 1.1 mS/μm. Oxide thickness scaling is performed to improve the on-state/off-state performance and G_m is further improved to 1.3 mS/μm. HBr pre-cleaning, retro-grade structure and halo-implantation processes are first time introduced into III-V MOSFETs to steadily improve high-*k*/InGaAs interface quality and on-state/off-state performance of the devices. We have also demonstrated the first well-behaved inversion-mode InGaAs FinFET with ALD Al_2O_3 as gate dielectric using novel damage-free etching techniques. Detailed analysis of SS, DIBL and V_T roll-off are carried out on FinFETs with L_{ch} down to 100 nm and W_{Fin} down to 40 nm. The short-channel effect (SCE) of planar InGaAs MOSFETs is greatly improved by the 3D structure design. The result confirms that the newly developed dry/wet etching process produces damage-free InGaAs sidewalls and the high-k/3D InGaAs interface is comparable to the 2D case. Finally, ultra-shallow doping for V_T adjustment in deep submicron InGaAs MOSFETs using sulfur monolayers is demonstrated. This brings new potential solution to ultra-shallow junction formation for the further scaling of III-V MOSFETs.

I. Introduction

In the quest for perfect dielectrics for III-V semiconductors, significant progress has been made recently on inversion-type enhancement-mode InGaAs NMOSFETs, operating under the same mechanism as Si MOSFETs, using high-k gate dielectrics. The promising dielectric options include ALD Al_2O, HfO_2, HfAlO, ZrO_2 and in-situ MBE $Ga_2O_3(Gd_2O_3)$. Most recently, record-high inversion current above 1 A/mm has been achieved for long-channel Al_2O_3/InGaAs MOSFETs. In order to further verify the potential of scaling of the InGaAs MOSFETs towards the deep-submicron regime, we have made the surface channel inversion-type InGaAs MOSFETs with gate lengths down to 150 nm using electron beam lithography (EBL), and performed various techniques including oxide thickness scaling, channel engineering, novel surface treatment and 3-dimensional InGaAs FinFET with Fin width down to 40nm. These devices are compared in terms of the on-state performance and off-state performance. The results show that these InGaAs surface channel MOSFETs have great potential for next generation high performance applications.

II. Oxide Thickness Scaling of InGaAs MOSFETs

Fig.1 illustrates the cross section of an ALD $Al_2O_3/In_{0.75}Ga_{0.25}As$ MOSFET. A 500 nm p-type 4×10^{17} /cm^3 buffer layer, a 300 nm p-type 1×10^{17} /cm^3 $In_{0.53}Ga_{0.47}As$ layer, and a 12 nm strained p-type 1×10^{17} /cm^3 $In_{0.75}Ga_{0.25}As$ channel were sequentially grown by molecular beam epitaxy on a 2-inch p$^+$-InP wafer. Fig. 2 shows the process flow for the Inversion-type Enhancement-mode InGaAs MOSFET. After surface cleaning and ammonia passivation, the wafers were transferred via room ambient to an ASM F-120 ALD reactor. A 10 nm thick Al_2O_3 encapsulation layer was deposited at a substrate temperature of 300°C. All patterns were defined by a Vistec VB-6 UHR EBL system. The source and drain regions of the MOSFETs were formed by selective implantation of 1×10^{14} cm^{-2} at 20 keV Si and annealed at 600°C - 700°C for 10 s in N_2 for activation. Relatively low implantation energy was chosen here to avoid the penetration of implanted Si ions through the 280 nm thick electron beam resist used to protect the channel regions.

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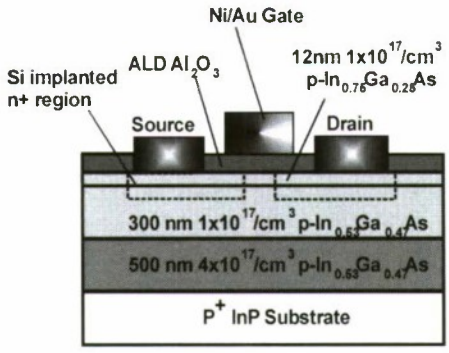

Fig. 1 Cross-section schematic view of InGaAs MOSFET.

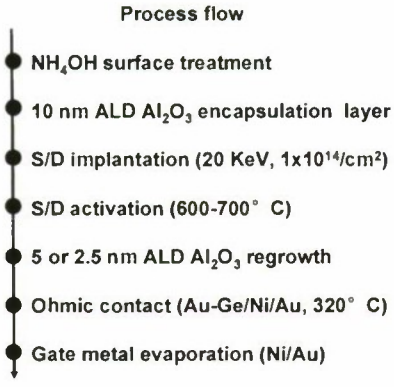

Fig. 2 Process flow of the Inversion-type Enhancement-mode InGaAs MOSFET.

After treated with $(NH_4)_2S$ solution for 10 minutes, another 5 nm Al_2O_3 or 2.5 nm Al_2O_3 was also grown by ALD after stripping away the encapsulation oxide layer. The ohmic source and drain contacts were made by electron-beam evaporation of AuGe/Ni/Au and annealing at 320°C for 30 s in N_2. The gate electrode was made by electron-beam evaporation of Ni/Au. The fabricated MOSFETs have nominal gate lengths L_g of 100, 110, 120, 130, 140, 150, 160, 170, 180 and 200 nm defined by the source-drain implant separation. The device process is not self-aligned.

The oxide thickness scaling has been introduced to explore the potential for the complete scaling. Reduction of Al_2O_3 down to 2.5 nm (EOT≈1nm) can improve the electrostatic control of the channel significantly, and can increase the electric field to the semiconductor surface at similar voltage supply. A typical 160 nm-gate-length inversion-mode $In_{0.7}Ga_{0.3}As$ NMOSFET with 5 nm Al_2O_3 as gate dielectric shows a I_{dss} of 840 μA/μm and peak G_m of 650 μS/μm at maximum supply voltage of V_{DD}=1.6 V. The contact resistance R_C of 350 Ω·μm is measured by TLM. After subtracting the contact resistance, the resulting intrinsic G_m is as high as 840 μS/μm. A similarly finished 160 nm-gate-length inversion-mode $In_{0.7}Ga_{0.3}As$ NMOSFET with 2.5 nm Al_2O_3 as gate dielectric shows I_{dss} of 810 μA/μm and peak G_m of 1100 μS/μm at maximum supply voltage of V_{DD}=1.6 V. After subtracting the contact resistance, the resulting intrinsic G_m is as high as 1790 μS/μm. The V_T shifts positively almost 0.5V as can be seen in the later part of this paper.

Fig. 3 compare I_{dss} and G_m of 2.5 nm and 5 nm Al_2O_3 devices without HBr treatment at V_{DD}=1.6V. Record high extrinsic transconductance G_m of 1.3 mS/μm is reached at L_{ch}=150 nm. Both the I_{dss} and G_m of the 2.5nm devices are significantly improved over the 5nm devices. Especially for the transconductance, the improvement is more than 50% for long channel devices and more than 80% for the shorter channel devices (channel lengths less than 170 nm). This shows the great potential InGaAs MOSFETs have in terms of the gate stack scaling.

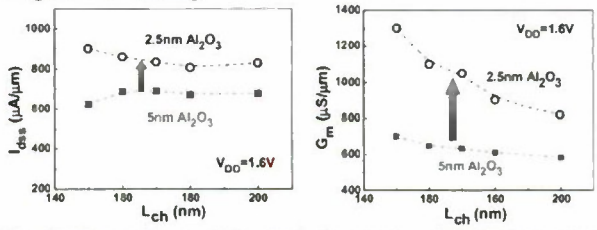

Fig. 3 Comparison of I_{dss} and G_m vs L_{ch} for devices with 2.5nm and 5nm thick gate dielectrics w/o HBr pretreatment and at V_{ds}=1.6V

Improved off-state characteristics are summarized in Fig. 4. S.S. improves through the better gate control by reducing the effect from the interface trap capacitance. Both the SS and DIBL show great potential to be further improved to be comparable with Silicon with better gate control. This comparison shows the potential of both on-state and off-state performance of the deep-submicron InGaAs MOSFETs for logic applications. The availability of even higher dielectric constant material, i.e., ALD $LaLuO_3$ (k=24-26), provides a pathway to further scale down the InGaAs MOSFETs.

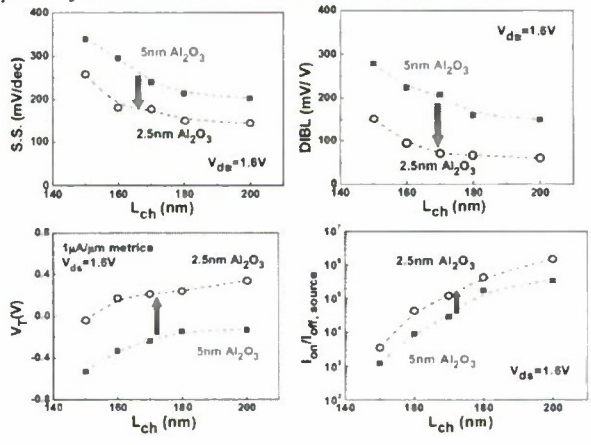

Fig. 4 Comparison of SS, DIBL, V_T and I_{on}/I_{off} vs. L_{ch} for the devices with 2.5nm and 5nm Al_2O_3.

III. Novel HBr Surface Pretreatment for InGaAs MOSFETs

The interface quality between the gate oxide and III-V

channel material is commonly regarded as one of the major challenges for high performance III-V MOSFETs. Although the ALD process has a self cleaning mechanism and can effectively reduce the interface trap density, it is one of the major causes for degrading transistor performance due to the contribution of C_{it}. To further improve the interface quality between ALD oxide and InGaAs channel, novel HBr / $(NH_4)_2S$ has been proposed in order to get better on-state performance as well as off-state performance.

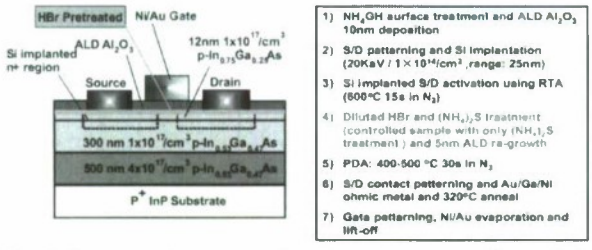

Fig. 5 Cross section schematic view and process flow of the HBr treated InGaAs MOSFET

Fig. 5 show the schematic cross section of HBr treated MOSFETs. ALD Al_2O_3 as gate dielectric was grown directly on MBE InGaAs surface. A 500 nm p-doped 4×10^{17} cm^{-3} buffer layer, a 300 nm p-doped 1×10^{17} cm^{-3} $In_{0.53}Ga_{0.47}As$ and a 12 nm 1×10^{17} cm^{-3} $In_{0.7}Ga_{0.3}As$ channel layer were sequentially grown by MBE on a 2-inch InP p+ substrate for all samples except for the retro-grade sample. The process flow is shown in Fig. 14. After surface degreasing and ammonia-based native oxide etching, the wafers were transferred via room ambient to an ASM F-120 ALD reactor. A 10 nm thick Al_2O_3 layer was deposited at a substrate temperature of 300 °C as an encapsulation layer after NH_4OH treatment. Source and drain regions were selectively implanted with a Si dose of 1×10^{14} cm^{-2} at 20 keV through the 10 nm thick Al_2O_3 layer. The implantation condition was chosen carefully to achieve the desired junction depth and S/D doping concentration. Implantation activation was achieved by rapid thermal anneal (RTA) at 600 °C for 15 s in a N_2 ambient. After removing the 10nm oxide in BOE, HBr / $(NH_4)_2S$ combination was used as the novel pretreatment and followed by another 5nm Al_2O_3 growth by ALD. HBr treated InGaAs surface is hydrophilic and is believed to be helpful to passivate InGaAs surface from surface recombination velocity measurements [16]. And it is expected to improve interface properties and the output performance. After 400-500 °C PDA process, the source and drain ohmic contacts were made by an electron beam evaporation of a combination of AuGe/Ni/Au and a lift-off process, followed by a RTA process at 320 °C for 30 s also in a N_2 ambient. The PDA temperature cannot exceed 500°C, as the remaining Sulfur atoms on the interface will be activated and serve as an n-type doping at temperatures above 600°C. The gate electrode was defined by electron beam evaporation of Ni/Au and a lift-off process.

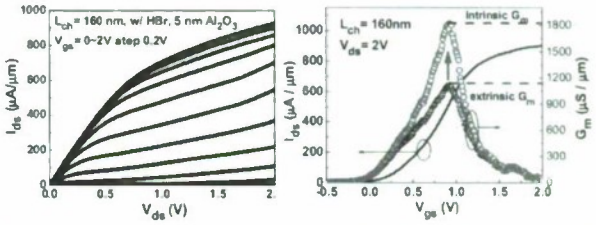

Fig. 6 output and transfer characteristic of an HBr treated 160 nm InGaAs MOSFET with 5nm Al_2O_3.

A well-behaved I-V characteristic of a 160 nm-gate-length inversion-mode $In_{0.7}Ga_{0.3}As$ NMOSFET with 5 nm Al_2O_3 as gate dielectric is demonstrated in Fig. 6 with I_{dss} of 925 μA/μm and peak G_m of 1.1 mS/μm at maximum supply voltage of V_{DD}=2.0V. The contact resistance R_C of 350 Ω·μm is measured by TLM. After subtracting the contact resistance, the resulting intrinsic G_m is as high as 1.8 mS/μm.

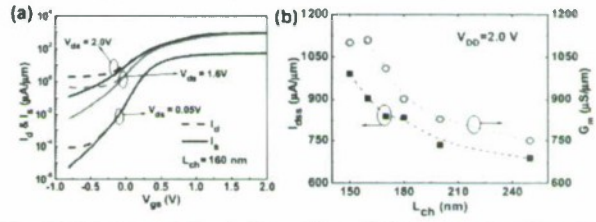

Fig. 7 (a) I_d and I_s at three V_{ds} of the same $In_{0.7}Ga_{0.3}As$ MOSFET with L_{ch}=160nm. (b) scaling characteristics of maximum drain current and peak transconductance vs L_{ch}

Fig. 7(a) shows I_d and I_s at V_{ds}=2.0V, 1.6V and 0.05V, respectively. It is clear that I_{sub} (the reverse-biased pn-junction leakage current) determines the leakage floor and I_d at $V_{gs} < 0$ as discussed before caused by the implantation and activation steps. The off-state is thus affected adversely by this parasitic effect. There is no Fermi-level pinning at $V_{gs} < 0$ since the gate still controls the channel well as shown in Is with 7-8 orders of magnitude change with the gate bias. The analysis on I_s reflects more accurately the intrinsic properties of devices by avoiding the substrate leakage. The major contribution of the difference of drain and source current comes from the non-optimized S/D junctions, which can be improved by the refined implant condition and following thermal activation. Fig. 7(b) summarizes the increase of I_{dss} and G_m, the on-state performance, versus the channel length L_{ch} from 250 nm to 150 nm. The maximum drain current changes from 700 μA/μm to 1 mA/μm and peak transconductance changes from 750 μS/μm to more than 1 mS/μm as the gate length scales. It shows pretty good trend of increasing output performance while scaling the channel length, which is promising for further scaling into the nanometer regime.

IV. Channel Engineering for InGaAs MOSFETs

Channel engineering–retro-grade structure and halo-implantation–has been studied to further improve off-state performance. The underlying heavily doped InGaAs layer beneath the channel of the retro-grade structure would

improve the S/D punch-through. The halo-implantation was performed by implanting Zn with ±30 degree angles to the normal.

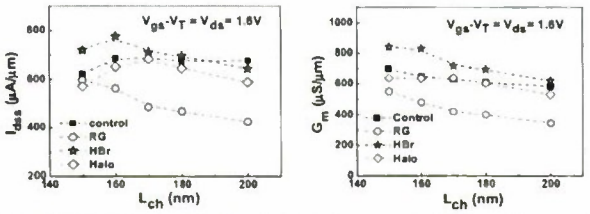

Fig. 8 Comparison of I_{dss}, G_m vs L_{ch} for 4 different types of channel engineering.

Fig. 8 summarize I_{dss} and G_m of 4 different types of devices with 5 nm Al_2O_3 at all L_{ch} measured. Uniform channel as shown in Fig. 1 without HBr pretreatment is used as a control sample. HBr treated sample (without channel engineering) has the best on-performance among the four and is attributed to the improved interface. Both retro-grade sample and halo-implanted sample are degraded on-current and peak G_m, which are expected from inducing scattering and reducing channel mobility. This is a trade-off for the improved off-state performance such as S.S. and DIBL as demonstrated in Fig. 9.

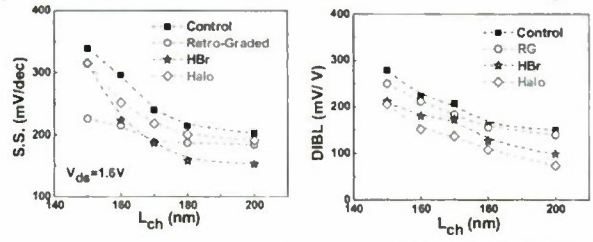

Fig. 9 Comparison of SS, DIBL vs L_{ch} for 4 different types of channel engineering

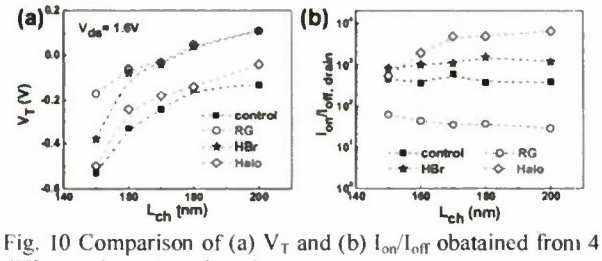

Fig. 10 Comparison of (a) V_T and (b) I_{on}/I_{off} obatained from 4 different channel engineering.

Fig. 10(a) shows V_T vs L_{ch} using I_{ds}=1μA/μm metrics at V_{ds}=1.6V. The typical roll-off of V_T at shorter gate lengths is also observed here. All treated samples have better V_T roll-off than control sample. Fig. 10(b) summarizes I_{on}/I_{off} vs L_{ch} of 4 different types of devices from I_d. I_{on}/I_{off} is chosen as I_{on} (V_{ds}=1.6V, V_{gs}=2/3V_{ds}+V_T)/I_{off} (V_{ds}=1.6V, V_{gs}=-1/3V_{ds}+V_T), where V_T is determined by 1μA/μm metric. The similar definition is also used for Is. Junction leakage is the dominant factor currently for I_d at V_{gs}<0 or I_{off}. For retro-grade sample, I_{sub} or I_{off} is higher due to heavily p-doped 2×10^{18}/cm^3 layer in source/drain. This junction leakage mainly comes from the non-optimized S/D junctions after implantation and activation which can be greatly improved by better control of the process. If eliminating the junction leakage or I_{on}/I_{off} taken from I_s, I_{on}/I_{off} is improved to 104-106 at 150-200 nm gate lengths. Without considering the contribution from short-channel effect, with the lowest S.S. of 126 mV/dec. For HBr treated samples at V_{ds}=0.05V, the upper limit for interface trap density D_{it} is 2.8×10^{12}/cm^2-eV. The short-channel effect will significantly degrade SS when the gate lengths get shorter. The first pitfall introduced in calculating D_{it} directly from SS comes from SCE, especially in the deep submicron region. The deteriorating of SS for short devices could be attributed to the enhanced SCE by adding a term of CGD, which is a function of drain induced barrier lowering. With DIBL of less than 100 mV/V, it is reasonable to assume the SCE is minimized for 250 nm long device. More detailed interface characterizations by CV and GV methods are on-going to more accurately to determine the interface properties of the deeply scaled InGaAs MOSFETs.

V. 3D structure: InGaAs FinFET

With the continuous request of carrier transport boosting in CMOS devices, very recently, much progress has been made on achieving on-state performance of inversion-mode In–rich InGaAs MOSFETs using high-k gate dielectrics. However, the off-state performance of InGaAs MOSFETs is far from satisfactory according to ITRS requirement. The short-channel effect (SCE) of InGaAs MOSFETs deteriorates more quickly than Si MOSFETs due to its nature of narrower bandgap and higher semiconductor dielectric constant. In order to achieve better gate control capability, new structure design like FinFET demonstrated successfully in Si devices, is strongly needed for short-channel III-V MOSFETs. However, unlike Si, the dry etching of III-V semiconductor surface has been believed to be difficult and uncontrollable, especially related with surface damage and integration with high-k dielectrics. In this paper, we report for the first experimental demonstration of inversion-mode $In_{0.53}Ga_{0.37}As$ tri-gate FinFET using damage-free etching and ALD Al_2O_3 as gate dielectric. The SCE is greatly suppressed in terms of SS, DIBL and V_T roll-off. Detailed analysis and comparison are performed on the FinFETs with channel length (L_{ch}) from 200 nm to 100 nm, fin width (W_{Fin}) from 100 nm to 40 nm, and fixed fin height (H_{Fin}) of 40 nm. The reduction in the SCE shows the great promise for InGaAs transistors to continue scale into the sub-100nm regime. Fig. 11 shows the schematic cross section of the uniform device structure and the device fabrication flow. A 500 nm p-doped 2×10^{18} cm^{-3} InP layer, a 300 nm p-doped 2×10^{16} cm^{-3} and a 40 nm 2×10^{16} cm^{-3} $In_{0.53}Ga_{0.47}As$ channel layer were sequentially grown by MBE on a 2-inch InP p+ substrate. The heavily doped InP layer beneath the channel was chosen to prevent punch through and reduce substrate leakage because of its higher bandgap.

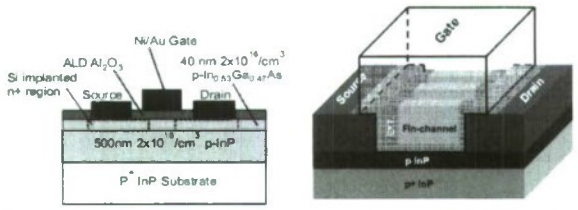

Fig. 11 Cross section schematic view and 3-dimensional schematic view of the InGaAs FinFET

Due to the non-optimized source/drain junctions, the heavily doped InP layer resulted in worsen junction leakage. After surface degreasing and ammonia-based native oxide etching, the wafers were transferred via room ambient to an ASM F-120 ALD reactor.. A 10 nm thick Al_2O_3 layer was deposited at a substrate temperature of 300°C as an encapsulation layer. Source and drain regions were selectively implanted with a Si dose of 1×10^{14} cm^{-2} at 20 keV through the 10 nm thick Al_2O_3 layer. The implantation condition was chosen carefully to achieve the desired junction depth and S/D doping concentration. Implantation activation was achieved by RTA at 600 °C for 15 s in a nitrogen ambient. The reduction of activation temperature from 750 °C to 600 °C resulted in much improved S/D junction leakage while achieving similar activation efficiency.

A combined dry and wet etching was used to pattern the fin structures. High-density plasma etcher (HDPE) BCl_3/Ar was used for dry etching at the chamber pressure of 2 mTorr. The gas flow of BCl_3/Ar is 15 sccm/ 60 sccm and the RF source power and bias power is 100 w and 50 w, respectively. The achieved etching rate for InGaAs under this condition is estimated to be 20nm / min. The positive E-beam resist ZEP-520A was used as an etching mask in this case. To achieve the desired small feature of 40nm, the original ZEP 520A resist was diluted with A-thinner (anisole) at the ratio of 1:0.7. The resist thickness of the diluted ZEP 520A is around 200nm at a spinning speed of 2000 rpm. A short dip of 3 seconds in diluted H_2SO_4:H_2O_2:H_2O (1:8:400) solution was carried out immediately after the dry etching to remove the damaged surface layer. The resulted fin channels have a depth of 40 nm which can be seen from the last SEM image in Fig. 12.

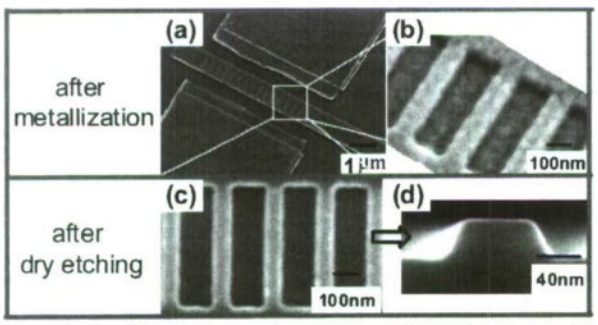

Fig. 12 (1) Tiled SEM of a finished FinFET device (b) Zoomed in image of the channel region with gate dieleetric and gate metal (c) SEM image of the Fin structure after dry etching (d) Cross section SEM image of a Fin after dry etching

More sophisticated process is needed to make the fin side-walls perfectly vertical. A 5 nm Al_2O_3 film was regrown by ALD after removing the encapsulation layer by BOE solution and $(NH_4)_2S$ surface preparation. After 400-500 °C PDA process, the source and drain ohmic contacts were made by an electron-beam evaporation of a combination of AuGe/Ni/Au and a lift-off process, followed by a RTA process at 320 °C for 30 s also in a N_2 ambient. The gate electrode was deposited by electron- beam evaporation of Ni/Au and a lift-off process. The fabricated MOSFETs have a nominal gate length varying from 100 nm to 150 nm and fin widths from 40 nm to 100 nm. From the SEM images of Fig. 12 (a) and (b), the gate metal covers uniformly on the parallel multi-fin channels. All patterns were defined by a Vistec VB-6 UHR electron-beam lithography (EBL) system. A Keithley 4200 was used for MOSFET output characteristics. The combined dry and wet etching for the formation of fin channels results in damage-free sidewalls. It is verified by the carrier transport through the fin channels without any significant degradation, compared to the planar devices. Fig. 13 depict the well-behaved output characteristic of a FinFET with 40 nm and 100nm W_{Fin} at same channel length of 100nm. There is no significant reduction of drain current even when the fin width is reduced down to 40 nm dimension. Note the current density is scaled by the fin width plus 2 x fin heights. Fig. 14(a) shows the typical output characteristics of a planar 100 nm-long MOSFET. It cannot be turned off at zero gate bias due to the SCE. Fig. 14(b) depicts the well-behaved output characteristic of a FinFET with 40 nm W_{Fin} at same channel length. From the comparison, it clearly shows the FinFET has much better behaved output characteristics in terms of off-state while maintaining the on-state performance compared to the planar device.

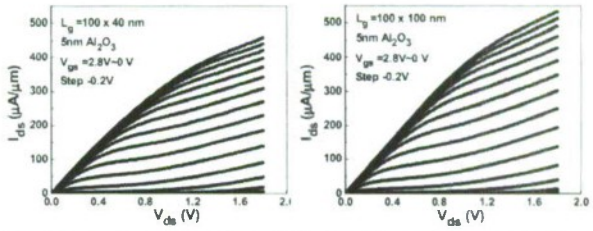

Fig. 13 I_{ds} vs V_{ds} of a FinFET with L_{ch}=100nm and W_{fin} = 40nm or 100nm.

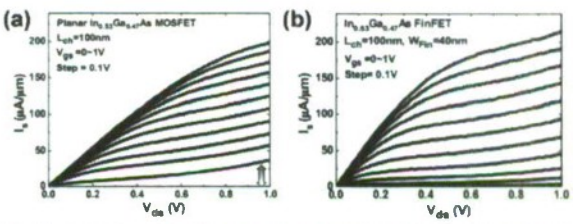

Fig. 14 I_s vs V_{ds} of a (a) Planar MOSFET with L_{ch}=100nm and (b) FinFET device with L_{ch} =100nm and W_{Fin}=40nm.

SS from the saturation region as well as DIBL are compared among FinFETs with 4 different WFin from 40 nm to 100 nm and the planar FET in Fig. 15. The trend shows the

device with narrower WFin has better SS and DIBL as expected. The SS of FinFET with 100 nm channel length improves more than 34% percent and degrades much slower when channel length gets shorter. The DIBL is greatly reduced from 440 mV/V for the planar device to 180 mV/V for the FinFET at 100 nm gate length.

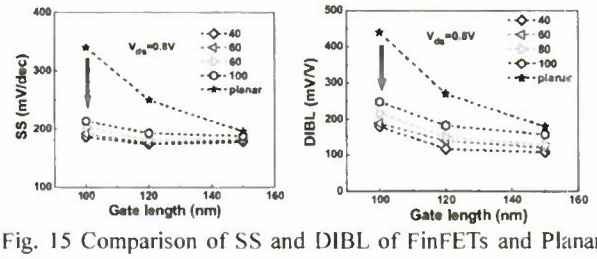

Fig. 15 Comparison of SS and DIBL of FinFETs and Planar FETs.

In order to evaluate the sidewall quality after the dry/wet etching, it is common to estimate the interface trap density (D_{it}) from SS. The channel surfaces of FinFET should be not better than the planar devices, if not worse after going through all the patterning and etching processes. From Fig. 36, it is clear that the SS is not only affected by interface trap density, but also by SCE. Simple estimation of D_{it} from SS would result in gross overestimation. The results show the linear region, similarly as in saturation region, SS of FinFETs are lower than those from the planar FET even in the 150 nm channel device which has small SCE. This indicates that the interface properties of Al_2O_3/InGaAs on the etched sidewalls are not degraded much by the Fin etching process, or D_{it} on the sidewalls is not much larger than that on the planar structures. It verifies that the newly developed dry/wet etching process is *damage-free* and suitable for 3D III-V device fabrication. The upper limit of average D_{it} on the top and sidewall surfaces in $In_{0.53}Ga_{0.47}As$ FinFET is $1.7x10^{12}/cm^2$-eV. The similar trend is also observed from the simple calculation of SS vs. W_{Fin}/L_{ch} as a function of D_{it}. The result confirms that the newly developed dry/wet etching process produces damage-free InGaAs sidewalls and the high-k/3D InGaAs interface is comparable to the 2D case.

VI. Sulfur doping effect for V_T adjustment

We study the thermal stability of the $(NH_4)_2S$ treatment by adding two different S activation annealing step in our gate-last $In_{0.75}Ga_{0.25}As$ devices. After S/D activation at 600°C and removing the encapsulation Al_2O_3 layer, $(NH_4)_2S$ solution is used to passivate the surface. The samples were transferred to an ALD chamber immediately for 5nm ALD regrowth. Previous XPS studies show that after ALD growth, part of sulfur still exists at high-*k*/III-V interface. Two different S activation anneal were carried out at 400°C or 600°C after gate oxide deposition. Fig. 16 (a) shows the linear regime threshold voltage extracted for these gate-last devices. Devices annealed at 600°C with variable gate lengths exhibits a ~-0.35V V_T shift compared to the ones anncaled at 400°C. This is consistent with the split CV measurement results shown in Fig. 16 (b), showing a similar negative V_T shift on the C_{gs}-V_g curve. This indicates that the PDA process at 600°C partially activated the S layer at the interface, introducing extra negative charge that promotes inversion.

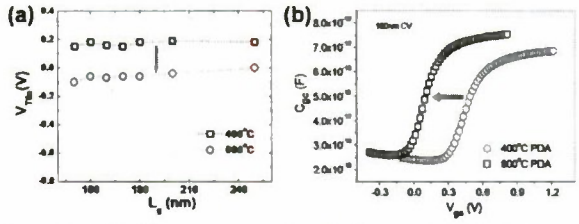

Fig. 16 (a) linear extrapolated V_T and (b) Split CV measurement of gate-last InGaAs devices with 400°C or 600°C PDA after gate oxide deposition.

In conclusion, threshold voltage adjustment has been realized by activating the sulfur surface layer. The same technique can be used to form ultra-shallow junctions of S/D, providing a solution for the further scaling of III-V MOSFETs.

VII. Conclusion

In summary, we have demonstrated high-performance deep-submicron inversion-mode InGaAs MOSFETs with record G_m exceeding 1.1 mS/μm. HBr pre-cleaning, retro-grade structure and halo-implantation processes are first time introduced into III-V MOSFETs to steadily improve high-k/InGaAs interface quality and on-state/off-state performance of the devices. We have also demonstrated the first well-behaved inversion-mode InGaAs FinFET with ALD Al_2O_3 as gate dielectric. Detailed analysis of SS, DIBL and V_T roll-off are carried out on FinFETs with L_{ch} down to 100 nm and W_{Fin} down to 40 nm. The SCE of planar InGaAs MOSFETs is greatly improved by the 3D structure design. Much more work on high-k/InGaAs interface and InGaAs ultra-shallow junction are needed to make III-V an alternative technology at CMOS 15 nm technology node.

Acknowledgment

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Submicron InP/InGaAs Composite Channel MOSFETs with Selectively Regrown N^+-Source/Drain Buried in Channel Undercut

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Abstract

We demonstrated a high-mobility InP 5 nm/InGaAs 12 nm composite channel MOSFET with MOVPE regrown n^+-source/drain region for low series resistance and high source injection current. A gate dielectric was SiO_2 and thickness was 20 nm. A carrier density of regrown InGaAs source/drain layer was over 4×10^{19} cm^{-3}. In the measurement of submicron (= 150 nm) device, the drain current was 0.93 mA/μm at V_g = 3 V, V_d = 1 V and the peak transconductance was 0.53 mS/μm at V_d = 0.65 V, respectively. The channel length dependence of transconductance indicated the good relativity.

I. Introduction

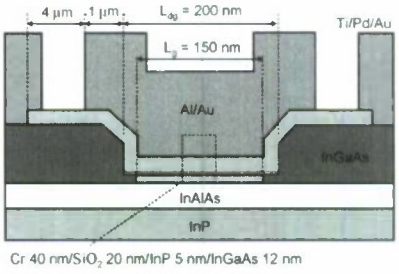
ITRS2009 (1) suggested that, III-V semiconductor device technology will potentially be introduced in LSI technology to realize circuits having capabilities superior to those of current CMOS circuits. Logic applications using III-V devices have already been researched. Conventional InP-based transistors with HEMT device structures have been fabricated (2). Furthermore, III-V MOSFETs with high-k dielectrics have been studied recently (3)–(6).

The ITRS stated that MOSFETs will be expected to have a saturation drain current (I_d) that is as high as 2 A/mm. To satisfy this requirement using a III-V channel, the source doping concentration must be greater than ~5×10^{19} cm^{-3} (7).However, this is difficult to realize using ion implantation technologies for III-V materials. A possible solution is a MOSFET with regrown source and drain(S/D) structures (8), (9) so that the transconductance (g_m) and I_d are high; such MOSFETs can be used to realize high-speed and low-power-consumption devices.

Previously, we have demonstrated InP/InGaAs MOSFETs with a laterally buried-regrown S/D structure and a gate length of 6 μm (10). However, I_d and g_m were not so high because of its long channel length. Here, we report a submicron channel (= 150 nm) MOSFET with a heavily doped (>4×10^{19} cm^{-3}) regrown S/D and InP 5 nm/InGaAs 12 nm composite channel structure.

II. Device structure and fabrication process

Figure 1 shows (s) a schematic image and (b) layer profiles of the fabricated MOSFET. In this research, InP 5 nm/InGaAs 12 nm composite channel structure was selected to suppress the effect of surface roughness scattering and to improve the interface characteristics between a channel and a gate dielectric. The channel InGaAs was grown on InAlAs barrier layer to make the quantum well channel structure for electrical confinement. The submicron gate length was designed by electron beam (EB) lithography and other structures were formed by contact UV lithography.



(a) schematic image of device structure

Gate stack	Source/Drain
-	Au 160nm
Au 160nm	Pd 20nm
Cr 40nm	Ti 20nm
SiO_2 20nm	regrown n-InGaAs
InP 5nm	
InGaAs 12nm	
i-InAlAs 100nm	
i-InP 100nm	
i-InAlAs 100nm	
SI-InP substrate	

(b) layer profile of device structure

Fig. 1 Schematic image of fabricated device

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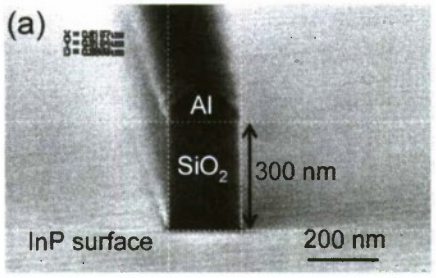
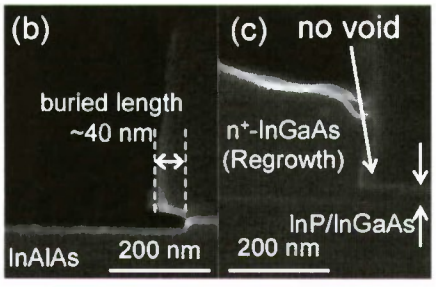
Fabrication process of regrown S/D MOSFET is as follows. First, an 300-nm-thick SiO_2 dummy gate for selective regrowth was formed on InP/InGaAs channel by plasma enhanced (PE) CVD and CF_4 dry etching using an Al mask which has width of 320 nm. While the dry etching, 60 nm lateral etching was occurred at both side of dummy gate. After an Al mask removal using H_3PO_4 etching for 10 min, the length along the channel and height of the dummy gate was around 200 nm and 300 nm, respectively, and its edge seems to be almost vertical as shown in Fig. 2 (a). Second, the undercut into the InGaAs channel was formed using $HCl:H_2O$ = 3:1 and citric acid:H_2O_2 = 1:1 solution. The lateral undercut length required to form a slight gate overlap was around 25 nm. After the cleaning of the InAlAs surface by $HCl:H_2O$ = 1:5, samples were immediately loaded into MOVPE chamber. The temperature was increased to 585°C in AsH_3 atmosphere (to prevent As from escaping InAlAs and InGaAs) and MOVPE selective regrowth was carried out.



(a) dummy gate structure (L_g = 200 nm)

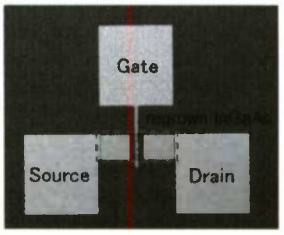


(b) before and (c) after regrowth (L_g = 2 μm)

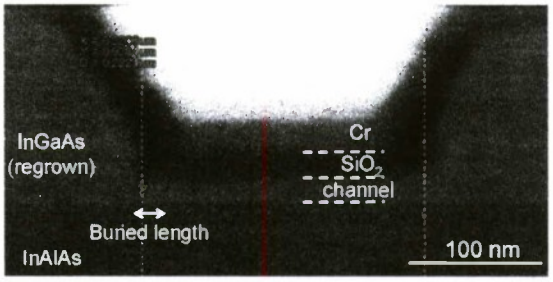
Fig. 2 SEM images of dummy gate

In this regrowth condition, the laterally buried length was estimated to be over 40 nm from SEM observation of a longer undercut structure with L_g = 2 μm, as shown in Figs. 2 (b) and (c). Therefore, it was expected that the 25-nm undercut was completely filled by regrown InGaAs. A thickness of regrown InGaAs was over 200 nm. The Hall measurement of regrown InGaAs which was grown on InAlAs/InP square substrate was carried out to evaluate the carrier profile. The carrier density was over 4×10^{19} cm^{-3}, electron mobility was 960 cm^2/Vs and sheet resistance was 13 Ω/square. That carrier density was comparable to required value and it indicated low series resistance and high injection ability.

After the regrowth, device isolation was carried out using a citric acid solution. Next, the dummy gate was removed by BHF and replaced with a 20-nm-thick SiO_2 gate insulator that was deposited using PECVD after channel surface passivation by $(NH_4)_2S$. Then, a Cr/Au gate electrode was formed by EB deposition. The gate stack was formed using Cr 40 nm/SiO_2 20 nm/InP 5 nm/InGaAs 12 nm. Finally, S/D contact holes were etched by BHF and Ti/Pd/Au S/D electrodes were also deposited. The (a) optical microscope image of fabricated device and (b) cross sectional SEM image of gate stack and regrown source/drain region was shown in Fig. 3.



(a) optical microscope image



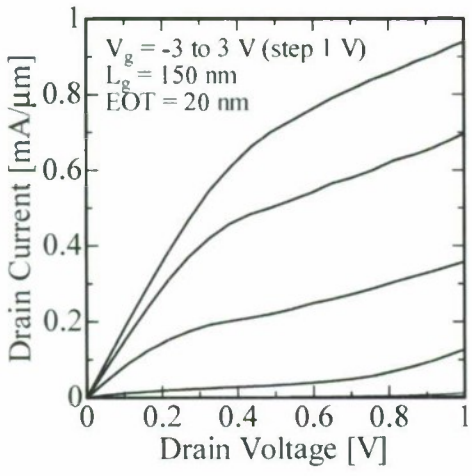
(b) cross sectional SEM image of MOSFET

Fig. 3 Device images of fabricated regrown MOSFET

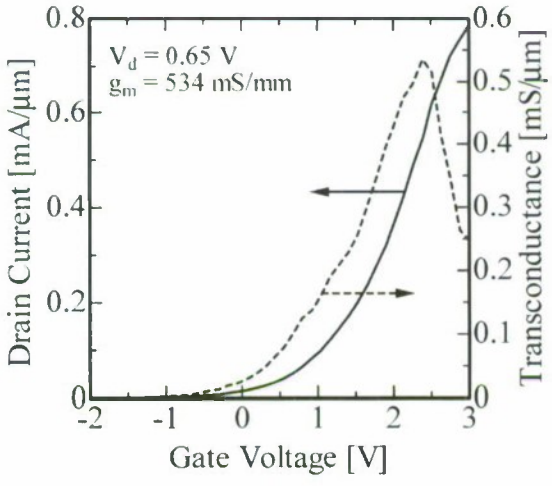
All devices in this report have the channel width of 20 μm. A cross sectional SEM image shows source to channel contact without void, gate stack structure with targeted thickness, intrinsic gate length of around 150 nm and good flatness of channel and insulator layer.

III. I–V characteristics of MOSFET

The (a) I_d–V_d and (b) I_d–V_g characteristics of the fabricated MOSFET with an intrinsic gate length (L_g) of 150 nm are shown in Fig. 4. Drain current modulation and MOSFET operation was clearly observed. I_d was 0.93 mA/μm at V_d = 1 V, V_g = 3 V and the maximum g_m was 0.53 mS/μm at V_d = 0.65 V. The gate leakage current was less than the measurement limit. I_d and g_m were larger than those in the previous regrown MOSFET with L_g = 2 μm (I_d = 0.42 mA/μm at V_g = 3 V, V_d = 1 V and g_m = 0.15 mS/μm at V_d = 0.65 V). Although the gate voltage was large due to the large effective oxide thickness (EOT) (≈ 20 nm), their values indicated that this device structure and MOVPE regrown S/D had good capabilities. These current improvements were caused by channel scaling and a three times higher S/D doping concentration compared with previous devices.



(a) I_d–V_d



(b) I_d–V_g

Fig. 4 I-V characteristics of regrown S/D MOSFET

The electron mobility was calculated to be around 3,000 cm^2/Vs from gate capacitance and g_m at V_d = 10 mV in L_g = 6 μm devices. Series resistance of regrown S/D MOSFET was around 0.5 Ω·mm. It was 3 times smaller than the series resistance of non-regrown S/D MOSFET.

Currently, subthreshold swing is around 1 V/dec and g_m is limited by the large EOT. These are caused by SiO_2/semiconductor characteristics such as large interface state density and low permittivity.

In the future, we intend to improve the gate dielectric characteristics by introducing high-k insulator having an EOT of several nanometers and optimizing surface passivation and post deposition/metallization annealing condition.

Figure 5 shows plots of estimated channel length versus transconductance at V_d = 0.65 V.

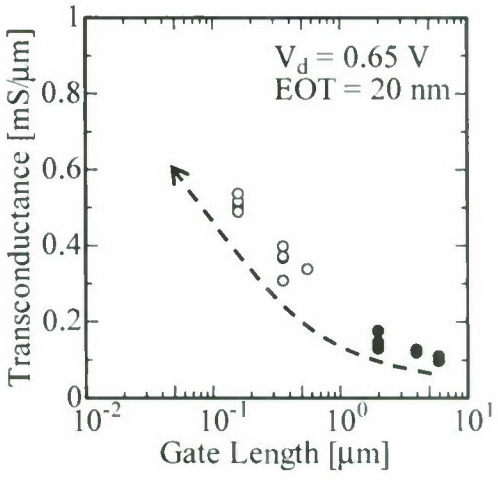


Fig. 5 g_m–L_g characteristics

The clear enhancement due to L_g scaling was observed in both of submicron and micrometer region. It indicates that I_d and g_m will be more enhanced by gate length scaling to less than 100 nm.

IV. Conclusion

We have reported the I–V characteristics of a submicron InP/InGaAs composite channel MOSFET. A heavily doped source/drain was formed by laterally buried regrowth using MOVPE. In the I–V measurement of MOSFETs with submicron gate lengths (= 150 nm), I_d was 0.93 mA/μm at V_g = 3 V, V_d = 1 V and the maximum g_m was 0.54 mS/μm at V_d = 0.65 V. This indicates that a channel scaling led to an increase in the current and the MOVPE regrown process had superior capabilities for high current operation.

Acknowledgement

The authors would like to thank Professors S. Arai and M. Asada and Associate Professors M. Watanabe and N. Nishiyama for their helpful discussions and S. Tamura for the technical assistance. This work was supported by the Ministry of Education, Culture, Sports, Science and Technology through a Grant-in-Aid for Specially Promoted Research, Scientific Research (A) and Young Scientist Research (B).

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FABRICATION AND CHARACTERIZATION OF 200-NM SELF-ALIGNED $In_{0.53}Ga_{0.47}As$ MOSFET

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***Abstract*—In this paper, a 200 nm n-channel inversion-type self-aligned $In_{0.53}Ga_{0.47}As$ MOSFET with a Al_2O_3 gate oxide deposited by Atomic Layer Deposition (ALD) is demonstrated. Two ion implantation processes using silicon nitride side-wall are performed for the fabrication of the n-type source and drain regions. The 200 nm gate-length MOSFET with a gate oxide thickness of 8 nm features the transconductance of 70 mS/mm and the maximum drain current of 200 mA/mm.**

Keywords-III-V MOSFET; $In_{0.53}Ga_{0.47}As$; inversion; self-aligned; ALD; Al_2O_3

I. INTRODUCTION

Fabrication of metal-oxide-semiconductor field-effect transistors (MOSFETs) using III-V based compounds, in particular the In-rich InGaAs, has recently gained considerable attention for high-performance application, since InGaAs can provide a high mobility to overcome the major roadblocks that Si technology is facing for advanced CMOS devices. Thanks to ALD [1-3,5-8] and in-situ UHV deposition [4], good insulators have been obtained for III–V MOSFETs. The first double ion implantation $In_{0.53}Ga_{0.47}As$ MOSFET using sidewalls process is demonstrated.

II. EXPERIMENT

A. *Epitaxy growth and oxide deposition*

Lattice matched $In_{0.53}Ga_{0.47}As$ epitaxial layers were grown using solid source molecular beam epitaxy (RIBER 32P) on semi-insulating InP substrate. The layers, from bottom to top, consisted of 500-nm-thick carbon-doped ($N_a = 1\times10^{19}$ /cm^3) $In_{0.53}Ga_{0.47}As$ and 300-nm-thick carbon-doped ($N_a = 1\times10^{17}$ /cm^3) $In_{0.53}Ga_{0.47}As$. After surface cleaning and pretreatement, an 8-nm-thick Al_2O_3 is grown by Atomic Layer Deposition (ALD) at 300°C using H_2O and $Al(CH_3)_3$ like precursors and annealed at 600°C during 1 min.

B. *Fabrication of 200 nm gate length self aligned InGaAs MOSFET*

The fabrication of the n-channel inversion mode $In_{0.53}Ga_{0.47}As$ MOSFET starts with a deposition, using sputtering technique, of a 300-nm-thick of Tantalum on the entire wafer. To define the self-aligned gates, an e-beam lithography using Hydrogen SilsesQuioxane (HSQ) resist is performed. After removing the uninsulated HSQ in TMAH solution, uncovered Ta layer is etched by Reactive Ion Etching (RIE) process using chlorine based gazes with Ar. A first ion implantation of Si is realized at 15 keV (5×10^{13} /cm^2) to form the light doping area. Before the second ion implantation, silicon nitride sidewalls are realized by depositing 20 nm-thick Si_3N_4 by PECVD and by anisotropic RIE etching, then fabricated by e-beam lithography and evaporation.

- Ammonia surface treatment
- 8nm alumina deposited by ALD, annealed at 600°C, 1min
- Ta sputtering 200nm
- HSQ lithography
- Ta RIE etching
- 1st implantation Si (15 keV)
- Si_3N_4 by PECVD 20nm
- Sidewall, RIE etching
- 2nd implantation, Si (35keV)
- Activation annealing 750°C 10s
- Ti/Pt/Au ohmic contacts
- Mesa wet etching
- Ti/Pt/Au body contact, annealing and Ti/Au pads

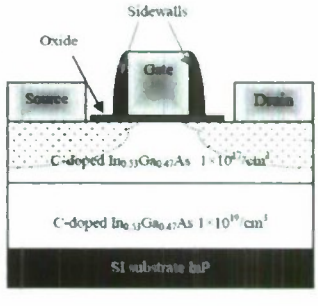

Figure 1. InGaAs MOSFET scheme (right) with fabrication process (left).

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After the second ion implantation at 35 keV (8.5×10^{13} /cm²), the wafer is annealed at 750°C during 10 s. Ti/Pt/Au ohmic contacts are Mesa isolation is realized by wet etching (H_3PO_4:H_2O_2:H_2O) through an optical lithography and air-bridge gates are created during this etching. Finally, Ti/Pt/Au back-gate contacts are realized by optic lithography, wet etching until p+-InGaAs layer and e-beam evaporation. Fig. 2 shows a TEM image of 200 nm gate length Ta/Al_2O_3/$In_{0.53}Ga_{0.47}As$ MOSFET.

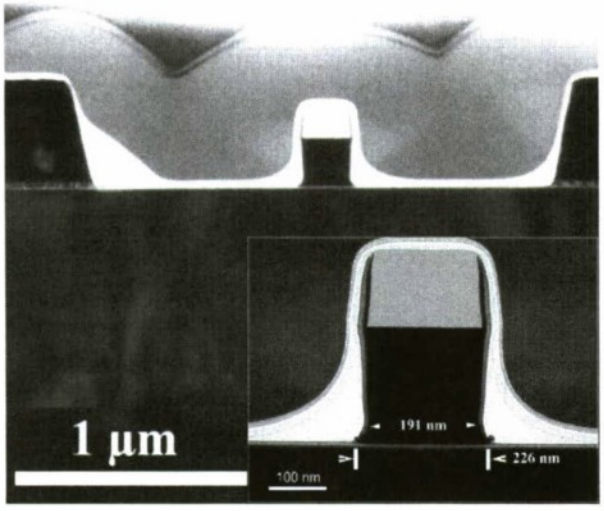

Figure 2. TEM image of 200 nm gate length $In_{0.53}Ga_{0.47}As$ MOSFET (zoom in inset).

III. RESULTS

A. DC measurements of 200 nm self aligned InGaAs MOSFET

On-wafer DC measurements are carried out at room temperature. Through TLM measurements implanted regions exhibit contact resistance of 0.4 Ω.mm and sheet resistance of 62 Ω/□. Fig. 3 shows typical drain current (I_d) characteristics versus source-drain voltage (V_{ds}) with a gate voltage (V_g) varying from 0 to 3V with a step of + 0.5V. The maximum drain current of 200 mA/mm is achieved at a gate bias of 3 V and a drain bias of 1 V (Fig. 4) and a maximum extrinsic transconductance g_m of about 70 mS/mm is obtained. Gate current as function of gate voltage is shown in Fig. 5. Using C-V measurements with HF-LF method (Fig. 6) and the equation (1), an interface trap density (D_{it}) of 2.8×10^{12} $eV^{-1}cm^{-2}$ has been evaluated on MOS capacitor.

$$D_{it} = \frac{C_{ox}}{q}\left(\frac{C_{BF}/C_{ox}}{1-C_{BF}/C_{ox}} - \frac{C_{HF}/C_{ox}}{1-C_{HF}/C_{ox}}\right) \quad (1)$$

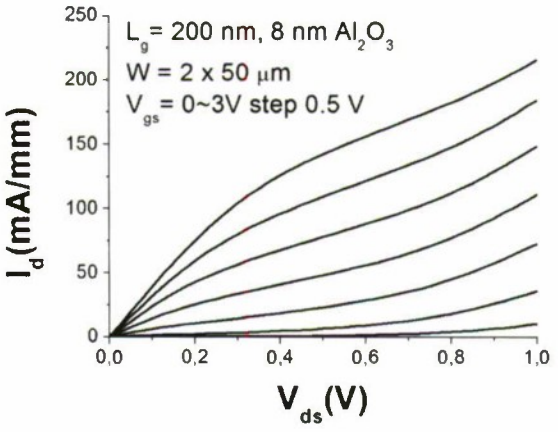

Figure 3. Drain current versus source-drain voltage for a 200 nm gate length Ta/Al_2O_3/$In_{0.53}Ga_{0.47}As$ MOSFET for different gate voltage varying from 0 V to 3 V with a step of 0.5V.

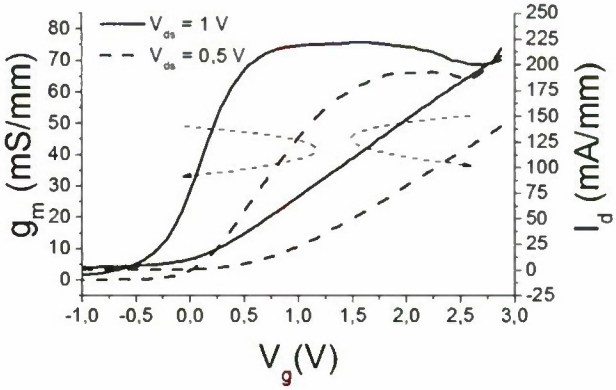

Figure 4. Transconductance versus gate voltage for a 200 nm gate length Ta/Al_2O_3/In0.53$Ga_{0.47}As$ MOSFET and his associated drain current for V_{ds} = 0.5 V and V_{ds} = 1 V.

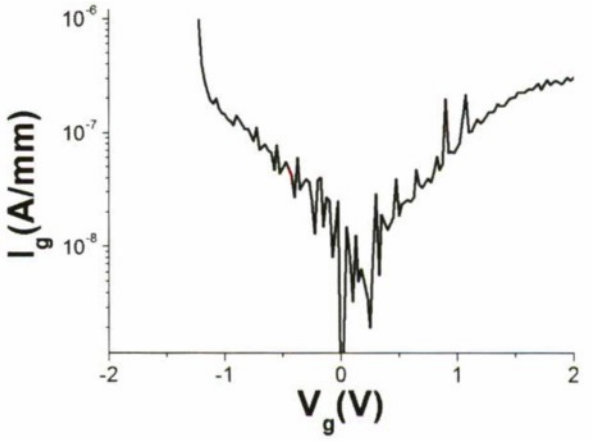

Figure 5. Gate current versus gate voltage for a Ta/8nm-Al_2O_3/$In_{0.53}Ga_{0.47}As$ MOSFET

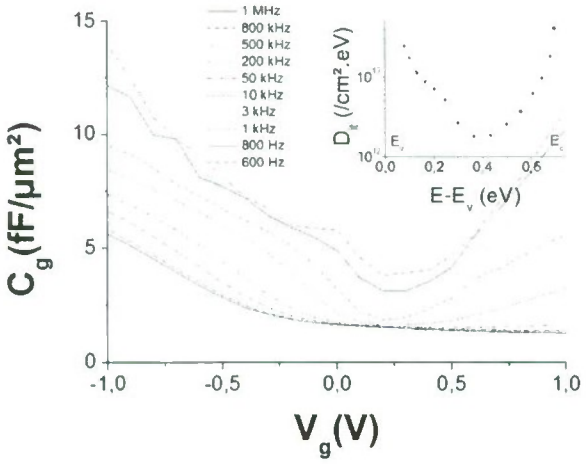

Figure 6. Capacitance versus voltage for Ti/8nm-Al_2O_3/$In_{0.53}Ga_{0.47}As$ MOSCAP at different frequencies. D_{it} versus E-E_v measured by HF-LF method in inset.

B. Discussion about D_{it} contribution to DC performances of 200 nm self-aligned InGaAs MOSFET

The results are not measured up compare to those of the literature but this transistor has potentialities. We suspect the presence of high interface trap density between alumina and InGaAs, higher than D_{it} measured with the MOSCAP by HF-LF method because of the different thermal budget. It is known that gate first process increases the native oxides content at the oxide/semiconductor interface without specific passivation compare to gate last process [9] and thus, D_{it} increases and reduces DC characteristics. But it also known that this specific passivation for gate first process exists reducing interface trap density [5]. So, higher drain current, transconductance could be expected for our device.

IV. Conclusion

A 200 nm gate length self-aligned $In_{0.53}Ga_{0.47}As$ MOSFET fabricated using side-walls process has been presented. This non optimized transistor exhibits good DC performances. Compare to the literature, these results are not the best because of high D_{it} due to gate first process and no specific passivation. But we expect better DC performance by removing D_{it} contribution.

Acknowledgment

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VERY-HIGH-BIT-RATE INTEGRATED PHOTONIC DEVICES FOR NEXT-GENERATION ETHERNET

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Abstract

Recent advances in integrated photonic devices for next-generation Ethernet are described. In particular, 1.3-μm-range uncooled photonic devices (namely, electroabsorption modulator integrated lasers, directly modulated lasers, and lens integrated devices) are focused on. A key technology for uncooled operation is an InGaAlAs multiple quantum well (MQW), which produces a strong electron confinement. The electroabsorption modulator integrated lasers, which incorporated an InGaAlAs-MQW absorption layer, exhibit uncooled 25.8-Gbit/s and 43-Gbit/s single-mode fiber 10-km transmissions. The 1.3-μm directly modulated laser, which consists of an InGaAlAs MQW distributed feedback (DFB) active stripe, exhibits uncooled direct modulation at 25 Gbit/s. To improve the optical coupling of the directly modulated laser, we developed a lens-integrated surface-emitting laser, which incorporates an InGaAlAs DFB active stripe. This lens-integrated laser exhibits 25-Gbit/s direct modulation up to 100°C. Furthermore, the lens-integrated photodiode exhibited high speed (35 GHz), high responsivity (0.8 A/W), and large alignment tolerance (26 μm) for direct coupling to a single-mode fiber. These photonic devices have demonstrated their potential for implementation in cost-effective 100-Gbit/s and 40-Gbit/s Ethernet.

I. Introduction

Recent growth in Internet traffic is increasing demand for more bandwidth in networks. To meet this demand, the IEEE P802.3ba Task Force has been working on the standardization of the next-generation high-speed Ethernet, namely, 100-Gb Ethernet and 40-Gb Ethernet. In the near future, standards for 100-Gb Ethernet and 40-Gb Ethernet are going to be released. A unique aspect of the 100/40-Gb Ethernet standards is the adoption of multi-channel transmission to achieve high data rate. In this way, the signal rate needed for each channel can be slower than the total data rate of 100 Gbit/s, which is still a challenge for a laser device to achieve.

In the 100-Gb-Ethernet standards, long-reach specifications (100GBASE-LR4 (10 km) and 100GBASE-ER4 (40 km)) are based on a wavelength division multiplexing (WDM) of four-channel, 25-Gbit/s signals with frequency interval of 800 GHz in the 1.3-μm wavelength range. For 40-Gb Ethernet, although a 10-km-transmission specification (40GBASE-LR4) is based on a 10-Gbit/s four-channel WDM in 1.3-μm range, a single-channel scheme using a 40-Gbit/s laser device is expected to be an effective way to reduce the cost and power consumption of 40-Gb Ethernet transceivers in the near future. A major technological challenge is therefore to build 1.3-μm photonic devices operating at 25/40 Gbit/s. In addition, if uncooled operation of the 25/40-Gbit/s devices were possible, further reduction in the power consumption of the transceivers would be possible. According to the currently discussed standards for 100/40-Gb

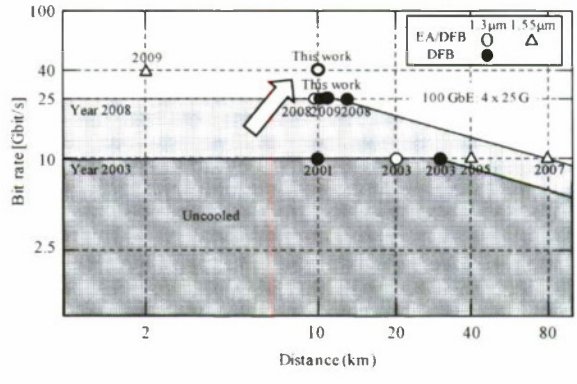

Fig. 1. Technology trend concerning uncooled lasers

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Ethernet, lasers should be cooled to stabilize the signal wavelengths on the narrowly spaced WDM grid. Such cooling, however, increases the power consumption of thermo-electric coolers. Uncooled operation of a laser is therefore a key to achieve compact, cost-effective, and low-power-consumption next-generation 100/40-Gb Ethernet transceivers.

There are two potential candidates for such very-high-hit-rate uncooled light sources: an electroahsorption modulator integrated distrihuted feedback (EA/DFB) laser and a directly modulated DFB laser. The advantages of an EA/DFB laser are high speed and low-chirp characteristics. Accordingly, very-high-hit-rate operation (25 to 100 Gbit/s) of EA/DFB lasers has been reported (1-5). On the other hand, the advantage of a directly modulated laser is its lower power consumption and cost effectiveness. Very-high-hit-rate uncooled operation of directly modulated DFB lasers has also heen reported (6-9). Figure 1 shows the technology trends in uncooled lasers over the last ten years or so. As for uncooled lasers, there is a trade-off between bit rate and link distance. Accordingly, our challenge has been to develop 25/40-Gbit/s uncooled lasers for 10-km transmission.

In the development of very-high-bit-rate devices for next-generation Ethernet, one of the key technologies is photonic integration of functional elements. Photonic integration not only reduces the size and cost of transceivers but also improves device performance. For example, the light output power of an EA/DFB laser is substantially higher than that of a discrete modulator owing to its lower insertion loss. Moreover, an integrated lens is very effective in developing a high-speed and high-efficiency photodiode because high-speed photodiodes have a very small junction aperture.

Focusing on uncooled lasers and lens-integrated devices, the following sections present recent advances in integrated photonic devices for next-generation Ethernet.

II. Electroabsorption modulator integrated DFB laser

An electroabsorption modulator integrated distrihuted feedhack (EA/DFB) laser is a promising light source for next-generation high-speed Ethernet. Because of its key features, namely, high speed, low chirp, and compactness, it is expected to provide transceivers with low power consumption and small foot print. To realize a high-speed, low-power-consumption EA/DFB laser, it is essential not only to optimize the design of a multiple quantum well (MQW) but also to incorporate the proper material for each functional element in the modulator and laser.

Butt-joint integration is a key technique for achieving independently optimizing the design of each functional element. By using this technique, it is possible to independently control the design parameters of each functional element, such as material composition, well number, well width, and band discontinuity. Accordingly, to achieve sufficient extinction ratio, output-power handling capability,

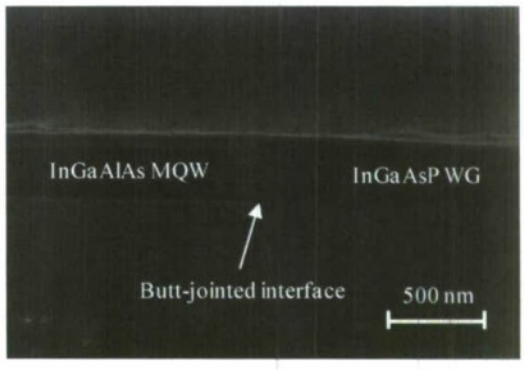


Fig. 2. Scanning-electron-microscope image of hutt-jointed InGaAlAs-InGaAsP interface

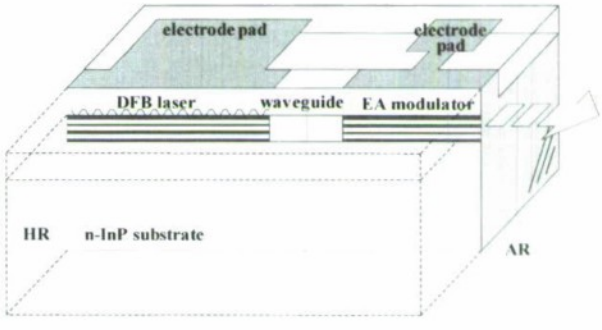


Fig. 3. Schematic structure of EA modulator integrated DFB laser

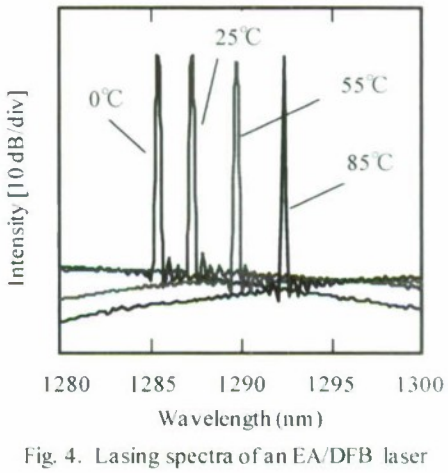


Fig. 4. Lasing spectra of an EA/DFB laser

and wide-temperature-range operation, an InGaAlAs MQW was incorporated in the EA modulator.

One of the major difficulties in developing hutt-joint

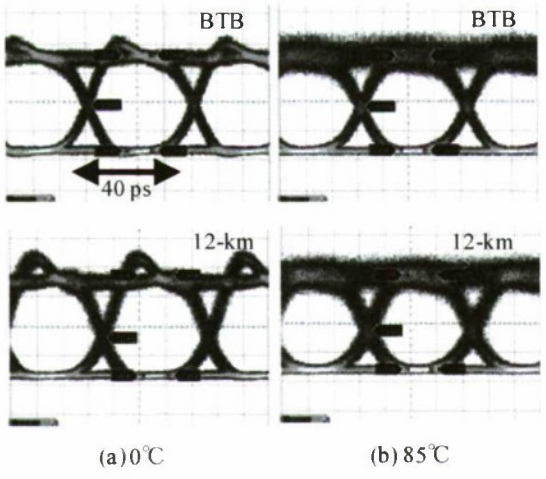


Fig. 5. 25.8-Gbps eye diagrams of EA/DFB laser before and after 12-km SMF transmission

integrated devices is to produce good optical coupling between the functional elements. We therefore previously developed a high-coupling-efficiency butt-jointing process with in situ cleaning (10). Figure 2 shows a scanning-electron-microscope image of the butt-jointed structure composed of a 1.3-μm-range InGaAlAs MQW layer and an InGaAsP waveguide (WG) layer. The InGaAsP layer was seamlessly connected to the InGaAlAs layer with the same thickness. Optical-coupling efficiency at the InGaAlAs-InGaAsP butt-jointed interface of a multiple butt-jointed laser was quantitatively estimated to be more than 97%. By using the butt-jointing process, we have developed high-speed EA/DFB lasers for next-generation Ethernet (1, 2).

Figure 3 shows the schematic structure of the fabricated EA/DFB laser—which consists of an InGaAlAs EA modulator (100 μm in length), a passive waveguide (60 μm in length), and a DFB laser (400 μm in length). The passive waveguide is incorporated to reduce the optical absorption at the jointed interface. All components are monolithically integrated on an n-InP substrate.

The fabrication process for the EA/DFB laser is explained as follows. First, the integrated structure was formed by multi-step butt jointing. A corrugation grating was then formed on the structure. After that, an InP cladding laser was grown on the structure. The wafer was then processed into a low-parasitic-capacitance structure with a small-area bonding pad of the EA modulator for high-speed modulation. The total capacitance of the EA modulator was designed to be lower than 0.2 pF. A highly reflective coating film and an anti-reflective coating film were then deposited on the facet at the end of the DFB laser and on the front of the EA modulator, respectively. The chip was die-bonded on a chip carrier with a 50-Ω terminal resistor.

Figure 4 shows the lasing spectra of an EA/DFB laser at 0°C, 25°C, 55°C, and 85°C. Stable single-mode operations

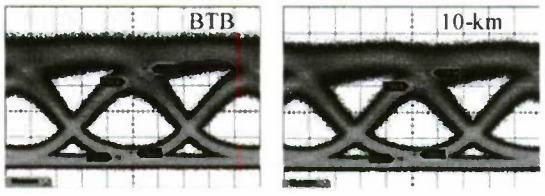


Fig. 6. 43-Gbps eye diagrams of EA/DFB laser before and after 10-km SMF transmission at 85℃

with a side-mode suppression ratio of over 40 dB were confirmed at all operating temperatures.

Figure 5 shows non-filtered eye diagrams obtained under 25.8-Gbit/s modulation at 0°C and 85°C. Clear eye openings were obtained even after 12-km transmission at both temperatures. The measured dynamic extinction ratios were 9.9 dB and 9.6 dB at 0°C and 85°C, respectively. As shown in Fig. 6, uncooled 43-Gbit/s 10-km transmission of an EA/DFB laser was also confirmed (2).

III. Directly modulated DFB laser

Uncooled operation of lasers is critical for developing compact and low-power-consumption transceivers. Uncooled 25-Gbit/s direct modulation of 1.3-μm DFB lasers has been demonstrated and shows their potential for implementation in next-generation 100-Gb Ethernet (6-8). A key technology in achieving such uncooled operation is the InGaAlAs MQW, which produces a strong electron confinement. We have previously demonstrated uncooled 25-Gbit/s direct modulation of an InGaAlAs-MQW laser up to 95°C (8).

To improve the drive-current dependence of the relaxation oscillation frequency (f_r) of the laser, a short cavity structure was incorporated in the laser. Figure 7 shows the cavity-length (L_c) dependence of the lasing characteristics of a Fabry-Perot laser at 85°C. The slope of f_r increases monotonically by shortening L_c. Shortening of L_c is also effective for lowering threshold current and slope efficiency. Given this result, we fabricated a laser with a 160-μm-long cavity because the increase of the slope of f_r deviates from the proportional relation at L_c below 200 μm.

The fabricated laser consists of a DFB laser stripe with a ridge-waveguide structure. Figure 8 shows the temperature dependence of the light-current characteristics of the fabricated DFB laser. The threshold currents were 13.1 mA and 14.9 mA at 85°C and 95° C, respectively. The slope efficiencies were 0.36 W/A and 0.34 W/A at 85°C and 95°C, respectively. To evaluate the high-bit-rate performance, a digital modulation test was carried out at 25 Gbit/s. Thanks to the high-gain InGaAlAs MQW and the short-cavity structure, clear eye openings were obtained from 25°C to 95°C (8).

Although the DFB laser exhibits superior performance, it is not completely satisfactory because it has a 30°-wide, edge-emitting output beam, which prevents the use of simple

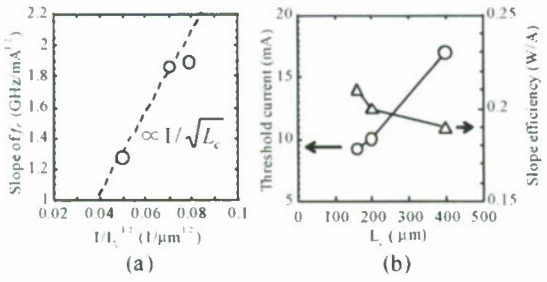


Fig. 7. Dependence of f_r slope, threshold current, and slope efficiency on cavity length L_c at 85°C

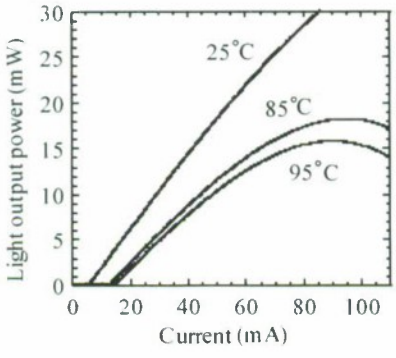


Fig. 8. Light-current characteristics of a directly modulated DFB laser

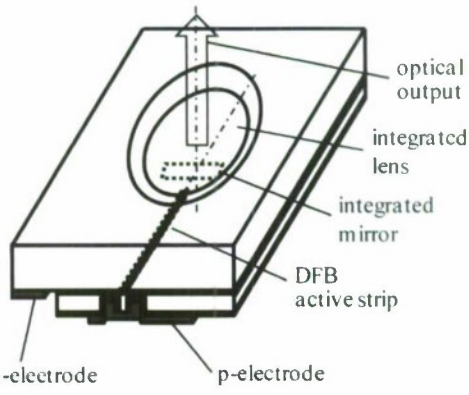
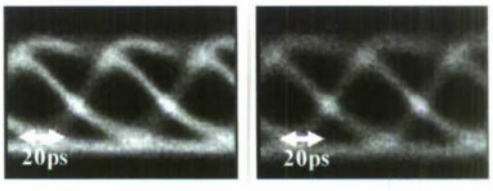


Fig. 9. Schematic structure of lens-integrated surface-emitting laser



(a) 25°C (b) 100°C

Fig. 10. 25-Gbps eye diagrams of lens-integrated surface-emitting laser

surface-mounting technology. A standard approach for surface mounting is to use 1.3-μm vertical-cavity surface-emitting lasers (VCSELs) (11). However, it is still a challenge for a 1.3-μm VCSEL to operate at the ultra-high speed at elevated temperature because of saturation of laser-chip output power due to its small active volume. We have thus integrated a 45° total-reflection mirror and an aspheric lens into a DFB laser, namely, a lens-integrated surface-emitting laser (LISEL), and demonstrated 1.3-μm surface emission of a very narrow beam (2°) (12). Furthermore, we have recently demonstrated the 100°C, 25-Gbit/s operation of a novel LISEL, which is directly mountable on a high-frequency coplanar line (9).

Figure 9 illustrates the schematic structure of our novel LISEL. It consists of a short InGaAlAs-MQW DFB active stripe with length of 150 μm, a 45° total-reflection mirror, a monolithic aspheric lens, and flip-chip bondable electrodes. The laser beam produced in the DFB active stripe is internally reflected at the 45° mirror and emitted from the bottom surface of the InP substrate through the monolithic lens for output collimation. We expect that using flip-chip bonding will result in superior high-speed characteristics because the parasitic inductance produced by wire bonding is eliminated.

The fabrication process for the LISEL is as follows. An InGaAlAs-MQW active layer was first grown on an InP substrate by metal-organic vapor-phase epitaxy (MOVPE). After a corrugation grating was formed, an InP cladding layer was grown on the structure. The wafer was then processed into a standard ridge-waveguide structure. After that, a 45° mirror was fabricated by etching. After the wafer was thinned, an aspheric lens was fabricated on the bottom side of the InP substrate by etching. The profile of the etched InP lens was estimated to be a highly symmetrical parabolic shape, which is ideal for collimation of a Gaussian beam (13). An anti-reflective coating film was formed on the surface of the monolithic lens. The device was mounted on an AlN heat sink with a high-frequency coplanar line in a junction-down configuration.

Threshold currents of fabricated LISELs are 6.4 mA at 25°C and 13.8 mA at 85°C. Single longitudinal mode operation with side-mode suppression ratio of more than 40 dB was obtained at both temperatures. The slope of f_r was estimated to be 3.6 GHz/mA$^{1/2}$ at 25°C and 3.2 GHz/mA$^{1/2}$ at 85°C. These high values are due to the high gain of the InGaAlAs MQW.

Eye diagrams obtained under 25-Gbit/s direct modulation at 25°C and 100°C are shown in Fig. 10. The center bias current and the peak-to-peak modulation current are, respectively, 25 and 37 mA at 25°C and 40 and 41 mA at 100°C. 25-Gbit/s eye opening are obtained even at 100°C owing to the steeper slope of f_r at high temperature. To the

best of our knowledge, this is the first time 1.3-μm surface-emitting lasers have produced a 25-Gbit/s eye opening at 100°C.

IV. Lens-integrated photodiode

In multi-channel high-speed systems, high-speed and high-efficiency photodiodes with large alignment tolerance will be a key component in improving overall system performance. However, achieving large alignment tolerance of high-speed photodiodes is difficult because these photodiodes need a small aperture. Monolithic integration of a lens is a key technology for achieving such large alignment tolerance, although more processing steps are required. Accordingly, we have developed an aspheric-lens-integrated photodiode (14).

The schematic structure of the fabricated lens-integrated photodiode is illustrated in Fig. 11. This photodiode is a mesa-type back-illuminated PIN photodiode, which has a small circular junction area (10 μm in diameter) and a backside-etched lens. The surface of the lens is coated with an anti-reflection film. Furthermore, the photodiode has a highly reflective mirror on the top of the photosensitive region to cope with the bandwidth-efficiency trade-off that occurs with conventional vertically illuminated photodiodes.

The bandwidth of the fabricated photodiodes at a reverse bias voltage of 3 V was estimated to be 35 GHz. This large bandwidth is due to the small junction area. Figure 12 shows the measured responsivity curves as a function of transverse distance from the optical axis for a lens-integrated photodiode and a photodiode without a lens. A flat-ended single-mode fiber was used for the measurement. The maximum responsivity is larger in the case of the lens-integrated photodiode. This responsivity improvement is due to the shrinking of the beam spot size on the focal plane. Moreover, the misalignment tolerance of the lens-integrated photodiode (26 μm) is more than four times larger than that for the photodiode without a lens (6 μm). This enlargement is due to two lens effects: compensation of incident-light-position deviation and shrinking of the spot size on the focal plane.

By using such lens-integrated photodiodes, we have developed a compact quadplex receiver for 100-Gb Ethernet (15). This receiver consists of an optical Demux module and four 25-Gbit/s receiver optical sub-assemblies (ROSAs). Using the lens-integrated photodiodes resulted in uniform and highly efficient optical coupling for each wavelength. The quadplexer receiver achieved error-free 10-km single-mode fiber transmission.

V. Summary

Four kinds of 1.3-μm-range, very-high-bit-rate uncooled devices, namely, 25/40-Gbit/s EA/DFB lasers, 25-Gbit/s directly modulated lasers, 25-Gbit/s surface-emitting lasers, and lens-integrated photodiodes, have been developed. These uncooled devices are expected to provide cost-effective

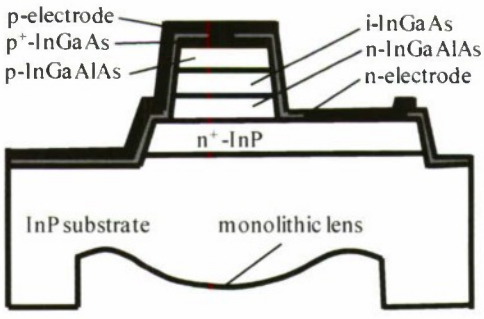


Fig. 11. Schematic view of lens-integrated photodiode

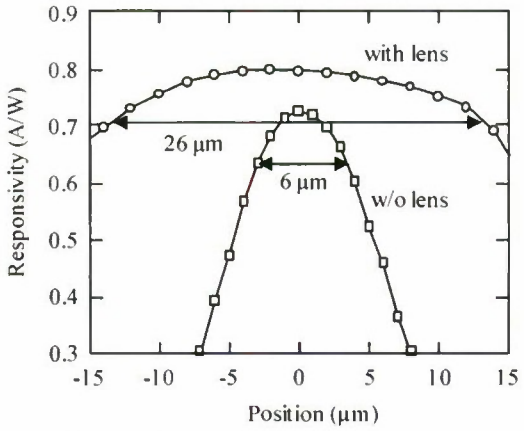


Fig. 12. Responsivity curves as a function of transverse distance from optical axis

transceivers for high-speed data links, especially for next-generation Ethernet.

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40Gb/s SOA-integrated EAM using cascaded structure

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Abstract: A 40Gb/s data transmission is demonstrated through a new approach, the cascaded integration of EAM and SOA. Low driving power 1Vpp with -3dB bandwidth 47GHz, extinction ratio 20dB, and optical gain of 11.8dB are attained.

Introduction

40Gb/s data transmission based on electroabsorption modulators (EAM) has been widely used in high-speed optical telecommunication due to their high extinction ratio, low driving power and the capability of integrating with other semiconductor devices [1]. However, in a single EAM waveguide made by p-i-n material, the highly loaded capacitance and also the intrinsic optical absorption in i-layer will lead to low electrical- and optical- transmission. Monolithic integration of laser, electroabsorption modulator (EAM), and semiconductor optical amplification (SOA) is a promising solution due to the performance, such as compactness, multi-functions, optical gain. Using cascaded EAMs integrated high impedance transmission lines (HITL), several advantages have been found, for example, high modulation efficient, and lower impedance mismatch into 50-ohm instrument in comparison with single EAM waveguide [2-5]. In this work, a cascaded EAMs monolithically integrated with SOAs in a long waveguide is used for 40Gb/s data transmission. Also, in the same chip, it allows the cascaded EAMs to interconnect the cascaded HITLs, leading to successful 40Gb/s data transmission with low driving power, high A.C. modulation efficient, and the optical gain.

Experiment and Results

The schematic plot of the integrated SOAs-EAMs is shown in figure 1. Both EAMs and SOAs are serially and periodically connected in a optical waveguide, performing the distributed modulation and amplification processing. HITLs [4] are utilized for by-passing SOA and high-speed interconnecting line. The same active region used in EAMs and SOAs is MOCVD-grown InGaAsP M.Q.W.s (6 wells) sandwiched by p- and n- InP layers. The width of optical waveguide is 3μm. The lengths of three EAMs and two SOAs are 300μm and 600μm respectively. The isolation regions between EAMs and SOAs are formed by H-ion implantation. N- and p- contacts are made by evaporating Ni/AuGc/Au and Ti/Au metals. PMGI is used for planarization, HITL and final CPW line bridging.

Figure 2 shows the D.C. fiber-to-fiber optical transmission against with bias. The incident optical power of 0dBm centered at 1590nm is used to excite the device. As shown, the high modulation extinction ratio of 20dB in 2.5V is obtained. As it can be seen, the relations of transmission against voltage are similar as the pump current increases from zero to 70mA, implying that the operation of SOA doesn't degrade the extinction ratio in such cascaded structure. In high-speed characterization, a high-speed vector network analyzer incorporating with a high-speed photodetector is used for measuring the electrical-to-optical (EO) transmission. The output and input microwave feed lines are terminated by 50-ohm instrument. As shown in figure 3, the broadband EO response with as high as 47GHz of -3dB bandwidth is attained. As examining the overall device electrical response, the microwave reflection (S11) is below -10dB from D.C. to 35GHz, suggesting that employing the cascaded EAMs with HITLs can have benefit over the conventional single waveguide of EAM. A 40Gb/s data transmission test setup is used for characterizing the large signal response. Figure 4 shows the eye diagrams of the cascaded EAMs and SOAs. Due to the low microwave reflection, the high built-up microwave power inside the cascaded EAMs lead the device to perform under low driving electrical power. The driving electrical power is as low as 1v (V_{pp}), suggesting the high-extinction modulation along long waveguide can still be sustained at high-speed regime. A bit error rate test with pattern length of 2^{15}-1 is utilized to measure the data modulation quality. As shown in figure 4, an error-free performance is observed, implying that such cascaded scheme of integration can have high potential for >40Gb/s data modulation application.

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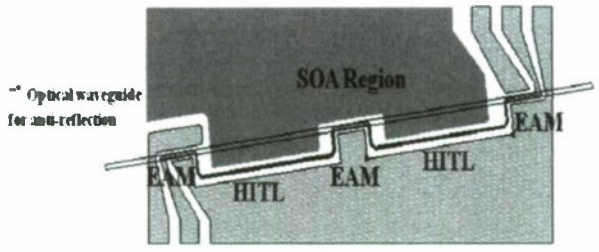

Fig1. The schematic plot of the integrated SOAs-EAMs.

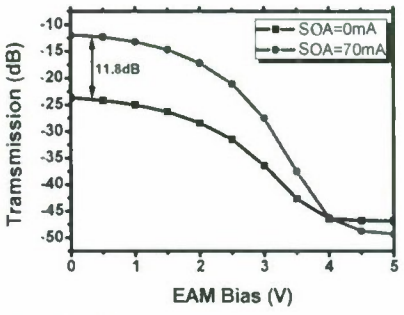

Fig. 2. Optical transmission with reverse bias for chain integrated EAMs and SOAs.

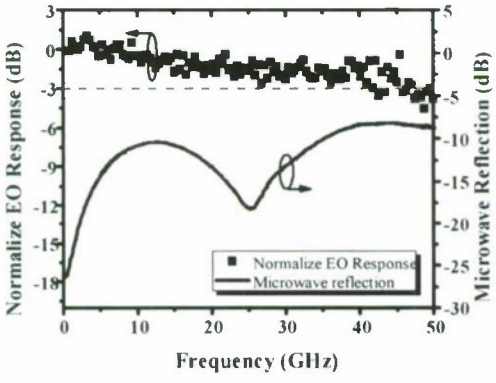

Fig. 3. The measured microwave reflection and electrical to-optical (EO) response of chain integrated EAMs and SOAs.

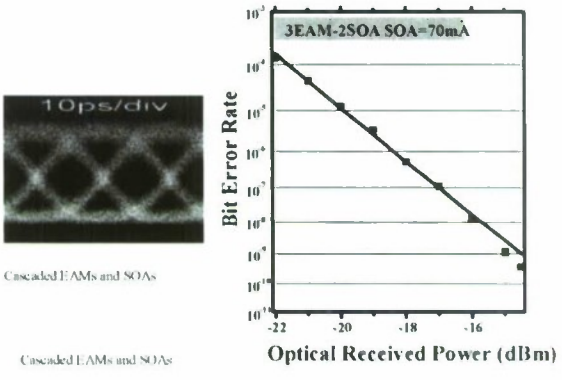

Fig. 4. The 40Gb/sec eye diagram and the BERT test result.

4. Conclusion

We proposed and demonstrated a 40Gb/s data transmission based on the cascaded integration of SOAs and EAMs. By cascaded connection between HITLs and EAMs, -3dB bandwidth of 47GHz with low microwave reflection of <10dB allow such device to operate at 40Gb/s data transmission at low driving voltage of 1V.

5. Acknowledgements

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CHIRP OPTIMIZATION OF 1550nm InAs/InP QUANTUM DASH BASED DIRECTLY MODULATED LASERS FOR 10Gb/s SMF TRANSMISSION UP TO 65Km

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***Abstract*—Static and dynamic properties of InP-basecl Quantum Dashes of 1.55µm directly modulated lasers are reported. Using growth and design optimization, wc demonstratc linewidth cnhancemcnt factor above thrcshold as low as 2 and decreasing with injected current. This unique chirp behavior leads to uncompensated and non-amplifiecl SMF 10Gb/s transmissions at a constant bias currcnt from back-to-back up to 65km. This rcsult opens the way to the fabrication of a low cost DML for acccss and metro applications.**

Keywords; Quantum dashes, gas source molecular beam epitaxy, opto electronic devices, InP-based directly modulated lasers

I. INTRODUCTION

Quantum Dots (QDots) and Quantum Dashes (QDashes) struetures emitting in the 1.55µm window are very promising for metropolitan and access networks requiring low-cost devices. In particular, the expeeted higher differential gain and lower chirp in low dimensional heterostructure [1] should lead to directly modulated lasers (DML) with high modulation bandwidth and should enable long distance transmission.

The standard transmission distanee without dispersion compensation obtained with 1.55µm direetly modulated multi-quantum-well (MQW) lasers is around 20 km. For longer distances, new limitations arise from linewidth enhancement factor -induced chirp. Long reach 10Gb/s transmission (typically 40 km and above) using DML has already been demonstrated by compensating the fiber dispersion to avoid the chirp induced signal degradation. It was achieved for instanee by using dispersion compensation fibre, specific filtering or electronic compensation. These solutions are in general not compatible with low cost and low power consumption applications. The devclopment of a low cost DML allowing to cover a large range of transmission distance (typically 10:60km) without using complex compensation requiring specific in-line adjustment or power consuming cards is therefore of paramount importance.

QDashes laser with modulation bandwidth in continuous wave (CW) mode operation up to 10GHz [2,3] and high temperature behavior for short distanee 10Gb/s transmission [4] have been demonstrated, opening thc way to a further optimization. In this paper, we demonstrate that the design optimization of QDashes devices leads to very low chirp distributed feedback (DFB) lascrs, evcn at high injected current. As a consequence, error-free uncompensated and non-amplified SMF 10Gb/s transmissions is demonstrated at a constant bias current from back-to-back up to 65km.

II. EXPERIMENTS

Thc dashes-in-a-well (DWELL) lascr structure was grown by gas source molecular beam epitaxy on a S-doped (001) InP substratc. It eomprises 6 laycrs of InAs QDs embedded within a 6nm-thick InGaAsP quantum well (λg=1.45µm) each, separated by 20nm-thick InGaAsP p-doped barriers (λg=1.17µm). The optical confinement is obtained by a separated confinement heterostrueture (SCH). The p-side and n-side SCH layers are respectively 20 nm and 70 nm thick in order to reduce the carrier transit timc and to limit the recovery of the optical modc and the absorbing p-doped layers. Optimized growth condition leads to the formation of high-density QDashes with significantly rcduced PL lincwidth (down to ~50meV) due to homogeneous dash size.

We studied 500µm- and 1mm-long DFB lasers. An anti rcflectivity (AR) coating has been depositcd on the front facet whereas the baek facet is as-eleaved. As shown in Fig.1, threshold current of 30mA and external efficicncy of 0.15W/A are observed for 500µm DFB buried lasers. As a result, output power up to 10mW is achieved at 100mA in CW opcration. DFB lasing emission is 1540nm as illustrated in Fig.2. The gain peak is in thc rangc of 1530:1560nm, depending on cavity length. For 1mm-long lasers, the DFB detuning is about -20nm, which is an optimum for the diffcrential gain. For 500µm-long lasers, the detuning is about +5nm, which appears

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as a good compromise between dynamic properties and temperature behavior allowing the investigation of 10Gb/s transmission both at room temperature and in semi-cooled operation.

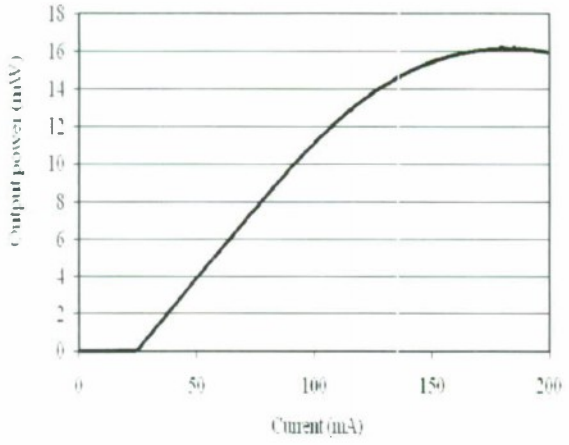

Fig.1: Output power versus injection current of the 500µm-long BRS DFB laser measured under CW operation at 25°C.

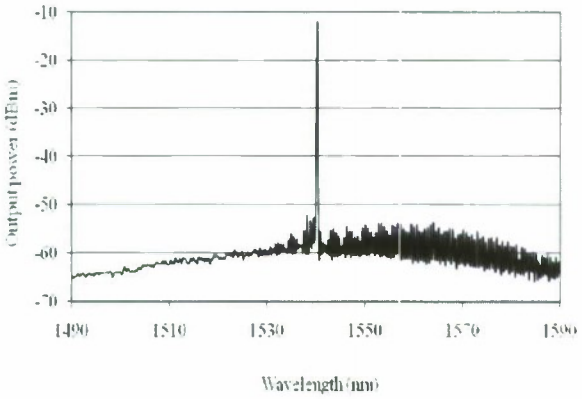

Fig.2: Lasing spectra of a 1mm-long DFB buried laser.

III. DYNAMIC PROPERTIES

As shown in Fig.3, the small signal -3dB modulation bandwidth of the 1mm-long DWELL-based BRS laser is about 10GHz at 140mA. The modulation bandwidth is electrically limited by the RC parasitic limitation related to the BRS process. From the electrical response, we can extract the intrinsic response of the DFB laser and derive a theoretical modulation bandwidth as large as 16GHz as illustrated in Fig.3. The high intrinsic dynamic properties are confirmed by a damping factor as low as 0.3ns. Such low κ factor indicates a damping limit of modulation bandwidth of about 30GHz and therefore confirms the potential of QDash lasers for high speed applications.

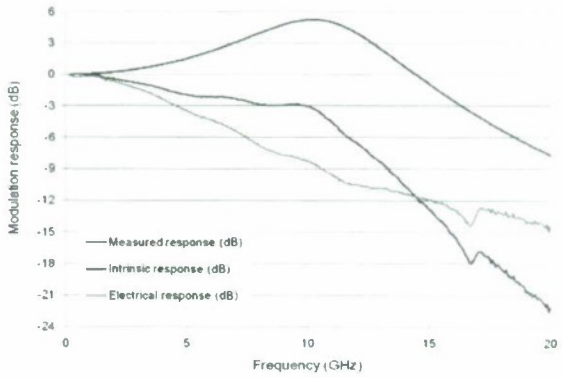

Fig.3: Small signal modulation response of a 1mm-long DFB laser.

The linewidth enhancement (LEF) factor above threshold of the 1mm-long DWELL-based BRS laser is as low as 2 (Fig.4), which is then comparable to the best MQW-based lasers. More remarkable, the LEF decreases with the injected current from ~2.1 to 1.8 (Fig.4) whereas the LEF increases significantly with injected current for standard MQW-based DFB lasers. At 10Gb/s, the transmission performances are in general strongly limited both by the transient chirp and the adiabatic chirp. This unique behavior of QDash-based sources would open the way to operate the DML at high current, which is very efficient to reduce the transient chirp, but keeping a low LEF. It would allow for increasing either the extinction ratio or the transmission distance.

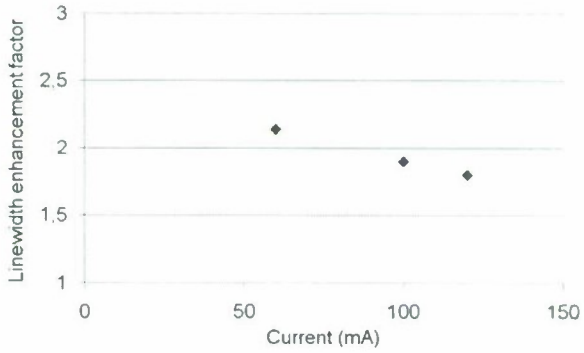

Fig.4: Linewidth enhancement factor above threshold of a 1mm-long DFB laser as a function of injected current.

IV. LARGE SIGNAL 10GB/S TRANSMISSION

For transmission evaluation, the output signal is sent to a 10Gb/s APD receiver, before error detection, either directly after the laser (back-to-back measurement) or after transmission in a 15, 25, 40 and 65km standard single-mode fiber. There is no EDFA and no filter in the setup and the launch power sent in the fiber is attenuated down to 3dBm for each biasing current in order to minimize non linearities.

Using a 500µm-long cavity DWELL based laser, the average DC current (100mA) and the modulation depth (+/- 50mA) were chosen to optimize the bit error rate (BER) at

10Gb/s for 65km transmission and these bias conditions were kept constant for shorter distances. The resulting extinction ratio was 3dB. As shown in Fig.5, the BER is reported in back-to-back configuration and for fibre lengths of 15, 25, 40 and 65km. Error free 10Gb/s transmission is achieved at constant bias current from back to back up to 65km. Notice that 10Gb/s transmission over the 38km theoretical limit has been already demonstrated using dispersion supported transmission [5] but this approach requires to modify the bias conditions for each distance as the dispersion in the fibre is compensated by the DFB chirp. This result obtained using a very simple configuration opens the way to the fabrication of low cost DML for access and metro applications.

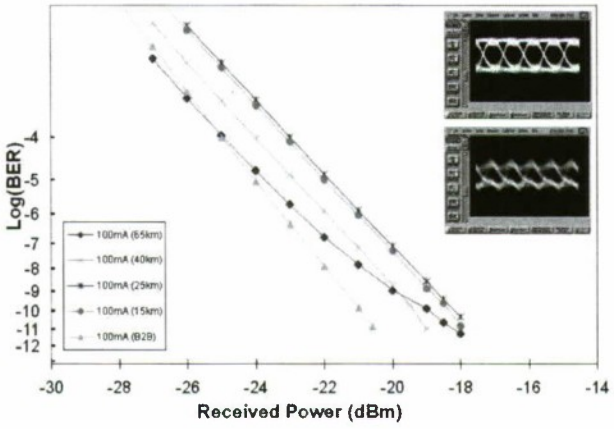

Fig.5: 10Gb/s bit error rate at 25°C in back to back and after 15, 25, 40 and 65km SMF transmission of a 500µm-long DFB laser. Inset: eye diagrams in back to back and after 65km.

V. Conclusion

The optimization of InP-based Quantum Dashes buried distributed feedback lasers including growth conditions, design and processing has been carried out. As a result, we demonstrated directly modulated lasers with modulation bandwidth of 10GHz and linewidth enhancement factor as low as 2 even at high injected current. Error free 10Gb/s transmission was achieved at constant bias current from back to back up to 65km of standard fibre. This result opens the way to the fabrication of a low cost DML for access and metro applications. Further optimization would be to increase the optical budget and the temperature operation for access applications and to enlarge the extinction ratio for metro applications.

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ULTRA-LOW THRESHOLD 1490 NM SURFACE-EMITTING BH-DFB LASER DIODE WITH INTEGRATED MONITOR PHOTODIODE

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Abstract

1490nm surface emitting BH-DFB-laser diodes incorporating a 45° turning mirror and an integrated monitor photodiode are presented for the first time. The devices show VCSEL-like threshold currents of as low as 3...7mA in the operation temperature range between 20°C and 90°C and a modulation bandwidth of >8GHz. The integrated monitor diode operates temperature independent and is therefore well suited for laser power control.

I. Introduction

Fabrication costs of conventional edge emitter DFB lasers are largely determined by the costs for facet coating, screening and selection of devices to guarantee key specifications, such as output power and single mode behaviour. These costs are significant because all this work has to be done on bar or even chip level. VCSELs represent a very attractive alternate laser structure because - apart from their high-speed capability in conjunction with low-power consumption - they offer the possibility of full on-wafer processing and testing associated with substantial cost reduction. However InP based VCSELs emitting in the long-wavelength range used for telecom applications still suffer from limited single-mode optical output power, especially in uncooled operation. Additionally, it is very challenging to achieve the wavelength accuracy required for DWDM or CWDM systems, and the combination with a monitor diode is rather difficult to accomplish.

Regarding single-mode surface emitting lasers there are alternatives to VCSELs, namely horizontal cavity DFB lasers using second order gratings [1,2] and DFB lasers employing a 45° turning mirror [3], the latter structure being commonly referred to as HCSEL. In this paper we present single-mode 1490 nm HCSEL devices featuring optical power-current characteristics that are approaching those of state-of-the-art InP based VCSEL to open up the way to eventually use very low power consumption VCSEL drivers. Furthermore we demonstrate the integration with a monitor photodiode. As with VCSELs the developed HCSEL devices allow for full on-wafer processing and testing.

II. Device Structure and Processing

The fabricated DFB-HCSEL devices rely on a MOVPE grown strain compensated MQW InGaAsP/InP layer structure, as used with edge emitting lasers, and a BH design with pn current blocking layers. Careful optimization of active layer, optical waveguide and DFB grating was the key to achieving low threshold operation. The 1st order DFB grating incorporating a $\lambda/4$ phase shift was formed by means of electron beam direct writing. The laser and the integrated monitor diode sections were defined by two separate p-contacts whilst otherwise using the same active layer structure. Employing an optimized chemically assisted ion beam etching process 45° facet mirrors were etched on both sides of the laser cavity, as sketched in Fig. 1.

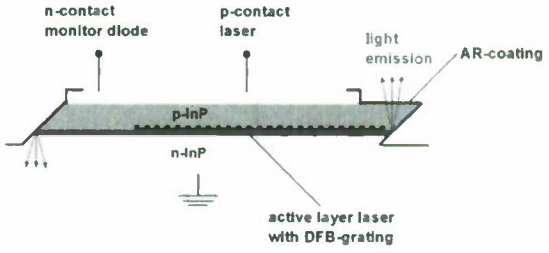

Fig. 1: Schematic cross-sectional view of developed HCSEL-structure

The front mirror deflects the emitted light to the surface facet via total internal reflection, whereas the rear mirror couples non-absorbed light out of the laser cavity thus suppressing

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back reflections. The surface above the output facet (right side) was anti-reflection coated applying an on-wafer deposition process. Thanks to the specific HCSEL design all lasers can be individually characterized and tested on-wafer using an adapted conventional wafer prober. The footprint of the HCSEL chip including the monolithically integrated monitor diode amounts to 310µm (L) x 250µm (W) only, being comparable to VCSEL lasers.
Fig. 2 shows a microscopic image of a processed device.

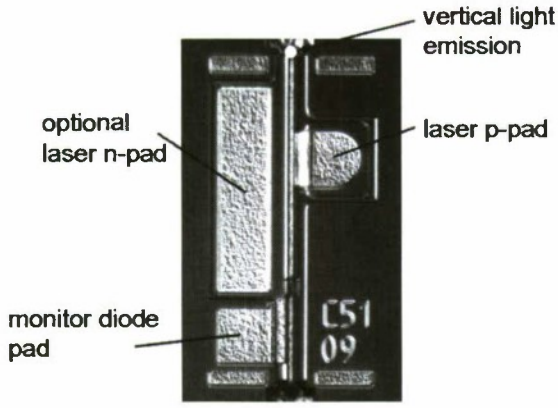


Fig. 2: Microscopic image of a processed HCSEL device with integrated monitor diode

III. Characteristics

The optical output power characteristics of a fabricated HCSE-DFB-laser is depicted in Fig. 3. The lasers exhibit extremely low threshold currents ranging from 3...7 mA over the operation temperature range from 20°C to 90°C associated with a T_0-value of >70K.

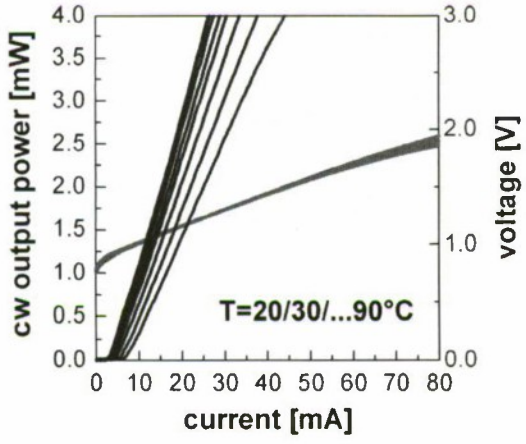


Fig. 3: CW HCSEL output power (mounted on heatsink)

The lasers show stable single mode emission with a side mode suppression ratio of 45dB at an operation current of 6mA only proving that both the on-wafer AR-coating on the front facet and the angled back facet yield sufficiently low residual facet reflectivity (Fig. 4).

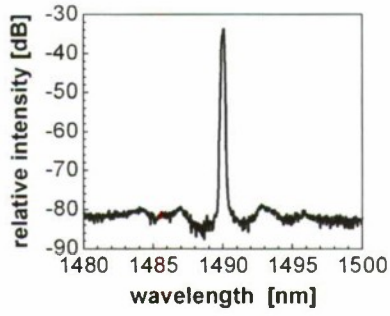
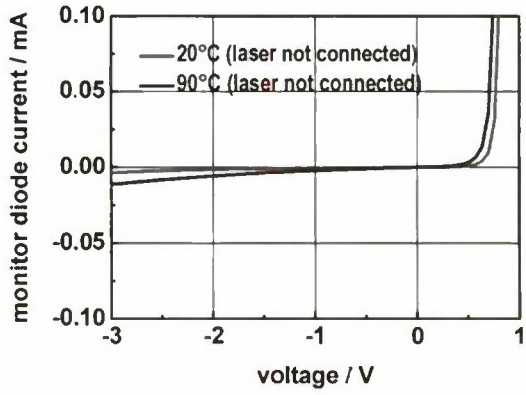


Fig. 4: HCSEL optical spectrum at 6mA operation current and T=20°C



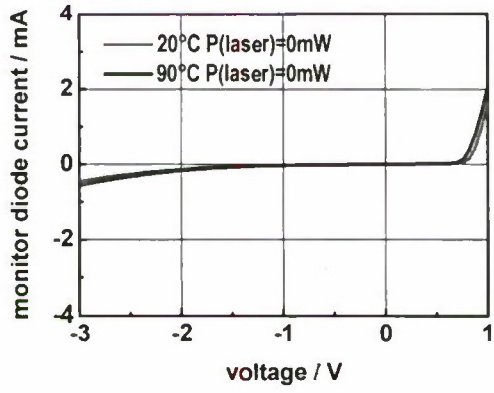


Fig. 5: Monitor diode current in dependence of the bias voltage at 20°C and 90°C: (top) laser not electrically contacted, (bottom) laser operation current = 0mA

Fig. 5 depicts the voltage dependence of the dark current of the monitor diode measured without having electrically contacted the laser section (top) and with the laser operation current set to 0mA (bottom), respectively. In the latter case an enhanced current flow at voltages < -2V is observed due to leakage current into the laser section caused by the limited electrical separation resistance of about 5kΩ between monitor diode and laser.

Nevertheless the integrated monitor diode shows a good linear dependence of the photo current on the optical output power (Fig. 6) and a weak temperature sensitivity only. Operation at -2V bias voltage turned out to be the optimum bias condition for temperature independent operation of the monitor diode. The difference between the 20°C and 90°C monitor current values at -2V bias voltage and at a fixed laser power amounts to about 8% only. This relatively small deviation suggests that the integrated monitor diodes can be used to control the laser output power in the full temperature range between 20°C and 90°C.

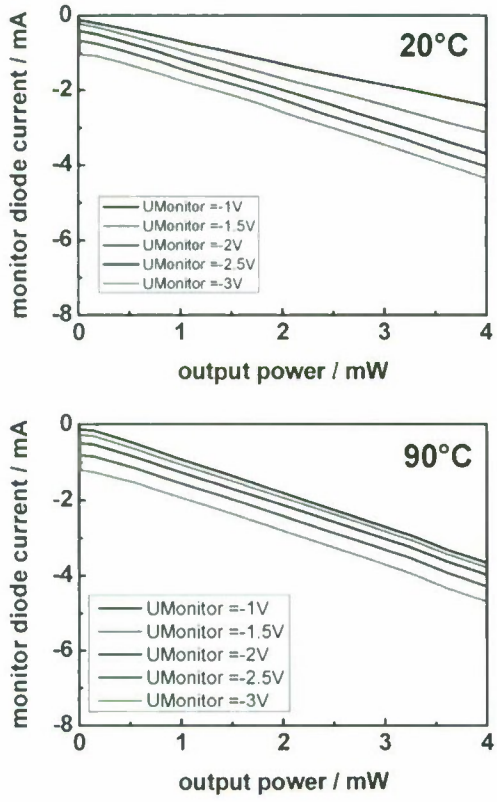


Fig. 6: Monitor diode current in dependence of the laser optical output power at T=20°C (top) and 90°C (bottom)

The optical far-field pattern of the vertically emitted optical beam is depicted in Fig. 7. The measured FWHM angles amount to 20° and 23° in the two perpendicular lateral directions thus providing a fairly circular beam profile to enable efficient fiber coupling of the devices.

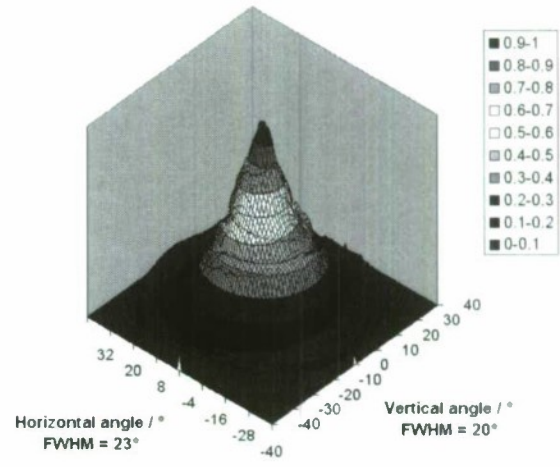


Fig. 7: Optical farfield of a HCSEL measured in vertical direction

The modulation bandwidth was determined by directly contacting the surface n- and p-contact of the laser with a RF probe head. No 50 Ω adaption was implemented here. As shown in Fig. 8 the modulation bandwidth at 12mA bias current amounts to about 7 GHz at 20°C and 5.5 GHz at 90°C allowing for low bias current uncooled direct modulation at 2.5Gb/s. The maximum 3 dB modulation bandwidth of these lasers amounts to > 8GHz.

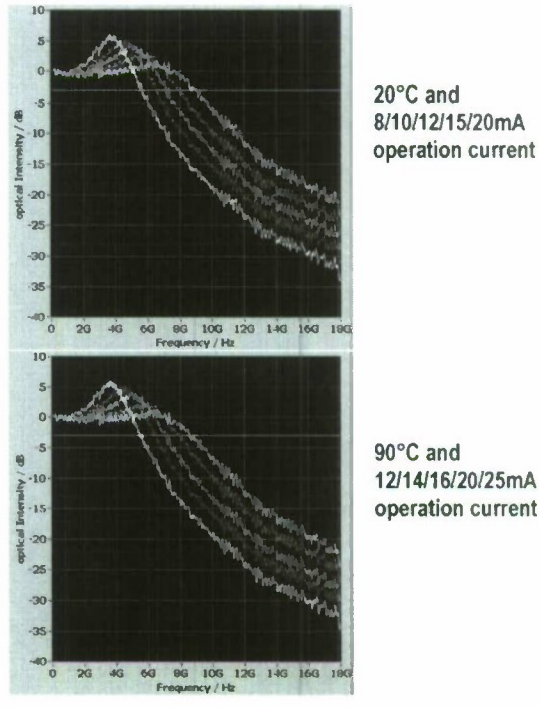


Fig. 8: Small signal frequency response of the HCSELs at 20°C (top) and 90°C (bottom) respectively

IV. Conclusion

1490nm DFB-HCSELs with integrated monitor diodes have been presented for the first time. The devices show ultra low threshold currents of 3mA at 20°C and 7mA at 90°C and deliver optical output power of well above 5mW in this temperature range. Whilst the current characteristics are approaching those of state-of-the-art VCSELs the output power performance is clearly superior. With further optimizing the laser design even lower currents are believed to be achievable thus eventually allowing to employ conventional low-power VCSEL driver circuits. The integrated monitor diode works nearly temperature independent although it uses the same layer structure as the laser itself. Nonetheless, if required for further refined photodiode performance an InGaAs based structure implemented by selective area growth could optionally be used.

Furthermore these devices can be fabricated also in one- or two-dimensional arrays enabling simultaneous coupling to multiple waveguides or fibers for parallel optical links.

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Thin-Film GaInAsP/InP Lateral Current Injection Type Fabry-Perot Laser — Improved Quantum Efficiency Operation —

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Abstract

Based on a theoretical analysis of internal quantum efficiency of a thin-film GaInAsP/InP lateral current injection type Fabry-Perot laser prepared on the semi-insulating InP substrate, its fabrication process was modified. As the results, the internal quantum efficiency was improved by a factor of 2 and the waveguide loss was reduced to 2/3 in comparison with previously reported devices. A threshold current of 11 mA and an external differential quantum efficiency of 33% were obtained for the device with 720 μm-long cavity and 1.7 μm-wide stripe under a room temperature continuous-wave condition.

Keywords- Lateral current injection, Membrane structure, Photonic Integrated Circuit

I. INTRODUCTION

With the ever increasing amount of data in LSI circuits, the CMOS speed should increase by utilizing the scaling law. However, scaling law has other effects such as signal delay, heat generation, and crosstalk for global wiring in the chips, which limit total performance of LSI chips. An introduction of optical interconnection can be a possible solution for these problems [1]-[4].

As the low power consumption light source for the optical interconnection on the chip, a membrane distributed-feedback (DFB) laser has been proposed. A membrane laser consists of a thin (~150 nm-thick) semiconductor core layer including the wirelike quantum-well (QW) active regions sandwiched by low-index polymer claddings [5]. Since this membrane DFB structure has a strong optical field confinement feature into the active region due to its high index-contrast waveguide structure as well as small volume of the active region, very low threshold operation was predicted and was demonstrated under an optical pumping at room-temperature continuous-wave (RT-CW) condition [5],[6]. A threshold pump power of as low as 0.34 mW under a RT-CW condition and a stable single-mode operation with a sub-mode suppression ratio (SMSR) higher than 30 dB up to 85°C have been reported [7]. However, no electrical injection has been reported.

To achieve injection-type membrane laser for light source in the photonic integrated circuits on the Si-LSI, a lateral current injection (LCI) structure is promising candidate. Although a LCI laser with thick (1 μm) current guiding layer has already been reported [8], [9], a thinner semiconductor layer is needed for the injection-type membrane laser to obtain high optical field confinement along the vertical direction. A RT-CW operation of a LCI buried-hetero structure (BH) laser, which consists of an only 400 nm-thick GaInAsP core layers with 5 QWs on a semi-insulating (SI) InP substrate as shown in Fig. 1, has been demonstrated [10]. However, due to the low internal quantum efficiency (19%), operation characteristics of this device were poor compared with those of vertical current injection type lasers [11].

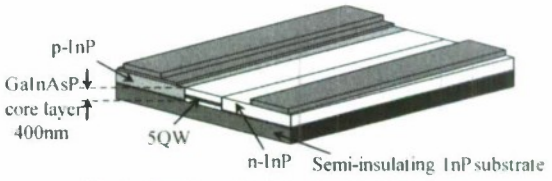

Fig. 1 Structure of a thin-film LCI-BH laser.

In this paper, we report a theoretical analysis of internal quantum efficiency of the LCI-BH laser and also a demonstration of improved lasing characteristics attributed to higher internal quantum efficiency.

II. THEORETICAL ANALYSIS

To investigate the causes of poor quantum efficiency in the previous reported device, the radiative recombination profiles of the LCI-laser have been simulated based on a semiconductor device simulator APSYS (Crosslight Software Inc.). Figures 2 (a) and (b) show the simulation results for the previous device [11] and for the present device, respectively. The active region

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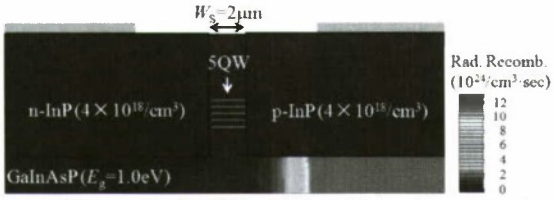
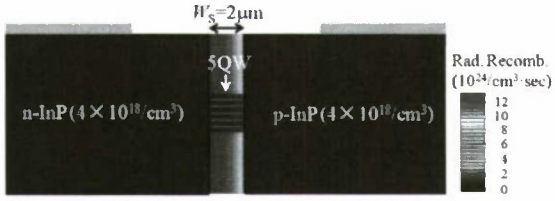


(a) With residual OCL (GaInAsP) under p- and n-regions.



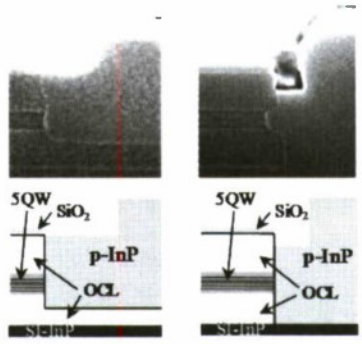
(b) No residual OCL under p- and n- region.

Fig. 2 Calculated amount of radiative recombination.

of these LCI-BH lasers consist of five 1% compressively-strained QWs (6 nm-thick, E_g = 0.8 eV) and 0.15% tensile-strained barriers (10 nm, E_g = 1.0 eV), sandwiched between optical confinement layers (OCLs, E_g = 1.0 eV, 150 nm-thick). The total GaInAsP layer thickness is 400 nm, designed to have about 5% optical confinement factor for 5QWs. Doping concentration of both p- and n-InP layers is 4 × 10^{18} /cm^3. The stripe width and the distance between p- and n- electrode are fixed to 2 μm and 10 μm, respectively.

The simulations were done at the injection current of 0.02 mA per μm (unit length along the stripe) which corresponds to an injected sheet carriers per unit time of 1.25 × 10^{18} /cm·sec carriers or 10 mA with the cavity length of 500 μm. In the previous device as shown in Fig. 2(a), about 90 nm-thick OCLs remained under the p-InP caldding layer (as can be seen in the SEM views and corresponding illustrations in Fig. 3).

Due to the carrier leakage in the residual OCL, 2.1 × 10^{17} /cm·sec of carriers are radiative recombination element in the active region. This means that expected internal efficiency at this current level can be only 17%. On the other hand, 57% (7.1 × 10^{17} /cm·sec) of carriers are consumed as radiative recombination in the residual OCL. This phenomenon is especially apparent under the p-InP region because of the slower mobility of holes compared to that of electrons. By eliminating this residual OCL, the radiative recombination outside of the quantum wells reduces and the recombination in the active layer increases to 37% (4.6 × 10^{17} /cm·sec), which is approximately two times higher than that for the previous one, as shown in Fig. 2(b).



(a) Previous (b) This work

Fig. 3 Cross sectional SEM views (upper) and corresponding illustrations (lower).

III. EXPERIMENTAL

Figure 3 shows the cross sectional SEM views and schematic illustrations of two types of devices in the previous report (a) and this work (b). In this work, the OCL at p- and n- regions were totally etched to reduce carrier leakage. The fabrication processes illustrated in Fig. 4 are as follows. Firstly, an initial wafer with undoped GaInAsP core layers consisting of strained compensated 5 QWs as mentioned in simulated structure, were prepared by organo-metallic vapor-phase-epitaxy (OMVPE) growth on a SI-InP substrate (Fig. 4-1). Then, the lateral junction structure was fabricated by 2-step photolithography, reactive-ion-etching (RIE), and OMVPE selective area regrowth [10]. A 7 μm-wide mesa structure were formed with a SiO_2 mask and RIE (Fig. 4-2). After removing the plasma damaged surface by sulfuric acid based solution, n-InP was selectively regrown at the side of the mesa as a cladding layer (Fig. 4-3). Next, by etching the part of the wide mesa and the one side of the buried n-type layer, narrow wide stripes were formed (Fig. 4-4). Then, p-InP cladding and p-GaInAs contact layers were regrown (Fig. 4-5). After these junction formation processes, a part of the contact layer near the stripe edge was removed by sulfuric acid solution to reduce optical absorption by p-GaInAs. Finally, Ti/Au electrodes were deposited on the p-GaInAs and the n-InP area (Fig. 4-6).

After polishing the wafer and cleavage into bars, measurements were done under a RT-CW condition. Figure 5 shows typical light output (*L-I*) and applied voltage-current (*V-I*) characteristics of the previous and present devices. A minimum threshold current of 11 mA and an external differential quantum efficiency of 33% were obtained for the device with 720 μm-long cavity and 1.7 μm-wide stripe while those for previous device were 19 mA and 8.1% for the device with 730 μm-long cavity and 1.4 μm-wide stripe under RT-CW conditions, as shown in Fig. 5. The threshold current density (J_{th}) normalized by the stripe width W_s and the cavity length L was as low as 900 A/cm^2

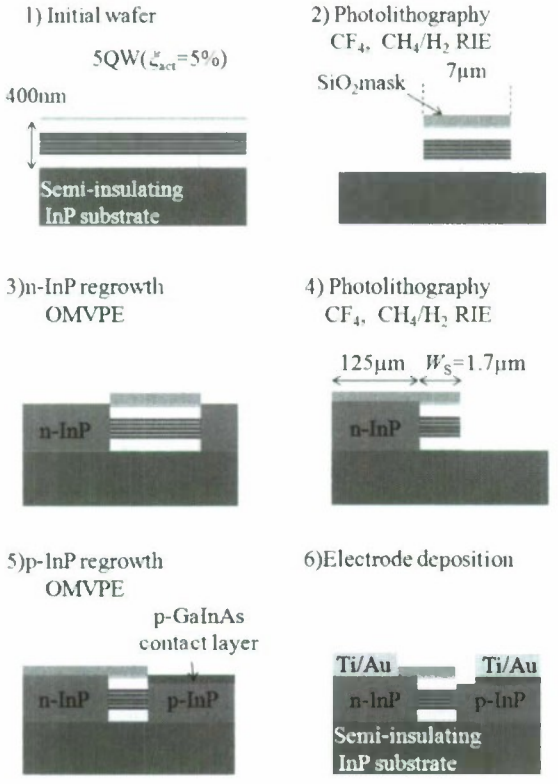


Fig. 4 Fabrication processes.

which is almost a half of that of the previous device (1.9 kA/cm^2). A waveguide loss of 4 cm^{-1} and the internal quantum efficiency of 40% were obtained from the relation between the cavity length and the inverse of the differential quantum efficiency as shown in Fig. 6. This internal quantum efficiency was two times higher than that (19%) of the previously reported device. Hence these results quantitatively agree with the above mentioned simulation results in Section II. The waveguide loss of the previous device was 6 cm^{-1} [11], which can be attributed to slight roughness of the surface of residual OCL. The rise-up voltage was observed to be 0.8 V and the differential resistance at the threshold current was around 20 Ω which is 2-3 times higher than that of our conventional DH lasers.

The transparent current density J_{tr} per well is estimated to be 90 A/cm^2 from the dependence of the square root of J_{th} on the inverse of cavity length, as shown in Fig. 7 [12]. This value is slightly higher than that of conventional DH lasers fabricated in our laboratory. Even though the internal quantum efficiency was much improved, it is still low compared with conventional DH lasers. These poor characteristics are mainly attributed to weak carrier confinement in the LCI structure because the hetero

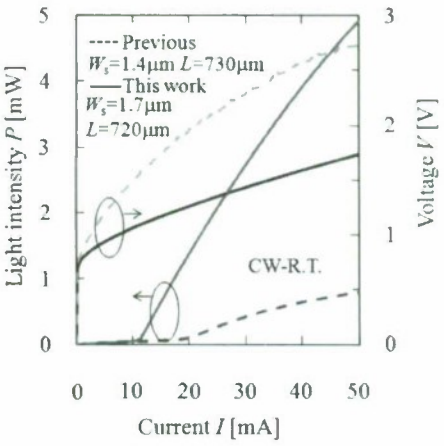


Fig. 5 L-I and V-I characteristics.

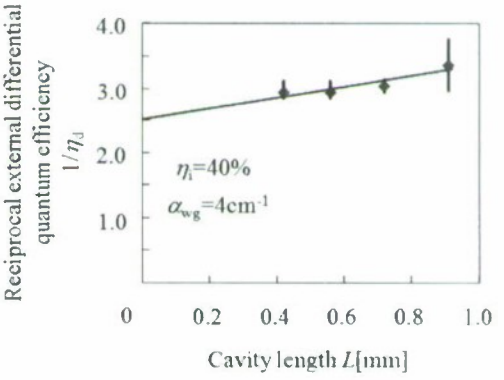


Fig. 6 Dependence of inverse of external differential quantum efficiency on cavity length.

barrier between the quantum well and the OCL is parallel to the carrier's flow.

Further increase of internal quantum efficiency can be attained by an adoption of wider band gap materials like an InP for the OCLs and barrier layers and an increase of the number of QWs because the LCI lasers are immune from carrier pile-up problem of holes in conventional vertical injection type lasers. Furthermore an adoption of thin (150-200 nm thick) membrane structure sandwiched by low refractive-index material such as benzocyclobutene enhance the optical confinement factor by a factor of around 3, hence much lower threshold current as well as higher quantum efficiency.

IV. Conclusion

Lateral current injection type buried-hetero structure lasers were investigated by using a simulation tool, and improved lasing properties attributed to increase of internal quantum efficiency

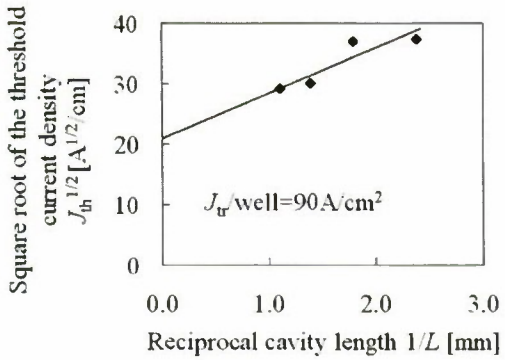


Fig. 7 Dependence of square root of threshold current density on reciprocal cavity length.

were obtained experimentally by completely etching the residual GaInAsP optical confinement layer beneath the n- and p-InP cladding layers. These experimental results were in good agreement with theoretical ones. This lateral current injection structure can be applied to electrically driven low power consumption membrane lasers as well as other photonic components for future on-chip optical interconnections.

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ANTIMONIDE BASED INFRARED MATERIALS: DEVELOPMENTS IN InSb AND GaSb SUBSTRATE TECHNOLOGIES

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Abstract

In this work we report on the crystal growth and surface characterization of antimonide substrate materials. The Czochralski technique has been used to grow single crystal InSb and GaSb ingots with typical etch pit densities of <1E2 cm^{-2} and <2E3 cm^{-2}, respectively. X-Ray topographs (XRT) have enabled the high resolution mapping of the defect structure in GaSb substrates, demonstrating that ingots can be produced with large areas of zero dislocation density. Epitaxy-ready surfaces with very low levels of surface roughness and uniform oxide coverage have been demonstrated for 4" GaSb. We have shown that smaller diameter antimonide ingot and wafer production processes can be scaled to deliver high quality substrates in large diameter form.

I. Introduction

Indium antimonide (InSb) and gallium antimonide (GaSb) are important Group III-V compound semiconductors for photodetectors that operate in the mid (3-5 μm) to the long wavelength region (8-12 μm) of the infrared (IR) spectrum. Interest in these materials is driving the development of several new detection technologies that are important for military, industrial and medical applications[1,2,3]. Furthermore, several niche applications for antimonides also exist which include mid-infrared edge emitting lasers, ultra-high high mobility transistors, magnetic sensors and thermo-photovoltaic cells.

When compared with other commercially available compound semiconductors such as GaAs and InP, the antimonides are considered as a niche product manufactured in limited quantities and mostly in 2" diameter wafer form. As such, demand for these materials has matured slowly, but more recently requirements for large format, high performance infrared detectors is driving substantial new interest in the development of larger diameter substrates. Of particular note is the industry's requirements for photodetectors that operate in the long wavelength IR region, this being met by sophisticated Ga(In)Sb/InAs based strained layer superlattice (SLS) structures deposited by molecular beam epitaxy (MBE)[4]. For such devices, 4" GaSb substrates will be required, requiring current small diameter wafer production technologies to be successfully scaled.

In this paper, we report on the bulk crystal growth of InSb and GaSb materials. Then we discuss our latest work on the scaling of our GaSb processes to deliver 4" substrates suitable for the deposition of high quality epitaxially grown detector structures.

II. Growth and Characterization of Antimonide Substrates

A. Bulk Crystal Growth

GaSb (100) and InSb (211) ingots were grown by the Czochralski (Cz) method[5,6]. The Cz method is well established for the growth of Group III-V compound semiconductor crystals and in addition to being the choice of production technique for antimonide crystals, it is also used within the industry to manufacture InP materials too[7]. Fig. 1 shows examples of typical GaSb and InSb crystals grown by the Cz method.

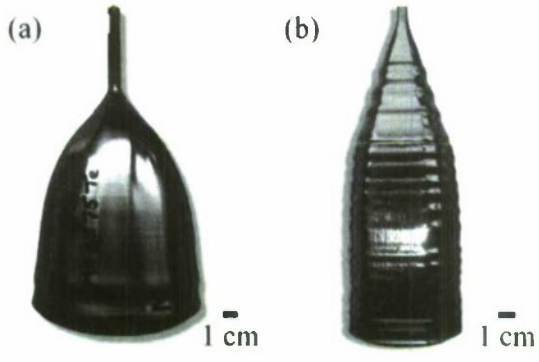

Fig. 1: Images of single crystal (a) 3" GaSb-Te (100) and (b) 3" InSb-Te (211) ingots

For the commercial production of InSb, the majority of ingots are grown in the (211) direction. This orientation strikes the optimum balance between growth yield and the requirement of InSb detector devices to be fabricated on (n11) type substrates. Production of InSb (100) crystals is possible, but difficulties are encountered in the growth of this orientation type which can have an adverse effect on yield. Furthermore, applications of InSb (100) remain very limited, so should wafers of this orientation be required, these are oblique cut from (n11) type crystals. GaSb crystals are grown in the (100) plane. The exclusive application of this material remains as a

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mono-crystalline substrate for epitaxial growth where the orientation of the wafer remains unchanged, or is subtlety mis-oriented away from the (100) direction to optimize epitaxial morphology for a given layer deposition condition.

In the production environment, the aim is always to maximize the number of substrates that can be cut from each ingot that meet a well defined set of physical, electrical and crystallographic specifications. For InSb and GaSb, the quantity of 2" and 3" wafers that can be cut from one ingot is already reasonable, Table 1, but as production demands increase it is anticipated that longer ingots will be required. This is especially the case for 4" diameter crystals where the number of wafers that each ingot can yield is relatively low. This is the subject of development efforts at Wafer Technology and the target will be to increase the number of wafers that each ingot yields.

Table 1. Comparison of antimonide ingot dimensions and typical wafer quantities cut.

Ingot Diameter (inches)	Length (mm)	Number of Wafers
2	80-220	50-150
3	80-110	50-75
4	50-70	30-40

B. Crystal Quality Assessments

Growth of any III-V semiconductor crystal is prone to the incorporation of several defect types. These can have the effect of reducing yield or limiting the bulk material specification that can be offered. Examples of such defects are twins, polycrystalline growth and dislocation clusters[8]. Whilst the long-term vision of crystal growth has always been to produce dislocation-free crystals, the complexities of the Cz system means that defect suppression is very much part of any growth process methodology. Scaling growth processes presents further challenges to address in defect reduction and in support of growing high quality antimonide crystals, this topic has received significant attention in this work.

Dislocation density is a measure of crystalline quality and assessments were made using a proprietary dislocation revealing etch and measurement by optical contrast microscopy. Typical etch pit densities (EPD) of <1E2 cm^{-2} are found in InSb which is considered one of the lowest defect type compound semiconductor materials available commercially. GaSb though is a more dislocative material where EPD values of 1-2E3 cm^{-2} are typically obtained. The spatial distribution of etch pits was assessed by the same technique where the density of etch pits at 69 individual locations across a wafer was mapped. Although considered as a low resolution method of assessment that is mostly used to provide feedback on crystal homogeneity, it is potentially of significant interest at the device level where the spatial performance of for example, a detector can be correlated with the local quality of the underlying substrate and epitaxial layers. Fig. 2 shows etch pit density maps for typical 3" InSb-Te (211) and 3" GaSb-Te (100) substrates

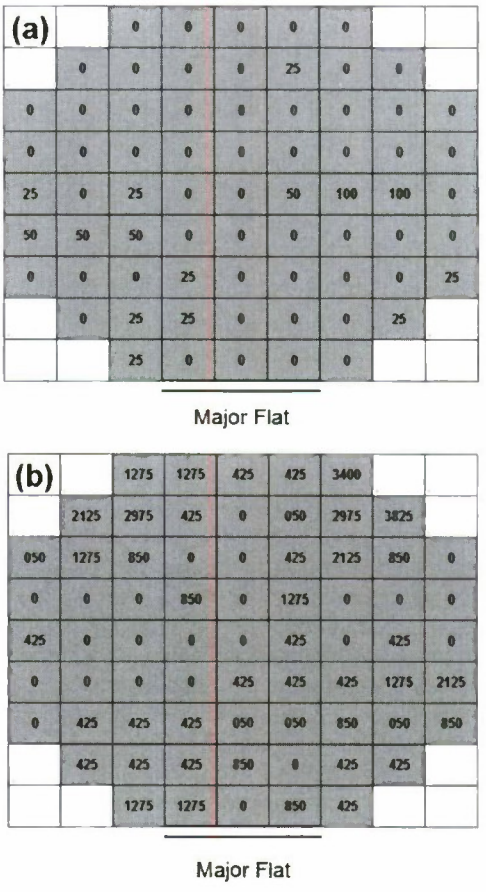

Fig. 2: Etch pit density maps measured by optical contrast microscopy for (a) 3" InSb-Tc (b) 3" GaSb-Te substrates.

The crystal quality of GaSb substrates has also been assessed by synchrotron white beam X-Ray topography (XRT). This high resolution method of dislocation imaging has been used to characterize extended defects and strain in GaSb substrates and has supported improvements in the bulk quality of our GaSb over successive generations of 2" and 3" ingots grown. Details of this measurement technique are outside the scope of this work, but can be found elsewhere[9]. Fig. 3(a) shows a topograph taken at the centre of an older generation 3" GaSb substrate with a dislocation density of 1,700 cm^{-2}, these dislocations appearing as bright lines in the topograph. In contrast to that result, the topography for current generation 3" product (Fig. 3b) shows no dislocations in the centre part of the wafer, although analyzing the defect density at the wafer edge revealed that the dislocation density in this part of the substrate is still higher than in the centre of the wafer.

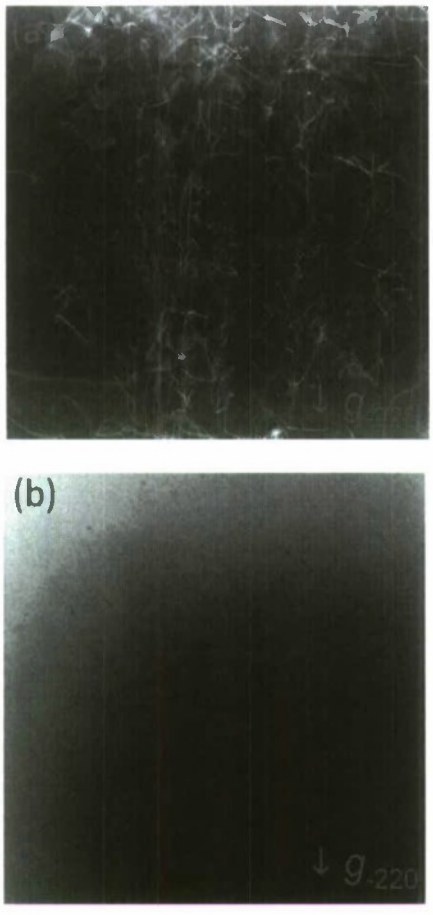

Fig. 3: X-Ray topographs from (a) the centre of a first generation 3" GaSb-Te substrate. Dislocation lines with a density of 1,700 cm-2 show up as bright lines and (b) centre of a current generation 3" GaSb-Te substrate where no dislocations are present.

Analysis of a first generation 4" GaSb wafer by XRT, Fig. 4, reveals a similar trend where the central portion of the substrate has a zero or very low number of dislocations which then increase in density towards the substrate edge. It should be pointed out that the cellular structure shown in the image is a measurement artefact and does not relate to the dislocation structure of the crystal grown.

Although XRT is a powerful method that can analyse the defect structure of crystals in significant detail, its application on a routine basis is limited because of cost practicality issues associated with the use of a synchrotron light source facility. Usefully though, etch pit density assessments performed by optical contrast microscopy are quick, easy to perform and the results can be correlated with high resolution determinations by XRT in a semi-quantitative way.

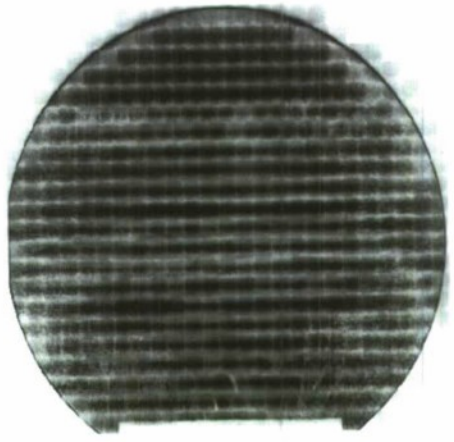

Fig. 4: X-Ray Topograph of a 4" GaSb-Te substrate. Dislocations show up as fine bright lines. Note that the cellular structure in the image is an artefact of the measurement scan.

The results presented for first generation 4" GaSb substrates shows a similar trend to past iterations of 2" and 3" GaSb ingots grown. Whilst a large proportion of the wafer area is characterized by regions of high quality material with zero or low levels of dislocation density, the peripheral structure at the wafer edge demonstrates that enhancements to the crystal growth process are required. There are several strategies by which such improvements can be made and these are the subject of on-going development efforts at Wafer Technology.

C. Surface Analysis

High quality surface finishing is an important requisite for all compound semiconductor substrates. This is especially the case for epitaxial layer growth where a clean and uniform starting substrate surface is required that needs no form of pre-treatment prior to growth. Whilst the vast majority of InSb devices are based on the fabrication of implanted junction devices that do not demand 'epi-ready' levels of finishing, GaSb surfaces are challenging to prepare for epitaxy, not only when compared with InSb, but with respect to other compound semiconductor materials too[10]. Surface polishing techniques have previously been developed here that address this concern. Supporting this is the formation of a uniform surface oxide which must desorb cleanly and consistently prior to layer growth. Surface oxides on epitaxy ready polished substrates were assessed using a Woollam VASE spectroscopic ellipsometer (SE) that maps oxide uniformity using the analysis of polarized light reflections from the substrate surface[11]. The 4" GaSb oxide thickness uniformity map, Fig. 5, shows an average oxide thickness of 45 Å and uniformity of 4 Å which is very comparable to that seen on 2" and 3" GaSb.

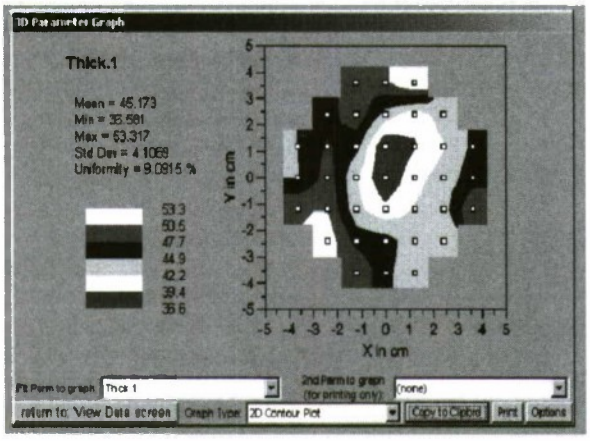

Fig. 5: SE map of oxide thickness on a 4" GaSb substrate

Morphology assessments have been made on substrates using a Taylor Hobson 3D optical profiler that maps surface roughness using white light interfometry[12]. Surface roughness (rms) measurements were made over a sample area of ~300 μm^2 at five points across the surface of a 4" epitaxy-ready substrate. From this we have demonstrated a uniformly smooth surface with an average (rms) surface roughness of 2.0 nm which is very comparable to assessments made on 2" and 3" GaSb substrates.

Fig. 6 shows an example of a surface roughness (peak to valley, nm) map measured using the same technique and displayed as a color image where height information is represented by color changes.

These results demonstrate that high quality 4" GaSb surfaces have been produced that are very comparable in their characteristics to those of smaller diameter GaSb substrates. Reproducible substrate preparation techniques have enabled uniform oxides and low roughness surfaces to be produced, both of which are important requirements for high quality epitaxial growth. Epitaxial growth testing of these 4" GaSb substrates has recently been reported elsewhere[13].

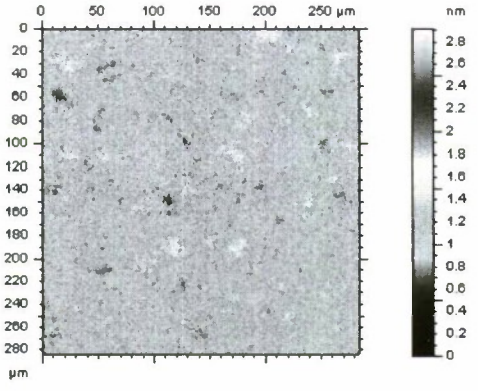

Fig. 6: Surface roughness (peak to valley, nm) map of 4" GaSb substrate.

III. Conclusion

In conclusion, we have shown that high quality single crystal 3" and 4" InSb and GaSb ingots can be produced by the Cz method. Defect mapping by optical contrast microscopy and X-Ray topography has enabled the dislocation structure of ingots to be quantified. Epitaxy-ready surface finishing processes have been successfully scaled to larger format GaSb substrates delivering surfaces with high quality attributes for layer growth.

Acknowledgements

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EFFECT OF GRAVITY ON THE GROWTH OF TERNARY ALLOY SEMICONDUCTOR BULK CRYSTALS

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The paper describes microgravity experiment using Chinese recovery satellite and the in-situ measurement of composition profile in the solution by X-ray penetration method to make clear the effect of gravity on the growth of InGaSb ternary alloy semiconductor crystals.

I. Introduction

High quality homogeneous $In_xGa_{1-x}Sb$ alloy semiconductor crystals are required for the fabrication of optoelectronic devices such as detectors, thermo-photo-voltaic cells, etc., since wavelength and lattice constant are controlled in the range of 1.7 – 6.8 μm and 6.0959-6.4794 Å by adjusting the indium composition, respectively. However, it is very difficult to grow high quality homogeneous $In_xGa_{1-x}Sb$ bulk crystals due to the large separation between the solidus and liquidus lines in the InSb-GaSb phase diagram (1). Since the composition in the crystal is different from that in the solution, the rejected solute accumulates in the solution during growth. As a result, the composition in the crystal changes with time. Due to segregation phenomenon and temperature fluctuation caused by convection, interface breakdown easily occurs and consequently polycrystalline crystals are grown (2-3). Since the transportation of the solute is affected by convection, the dissolution and growth processes are strongly influenced by gravity. The main attraction for the microgravity condition is that it is possible to suppress the complex convective heat and mass transports and make deeper insight into transport phenomena.

There are several crystal growth related studies carried under microgravity conditions. For instance, Witt et al. grew a Te-doped InSb crystal in Skylab and achieved uniform dopant distribution (4). Kinoshita et al. grew PbSnTe crystals in the SL-J/FMPT mission, and demonstrated that the etch pit density was reduced (5). Nishinaga et al. and Duffar et al. showed that the quality of GaSb crystals was improved under microgravity (6-7).

We have performed several microgravity experiments using space shuttle, drop tower, Chinese recoverable satellite and airplane (8). The effects of diffusion and Marangoni convection on the mixing of multi-component melts have been investigated in the space shuttle (9-11). In the drop tower experiments, in-situ solidification process was observed using a high speed CCD camera (12). The effects of gravity on the shape of liquid-solid interface and composition profiles have been clarified by comparing the experimental results in the Chinese recoverable satellite and on earth (13). The effects of the gravitational direction on the dissolution and growth processes were investigated by inclining the electric furnace on earth (14). The flow pattern and composition profiles have been calculated as a function of gravity level (15-16). The experimental and numerical results showed that the shape of the growth interface and composition profiles were strongly influenced by gravity.

We have grown ternary bulk crystals by the temperature gradient freezing method combined with the heat pulse technique. (17-18). To grow homogeneous crystals, the balance among the dissolution rate of feed, growth rate of crystal and the transportation of solute in the solution is very important. Therefore, the development of the in-situ measurement technique of the composition profile in the solution during growth is strongly required. We have applied the X-ray penetration method using a CdTe line detector to investigate the composition profile in the solution (19).

The paper describes microgravity experiment using Chinese recovery satellite and the in-situ measurement of composition profile in the solution by X-ray penetration method for making clear the effect of gravity on the growth of InGaSb ternary alloy semiconductor crystals.

II. Microgravity experiment using Chinese recoverable satellite

A. Experimental method

To prepare the samples for microgravity experiment, GaSb single crystals were grown by the Czochralski method. For the growth of GaSb, elements of Ga and Sb were charged in a carbon crucible, and were heated by r.f. induction current in the hydrogen atmosphere. The grown crystal pulled in the <111> direction was about 10 mm in diameter

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and 110 mm in length. InSb crystals were grown by the same method. These crystals were transformed into cylindrical shape by using a lathe blade and the GaSb(111)A-InSb-GaSb(111)B sandwich sample was prepared as shown in Fig. 1(a). Fig. 1(b) shows the configuration of an ampoule. The size of the ampoule was 13 mmφ x 122 mm long. The GaSb(111)A-InSb-GaSb(111)B sandwich sample was inserted in a BN tube and then put into a quartz tube. To prevent accidental breaking of the ampoule and to adjust the volume change from solid to liquid and vice versa, both the ends of the sample were packed by carbon sheets. The ampoule was evacuated to 10^{-4} Pa, and then sealed off. The outside view of the ampoule is shown in Fig. 1(c). The white portion is the BN tube and the black parts are carbon sheets. Mechanical test was done on the ampoule both by applying vibration and by rapid heating and cooling. Subsequently it was made sure that the ampoule could be used safely for the microgravity experiment.

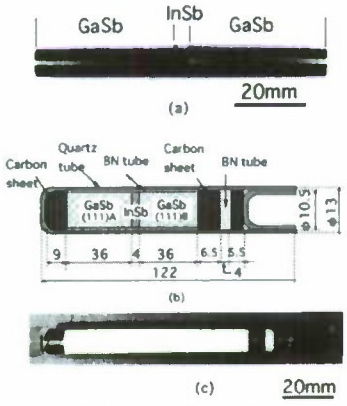

Fig. 1 (a) GaSb(111)A-InSb-GaSb(111)B sandwich sample, (b) Ampoule configuration (c) Outside view of ampoule.

The temperature-time profile of the microgravity experiment using a Chinese recovery satellite is shown in Fig. 2. The temperatures were measured by two thermocouples inserted into the heater block. T_1 was used to measure the temperature at the center of the sample, and T_2, at a point 20 mm away from the center. The temperature difference between T_1 and T_2 was about 20°C. The sample was heated to 706°C, and decreased at an average rate of 0.5°C/min. The total period of the experiment was 6 hours. The gravitaty level was $10^{-4} \sim 10^{-5}$ G. The experiment was carried out on earth in a vacuum chamber using the same furnace to compare with the microgravity experiment. The temperatures were measured at three different points: center of the sample and at two other symmetrie points 20 mm away from the center. The temperatures were the same at the symmetric points.

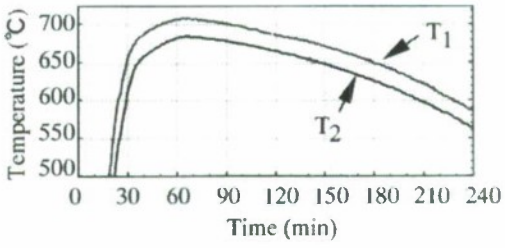

Fig. 2 temperature-time profile of the microgravity experiment using a Chinese recovery satellite.

B. Numerical method

In order to understand the effect of gravity on the shape of solid/liquid interface, numerical simulation was carried out. Fig. 3 shows the configuration and coordinate system for the analysis. The symmetrical model was used, and the half-zone of the system was solved. The governing equations of continuity equation, Energy equation, Diffusion equation, and the boundary conditions were solved by the finite difference method. The relationship between temperature and composition was obtained using InSb-GaSb binary phase diagram.

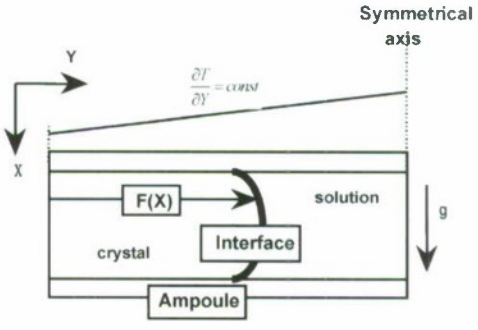

Fig. 3 Configuration and coordinate system for the analysis.

C. Results and discussion

Figs. 4(a) shows the outside view, the schematic representation of the dissolved area, and the Ga composition profile around the center of the space-grown crystal. For the comparison, the results of the earth-grown crystal are shown in Fig. 4(b). The Ga composition was measured by Energy Dispersive X-ray Spectroscopy (EDS) in the divided areas of 2.0 x 1.6 mm^2. The shape of the interface was almost parallel and the Ga composition was almost uniform across the radial direction for the space-grown crystal. On the other hand, the shape of the interface of the earth-grown crystal broadened toward the

gravitational direction. The Ga composition deereased from the upper region towards the lower region. This indieated that the gravitational segregation occurred on earth. Thcse results elearly suggest that gravity affeeted not only the eomposition profiles but also the shape of the solid-liquid interfaee.

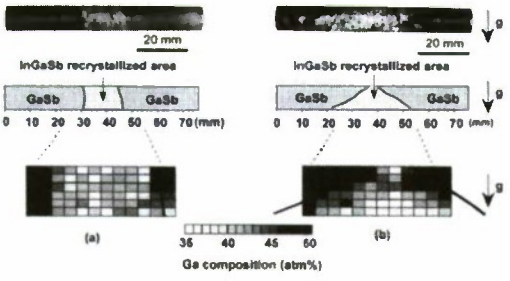

Fig. 4 Outside view, the sehematie representation of the dissolved area, and the Ga composition profile around the eenter of the samples. (a) Spaee-grown erystal, (b) Earth-grown crystal.

Figs. 5 (a) and (b) show the numcrical simulation results at 587 °C for zero and 1G gravity fields, respectively. The Ga eomposition profiles in the solution were quite different for both the eases. Under zero gravity, dissolved GaSb diffused from the interfaee towards a region far from the interfaee in the solution. This brought about the composition gradient along the axial direetion in the solution. However, the Ga eomposition was uniform along the radial direction. Therefore, the dissolution of GaSb took plaee uniformly at the interface. This resulted in the flat interface. On the contrary, under 1G gravity, the Ga composition was not homogeneous in the radial direetion. A large amount of Ga-rich solution moved to the upper region due to buoyaney sinee the density of liquid GaSb (6010 kg/em^3) was smaller than that of liquid InSb (6320 kg/em^3). This eomposition gradient beeame a driving foree of flow at the interface. At the solid-liquid interfaee, the dissolution of GaSb in the upper region was suppressed due to the existence of large amount of Ga eomposition in the upper region of the solution. On the other hand, in the lower region of the solution, a large amount of In eomposition was aeeumulated. Sinee the GaSb eomponent was insuffieient, the dissolution of GaSb into the solution was enhaneed. As a result, the shape of solid-liquid interfaee broadened towards the bottom. These numerieal results qualitatively explain the experimental results shown in Fig. 4.

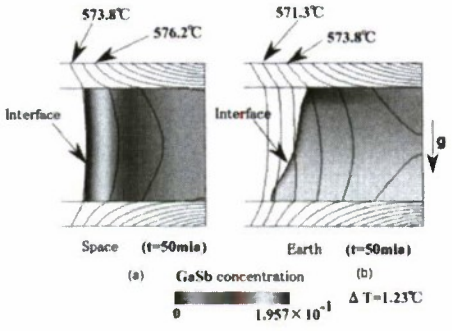

Fig. 5 Calculated Ga compositi0n profiles under (a) Zero gravity, (b) 1G Gravity.

III. Measurement of composition profile by X-ray penetration method

Fig. 6 indieates the eonfiguration of the sample and the temperature profile. Reetangular shaped GaSb(seed)/InSb/GaSb(feed) sandwieh sample was used for the experiment. The dimensions of GaSb (seed, feed) and InSb samples are 6 mm x 6 mm x 3mm and 6 mm x 3 mm x 3 mm, respectively. In order to observe the dissolution process and composition profile of the solution, the sample should be inserted into the material whieh is transparent to X-rays. In the present investigation, boron nitride (BN) and quartz were seleeted as transparent materials for X-rays sinee the absorption by them was very small eompared with GaSb and InSb. The sandwieh sample was inserted into the BN tube and it was inserted into the quartz ampoule. The quartz ampoule was evaeuated about 10^{-4} Pa and then sealed.

The sealed ampoule was fixed into the furnaee vertically. In order to get the inside temperature profile at the sample position, dummy sample was prepared with BN tube and it was inserted into the quartz. The quartz ampoule with dummy sample was sealed and then made a hole through feed side to seed end. The temperature profile in the furnaee at the sample position was measured by eonneeting the CA thermoeouples inside a dummy sample at the seed end and feed end before the X-ray penetration experiment. With respect to the reference temperature 650°C, the inside temperatures of seed end and feed end were measured as 525.2°C and 581.7°C, respectively. The temperature gradient at the sample position was fixed as 3.7°C/mm. The GaSb feed side was set up at high temperature region and GaSb seed side was set up at low temperature region. During the experiment, the thermoeouple was eonneeted at

the middle of the furnace for the measurement of reference temperature. The temperature of the furnace was monitored by using the reference temperature.

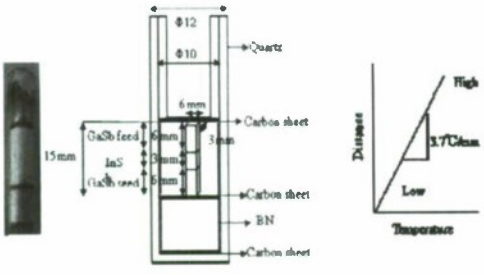

Fig. 6 Sample configuration and temperature profile

Fig.7 shows the X-ray penetration measurement system configuration. The furnace was fixed on a platform, which can be moved along the three directions x, y, z and can be rotated along the 360°. X-ray souree is the tungsten target with an acceleration voltage 150 kV and the current 0.1 mA. The detector is a rectangular shape CdTe line sensor which has 64 cells in x-direction and 1510 cells in y-direction. The size of the each eell is 0.1 mm. So the total active area of the detector is 6.4 mm x 151 mm. In order to get the relationship between the X-ray intensity and $In_xGa_{1-x}Sb$ composition, the solidus and liquidus X-ray penetration intensities of the GaSb and InSb standard samples were measured. By making the calibration line between the penetrated X-ray intensities of the standard samples, $In_xGa_{1-x}Sb$ composition was measured.

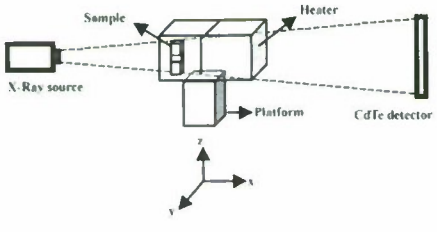

Fig. 7 X-ray penetration measurement system configuration.

Fig. 8 shows the combined X-ray images of the sample as a function of time. The room temperature figure shows that solid GaSb(seed)/InSb/GaSb(feed) sandwich sample. The light region and dark region indicate the GaSb and InSb, respectively. Since the X-ray penetration intensity of InSb is smaller than that of GaSb, the InSb region is seen as darker compared with GaSb region. While increasing the temperature, InSb was melted at 640°C in 4 min. During this phase transition, volume of InSb melt was reduced due

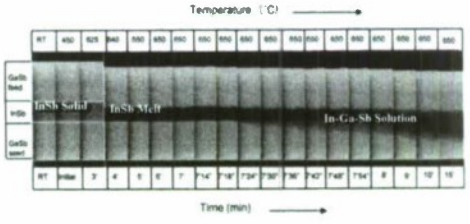

Fig. 8 X-ray images of the sample as a function of time.

to the density difference between the solid (5.78 g/cm^3) and liquid (6.32 g/cm^3) of InSb, and InSb melt region became darker compared with InSb solid region. Since the X-ray penetration intensity of InSb melt was smaller than that of InSb solid, the InSb melt region looked darker. Once the InSb was melted, the temperature was maintained as constant at 650°C for the enhancement of dissolution of GaSb into InSb melt. From 7 min 30 sec, GaSb seed and feed were started to dissolve into the InSb melt and the interface position moved towards the GaSb seed end.

Gallium composition profile of the solution was measured by making the calibration line between the liquidus intensities of GaSb and InSb. Fig. 9 (a), (b), (c), (d) and (e) show the Ga composition profile of the In-Ga-Sb solution at 7 min 30 sec, 7 min 42 sec, 8 min, 10 min and 15 min, respectively. All the profiles are compared with the InSb melt at 7 min profile to see the dissolution process clearly. The distance between 0 to 6 mm shows the initial GaSb seed position. The distance between 6 to 9 mm shows the initial InSb position and the distance between 9 to 15 mm shows the initial GaSb feed position. In Fig. 9 (a), the 7 min data show the Ga composition profile after InSb was melted. The length of InSb melt was redueed to 2 mm compared with the InSb solid length of 3 mm due to the density differenee between the solid and liquid of InSb. From the X-ray penetration method, the reduction of the volume change from solid to liquid was clearly seen. From the 7 min 30 sec data, it is obvious that GaSb seed and feed were started to dissolve into InSb melt. So, the Ga composition in the In-Ga-Sb solution was gradually increased due to solutal transport from GaSb seed and GaSb feed to the InSb melt, in other words In composition of the In-Ga-Sb solution was decreased as Ga incorporated in the solution.

After 7min 42 sec, only the seed interface was shifted towards the lower region as shown in Fig. 9 (b). On the other hand, feed interface was in the same position. It indicates that the dissolution of feed into InSb melt was suppressed and the dissolution of seed into InSb melt was enhanced. The reason is that the dissolved GaSb moved towards the upper region due to solutal convection since the density of liquidus GaSb (6.01 g/cm^3) was smaller than

that of liquidus InSb (6.32 g/cm^3). So, most of the GaSb components were accumulated at the feed interface which suppressed the further dissolution of GaSb feed into InSb melt. In other words it enhanced the dissolution of GaSb seed into InSb melt since the large amount of InSb existed at the lower region (near the seed-solution interface). From the 8 min data shown in Fig. 9 (c), Ga composition of the solution further increased since almost 2 mm of the GaSb seed was dissolved into the solution and the dissolved Ga solute transported to the feed/solution interface.Therefore, the Ga composition gradually decreased from the seed interface to the middle of the solution. At 10 min as shown in Fig. 9 (d), only a small amount of GaSb dissolved into solution. The Ga composition near the seed/solution interface was decreased and it was increased near the feed/solution interface. As can be seen from the Fig. 9 (e), the dissolution became slower and dissolved GaSb diffused to the feed/solution interface at 15 min. The results clearly demonstrated that the GaSb seed was dissolved faster than GaSb feed even though the GaSb feed temperature was higher than that of GaSb seed temperature. The X-ray images clearly indicate that gravity plays the major role during the dissolution of GaSb into the InSb melt.

IV. Conclusion

Microgravity studies on the dissolution and crystallization of $In_xGa_{1-x}Sb$ have been done having the sandwich combination of InSb and GaSb{111} as the starting material using the Chinese recoverable satellite. The same type of experiments were performed under 1G gravity condition for comparison. The shape of the solid/liquid interface and composition profiles in the solution were found to be significantly affected by gravity. The dissolution process of GaSb into InSb melt was observed by X-ray penetration method. GaSb (seed)/InSb/GaSb (feed) sandwich sample was used for the experiment. GaSb seed was dissolved faster than GaSb feed even though the GaSb feed temperature was higher than that of GaSb seed temperature. The dissolved GaSb moved to the upper region due to solutal convection since the liquid GaSb density was smaller than that of liquid InSb. So, most of the GaSb components were accumulated at the feed interface which suppressed the further dissolution of GaSb feed. Therefore, the dissolution of GaSb seed into InSb melt was enhanced. These results clearly indicate that gravity affects solute transport and dissolution and growth processes of alloy semiconductor bulk crystals.

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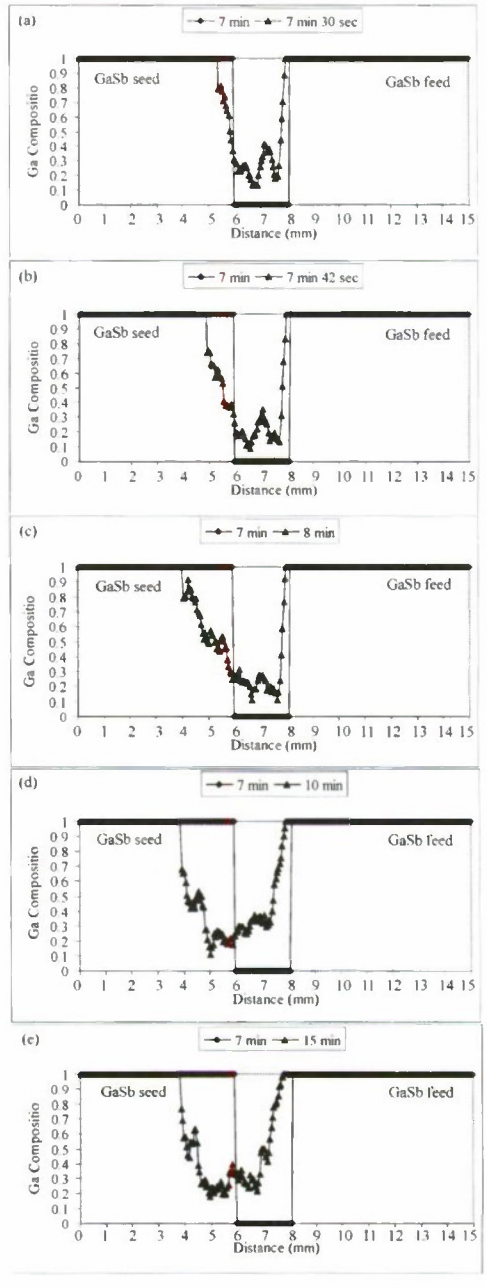

Fig. 9 Ga composition profile of the In-Ga-Sb solution at (a) 7 min 30 sec, (b) 7 min 42 sec, (c) 8 min, (d) 10 min and (e) 15 min, respectively.

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GROWTH OF LARGE PLATY InGaAs CRYSTALS AND FABRICATION OF SEMICONDUCTOR LASER DIODES

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Abstract—**We have succeeded in increasing size of $In_xGa_{1-x}As$ (x: 0.1 – 0.13) platy single crystals to 30 $\times$30 mm^2 in surface area for mass production of laser diodes. Key points are to suppress convection in a melt and to keep constant temperature gradient for obtaining homogeneous crystals. Grown crystals have enough quality as substrates for 1.3 μm laser diodes. Fabricated laser diodes on these substrates were evaluated by measuring lasing characteristics at various temperatures and by measuring bit error rate for transmission through a single mode fiber up to 20 km. Lasers showed high temperature stability and error free transmission and showed the merit of ternary substrates.**

Keywords-component; bulk crystal growth, ternary, a new growth method, substrates for 1.3μm laser diodes, laser fabrication

I. INTRODCTION

$In_{1-x}Ga_xAs$ ternary substrates are promising for laser diodes with λ = 1.3μm because a large conduction band offset between the well and barrier layer is possible and output power decrease at high temperatures is much less than those on InP substrates. We have invented a new crystal growth method named the travelling liquidus-zone (TLZ) method and succeeded in growing compositionally uniform $In_{1-x}Ga_xAs$ ternary single crystals(1-3). Here, we report large platy $In_{0.13}Ga_{0.87}As$ crystal growth by the TLZ method, fabrication of laser diodes on ternary substrates, and results of laser performance tests.

II. CRYSTAL GROWTH AND CHARACTERRIZATION

Crystal growth method used in the present experiments is a TLZ method. The TLZ method is a kind of zone melting method but is different from a conventional zone melting method in melting source materials at relatively low temperature gradient(1-3). Crystal growth procedures are as follows. A GaAs seed, an InAs zone former, and a GaAs feed were cut into plates with 2 mm thickness and were inserted into a boron nitride crucible with a rectangular bore and were sealed in vacuum in a quartz ampoule and then heated in a gradient heating furnace. The principle of the TLZ method is shown in Fig. 1. In the TLZ method, low melting point InAs is melted at temperatures around 1000℃ and forms a liquidus zone by dissolving the adjacent solid GaAs. Narrow liquidus zone is formed when small amount of InAs is used. Due to low temperature gradient in a zone (about 10 K/cm) as well as narrowness of the zone, solute in the zone is almost saturated and it can be called liquidus-zone. This liquidus-zone travels to the lower In concentration side spontaneously due to interdiffusion between InAs and GaAs (to the higher temperature side). When the ampoule is translated towards the lower temperature side in accordance with the freezing rate, homogeneous crystals are grown because the freezing interface is kept at a fixed temperature. We increased dimensions of grown crystals from 10 $\times$50 to 30 $\times$50 in surface area with keeping the thickness to 2mm in platy shape. Growth direction was <100>. Compositional profiles of grown crystals were measured by EPMA (Electron Probe Micro-Analyzer) and crystal quality was evaluated by measuring X-ray rocking curves.

III. LASER FABRICATION

Laser diodes were fabricated on $In_{0.13}Ga_{0.87}As$ substrates using the usual laser process. Strained MQWs having the combination of $In_{0.12}Ga_{0.88}As$ and $In_{0.38}Ga_{0.62}As$ were prepared by metal-organic vapor phase epitaxy (MOVPE)(4). The stripe mesa type laser was fabricated by chemical etching. Bottom ridge width of 1.7 μm enabled single mode lasing. Laser performance was evaluated by measuring lasing characteristics and 20 km transmission test through a single mode fiber.

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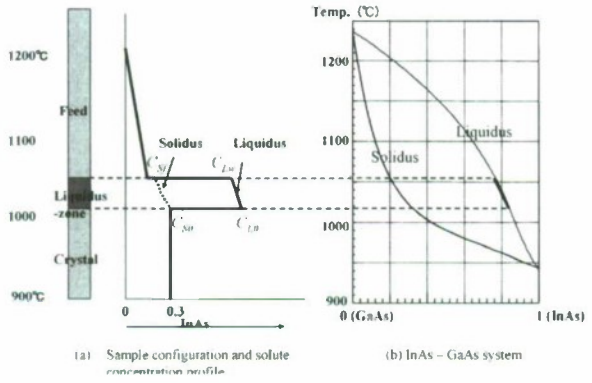
IV. RESULTS AND DISCUSSION

Figure 2 shows an example of a grown crystal by the TLZ method. A roughly polished surface of the crystal shows that single crystal region extends more than 30×30 mm^2. Compositional uniformity is excellent as shown in Fig. 3: InAs mole fraction 0.13 ± 0.01 is achieved in this single crystal region and good crystallinity with the full width at half maximum (FWHM) of less than 0.04° in X-ray rocking curves is obtained (Fig. 4). Such excellent compositional uniformity and crystal quality owes to matching of sample translation rate and freezing rate and resulting in a fixed freezing interface position relative to heater segments. In this point of view, constant temperature gradient during translation of a sample was important for obtaining compositional uniformity. This is because the freezing rate is determined by the temperature gradient and variation of temperature gradient causes variation of freezing rate and compositional fluctuation. Such increase in surface area in platy crystals without deteriorating crystal quality also shows that convection in a melt is suppressed by the limitation of melt thickness (2 mm) and enlargement in melt width did not cause convection. If convection occurs in a melt, local inhomogeneity will be resulted due to stirring of a melt by convection. Good homogeneity shows that convection was suppressed in the course of crystal growth.

In the TLZ method, spontaneous growth rate is determined by temperature gradient because concentration gradient is determined by temperature gradient in a saturated melt zone; higher temperature gradient gave higher growth rate. Higher growth rate is favorable for mass production, but higher growth rate caused constitutional supercooling in a melt. This is because solute concentration profile deviated from linear gradient and formed a concave profile at higher temperature gradient. Too low temperature gradient is not mass productive. were applied. Temperature stability was important for high



(a) Sample configuration and solute concentration profile (b) InAs – GaAs system

Fig. 1 Principle of the TLZ method with referring to the InAs-GaAs system.

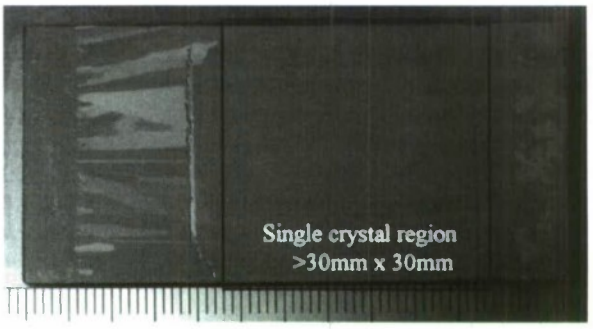


Fig. 2 Roughly polished surface of a TLZ-grown platy crystal.

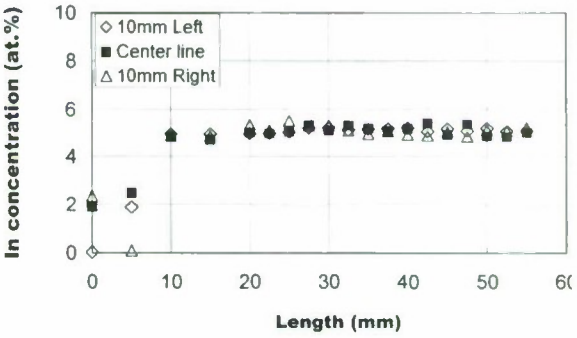


Fig.3 In concentration profiles along the growth axis.

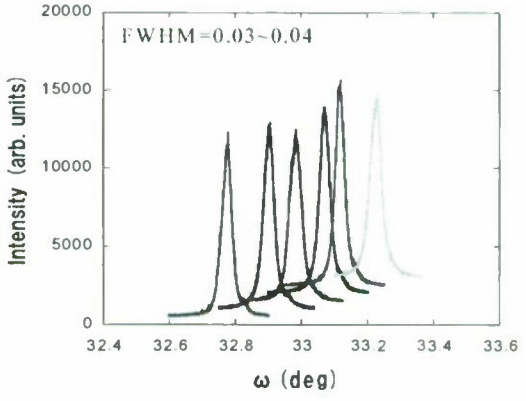


Fig. 4. X-ray rocking curves at various positions. Figures show the length from the left end of the crystal in Fig. 2.

quality crystal growth. If air flow around the growth ampoule occurs, it causes temperature fluctuation. In the experiments, ampoules were sandwiched by glass wool in a furnace tube and air flow around ampoules was prevented.

Figure 5 shows cross sectional view of a fabricated laser diode. The stripe mesa was in the [011] direction, forming a reverse mesa. The active region was consisted of four $In_{0.38}Ga_{0.62}As$ wells and five $In_{0.12}Ga_{0.88}As$ barriers. Single mode operation was realized by reducing a ridge width to 1.7 μm. Selective wet etching was utilized for such narrow ridge formation.

Figure 6 shows continuous wave (CW) lasing characteristics at various temperatures. It is shown that high output power is obtained even at 150℃. Such high temperature stability in output power is made possible on ternary $In_{1-x}Ga_xAs$ substrate for the first time. A 10-Gbps direct modulation and transmission tests through a single mode fiber up to 20 km were successfully performed using a fabricated laser diode as shown in Fig. 7. Bit error rate (BER) for back-to-back configuration after 20km transmission was less than 10^{-7} at -18 dBm. The result shows feasibility of the fabricated laser diode.

V SUMMARY

We succeeded in growing device quality $In_xGa_{1-x}As$ platy crystals with x~0.13 and single crystal region larger than 30 × 30 mm^2 by the TLZ method. High quality of thus prepared ternaly crystals as substrates was proved by fabrication of high performance laser diodes with λ = 1.3 μm.

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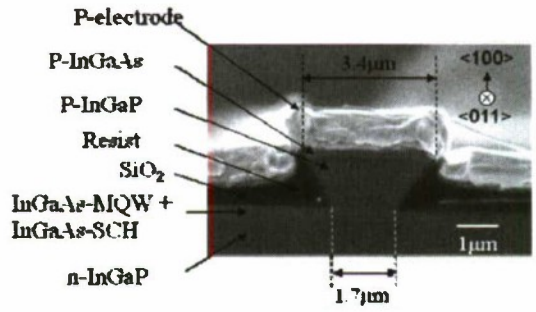

Fig. 5. Cross sectional view of a fabricated laser diode.

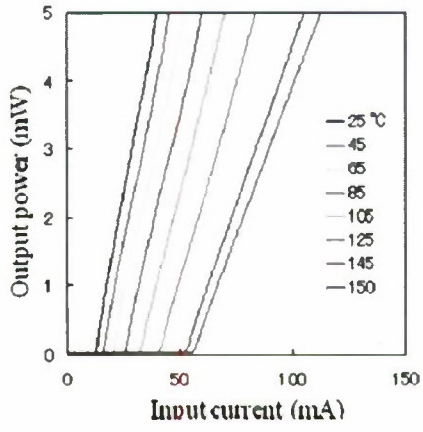

Fig. 6 Lasing characteristics at various temperatures.

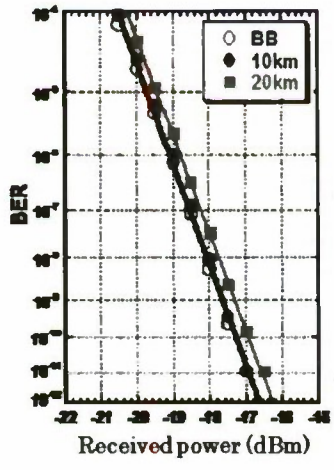

Fig. 7. Bit error rate at various detector sensitivity.

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OPTICAL AND ELECTRICAL PROPERTIES OF InP POROUS STRUCTURES FORMED ON P-N SUBSTRATES

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We demonstrated to form InP porous structures on n-type epitaxial layers grown on p-type (001) substrates. The high-density array of straight pores with 150nm diameter and 5000nm depth was formed by the electrochemical anodization process, where the pore depth could be controlled by the anodization time in the n-type layer. The present p-n InP porous structures show the low optical reflectance in UV-, visible- and near-infrared region. The current transport properties clearly show the rectifying behavior. These features are very promising for practical application to high-efficiency photo-sensitive devices.

I. Introduction

Recently, intensive research efforts have been made on the high-density formation of semiconductor nanostructures for applications such as photonic crystals, quantum and optoelectronic devices. Mainstream approaches to forming semiconductor nanostructures have used conventional methods such as the lithography, dry-etching, or crystal growth processes. However, there are severe limitations in downsizing and increasing the density of nanostructures because most processes involved require lithography in defining the size and position of the nanostructures.

One possible alternative technique is the electrochemical process, which can form various semiconductor nanostructures in self-assembled fashion. The most well-known application of the electrochemical process is the anodic formation of porous structures. The direct formation of porous structures onto semiconductor substrates has been reported first on Si [1-3] and later on III-V semiconductor materials such as GaAs,[4,5] GaP,[6,7] InP,[8-10] GaN,[11,12] and SiC.[13]

In this paper, we report the electrochemical formation of porous nanostructures on n-type InP epitaxial layers grown on p-type InP substrates. As for the anodic pore formation on n-InP substrates, we have already reported that structural features such as pore diameter and depth can be controlled by anodic conditions.[14-17] In this paper, the pore formation of p-n substrates was first optimized. The surface reflectance and electronic transport properties were investigated for the application to the optoelectronic devices.

II. Experimental

The setup of the electrochemical process used in this study is shown in Fig. 1(a). The electrochemical process was performed using a standard cell with three electrodes, i.e., an InP working electrode, a Pt counter electrode and a saturated calomel electrode (SCE) as reference. The sample structures are schematically shown in Fig. 1(b). n-type InP epitaxial layers (N_D = 8×10^{17} cm^{-3}) grown on p-type InP (001) substrates (N_A = 5×10^{18} cm^{-3}) were used for the porous formation. For current supply, a AuZn ohmic contact was made on the back surface of the InP substrate using conventional metal evaporation and annealing. Anodization was carried out to form a porous structure in HCl-based electrolyte. In this study, the anodic bias V_s was set at 6 V with reference to the SCE, as shown in Fig. 1(a). All the experiments were performed in the dark at room

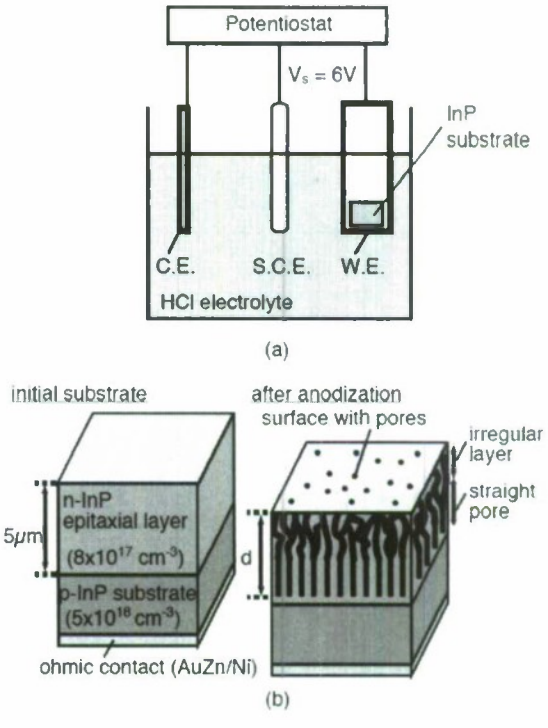

Fig.1 (a) Experimental setup and (b) schematic illustrations of InP porous structures.

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temperature.

To clarify the tunability of the pore depth, InP porous structures were formed by changing the anodization time. After that, the surface reflectance properties and the current transport properties were investigated on the sample having a different pore depth, *d*. The reflectance measurements were performed using an ultra-violet (UV)-visible spectrometer (UV-1700, Shimadzu) in the back reflection configuration. The wavelength range of the light source was set from 205 to 1100 nm corresponding to the photon energy range from 1.12 to 6.0 eV. The I-V measurements were performed using a parameter analyzer (HP4156A, Agilent technologies) and compared with the planar p-n junction diodes.

III. Results and Discussion

A. Anodization of p-n InP substrates

Figure 2(a) shows the anodic currents measured during the anodization of p-n InP substrates illustrated in Fig. 1(b). As shown in Fig. 2(a), the anodic currents gradually decreased with the anodization time, and then the currents steeply increased at around 6s. This kind of behavior has not been seen in the case of the porous formation on n+InP substrates.[15]

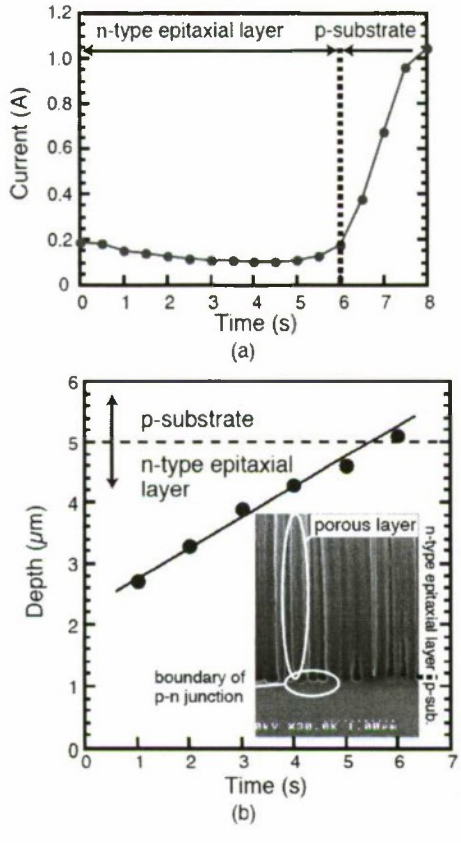

Fig.2 (a) Correlation between anodic currents and anodization time during pore formation. (b) Pore depth measured as a function of anodization time.

Figure 2(b) plots the pore depth as a function of the anodization time during the pore formation in the n-type layer. The inset of Fig. 2(b) shows the cross-sectional SEM images of the InP porous structure anodized for 6s. It was found that the straight pores with a diameter of about 150 nm reached at the boundary of p-n junction. As shown in the inset of Fig. 2(b), the pore diameter was slightly enlarged in the p-type region as compared with the top n-type region. This is probably because large amounts of positive holes are supplied in p-type substrate and used for the anodic etching. The steeply increased currents obtained in Fig. 2(a) are very consistent with this result showing that the pore depth reached to the p-type substrate at around 6s.

Experimental data measured from the SEM observation showed linear relation between the depth and time, as shown in Fig. 2(b). From these results, it was found that the depth of the regular pore can be controlled by the anodization time in the n-type epitaxial layer. However, the experimental data did not pass through the origin and it was 2μm larger than the theoretical values calculated by the electric charge based on Faraday's law. This result suggests that the irregular top layer with smaller pore diameter was formed at very beginning of the pore formation, as schematically shown in Fig. 1(b).

B. Optical and electrical properties

In order to clarify the feasibility for the device application, the basic optical and electrical properties on the p-n InP porous structures were investigated. We first investigated the effects of the irregular top layer on the surface reflectance by comparing two kinds of porous samples with and without the irregular top layers. The sample without the irregular top layer was prepared by the wet chemical etching or the photo-electrochemical (PEC) etching[17] after the anodic pore formation.

Figure 3 shows the surface reflectance of three kinds of samples measured in UV-, visible- and near infrared- region. First, the reflectance of the planar sample was higher than 30% over the measurement range. Typical peaks were observed around 880 nm (1.4 eV), 410 nm (3.0 eV), and 450 nm (5.0 eV), which were attributed to the interband transitions.[18] The reflectance obtained from the porous sample with the irregular top layer was 5–10% lower than that obtained from the reference sample. As plotted in Fig. 3, the spectral features of the InP bulk remained in the porous sample, showing that crystal quality was maintained beyond a certain level after the pore formation.

On the other hand, the reflectance of the porous sample without the irregular top layer drastically decreased as compared with the other two samples. The reflectance was lower than 1.0% over the measurement range. In the visible light range of 380–750 nm, which corresponds to the energy range of 1.6–3.2 eV, the reflectance dropped to below 0.3%, which was much lower than the values of 5–10% reported for Si porous structures.[19] These results indicate that the optical view of the porous surface was reflected in the difference of the microscopic surface morphology. As shown in the inset of Fig. 3, it was found that the porous sample without the irregular top layer has

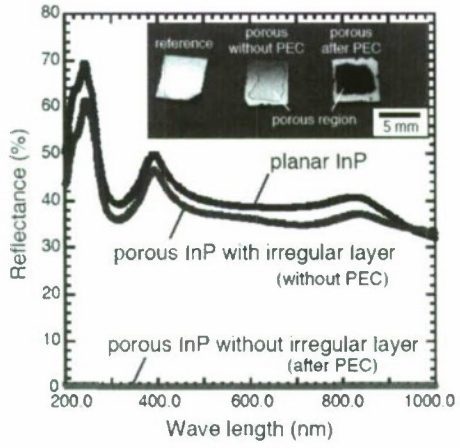

Fig.3 Surface reflectance spectra measured as a function of wavelength of incident light.

diffuse optical reflection resulting in a black surface.

Then, we investigated the photovoltaic properties of the porous p-n diodes by focusing on the difference of the microscopic surface morphology. For the electrical measurements, GeAuNi ohmic contacts were formed on the top surface of p-n InP porous samples. Figures 4(a) and (b) show the current-voltage (*I-V*) curves measured on two kinds of diodes under the dark and light conditions. The obtained data shows clear rectifying behavior for both diodes, indicating that InP nanowalls between each pore show proper conductivity and carrier mobility. However, the photo-currents obtained on the porous samples varied greatly between the samples with different surface morphology. We found the photovoltaic response was remarkably improved after the removal of the irregular top layer around the top electrode. These results indicate that the photovoltaic response strongly depends on the structural properties in reflection to the surface optical reflectance. The results obtained here are promising for the application to the practical devices based on the InP porous structures.

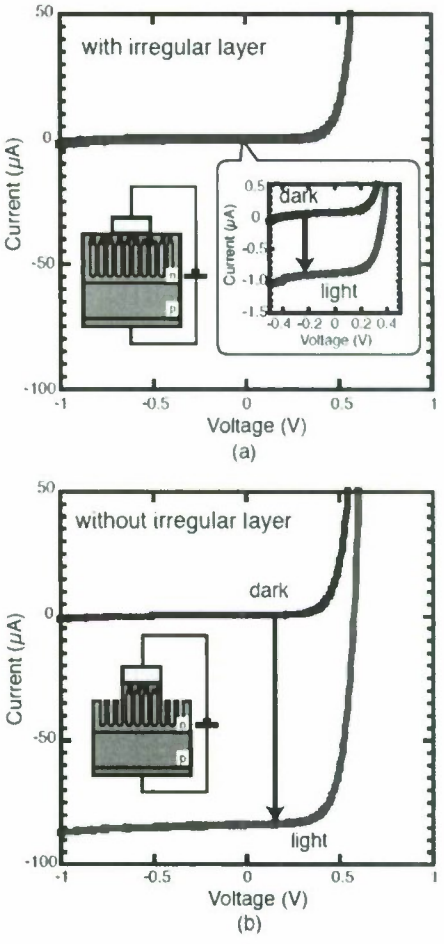

Fig.4 *I-V* characteristics of p-n InP porous structure; (a) with irregular layer and (b) without irregular layer around the top electrode.

IV. Conclusion

In this study, an electrochemical anodization process was applied to the fabrication of a porous nanostructure for n-type InP epitaxial layers grown on p-type InP(001) substrates. The straight pores were formed in the n-type layer, where the pore depth could be controlled by the anodization time. The surface reflectance properties were reflected in the difference of the microscopic surface morphology, showing that the porous sample without the irregular top layer has diffuse optical reflection. As for the current transport properties, the p-n porous structure shows clear rectifying behavior and large photocurrents for the sample without the irregular top layer. The results obtained here are promising for practical application to high-efficiency photo-sensitive devices, such as solar cells and photodetectors with built-in anti-reflective (AR) functions.

Acknowledgment

The work reported here was supported in part by a Grant-in-Aid for young scientists (A) - 21686028 from the Japanese Ministry of Education, Culture, Sports, Science, and Technology (MEXT) and by a Grant-in-Aid for Challenging Exploratory Research - 21656078, from the Japan Society for the Promotion of Science (JSPS).

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PREPARATION OF N-TYPE InP SUBSTRATES BY VERTICAL BOAT GROWTH

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Abstract

N-type InP substrates have been manufactured using Vertical Boat (VB) Technique. In this paper, we will report improvement in etch-pit density (EPD) distribution for 2-inch S-doped, 2-inch -Sn-doped and 4-inch S-doped VB InP substrates in comparison to VCZ (SEI's proprietary Vapor pressure controlled Czochralski) InP substrates. EPD of 2-inch S-doped VB InP substrate is lower than SEI's standard EPD specification 500 cm^{-2} from seed-end to tail-end. Etch-pit densities are drastically reduced compared to those of VCZ with carrier concentration ranging from 3E18 cm^{-3} to 4E18 cm^{-3}. The VB technique enables a decrease in slip-line defects of S-doped InP with low carrier concentration range. Average lot size of 2-inch S-doped VB InP is almost 1.4 times larger than that of VCZ InP. 4-inch S-doped VB substrates and 2-inch Sn-doped VB substrates are also manufactured using the VB technique.

I. INTRODUCTION

N-type InP substrates have been widely used for photonic devices such as photodetecters, laser diodes and light emitting diodes. For photonic device application, low dislocation densities are required. SEI has already developed a new Vertical Boat (VB) technique which improves microscopic and macroscopic uniformity of 4-inch Fe-doped semi-insulating InP substrates (1-4). 3-inch Fe-doped InP was also grown by the VB method in mass production scale following to the volume production of 4-inch Fe-doped InP crystals. These Fe-doped VB InP substrates have lower dislocation density (EPD) compared to conventional VCZ (SEI's proprietary Vapor pressure controlled Czochralski (5-6)) substrates. For example, a standard EPD specification of the 3-inch Fe-doped VB InP is 5000cm^{-2} while that of VCZ InP is 10000cm^{-2}, however, process capability index of EPD at seed-end wafer is 1.4 for 3-inch Fe-doped VB whereas that of Fe-doped VCZ is less than 1. The VB technique is suitable for preparing semi-insulating Fe-doped InP substrates which have stable quality in mass production scale.

We had tried to prepare high quality n-type InP crystals by the VB technique, however, VB growth of 2-inch S-doped InP had been difficult because a twinning problem was serious for low dislocation density 2-inch S-doped InP. In this paper, we report success in developing n-type InP such as 2-inch S-doped, 2-inch Sn-doped and 4-inch S-doped InP crystal growth by VB technique.

II. EXPERIMENTAL

Figure 1 shows VB technique for InP single crystal growth in SEI (1-4). The VB technique used in the study was fundamentally the same as that used in VB growth of semi-insulating InP crystals. InP crystals were grown in high-pressure stainless steel puller under a 4-5 MPa nitrogen gas atmosphere. Heat shield and heaters were modified for 2-inch InP growth to prevent twinning caused by temperature fluctuation.

Dislocation density is one of the most important properties of InP substrates. Dislocation density can be quantified by measuring the etch-pit density. (100) substrates were polished and etched in a H_3PO_4-HBr solution for etch-pit density measurement. Distribution of etch-pit density was measured by an automatic counting system (7).

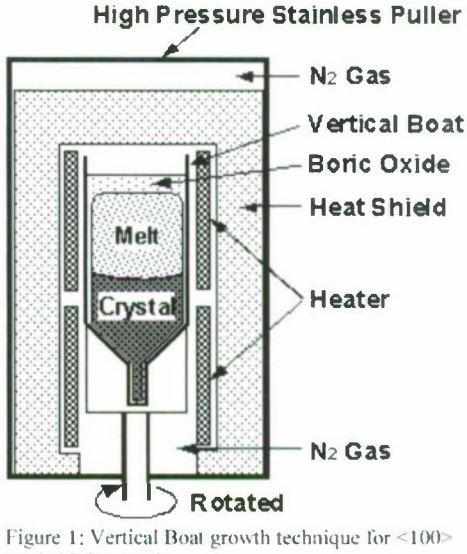

Figure 1: Vertical Boat growth technique for <100> seeded InP crystals.

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III. RESULTS

(A) 2-inch S-doped InP

Figure 2 shows 2-inch S-doped InP crystals manufactured by (a)VCZ and (b)VB. The round-shaped VB crystal is much longer than the VCZ crystal. Length of crystal within standard specification is limited by EPD and/or carrier concentration. Figure 3 shows comparison of carrier concentration dependence on normalized crystal length in VCZ and VB. The VB crystal is longer than the VCZ crystal with the same carrier concentration range (3-8 E18 cm^{-3}).

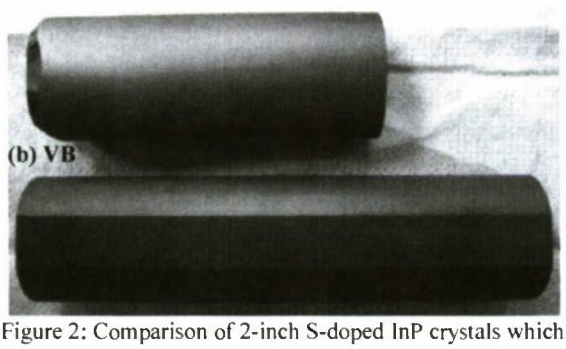

Figure 2: Comparison of 2-inch S-doped InP crystals which were round-shaped. (a) VCZ crystal (b) VB crystal.

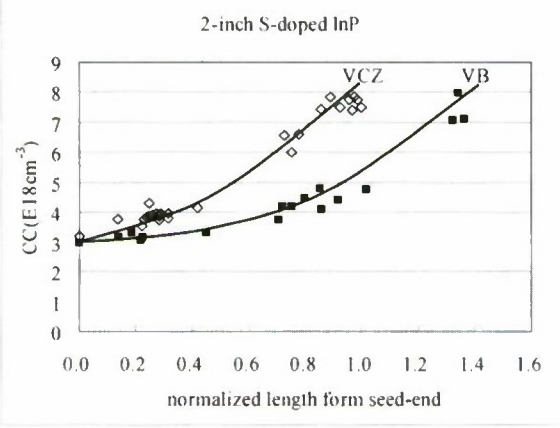

Figure 3: Comparison of carrier concentration between VCZ crystals and VB crystals as a function of normalized crystal length. VB crystals are 1.4 times longer than VCZ crystals under the same carrier concentration range.

Figure 4 shows comparison of EPD distribution of 2-inch S-doped InP. A Peripheral region of a VCZ wafer(a) has a higher EPD value than that of a VB wafer at the same carrier concentration. Figure 5 shows dependence of EPD on carrier concentration in VCZ and VB substrates. Average EPD values of VCZ substrates are higher than standard EPD spec 500 cm^{-2} in low carrier concentration region of less than 4E18 cm^{-3}. Slip lines are the reason why the VCZ wafer has higher EPD values and larger EPD deviations. On the other hand, EPD values of VB substrates are lower than standard specification 500 cm^{-2} in carrier-concentration from 3E18 cm^{-3} to 8E18 cm^{-3}. EPD becomes extremely low where carrier concentration is higher than 5E18 cm^{-3} for both VCZ and VB substrates.

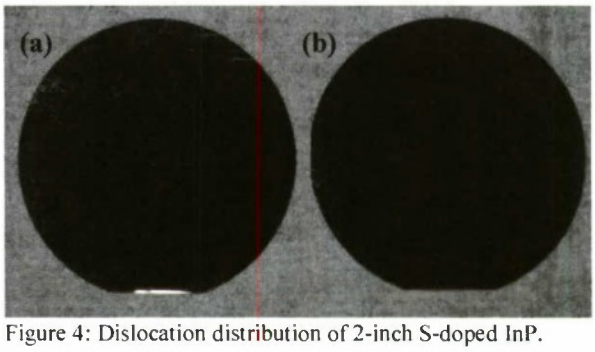

Figure 4: Dislocation distribution of 2-inch S-doped InP.
(a) VCZ-InP; EPD average is 390 cm^{-2}, carrier concentration 4E18 cm^{-3}, (b) VB-InP; EPD average is 220 cm^{-2}, carrier concentration 4E18 cm^{-3}

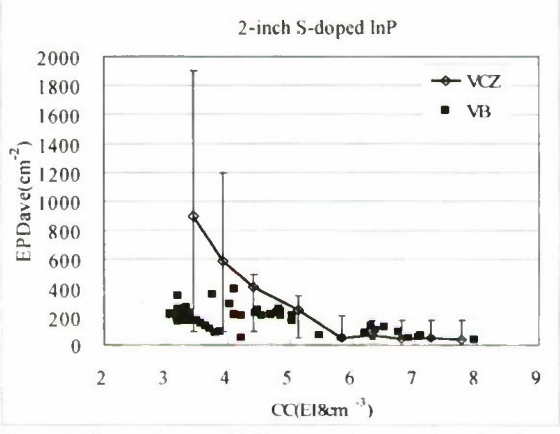

Figure 5: Dependence of EPDon carrier concentration in 2-inch S-doped VCZ and VB crystals.

(B) 2-inch Sn-doped InP

Twinning problem is not serious in case of Sn-doped InP because solidification hardening effect by Sn is smaller than that of S. This indicates that growth of low dislocation density Sn-doped InP is difficult. We have optimized growth condition to decrease EPD in our VB technique for Sn-doped InP. Figure 6 shows dislocation distribution of 2-inch Sn-doped VB InP in comparison with that of VCZ InP. Etch-pit density is drastically decreased by the VB technique. Slip lines are not observed in the VB wafer; Cellar dislocation structure at cent-

ral part of the wafer is not observed in the VB InP. Figure 7 shows effect of carrier concentration on EPD in 2-inch Sn-doped InP. EPD values are not sensitive to carrier concentration in case of Sn-doped InP at least within a standard carrier concentration specification. The VB technique enables decrease EPD of 2-inch Sn-doped InP.

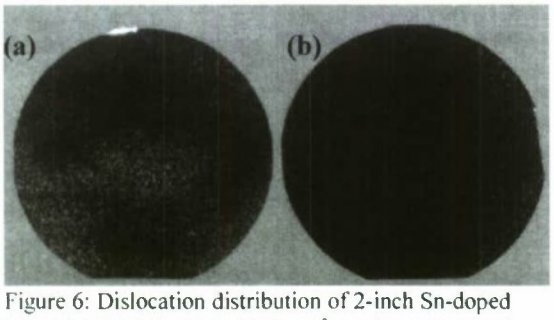

Figure 6: Dislocation distribution of 2-inch Sn-doped InP. (a) VCZ-InP; EPD 4400 cm^{-2}, carrier concentration 1.6E18cm^{-3}. (b) VB-InP; EPD 460 cm^{-2}, carrier concentration 1E18 cm^{-3}.

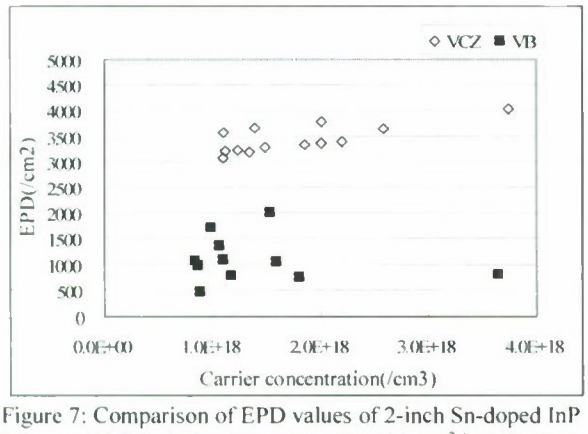

Figure 7: Comparison of EPD values of 2-inch Sn-doped InP between VCZ and VB. EPD average 5000 cm^{-2} is a mass production specification for VCZ. VB growth of 2-inch Sn-doped is R&D stage, therefore, mass production spec is not determined yet.

(C) 4-inch S-doped InP

Figure 8 shows an EPD map of 4-inch S-doped VB crystal where carrier concentration is at 4.5E18 cm^{-3}. 4-inch S-doped VCZ crystals under mass production stage was not available in SEI, therefore, we compared the 4-inch VB crystals with S-doped 3-inch VCZ crystals. Figure 9 shows an example of EPD dependence on carrier concentration for 3-inch S-doped VCZ InP and 4-inch S-doped VB InP. Etch-pit density of the VB substrate in low carrier concentration region is much smaller than that of 3-inch S-doped VCZ crystals. EPD of 4-inch S-doped crystal gradually decreases with increasing carrier concentration, however, the EPD decease rate of 4-inch VB crystal is much moderate compared to that of VCZ crystals. EPD values of 4-inch S-doped VCZ InP as R&D stage [6] was reported; a seed-end EPD was 9000 cm^{-2} at carrier concentration 3.4E18 cm^{-3} and a tail-end EPD was 400 cm^{-2} at carrier concentration 6.4E18 cm^{-2}. Advantage of VB technique is obvious for mass production of 4-inch S-doped InP. Mass production of 4-inch S-doped VB is possible under a specification where EPD is less than 5000 cm^{-2} and carrier concentration between 2E18 cm^{-3} and 8E18 cm^{-3}.

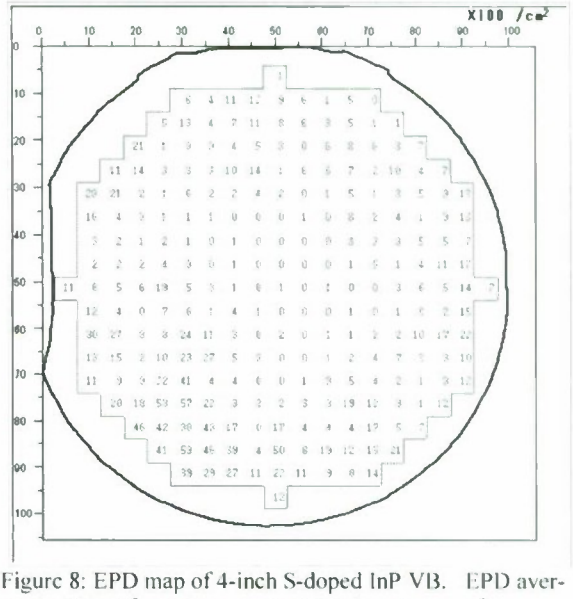

Figure 8: EPD map of 4-inch S-doped InP VB. EPD average is 840 cm^{-2}, carrier concentration is 4.5E18 cm^{-3}.

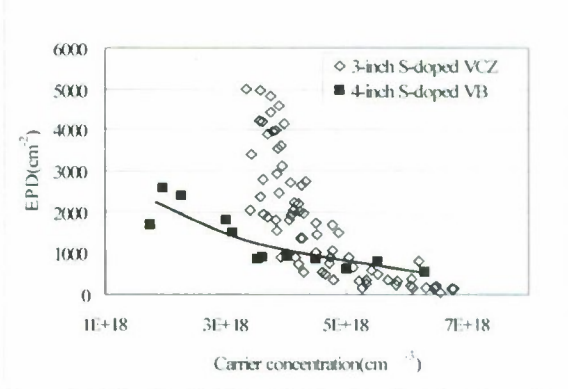

Figure 9: EPD distribution of a 4-inch S-doped VB crystal compared with 3-inch S-doped VCZ. EPD in low carrier concentration region is much smaller than that of 3-inch S-doped VCZ. Mass production of 4-inch-S doped InP is possible.

IV. Conclusions

N-type InP substrates were prepared by VB technique. Average etch-pit density of N-type VB substrates were lower than those of VCZ substrates. Etch-pit density of 2-inch S-doped VB substrates in low carrier concentration (3E18 - 4E18 cm^{-3}) was much smaller than that of VCZ substrate; Slip lines were prevented by the VB technique. This improves product yield and lot size of 2-inch S-doped InP crystals. Etch-pit density of 2-inch Sn-doped VB substrates were almost a half compared to that of VCZ substrates in any carrier concentration. Etch-pit densities of 4-inch S-doped VB substrates in low carrier concentration range (2E18 to 4E18 cm^{-3}) were much smaller than that of 3-inch S-doped VCZ substrate. VB technique enables preparing larger diameter substrate with lower seed-end carrier concentration.

SEI has started to apply the VB technique to preparing 3-inch S-doped, 2-inch Fe-doped and 2-inch Zn-doped crystals. SEI Standard specifications of InP substrates are summarized in Tables 1 and 2. SEI would like to shift growth technique from VCZ to VB which will improve quality.

Table 1: Standard specification of N-type InP in SEI

Dopant	Carrier concentration(cm^{-3})	Size (inch)	VCZ EPD (cm^{-2})	VB EPD (cm^{-2})
S	2~8E18	4	R&D	≦5000
S	3~8E18	3	≦5000	≦5000
S	3~8E18	2	≦500	≦500
Sn	1~4 E18	2	≦5000	(≦3000)

Table 2: Standard specification of semi-insulating InP in SEI

Dopant	Resistivity (Ωcm)	Size (inch)	VCZ EPD (cm^{-2})	VB EPD (cm^{-2})
Fe	>1E7	4	≦10000	≦5000
Fe	>1E7	3	≦10000	≦5000
Fe	>1E7	2	≦5000	R&D

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FABRICATION OF III-V SEMICONDCTOR NANOWIRES BY SA-MOVPE AND THEIR APPLICATIONS TO PHOTONIC AND PHOTOVOLTAIC DEVICES

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We fabricated various kinds of III-V semiconductor nanowires and eore-shell nanowires using selective area metalorganic vapor phase epitaxy (SA-MOVPE) on (111) oriented substrates, sueh as GaAs, GaAs/AlGaAs, InP, InP/InAs/InP on III-V substrates, and InAs and GaAs on Si. As for device applications, we fabrieated GaAs/GaAsP core-shell nanowire photo-exeited lasers, and InP eore-shell pn junetion solar eells. I will also introduee III-V semieonductor nanowires grown on Si (111) substrates .

Recently, semieonduetor nanowires have attraeted much attention for their physieal properties and possible applications. These nanowires have small diameters on the nanometer seale, and they are expeeted to exhibit the 1D transport property and the 2D quantum confinement effeet. We can also eontrol the type of eonduetion of semieonduetor nanowires and fabricate pn junctions and heterostructures, which are important for applieations of low-dimensional deviees. Most semieonduetor nanowires have been fabrieated by using Au or In metal droplets as catalysts under vapor-liquid-solid (VLS) mechanisms.

Reeently, a new fabrieation proeess of nanowire growth using solid eatalyst partieles under the vapor-solid-solid (VSS) meehanism has been reporte. Oxide-assisted growth also been proposed without metal eatalyst. This means that nanowire growth modes and their mcchanisms are still a controversial topic.

We fabricated semieonduetor nanowires by using seleetive-area metalorganic vapor phase epitaxy (SA-MOVPE)(1-3). GaAs nanowires were grown with six-fold symmetrie {-110} vertieal sidewall faeets on the opening area of partially masked GaAs (111)B substrate. A seanning eleetron microscope (SEM) image of a typieal high-density GaAs nanowire array with a 100-nm diameter grown by SA-MOVPE is shown in Fig. 1. GaAs nanowires with excellent size and shape uniformities were obtained. We eonfirmed that the nanowire formation attributes of {-110} sidewall facets vertical with respeet to (111)B substrates appeared during growth. Therefore these nanowires grown by SA-MOVPE attributes of neither an oxide-assisted nor eatalytic growth, in whieh the growth of nanowires should have no relationship to the orientation of the substrates.

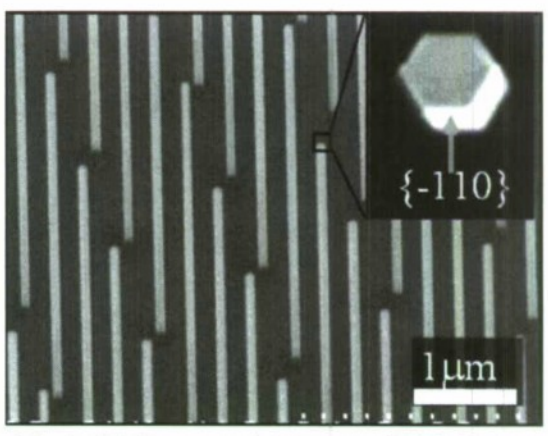

Fig. 1. Bird's-eye and top view of SEM images of typical GaAs nanowires on GaAs (111)B substrate.

We also suceessfully fabricated single GaAs/GaAsP coaxial eore-shell nanowires nad applied to lasers. Highly uniform

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GaAs/GaAsP coaxial nanowires were prepared. Photoluminescence spectra from a single nanowire indicate that the obtained heterostructures can produce near-infrared (NIR) lasing under pulsed light excitation at 4.2K as shown in fig.2. Lasing wavelength is 816nm. The end facets of a single nanowire form natural mirror surface to crcate an axial cavity, which realizes resonance and give stimulated emission. This study is a considerable advance towards the realization of nanowire-based NIR light sources (4).

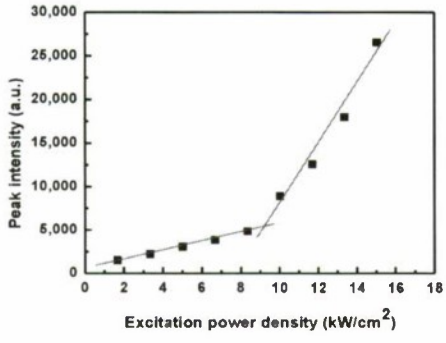

Fig. 2 PL intensity vs excitation power intensity

A periodically aligned dense core–shell InP nanowire array was fabricated and used in photovoltaic device applications. We fabricated a photovoltaic device using the core–shell pn junction InP nanowire array covering a 7.0x2.6mm^2 area on the p-type lnP (111)A substrate. The structure of the SiO_2 mask pattern and growth conditions were the same as already reported (5). After nanowire growth, the space between nanowires was filled with CYCLOTENE resin (Dow Chemical) as a transparent electrical insulator, by spin coating. The overlaid excess resin was removed by reactive ion etching, exposing the tips of nanowires. A transparent indium tin oxide (ITO) film electrode was then sputtered onto the nanowire array at room temperature, followed by heat treatment at 400°C to reduce the resistance of ITO. A comb-shaped Ag electrode was also formed on the transparent ITO electrodc. The backside electrode of the substrate was formed by alloying Au–Zn. Figure 3 shows an actual solar cell devices obtained by scanning electron microscope (SEM) observation after substrate cleavage. The chip size was 1x1 cm^2 and the active nanowire area consisted of three 2.0x2.6mm^2 segments. The active-arca contained the space bctween nanowires, but excluded domains that were covered with the Ag electrode connecting the whole array.

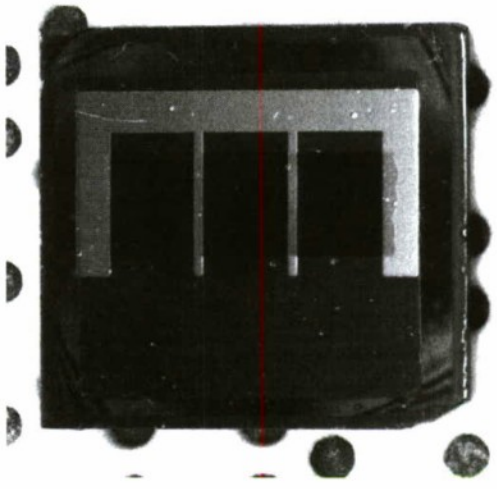

Fig. 3 SEM image of a core–shell pn junction nanowire photovoltaic device

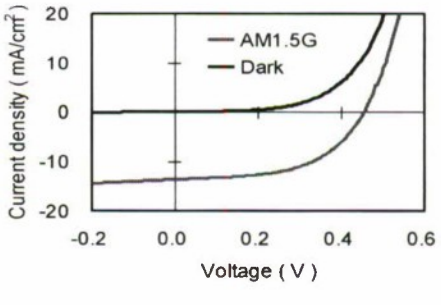

Fig.4 Measured I–V characteristics of a solar cell fabricated with core–shell pn junction nanowires on a p-type InP(111)A substrate.

Photovoltaic performance was measured under Air Mass 1.5 Global

(AM1.5G) illumination, where the radiation intensity was ealibrated using a referenee cell module just before measurement. Figure 4 shows current–voltage (I–V) eharaeteristies of the InP nanowire array cell. The device exhibited 0.43V of open eireuit voltage (V_{OC}), 13.72 mA/em^2 of short eireuit eurrent (J_{SC}), and a fill faetor (FF) of 0.57 for 3.37% overall efficieney.

Finally, we demonstrate vertieal InAs and GaAs nanowire growth on Si (111) substrates by modifying initial Si (111) surfaee. Si has no polar nature, that is, both (111) oriented surface can exist in terms of III-V nanowire growth. Therefore, vertieal and tilted nanowires ean grow on the same surfaee. To control the growth direction to vertical direction, we used the specific growth sequence.

First, the substrate was eooled down to 400 °C after thermal eleaning. Next, AsH3 was supplied at this temperature to form the As-ineorporated Si^{3+} surfaee. Moreover, As atoms and In atoms should be effieiently supplied to the Si(111) surfaee to form a (111)B-oriented surface just before InAs nanowire growth. We therefore introdueed the flow-rate modulated epitaxy (FME) mode at 400 °C. FME is a method of alternating group III- or V-preeursor supply during MOVPE. The purpose of the FME is to enhanee the termination of In atoms to As ineorporated Si^{3+} and bare Si^{1+} surfaees beeause the In termination to a bare Si^{1+} surface also forms (111)B-like surface. We also introduced an H_2 interval between the TMIn and AsH_3 supply to enhance the exehanges of supplied materials. The FME mode was carried out for 20 cycles at 400 °C. After the FME mode, typieal InAs nanowire growth was earried out at 540 °C. As a result, almost of all nanowires were eontrolled to vertieal direetion. The results suggest that a (111)B-oriented surfaee was effectively formed on Si(111) by using this growth sequenee (6). Using similar growth sequence, we also successfully eontrol the growth direetion of GaAs nanowires on Si(111) substrates as shown in Fig.5 (7). Cross-seetional transmission eleetron mieroseope images showed that misfit disloeation with local strains was aeeommodated in InAs/Si interface, while no misfit dislocation was observed in GaAs/Si interfaee.

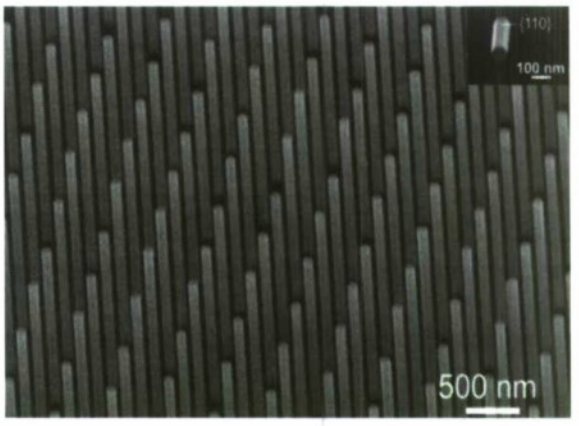

Fig. 5 SEM image of GaAs nanowires on Si (111) substrate.

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Epitaxial III-V Planar Nanowires: Self-aligned, High-mobility and Transfer-Printable

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Abstract: We present planar, self-aligned, twin-free, and high-mobility GaAs semiconductor nanowires epitaxially grown on (100) and (110) GaAs substrates. In addition, such planar nanowires are directly transfer-printable and compatible with existing processing technology and integratable with various devices.

I. Introduction

Semiconductor nanowires (NWs) have been extensively studied in the past decade for applications in nanoelectronics and nanophotonics. III-V semiconductor NWs are of particular interest because of their direct band gap, high carrier mobility, and ability to form versatile heterojunctions. It has been shown that the lowest free energy surface is (111)B and thus NWs grown on (111)B substrates are vertically aligned and perpendicular to the substrate. However, the out-of-plane NW geometry remains a challenge for wafer-scale integration with current planar processing technology. In addition, the abundance of twin-plane defects, widely reported in <111> III-V NWs, has been found to degrade the optical and electronic properties.

When (100) substrates are used, NWs still mostly grow in the <111> direction, which is 35.3° angled from the substrate. Other growth directions have been observed sporadically during NW growth, presumably due to modification of free energy by strain, surface tension etc., and such NWs have reportedly shown fewer twinning defects (1).

Here we report the controlled large area growth of self-aligned, twin-free, high mobility and transfer-printable, planar <110> nanowires on (100) substrates using metalorganic chemical vapor deposition (MOCVD). Structural and electrical characterization will be presented and discussed.

The sensitivity of nanowire morphology to growth conditions (e.g. pressure, temperature, growth surface preparation) has been exploited in vapor phase growth systems to produce novel nanostructures that extend the nanowire application space (e.g. Tian et al. (2)). We show that by introducing low level p-type vapor phase precursors into the growth chamber during nanowire growth, we show it is possible to induce periodic notching in planar GaAs nanowires. Furthermore, we demonstrate that by choosing the crystal orientation of the growth substrate, the growth direction of planar nanowires can be engineered. Importantly, we have determined a route towards completely unidirectional growth of planar III-V nanowires through growth on a (110) substrate.

II. Experimental Details

The controlled growth of III-V planar NWs on semi-insulating (SI) GaAs (100) (on-axis and misoriented) and (110) substrates was achieved using Au nanoparticle catalyst (5 – 300 nm in diameter) in an atmospheric MOCVD reactor. Before growth, substrates were annealed at 620°C in the MOCVD reactor. Trimethylgallium (TMGa), trimethylindium (TMIn), and arsine (AsH_3) were used as Ga, In and As precursors respectively. Intentional doping was obtained with disilane ($Si2H_6$) for n-type, and carbon (CBr_4) and Zn (DEZn) for p-type. Nanowires were grown with an excess flow of AsH_3 (>100 V/III ratio) unless otherwise mentioned. The effect of growth temperature, pressure, and substrate on the nanowire orientation and alignment were studied systematically. Detailed nanowire MESFET device fabrication, measurement and modeling have been reported (3,4).

III. Results and Discussion

A. GaAs nanowire growth on (100) substrates

A systematic growth study shows that the morphology and yield of the GaAs planar NWs can be controlled primarily through the growth temperature under our growth conditions. Shown in Figure 1 are SEM images of NWs grown in different orientations. The growth of the planar NWs self-aligned laterally along either the [1-10] or [-110] crystal direction with uniform diameters (Figure 1a and 1b) can be achieved at growth temperatures of 470±10°C with yield as high as 96%. For temperatures outside of this window, angled <111> (Figure 1c) and tapered <110> planar NWs (Figure 1d) form at lower and higher temperatures, respectively. The growth rate of the tapered NWs is noticeably slower than the planar NWs grown at the lower temperature of 460°C. The triangular shape and reduced growth rate are

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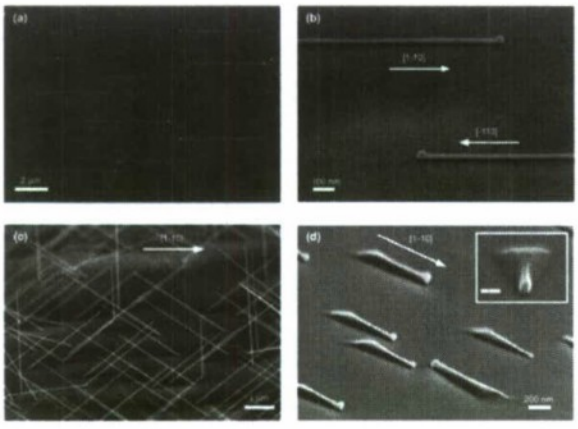

Figure 1. GaAs nanowires grown on GaAs (100) substrate. The nanowire orientation and morphology is controlled primarily through modulation of the growth temperature. (a-d) SEM images show (a,b) well-aligned <110> planar nanowires grown at 475°C, (c) predominantly <111> nanowires grown at 420°C, and (d) tapered, well-aligned <110> planar nanowires grown at 520°C. Inset of (d) shows high-magnification SEM image of tapered planar nanowire as viewed along its growth axis (scale bar is 100 nm). Sample is not tilted in (a) and tilted 85° in (b-d). Adapted from (3).

attributed to temperature-enhanced NW sidewall growth that reduces the amount of material (presumably Ga) available to the Au seed particle, thereby limiting the VLS growth rate along the axial direction of the NW.

In addition to temperature, the growth orientation can also be perturbed by impurity incorporation (discussed later), and total reactor pressure parameters. A low yield of planar NWs is observed (~10%) when grown at a total reactor pressure of 100 mbar.

B. TEM results

Transmission electron microscope (TEM) analysis was carried out on a JEOL 2010 microscope equipped with a LaB_6 filament. Shown in Figure 2a is a TEM image of a planar GaAs NW terminated by an Au particle. Figure 2b shows a high resolution TEM image obtained from the interface between the GaAs planar nanowire and the (100) GaAs substrate as viewed along a <110> direction that is perpendicular to the nanowire growth direction. The GaAs nanowire clearly extends the substrate zinc-blende lattice epitaxially and the growth direction is along the <110> direction. No apparent misfit dislocations are found. Remarkably, the planar NWs are essentially free of twinning defects, in contrast to the widely reported <111> III-V NWs.

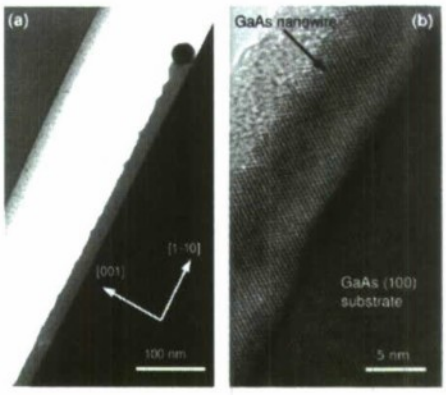

Figure 2. TEM images of planar GaAs nanowires. (a) Low-magnification TEM image of <110> planar nanowire without stacking faults. (b) High-resolution TEM image of the nanowire-substrate interface. Adapted from (3).

C. GaAs planar nanowire MESFET

A long channel planar GaAs nanowire metal-semiconductor field effect transistor (MESFET) device has been used to characterize the NW carrier concentration and mobility. Shown in Figure 3 are the NW-MESFET geometry and output and transfer characteristics for an intentionally silicon doped GaAs NW channel that is ~ 200 nm wide in trapezoidal

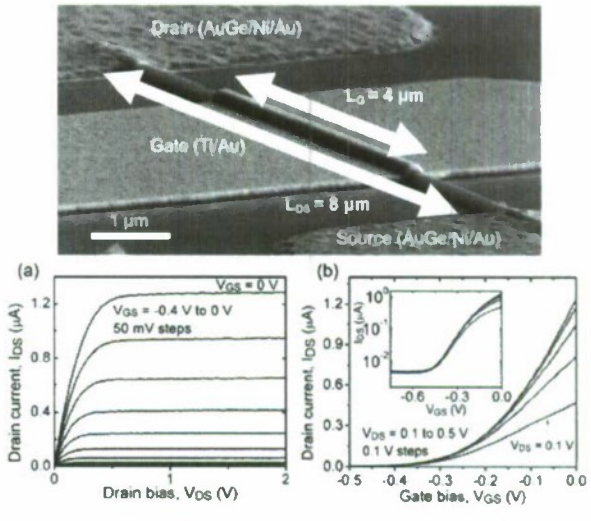

Figure 3. Top: SEM image of a fully-processed GaAs NW MESFET with dimensions labeled. Bottom: electrical characterization (a) I_{DS}-V_{DS} family of curves for V_{GS} = -0.4 to 0 V with 50 mV steps. (b) I_{DS}-V_{GS} transfer characteristics for V_{DS} = 0.1 to 0.5 V with 100 mV steps. Inset shows I_{DS}-V_{GS} plot on a semilog scale. Adapted from (4).

cross-section. A doping concentration of $N_d = 2.3 \cdot 10^{17}$ cm^{-3} was extracted from experimental data by numerically solving Poisson's equation for the NW channel transverse cross section at the threshold bias conditions. To obtain the low-field electron mobility, we modified a standard long-channel electrical model to include the effect of source/drain resistances and a trapezoidal channel cross section. An electron mobility of $\mu_n = 4120$ $cm^2/V \cdot s$ was extracted from experimental I_{DS}-V_{DS} measurements and provided excellent fit between the model and experimental results. This value corresponds closely to reported values of electron mobility in bulk GaAs with a doping density of $N_d \sim 2 \cdot 10^{17}$ cm^{-3} and thus indicates the excellent material quality of planar GaAs NWs.

D. Transfer-printed planar nanowires

For a number of applications it is desirable to transfer NWs from their growth substrate onto another substrate. For example, III-V materials can be integrated with Si without the issues related to epitaxial growth of mismatched materials. NWs can also be deposited onto polymer or paper for use in applications requiring mechanically compliant substrates.

For planar NWs, the unique growth properties of self-alignment along the <110> direction and epitaxial growth on the substrate can be exploited to transfer-print the NWs to other substrates while maintaining position and alignment. By growing the planar nanowires on a sacrificial layer that can be subsequently removed to release the epitaxially attached planar NWs, we demonstrate the possibility of parallel transfer of the highly-aligned planar NWs to a foreign substrate. Shown in Figure 4 are examples of picking up the released NWs using PDMS stamp and transfer to a Si substrate while maintaining both the original NW registration and alignment.

E. P-type doping in planar nanowires

We have found that CBr_4 or DEZn (carbon and zinc precursors respectively) under certain vapor phase concentrations (approximately 0.01% of DEZn/TMGa or CBr_4/AsH_3) induce periodic notching along the growth axis of planar GaAs nanowires with a period that is proportional to the Au seed diameter and a delayed incorporation depending on dopant type (Figure 5).

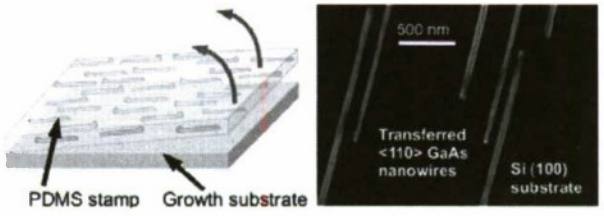

Figure 4. Schematic of removal of planar NWs with PDMS stamp and subsequent transfer-printing to silicon substrate (right). Adapted from (3).

Preliminary transmission electron microscopy analysis show the notching is associated with periodic twinning of the crystal; similar to what was reported for vertical III-V nanowires grown on (111)B substrates (5). Such periodic twinning has been predicted to alter the electronic band structure and produce miniband effects that have device applications.

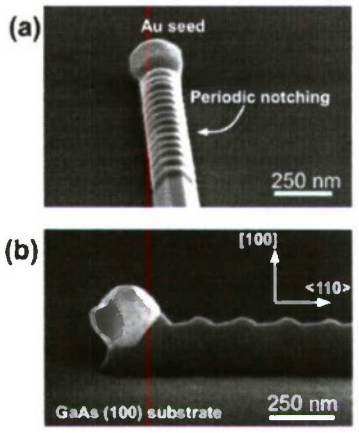

Figure 5. Scanning electron microscope images (SEM) of planar <110> GaAs nanowires exhibiting periodic notching induced by a low concentration of CBr_4 added to the growth reactor.

F. Nanowire growth on other substrate orientations

We have investigated growth of planar nanowires on substrates with various different crystal orientations. Described above, planar <110> GaAs nanowires grown on GaAs (100) substrates grow in one of two antiparallel directions; however, self-alignment along a single <110> direction is, from an integratability point of view, more desirable. When planar nanowires are grown on (100) substrates with a 10° offcut towards [1-10], the planar nanowires orient in nonparallel directions yet still remain in the plane of the substrate (Figure 4a). This suggests that, through simple modification of the growth substrate

crystal orientation, the planar nanowire growth direction can be "tuned".

Indeed, when grown on (110) substrates, planar nanowires exhibit unidirectional growth along a single crystal direction (Figure 4b). The demonstration of unidirectional growth is an important step towards position and alignment controlled integrated nanowire devices in a form compatible with conventional planar processing technology.

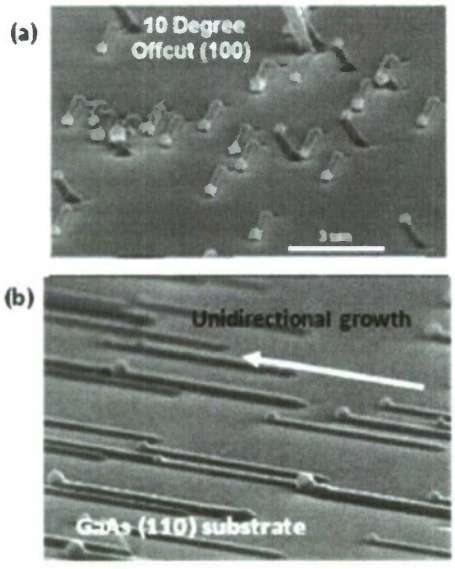

Figure 6. The planar nanowire growth direction can be engineered through choice of growth substrate. (a) Planar nanowires grown on a GaAs (100) with a 10° offcut towards [1-10] (b) Unidirectional <100> planar GaAs nanowires grown on the GaAs (110) substrate.

G. Extension of planar nanowire growth to other III-V materials

The planar growth mode demonstrated above for GaAs NWs can also be extended to InAs NWs. When grown at 380°C (Figure 7) on a (100) GaAs substrate, a small percentage (~30%) of NWs are planar and self-aligned with each other. On closer inspection (inset of Figure 7) the planar InAs NWs appear to have grown laterally and epitaxially on the (100) GaAs surface. The InAs planar NWs on the (100) GaAs surface may have misfit dislocations because of the large lattice mismatch between InAs and GaAs. Further work will be necessary to determine the structural characteristics of the InAs planar NWs.

Similar planar InAs NW growth was observed on InAs (100) substrates at the 380°C growth temperature; interestingly the yield of InAs planar NWs was significantly higher on the (100) GaAs substrate. This may not be surprising considering the low surface energy between Au and GaAs which may promote planar growth preferentially on the (100) GaAs surface.

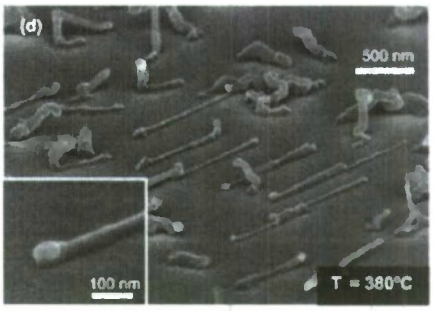

Figure 7. Planar InAs NWs grown on a (100) GaAs substrate. Inset shows close view of InAs planar NW.

IV. Conclusion

We have reported a novel type of GaAs NW that is planar, which makes it compatible and highly integrable with existing processing technology and photonic and electronic device designs. The planar GaAs nanowires are of high quality without twinning defects and can be transfer-printed to arbitrary substrates. Growth morphology and direction can be controlled through modification of growth parameters, introduction of impurities, or choice of growth substrate orientation. We demonstrated aligned, unidirectional growth of planar nanowires on (110) substrates; a major step towards achieving a highly integrated nanoelectronic or nanophotonic system based on self-assembled materials.

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RF-MBE growth of InN/InGaN MQW structures by DERI and their characterization

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Abstract

We successfully demonstrated fabrication of InN/InGaN multi quantum well (MQW) structures using a novel growth method by utilizing In droplet elimination by radical-beam irradiation (DERI). First, InGaN was grown under a metal rich (Ga+In>N*) condition by supplying Ga, In and N* simultaneously, in which In was preferentially swept out to the surface. Second, the swept In on the InGaN was transformed to InN by N* irradiation. Thus, by simply repeating these processes InN/InGaN MQW structure was fabricated. Three types of MQW structures were fabricated with different In beam flux. We found that thickness of In well layer can be controlled by changing the In beam flux during InGaN growth whereas In composition and thickness of the InGaN barrier layers were constant.

I. Introduction

InN and related alloys are very attractive materials for infrared optical devices because of their narrow direct band gap among III-nitride semiconductors. However, realization of such devices has been hindered by the intrinsic difficulties in the growth of these materials although several results on the fabrication of InN/InGaN multi quantum well (MQW) structure were reported [1-3]. Recently, for the growth of InN and InGaN by radio-frequency plasma-assisted molecular beam epitaxy (RF-MBE), we have developed a novel growth method by utilizing In droplet elimination by radical-beam irradiation (DERI) [4, 5]. Using the DERI method we are able to obtain high quality InN reproducibly. Furthermore, we have also found that for InGaN growth using the DERI method, preferential incorporation of Ga over In on an InGaN growing surface was occurred when the samples are grown under a metal-rich conditions. In this work, we will propose a new fabrication method of InN/InGaN MQW structures using the DERI method. We also discuss about

II. Experimental

The samples used in this study were grown in a conventional MBE system (EpiQuest RC2100NR) equipped with conventional effusion cells for In and Ga. An active nitrogen radical beam is generated by a commercialized nitrogen plasma source (SVT Associates 6.03). The structures of InN and InGaN can be monitored in situ by reflection high-energy electron diffraction (RHEED) analysis using kSA400 (k-Space Associates). A GaN template grown on (0001) sapphire by metalorganic vapor phase epitaxy (MOVPE) was used as a substrate in this study. After the deposition of GaN and InN intermediate layers on the GaN template, 10 periods of InN/InGaN MQW structures were fabricated using the DERI method. Figure 1 shows growth process of InN/InGaN structure by DERI. This

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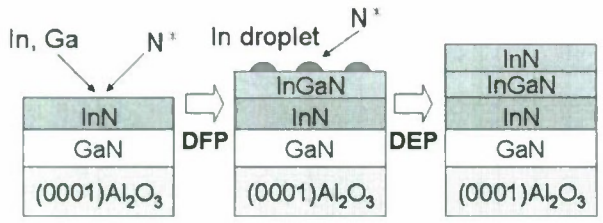

Figure 1 Growth process of InN/InGaN structure using the DERI method, which is composed of droplet formation process (DFP) and droplet elimination process (DEP).

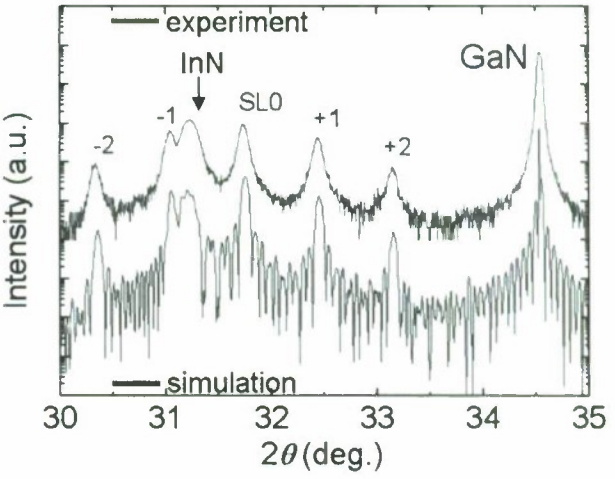

Figure 2 XRD ω–2θ profiles of the InN/InGaN MQW structure grown with an In beam flux of 1.32×10^{-6} Torr. Red and blue profiles show experimental and simulated data, respectively.

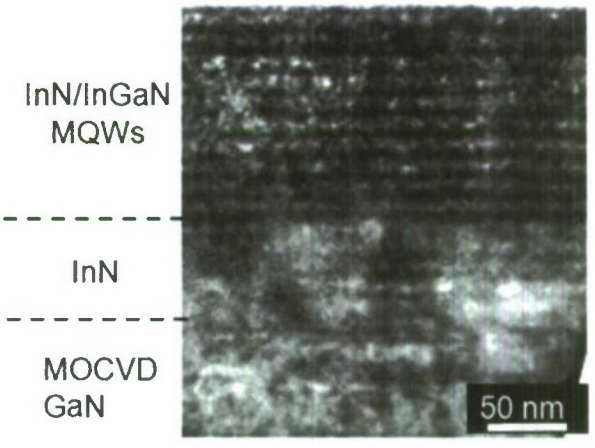

Figure 3 Cross-sectional TEM image of the InN/InGaN MQW structure fabricated by repeating the DERI method.

method was composed of droplet formation process (DFP) and droplet elimination process (DEP). In the DFP, InGaN was grown under a metal rich (Ga+In>N*) condition by supplying Ga, In and N* simultaneously. In this process, Ga was preferentially incorporated into the growing InGaN layer, and whereas In was preferentially swept out to the surface [5]. This swept In on the InGaN underlayer was transformed to InN by the DEP using N* irradiation. Thus, by simply repeating the DFP and DEP, InN/InGaN MQW structure was fabricated. During the MQW growth, rf power and Ga beam flux were kept constant at 100 W and 1.7×10^{-7} Torr, respectively. Three types of MQW structures were fabricated with different In beam flux; 0.90×10^{-6}, 1.08×10^{-6}, 1.32×10^{-6} Torr.

The structural characterization of the InN/InGaN MQW structures grown by DERI were carried out by X-ray diffraction (XRD, PANalytical X'Pert MRD) and transmission electron microscopy (TEM, JEOL2010).

III. Results and Discussion

Figure 2 shows ω–2θ XRD profiles of the InN/InGaN MQW structure grown with an In beam flux of 1.32×10^{-6} Torr. Addition to the peaks from GaN and InN, 1st and 2nd order of satellite peaks originated from MQW periodic structure were clearly observed. From all of samples, satellite peaks as shown in Fig. 2 were confirmed. Figure 3 shows a cross-sectional TEM image of the InN/InGaN MQW structure fabricated in this study. Periodic contrast of the InN/InGaN MQW structure was observed. These results confirmed that the InN/InGaN MQW structures with abrupt hetero-interfaces and

Table I In composition and thicknesses of $In_xGa_{1-x}N$ barrier and InN well of InN/InGaN MQW fabricated with different In beam flux.

	In beam flux ($\times 10^{-6}$ Torr)		
	1.32	1.08	0.90
In composition: x	0.73	0.73	0.72
InGaN barrier thickness (nm)	6.5	6.6	6.6
InN well thickness (nm)	6.6	4.0	2.1

uniform layer thickness were successfully fabricated by the DERI method.

The In composition and layer thicknesses of InN well and InGaN barrier layers of MQW structures were determined by fitting experimental XRD profiles with simulation. Table I summarizes structural parameters of the InN/InGaN MQW structures fabricated with three different In beam flux. In composition and layer thickness of InGaN barrier layers for three types of InN/InGaN MQW structures are about 072 and 6.6 nm, respectively. It is found that the In composition and thickness of the InGaN barrier layers were almost constant although In beam flux was varied during the growth of InGaN barrier. On the other hand, the thickness of InN well layer was increased with the increase of In beam flux. These results indicate that the relationship between the supplied Ga and N* during InGaN growth determines the In composition and thickness of the InGaN barrier layer. Figure 4 shows dependence of the In beam flux on the thickness of InN well layer. The thickness of InN well layer was linearly increased with the increase of In beam flux. It is considered that when we increased the In beam flux, the amount of In droplet which was swept out to the surface during InGaN growth increased. Therefore, the thickness of InN well layer which was transformed from In droplet during the DEP process increased.

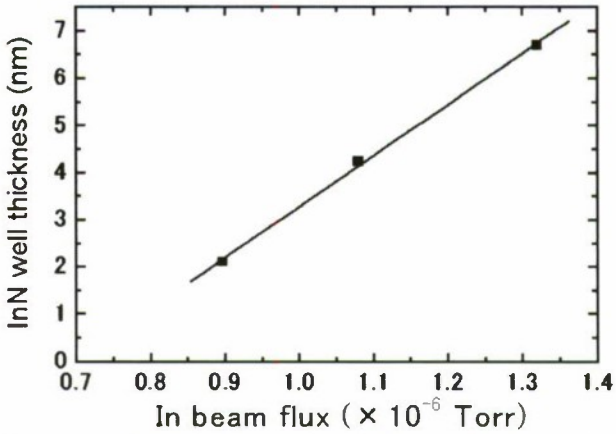

Figure 4 Dependence of the In beam flux on the thickness of InN well layer.

IV. Summary

We have successfully demonstrated that the DERI method for InN growth by RF-MBE is also very useful for the fabrication of InN/InGaN MQW structures. The thickness of the InN well layer increased by increasing the In beam flux, whereas the In composition and thickness of InGaN barrier layer remained the same. These results are successfully explained by taking the growth process during the DERI method into account.

Acknowledgments

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SELECTIVE AREA GROWTH OF III-V SEMICONDUCTORS: FROM FUNDAMENTAL ASPECTS TO DEVICE STRUCTURES

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Abstract

Fundamental aspects in the selective-area metal-organic vapor-phase epitaxy (MOVPE) of III-V semiconductors are presented in this paper, with an emphasis on the role of vapor-phase diffusion of a group-III precursor, which plays the dominant role for substantial modulation of an effective bandgap around wider (>100 μm) masks and is a characteristic of MOVPE that is operated close to atmospheric pressure. A single parameter, D/k_s (vapor-phase mass diffusivity / surface incorporation rate coefficient), determines modulation of both thickness and composition of a layer. The value of D/k_s can be regarded as an effective lateral diffusion length of a group-III precursor, and the value of k_s can be decoupled from D/k_s, providing insight to surface reaction kinetics of MOVPE. Coupling with reactor-scale distributions provides unique basis for the discussion of comprehensive reaction mechanism. The values of k_s will be presented for basic materials composing InGaAsP system. Luminescence wavelength from multiple quantum wells (MQWs) around a given mask pattern can be simulated precisely based on a simple diffusion/reaction model and it is applicable to monolithic integration of devices using selective-area growth of InGaAsP-related materials. The same framework can be applied to III-nitride materials, and k_s values for GaN growth have been obtained. Visible luminescence from InGaN/GaN MQWs on a patterned GaN template was red-shifted according to the mask width, for which only the thickness modulation of the InGaN wells has been suggested to be the governing mechanism.

I. Introduction

Single-chip integration of functional components of a semiconductor optical device necessitates multiple bandgaps on a chip. As shown in Table 1, among other integration techniques, selective-area metal-organic vapor-phase epitaxy (MOVPE) of III-V semiconductors, in which a substrate surface is partially covered with amorphous masks such as SiO_2, is beneficial in that it requires only a single growth and thus high-yield of device fabrication can be expected (1-4). In the selective-area growth, group-III precursors are incident on the surface, and are re-distributed in the lateral direction around the masks, leading to in-plane modulation of thickness. When more than two group-III elements are involved, enhancement of growth rate around a mask is different among group-III vapor-phase precursors, leading to modulation of group-III atomic content as well as thickness. Band edge of such a compound layer is also modulated accordingly. Compared with bulk layers, luminescence wavelength from

Table. 1 Comparison of process methods for lateral integration of multiple bandgaps that is necessary for integrated optical devices.

Method	Pros	Cons
Selective-area growth (SAG) Growth on a patterned surface	■A single growth for a number of bandgaps → High yield	■Non-abrupt lateral interface ■Carriers at waveguide → large loss
Etching and re-growth Grow a single bandgap →Remove unnecessary part → Repetition	■Abrupt lateral interface ■Carriers only at active region → low loss	■Re-growth is not straight-forward ■Increased number of process steps → Low yield
Hybrid approach Bonding different epi-layers on a platform	■Free from sophisticated growth ■Freedom of design	■Severe alignment ■Bonding necessary

Mechanism	Diffusion length	Modulation
Vapor-phase diffusion	~100 μm	Large
Surface diffusion	~μm	Small

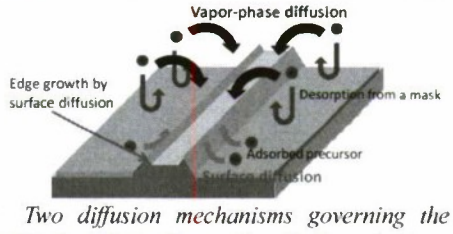

Fig. 1 Two diffusion mechanisms governing the local growth rate in patterned growth. In the selective growth area, surface diffusion is effective only within several μm from the mask edge, while vapor-phase diffusion exhibits its effect within an order of 100 μm from the mask edge.

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multiple quantum wells (MQWs) exhibits larger modulation around a maskdue to tailored quantum confinement effect with the modulated thickness of the well layers.

In order to obtain substantial modulation of the wavelength, a mask width should be more than 100 μm. In such a situation, balance between vapor-phase diffusion and surface incorporation of a group-III precursor determines local enhancement of growth rate around a mask, as shown in Fig. 1. Dominant contribution of the vapor-phase diffusion is a characteristic of MOVPE that is operated close to the atmospheric pressure.

Even in a selective area growth in which surface diffusion seems dominant, vapor-phase diffusion is also coupled and determines the enhancement of growth rate. Figure 2 shows an example. Pyramidal shape of a GaN island is formed by surface diffusion of a Ga precursor among different crystal planes. The size of the mask surrounding the island, when it is larger than a diffusion length of the precursor on the mask (typically ~10 μm), determines the amount of the precursor accumulated in the vapor phase and leads to larger growth rate in the vicinity of a wider mask *via the vapor-phase diffusion.* We can, therefore, conclude that modeling and control of vapor-phase diffusion is essential for the selective-area growth to be genuinely applicable to monolithic integration of semiconductor optical devices.

II. Modeling of vapor-phase diffusion process

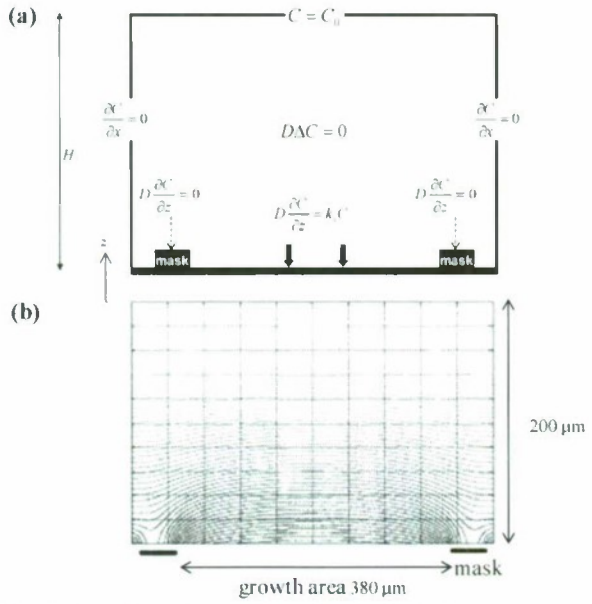

Fig. 3 (a) A mathematical model to obtain the concentration profile of a group-III precursor that governs a growth-rate profile in the selective growth area.
(b) An example of concentration contours of a group-III precursor in the vicinity of the selective growth area. The precursor diffuses in the perpendicular direction to the contours, resulting in lateral transport from above the mask to the selective growth area.

Figure 3 (a) depicts the governing equation and the boundary conditions for obtaining the concentration of a group-III precursor in the vicinity of the masks (5). An example of a calculated concentration field is shown in Fig. 3 (b). A height of the simulation area *H* should be sufficiently large so that there is no effect of *H* on the calculated concentration gradient. In other words, lateral re-distribution of the precursor occurs within a distance *H* from the surface, and *H* is normally much smaller than the thickness of a concentration boundary layer on the surface which is often discussed regarding a reactor-scale concentration field.

A single parameter, D/k_s (vapor-phase mass diffusivity / surface incorporation rate coefficient), determines a profile of growth rate enhancement, which is proportional to the concentration adjacent to the surface. D/k_s has a unit of length and can be regarded as an effective lateral diffusion length of a group-III precursor in the vapor phase. We should note that *D* is inversely proportional to a reactor pressure and is strong-

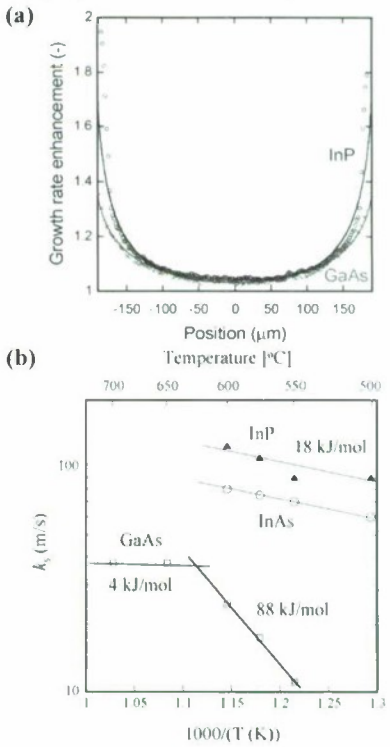

Fig. 4 (a) Typical parabolic growth-rate enhancement (GRE) profiles in a selective growth area for InP (open squares) and GaAs (crosses) at 10 kPa total pressure and 600°C growth temperature. The solid lines are calculated using D/k_s as a single fitting parameter. In the vicinity of masks, growth rate of InP deviates from the theoretical line due to existence of "rabbit's ear" which is formed as a result of preferential appearance of crystallographic planes.
(b) Arrhenius plot of k_s values (surface incorporation rate coefficients of a precursor) which are roughly proportional to the probability of a group-III precursor to be incorporated to the surface upon collision to the surface.

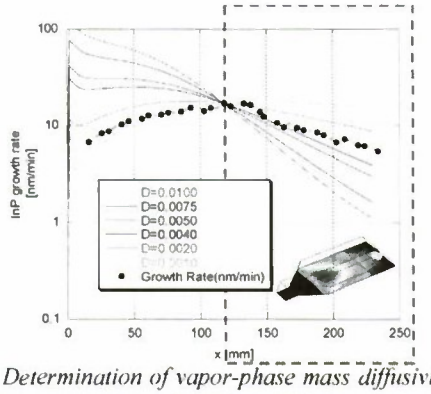

Fig. 5 Determination of vapor-phase mass diffusivity D of an indium precursor, probably $(CH_3)In$, in the actual MOVPE environment. The growth rate profile of InP in the flow direction is governed by the diffusion of CH_3In from the vapor phase to the InP surface, at the downstream part of the reactor (X>120 mm). Since the rate of vapor-phase diffusion is a function of D, the most probable value of D can be determined as the value that yields the best agreement of the simulated growth rate profile with the experimental data.

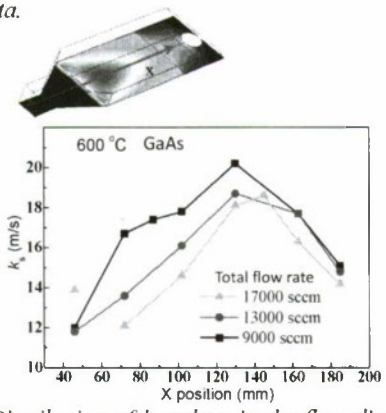

Fig. 6 Distribution of k_s values in the flow direction of a horizontal MOVPE reactor.

ly affected by the kind of carrier gas, e.g., D under H_2 carrier is significantly larger than that under N_2. The value of D/k_s, therefore, depends on growth conditions.

Growth rate in the selective growth area is often normalized by the value at the position far from any masks, yielding growth-rate enhancement (GRE), as shown in Fig. 4(a). The value of D/k_s can be extracted for a specific material and a growth condition, by fitting a calculated curve to the experimental data taking D/k_s as the only parameter. The value of D can be estimated if we assume a molecular weight and an equivalent spherical diameter (so-called L-J size parameter) of a group-III precursor, using Chapman-Enskog's theory (6). Figure 4(b) is an Arrhenius plot of k_s values for binary materials (7, 8). InAs has larger k_s than GaAs, indicating that indium "sticks" on the surface more readily than Ga on an As-stabilized surface. The activation energy for GaAs changed drastically around 600 °C due to transition in surface reconstruction structure (9).

For the design of selective-area masks, it is necessary to collect the values of k_s for all the possible combinations of a group-III precursor and a crystal surface as a function of temperature.

III. Coupled analysis with reactor-scale distributions

Even if we are not certain about the vapor-phase group-III precursor forming a crystal, a value of D can be estimated, or validated, through analysis of reactor-scale growth-rate profiles of that crystal layer. As shown in Fig. 5, D has a significant effect on the growth rate profile in the downstream part of a reactor, making it possible to determine the value of D using that profile (10). For GaAs and InP, the values of D determined in such a way agree well with the estimated values by Chapman-Enskog's theory.

Interestingly, as shown in Fig. 6, it was found that the k_s for GaAs was not constant over an entire susceptor, although the susceptor temperature was uniform. This is contrary to the assumption in Fig. 3, where k_s is unique to a vapor-phase precursor. With an increased total flow rate, the profile in the upstream (X<130 mm) is pushed to the downstream, indicating that k_s varies due to a vapor-phase phenomena. This variation of k_s seems to be an indication that two species, probably $(CH_3)_3Ga$ and CH_3Ga, participate in GaAs growth; in the upstream, a fraction of a parent molecule $(CH_3)_3Ga$ is dominant, resulting in a smaller value of overall k_s because $(CH_3)_3Ga$ has smaller reactivity (smaller k_s) than CH_3Ga. The decay of k_s for X>130 mm is almost independent of the flow rate and seems to be related with surface reaction kinetics with CH_3Ga; in detail, the rate of Ga surface incorporation is not simply proportional to a vapor-phase concentration of CH_3Ga but exhibits a tendency in which the incorporation rate is less dependent on the CH_3Ga concentration when the concentration is too much, i.e., Langmuir-Hinshelwood surface reaction mechanism.

IV. Modeling luminescence wavelength from the MQWs by selective-area growth and application to monolithic integration of semiconductor optical devices

If the value of k_s is known for the target layer, we can simulate the distributions of layer thickness and composition around a given shape of masks. Band lineup of MQWs at a given position around the mask can be obtained based on the thickness and composition, as shown in Fig. 7. Quantum energy levels are, then, obtained by solving Schrödinger's equation with effective-mass approximation. For the case of InGaAsP MQWs, a red-shift of luminescence wavelength by approximately 200 nm can be obtained as a result of modulation in both the band-edge energies and the quantum energy levels.

As shown in Fig. 8, such a simulation reproduces the measured dependence of luminescence peak wavelength on the mask width for both bulk InGaAsP layers and the MQWs that are composed of these layers (11).

Figure 9 shows an example of monolithic integration de-

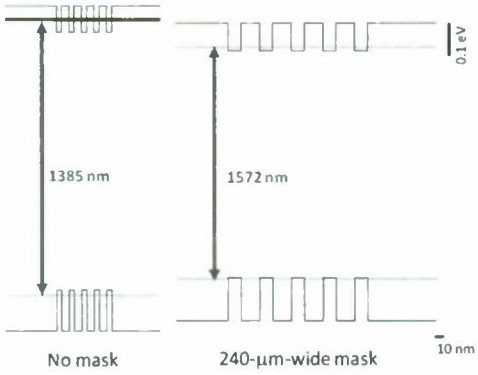

Fig. 7 Schematic illustration on what happens in the selective-area growth of MQWs. Growth without masks and in the center of a 60-μm-wide growth area that is sandwiched by 240-μm-wide masks. The lateral direction represents layer thickness and the vertical direction represents energy. The well and the barrier are InGaAsP with different atomic content in the growth without masks. The masks bring about modulations in two aspects: (1) group-III atomic content to alter the position of band edges, (2) thickness of the well to alter the extent of quantum confinement. Luminescence wavelength from the two MQWs are brought about by those two effects.

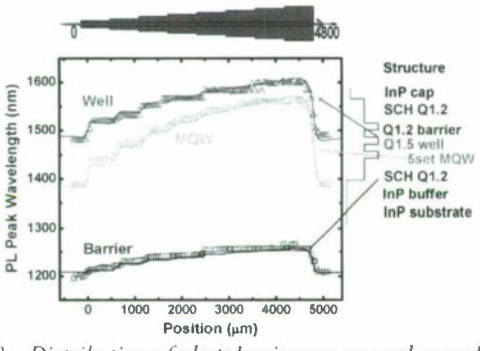

Fig. 8 Distribution of photoluminescence peak wavelength at the center of the 60-μm-wide stripe growth area that is sandwiched by the staircase-like masks as shown on the top. The graph contains luminescence from the bulk InGaAsP layers corresponding to the well (Q1.5; triangles) and the barrier (Q1.2; squares), and luminescence from the MQWs (circles). Shift of luminescence wavelength from the bulk layers is the result of more In-rich atomic content for wider masks. Luminescence from the MQWs exhibits more red-shift according to the wider masks, which, as well as the compositional change described above, reflects reduced quantum confinement effect due to increased thickness of the well. Simulation results, considering the effects of modulation in both group-III atomic content and layer thickness, agrees well with the experimental data.

vice: 4-ch DFB lasers are coupled with waveguides and a coupler (12). A peak wavelength in the gain spectrum from the active layer was red-shifted by setting wider masks at both sides of the waveguide-type laser structure. A lasing wave-

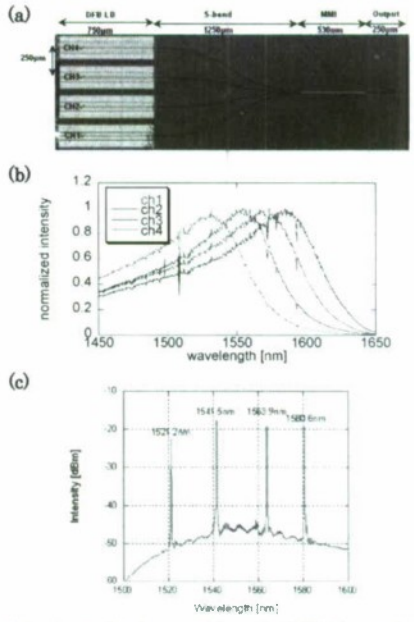

Fig. 9 A 4-ch multiple wavelength DFB laser integrated with a coupler by monolithic integration using selective-area growth. (a) An outlook of the device observed by an optical microscope. (b) Photoluminescence spectra for each active layer which are sandwiched by the masks with varied thicknesses. (c) A lasing spectrum observed at the output port of the device, which contains lasing at 4 different wavelengths in 4 channels.

length was finally determined by the grating pitch on the active layer, but tuning of the gain peak in the vicinity of the lasing wavelength is mandatory, which has been achieved by adjustment of the mask width. Further size reduction of this device is possible by narrowing the spacing between the channels, which induces interference among neighboring masks in growth rate enhancement. Our numerical simulation is of crucial help for the mask design in such a complicated situation. As well as the control of luminescence wavelength, we can control of strain in the well layer and thus polarization control has been demonstrated (13).

V. Extension to III-nitride materials

Selective-area growth of GaN-based materials is far more difficult than that of InGaAsP materials. Specific crystal planes tend to emerge preferentially, just as the pyramidal growth in Fig. 2. Nonetheless, elaborate choice of the direction of a stripe growth area on the surface of a c-plane GaN template, as well as appropriate growth temperature, make it possible to obtain smooth GaN surface in the growth area. Parabolic profiles, which are proof of the contribution of vapor-phase diffusion, were successfully obtained as shown in Fig. 10 (14). These profiles can be reasonably fitted by the simulated curves of growth rate enhancement, allowing us to extract the value of D/k_s for the growth of GaN.

Decoupling k_s from D/k_s is not straightforward because the

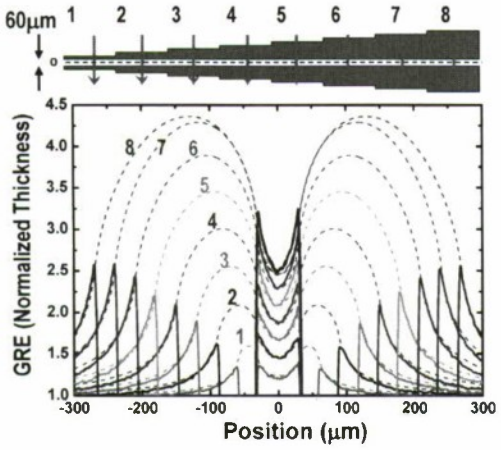

Fig. 10 Measured and simulated growth-rate enhancement (GRE) profiles of GaN along the arrows 1-8 in the schematic of the mask pattern. Growth temperature was 1150°C and total pressure was 10 kPa with H_2 carrier gas. The solid lines denote experimental GRE values and the dashed lines denote calculated GRE profiles with an assumption of D/k_s = 50 μm, which show excellent agreement with the experimental data, suggesting that the growth rate of GaN around the masks is largely governed by the vapor-phase diffusion of a Ga precursor and its surface incorporation, similarly to the selective-area growth of InGaAsP materials.

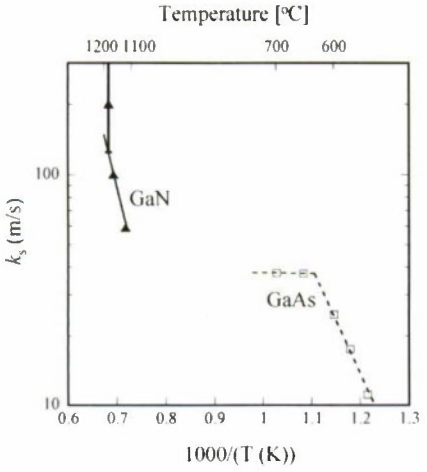

Fig. 11 Arrhenius plot of k_s for GaN surface reaction as a comparison with k_s for GaAs surface reaction (the same data in Fig. 4 (b). The ks values for GaN has an activation energy of 180 kJ/mol, which is much larger than the value for GaAs.

vapor-phase precursor leading to GaN crystal growth has been still unelear. We, therefore, have analyzed reactor-scale profiles of GaN growth rate and tentatively concluded that the major vapor-phase precursor for GaN crystal is likely to be $(CH_3)_2Ga{:}NH_2$, which is a reaction product between the source materials $(CH_3)_3Ga$ and NH_3 (15). The value of D for this molecule has been also estimated based on the growth-rate profile, allowing us to obtain k_s values as shown in Fig. 11. Comparison between GaN and GaAs is not straightforward because selective-area growth of each material is possible at much different temperatures. It is, however, clear that k_s for GaN is much larger than GaAs: based on the k_s values, surface sticking probability of $(CH_3)_2Ga{:}NH_2$ on GaN is almost unity while that of CH_3Ga on GaAs is roughly 0.2. This is possibly one of the reason why surface morphology of GaN is difficult to control.

Similarly to the InGaAsP MQWs, we have attempted to shift visible luminescence wavelength from InGaN/GaN MQWs to longer wavelengths by setting wider masks (14). Figure 12 (a) shows the effect of mask width on the luminescence peak wavelength for both a bulk InGaN layer and InGaN MQWs. The peak wavelength from the bulk is independent of the mask width, indicating no modulation of indium composition according to the mask width. This is contrary to the case of an InGaAsP layer, which contained more indium in the vicinity of a wider mask. The peak wavelength shift for the MQWs is, then, solely due to thickness modulation of the InGaN wells according to the mask width. This assumption is confirmed when we plot the peak wavelength versus the thickness of the InGaN wells, as shown in Fig. 12 (b).

Why there was no modulation of indium content? At the growth temperature of 830 °C, InN layer cannot be grown due to its poor thermal stability. It is, therefore, possible that incorporation of indium to InGaN occurs only when Ga is incorporated to the InGaN at a fixed In/Ga incorporation ratio. For wider range of wavelength modulation, modulation of indium content is demanded, which may be possible at a lower temperature and/or a higher NH_3 partial pressure.

V. Summary

In selective area growth of III-V semiconductor MQWs, in-plane modulation of a luminescence peak wavelength, which is mandatory for monolithic integration of semiconductor optical devices, is mainly brought about by modulation of the thickness and composition of the well layers. Substantial modulation is mainly due to vapor-phase diffusion of a group-III precursor, and it is well described by a simple diffusion/reaction model, provided that surface reaction rate coefficients for the precursors are available. The rate coefficients can be obtained through observation of growth rate enhancement with a well-defined mask pattern, and they provide insight into basic surface reaction kinetics in MOVPE. The framework of modeling is common for both InGaAsP and III-nitride materials. Accurate prediction of luminescence wavelength for InGaAsP MQWs has been achieved. InGaN/GaN MQWs for visible luminescence are accompanied by complicated incorporation mechanism of indium, and InGaN with large indium content needs more comprehensive analysis.

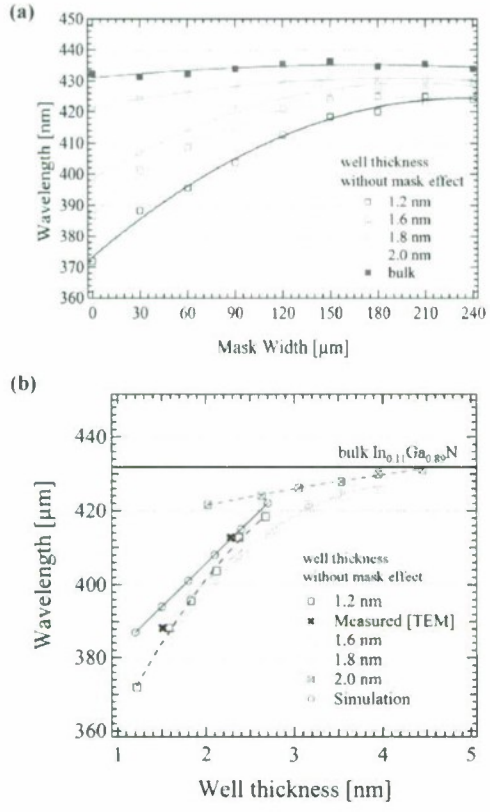

Fig. 12 Cathode luminescence (CL) peak wavelength of InGaN bulk layer and InGaN/GaN MQWs with varied growth periods of the well. The layers were grown at 830°C and 100 mbar with N_2 carrier gas. The thickness of the wells without the effect of masks varied from 1.2 to 2.0 nm accordingly. The luminescence was observed at the center of a 60-μm-wide selective growth area between the masks, the width of which increased stepwise. The graph (a) represents the effect of the mask width, indicating that wider mask resulted in red-shift of the peak wavelength. In the graph (b), the peak wavelength was plotted against an InGaN well thickness, where a well thickness at each position was estimated by multiplying the thickness at the position sufficiently far from masks by the GRE value of a bulk InGaN at the position of luminescence measurement, which had been measured in another experiment. Dependence of the peak wavelength on the well thickness almost fits with a single curve, suggesting that the red-shift of the luminescence wavelength is due to an increased thickness of the well with an increased mask width. The lines are guides to the eye.

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TYPE-II InP/GaAs$_X$Sb$_{1-X}$ DHBTs WITH SIMULTANEOUS F_T AND F_{MAX} >340 GHz FABRICATED BY CONTACT LITHOGRAPHY

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Abstract

InP/GaAsSb/InP DHBTs with 125 and 150 nm collector thicknesses were fabricated by optical contact lithography in a standard triple mesa process. It is shown that a peak current-gain cut-off frequency f_T = 343 GHz and maximum oscillation frequency f_{MAX} = 351 GHz were simultaneously achieved on devices with an emitter area of 0.6 × 11.5 μm^2 and a 150 nm collector. To the best of our knowledge, these are the first InP/GaAsSb DHBTs to offer balanced figures-of-merit exceeding 300 GHz and a current gain $\beta > 60$. Similar devices with a thinner collector (125 nm) exhibit a peak f_T = 377 GHz with f_{MAX} = 318 GHz due to the interplay between a reduced collector transit time and the increased collector-base depletion capacitance. For the devices under study, the extrinsic collector-base capacitance was observed to have a small impact on f_{MAX}. However, the base mesa over-etching is essential to reduce the extrinsic capacitance and thus improve f_T.

I. Introduction

Type-II InP/GaAsSb DHBTs have attracted interest in recent years due to the advantages conferred by the staggered "type-II" band alignment between the GaAsSb base and the InP collector, which prevents the electron blocking effect that occurs in Type-I InP/InGaAs DHBTs at higher current densities. Additionally, the large valence band discontinuity ΔE_V at emitter/base (E/B) junction suppresses hole back-injection into the emitter, and base spreading into the collector under saturation-mode operation. Despite these attractive features and some interesting device demonstrations, the gain-bandwidth properties of InP/GaAsSb DHBTs still remain to be optimized.

Recent work on Type-II InP/GaAsSb DHBTs fabricated using electron-beam lithography demonstrated f_T = 600 GHz and f_{MAX} = 300 GHz with an emitter size of 0.3 × 11.5 μm^2 [1]. Other devices defined by e-beam lithography with an emitter size of 0.46 × 3.1 μm^2 showed simultaneous values f_T = 480 GHz and f_{MAX} = 420 GHz [2]. Although these devices exhibited record performances for Type-II InP/GaAsSb DHBTs, electron beam lithography is not the most attractive avenue for the production of high-speed devices due to its throughput and associated costs. As well, it would be highly desirable to engineer devices with balanced values for f_T and f_{MAX} with more relaxed critical dimensions.

In this work, we study the scaling of InP/GaAsSb DHBTs fabricated by optical contact lithography, and we report devices which achieve f_T = 343 GHz and f_{MAX} = 351 GHz with the emitter size of 0.6 × 11.5 μm^2 while maintaining a breakdown voltage BV_{CEO} = 5.85 V. The effects of base metal undercut etch and of the base metallization contact width on the RF performances of our InP/GaAsSb DHBTs are also be discussed.

II. Experimental Procedure

The epitaxial layer structures used here consist of a 300 nm $n = 3 \times 10^{19}$ cm^{-3} InP sub-collector; a heavily doped $n = 3 \times 10^{19}$ cm^{-3} 20 nm $Ga_{0.47}In_{0.53}As$ etch-stop layer, a 50 nm collector pedestal and an InP collector with a doping of $n = 3 \times 10^{16}$ cm^{-3}; a 20 nm base and a 40nm (Ga,In)P composite emitter; a 110 nm $Ga_{0.47}In_{0.53}As$ emitter cap layer, and a 35 nm composite emitter contact layer. The 20 nm thick base is a C:GaAs$_x$Sb$_{1-x}$ graded layer with an average carbon doping level of 8×10^{19} cm^{-3} and an [As] concentration increasing from $x = 0.4$ on the collector side to $x = 0.6$ at the emitter side. Samples with InP collector thicknesses of 125 and 150 nm were grown. The measured base sheet resistances for both samples were practically identical (1200 Ω/sq).

Transistors were fabricated in a standard triple-mesa etching process. The base mesa was formed by dry and wet etching, in a combination engineered to result in a 0.75 μm undercut of the base contact of width W_B in order to reduce the extrinsic base collector capacitance C_{CBX} by leaving a portion of width W_S over the semiconductor material. Fig. 1 shows the cross-section of a device with the B/E junction protected by a positive photoresist mask after the base mesa etching step. It

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shows that a good alignment by optical contact lithography is necessary in order to permit an aggressive base mesa etching.

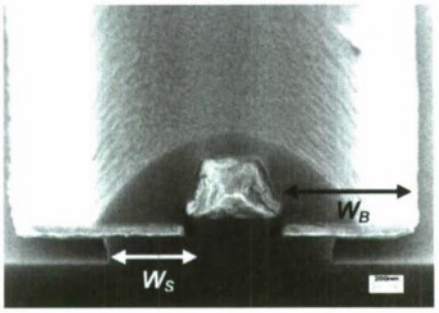

Fig. 1 Scanning electron microscopy (SEM) picture after aggressive base mesa etching. It shows an undercut of ~0.75 μm for both the base and the collector.

III. Results and Discussions

Fig. 2 shows Gummel characteristics from 0.6 × 11.5 μm^2 devices for both collector thicknesses. Both feature identical base and collector currents before the Kirk effect sets in. This indicates that the epitaxial layers are practically identical with the exception of the collector thickness, and it demonstrates excellent growth and processing reproducibility.

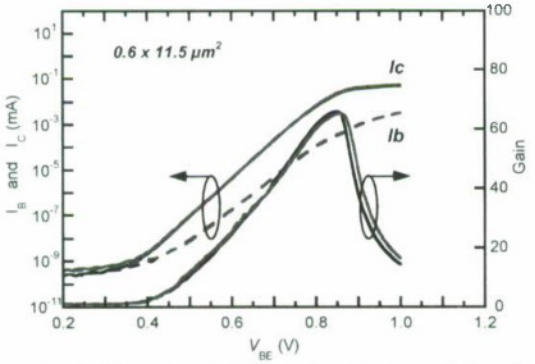

Fig. 2 Typical Gummel plot of 0.6 × 11.5 μm^2 devices with the collector thickness of 125 and 150 nm, respectively. The base and collector currents overlap well at low biases. At the higher biases, the device with the thinner collector shows a slightly higher collector current due to its higher Kirk current.

The peak current gain exceeds $\beta > 60$ for both wafers, suggesting that gain is available to be traded-off to further lower the base sheet resistance. As expected, the device with 125 nm collector shows a slightly higher Kirk current than the device with 150 nm collector. This is also verified by the plots of gain as a function of V_{BE} as also shown in the same plot.

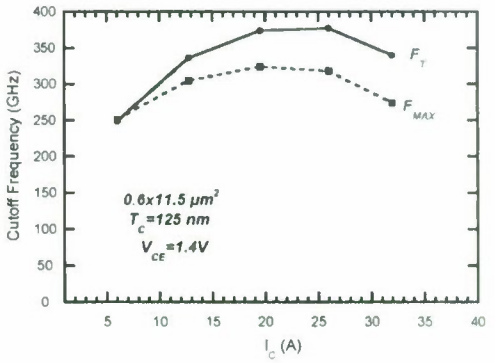

Fig. 3 Current gain cut-off frequency maximum oscillation frequency as a function of collector current for 0.6 × 11.5 μm^2 devices with the collector thickness of 125 nm. V_{CE} was set to 1.4 V.

Fig. 3 shows f_T and f_{MAX} as a function of collector current for 0.6 × 11.5 μm^2 devices built with a 125 nm InP collector at the bias of V_{CE} = 1.4V. f_T and f_{MAX} roll-off as the Kirk effect occurs. The devices with a 125 nm InP collector exhibit a peak f_{MAX} at the bias of V_{CE} = 1.4 V whereas devices with a 150 nm InP collector show a peak f_{MAX} at the bias of V_{CE} = 1.6 V.

Fig. 4 shows f_T and f_{MAX} as a function of collector current for 0.6 × 11.5 μm^2 devices from each wafer at the collector emitter bias of V_{CE} = 1.6 V. Under this bias, the InP collector is depleted in both devices. Fundamental differences in device performance are highlighted at high current densities, when the Kirk limit is exceeded in the thicker collector device, bringing about a precipitous roll-off of f_T and f_{MAX} with increasing current levels. On the contrary, the 125 nm collector transistor shows $f_{MAX} < f_T$ due to the higher base-collector capacitance but maintains a better performance at high current densities.

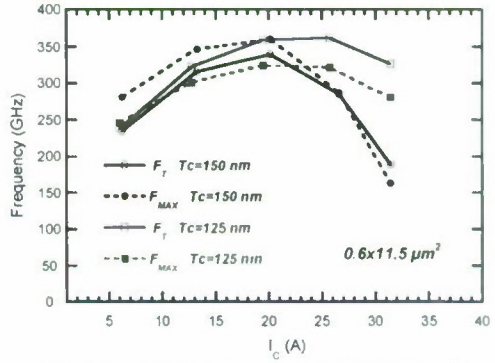

Fig. 4 Current gain cut-off frequency and maximum oscillation frequency as a function of collector current for 0.6 × 11.5 μm^2 devices with collector thickness of 125 and 150 nm, respectively. V_{CE} was set to 1.6 V.

TABLE I: UNDERCUT EFFECTS FOR A 125 NM INP COLLECTOR.

Undercut (μm)	W_B (μm)	W_S (μm)	f_T (GHz)	f_{MAX} (GHz)	$f_T/(8\pi f_{MAX}^2)$ (fs)	C_{CB} (fF)
0.45	1.25	0.80	360	313	146.3	7.3
0.45	2.0	1.55	313	278	161.3	8.1
0.75	1.25	0.50	377	318	149.6	7.5
0.75	2.0	1.25	325	288	155.9	7.8

Similar devices with different base undercut etching and with various base metallization contact widths were also fabricated on the wafer with a 125 nm InP collector. Table I above summarizes the RF performance of these devices. Devices with $W_B = 2$ μm base metallization contact show lower f_T and f_{MAX} values than those with 1.25 μm base contact. The devices with undercut of ~0.75 μm by aggressive base over-etching show higher f_T values than those with ~0.45 μm base undercut over-etching. The measured base contact resistivity determined from linear TLM patterns is $\sim 4 \times 10^{-7}$ Ω-cm^2, corresponding to a calculated total base resistance of $R_B \sim 19.4$ Ω, according to the device geometry shared by all transistors. The R_B value extracted from RF measurements is in good agreement, showing a value of $R_B = 20$ Ω.

In the simplest approximation, the maximum oscillation frequency f_{MAX} is related to f_T by

$$f_{MAX} = \sqrt{f_T / (8\pi R_B C_{CB})} \quad (1)$$

Table I shows the effective R_BC_{CB} products determined from the measured f_T and f_{MAX} values, as well as the corresponding C_{CB}. It is found that all the devices show very similar base-collector capacitances ~7-8 fF, regardless of very different amounts of base contact undercut etching. In other words, the extrinsic base capacitance C_{CBX} only plays a secondary role in determining f_{MAX}, and the intrinsic capacitance C_{CBI} dominates. This observation is in good agreement with the analysis of Kurishima [3].

Although an aggressive base over-etching to reduce the total base-collector junction area does not directly reduce the effective R_BC_{CB} value which determines f_{MAX}, Table I shows that it is beneficial to increase f_T: for the 125 nm collector, reducing W_B and W_S can result in substantial improvements in f_T, leading to an increase of 60 GHz/μm of extrinsic base/collector width reduction.

IV. Conclusions

The developments presented in the present work show, for the first time since the demonstration of 300 GHz transistors by Dvorak *et al.* [4], that a balanced performance can be achieved in InP/GaAsSb DHBTs even without aggressive lithographic scaling. The extent of the progress can be better assessed by noting that Chu-Kung *et al.* reported 0.38×8 μm^2 devices with $f_T = 358$ GHz and $f_{MAX} = 194$ GHz with $BV_{CEO} = 4.2$ V and a current gain of $\beta = 19$ in an electron beam lithography process [5].

The present results suggest that transistors with f_T and f_{MAX} approaching 400 GHz should be possible in an all-optical process if the total base resistance can be further reduced. In this context, optical lithography has already permitted the demonstration of devices with $f_T = 384$ GHz [6]. From the base resistance point of view, assuming base recombination is dominated by Auger processes would suggest a doubling of the base doping level would be accompanied by a 4-fold gain reduction [7], leading to an expected $\beta = 15$ for a 600 Ohm/sq. base sheet resistance. There are however some indications that Auger might not be dominant in GaAsSb materials grown by different methods or with alternate precursors as in [8], permitting one to anticipate potential even more favorable outcomes. In any case, the present current gain levels should comfortably allow for a reduction of the base sheet resistance to values 700-800 Ohms/sq.

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400 GHz F_{MAX} InP/GaAsSb HBT FOR MILLIMETER-WAVE APPLICATIONS

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Abstract

This paper presents multi-finger InP/GaAsSb/InP HBTs designed for millimeter-wave applications. The 0.7x10 µm² emitter size 4- and 8- finger devices demonstrated f_T and f_{max} above 200 GHz and 400 GHz respectively, a current gain of 28 and an emitter breakdown voltage of 7V. We also report on the performances of a 2-stage power amplifier based on more conservative devices (1x15 µm² two-emitter finger). This circuit delivers an output power above 15 dBm at 60 GHz.

I. INTRODUCTION

In recent years, the interest for InP HBT MMICs has developed, owing to their large potential for low noise and power applications at millimeter waves. Most of the recent work on oscillators (1-2) and amplifiers (3-4) was done using the mainstream InGaAs-based structures. The GaAsSb-based double heterojunction technology (5) which does not need a spacer nor transition layers in the collector offers some potential advantage for lower thermal resistance and thus for higher performance.

In this paper, we present submicron multi-finger GaAsSb-based DHBTs with high bandwidth (f_{max}>400 GHz) and large breakdown voltage. These characteristics are suitable for millimeter-wave applications.

II. HBT STRUCTURE AND PROCESS

HBT heterostructures were grown by Solid Source MBE on a 3'' SI-InP substrate. The epitaxial layers include a 230 nm thick low-doped InP ($5x10^{16}$ cm^{-3}) collector to ensure both a large breakdown voltage (>7V) and a small collector capacitance. A rather thin (28 nm) uniformly doped GaAsSb base layer was used (C-doping: $1.5x20$ cm^{-3}). A moderately thin (50 nm) sub-collector InGaAs layer was also used for low thermal resistance.

HBT emitters were designed with a 0.7 or 1 µm nominal width (actual emitter crystal width is 0.6 and 0.9 µm respectively) and 10 µm to 20 µm length. Devices with 1, 2, 4 and 8 interdigitated emitter fingers were realized (Fig. 1). The distance between fingers is 8 µm. The base contact extends 0.4 and 0.5 µm on each side of the emitter for the 0.7 and 1µm emitter width device, respectively.

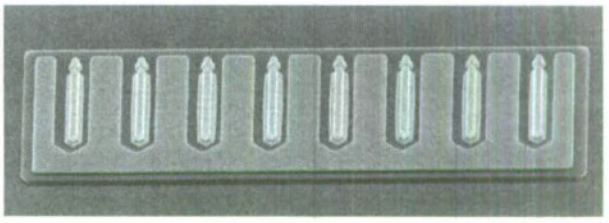

Figure 1: 1x15 µm² 8-finger HBT before interconnection

The devices were fabricated using an all wet-etched self-aligned triple mesa technology. Emitter and base contacts were defined by electron beam lithography in order to obtain a high alignment accuracy. Additional steps for circuits included thin film resistors and capacitors and 3-metal layer interconnects. BCB was used for passivation and isolation.

III. DEVICE PERFORMANCES

A. DC CHARACTERISTICS

DC characteristics show a current gain of 28 and a breakdown voltage of 7V @ 10 µA for the mono- and multi-finger devices. The ideality factors are 1.0 and 1.49-1.58 for the base-collector and emitter-base junction, respectively. The current-voltage characteristics scale with the number of

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emitter fingers as illustrated on Fig. 2 and Fig. 3.

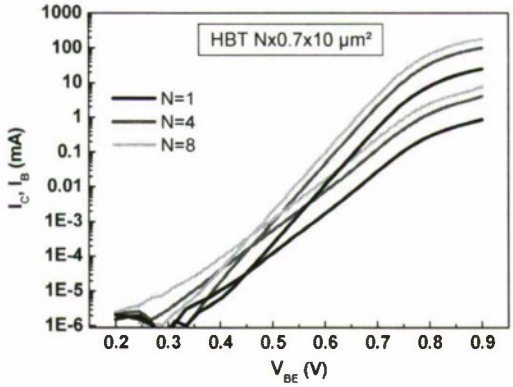

Figure 2: Gummel plot of HBTs with 1, 4 and 8, 10µm-long emitter fingers

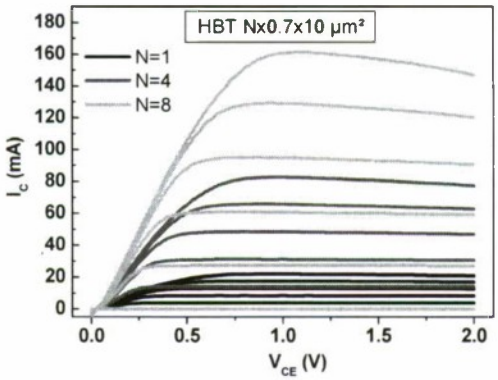

Figure 3: I(V) characteristics of HBTs with 1, 4 and 8, 10µm-long emitter fingers

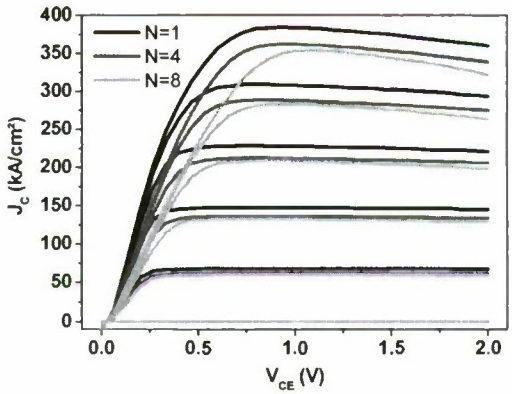

Figure 4: J_C (V_{CE}) characteristics of HBTs with 1-, 4- and 8, 10µm-long emitter fingers. The base current density varies from 0 to 13 kA/cm² (step ~ 2.2 kA/cm²)

As shown on I(V) characteristics, the saturation slope increases with the emitter finger number due to emitter resistance reduction. As a result, for a constant collector current, the knee voltage decreases with the emitter finger number. Its value is 0.51V at I_C=60 mA and 0.72V at I_C=120 mA for the 4-finger and 8-finger HBT, respectively. At very high collector current, we observe a negative slope indicating that device self-heating is occuring. As illustrated on Fig. 4 representing the collector current density versus emitter-collector voltage, the phenomenon is more important for the 8-finger device which is more impacted by thermal coupling. Actually, the thermal resistances of the multi-finger devices do not decrease linearly when the number of fingers increases (Table 1): the 8-finger HBT thermal resistance is only 5 times lower than the mono-finger one.

Table 1: Thermal resistance versus the number of fingers (N) at J_C=300kA/cm² and V_{CE}=2V

N	1	4	8
R_{TH} (°C/W)	2940	1000	590

The thermal resistances were extracted following the method detailed in (6).

B. AC CHARACTERISTICS

For the 0.7 µm HBTs, current gain cut-off frequency f_T as deduced from S-parameter measurements up to 60 GHz peaks at 210 GHz, independently of the fingers number for V_{CE}=1.6V. This value is in agreement with the collector thickness. Kirk effect (defined at peak f_T) associated with upward band bending in collector occurs at 350 kA/cm² (Fig. 5).

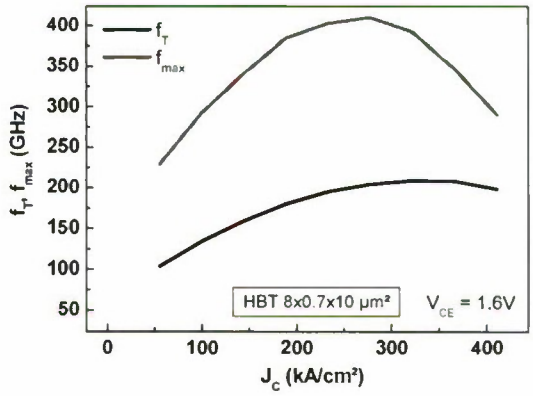

Figure 5: Variation of f_T and f_{max} for a 8x0.7x10 µm² HBT, illustrating the high collector current density at peak f_{max} and f_T

F_{max} peaks at 410 GHz for J_C = 280 kA/cm^2, and does not depend on the number of emitter fingers (Fig. 6). We extracted a Gmax of 15 dB at 60 GHz for the three devices (Fig. 7). This seems to illustrate the low thermal resistance benefiting from the all-InP collector. The high f_{max} results from a low base resistance value (10.8 Ω and 1.55 Ω for the 1-finger and 8-finger respectively) in spite of the limited base thickness (28 nm). For the 8-finger device, peak f_{max} occurs at a collector current of 120 mA for V_{CE} = 1.6 to 2V. These characteristics appear quite attractive for mm-wave applications.

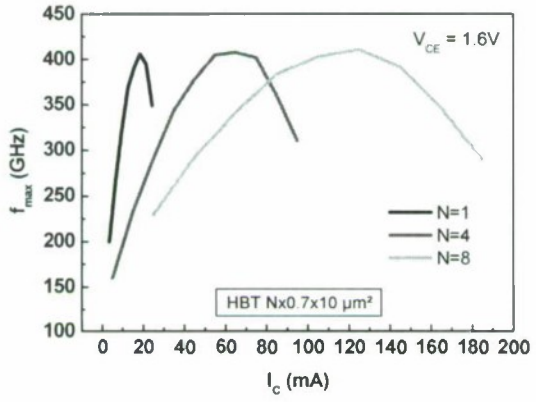

Figure 6: f_{max} variations with current for HBTs with varying number of emitter fingers. While $f_{max,peak}$ remains constant, I_{Cpeak} scales up

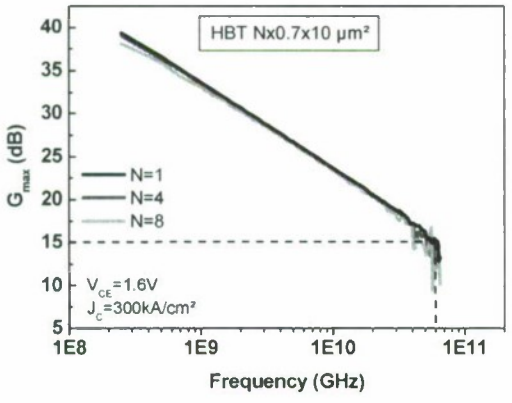

Figure 7: G_{max} versus frequency for HBTs with 1, 4 and 8 emitter fingers, showing a constant f_{max} value

IV. FIRST CIRCUIT APPLICATIONS

First circuits have been designed (amplifiers and oscillators), based on conservative HBT designs (2-finger HBTs with 1x15 µm² emitter size) because of their higher fabrication yield. The frequency characteristics of these devices are F_T ~ 200 GHz and f_{max} > 300 GHz for V_{CE} = 1.6V to 2.2V at J_C = 300kA/cm². The characteristics of a 60 GHz 2-stage amplifier (6) shown on Fig. 8 are presented on Fig. 9 for biasing conditions: V_{CE1}=3V, I_{C1}=35 mA, V_{CE2}=3V, I_{C2}=55 mA. For 2.4 dB compression, the measured linear gain is 9.8dB, P_{OUTmax}=15.4 dBm and PAE_{max}=11%. The better results observed in measurements compared to the simulation is due to a slight epitaxy difference between modeled and final devices. These results are quite encouraging and show GaAsSb-based HBT process suitability for millimeter wave IC realization.

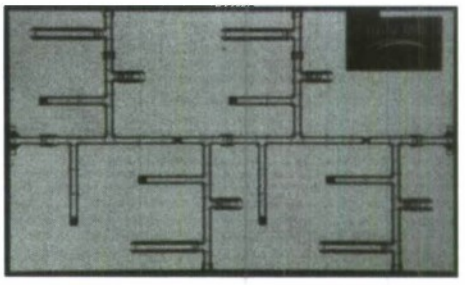

Figure 8 : 3.9x2.3mm² 2-stage amplifier µphotograph

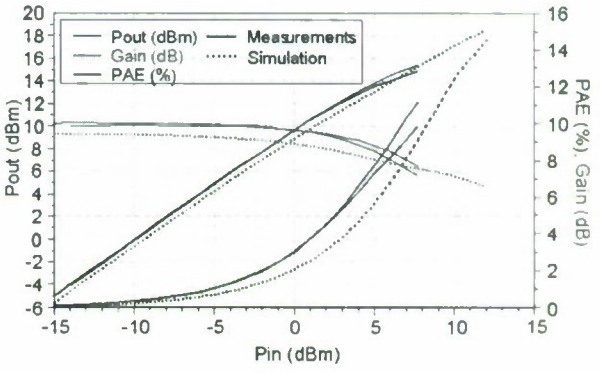

Figure 9: Characteristics of the 2-stage 60 GHz amplifier designed and fabricated in an InP/GaAsSb process (1 µm emitter width)

The same HBTs were used to design MMIC oscillators operating at 45 GHz. The characteristics of these circuits are detailed in (7).

V. CONCLUSIONS

InP/GaAsSb multi-finger DHBTs have been developed for millimeter-wave applications. Small base resistance associated to a high base doping level resulted in 0.7 emitter width 4- and 8-finger devices offering f_{max} above 400 GHz, together with a large collector current. The thermal effects existing particulary in 8-finger devices are not detrimental to AC performances for V_{CE} = 1.6V to 2V. These results are very promising for the realization of amplifiers for E-band transmission.

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InP DHBTs Having Sidewall and Lateral Collector Schottky Contacts

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Low Surface Recombination Velocity in InAlAs/InGaAsSb/ InGaAs Double Heterojunction Bipolar Transistors

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Paper is not available.

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A 120-Gbit/s 520-mV$_{PP}$ MULTIPLEXER IC USING 1-μm SELF-ALIGNED InP/InGaAs/InP DHBT WITH EMITTER MESA PASSIVATION LEDGE

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Abstract

We fabricated 2:1 multiplexer IC (MUX) with a retiming function by using 1-μm self-aligned InP/InGaAs/InP double heterostructure bipolar transistors (DHBTs). As a result of the high performance DHBTs and the circuit design, in which we implemented broadband impedance matching, the MUX operated at 120 Gbit/s with a power dissipation of 1.27 W and an output amplitude of 520 mV when measured on the wafer. The MUX was assembled in a module using V-connectors for practical use. In this module, the MUX operated at 113 Gbit/s with an output amplitude of 514 mW and a power dissipation of 1.4 W.

I. Introduction

Demands for high-bit-rate optical communication systems continue to rise in response to the explosive increase in data traffic. The communication systems themselves and test-and-measurement equipment used to construct these systems require various kinds of high-speed digital ICs. The multiplexer IC (MUX) is an important component of this equipment, and the development of various ultra-high-speed MUXes that use SiGe heterostructure bipolar transistors (HBTs), InP HBTs, and InP high electron mobility transistors (HEMTs) and that demonstrate an excellent performance has been reported previously [1–15]. However, most of these reports have not emphasized practical usefulness or ease of handling.

This paper reports the development of an ultra-high-speed 2:1 MUX fabricated using self-aligned InP/InGaAs/InP DHBTs that are characterized by a ledge structure for emitter mesa passivation, high-speed operation even under low bias conditions, and a high breakdown voltage [16]. When designing the MUX, we devised a clock buffer configuration to reduce power dissipation and layout complexity and to increase the operating speed. We also left safety margins in the internal logic swing and output amplitude to allow for module assembly. After conducting on-wafer measurements, we assembled the MUX in a module using V-connectors for easy use. We then confirmed that the module could operate at a high-speed.

As a result of the device and circuit design technologies we used, the MUX operated at 120 Gbit/s with an output amplitude (V_{pp}) of 520 mV at a supply voltage (V_{EE}) of –3.4 V and a power dissipation (P_{dis}) of 1.27 W when measured on the wafer. When assembled in a module, MUX operated at 113 Gbit/s with a V_{pp} of 514 mV, a V_{EE} of –3.5 V, and a P_{dis} of 1.4 W.

II. Device Technologies

A schematic cross-sectional view of the InP/InGaAs/InP DHBT used in the MUX is shown in Fig. 1. The DHBTs have a feature emitter size of 1 μm, self-aligned base/emitter structure, and a passivation ledge surrounding the emitter mesas. Uniform, reproducible ledges were formed by inserting a thin InGaAs etch stop layer in the InP emitter [16]. The ledge suppresses recombination at the emitter mesa periphery, increasing reliability [17]. The collector structure of the DHBTs was devised to enable both high-speed operation under low bias conditions and a high breakdown voltage.

Figure 2 shows the I_C-V_{CE} curves of a DHBT with an emitter size of 1 × 5 μm^2. The DHBT current gain is 44 in the I_C region in the figure. The current gain is almost constant from an I_C level of μA. The contour lines of the current gain cut-off frequency (f_T), and maximum oscillation frequency (f_{max}) in the I_{CE}-V_{CE} plane are also plotted in Fig. 2. A peak f_T of 233 GHz

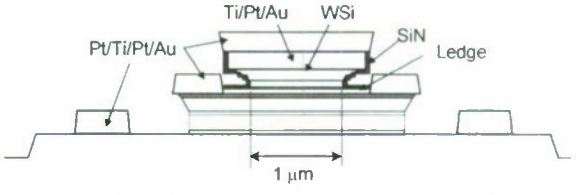

Fig. 1. Schematic cross-sectional view of self-aligned DHBT with a passivation ledge.

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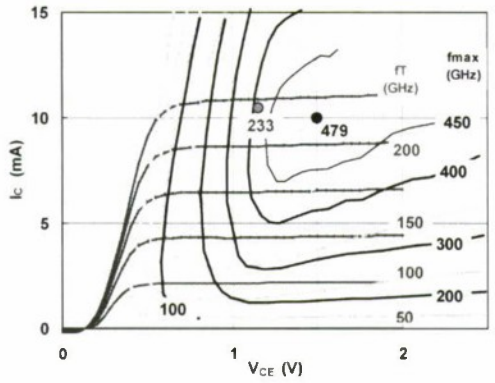


Fig. 2. *I-V* characteristics and contour lines of f_T and f_{max} in the same V_{CE}-I_C plane. The emitter area of the DHBT is 1×5-μm^2. The I_B step for the *I-V* curves is 50 μA. The contour lines were obtained by s-parameter measurements at more than 1000 bias points.

and a peak f_{max} of 479 GHz were obtained at bias points of (1.15 V, 10.5 mA), and (1.5 V, 10 mA), respectively. It should be noted that not only are the peak values of f_T and f_{max} large, but that both f_T and f_{max} also far exceed 200 GHz even in the low-V_{CE} region below 0.85 V. These high-speed characteristics under low-V_{CE} conditions make it possible to reduce the power supply voltage of the IC. Moreover, the DHBT has a breakdown voltage, BV_{CEO}, of as high as 6.2 V.

The passive components in the MUX included metal-insulator-metal (MIM) capacitors, two kinds of resistors with sheet resistances of 15.5 Ω/square and 200 Ω/square that were created using a subcollector layer and sputtered WSiN layer, and two-level interconnects. Benzocyclobutene (BCB) was used as the dielectric material for planerization.

III. Circuit Design

Figure 3 shows a block diagram of the MUX, showing the clock lines in detail. The MUX has two data buffers, a clock buffer, a master-slave (MS-) D-type flip-flop (DFF) with two latches, a master-slave-master (MSM-) DFF with three latches, a selector, and an output buffer. A logic swing of 300 mV was used to allow for module assembly, because the inductance of the wire bonds in the module could cause waveform ringing and incorrect operation if the logic swing was too small. In practical use, a large *V*pp is best, especially in ultra-high-bit-rate operations, because output signals from the MUX or module are inevitably degraded by loss in the bonding wires, housing substrate transmission lines, V-connectors in the module and cables. We therefore

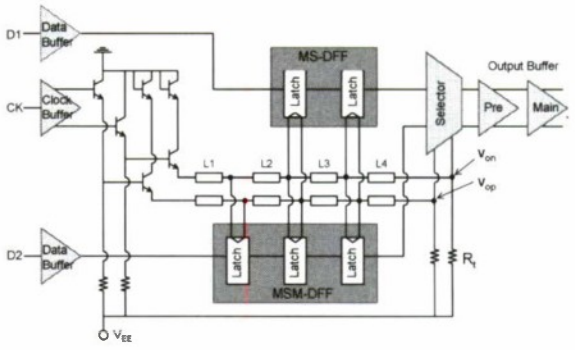


Fig. 3. Block diagram of MUX with detailed configuration of clock lines designed for broadband impedance matching.

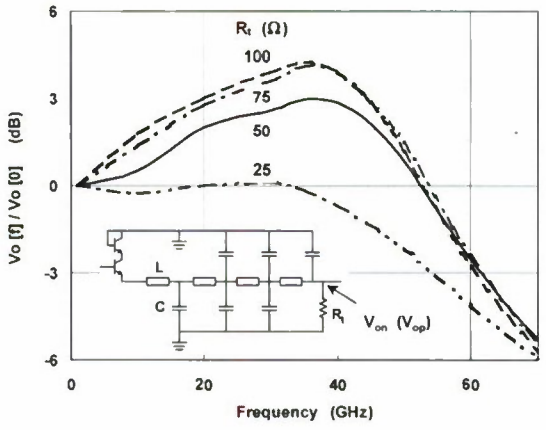


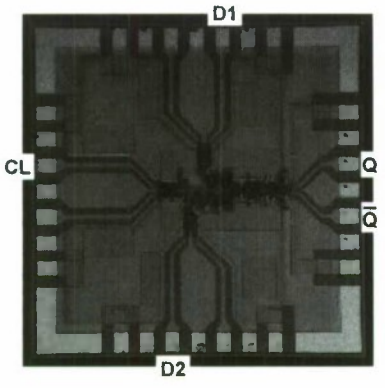
Fig. 4. Frequency dependencies for difference between differential clock line outputs, $V_o = |v_{op} - v_{on}|$, for terminating resistances of 25, 50, and 100 Ω, obtained by using simulation. The inset is an equivalent circuit model of the clock line used in the simulation.

used a *V*pp of greater than 500 mV in this design.

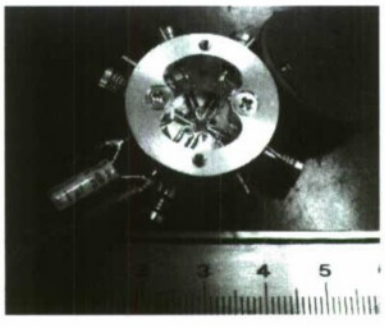
We designed the clock buffer configuration in the MUX very carefully. The clock lines have six fanouts, including two latches in the MS-DFF, three latches in the MSM-DFF and the selector. All of these must operate at high speed. Conventionally, two differential clock signal lines from a clock buffer are divided into three differential lines followed by three separate buffers. Although this configuration is good for high-speed operations, it increases the power dissipated by the three buffers as well as the design layout complexity. To maintain a high operating speed while suppressing power dissipation and layout complexity, we used the novel clock buffer configuration shown in middle part in Fig. 3. In this

configuration, a pair of differential-signal lines drives six fanout blocks passing through microstrip lines. The clock signals were able to operate at high speeds because we used broadband impedance matching for the microstrip transmission lines with capacitor and inductor components and resistors at the current source acting as terminating resistors. Figure 4 shows the frequency dependencies of the difference between differential clock line outputs, $V_0 = |v_{op} - v_{on}|$, for terminating resistances of 25, 50, 75 and 100 Ω. These dependencies were obtained by simulations performed by using an equivalent circuit model that corresponds to the clock line configuration shown in the inset. The lengths of clock lines *L1*, *L2*, *L3*, and *L4* are 76, 82, 82, and 30 μm, respectively, so that the length of the data lines is minimized in the layout. The width of the clock lines is 5 μm and the gap between the differential lines is also 5 μm. We found that a terminating resistance of 50 Ω was best considering the increased 3-dB-down bandwidth and suppressed peaking characteristics of V_0 needed for stable operation. The power dissipation of the clock buffer in this design is 292 mW, while the power dissipation in the conventional design is 415 mW.

Large margins were left both in the internal logic swings and in the output voltage. In order to guarantee normal operation of the internal circuits even when assembled in a module (where the inductance of the wire bonds could have undesirable effect), the internal logic swings in the DFFs and selector were set to as large as 300 mV. The output voltage of the main amplifier was set to greater than 500 mV to counter the decay caused by module assembly and to allow for practical use.



(a)



(b)

Fig. 5. Fabricated 2:1 MUX chip with a size of 2×2 μm² (a) and assembled MUX module with five V-connectors (b).

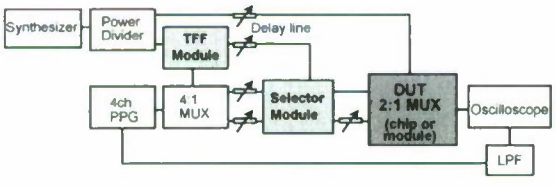


Fig. 6. Setup for measuring ultrahigh-speed operation of 2:1-MUX chip and module.

IV. Results and Discussion

Figure 5 shows photographs of a 2:1 MUX chip with a size of 2 × 2 μm² (Fig. 5 (a)) and an assembled MUX module with five V-connectors (Fig. 5 (b)). The high-bit-rate operations of chip and module DUTs were tested using the setup shown in Fig. 6. In the case of on-wafer measurements, 65-GHz RF probes were used. The output waveforms of the DUTs were measured by using a sampling oscilloscope with a precision time base and a 70-GHz bandwidth sampling head. Aside from conventional equipment such as a synthesizer, a power divider, a 4-channel PPG, and a 4:1 MUX, we also used a 2:1 selector module [6] and a frequency divider (TFF: toggle flop-flop) module. The selector and TFF chips were fabricated by using the same DHBT IC process as that of the MUX chip, and both modules were essentially the same as the MUX module. We confirmed that the TFF module operated stably up to 62 GHz and that the selector module provided clear eye openings in output waveforms with a 520-mV amplitude at 100 Gbit/s. The maximum amplitude of the sinusoidal signals measured just before feeding the signals into the MUX IC was 400 mV at 60 GHz and 530 mV at 50 GHz. These values were limited by the synthesizer's output power capability, the insertion of a power divider, and cable loss in the high-frequency region.

Figure 7 shows the output waveforms measured at 120 Gbit/s with a bias of −3.4-V V_{EE} (1.27-W P_{dis}) using the MUX chip (Fig. 7. (a)) and those measured at 113 Gbit/s with a bias of −3.5-V V_{EE} (1.4-W P_{dis})

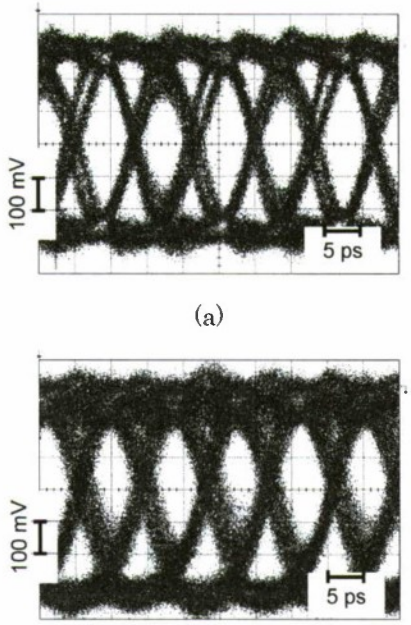


Fig. 7. 120-Gbit/s waveforms output from the MUX chip (a) and 113-Gbit/s waveforms output from the MUX module.

using the MUX module (Fig. 7 (b)). Vpp and the rms jitter were 520 mV and 770 fs, respectively, for the chip, and 514 mV and 979 fs for the module. It was also confirmed that the values for the chip and the module at 100 Gbit/s under the above-mentioned bias conditions were 540 mV and 530 fs, and 556 mV and 748 fs, respectively. The dominant factor that restricts the maximum operating bit rate is the reduced amplitude of the clock fed into the MUX.

Although the eye openings are clear in both Fig. 7 (a) and Fig. 7 (b), the waveforms of the module are inferior to those of the chip. The main reason for the difference in the waveforms is that the reduced-amplitude clock signals were degraded by loss in the V-connectors and transmission lines on the quartz substrate in the module at such high frequencies.

V. Summary

We designed and fabricated a 2:1 MUX with a retiming function using our own InP/InGaAs/InP DHBT process, which is characterized by a passivation ledge structure around the emitter mesa, high-speed operation even under low bias conditions, and a high breakdown voltage. In the MUX design, a clock buffer configuration was devised for reducing power dissipation and layout complexity and increasing the operating speed, and margins were left in the internal logic swing and output amplitude to provide for module assembly. After on-wafer measurements, the MUX chip was assembled in a module using V-connectors to enable easy use.

When measured on the wafer, the MUX operated at 120 Gbit/s with a P_{dis} of 1.27 W and an output amplitude of 520 mV. When assembled in a module, the MUX operated at 113-Gbit/s with a Vpp of 514 mV and a P_{dis} of 1.4. To our knowledge, the operating speed of 113-Gbit/s is the fastest ever reported for a MUX module.

Acknowledgments

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SENSITIVITY OF A 20-GS/s InP DHBT LATCHED COMPARATOR

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Abstract

We present simulations and measurements of the sensitivity of a master-slave emitter-coupled logic (*ECL*) latched comparator implemented in an InP/GaInAs DHBT technology. The circuit exhibited simulated and experimental sensitivities of 11.5 mV and 17 mV, respectively, at a clock rate of 20 GHz, with no preamplifier

I. Introduction

Analog-to-digital converters (*ADCs*) based upon heterojunction bipolar transistor (*HBT*) technologies have reached record sampling rates (1-4). An important concern in the design of ADCs is avoiding metastability at the output of the comparators (5). The probability of metastability is determined by the sensitivity of the comparator, which may be defined as the minimum voltage difference at the input at which metastability is avoided. The evaluation of the sensitivity of a given comparator by simulation, and its comparison to measured values, is thus desirable information for the design and diagnosis of an ADC.

Measuring the sensitivity at high bit rates is not an easy task. For example, a 16-GS/s SiGe latched comparator was evaluated in (6) using a fast logic analyzer and a sensitivity of 20 mV was indirectly inferred. Here, we present sensitivity simulations and experimental evaluation of a 20-GS/s InP DHBT latched comparator. An analog experimental setup to evaluate the sensitivity at this high bit rate is described.

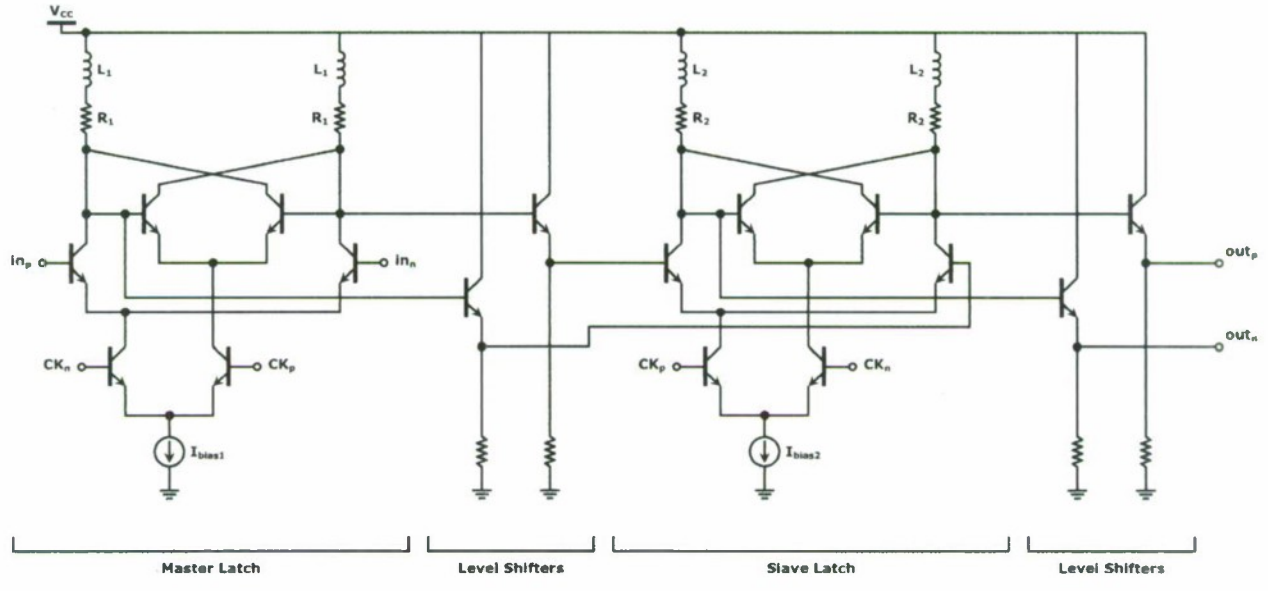

Fig. 1. Schematic circuit diagram of the comparator

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Fig. 2. Microphotograph of the circuit

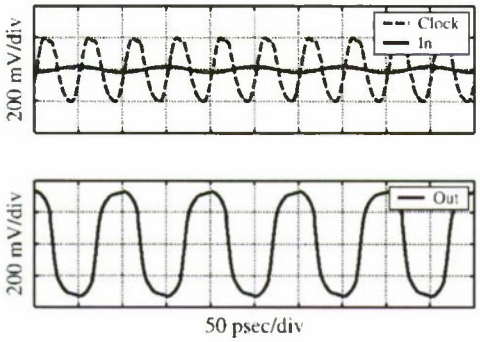


Fig. 3. Simulated waveforms of the circuit at 20 GS/s

II. Comparator Design

The circuit diagram of the master-slave emitter-coupled logic (*ECL*) comparator (7) is shown in Fig. 1. The master D-latch incorporates a 30 Ω load resistance and a peaking inductance of 240 pH. It is followed by common collector level shifters. The slave D-latch includes smaller load inductors, since sensitivity enhancement is less crucial in the slave latch. Level shifters at the output isolate the slave D-latch from the load. The input signal is not amplified by a preamplifier in order to directly evaluate the sensitivity of the comparator. The comparator was designed for a clock frequency of 20 GHz. Transmission lines were used for clock distribution and for the implementation of inductors. If spiral inductors are used instead of transmission lines in order to reduce chip size, their parasitic resistance should be subtracted from the load resistors (8).

The comparator was fabricated by the Fraunhofer Institute for Applied Solid State Physics (*IAF*) using their InP/GaInAs DHBT technology (9). A microphotograph of the chip is shown in Fig. 2. Total die area is 1x1 mm^2.

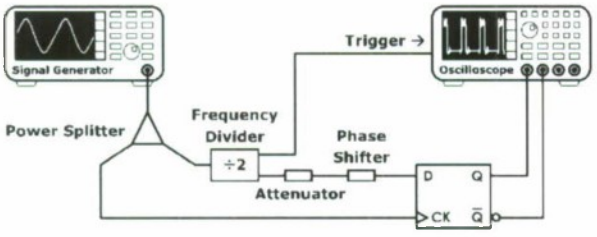
III. Comparator Characterization

The circuit was simulated at a 20 GHz clock rate and 10 GHz input signal. When the clock edges were aligned with the signal crests, the output toggled its value every clock cycle, as shown in Fig. 3. Since the definition of sensitivity is not unique in the literature we have arbitrarily defined the sensitivity as the input voltage for which the output amplitude was reduced by a factor of two. The simulated sensitivity was 11.5 mV.

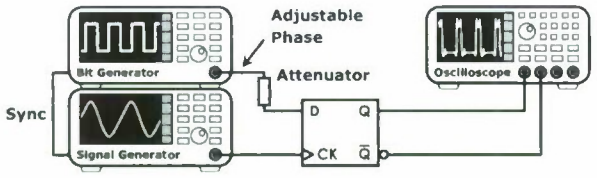
Experimental evaluation of the sensitivity was carried out along the same lines as in the simulations. To minimize the effect of jitter of lab instruments on output sampling, we have used the fully synchronized setup shown in Fig. 4a. The clock signal was generated by a Wiltron 68177B synthesized sweep generator, and divided by a power splitter. One of the splitter's outputs was used for clocking the comparator, and the other was applied to a Fraunhofer IAF ASD201M frequency divider. The differential output of the divider was used both for the input signal and for triggering an oscilloscope. In order to reduce the effect of clock kickback in the master latch, the single-ended clock was introduced at the positive clock input (CK_p), and a DC voltage at the negative input (CK_n). The input signal was applied to the negative input (inn) in a similar manner. The outputs were sampled by an Agilent 86100B oscilloscope. The supply voltage was 6 V, the input DC voltage was 3.5 V, and the clock DC voltage was 2 V. The total power consumption was 420 mW, where the comparator itself consumed 336 mW, and the auxiliary biasing circuits 84 mW.

Shown in Fig. 5 is the output waveform of the circuit when being tested by applying a 20 GHz clock signal and 10 GHz input signal. Although this measurement setup provides very good synchronization between the various signals, control over the input amplitude is possible only by external fixed attenuators. We have therefore used another setup to observe the sensitivity of the comparator.

The sensitivity measurement setup is shown in Fig. 4b. The input signal was generated by an Anritsu MP1758A pulse pattern generator. The MP1758A offers a convenient way to adjust the signal's phase, but limited control over the amplitude. However, using various attenuators we could cover the entire range from 1 mV to 1 V. The outputs were sampled



(a)



(b)

Fig. 4. Measurement setups: (a) fully-synchronized setup (b) sensitivity measurement setup

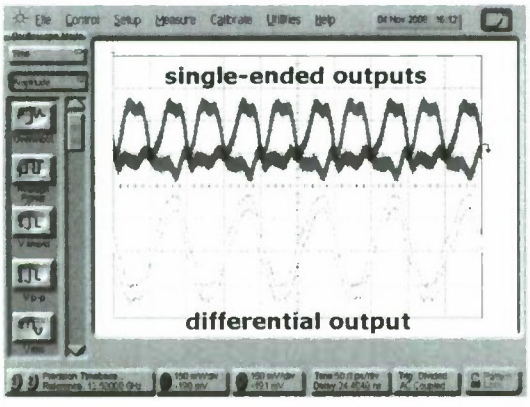


Fig. 5. Measured waveforms of the comparator outputs at 20 GS/s with input amplitude of 100 mV, using the fully synchronized setup

by an HP 83480A oscilloscope, which was triggered by one of the bit generator's output.

To measure the sensitivity of the comparator the input amplitude was gradually reduced from 500 mV until the output voltage of the comparator circuit dropped by a factor of two. The lowest input voltage at which the comparator toggled at half amplitude was 17 mV; at an input of 16 mV no toggling was observed, as shown in Fig. 6. As evident in Fig. 6, the oscilloscope triggering suffered from considerable jitter noise. The noisy data were smoothed using the averaging sliding window method, where the window width was 5 psec.

IV. Conclusion

The sensitivity of an InP DHBT-based 20-GS/s master-slave ECL comparator, with no preamplifier, was simulated and evaluated. The differential input voltage at which the simulated output amplitude dropped by a factor of two was 11.5 mV. Experimentally, the differential input voltage below which the comparator stopped toggling was 17 mV. If a preamplifier with a voltage gain of 26 dB at 10 GHz is introduced, we estimate that the sensitivity will improve to below 1 mV. In this case, a 9-bit ADC can be implemented, assuming a differential dynamic range of 1 V peak-to-peak.

Acknowledgement

The authors would like to thank Thomas Mayer and Dr. Josef Rosenzweig of Fraunhofer IAF for their help in the measurements, and Dr. Michael Schlechtweg for his continuous support of this work. Also, thanks are given to Prof. Boris Murmann of Stanford University for his helpful advice and to Dr. David Rosenfeld for supporting the project.

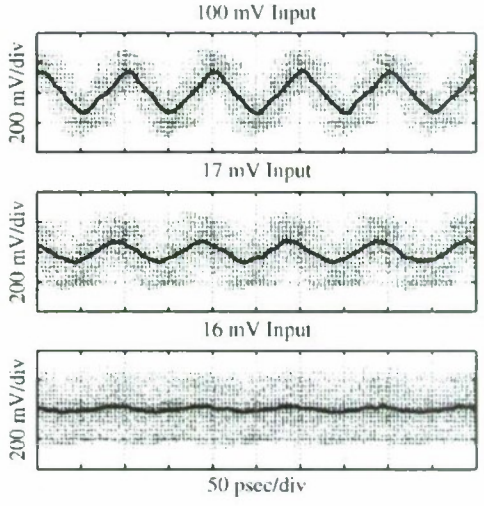


Fig. 6. Measured waveforms of the comparator differential output at 20 GS/s at various input amplitudes, using the sensitivity measurement setup. Data are presented both before and after smoothening by a 5 psec-wide sliding window.

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RELIABILITY STUDY ON InP/InGaAs EMITTER-BASE JUNCTION FOR HIGH-SPEED AND LOW-POWER InP HBT

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Abstract

The reliability of sub-micrometers InP-based heterostructure bipolar transistors (HBTs), whieh are being applied in over-100-Gbit/s ICs, was examined at high current injection conditions. These HBTs had a ledge structure and an emitter electrodc consisting with a refractory metal of W, which suppressed surface degradation and metal diffusion, respeetively. We eondueted bias-temperature (BT) stress tests in several stress conditions of eurrent densities, J_c, up to 10 mA/μm^2 in order to investigate the stability of InP/InGaAs emitter-base (E-B) junction. At 10 mA/μm^2 operation with the junction temperature of 210 °C, de current gain, β, was stable for 1000 h. The aetivation energy for the reduction of β, however, decreased to 1.1 eV, which is suggesting the degradation of the emitter-base (E-B) junetion. For the reliability of sub-micrometer, high-speed and low-power InP HBTs at high eurrent densities, stability around the E-B junetion has beeome more dominant.

I. Introduction

The progress in the research and development of InP HBT technologies has given a boost to their introduction into optical communications systems [1, 2]. We confirmed lifetime of over 1 x 10^8 h for InP HBTs for 40-Gbit/s ICs with passivation ledge structures [3] and with refractory emitter electrodes [4]. On the other hand, we have also developed reliable InP HBTs with high-frequency performance up to f_t and f_{max} of over 300 GHz [5, 6, 7]. These devices have sub-micrometer dimensions aiming high-speed and low-power operation of over-100-Gbit/s ICs. For the sub-micrometer HBTs, we must attain reliability in high current injection conditions, where devices reach near maximum operation speeds and which are essential for ICs in operating at high-speed. This paper reports reliability studies on sub-micrometer InP HBTs at high J_c and shows the J_c dependence of degradation characteristics.

II. Experiments

We examined HBTs with a 0.6-μm-wide and 3-μm-long emitter. The device cross-sectional structure is shown in Fig. 1. The device fabrication sequence is as follows, first, W-based emitter metals are deposited. Next, dry etching is performed to form the emitter mesa structure. The emitter layer is used as a ledge layer whose thickness is 15 nm [7]. The surface of the ledge layer is covered with SiN films for passivation [6]. The average β is around 60, which indicates that the recombination current at the periphery of the emitter is suppressed by the passivation ledge.

The emitter metal configuration was Ti/W/Ti/Pt/Au. The

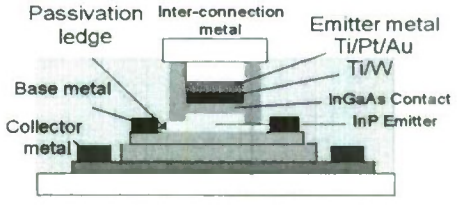

Fig. 1. Cross-sectional schematic view of an InP HBT.

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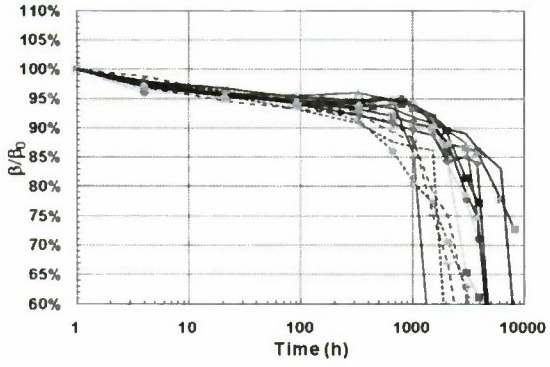
use of W to prevent Ti/Au diffusion has been confirmed [4]. We conducted BT stress tests in several J_c stress conditions from 2 to 10 mA/μm^2 and at ambient temperatures in the range of 100 to 195 °C.

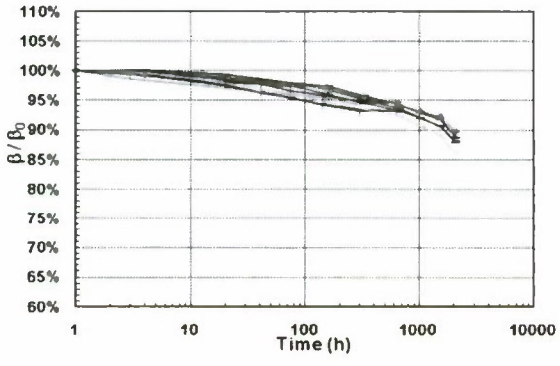
III. Results and discussion

A. Two modes of degradation at high current densities

Figure 2 shows the timewise change in β at J_c = 1 mA/μm^2 for several devices stressed continuously at J_c of



(a)



(b)

Fig. 2. Timewise change in β at Jc = 1 mA/μm^2 for 0.6x3-μm HBTs under J_c stress of (a) 10 and (b) 5 mA/μm^2. The device junction temperature was about (a) 210 and (b) 225 °C.

(a) 10 and (b) 5 mA/μm^2 and at the device junction temperature, T_j, of about (a) 210 and (b) 225 °C, respectively. Even at extremely high current density of J_c = 10 mA/μm^2, degradation in β was less than 15 % for 1000 h. After that, β decreased rapidly. The change in the current voltage (I-V) characteristics of a typical sample in Fig. 2 (a) is shown in Fig. 3. The base current, I_B, at low emitter-base voltage, V_{BE}, increased significantly with time. The increase in I_C for fixed V_{BE} began after 2000-h BT stress. These changes in I_B and I_C suggested degradation of the E-B junction in the intrinsic region. This is probably due to the increase in the recombination tunneling current. [8], and to

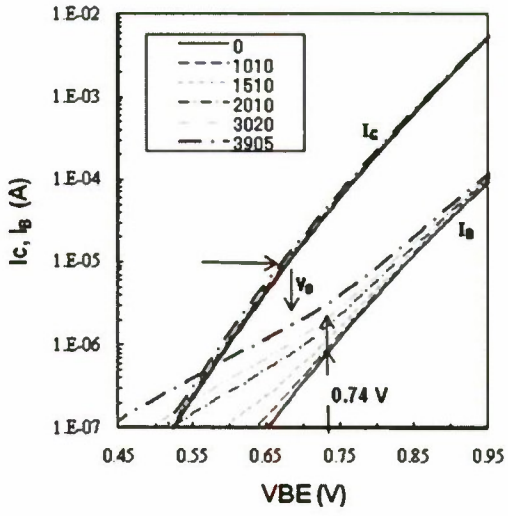


Fig. 3. I-V characteristics of a typical HBT stressed at J_c = 10 mA/μm^2.

the change in the turn-on voltage.

The activation energy for the reduction of β was evaluated for sub-micrometers InP HBTs. The criterion was a 15 % reduction of β. Temperature dependence of the median time, t_{50}, for the critical times is shown in the Fig. 4. For the BT test at 5 and 7 mA/μm^2, the activation energy E_a was 1.7 eV, which is consistent with our previous result for HBTs with a 1-μm emitter [6]. This E_a was explained as surface recombination at the external base region. However, t_{50} for HBTs tested at J_c of 10 mA/μm^2 did not follow the tendency observed at 5 and 7 mA/μm^2. The increase in the recombination tunneling current in the intrinsic E-B junction, which was shown in Fig. 3, probably caused this lowering of E_a.

The temperature dependence of the increase in I_B, which was significant at stress of 10 mA/μm^2, was then analyzed. The criterion was a 0.5-μA increase in I_B at V_{BE} = 0.74 V. The temperature dependence of the median time is shown in Fig. 5.

For J_c of 7 and 10 mA/μm^2, the activation energy for increasing I_B was around 1.1 eV, which was lower than that for the β reduction. This value agrees the E_a for β reduction at J_c of 10 mA/μm^2. For devices stressed at J_c of 7 mA/μm^2, the E-B junction degradation must appear after much longer stress time.

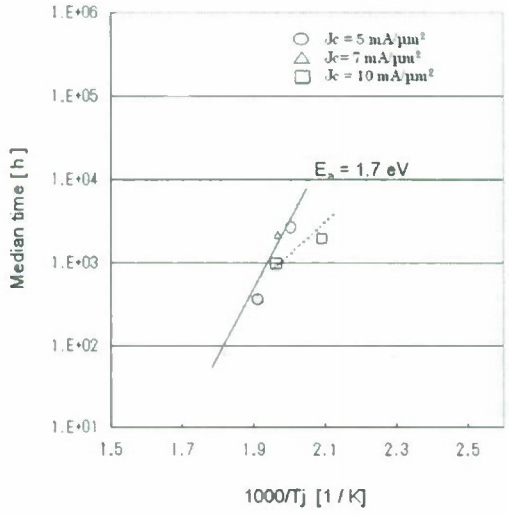


Fig. 4. Temperature dependence of the median lifetime for a 15% reduction of β at J_c = 1 mA/μm^2.

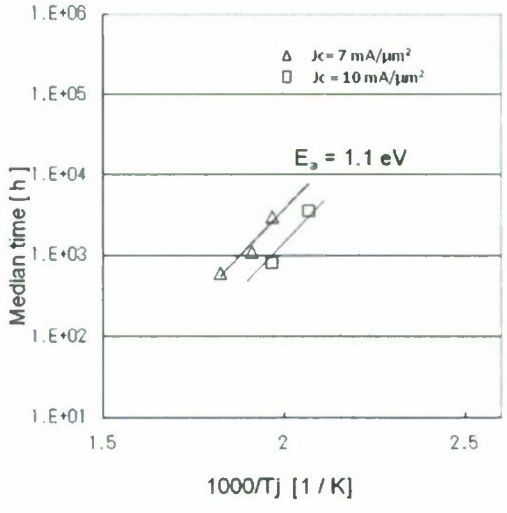


Fig. 5. Temperature dependence of the median lifetime for a 0.5-μA increase in I_B at V_{BE} =0.74 V.

B. E-B junction degradation in the intrinsic region

Since the increase in the tunneling recombination current

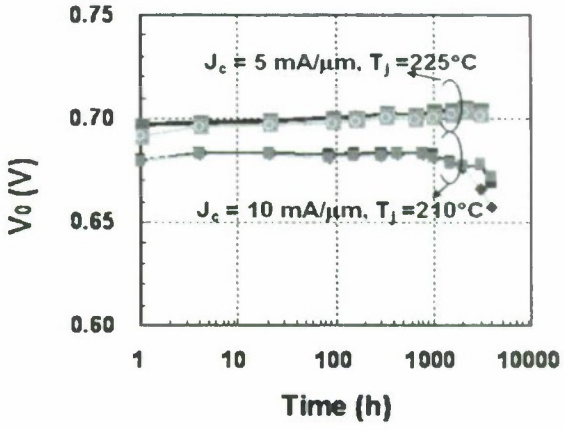


Fig. 6 .Timewise change in V_0.

in I_B means the degradation of the E-B junction, the turn-on voltage must be shifted later. We defined V_0 as the V_{EB} at the collector current, I_C, at 1 μA, which is shown in Fig. 3. Figure 6 shows the time-wise change in V_0 for the devices in the Fig. 2(a) and (b) at J_c of 10 and 5 mA/μm^2, respectively.

The reduction of V_0 began after 2000 h for J_c of 10 mA/μm^2, whereas V_0 did not drop for J_c of 5 mA/μm^2

Figure 7 shows the cross-sectional transmission electron microscopy (TEM) image of a degraded device, which had similar I-V characteristics after a 1990-h stress at J_c of 7

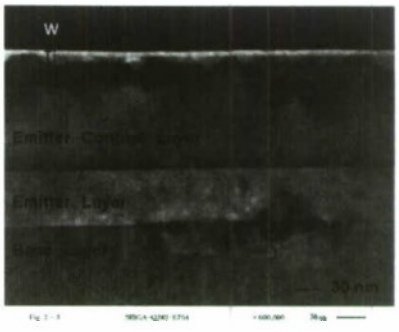


Fig. 7. TEM image of the HBT after stress at J_c of 7 mA/μm^2 and T_j = 322°C for 1990 h.

mA/μm^2 and T_j = 322 °C. Some defects at the EB junction are observed. The degradation of the junction became critical at high current densities and more dominant in sub-micrometer HBTs.

The quality of the interface between the emitter and the base layer became dominant at high current densities, so its improvement is one of the ways to enhance the reliability at high current density.

IV. Conclusions

In summary, we examined the reliability of sub-micrometers InP HBTs at high current densities. We conducted bias-temperature stress tests in several J_c stress conditions up to 10 mA/μm^2. At J_c = 5 and 7 mA/μm^2, the main degradation mechanism was found to be surface recombination, because the activation energy was 1.7 eV, which is the same as for 1-μm InP HBTs. When the stress current density was 10 mA/μm^2, degradation of the EB junction plays the main role in determining the device lifetime.

The degradation of the E-B junction was confirmed by a TEM analysis and by changes in the I-V characteristics, which showed an increase in the base current and the shift in the emitter-base voltage at I_C = 1 μA . For this degradation, the activation energy was about 1.1 eV, which was due to the rapid decrease in the lifetime for β reduction.

For the devices with a ledge structure and refractory metal of W, primitive failure modes were suppressed, so the degradation around the EB junction became critical. We need to further improve the quality of the interface of the emitter and the base layer.

Acknowledgements

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ADVANCES IN THE GROWTH AND PERFORMANCE OF ANTIMONIDE-BASED MID-INFRARED INTERBAND CASCADE LASERS

W. W. Bewley, C. L. Canedy, C. S. Kim, M. Kim, J. R. Lindle, J. Abell, I. Vurgaftman, and J. R. Meyer

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We discuss the growth and state-of-the-art performance characteristics of mid-infrared interband cascade lasers. Broad-area devices with 5 active stages display pulsed threshold current densities as low as 400 A/cm^2 at room temperature, owing to an unexpectedly strong suppression of Auger recombination. New designs also produce lasers with internal losses as low as ≈ 6 cm^{-1} at room temperature. We also study the performance of narrow ridges that dissipate heat efficiently for high-temperature cw operation. The degradations of the threshold current density and differential slope efficiency are modest until the ridge width is decreased to 3 μm. A 13-μm-wide uncoated ridge produces up to 45 mW of cw power at 293 K, and displays a maximum wall-plug efficiency of 3.5%. A 5-μm-wide 3-mm-long ridge without any facet coatings operates cw to 345 K, which is a new record high temperature for any semiconductor laser emitting in the 3.0-4.6 μm spectral range.

I. INTRODUCTION

The interband cascade laser (ICL) (1-3) based on antimonide type-II active regions is currently the leading semiconductor source technology for the important 3-4 μm spectral window. Other competing approaches such as the intersubband quantum cascade laser (QCL) (4-5) and type-I quantum-well diode laser (6-8) cover the shorter-wavelength and longer-wavelength sides of the window, respectively, but still suffer from limitations within the window in spite of recent performance improvements.

In the ICL, electrons make optical transitions in the type-II "W" active region (9) and are subsequently removed from the valence band at the structure's *other* type-II interface, between the electron and hole injectors. Upon dropping a voltage somewhat larger than the photon energy over a single stage, the electrons are then reinjected into the next stage so that the same current flows through all the active wells. Therefore, just as in the case of the QCL, the ICL features a series connection of all the active transitions as opposed to the effectively parallel connection of the wells in the better-known multiple-quantum-well diode laser. The lower current is combined with a higher bias voltage, whose minimum value is the photon energy multiplied by the number of stages.

Recently, an ICL emitting at 3.7 μm operated to a maximum temperature of 335 K in continuous-wave (cw) mode (10). This achievement was made possible by careful optimization of the design, growth, and processing of the structure. In this article, we will describe the growth procedures (Section II), implications of the pulsed ICL characteristics on the Auger recombination rates and internal waveguide loss (Section III), and the cw performance of narrow-ridge devices (Section IV). A summary of the results will be presented in Section V.

II. INTERBAND CASCADE LASER GROWTH

Solid-source MBE growth was performed using a compact 21T Riber system equipped with both As and Sb crackers, as well as dual Indium cells for greater flexibility (11). The cracking zones of the group V sources were held at temperatures above 900 °C, to provide dimer or monomer atomic species. The ICLs with 5 stages were grown on Te-doped (~ 1 x 10^{18} cm^{-3}) epi-ready 2" GaSb substrates at a growth temperature of 445 °C. These temperatures were measured using an IRCON optical pyrometer whose emissivity setting was calibrated to the (1 × 3) to (1 × 5) surface reconstruction transition for GaSb (~ 414 °C for an Sb_2 flux of 1 ML/s) (11). Growth rates for the group-III species were deduced from *in situ* reflection high-energy electron diffraction (RHEED) intensity oscillations. These rates were also referenced to the various SL periods in the ICL, as determined from satellite peak positions in the high-resolution X-ray diffraction spectra of calibration structures. The X-ray spectra were also used to assess lattice matching of the various superlattice layers. Fine tuning of the strain compensation was achieved by adjusting the Sb-soak time (typically 0.1–0.5 s) at the arsenide-to-antimonide SL interface, for fixed group V fluxes and growth rates. Although the arsenic valve was toggled down during the antimonide layer growth (by about a factor of 100 in beam-equivalent pressure), in order to reduce the amount of arsenic incorporation, the antimony valve remained open during the arsenide layer growth. The group V/III flux ratio was held in the range 1.5–2 except when growing the "W" QW region. The designs of samples commencing with T080828 were further altered with the specific goal of reducing the internal loss.

At the conference, we will present the characteristics of interband cascade electroluminescent samples, in which only the IC active region is grown, as a function of the most

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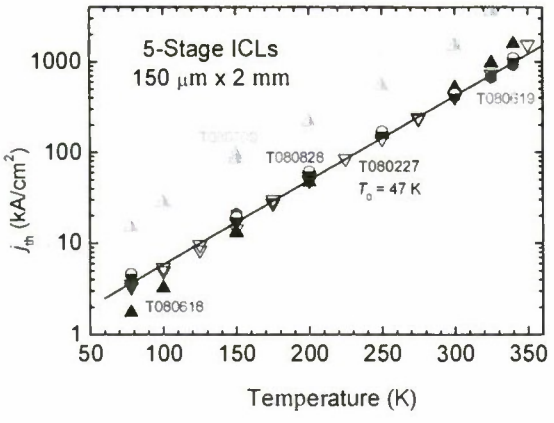

Fig. 1. Threshold current densities *vs.* temperature for five broad-area ICLs with 2-mm-long cavities. The room-temperature center emission wavelengths of the samples are: 3.69 μm for T080227, 4.18 μm for T080618, 3.24 μm for T080619, 5.02 μm for T080709, and 3.67 μm for T080828. The line represents T_0 = 47 K, the characteristic temperature for T080227 over the 78-320 K temperature range.

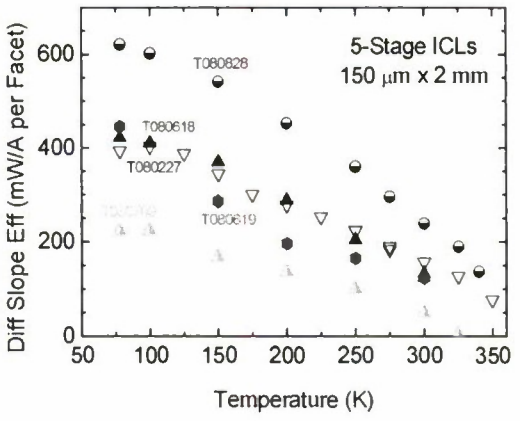

Fig. 2. Pulsed differential slope efficiencies per uncoated facet *vs.* temperature for the samples of Fig. 1. The pulse length was 1 μs.

important growth parameters such as growth temperature, the group V/III flux ratio, *etc.*

III. PULSED CHARACTERIZATION AND ANALYSIS OF INTERNAL LOSS AND AUGER RATES

We obtain the most reliable information about "intrinsic" device performance, uncomplicated by lattice heating and the sidewall quality of narrow ridges, by measuring the pulsed properties of broad-area lasers. Since cavity-length measurements are too laborious to perform on a large number of samples, we will assume internal efficiencies η_i based on those obtained from a detailed temperature-dependent investigation of an earlier 5-stage ICL sample (12). In that case, η_i decreased gradually with increasing temperature, from 83% at 78 K to 64% at 300 K. Figure 1 plots the temperature dependences of threshold current densities for several 5-stage samples with the room-temperature emission wavelengths indicated in the caption. In order to minimize lattice heating, the characterizations employed 100-350 ns pulses for $T \geq 300$ K, 1 μs pulses in the 150-300 K temperature range, and cw injection at the lowest temperatures (where pulsed measurements are impractical due to the very low currents). The threshold current densities at 78 K were extremely low, e.g. 1.7 A/cm^2 for T080618, which makes them effectively negligible for devices producing significant optical powers.

The room-temperature thresholds of ≈ 400 A/cm^2 for the best ICLs emitting near 3.7 μm are comparable to those measured previously for 10-stage ICLs with higher doping levels in the optical cladding layers. The threshold current densities exhibit surprisingly little variation over the 3.0-4.2 μm spectral range, which is attributable to a very weak dependence of the Auger coefficient on wavelength as discussed below. We do, however, find an increase of j_{th}(300 K) at the longest wavelengths, *e.g.*, ≈1.5 kA/cm^2 for λ = 5.0 μm. Over the entire T = 78-300 K range the data imply characteristic temperatures of $T_0 \approx$ 37-49 K, although these are not the best predictors of high-T cw performance since j_{th} is governed by different non-radiative mechanisms at low and high temperatures (Shockley-Read *vs.* Auger). Nevertheless, the T_0 values near ambient are comparable to those derived for the full temperature range, with the minor variations correlating well with the Auger coefficients deduced below.

The two primary figures of merit for achieving high-temperature cw operation are the threshold power density (P_{th}), which is obtained from the product of j_{th} and the bias voltage at threshold (V_{th}), and the rate of the threshold power density's increase above room temperature. Although there is some variability, the best ICL structures grown at NRL do not require any extra voltage beyond the transparency value of $N \times \hbar\omega$, plus the ohmic contribution ($V_\Omega = j_{th} \times \rho_s^{th}$, where at threshold the differential series resistivity ρ_s^{th} is typically in the range of 0.7-1.1 mΩ–cm^2 at 300 K) and an additional voltage of order $k_B T$ per stage needed to overcome losses.

Figure 2 plots temperature-dependent differential slope efficiencies for the samples of Fig. 1. Note that the redesign of T080828 quite effectively increases the efficiency at both low and at high temperatures. For ICLs emitting at λ ≈ 3.7 μm, typical dP/dI values of 450-490 mW/A at 78 K and 140-180 mW/A at 300 K before the redesign increased to 621 and 239 mW/A after. For ICLs emitting near 3.7 μm, the internal loss before the redesign was as low as 8.7 cm^{-1} but more typically ≈ 12 cm^{-1}. After the redesign, α_i(300 K) decreased to the range 5.7-8.7 cm^{-1}. There is little dependence on wavelength between 3.2 and 4.2 μm, although more work is needed to confirm the preliminary indication that the internal loss begins to increase with wavelength for λ > 4.2 μm.

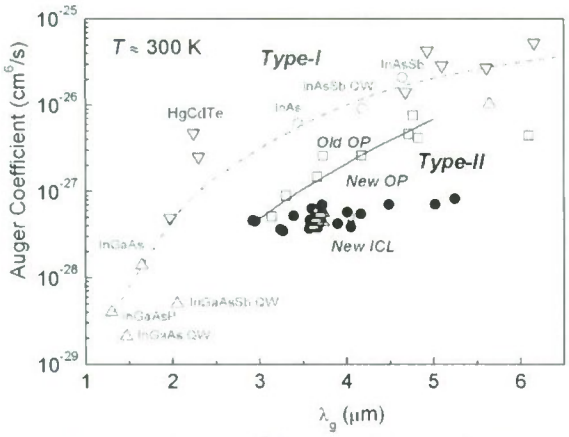

Fig. 3. Room-temperature Auger coefficient *vs.* emission wavelength (lasers) or effective wavelength corresponding to the energy gap (other devices), for a wide variety of pulsed, broad-area ICLs.

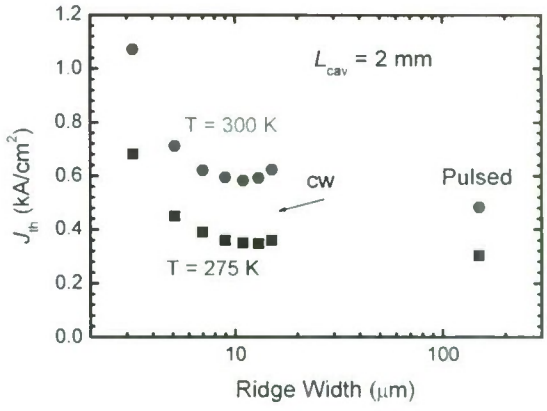

Fig. 4. Room-temperature Auger coefficient *vs.* emission wavelength (lasers) or effective wavelength corresponding to the energy gap (other devices), for a wide variety of pulsed, broad-area ICLs.

The derived internal loss, measured threshold current density, and calculated modal gain can be combined to estimate the Auger coefficient (γ_3) for each structure. Results at room temperature are plotted *vs.* wavelength in Fig. 3 for a much larger sampling of 3-, 5-, and 10-stage ICLs with a variety of active-region designs. The additional data for bulk and type-I QW materials, and for optically-pumped type-II structures, are taken mostly from (13). Clearly, at most λ the derived Auger coefficients for type-II QWs in ICLs are much lower than had been anticipated based on the earlier optically-pumped laser and photoconductivity experiments. Furthermore, the dependence on wavelength is much weaker than was implied by the earlier work. Both of these findings are highly beneficial to the prospects for high-temperature lasers operating in the 3.0-4.2 μm window. The observed γ_3 are 4-6 × 10^{-28} cm^6/s in this range, with any trends being weaker than the rather modest variations between samples. When λ is further increased to 4.5-5.0 μm, the derived Auger coefficients increase slightly to ≈ 7 x 10^{-28} cm^6/s.

In the next section, we will examine the narrow-ridge characteristics of an ICL sample (T091111) emitting at 3.45 μm at 300 K, with performance characteristics comparable to the best ICLs presented above. The pulsed threshold current density at room temperature for this sample was 482 A/cm^2, which combined with the threshold voltage of 2.46 V yields a threshold power density of P_{th} = 1.19 kW/cm^2. At T > 300 K, the characteristic temperature associated with threshold power density was T_{0P} = 31 K. The external differential slope efficiencies were dP/dI = 601 and 188 mW/A per facet at 78 and 300 K, respectively, which correspond to external differential quantum efficiencies (from two facets) of 59% and 21%. We also derive an approximate internal loss of 9.2 cm^{-1} at 300 K for this sample.

IV. CW PERFORMANCE OF NARROW-RIDGE DEVICES

Narrow ridges with widths 3.2 to 15.1 μm were fabricated from T091111 by photolithography and reactive-ion etching (RIE), using a Cl-based inductively-coupled plasma (ICP) process that again stopped at the GaSb SCL below the active QWs. The ridges were subsequently cleaned with a phosphoric-acid-based wet etch to minimize damage from the ICP RIE. This wet etch was observed to induce some selective undercutting of the AlSb barriers in the active region, owing to preferential etching by the phosphoric acid. A 200-nm-thick Si_3N_4 dielectric layer was deposited by plasma-enhanced chemical vapor deposition, and a top contact window etched back using SF_6-based ICP. Next, 100 nm of SiO_2 was sputtered to block occasional pinholes in the Si_3N_4. The ridges were metallized and electroplated with 5 μm of gold to improve the heat dissipation.

Figure 4 plots cw threshold current densities for the series of narrow ridges with 2-mm-long cavities mounted epi-side up at T = 275 (blue points) and 300 K (red points). Owing to the trade-off between sidewall effects and lateral heat dissipation, the cw J_{th} at 300 K exhibits a minimum at w = 11.1 μm, where the threshold of 582 A/cm^2 is only 21% higher than the pulsed result for the broad stripe. Since heat removal becomes less critical with decreasing temperature, at T = 275 K the ridge width corresponding to the minimum threshold shifts to 13.0 μm. On the other hand, the sharp J_{th} increase in very narrow ridges (*e.g.*, by nearly a factor of 2 when w = 3.2 μm) may be attributed to surface recombination and current leakage at defects in the processed sidewalls.

We also observe an increase in the threshold voltage as the ridge width is reduced. Most of the increase in V_{th} for the narrowest ridge widths (at T = 300 K, from 2.26 V for w = 11.1 μm to 2.46 V for w = 3.2 μm) is explained by the higher J_{th} for those devices. Since the change in V_{th} is quite small compared to that of J_{th}, the degradation in threshold power density (from P_{th}(300K) = 1.3 kW/cm^2 for w = 11.1 μm to 2.6 kW/cm^2 for w = 3.2 μm) is attributable primarily to the effects of sidewall damage on the threshold current density.

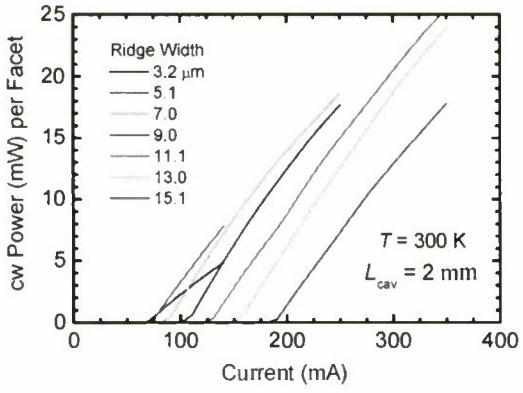

Fig. 5. CW output power per facet *vs.* current density for the narrow-ridge ICLs at $T = 300$ K. The cavity length is 2 mm for all the devices.

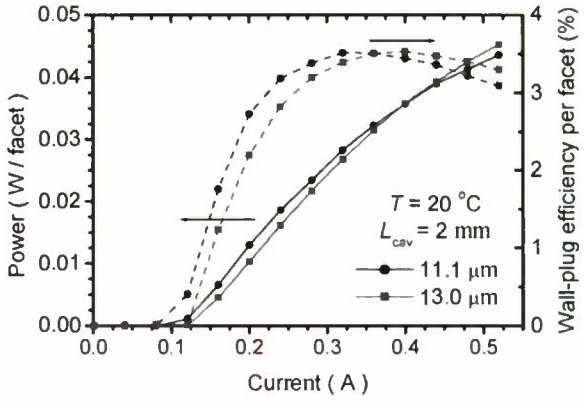

Fig. 6. CW output powers and wall-plug efficiencies per facet *vs.* current density for the 11.1- and 13.0-μm-wide ICLs with 2-mm-long cavities.

Figure 5 shows *L-I* characteristics for the seven ridges at $T = 300$ K. Owing to the competing effects of more efficient heat dissipation and greater leakage and optical losses in the narrowest ridges, the maximum differential slope efficiency of ≈ 140 mW/A is reached at intermediate ridge widths between 7.0 and 13.0 μm. This value is somewhat lower than for the broad-area device due to active-region heating. The lower slope efficiencies of 120 and 75 mW/A for the 5.1 and 3.2-μm-wide ridges, respectively, may be attributed to higher internal losses associated with the sidewalls.

Because wide ridges exhibit high thermal impedance per unit power density while narrow ridges suffer from excessive leakage currents and optical losses at the sidewalls, the output power and wallplug efficiency tend to peak at intermediate ridge widths. Figure 6 shows the cw *L-I* characteristics and wallplug efficiencies for the $w = 11.1$ and 13.0 μm ridges at $T = 20$ °C. Both devices reached similar maximum cw output powers of 44-45 mW per facet. The two devices also displayed similar maximum wall-plug efficiencies of 3.5%.

We have also carefully examined the spectral characteristics of the narrow ridges discussed in this section. The spectrum for the $w = 7.0$ μm ridge contains two distinct sets of longitudinal modes with spacing different by 0.6%, corresponding to the two lowest-order lateral modes. On the other hand, ridges with $w \leq 5.1$ μm display single-lateral-mode operation. Therefore, the latter are most likely to be useful for applications where single-mode emission is required. Since the performance penalty due to sidewall damage remains modest for ridges with $w \geq 5.1$ μm, we measured $T_{max}^{cw} = 345$ K (72°C) for a device with $w = 5.1$ μm, $L_{cav} = 3$ mm, and uncoated facets. This is a new record for semiconductor lasers emitting between 3.0 and 4.6 μm.

V. Conclusions

One significant discovery in this study is that the Auger non-radiative decay rates in these type-II structures are much lower than was expected based on prior experiments and theoretical projections. Auger coefficients extracted from the lasing thresholds and differential slope efficiencies are remarkably consistent, and display no statistically significant dependence on wavelength in the 3.0-4.2 μm window.

We have also demonstrated that the cw performance of narrow-ridge ICLs does not start to degrade except in the narrowest ridge of width 3.2 μm. Compared to all QCLs reported to date, the narrow-ridge ICLs described above require far lower input powers to achieve lasing (*e.g.* only 0.17 W at 300 K for the 5.1 μm single-lateral-mode device).

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InAsSb AND InPSb MATERIALS FOR MID INFRARED PHOTODETECTORS

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Abstract

III-V semiconductor materials are under active investigation for use as optical detectors in the mid infrared wavelength region from 3 to 12 μm. In this paper we summarize recent progress on the development of III-V materials for this application based on the material InAsSb. We first present the results of investigations in the use of strained balanced type II superlattices of InAsSb/InAs to extend the absorption wavelength of this material system beyond the limits of the maximum InAsSb bulk value. We present results on the growth of InPSb heterojunction structures with the aim of reducing thermal diffusion current and surface leakage. Finally we present some preliminary device results indicating the promise of this material system.

I. Introduction

III-V mid infrared photodetectors for pollutant sensing and focal plane arrays (FPA) have been under development for several years now. While HgCdTe detectors are now relatively mature and offer exceptional performance in FPA applications, there are several materials challenges with this material system such as costly substrates and challenging growth and fabrication technologies. As a result there is considerable interest in the development of III-V detectors with their readily available and relatively low cost substrates, and more straightforward doping and fabrication techniques. Some notable examples of mid IR FPAs that have been recently developed include short period type II GaSb/InAs superlattices [1] and InGaSb/InAs superlattices [2] grown on GaSb substrates and inter sub-band detectors grown on low cost GaAs substrates.[3] Among III-V materials, InAsSb has the lowest observed bandgap of all at 150 meV, corresponding to a wavelength of ~8.3 μm (Fig. 1). Unfortunately these long wavelengths cannot be exploited directly because of the lack of suitable lattice matched substrates. InAsSb alloys can be grown lattice matched to GaSb at a composition of x=0.09 corresponding to a 77K bandgap of 0.33 eV (3.7 μm). In a recent work we demonstrated a method for extending this by forming strain balanced superlattices consisting of alternating layers of compressively strained $InAs_{1-x}Sb_x$ (x>0.9) and tensile strained InAs, grown on a GaSb substrate.[4] Using this method we were able to demonstrate emission wavelengths from type II luminescence out to 10 μm for an Sb composition of only 0.27. In comparison, relaxed InAsSb exhibits a maximum emission wavelength of 8.3μm at a Sb composition of x=0.65.

In this work we discuss some of the issues involved in realizing optical detectors based on this material combination. First we review some of the properties of strain balanced InAsSb superlattices with the aim of achieving absorption wavelengths longer than are possible with lattice matched $InAs_{1-x}Sb_x$. Next we demonstrate some of the steps required to incorporate these layers in future devices. These include (1) the growth of InPSb/InAsSb heterostructures for suppression of thermal diffusion and leakage currents, (2) investigation of the properties of parasitic rectifying n-InAsSb/n-GaSb heterojunctions and (3) growth, fabrication, and testing of heterojunction and homojunction photodiodes with InAsSb active layers.

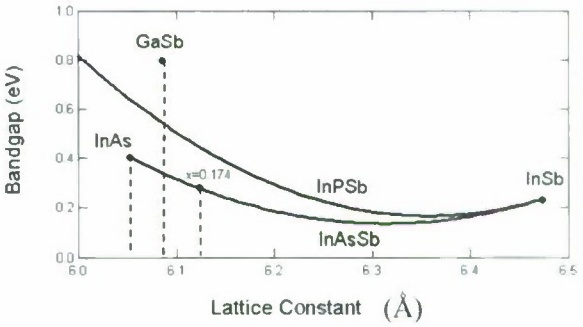

Fig.1 Section of the 77K bandgap vs. lattice constant curves for the InAs/InSb/InP material system. Dashed lines show positions of tensile strained InAs, lattice matched InAsSb, and compressively strained InAsSb respectively.

II. Experiment

Epitaxial layers were grown in a vertical MOCVD reactor with an optical showerhead configuration.[5] The reactor pressure was maintained at 50 Torr. Source precursors were tertiarybutylarsine (TBAs), tertiarybutylphosphine (TBP), trimethylantimony (TMSb), triethylgallium (TEGa), and trimethylindium (TMIn). Diethylzinc and diethyltellurium were used as the p-and n-type dopants respectively. Samples were grown on 001 GaSb substrates doped with Te to ~1×10^{18} cm^{-3} and miscut by 2° towards 111B. Mesa diode device fabrication performed at Simon Fraser University (Fig. 8) was achieved using a wet chemical etching/liftoff process discussed previously.[6] The devices processed at the

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University of New Mexico (Figs. 6,7) were fabricated using a dry etching technique.

III. InAsSb growth

Figure 2 shows the basic idea behind the type II InAsSb/InAs superlattice scheme. For the case when t_{InAs} is equal to ½ t_{InAsSb}, strain balance is achieved for an Sb composition of ~17-18%. In a previous work we demonstrated that the alignment is type II. Theoretical calculations of the emission energies indicated best agreement assuming that the conduction band of the InAsSb layers is at higher energy than the InAs. For strain balanced structures we demonstrated that the emission wavelengths were red shifted significantly from the expectations of the bulk InAsSb bandgaps, extrapolating to zero emission wavelength at an InAsSb composition of approximately x=0.37.

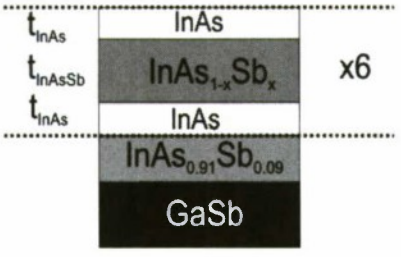

Fig. 2 Single repeat unit of an InAsSb/InAs superlattice. For t_{InAs}=0.5, t_{InAsSb} the alloy composition is x=0.174 as shown in Fig. 1.

Figure 3 shows a schematic of the proposed band alignment from ref. [4]. The values of the offsets obtained depend somewhat on the assumptions on whether the band bowing occurs in the valence band or the conduction band. Assuming strain balanced conditions, with equal InAs and InAsSb thicknesses the conduction and valence band offset estimates are as follows. Assuming all band bowing in the conduction band: ΔE_c=0.056eV, ΔE_v=0.11eV. For all band bowing in the valence band, ΔE_c=0.15eV, ΔE_v=0.21eV.

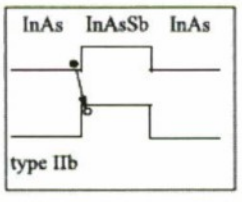

Fig. 3. Type II band alignment for InAsSb/InAs heterojunctions.

IV. InPSb growth

The use of InAsSb lattice matched to GaSb has been investigated by several groups as a potential material system for mid IR photodetectors. In an effort to push the operating temperatures to higher values, several groups have investigated the use of wider gap barrier layers such as AlInAsSb in order to reduce the thermal diffusion current contribution and thereby increase the R_0A product.[7] Al-containing alloys are challenging for MOCVD, particularly at the low growth temperatures typically used to deposit Sb containing alloys such as InAsSb. InPSb is lattice matched to GaSb at an Sb mole fraction of x=0.36. The corresponding bandgap at 300 K is between 0.48-0.50 eV[8,9], compared with 0.26 eV for lattice matched InAsSb, providing the potential for a substantial decrease in thermal diffusion current for p-InPSb/n-InAsSb heterojunctions. Fig. 4. shows the energy bands calculated according to a numerical self consistent energy band code.[10]

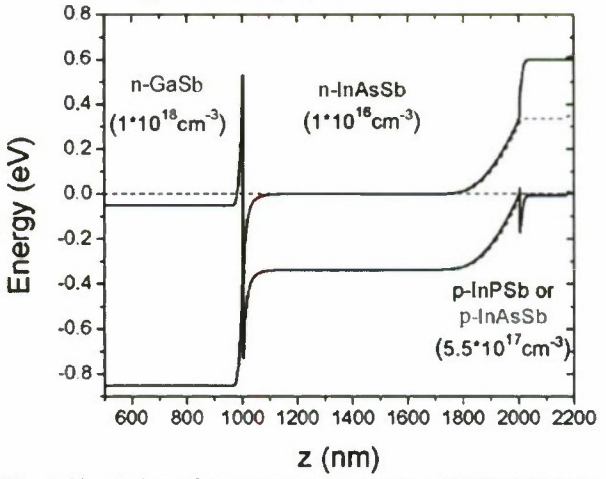

Fig. 4 Simulation of the energy bands of a p-InPSb/n-InAsSb heterojunction diode on an n^+ GaSb substrate. Dotted lines show the band energies for the case where the p-layer is lattice matched InAsSb (homojunction diode)

Another potential advantage of using a wider gap heterojunction p-contact is the ability to suppress sidewall leakage currents in small mesa diode devices. InAsSb suffers from a strong surface accumulation layer due to the fact that the surface Fermi level is approximately 200meV above the conduction band minimum. In a p-n homojunction device this layer can act as a conduction shunt in parallel with the p-n junction. As the simulation in Fig. 4 indicates, the conduction band of InPSb is more than 200 meV higher compared with InAsSb, which means that the surface states may be located inside the gap. This should reduce the effect of surface leakage in unpassivated p-InPSb/ n-InAsSb diode structures.

We grew lattice matched $InP_{0.63}Sb_{0.37}$ on $InAs_{0.91}Sb_{0.09}$ with excellent structural and surface morphology at 500°C despite the fact that thermodynamic calculations show this composition to be well inside the miscibility gap for this ternary alloy system.[9] In a previous work we showed that the presence of an InPSb p-doped layer reduced R_0A products compared with InAsSb homojunctions.[6]

V. Electrical properties of GaSb/InAsSb interfaces

One issue that arises from the growth of InAsSb on GaSb is the formation of a strongly staggered type II junction at the interface between InAsSb and GaSb as shown in Fig. 5. The properties of this interface must be understood in order to

make practical device structures. Various possibilities arise depending on the relative doping between the two layers. For example, growth of lightly n-type InAsSb on an n-type GaSb substrate was shown several years ago to result in a rectifying junction.[11] In contrast, n-type InAsSb on p-type GaSb results in a barrier free heterojunction since the Fermi levels of the two materials are essentially aligned before junction formation. The possibility of a parasitic junction at the GaSb substrate/InAsSb interface must be considered when designing a photodetector. In a recent work we showed that the n-InAsSn/n-GaSb heterojunction is rectifying for n-GaSb < 5×10^{17} cm^{-3} and increasingly Ohmic above that concentration.[12] This is presumably due to the formation a tunneling junction for higher doping levels. Thus, if a back side contact device is to be used, the doping level in the GaSb side must be at least 10^{18} cm^{-3}.

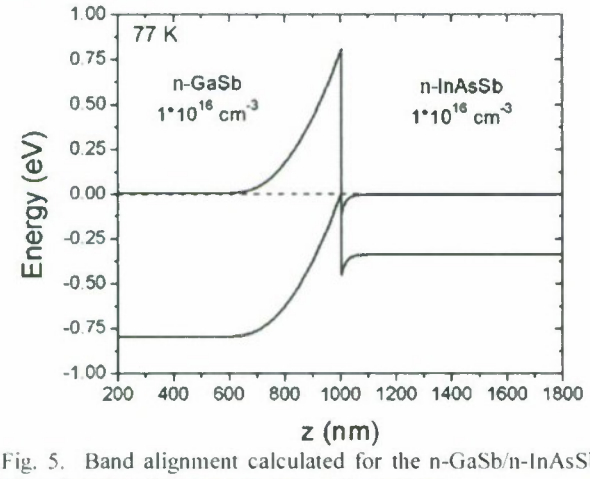

Fig. 5. Band alignment calculated for the n-GaSb/n-InAsSb heterojunction showing Schottky-like junction.

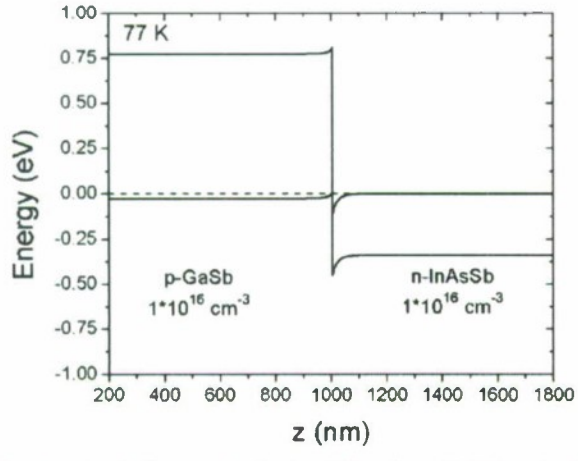

Fig. 6. Band alignment calculated for the p-GaSb/n-InAsSb heterojunction showing zero barrier lineup.

VI. Device Results

Large area homojunction InAsSb detectors with outstanding R_0A values were grown by liquid phase epitaxy on GaSb substrates many years ago[13], however, this technique is not suitable for heterojunction bandgap engineering and small area devices suitable for FPAs. The growth of InAsSb based detectors has been reported recently by several groups using molecular beam epitaxy.[14,15] In the present work, mesa diode structures were fabricated consisting of a top p-type contact layer of either InAsSb or InPSb (~10^{17} cm^{-3}), following by an non intentionally doped (nid) 1μm absorption layer of InAsSb. Typically measurements were performed via top side contacts placed on the mesa (p-contact) or on the exposed n^+GaSb substrate (n-contact). Since the structures were grown on oxide free n+ GaSb substrates, there was no parasitic interface between the n-contact and the InAsSb absorption layer.

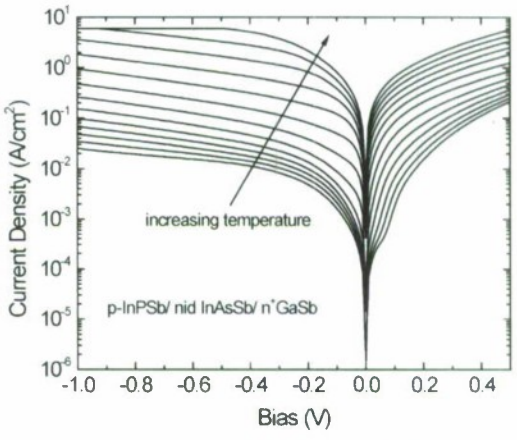

Fig. 7 IV data for a p-InPSb/ nid-InAsSb/n^+GaSb mesa photodiode. Lowest temperature is 40K, increasing in 20K steps until 280K.

Figure 7 shows a set of *IV* curves for the p-InPSb/n-InAsSb junction diodes fabricated without any passivation. Diodes fabricated from homojunction layers (p-InAsSb/n-InAsSb) invariably showed much higher leakage currents and very poor rectification, for reasons to be discussed later in this work.

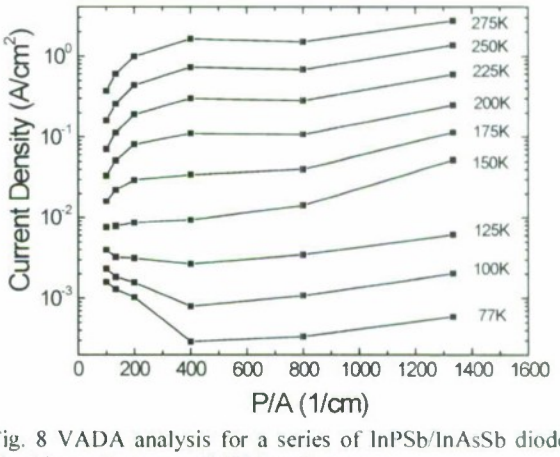

Fig. 8 VADA analysis for a series of InPSb/InAsSb diodes.. The bias voltage was -0.1V for all curves.

Figure 8 shows the results of variable area diode array analysis (VADA) on an InPSb/InAsSb heterojunction device. These data were taken from a set of mesa photodiodes fabricated with mesa dimensions ranging from 400 μm× 400 μm to 30 μm ×30 μm. At low temperatures, these curves are almost flat, which means that the surface sidewall component of the dark current is small. Similar measurements performed in homojunction devices showed a large increase in dark current density with increasing P/A ratio. This indicates that the presence of the wide gap InPSb layer greatly reduces surface leakage compared with the homojunction devices. The most probable explanation is the fact that the wide gap layer does not have a surface accumulation layer, in contrast to the InAsSb active layer.

Figure 9 shows the uncalibrated 77K photo response from an unpassivated lattice-matched InAsSb homojunction photodiode. These data were obtained by mounting the detector on a liquid nitrogen cooled copper header in the detector arm of a Bomem Fourier transform spectrometer, using a glow bar for the infrared radiation source. The data were acquired under zero bias. The detector cutoff on the low energy side is 2406 cm-1 (0.30 meV) corresponding to a wavelength of 4.2 μm. Absorption lines from atmospheric H_2O are clearly evident in the inset. We do not yet have calibrated responsivity data for this device, but the absolute responsivity is comparable to that of a commercial InAs photodiode when scaled by device area. This is rather surprising considering the fact that all the homojunction devices exhibited large leakage currents. This is further evidence that the poor reverse bias leakage of the homojunctions devices results from surface accumulation conduction, which should not appreciably affect zero bias photocurrent measurements.

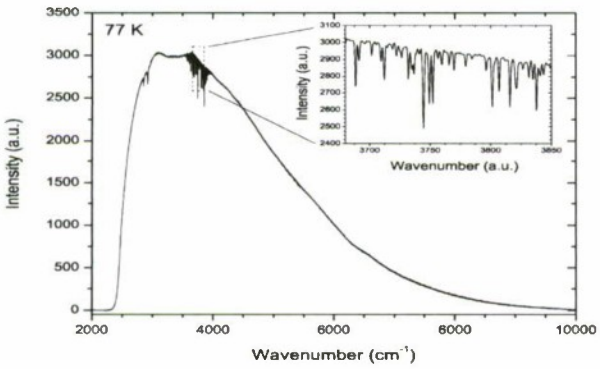

Fig. 9 Uncalibrated photodetector results from an unpassivated p-InAsSb/nid-InAsSb/n⁺GaSb photodiode structure.

VII. Conclusions

InAsSb/InPSb heterostructures are promising materials for the growth of mid IR detectors spanning the wavelength range from 3.5 to 10 μm. We have shown the feasibility of InAsSb/InAs strained layer type II active layers to achieve longer wavelengths on GaSb substrates. We have demonstrated that care needs to be taken to minimize paraisitic junctions when growing InAsSb-based devices on GaSb substrates. We have demonstrated that the use of a wider gap p-InPSb top contact layer is a promising method for suppressing sidewall current leakage in unpassivated photodiodes. Finally we present preliminary detector results for homojunctions InAsSb photodiodes.

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Electronic Properties of the $Al_{0.56}In_{0.44}Sb/Ga_{0.5}In_{0.5}Sb$ Heterostructure

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Low Temperature Grown GaAsSb as Photoconductive Material near 1.06 μm

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Paper is not available.

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Zn-DOPED InGaAs WITH HIGH CARRIER CONCENTRATION ENHANCED BY Sb SURFACTANT FOR LOW SPECIFIC CONTACT RESISTANCE

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Abstract

A dramatic increase of carrier concentration in Zn-doped InGaAs layer was achieved by adding a small amount of Sb as a surfactant during MOVPE growth. A carrier concentration as high as 6×10^{19} cm^{-3} was obtained and resulted in a specific contact resistance lower than 2×10^{-7} Ωcm^2.

I. Introduction

Low contact resistance between a p-type semiconductor and an electrode is effective in improving the characteristics of semiconductor devices [1]. Decreasing the band-gap energy of a semiconductor contact layer is useful for reducing the contact resistance [2]. InGaAs has the smallest band-gap energy among InGaAsP materials lattice-matched to InP and is therefore commonly used as a contact layer in InP-based devices. Increasing the carrier concentration in the contact layer is also useful for reducing the contact resistance. Zinc (Zn) is used extensively as a p-type dopant of InGaAs. However, it is difficult to obtain InGaAs with a high concentration of Zn atoms by epitaxial growth because of the low incorporation efficiency of Zn into an InGaAs layer. Therefore, the carrier concentration in an InGaAs layer grown by the metalorganic vapor phase epitaxy (MOVPE) commonly saturates at 2-3 $\times 10^{19}$ cm^{-3}, and then the specific contact resistance is only in the 10^{-6} Ωcm^2 range [3]. In this study, we investigated the use of Sb surfactant as a way to increase the carrier concentration in a Zn-doped InGaAs layer grown by MOVPE. This is because surfactants can influence the structure of a growing surface, which could govern the Zn incorporation. In addition, we examined the specific contact resistance for the heavily Zn-doped InGaAs contact layer obtained by using Sb surfactant.

II. Experiment

Zn-doped InGaAs layers were grown on InP (100) substrates in a horizontal MOVPE reactor at 50 Torr. The precursors for In, Ga, As, and Zn were trimethyl-indium (TMIn), triethyl-gallium (TEGa), arsine (AsH_3), and diethyl-zinc (DEZn), respectively. The Sb precursor as a surfactant was tris-dimethyl-amino-antimony (TDMASb) [4]. The growth temperature was varied from 500 to 620°C. Carrier concentration was measured by electrochemical capacitance-voltage (ECV) depth profiling, and Zn concentration and Sb composition were measured by secondary ion mass spectroscopy (SIMS). The specific contact resistance was determined by using the transmission line model (TLM) [5]. The TLM pads, which consist of Ti, Pt, and Au and were 100-μm long and 280-μm wide, were patterned by using a standard photolithographic technique and lift-off. The gap spacing between the pads (d) was varied from 10 to 500 μm. The contacts were heat-treated by a rapid thermal annealing at 400°C for 180 seconds in nitrogen ambient.

III. Surfactant effect on Zn incorporation efficiency

We first investigated the maximum carrier concentration obtained by typical growth conditions without Sb surfactant. Figure 1 shows the DEZn flow rate dependences of the carrier concentration in Zn-doped InGaAs layers grown at different temperatures. When the DEZn flow rate was increased and/or the growth temperature was decreased, the carrier concentration was increased from 1×10^{18} to 3×10^{19} cm^{-3}. However, it was saturated at 3×10^{19} cm^{-3}. The SIMS analysis revealed that the saturation of the carrier concentration was caused by decreasing the incorporation of Zn atoms.

The effect of Sb surfactant on the Zn incorporation efficiency into InGaAs layers was investigated to determine whether a carrier concentration higher than 3×10^{19} cm^{-3} could be obtained. Figure 2 shows the TDMASb flow rate dependence of the carrier concentration in Zn-doped InGaAs

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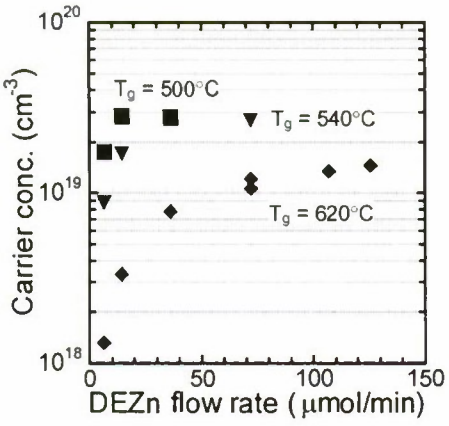

Fig. 1. DEZn flow rate dependence of the carrier concentration in Zn-doped InGaAs layers grown at different temperatures.

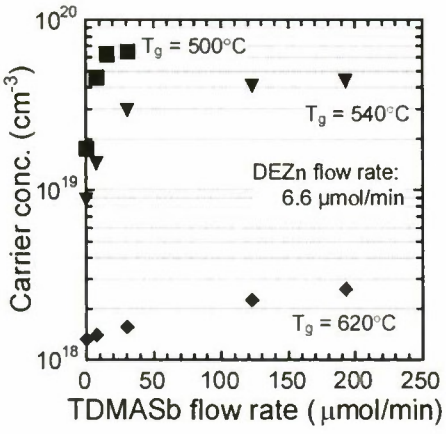

Fig. 2. TDMASb flow rate dependence of the carrier concentration in Zn-doped InGaAs layers grown at different temperatures. DEZn was kept at a constant flow rate of 6.6 μmol/min

layers grown at different temperatures. The DEZn flow rate was 6.6 μmol/min. The carrier concentration increased with increasing TDMASb flow rate and/or decreasing growth temperature even when DEZn was kept at a constant flow rate. When the growth temperature was decreased, the carrier concentration markedly increased by supplying a small amount of TDMASb. As a result, for a growth temperature of 500°C, we could obtain an InGaAs layer with a carrier concentration as high as 6.5×10^{19} cm^{-3}. The carrier concentration was more than twice that of the InGaAs layers grown without supplying TDMASb as shown in Fig. 1. Figure 3 shows the SIMS depth profiles of Zn, Sb, C, and H atoms in InGaAs layers grown at 540°C. The TDMASb flow rate was varied from 0 to 192 μmol/min during the growth of the InGaAs layers. When the TDMASb flow rate was increased, the Zn concentration increased with increasing Sb composition, although the DEZn was kept at a constant flow rate of 6.6

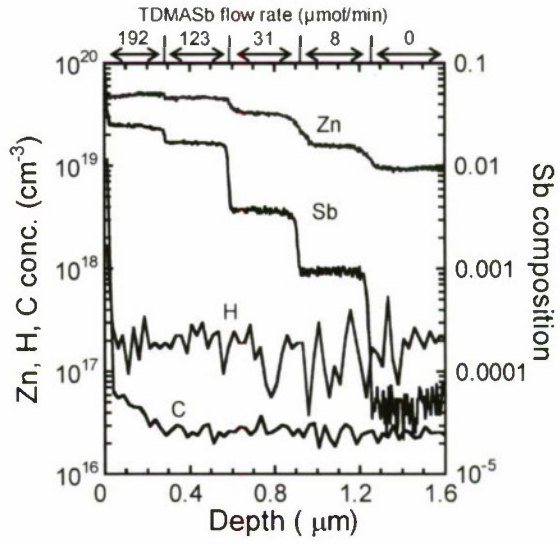

Fig. 3. SIMS depth profiles of Zn, Sb, C, and H atoms in InGaAs layers grown at 540°C. The TDMASb flow rate was varied from 0 to 192 μmol/min during the growth of InGaAs layers.

μmol/min. This result indicates that the increase in the carrier concentration, as shown in Fig. 2, was due to the increasing Zn incorporation efficiency into InGaAs layers by supplying TDMASb. In addition, the activation rate of Zn atoms was estimated at as high as 90% from Figs. 2 and 3. This seems to be because the impurities, such as C and H, were not increased as shown in Fig. 3. Furthermore, for a growth temperature of 500°C, an increase in Zn incorporation efficiency and an activation rate of Zn atoms of about 90% were obtained by supplying TDMASb.

Figure 4 shows the relationship between the TDMASb

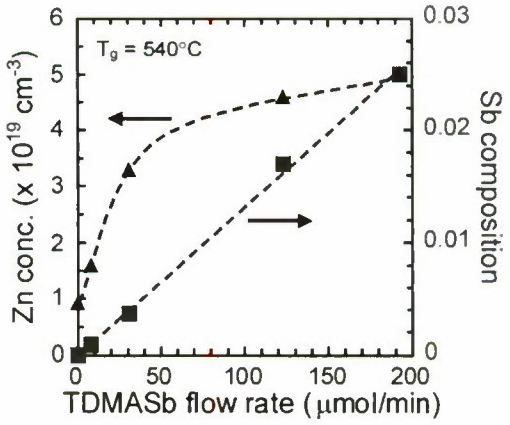

Fig. 4. Relationship between TDMASb flow rate and Zn concentration and Sb composition in InGaAs layers grown at 540°C measured by SIMS analysis.

flow rate and Zn concentration and Sb composition in InGaAs layers shown in Fig. 3. The Sb composition was proportional to the TDMASb flow rate, but the Zn concentration rapidly increased with a small amount of TDMASb supplied. This indicates that the Zn incorporation does not depend on the Sb composition in the InGaAs layer. From this result and that from the dependence of the increase in Zn atoms on the TDMASb flow rate as shown in Fig. 2, Sb atoms remaining on the growing surface seem to enhance the incorporation of Zn atoms into InGaAs layers. That is to say, the incorporation efficiency of Zn atoms is increased by the surfactant effect of Sb atoms.

IV. Specific contact resistance for heavily Zn-doped InGaAs layer

Finally, we investigated how the heavily Zn-doped InGaAs layer obtained by using Sb surfactant contributes to reducing the specific contact resistance. The specific contact resistances were measured by TLM for Zn-doped InGaAs contact layers with carrier concentrations of 3.0, 4.5, and 6.0 × 10^{19} cm^{-3}. To determine the ohmic contact parameters with TLM, we used the relationship between the total resistance (R_T) between two pads and the gap spacing (d) shown in Fig. 5. R_T is given as

$$R_T = \frac{2R_{SK}L_T}{W} + \frac{R_{SH}d}{W}, \qquad (4.1)$$

where R_{SK} is the sheet resistance of the layer directly under the contact, R_{SH} is the sheet resistance of the semiconductor layer outside the contact region, W is the pad width, L_T is the transfer length. L_T is given as

$$L_T = \sqrt{\frac{\rho_c}{R_{SK}}}, \qquad (4.2)$$

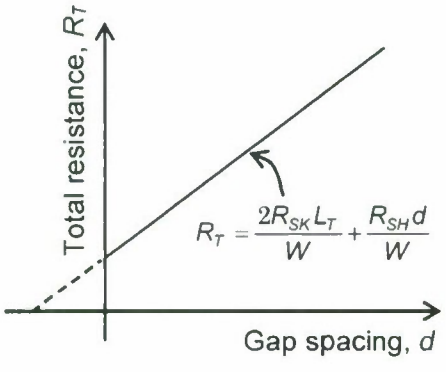

Fig. 5. Plot of total resistance (R_T) between two pads as a function of gap spacing (d) to obtain the ohmic contact parameter.

where ρ_c is the specific contact resistance. When we assume that R_{SK} is equal to R_{SH}, ρ_c is given as

$$\rho_c = R_{SH}L_T^2. \qquad (4.3)$$

The ρ_c can be calculated from the relationship between R_T and d as shown in Fig. 5 and (4.3). Figure 6 plots the measured R_T between two pads as a function of the d for the InGaAs contact layer with a carrier concentration of 4.5 × 10^{19} cm^{-3}. In this case, the value was 2.9 × 10^{-6} Ωcm^2. Figure 7 shows the relationship between the specific contact resistance and the carrier concentration in the InGaAs contact layer. The specific contact resistance decreased with increasing the carrier concentration. As a result, we achieved a specific contact resistance of less than 2 × 10^{-7} Ωcm^2 for the InGaAs contact

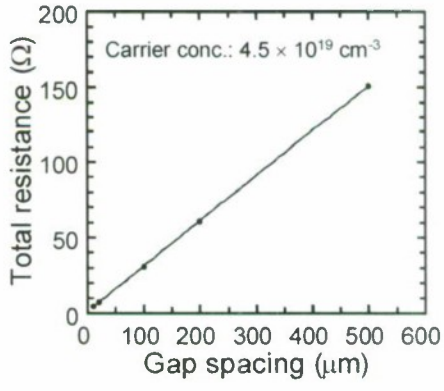

Fig. 6. Plot of total resistance between two pads as a function of the gap spacing for an InGaAs contact layer with a carrier concentration of 4.5 × 10^{19} cm^{-3}.

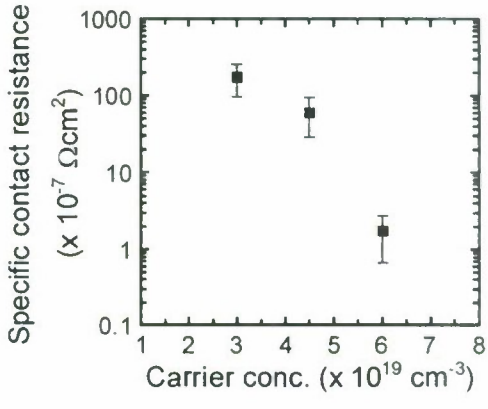

Fig. 7. Relationship between specific contact resistance and carrier concentration in InGaAs contact layers.

layer with a carrier concentration of 6.0×10^{19} cm^{-3}. This indicates that the heavily Zn-doped InGaAs layer obtained by using Sb surfactant is very useful for reducing the specific contact resistance.

V. Conelusion

We obtained a Zn-doped InGaAs layer with a carrier concentration higher than 6×10^{19} cm^{-3} by MOVPE growth using Sb as a surfactant. By using the heavily Zn-doped InGaAs as a contact layer, the specific contact resistance was reduced to lower than 2×10^{-7} Ωcm^2. This result will be useful for improving the characteristics of InP-based devices, such as lasers and modulators.

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Sub 50 nm InP HEMT with fT = 586 GHz and Amplifier Circuit Gain at 390 GHz for Sub-Millimeter Wave Applications

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Abstract

In this paper, we report recent advances on sub-50 nm InP HEMT have achieved new benchmarks of 586 GHz fT and 7 dB amplifier circuit gain at 390 GHz

There has been significant advancements in sub-50 nm HEMT devices[1,2] and circuits[3] operating in sub-millimeter-wave (sub-MMW) band above 300 GHz. These are expected to provide a new generation of products for imaging and communications that are expected to provide benefits such as higher available bandwidth and reduced aperture and instrument size for radar and remote sensing applications. To date, the highest frequency amplifier performance has reached 350 GHz with an InP HEMT exhibiting an fT of 500 GHz and Fmax > 1 THz [1]. This paper describes the latest advancements of sub-50 nm InP HEMT S-MMIC technology that have achieved fT =586 GHz and a new record high frequency amplifier gain at 390 GHz.

The sub-50 nm InP HEMT device and S-MMICs previously implemented focused on improvements in device epitaxy, ohmic resistance reduction, gate length reduction and compact passive circuit components, Further optimization to push higher frequency have focused on further device gate length reduction and device epitaxy scaling. Initial device model extraction indicates a reduction in equivalent circuit model Cgs for the smaller gate length process. Figure 1 and 2 depict the typical device IV characteristics.

The device epitaxial scaling has proved to accommodate the shorter gate length with good device IV characteristics, controlled output conductance and sharp device pinchoff as shown. Peak device transconductance >2300 mS/mm has been achieved at 1V drain bias.

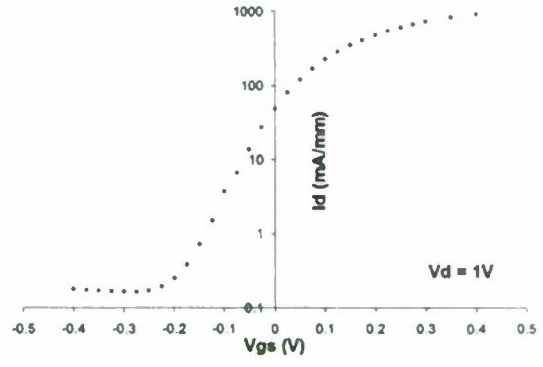

Figure 1. Ids vs. Vgs at Vds=1V of a 2 finger 40um InP HEMT. Sub-threshold current is < 0.2 mA/mm.

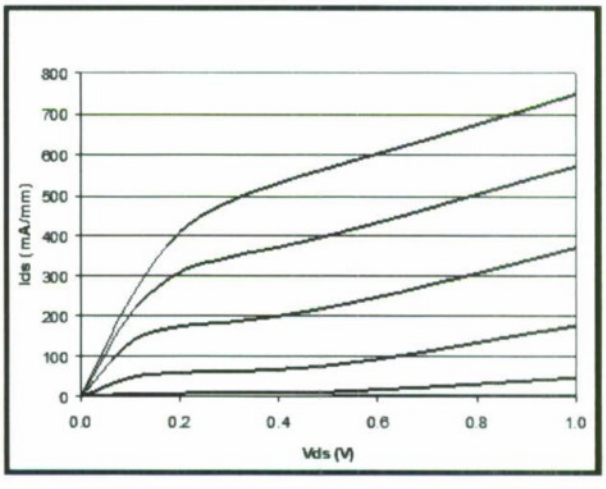

Figure 2. Ids vs Vds for a two finger 40um InP HEMT. Vg from -0.1V to +0.3V in 75 mV steps

Figure 3 shows H21 vs. frequency derived from measured S-parameters up to 110 GHz for a 2 finger 40 um InP HEMT with an fT of 586 GHz at Vd = 0.8V and Id = 12 mA. The devices are configured with extended reference planes to minimize probe to probe interaction and the measured S-parameter data is calibrated to the device reference planes.

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The fT for the InP HEMT derived from S-parameters was measured over a current and voltage range from 0.5 to 1V and 200-400 mA/mm, respectively.

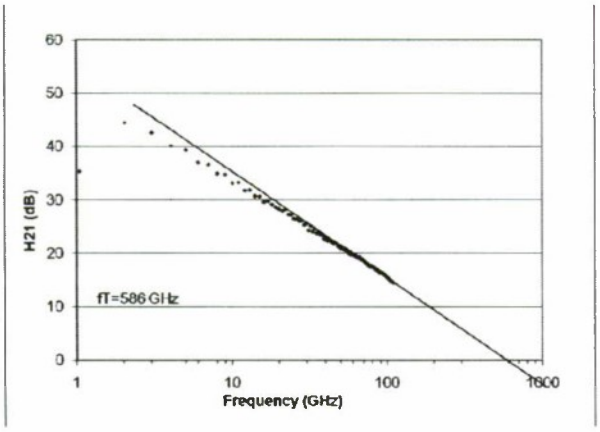

Figure 3. De-embedded H21 vs. Freq. for InP HEMT device with two fingers and 40µm gate width. fT =586 GHz at Vd=0.8 V, Id = 16 mA.

The data is shown in Figure 4 and peak fT was achieved at 0.8V and 400 mA/mm. At Vds of 0.5V and 300 mA/mm, the fT remains greater than 500 GHz.

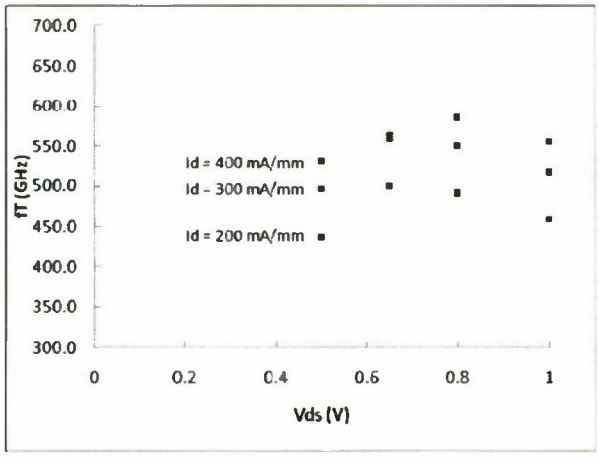

Figure 4. Device fT vs. Vds and Ids for sub 50 nm InP HEMT

To realize the high frequency amplifier sub-MMW circuits, extremely compact, low-loss RF components and interconnection necessary to scale design footprints in conjunction with the frequency of operation. The S-MMIC circuit layout size is as much as 10 times smaller compared to their MMIC counterparts at lower frequencies.

The wafers are thinned to 2-mil (50 um) thickness with through substrate slot vias etched through the InP wafers. The backside is plated with Au metal. On-chip probe transitions from coplanar to waveguide are designed into the S-MMIC. A WR2.2 fixture has been designed to accommodate the S-MMIC chip to enable higher frequency measurements above 340 GHz.

The fixture 3-stage single-ended coplanar S-MMIC amplifier demonstrates gain from 350-390 GHz biased at Vds = 1V and 18 mA total current as shown in Figure 5 with the reference plane at the waveguide flange. Subtracting the estimated loss of 1.5 dB per on-chip transition, a gain of 7 dB at 390 GHz has been achieved at the S-MMIC reference plane. The gain amplifier at 390 GHz represents to the best of our knowledge a new record for high frequency amplifier gain achieved. Further designs are being evaluated to even higher frequencies and will be reported if the circuit designs are successful.

With this newly developed InP HEMT MMIC process, a new generation of military and commercial applications in telecommunications and radio astronomy are enabled at frequencies above 300 GHz with the future promise to approach 1 THz

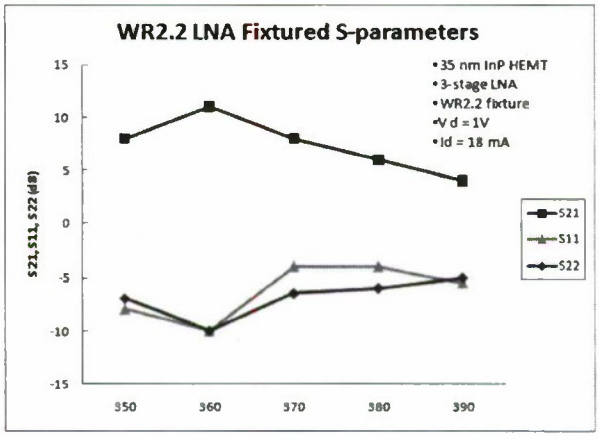

Figure 5. Measured S(21) of 3-stage InP HEMT S-MMIC with peak gain of 11 dB at 360 GHz and 4 dB gain at 390 GHz. Reference plane is at WR2.2 waveguide flange

Acknowledgements

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High Performance InP mHEMTs on GaAs substrate with Multiple Interconnect Layers

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***Abstract*—We report the development of high performance metamorphic InP high electron mobility transistors (mHEMTs) with InAs composite channel design and three interconnect metal layers suitable for advanced RF and mixed signal integrated circuits. An un-passivated 35nm L_g device showed RF figures-of-merit of 533 GHz f_τ and 343 GHz f_{max}. After full circuit processing, encapsulated in BCB, a 35nm L_g, 2×20um W_g mHEMT showed 387GHz f_τ, 580GHz f_{max}. Four-inch wafer mapping shows excellent device uniformity and yield. We also report a broadband (206-294GHz) 3-stage G-, H-band common-source amplifier having a nominal S_{21} mid-band gain of 11-16dB employing thin-film microstrip wiring.**

Keywords-InP high electron mobility transistor; metamorphic low loss dielectric layer; mutiple interconnect layer; D-mode transistor; E-mode transistor; feedback amplifier

I. INTRODUCTION

High performance HEMTs with high indium composition channel material are attractive devices for applications such as radiometric-imaging systems using atmospheric windows around 140 GHz and 220 GHz, remote atmospheric sensing, weapon detection, and 140 GHz MMICs for next generation automobile collision avoidance systems [1-4]. The advanced performance and high bandwidth of HEMTs on InP substrate is attributed to the superior electron transport properties of the high indium composition InGaAs based material system. High indium composition channel materials have merits including high low-field electron mobility, high peak electron saturation velocity, and high sheet carrier density.

Metamorphic InP HEMT (mHEMT) devices on GaAs substrates offer similar benefits by having a high indium composition channel like its InP counterpart. The advantages of GaAs substrates include greater mechanical strength, lower substrate cost, and well-established processing technology. With 6" GaAs substrates, the cost advantage of InP mHEMTs is far superior to InP-based HEMTs and provides opportunity for large volume manufacturing. Having been grown on a strain relaxed and compositionally graded metamorphic buffer layer, mHEMT technology provides more freedom for channel design compared to HEMTs grown on InP subtrates (i.e. higher indium content without strain relaxation). There have been numerous reports of mHEMTs with compatible performance to its InP HEMT counterpart [5-7].

In this paper, we will discuss high performance mHEMT in a multiple interconnect wiring environment with a low-ε_r interlayer dielectric, and a G-, H-band multi-stage amplifier result. The merits of multiple layer interconnect permit designers to create circuits achieving high speed, low-noise, and low power consumption; these include millimeter-wave stripline MMICs, low noise multiple stage high-frequency amplifiers, and a sample-and-holder circuit, where no static power dissipation is required to realize a high bandwidth, low-noise sampling switch.

II. DEVICE DESIGN AND FABRICATION

A. *HEMT Epitaxy*

Figure 1 shows a cross-sectional schematic of a completed mHEMT with epitaxial layers. The mHEMTs are grown with a multi-wafer production molecular beam epitaxy (MBE) reactor using a 7x4" platen configuration. The metamorphic buffer on 4" semi-insulating GaAs substrate begins with 3,000 Å of graded buffer. The linear compositional grade starts from AlAs and ends at $In_{0.52}Al_{0.48}As$. The substrate temperature drop and the aggressive linear grading during the graded buffer growth have been optimized to accelerate buffer relaxation and growth time. This aggressive linear grading layer also reduces growth cost. Then, another 4,000 Å of $In_{0.52}Al_{0.48}As$ buffer is grown directly on top of the graded buffer. After this lower buffer/barrier of $In_{0.52}Al_{0.48}As$ layer, 8nm $In_{0.7}Ga_{0.3}As$-InAs- $In_{0.7}Ga_{0.3}As$ composite channel was grown. This channel was aggressively optimized to provide high mobility and high saturation velocity without incurring material relaxation. $In_{1-x}Al_xAs/In_{0.52}Al_{0.48}As$ upper barrier with Si planar doping and spacer was grown on top of the

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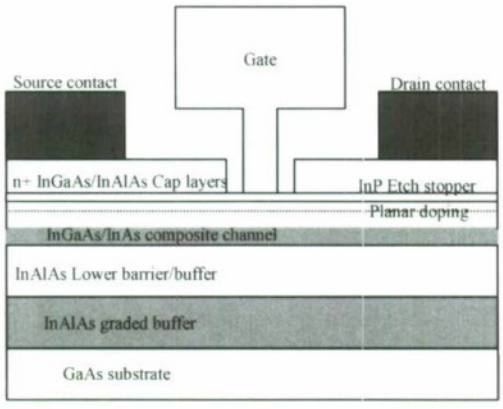

Figure 1.Schematic of a fabricated MHEMT with epitaxial layers.

composite channel. Upper barrier material composition was optimized to achieve lower device on-resistance. The InP etch-stop layer and n+ InGaAs/InAlAs cap layers were grown on top of the upper barrier layers. Between these upper barrier and cap layers, Si planar doping layers were added to reduce access resistance and sheet resistance. Sheet carrier density and mobility of 3.0×10^{12} cm^{-2} and 9000 $cm^2/V\text{-}s$ were measured from samples without heavily doped cap layers.

B. Device Fabrication

Device fabrication begins with HEMT mesa isolation of the active area by selective wet-chemical etching. Thin film resistors (TFR) are then pattern deposited by e-beam evaporation on the dielectric layer outside the isolation area. By optical lithography the source-drain ohmic contacts are then patterned and formed by evaporated metal liftoff. To ensure low source and drain contact resistance and thermal stability during the thermal cycles associated with device and circuit formation, they are formed by a non-alloyed Mo/Ti/Pt/Au metal stack.

Gates are patterned by a well-established electron beam lithography (EBL) process with a tri-layer resist (ZEP/PMGI/ZEP) and formed by Pt/Ti/Pt/Au evaporated metal lift-off. Wafers are then annealed at 250°C for one hour in a nitrogen ambient to diffuse Pt into the semiconductor. More detailed information of the TSC InP HEMT process is described in [8].

This mHEMT device technology is integrated with a high-yield, 3-level interconnect process utilizing benzocyclobutene (BCB) as the spin-on inter-metal dielectric layer(ε_r=2.7). This process with thin BCB allows a thin film microstrip wiring to be used, where a ground plane is formed in the first metal layer, shielding the RF signal formed in the top metal layer from forming parasitic modes associated with the thick 25-mil substrate. Thin film microstrip also allows for more compact circuit layout, is accurately modeled by EM-simulators, and shows well-behaved on-wafer measurement without time consuming backside processing. A gold-based electroplating process forms metal interconnects and electrical connections

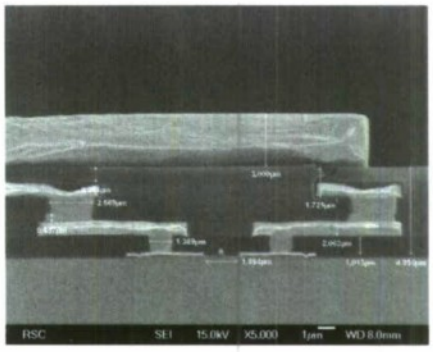

Figure 2. Cross sectional SEM image of the processed HEMT with three interconnect layers.

through the vias to the device and thin-film resistors. MIM capacitors are generated by using Si_xN_y dielectric between the first and second interconnect metal layers. Figure 2 shows a cross sectional scanning electron microscopy (SEM) image of a processed HEMT with three interconnect layers.

III. Device and Circuit Results

Figure 3 shows the measured DC characteristics of a 35 nm gate length (L_g) mHEMT. This device shows good pinch-off characteristics with a threshold voltage (V_{th}) of -0.4 V, low on-resistance (R_{on}) of 0.3 ohm-mm at V_{ds} = 0.6 V, and $g_{m,max}$ of 1.8 S/mm. I_{dmax} exceeds 1.4 A/mm. The device may be safely biased to 1.6 V V_{ds} and 1.0A/mm I_d with negligible DC and RF performance degradation due to breakdown or impact ionization – with greater than 1.2V ($0.4 < V_{ds} < 1.6$V) of usable voltage to support high mm-, sub-mm wave power amplification. Figure 4 shows the measured RF characteristics of a 35nm L_g, 2×50um W_g mHEMT prior to BCB encapsulation, where a peak f_T of 533 GHz and f_{MAX} of 343 GHz were extrapolated. This high f_T can be attributed to extremely short gate to channel distance and high saturation velocity of composite channel. To our knowledge, this is one of the highest performance mHEMTs reported to date. Figure 5 shows the measured RF characteristics of a 35nm L_g, 2×20μm W_g device after completed circuit fabrication. From Mason's unilateral power gain, an f_{max} of 580 GHz was extrapolated – this is consistent with the TSC large signal model. Description

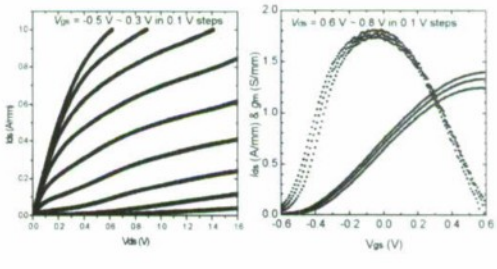

Figure 3. Measured DC characteristics of 35nm mHEMT.

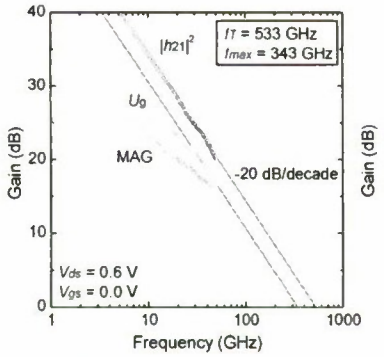

Figure 4. Measured RF gains of a 35nm L_g, 2x50um W_g mHEMT before BCB process.

of the measurements can be fournd in [9]. Figure 6 shows the NF and associated gain measurement results of a 35nm L_g, 2×20 μm W_g device after circuit fabrication at g_m peak bias condition. It shows low NF of 1 dB at 26 GHz, making this technology suitable for low noise amplifier applications.

Based on the device measurements, a large signal model (Agilent EEHEMT model) has been developed and utilized for millimeter-wave, sub-mm wave monolithic integrated circuit (MMIC) amplifier design. Figure 7 shows a microscopic image of a fabricated 3-stage common-source, G-, H-band amplifier. Each stage is composed of a single common-source configured 35nm L_g, 2×20μm W_g mHEMT employing thin film microstrip (ε_r = 2.7). The amplifier was designed and simulated using the TSC large signal model and was to have a center frequency of 240GHz. The measured S-parameters (206-320 GHz) of the 3-stage common-source amplifier are shown in figure 8. The results show 11-16 dB S_{21} mid-band gain, with 3 dB bandwidth at 294 GHz. The HEMT gate and drain bias voltages are common to all stages – V_{ds} = 1.05 V, V_g=50 mV, $I_{d,total}$ = 64.7 mA, P_{total} = 82.5 mW. Complete details of this amplifier can be found in [9].

IV. Conclusion

A high performance 35nm gate length InP mHEMT technology has been developed at Teledyne Scientific, co-integrated with low-loss multi-layer interconnects. The device technology has demonstrated excellent DC characteristics with

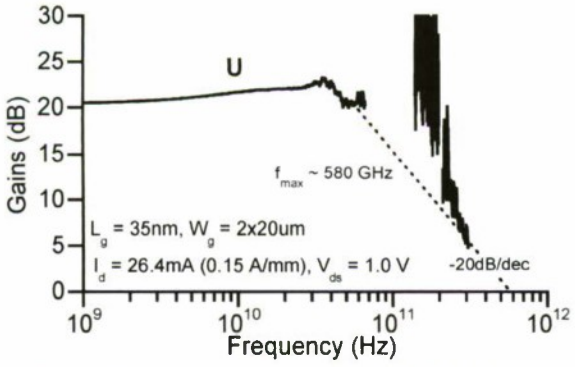

Figure 5. Mason's Unilateral Gain of a 35nm Lg, 2x20um Wg mHEMT after multi-layer interconnect processing.

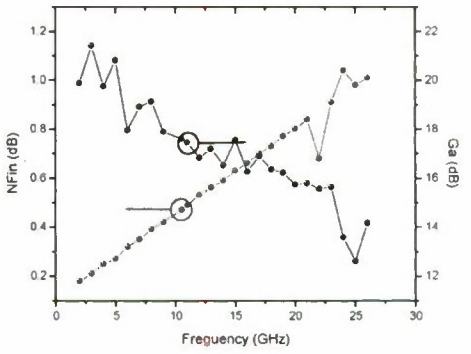

Figure 6. Measured NF_{min} and associated gain of a 35nm L_g, 2x20um W_g mHEMT after multi-layer interconnect processing.

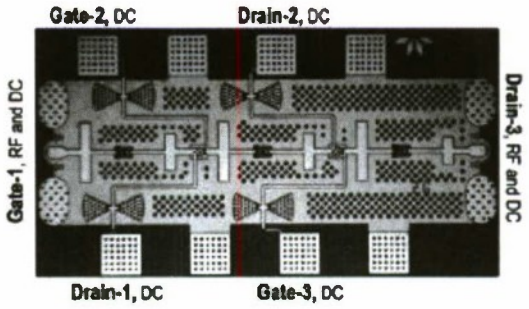

Figure 7. IC micrograph of 3-stage InP mHEMT amplifier MMIC employing thin-film microstrip wiring. Die area, 0.77 x 0.40mm².

many potential capabilities ranging from high mm-, sub-mm-wave power amplifiers to very low noise amplifiers. The TSC mHEMT demonstrates low 0.3 Ohm-mm on-resistance, high 1.8 S/mm g_m, breakdown voltage exceeding 1.6V, I_{dmax} exceeding 1.4 A/mm, f_T of 533 GHz before passivation (2x50 μm W_g) and f_{max} of 580 GHz after passivation (2x20 μm W_g). Accurate modeling has permitted the demonstration of a 3-stage MMIC amplifier operating in G-, H-band with 11-16 dB S_{21} mid-band gain, and 3dB bandwidth at 294 GHz.

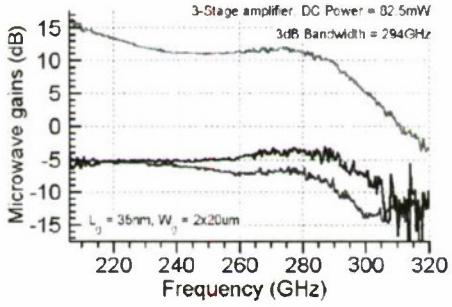

Figure 8. Measured S-parameters for the 3-stage amplifier. 11-16dB S_{21} mid-band gain, 206-294 GHz bandwidth, P = 82.5 mW.

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High Frequency Performance of Vertical InAs Nanowire MOSFET

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***Abstract*—We report on RF characterization of vertical, 100-nm-gate length InAs nanowire MOSFETs, utilizing wrap-gate technology and Al_2O_3 high-κ gate oxide. The transistors show f_t=5.6 GHz and f_{max}=22 GHz, mainly limited by parasitic capacitances. The RF device performance is described using a hybrid-π model taking hole generation at the drain into account. Electrostatic modeling of the parasitic capacitances for arrays of vertical nanowires indicates that a strong reduction in extrinsic capacitances can be achieved for devices with a small inter-wire separation.**

I. INTRODUCTION

The high electron mobility and injection velocity of InAs makes it a candidate for MOSFET scaling beyond the 22 nm node. However, gate scaling can cause short-channel effects, unless the body and oxide thickness are scaled together with the gate length. The body and oxide thickness scaling can be kept smaller by using a wrap gate, or gate-all-around (GAA) architecture, which is the natural gate shape for a nanowire MOSFET. InAs nanowire MOSFETs in vertical geometry have demonstrated a high transconductance g_m= 0.8 mS/μm and small sub threshold slopes of 100 mV/decade [1]. We here report RF measurements on an array of epitaxially grown, vertical InAs nanowire MOSFETs on an S.I. InP substrate. The use of an array of wires simplifies the S-parameter measurements, since the device impedances can be well matched to the 50 Ω measurement system, as compared with single nanowire devices. This is the first RF-data from vertical nanowire FETs (nwFET) [2].

II. FABRICATION

Arrays containing between 1 and 100 nanowires are fabricated on an (111)B semi-insulating InP substrate by first forming Au seed particles using electron beam lithography and lift-off. InAs nanowires are then grown using metal organic vapor phase epitaxy at a growth temperature of T=420 °C. The wires are uniformly doped using Sn. The diameter of the wires are nominally between 35-55 nm and the wire lengths are 1μm. Using sputtering and dry/wet etching, an Al/W wrap contact is fabricated around the base of the nanowires, forming the source contact with a contact length of ~ 200nm. A 9-nm-thick Al_2O_3 high-κ oxide (ε_r=8.7) is then deposited using atomic layer deposition at 250 °C. A spacer layer, used to separate the source and gate layer is fabricated using a spin-on dielectric and O_2 ashing. An L_g≈100nm Al/W gate is then formed on top of the spacer layer using sputtering and dry/wet etching. A second spacer layer gate, separating the gate and drain metal is formed in the same way. The gate-drain and gate-source electrode separation is both equal to 350 nm. Finally, a Ti/Au drain contact, as well as 50 Ω coplanar wave guide that leads to the drain, gate and source contacts are formed by sputtering and wet etching. A schematic cross section of the device is displayed in Fig. 1a. All steps except for the seed particle formation utilize standard optical contact lithography. Figure 1b displays a top view of a transistor. An overview of nanowire processing can be found in [3].

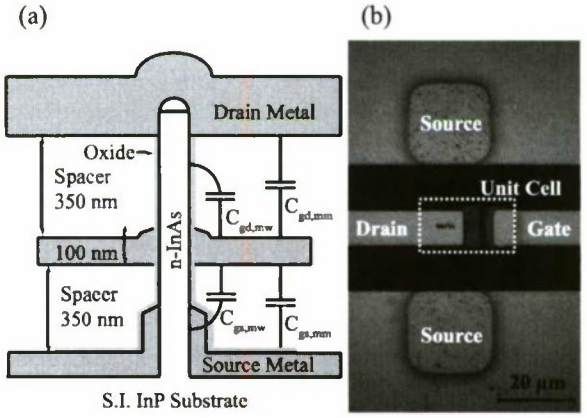

Figure 1. (a) Schematic device cross section, including the parasitic capacitances. (b) Top view of a fabricated transistor. The device unit cell is also indicated.

III. DC&RF CHARACTERIZATION

A. DC Data

Figure 2 shows the measured DC I_{ds}-V_{ds} characteristics for a single nanowire FET with a nominal nanowire radius of

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r_w=25 nm. The single nanowire devices show a maximum drive current of I_{on}=0.6 mA/μm with a transconductance of g_m=160μS/μm, normalized to the nanowire circumference. These numbers are comparable to currently reported III-V MOSFETs, although the transconductance is somewhat lower, which we in part can attribute to the use of a comparable thick Al_2O_3 oxide. The present devices however show a degraded sub threshold slope, as compared with our earlier nwFET data (SS<100mV/decade) [1]. We attribute the degraded sub threshold mainly due to a higher D_{it} originating from the current source contact process.

B. RF Data

In order to accurately measure the S-parameters of a device, its output and input impedance should be matched to the 50 Ω environment of a network analyzer. This is achieved for the nanowire FETs by measuring devices with several nanowires in parallel, in our case 50-100 wires. These FETs have drive currents of a few mA and transconductances in the mS range. S-parameter data was obtained from devices using a co-planar wave guide geometry with a pitch of 100 μm, in a 50 Ω environment. The measurements were performed using an Agilent E8361A network analyzer from 110 MHz to 20 GHz, at a port power of -27 dBm. A two port LRRM calibration was performed off chip. The device response was further obtained after de-embedding the pad capacitance using on chip open structures, with the intrinsic device defined as indicated in Fig. 1b.

Figure 3 shows the measured data and small signal model fits of MSG and h_{21} after de-embedding for a FET consisting of 70 nanowires, with I_{on}=3.5 mA and g_m=1.7 mS. This device shows f_t=5.6 GHz and f_{max} ~ 22 GHz. The maximum measured f_t of our devices is 7.6 GHz, and the highest f_{max} is 22 GHz. These data compare well to earlier published RF data from InAs nanowire FETs [4].

The current gain, h_{21}, shows a close to ideal -20 dB/decade slope, with a small deviation due to either impact ionization or gate-drain band to band tunneling. The narrow band gap (E_g=0.36 eV) of InAs can lead to large band-to-band tunneling or impact ionization at the gate-drain region.

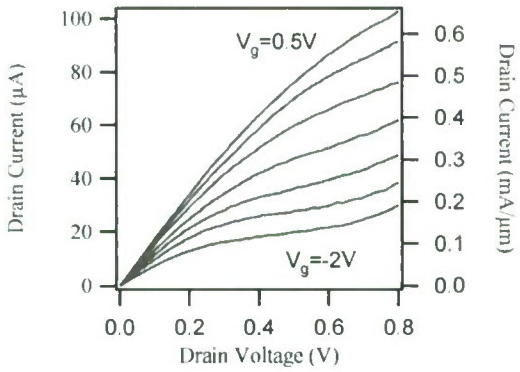

Figure 2. Common Source DC data for a single nanowire FET with r_w=25nm. The gate voltage varies from 0.5 to -2V.

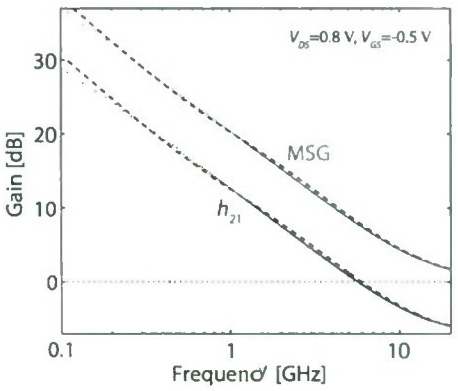

Figure 3. Current gain, h_{21}, and maximum stable gain, MSG for a nanowire FET consisting of 70 nanowires. The dashed lines are small signal model fits from the model in Fig. 4.

The generated holes can further be trapped in the gate region, leading to a feedback mechanism which introduces excess output conductance in the device [5]. Due to the finite time needed for the buildup of the hole concentration under the gate, the effect on the output conductance becomes frequency dependent, with a strong response mainly at lower frequencies.

Following [6], we have developed a small-signal equivalent model of the nanowire FET, including the effect of hole feedback. The small signal model is shown in Fig. 4. We use a standard small signal FET hybrid-π model, with two additional current sources on the output, depending on V_{dg} and V_{gs}. The sources are suppressed at higher frequencies as $1/(1+j\omega\tau_i)$, which models the finite time of the hole build up. Using a combination of analytical and numerical techniques, we extract the small-signal elements from a fitting to the S-parameter data.

Figure 5 shows the measured and fitted S-parameter data, showing good agreement. The anomalous behavior of S_{21} and S_{22} at lower frequencies behavior due to hole accumulation is well captured by the small-signal model. We obtain a best fit for the time constant τ_i=110 pS, similar to the data obtained for an AlSb/InAs HEMT from [6].

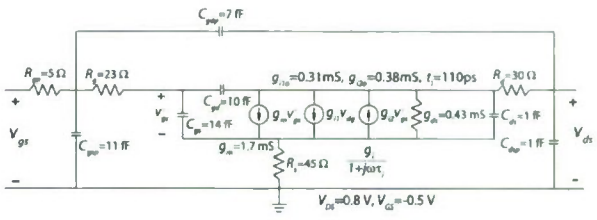

Figure 4. Extracted small signal equivalent model at V_{DS}=0.8V and V_{GS}=-0.5V. The two additional current sources are needed for modeling of the hole generation and accumulation.

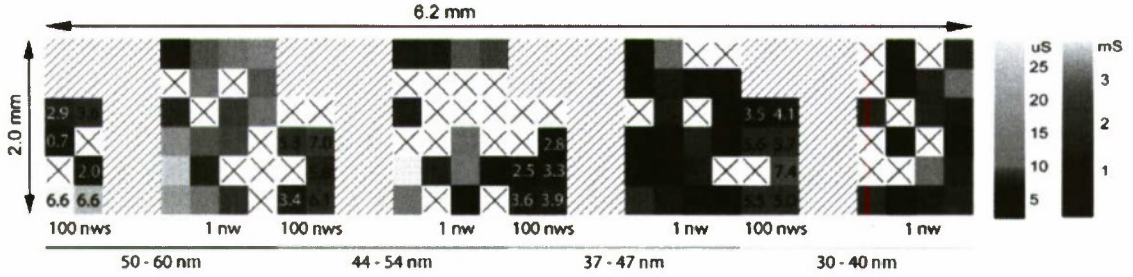

Figure 5. Wafer map showing maximum transconductance for transistors with 1 nanowire and nominally 100 nanowires, for different nanowire diameters between 30 to 60 nm. For the 100 nanowire FETs, the number indicate maximum f_t. X indicates a broken device.

In order to obtain a good fit, the current source controlled by V_{gs} has a different sign as compared with the HEMT in [6], i.e. the effect of the hole accumulation decreases as V_{gs} is increased. This can be understood as a lowering of the gate-source potential for the trapped holes, making it easier for the holes to escape into the source. In contrast, the main leakage mechanism for the holes in a HEMT is towards the gate electrode, which is isolated in our case through the gate oxide. An interesting approach that can be used for a vertical nwFET is to introduce a heterostructure in the channel [7] to suppress impact ionization and band-to-band tunneling, similar to the wide band gap collector used for double heterostructure bipolar transistors.

As shown in Fig.3, good agreement between modeled and measured h_{21} and *MSG* are also obtained. We further extract a total gate capacitance of C_{gg}= 42fF, as well as a source resistance of 3.2 kΩ and a drain resistance of 2.1 kΩ per wire.

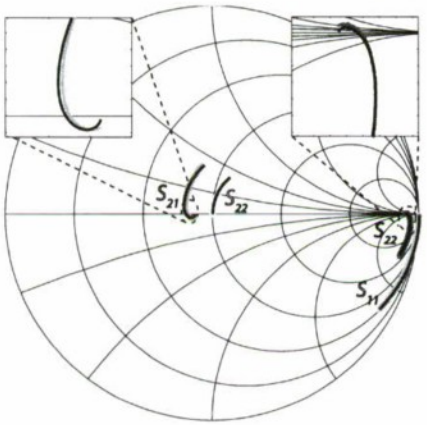

Figure 6. Measured (thick) and modeled (thin) S-parameters at V_{ds}=0.8V and V_{gs}=-0.5V. The frequency span is 110MHz to 20 GHz. The insets display S_{21} and S_{22} at low frequencies, showing the effect of impact ionization.

C. Wafer statistics

Figure 6 shows a wafer map showing g_m for 1 nanowire and nominally 100 nanowire FETs. For the FETs containing a larger amount of wires, we obtain a yield of roughly 77%, with a mean f_t of around 4.5GHz. A fairly high yield in spite of the early stage of process development can thus be achieved.

IV. Performance Modeling

A. Modeling of measured capacitance data

Due to the optical lithography used, the electrode line width of the device is 20 µm. This leads to a large electrode overlap, which, due to the vertical geometry, can give large extrinsic parasitic capacitances, $C_{gd,mm}$ and $C_{gs,mm}$ as indicated in Fig. 1a. For the used device geometry, we have calculated the intrinsic and extrinsic gate capacitances. The intrinsic gate capacitance, $C_{gg,i}$, has been evaluated using a Schrödinger-Poisson solver in the effective mass approximation, yielding $C_{gg,i}$=6.4 fF. The extrinsic pad-pad, $C_{xx,mm}$, and pad-wire, $C_{xx,mw}$, capacitances have been calculated using 3D FEM electrostatic modeling for the regions in the vicinity of the wires and analytical expressions for the larger parallel-plate like areas.

From the calculations, we obtain a total gate capacitance of $C_{gg,model}$=41.4 fF, which is in excellent agreement with the measured value of C_{gg}=42 fF. The intrinsic capacitance thus only makes up 15% to the total value. Also, we find that 70% of $C_{gg,model}$ originates from pad-pad capacitance. In the present layout, the source-gate and drain-gate electrode overlap is 196 µm^2 and 110 µm^2 respectively, while the area covered with wires is only 12.5 µm^2. A large reduction in the pad-pad capacitance is thus foreseen using narrower source and drain leads.

B. Optimization of layout

While the effects from parasitic capacitances are well known for different planar FET geometries, there is only little information for *vertical* nanowire FETs. We have therefore investigated the parasitic gate capacitances in different nanowire geometries using electrostatic 3D FEM modeling. It

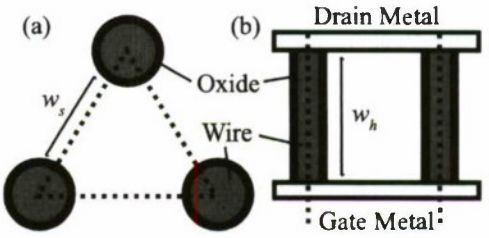

Figure 7. Layout for electrostatic FEM calculations of the parasitic gate capacitances. Top view (a) and side (b) view, where w_s and w_h are the wire spacing and the height. The dashed line is the edge of the unit cell, to which periodic boundary conditions are applied.

The modeling shows that by using a dense nanowire array, both the parasitic gate-wire and gat-pad capacitance can be minimized. To illustrate this effect, we first model the gate capacitance of a triangular nanowire unit cell, as illustrated in Fig. 7.

The nanowires are modeled as metallic elements with r_w=15nm, which are coated with a high-κ oxide with t_{ox}=10nm and ε_r=25. The space between the wires is filled with a low-k dielectric medium with ε_r=3.9. We vary the wire height (w_h), or equivalently the gate-pad distance between 30 and 500nm, as well as the distance between the nanowires in the unit cell (w_s), that also varies between 30 and 500nm. By numerically solving Laplace's equation, we can calculate the parasitic capacitance between the gate metal, wires and drain metal. The calculated total parasitic gate capacitance is shown in Fig. 8.

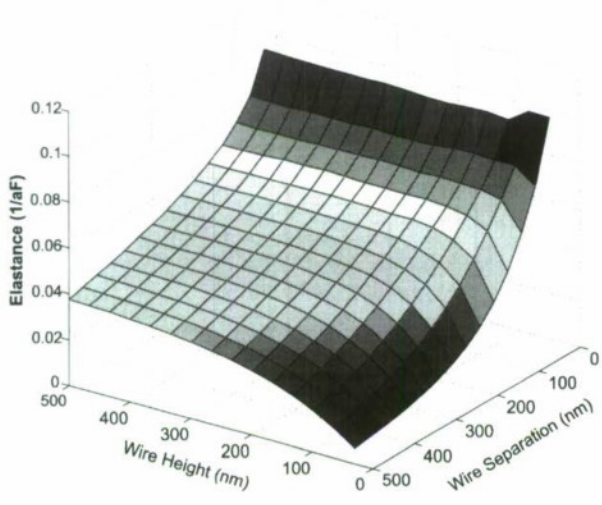

Figure 8. Calculated parasitic elastance (1/C) for a triangular nanowire unit cell, as a function of both wire spacing and wire height. A strong reduction in the calculated capacitance is achieved for a small wire separation

As is clearly visible, the parasitic gate capacitance decreases with decreasing wire separation. Also, for small wire separations, the capacitance becomes independent of the wire height. For tight wire spacing, the electric field is screened by the wires, and is strongly localized at the wire-gate metal region. Since the capacitance is related to the volume integral of the electrical energy, the localization leads to a reduced capacitance. Also, the screening makes the capacitance independent of the wire height. For a large wire separation, the capacitance is large, and follows essentially a $1/w_h$ dependence. In this case, the FET resembles a parallel plate capacitor perturbed by a small wire. A vertical nanowire FET layout thus requires very tightly spaced nanowires. This allows for both small parasitic capacitances, as well as short wire leads which limit the source and drain resistance.

For calculations of a real device structure containing a finite amount of wires, the complete device structure has to be simulated. We propose a vertical FET structure similar to a transfer substrate HBT [8], with a two densely spaced rows of wires using narrow source and drain leads and a vertical T-gate. The simulations show that the best performance is achieved by reducing the intra-wire spacing, essentially down to same scale as the wire diameter, similar to that of the triangular nanowire unit cell. For an device with an wire radius of 10nm, a t_{ox}=5 nm, a gate length L_g=33 nm and a spacing of 10 nm, we numerically obtain an intrinsic C_{gg}=100aF/μm, and extrinsic parasitic capacitances $C_{gs,parasitic}$=$C_{gd,parasitic}$=200 aF/μm. As for planar FETs, the parasitic capacitances are larger than the intrinsic. Assuming an intrinsic g_m=3 mS/μm [9] and realistic source and drain contact resistivities, we calculate a f_t and f_{max} above 700 GHz. Similar performance as for planar FETs can thus be achieved for vertical FETs, assuming that the wire spacing can be made sufficiently small.

V. Conclusions

We have fabricated and performed RF-measurements on vertical InAs nanowire MOSFETs with L_g=100 nm. A maximum f_t=7.6 GHz and f_{max}=22 GHz are obtained, mainly limited by large parasitic capacitances. 3D electrostatic simulations of the vertical nanowire FET indicate that good device performance is obtained by using arrays of tightly spaced wires, and that for a realistic device geometry RF performance similar to that of an HEMT should be possible.

Acknowledgment

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SELECTIVE UNDERCUT ETCHING FOR ULTRA NARROW MESA STRUCTURE IN VERTICAL InGaAs CHANNEL MISFET

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Abstract

It is important for shrinking the mesa width of a channel region in a vertical InGaAs channel MISFET for carrying out high-speed operation and for obtaining a steep sub-threshold slope. Therefore, we introduced selective undercut etching after the dry etching of the mesa structure. In the fabricated device with 60-nm-long channel, the channel mesa width became 15 nm. The maximum drain current density at V_{ds} = 0.75 V and V_g = 1.5 V was 1.1 A/mm and the maximum transconductance at V_{ds} = 0.75 V and V_g = 0 V was 530 mS/mm.

I. Introduction

High speed operation in transistor has been demanded because of the development of communication technology. In general, III-V compound semiconductors that have lighter effective mass and higher electron mobility than Si have advantage for high speed operation. Especially, InP based heterojunction bipolar transistor obtained the highest cutoff frequency [1]. However, the base layer of HBTs is heavily doped; the electrons emitted from the emitter are scattered by plasmons in the base layer [2]. If we introduce intrinsic semiconductor for channel region, higher speed operation than HBTs is expected. According to a Monte Carlo simulation [3], the estimated speeds of electrons are over 7.5×10^7 cm/s in a 60 nm channel length. When the current density is over 1 MA/cm^2, a cutoff frequency of over 1 THz can be expected. However, the ultra narrow mesa structure is essential for the good drivability in the devices. The narrow mesa can provides a short charging time for high speed operation and steep sub-threshold slope for logic circuit applications. A 20-nm-wide channel mesa is assumed in the calculation.

To demonstrate the proposed structure, we fabricated a device that has a 120-nm-long channel [4-6]. In our former trial, current-voltage characteristics were not observed in the device with a 20-nm-wide mesa structure, although we observed 400 mA/mm at a 50-nm-wide mesa structure [6].

The observed maximum drain current density was 1 A/mm at a 60-nm-wide mesa structure [6]. However, calculated maximum drain current density by using simple model was 2.4 A/mm at a 60-nm-wide mesa structure [4].The increase in the current density was 600 mA/mm when the source width was increased from 50 nm to 60 nm. This is close to the calculated increase in the current density, i.e., 400 mA/mm with an increase of 10 nm in width. Thus, the mesa width operated in theory might only be 10 or 20 nm.

Our device was fabricated by the top down process and inductive coupling plasma reactive ion etching (ICP-RIE) was used to form the vertical mesa structure. Thus, the sidewall of the channel and source might be damaged by plasma. When the lateral damaged depth is about 20 nm, we could explain the observed current reduction.

As another reason of reducing the current, Fermi level pinning might limit the source region. The width of the depletion layer caused by Fermi level pinning is estimated as 17 nm when the source doping concentration is 2×10^{18} cm^{-3} and the pinning level of InP is 0.9 eV from the top of the valence band [7].

In this report, we introduced selective undercut etching of InGaAs channel region after dry etching to form the ultra narrow mesa structure and to remove the plasma damaged region. By this selective etching, we could fabricate 15-nm-wide channel mesa structure.

II. Device Structure

Schematic structure of fabricated device is shown in Fig. 1.

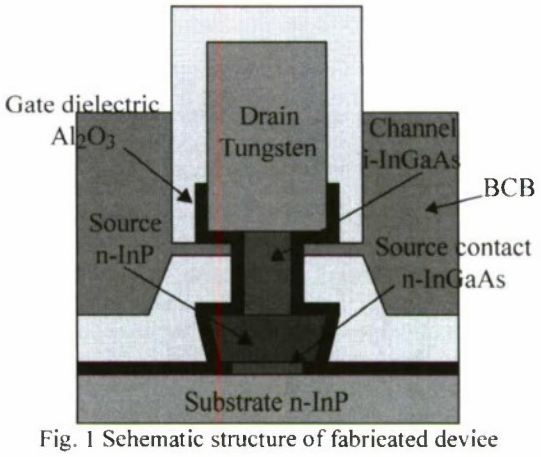

Fig. 1 Schematic structure of fabricated device

The specifications of this device are as follows—source thickness: 40 nm; channel length: 60 nm; source mesa width: 75 nm; channel mesa width: 20 nm; source doping concentration: 5×10^{18} cm^{-3}; and an undoped channel region. Because there is InP/InGaAs hetero interface between source and channel, hot electrons are launched from source to channel. We use high-k material, Al_2O_3, for gate dielecric. Finally, drain electrode was tungsten for schottky contact to channel.

The etchant for the undercut require the feature of selectivity between InGaAs and InP. Moreover, to achieve

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vertical sidewall of channel region, the etchant also has anisotropic feature. Thus, the etchant for the undercut is phosphoric acid solution (H_3PO_4:H_2O_2:H_2O = 1:2:40) [8]. The etching speed of this etchant in the <01-1> direction is two times slower than that in the <-100> direction. The etching of InP was not observed in our experiment. Thus, the etching rate of InP was much slower than that of InGaAs. The result of undercut etching after fabrication of the mesa structure by ICP-RIE is shown in Fig. 2.

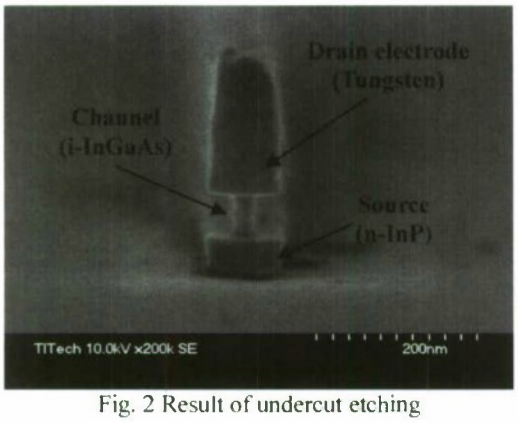


Fig. 2 Result of undercut etching

20-nm-wide channel mesa structure with vertical sidewall could be fabricated. The width of undercut was about 30 nm. Therefore, we might remove plasma damaged region and lead to high drivability with narrow channel mesa structure.

The width of channel mesa structure is narrower than the width of source mesa structure by this undercut etching. The estimated deplesion layer width by Fermi level pinning is 12 nm in the result of deplesion approxymation. The estimated width is narrower than previous estimation, because source doping concentration was increased to 5×10^{18} cm^{-3}. Therefore, if the undercut width is 30 nm, the influence of Fermi level pinning might be neglected.

To observe the drain current modulation, we must form the gate stack of gate dielectric and gate metal to the undercut region. At first we used sputtered Ti for formation of gate metal [5].

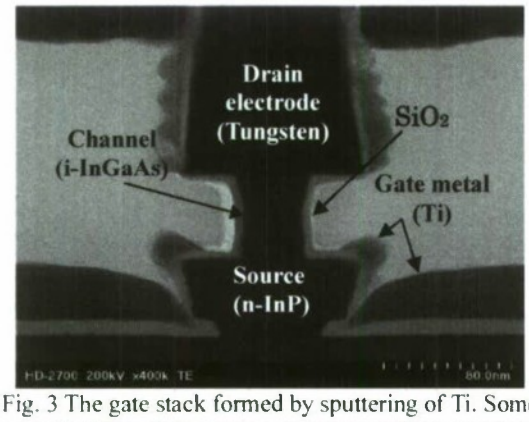


Fig. 3 The gate stack formed by sputtering of Ti. Some non-uniformity of dielectric was observed because SiO_2 deposited by plasma enhanced chemical vapor deposition was used. The mesa width was not so narrow because this test pattern was fabricated from wider mask pattern.

The gate metal was not formed to the sidewall of the channel mesa structure as shown in Fig.3. The drain current modulation by gate bias was observed in fabricated device shown in Fig. 3. But the controllability of the gate was poor. The observed transconductance was 110 mS/mm, although 4 S/mm was estimated in the simple calculation.

As form of gate metal was difficult by sputtering, we change this process to the angled evaporation. The result of angled evaporation with an incident angle of 60° is shown in Fig. 4.

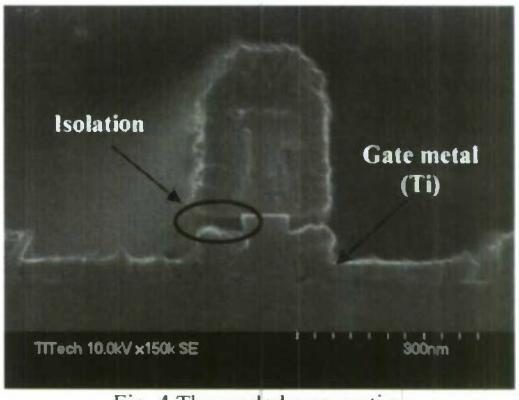


Fig. 4 The angled evaporation

As shown in Fig. 4, we could form the gate metal to the sidewall of the channel mesa structure. Moreover, the gate metal and the drain electrode can be isolated in the self-alignment manner by using a 30-nm undercut in the channel region. In the past process, the gate metal and the gate dielectric deposited to the top of the mesa structure were removed by BHF [5]. However, as the etching rate of the gate metal was not so controlable, the overlap of gate electrode to drain electrode was ineluctable. Therefore the capacitance between gate and drain was increased. By introduction of the self-alignement isolation, we could prevent the increase of the capacitance between gate and drain.

As the 20-nm-wide mesa structure and the gate stack to the undercut region were confirmed, we fabricated the proposed device. Fabrication processes are as follows. After growth of the n-InGaAs source contact layer, the n-InP source layer and 60-nm-thick i-InGaAs channel layer are fabricated by metal organic vapor phase epitaxy and the 250-nm-thick tungsten drain electrode was deposited by sputtering. A 75-nm-wide Cr line was formed on the tungsten surface by electron beam lithography and the liftoff process. The length of the line was 5 μm. The tungsten layer was etched by CF_4 RIE using the Cr line as an etching mask. Then, the i-InGaAs layer and a part of n-InP layer were etched by CH_4-H_2 ICP-RIE using the Cr line as the etching mask again. The remained n-InP was etched by hydro chlolic acid solusion (HCl:H_3PO_4 = 1:7). The Ti/Pd/Au source contact electrode was formed on the n-InGaAs surface. After undercut etching by phosphoric acid solution, a 7.5-nm-thick Al_2O_3 layer was deposited by atomic layer deposition in 250 °C. The gate insulator on the top of the drain electrode was eliminated by the combination of photoresist coating, etchback, and etching by BHF [9]. After the removal of the photoresist, the Ti/Au gate electrode was deposited by tilted evaporation with an incident angle of 60°. After the gate formation, the mesa was completely buried in the BCB

insulating layer, and annealed 1 hour in 250 °C at nitride atmosphere. After the etchback process was carried out to expose the drain electrode, the Ti/Au electrode pad was formed.

III. Results and Discussion

SEM image of fabricated device is shown in Fig. 5.

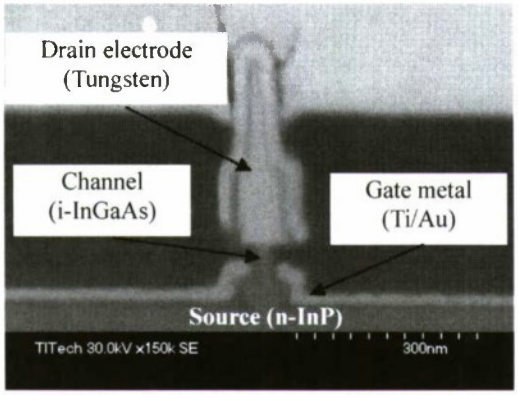
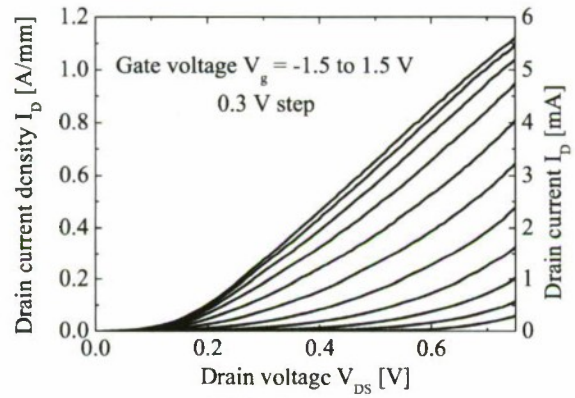


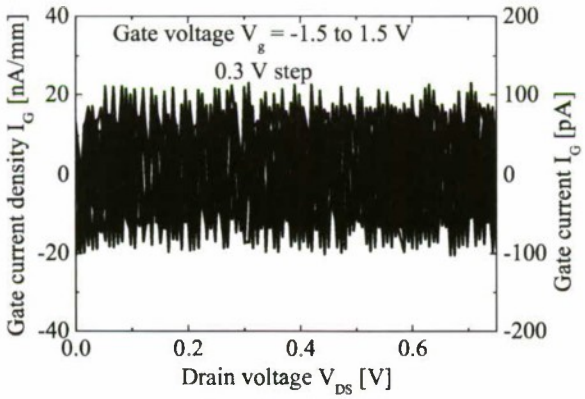
Fig. 5 SEM cross-sectional image of fabricated device

The channel mesa width was 15 nm. This is narrowest mesa width fabricated by top down process in III-V vertical transistors to our knowledge. The isolation between gate metal and drain electrode was also confirmed.

The common source characteristics are shown in Fig. 6.



(a) Drain current



(b) Gate current

Fig. 6 Common source charancteristics of fabricated device

The maximum drain current density at V_{ds} = 0.75 V and V_g = 1.5 V was 1.1 A/mm. Because channel mesa width is 15 nm, the maximum drain current density per width corresponds to 7 MA/cm^2. This value is enough for high speed operation in our calculation [3].

I_d-V_g and g_m-V_g characteristics are shown in Fig. 7.

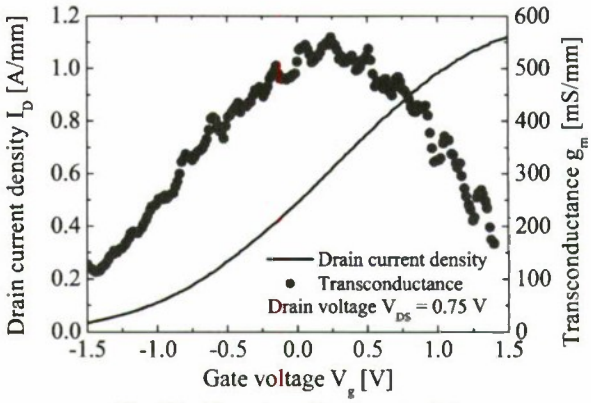


Fig. 7 I_d-V_g and g_m-V_g characteristics

From Fig. 7, the maximum transconductance at V_{ds} = 0.75 V and V_g = 0 V was 530 mS/mm. The sub-threshold slope was 650 mV/dec.

The estimated values by using simple calculation [4], were 1.9 A/mm as maximum drain current and 3.3 S/mm as maximum transconductance. These values are larger than observed values. Thus we considered the quantum reflection and tunnel effect in the calculation. The maximum drain current density and the maximum transconductance became 1.3 A/mm and 1.3 S/mm, respectively. The estimated maximum drain current density is almost equal to the value in the experiment in spite of the calculation is assumed pure ballistic transportation.

On the other hand, the maximum transconductance of experiment was smaller than that in the calculation. As described in a literature [10], Al_2O_3 requires adequate annealing for good interface characteristics. Although the wafer was annealed in 250 °C to cure BCB in our fabrication process, this was not be optimized for Al_2O_3 anneal condition. There might be some interfacial traps between Al_2O_3 and InGaAs or InP to terminate the electric field from the gate electrode.

The calculated sub-threshold slope with 15-nm-wide mesa structure and 60-nm-long channel was 100mV/dec. The calculated value is steeper than the observed result. This might be also influenced by interface trap.

IV. Conclusion

We introduced selective undercut etching after the fabrication of the mesa structure. In fabricated device, the channel mesa width became 15 nm and the maximum drain current density at V_{ds} = 0.75 V and V_g = 1.5 V was 1.1 A/mm. This current density per width corresponds to 7 MA/cm^2 from the cross section of the channel. The maximum transconductance at V_{ds} = 0.75 V and V_g = 0 V was 530 mS/mm.

Acknowledgement

We thank Professors S. Arai, M. Asada, M. Watanabe, and N. Nishiyama for helpful discussions and encouragement.

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RTD OSCILLATORS AT 430-460 GHz WITH HIGH OUTPUT POWER (~200 μW) USING INTEGRATED OFFSET SLOT ANTENNAS

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***Abstract*— We demonstrated the operation of GaInAs/AlAs resonant tunneling diode (RTD) oscillators with high output power (100–200 μW) at frequencies of 430–460 GHz using an offset-fed slot antenna, in which the RTD was placed 45 μm from the center of a 100-μm-long antenna. The highest output power obtained in this study was 200 μW at 443 GHz for a single RTD with a peak current density of 18 mA/μm^2. The output powers of 50-130 μW at frequencies of 460-490 GHz were also obtained in the oscillators with different structure. Higher output is expected by optimizing the position and mesa area of the RTD and the antenna length.**

I. INTRODUCTION

The terahertz (THz) frequency range has been receiving considerable attention because of its various applications such as ultrahigh-speed wireless communication, imaging, and spectroscopy [1]. Compact and coherent solid-state light sources are key components in these applications. Quantum cascade lasers oscillating in the THz range have been developed [2-4], and the development of electron devices operating in this range is also being pursued from the millimeter-wave side.

Resonant tunneling diodes (RTDs) have been considered as one of the potential candidates for THz oscillators operating at room temperature [5-7]. We recently observed 831 GHz fundamental oscillation in InGaAs/AlAs RTDs [8]. However, the output power of these RTD oscillators is usually small (on the order of 1–10 μW) even at the fundamental oscillation. This is because antennas that are considerably shorter than their own resonance lengths have to be used for high-frequency oscillation owing to the RTD capacitance. These antennas have low radiation conductance, and thus, the output power is low.

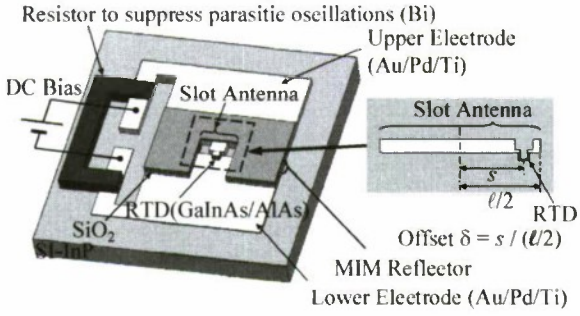

Fig. 1 RTD oscillator with offset slot antenna.

We previously proposed RTD oscillators with offset-fed slot antennas for simultaneously achieving high frequency and high output power [9]. In this paper, we demonstrated oscillations with high output power (50-200 μW) at frequencies of 430–490 GHz using an offset-fed slot antenna and an RTD having high current density.

II. DEVICE STRUCTURE

The structure of an RTD oscillator integrated with a slot antenna is shown in Fig. 1. An InGaAs/AlAs double-barrier RTD on a semi-insulating InP substrate was placed in the slot antenna with an offset from the center of the slot. The frequency was dominantly determined by the shorter portion of the slot antenna, while the output power was dominantly determined by the longer portion of the slot antenna [9]. Because the radiation conductance is almost independent from the resonance frequency, high output power is expected.

To apply a DC bias voltage to the RTD and generate a high-frequency standing wave in the slot simultaneously, metal-insulator-metal (MIM) reflectors were placed at both ends of the slot. A resistor made of a bismuth film was connected in parallel to the RTD outside the antenna electrodes to suppress low-frequency (2–3 GHz) parasitic oscillations of the external bias circuits.

The layer structures of the RTD and current-voltage characteristics are shown in Fig. 2(a) and (b), respectively. The RTD was grown by metal-organic vapor-phase epitaxy [10]. Except for the cap and well layers, the InGaAs layers were lattice-matched to InP. The cap and well layers were made of compressively strained $In_{0.7}Ga_{0.3}As$ and $In_{0.8}Ga_{0.2}As$, respectively. The contact resistance of the electrode on the cap layer was reduced by the strained composition with a high doping concentration. The first resonant level and peak voltage were reduced by the strained well structure [11]. A high

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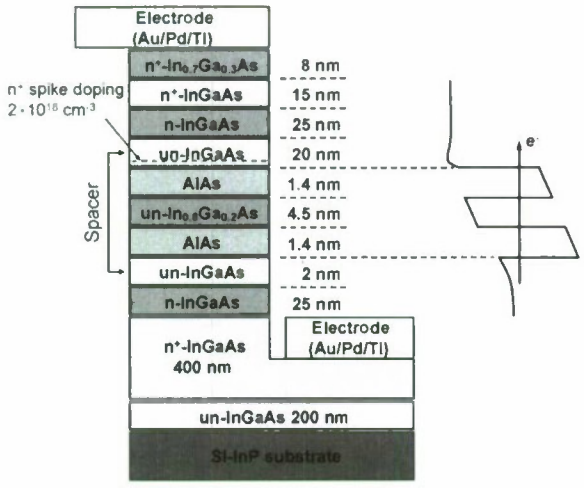
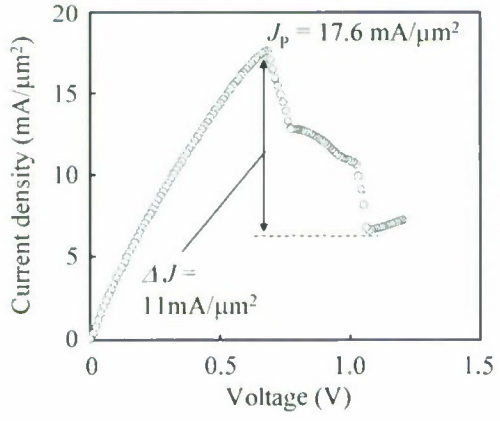
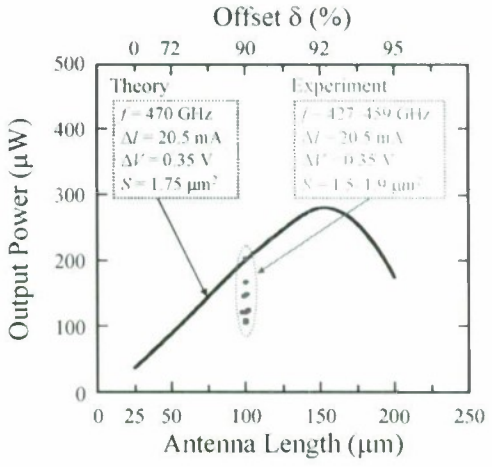


(a)

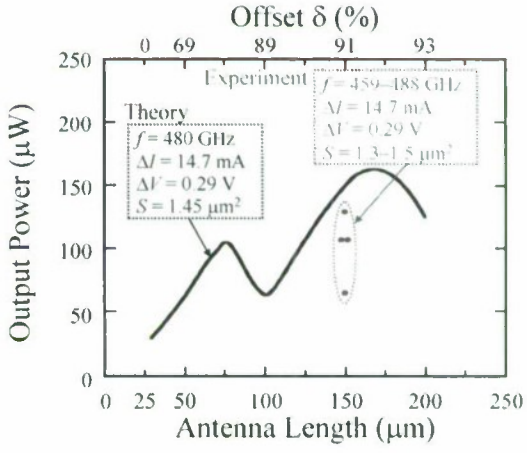


(b)

Fig. 2(a) Layer structure of RTD with spike doping, and (b) current-voltage characteristics.



(a)



(b)

Fig. 3 Experimental results and theoretical calculation of the output power as a function of antenna length for RTDs with different mesa areas of (a) ~1.75 μm², (b) ~1.45 μm².

emitter doping concentration and thin barriers were introduced to achieve high current density [8]. A 20-nm-thick spike-doped collector spacer was used, as shown in Fig. 2(a), to introduce a built-in potential and reduce the peak voltage [12]. Although, the voltage at the current peak of the RTD without spike doping was 0.94 V, as described in [8], the reduced peak voltages of 0.66 V is achieved by spike doping structure. The current direction used in the experiment was from the substrate to the top layer. The peak current density and peak-to-valley current ratio were 18 mA/μm² and ~3, respectively, as shown in Fig. 2(b). The mesa area of the RTD was 1.3–1.9 μm².

In this study, the output power was measured at the substrate side of the RTD oscillator through a hemispherical Si lens with a diameter of 30 mm and an off-axis paraboloidal mirror. A calibrated He-cooled Si composite bolometer was used as a detector. The total output power radiated from the slot antenna was estimated from the detected signal by taking into account the calculated radiation pattern of the antenna and the collection efficiency of the system including the Si lens and paraboloidal mirror. The estimated total output power might be reduced by the possible imperfect alignment of the system. Oscillation spectra were measured using a Fourier transform infrared spectrometer. Measurements were performed under a pulsed current condition by a lock-in technique to eliminate the surrounding noise from the detector, although the device can also operate under

continuous current conditions. The pulse duration was 0.3 ms, and the repetition frequency was 300 Hz.

To define the position of the RTD in the slot antenna, we introduced an offset δ; $\delta = s/(\ell/2)$, where s is the distance of the RTD from the center of the antenna and ℓ is the antenna length, as shown in Fig. 1. Although the maximum s is equal to $\ell/2$ in principle, it is less than $\ell/2$ in an actual structure owing to the finite areas of the RTD and upper electrode.

III. Experimental Results

The experimental results of the output power for oscillators with different structure were shown in Figs. 3(a) and (b). The antenna length ℓ (with offset δ) and mesa areas were (a) 100 μm (90 %) and ~1.75 μm^2, and (b) 150 μm (91 %) and ~1.45 μm^2. Same RTD structure, as shown in Fig. 2, was used in (a) and (b). Oscillations were obtained at (a) 427–459 GHz with output powers of 100–200 μW and (b) 459–488 GHz with 50–130 μW in single RTDs. The variation in the frequency was attributed to that in the mesa area of the RTD. The highest output power of 200 μW was obtained at 443 GHz in (a). The DC-to-RF conversion efficiency of this device was 0.18% and 1.1% with and without the external bismuth resistor, respectively, as shown in Fig. 1(a). The latter efficiency was comparable to that of oscillators with high-electron-mobility transistors (HEMTs) operating in the 300 GHz range [13]. The bismuth resistor was not optimized in the present study; furthermore, it could be replaced with an optimized circuit without the loss of bias current, as described in [14]. The highest oscillation frequency of 488 GHz with 128 μW was obtained in (b). The oscillation frequencies of (b) were slightly higher than that of (a), mainly because of the smaller mesa areas, although the antenna length and the offset amount were different.

III. Theoretical Calculation

The theoretically calculated output power is also shown in Fig. 3 as a function of the antenna length at a fixed oscillation frequency. The distance of the RTD from the center of the antenna was changed along with the antenna length to maintain the frequency at a constant value, as indicated by the offset δ on the upper horizontal axis of Fig. 3. The theoretical analysis was carried out in the same manner as that in [7]; the parasitic elements and the effect of tunneling and transit times were taken into account and the admittance of the antenna at the RTD terminals was calculated using a three-dimensional electromagnetic simulator (Ansoft HFSS). The real part of antenna admittance consists of radiation conductance, conduction loss, and loss due to penetration into the MIM reflectors. The following parameter values were used to plot the theoretical curve: the current width ΔI and voltage width ΔV of the negative differential conductance (NDC) region were (a) 20.5 mA and 0.35 V, and (b) 14.7 mA and 0.29 V, respectively, and the mesa areas of the RTD, S, were (a)

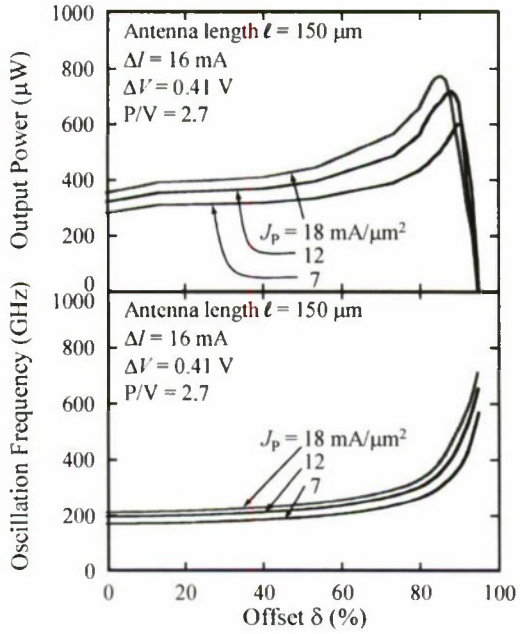


Fig. 4 Calculated output power and oscillation frequency as a function of offset.

1.75 μm^2 and (b) 1.45 μm^2. The narrower voltage width is obtained in (b) due to the increment of the contact resistance in fabrication process. Increased contact resistance was taken into account in the calculation of (b).

As shown in Fig. 3, the experimental results for the oscillation frequency and output power were in good agreement with the theoretical calculation. In Fig. 3(a), the theoretical output power rapidly increased as the antenna length was increased, and it reached the maximum value corresponding to the increase and peaking of the radiation conductance. However, the impedance matching between RTD and antenna wasn't achieved at the peak. Because the real part of antenna admittance was less than half the absolute value of the NDC [7], although the increase of radiation conductance with increasing antenna length.

In Fig. 3(b), the theoretical curve has two peaks. At the peak located around 75 μm, the impedance matching between the RTD and the antenna was achieved. However, the output was smaller than that of the other peak, because the proportion of radiation conductance was smaller in the real part of antenna admittance. The same situation of increasing and peaking of radiation conductance, as that described above for the theoretical curve in Fig. 3(a), occurred at the other peak located at around 170 μm. Because the experimental results did not provide the maximum values in both (a) and (b), higher output power is expected by adjusting the antenna length and the offset.

To demonstrate the possibility of higher output powers, Fig. 4 shows theoretical calculations of the dependence of the output power and oscillation frequency on the offset δ for various peak current densities with a fixed antenna length. In this analysis, ΔI and ΔV were assumed to be

constant for all the curves, while the mesa areas of the RTDs were different. The antenna length was 150 μm. As shown in Fig. 4, the output power and frequency simultaneously increased with δ. The frequency was dominantly determined by the susceptance (imaginary part of the admittance) of the smaller portion of the slot antenna, as viewed from the RTD, while the output power was dominantly determined by the conductance of the longer portion of the slot antenna, as viewed from the RTD [9]. The output power was maximum when the radiation conductance reached its peak.

As observed in Fig. 4, oscillation at 400 GHz with an output power of 760 μW was expected for an offset of 65 μm (87% of the half length of the antenna) and a peak current density J_P of 18 mA/μm^2. Oscillation at 600 GHz with an output power of 230 μW is expected at δ = 93% and J_p = 18 mA/μm^2. In general, the output power at a certain frequency can be maximized by optimizing the antenna length, offset, and mesa area of the RTD for given widths of current density and voltage of the NDC region.

Theoretically, the maximum output power that can be produced from an RTD is $(3/16)\Delta I/\Delta V$ if the radiation conductance equals half the absolute value of the NDC of the RTD and also if the effect of the parasitic elements is negligible [7]. The highest power obtained in the present experiment (Fig. 3(a)) corresponded to 15% of this value (1.34 mW). Even at the peaks of the theoretical curves in Figs. 3 and 4, the output power was still less than the maximum available power mentioned above, because the radiation conductance was less than half the absolute value of the NDC. To control the value of radiation conductance is possible by changing the antenna width. In this study, the antenna width was fixed at 4 μm. Therefore, further improvement of output power is expected to achieve an impedance matching between the RTD and the antenna for increasing radiation conductance by changing antenna width.

IV. Summary

We demonstrated the operation of RTD oscillators with high output power (50–200 μW) at frequencies of 430–490 GHz using an offset-fed slot antenna, in which the RTD was placed at a certain distance from the center of the slot. The highest output power obtained in the study was 200 μW at 443 GHz for a single RTD with a peak current density of 18 mA/μm^2. The output power obtained here is considerably higher than that obtained for conventional RTD oscillators in the sub-THz range, and thus, these RTD oscillators are expected to be very useful for many applications.

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MONTE CARLO STUDY OF STRAIN EFFECT ON HIGH FIELD ELECTRON TRANSPORT IN InAs AND InSb

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Abstract

We calculate the unstrained and the strained band structures of InAs and InSb by means of the empirical pseudopotential method. The impact ionization threshold energy, E_{th}, is calculated while keeping the energy and momentum conservation. Then the electron transport in the unstrained and the strained InAs and InSb is investigated by using the Monte Carlo (MC) method. In both InAs and InSb, the average electron velocity, v_d, increases monotonically with the electric field strength, f. The tensile strain makes the low field electron mobility, μ, higher, and vice versa, which is resulted from the dependence of the effective mass in the Γ valley, $m_{\|}^{*}(\Gamma)$, on the strain. At the high f, many electrons are restricted within the bottom of the Γ valley because of losing most of their energy by the impact ionization, which results in keeping v_d large at the high f. The tensile strain makes E_{th} smaller and then the impact ionization coefficient, α, larger, and vice versa. Consequently, v_d at the high f becomes larger under the tensile strain and smaller under the compressive strain.

I. Introduction

III-V narrow band gap semiconductors such as InAs and InSb have showed extremely high electron mobility because of their small electron effective mass, which has brought about an increasing interest in themselves as promising channel materials for future logic, communication and terahertz devices [1]-[3]. When they have been used as channels, strain has been likely to accompany them owing to lattice mismatch between channel and substrate. The strain has influenced the carrier mobility through the change of band structures [4]. In the Si MOSFETs, the strain has been used intentionally to increase the carrier mobility in the channels [5]. On the other hand, the small band gap energy of the narrow band gap semiconductors has resulted in promoting impact ionization, which has influenced the electron transport under the high electric field [6]-[8]. The strain has also influenced the impact ionization through the change in conduction and valence band structures [9]. In this paper, we calculate the band structures of the strained InAs and InSb. Then the effect of the strain on the impact ionization is investigated. Finally the electron transport under the high electric field in the strained InAs and InSb is investigated by using the Monte Carlo (MC) method.

II. Simulation Methodology

A. Band Calculation with Strain

We assume that the channel (*i.e.*, InAs and InSb) is on (001) substrate. The lattice constant of the channel parallel to the (001) plane, $a_{\|}$, is assumed to be the same as that of the substrate, a_s, and then the biaxial strain is applied on the channel when the substrate is lattice-mismatched. The strain ratio of the channel, $\varepsilon_{\|}$, is defined as:

$$\varepsilon_{\|} = \frac{a_0 - a_s}{a_s} \tag{1}$$

where a_0 is an original lattice constant of the channel without the strain. The lattice constant of the channel perpendicular to the (001) plane, $a_{\perp}$, is calculated by the elastic theory as [10]:

$$a_{\perp} = a_s\left(1 - 2\frac{c_{12}}{c_{11}}\varepsilon_{\|}\right) \tag{2}$$

where c_{11} and c_{12} are elastic constants. The band structure of the channel is calculated by means of the empirical pseudopotential method [11]. We take account of the strain effect on the band structure by means of the rigid ion approximation [12]-[13], where the change of pseudopotential by the strain solely arises from the change of cell volume as:

$$V'(\mathbf{G}) = \frac{a_0^3}{a_s^2 a_{\perp}} V(\mathbf{G}) \tag{3}$$

where $V'(\mathbf{G})$ and $V(\mathbf{G})$ are the pseudopotential with and without the strain, respectively. Then the local pseudopotential form factors at the strained reciprocal lattice vectors, $V'(\mathbf{G}')$, are reconstructed by performing a cubic spline interpolation through $V'(\mathbf{G})$.

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B. Impact Ionization Threshold

The impact ionization is a process in which the electron accelerated under the high electric field excites an electron from the valence band to the conduction band. The minimum energy of the electron required for the impact ionization, which is consistent with both energy and momentum conservation, is defined as threshold energy, E_{th}. In the work, E_{th} is calculated by searching a pair of electrons and hole that conserve both energy and momentum throughout the conduction and the valence bands [14]. Because of rather inaccuracy of the empirical pseudopotential method regarding the band gap energy, we adopt the empirical formula for it [15].

C. Monte Carlo Simulation

The band parameters such as effective mass, non-parabolicity parameter, valley separation *et al.* are extracted from the calculated unstrained and strained band structures along the fundamental axes, and these are employed in the MC simulation. In the MC simulation, three-valley (Γ, L, X) conduction band models are assumed [16]. The scattering mechanisms that are taken into account are acoustic, polar optical, non-polar optical phonons and the impact ionization. The scattering probability for the impact ionization, I, is calculated using the Keldysh formula as [17]:

$$I = S\left(\frac{E - E_{th}}{E_{th}}\right)^2 \tag{4}$$

where E is the electron energy, E_{th} is the threshold energy calculated according as Sec. II. A, and S is an impact ionization factor. We assume $S = 1\times10^{12}$ s^{-1}, which is well used in the narrow band gap semiconductors [6]-[8].

III. Simulation Results

A. Band Calculation

First, the unstrained and the strained band structures of InAs and InSb are calculated. Fig. 1 shows the calculated conduction band structures along [100] ([010]), [111] or [001] directions, where the biaxial tensile ($\varepsilon_{\parallel}$ = +1 %) or compressive ($\varepsilon_{\parallel}$ = −2 %) strains that are parallel to the (001) plane are assumed. In both InAs and InSb, the effects of the tensile and the compressive strains on the band structure are opposite, *i.e.*, the tensile strain ($\varepsilon_{\parallel} > 0$) makes the curvature around the Γ point smaller and the Γ-L and the Γ-X valley separations larger, and vice versa. The electron effective mass in the Γ valley along the [100] ([010]) direction, $m_{\parallel}^{*}(\Gamma)$, and the [001] direction, $m_{\perp}^{*}(\Gamma)$ are calculated. Fig. 2 shows the dependence of $m_{\parallel}^{*}(\Gamma)$ and $m_{\perp}^{*}(\Gamma)$ on $\varepsilon_{\parallel}$ for InAs and InSb. $m_{\parallel}^{*}(\Gamma)$ and $m_{\perp}^{*}(\Gamma)$ in InSb are smaller than those in InAs, which shows InSb to be the material of higher electron mobility. According to the change of the curvature around the Γ point, $m_{\parallel}^{*}(\Gamma)$ and $m_{\perp}^{*}(\Gamma)$ become smaller under the tensile strain ($\varepsilon_{\parallel} > 0$) and larger under the compressive strain ($\varepsilon_{\parallel} < 0$). It is seen that the difference

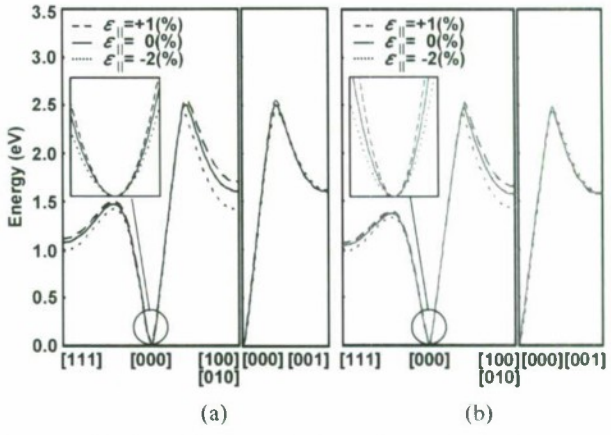

Fig. 1 Unstrained and strained conduction band structures of (a) InAs and (b) InSb along [100]([010]), [111] or [001] directions. Strain ratio, $\varepsilon_{\parallel}$, is varied as -2, 0 or +1 %.

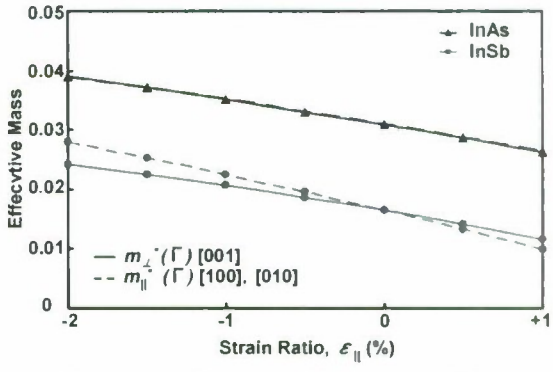

Fig. 2 Dependence of electron effective mass in Γ valley along [100] ([010]) direction, $m_{\parallel}^{*}(\Gamma)$, and [001] direction, $m_{\perp}^{*}(\Gamma)$ on $\varepsilon_{\parallel}$ for InAs and InSb.

between $m_{\parallel}^{*}(\Gamma)$ and $m_{\perp}^{*}(\Gamma)$ becomes pronounced in InSb, which is because of the induced anisotropy by the strain around the Γ point.

B. Impact Ionization Threshold

Second, E_{th} is calculated by using the calculated conduction and valence band structures. Fig. 3 shows the dependence of E_{th} on $\varepsilon_{\parallel}$ along [100] ([010]), [001] or [111] directions for InAs and InSb. E_{th} in InSb is smaller than that in InAs, which is primarily because of the smaller band gap energy of InSb. The strain makes the band gap energy and also the conduction and the valence band structures change, and then E_{th} varies according to $\varepsilon_{\parallel}$. In both InAs and InSb, we find the smaller E_{th} under the tensile strain ($\varepsilon_{\parallel} > 0$) and the larger E_{th} under the compressive strain ($\varepsilon_{\parallel} < 0$), which results mainly from the change of the band gap energy by the strain. E_{th} shows the large anisotropy under the tensile strain ($\varepsilon_{\parallel} > 0$), which originates from the pronounced anisotropy around the minima of the conduction and the valence bands.

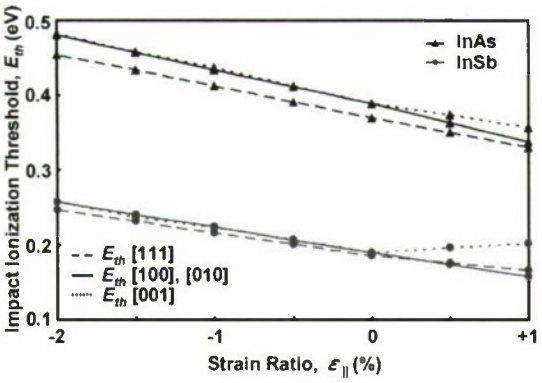

Fig. 3 Dependence of threshold energy for impact ionization, E_{th}, on $\varepsilon_{\parallel}$ along [100] ([010]), [001] or [111] directions for InAs and InSb.

C. Monte Carlo Simulation

Finally, the electron transport in the unstrained and the strained InAs and InSb are calculated. The band parameters that are extracted from the band structures for the MC simulation are summarized in Table I. Fig. 4 shows the average electron velocity, v_d, versus the electric field strength, f, for InAs (a) and InSb (b). v_d and the electric field are parallel to the [100] direction. $\varepsilon_{\parallel}$ is varied as −2, 0 or +1 %. In both InAs and InSb, v_d increases monotonically with f. The tensile strain ($\varepsilon_{\parallel} > 0$) makes v_d larger in a whole range of f, and vice versa. In Fig. 4, v_d that is calculated while ignoring artificially the impact ionization is also shown in order to identify the effect of the impact ionization on the electron transport: which will be discussed later.

Table. I Band parameters extracted from band structures of unstrained and strained InAs and InSb. "||" and "⊥" denote directions parallel and perpendicular to (001) plane, respectively. "l" and "t" denote longitudinal and transverse directions, respectively. α is non-parabolicity parameter.

	Strain Ratio, $\varepsilon_{\parallel}$ (%)					
	InAs			InSb		
	-2	0	1	-2	0	1
$E_{\Gamma L}$ (eV)	0.979	1.066	1.103	0.976	1.040	1.068
$E_{\Gamma X}$ (eV)	1.404	1.590	1.688	1.433	1.573	1.651
$m_{\parallel}^{*}(\Gamma)$	0.039	0.031	0.026	0.023	0.016	0.013
$m_{\perp}^{*}(\Gamma)$	0.039	0.031	0.026	0.028	0.016	0.010
$m_{l}^{*}(L)$	2.823	2.879	2.886	1.943	1.980	1.979
$m_{t1}^{*}(L)$	0.122	0.125	0.127	0.119	0.122	0.124
$m_{t2}^{*}(L)$	0.136	0.125	0.121	0.132	0.122	0.118
$m_{l}^{*}(X)$	0.981	0.973	0.972	2.959	1.883	1.630
$m_{t1}^{*}(X)$	0.277	0.272	0.269	0.278	0.271	0.267
$m_{t2}^{*}(X)$	0.279	0.272	0.267	0.278	0.271	0.267
α_{Γ}	1.773	2.317	2.762	3.219	4.975	7.599
α_{L}	0.344	0.450	0.504	0.461	0.562	0.616
α_{X}	0.135	0.128	0.124	0.157	0.148	0.143
$a_{\parallel}$ (Å)	5.933	6.054	6.115	6.349	6.479	6.544
$a_{\perp}$ (Å)	6.186	6.054	5.988	6.620	6.479	6.408

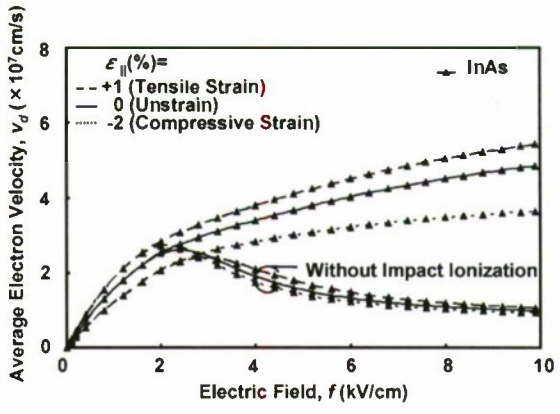

Fig. 4 Average electron velocity, v_d, versus electric field strength, f, for (a) InAs and (b) InSb. v_d and electric field are parallel to [100] direction. $\varepsilon_{\parallel}$ is varied as −2, 0 or +1 %.

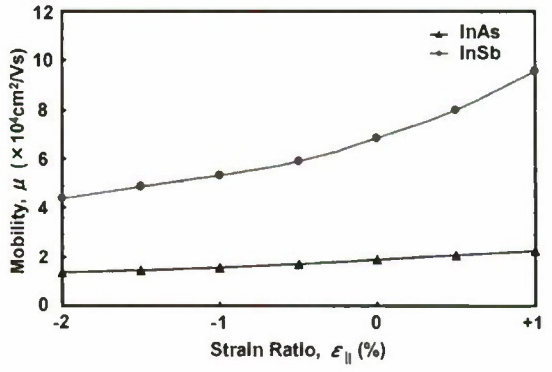

Fig. 5 Dependence of low field electron mobility, μ, on $\varepsilon_{\parallel}$ for InAs and InSb. μ and electric field are parallel to [100] direction.

First we discuss the electron transport at the low f, *i.e.*, f is not sufficiently high to cause the impact ionization. The low field electron mobility, μ, is estimated from the $v_d - f$ curves in Fig. 4. Fig. 5 shows the dependence of μ on $\varepsilon_{\parallel}$ for InAs and InSb. μ is estimated to be 19,000 and 68,000 cm^2/Vs for the unstrained InAs and InSb, respectively. The very small $m_{\parallel}^{*}(\Gamma)$

in InSb is a factor in its extremely high μ. In both InAs and InSb, the tensile strain ($\varepsilon_{\parallel} > 0$) makes μ higher and the compressive strain ($\varepsilon_{\parallel} < 0$) makes μ lower, which are attributed to the dependence of $m_{\parallel}^{*}(\Gamma)$ on $\varepsilon_{\parallel}$ (see in Fig. 2). It is found that the strain effect on μ is more pronounced in InSb.

Next we discuss the electron transport at the high f, in which the impact ionization occurs. We repeat that v_d increases monotonically with f in InAs and InSb. It is surprising that v_d reaches 4.8×10^7 and 7.7×10^7 cm/s at f = 10 kV/cm in the unstrained InAs and InSb, respectively. In the meanwhile, the negative differential resistance appears in the $v_d - f$ curves and then v_d decreases drastically at the high f, if the impact ionization is ignored. This clearly indicates that the impact ionization makes v_d larger at the high f. In the absence of the impact ionization, the electrons more gain energy from the field than lose it to the phonons, and then the electrons easily transfer to the upper-valleys of heavier effective mass, which causes the decrease of v_d. Meanwhile the electron loses most of its energy after the impact ionization, and then the electron again starts to accelerate near the minimum of the Γ valley in the field. Few electrons can avoid suffering the impact ionization before gaining enough energy for the inter-valley transfer. Consequently many electrons are restricted within the bottom of the Γ valley, which results in keeping v_d large even at the high f.

We find that v_d at the high f also depends on $\varepsilon_{\parallel}$ in InAs and InSb. Fig. 6 shows the dependence of the impact ionization coefficient, α, on $1/f$ for InAs and InSb with varying $\varepsilon_{\parallel}$ as −2, 0 or +1 %. α in InSb is larger than that in InAs, which is because of the smaller E_{th} in InSb (see in Fig. 3). It is seen that α becomes larger under the tensile strain ($\varepsilon_{\parallel} > 0$) and smaller under the compressive strain ($\varepsilon_{\parallel} < 0$) in both InAs and InSb, which are in accordance with the dependence of E_{th} on $\varepsilon_{\parallel}$ (see in Fig. 3). Consequently, more electrons are restricted within the bottom of the Γ valley under the tensile strain, and then v_d becomes larger. Meanwhile lesser electrons are restricted within there under the compressive strain, and then v_d becomes smaller.

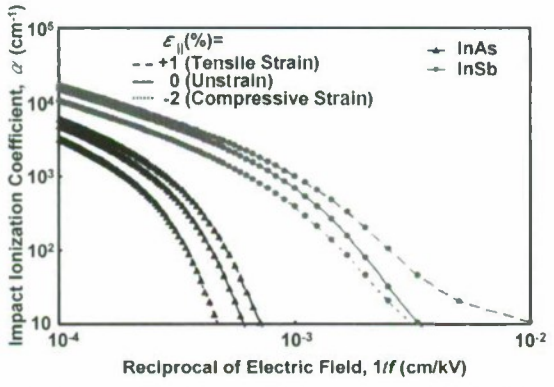

Fig. 6 Impact ionization coefficient, α, versus 1/f for InAs and InSb. $\varepsilon_{\parallel}$ = -2, 0 or +1 %.

IV. Conclusion

We have calculated the unstrained and the strained band structures of InAs and InSb by means of the empirical pseudo-potential method. The impact ionization threshold energy, E_{th}, has been calculated while keeping the energy and momentum conservation. Then the electron transport in the unstrained and the strained InAs and InSb has been investigated by using the Monte Carlo (MC) method. In both InAs and InSb, the average electron velocity, v_d, has increased monotonically with the electric field strength, f. The tensile strain has made the low field electron mobility, μ, higher, and vice versa, which has resulted from the dependence of the effective mass in the Γ valley, $m_{\parallel}^{*}(\Gamma)$, on the strain. At the high f, many electrons have been restricted within the bottom of the Γ valley because of losing most of their energy by the impact ionization, which has resulted in keeping v_d large at the high f. The tensile strain has made E_{th} smaller and then the impact ionization coefficient, α, larger, and vice versa. Consequently, v_d at the high f has become larger under the tensile strain and smaller under the compressive strain.

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INTEGRATION TECHNOLOGIES FOR AN 8X8 INP-BASED MONOLITHIC TUNABLE OPTICAL ROUTER WITH 40GB/S LINE RATE PER PORT

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Abstract

Large-scale photonic integration depends on robust epitaxial design and fabrication techniques. This paper reviews the integration strategy we developed to demonstrate an 8x8 InP-based monolithic tunable optical router capable of 40 Gbps operation per port.

I. Introduction

Large-scale photonic integrated circuits (LS-PICs) in InP are a critical technology to manage the increasing bandwidth demands of next-generation optical networks. By integrating many of the network functions typically handled by discrete optical components into a single device, the overall system footprint can be appreciably reduced. Additionally, a compact, single-chip solution can provide performance and reliability gains along with a reduction in packaging costs. Although the promises of large-scale integration have long been known, LS-PICs have only recently emerged in the marketplace, thanks to advances in InP epitaxial growth and device fabrication that have led to improved yield [1,2].

For most optical network applications, multi-channel LS-PICs that incorporate both active and passive device components on the same chip are desirable. Active/passive integration depends heavily on the epitaxial and fabrication schemes used. To this end, a number of different platform technologies have been proposed and developed in the last two decades [3-5]. Because the choice of an integration platform typically depends on the device requirements, there is not a one-size fits all integration solution. However, in general, an integration strategy should be designed to limit the degree of fabrication complexity and the number of epitaxial regrowth steps to provide high yield and lower cost.

All-optical packet switching at 40 Gbps is one application of interest for LS-PICs. In this approach, routing of data packets is confined solely to the optical domain, potentially easing the increasing power consumption demands of electronic-based routers at high data rates. As part of the U.S. Defense Advanced Research Projects Agency and U.S. Army sponsored DOD-N LASOR project [6], many important single-channel PIC building blocks such as wavelength converters, optical buffers and mode-locked lasers have been demonstrated [7]. Recently, we have further advanced our integration technologies to demonstrate multi-channel PICs with even greater component densities and chip functionality.

This paper will review the integration strategy we used to demonstrate an 8x8 monolithic tunable optical router (MOTOR) chip that serves as the packet-forwarding engine of an all-optical packet-switched router (Fig 1). The 8-channel device consists of an array of 8 tunable wavelength converters (WCs) and an arrayed-waveguide grating router (AWGR). It combines more than 200 building blocks into one chip and has a potential total data capacity of 640 Gbps. Single-channel operation of the device at 10 Gbps [8] and 40 Gbps [9,10] line rates has been achieved with reasonable power penalties. Our integration approach is based on quantum-well intermixing (QWI) and leverages risk by using only a single blanket epitaxial regrowth. To provide additional component functionality, advanced InP fabrication techniques are used to define three separate waveguide architectures that provide differing levels of optical confinement.

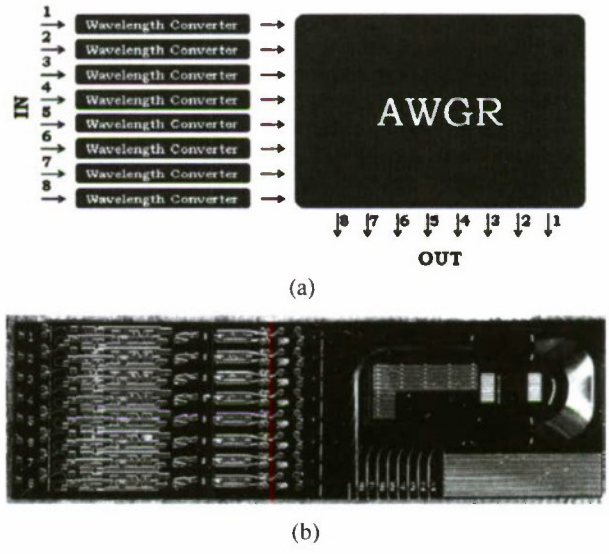

Fig. 1. a) Schematic of MOTOR chip architecture; (b) Photograph of fabricated 8-channel device

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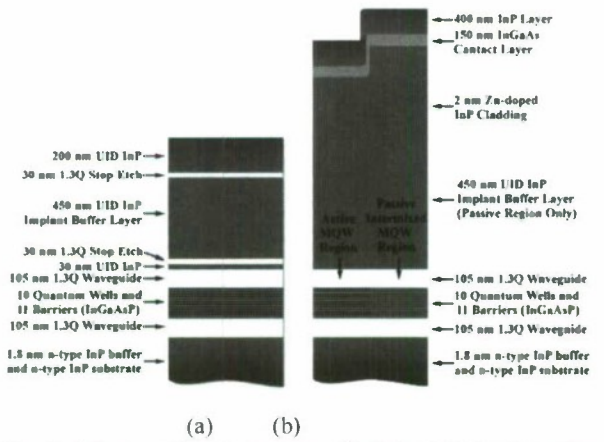
II. Device Design

Our integration strategy for the MOTOR chip was largely based on the design requirements of the WCs and AWGR. Wavelength conversion is accomplished through the use nonlinear semiconductor optical amplifiers (SOA) within a Mach-Zehnder interferometer (MZI) as in [11]. Input data pulses to these SOAs can cause a phase shift in the MZI to modulate an input CW signal, provided that the SOAs are sufficiently saturated. These SOAs necessarily require a high degree of optical confinement. In contrast to these saturated SOAs, the device also needs linear SOAs to amplify the input data signal before the MZI. Therefore, our integration approach must allow for the realization of both linear and nonlinear SOAs. To overcome the inherent limitations of slow carrier recovery time between input data pulses in the MZI SOA, each WC must also employ an integrated delay line to time-delay input pulses to one branch of the MZI relative to the other. Lastly, the WCs require integration of low-loss passive waveguides, splitters and phase tuners.

The AWGR at the output of the WCs should have a small footprint (which constrains the channel spacing), low insertion loss and low propagation loss. The loss is mainly governed by proper design of the input and output star coupler region and the waveguide fabrication. Most notably, the etch process used should provide smooth sidewalls in order to minimize scatter loss and good uniformity across the AWGR section to minimize index variations.

III. Integration Strategy

To achieve the functionality required for the MOTOR chip, we developed a four-point integration strategy. First, an epitaxial base structure in which the multiple quantum well (MQW) active region is sandwiched in the center of the passive waveguide layers is used in order to maximize optical confinement. This ensures that we can obtain the nonlinear MZI SOAs that are essential to wavelength conversion. Linear SOAs can also be realized with this approach, but their length



(a) (b)

Fig. 2. a) Base epitaxial structure; (b) Epitaxial structure after regrowth (the undoped buffer layer found in some passive regions of the device is also shown)

must be kept short to prevent saturation. However, this limits the total possible gain. Second, QWI is employed to blue-shift the active band edge from an as-grown PL wavelength of 1545 nm to a passive band edge of 1420 nm. This allows us to achieve low propagation loss and efficient phase tuners (due to the presence of detuned MQWs in the passive sections). Third, a single blanket p-type InP regrowth is used to clad the waveguide. Blanket regrowths have the advantage of simplicity and higher yield. However, using only one p-doped regrowth step can lead to increased propagation losses in passive regions. The technique we developed to address this issue is discussed in the next section. Finally, our device utilizes three different waveguide architectures so that components with differing optical confinement (and hence optical properties) can be realized. The specifics associated with these waveguide designs are also discussed below.

A. Passive Propagation Loss Reduction with Single Regrowth

It is well known that the interaction of an optical mode with Zn-doped InP can lead to significant loss via free-carrier absorption. In fact, this loss has been shown to be on the order of 20 cm^{-1} for every 1E18 cm^{-3} doping at a wavelength of 1.5 μm [12]. Doping of this level is required in active sections of our device to make efficient diodes. Since we limit our process to only one regrowth step, this means we would have equivalent doping in our passive sections and consequently high loss. This problem could be addressed through an additional undoped regrowth in passive regions, but that is not ideal in terms of cost and yield.

Our base growth (Fig. 2a) contains an undoped InP buffer layer above the MQW region. Historically, this layer has been used exclusively for QWI, after which it is selectively removed via wet etching [3]. However, there is no reason that this layer must be removed after QWI, so we now deliberately leave the buffer layer in certain passive regions of the chip (Fig. 2b) [13]. This effectively "inserts" an unintentionally doped (UID) setback layer between the optical mode and the Zn dopant atoms in the p-type cladding, thus reducing optical scattering losses. The key advantage with this approach is that no additional regrowth is required. Simulations have shown that the net loss with this approach can be decreased by as much as much as ~2.4X, depending on the waveguide structure.

B. Waveguide Designs and Implementation

The MOTOR chip can be divided into three sections with differing ideal optical requirements. To improve the performance of components in these regions, multiple waveguide architectures are defined across the device. First, the bulk of the WC array is defined with a surface ridge waveguide (Fig. 3a,c). This design is used primarily due to its fabrication simplicity and because it provides efficient pumping in gain regions. The waveguide is fabricated by both dry and wet chemical etching. A 400-nm PECVD SiO_2 hard mask is defined above the InP cladding by lithography and then CHF_3-based inductively-coupled plasma (ICP) dry

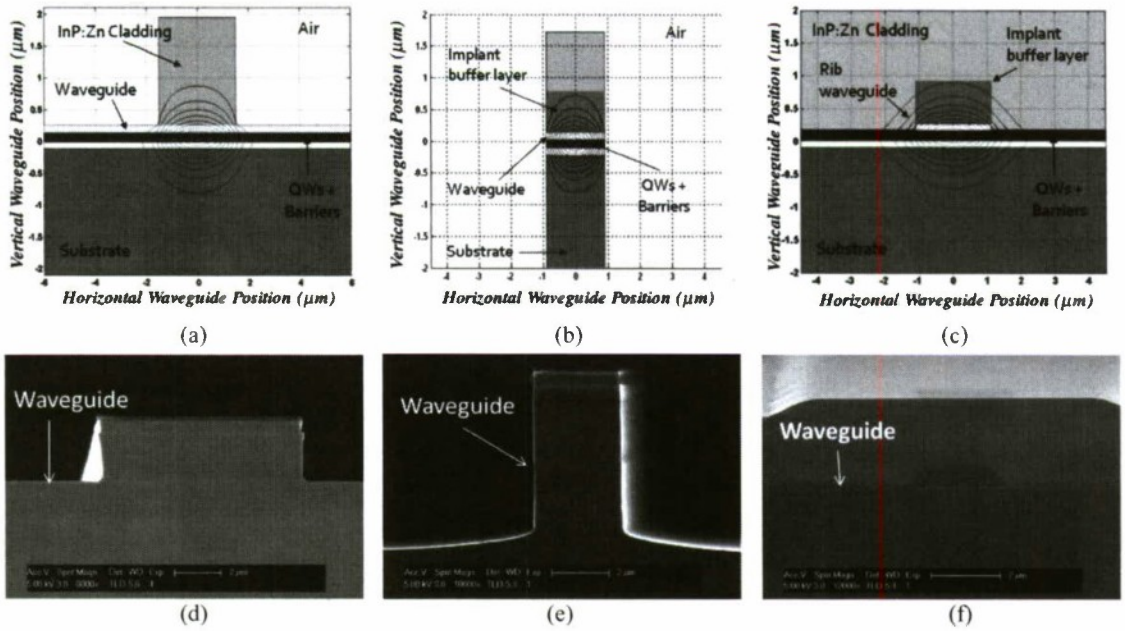


Fig 3. Waveguide architectures used in MOTOR: (a), (b), (c) show schematic cross-sections with the optical mode profile superimposed for surface ridge, deeply-etched ridge, and buried rib, respectively. (d), (e), (f) show SEM cross sections for surface ridge, deeply-etched ridge, and buried rib, respectively

etching. The InP ridge is etched via ICP to a depth of 1.8 μm in a Cl_2:H_2:Ar-based chemistry. By optimizing the gas flows and power levels, straight and smooth sidewalls can be obtained [14]. The remaining 0.6 μm of InP cladding is then removed by selective wet etching in a 3:1 H_3PO_4:HCl mixture. The quaternary waveguide layer above the MQW acts as a stop-etch layer. Because the etch does not go through the MQW region, we avoid surface recombination issues. However, the wet etch is crystallographic and the structure has relatively low lateral confinement, so high-angle structures and tight bends are problematic.

Second, to achieve the differential delay in the MZI that is required for 40 Gbps operation, a compact, 11-ps delay line is needed on chip. In order to minimize the footprint of this component, a deeply-etched waveguide structure is utilized (Fig 3b,e). The delay is fabricated using two dry etch steps. The first 1.8-μm etch is performed simultaneously with the dry-etch step of the surface ridge waveguide. Precise alignment between the surface ridge and deeply-etched regions is maintained because they share the same hard mask. The delay line region is protected with photoresist during the wet etch of the surface ridge. Next, a 350 nm PECVD SiO_2 hard mask is lifted off to open vias in the delay line region. A 2-3 μm dry etch that goes through the waveguide/MQW layers (using identical etch conditions as the first dry etch) is then performed. Since the deeply-etched waveguides are only used in passive sections, surface recombination is not relevant. However, because the optical mode can laterally interact with etched sidewalls, it is extremely important that the sidewalls are not rough.

The AWGR is defined with a 70-nm deep shallow rib waveguide that is etched into the upper waveguide layer (above the MQW) *prior* to the cladding regrowth, which subsequently buries it (Fig. 3c,f). Because a selective wet etch is avoided, this rib waveguide can be turned a full 180° to achieve a compact AWGR footprint. The insertion loss at the star couplers with this architecture is also low in comparison with that of a deeply-etched design.

IV. Results

The spectral response of the AWGR to amplified spontaneous emission (ASE) generated by forward biasing the MZI SOAs was measured in an optical spectrum analyzer. Fig. 4 shows the ASE spectrum from each output port using the SOAs in input port #3. The AWGR is well behaved with a free spectral range of 11.1 nm. Next, the wavelength-based switching capacity of the device was examined by biasing the SG-DBR of input port #3. Fig. 4 shows that with proper biasing of the mirror diodes, the wavelength of the laser can be tuned to the allowed wavelength of any output port. Output powers of more than -5 dBm were measured. This power level is reasonable given the long propagation length in the AWGR region and fiber coupling losses (~4-5 dB).

40 Gbps wavelength conversion and channel switching were then investigated by sending a modulated input data source into the chip and measuring the bit-error rate (BER) of the converted and routed data [10]. Fig. 5 shows that power penalties as low as 4.5 dB were achieved at a BER of $< 10^{-9}$ for multiple input/output port combinations.

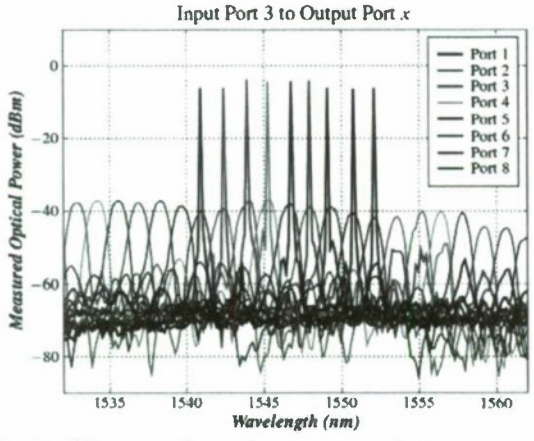


Fig. 4. ASE spectra from all output ports. Lasing spectra from the SG-DBR of input channel #3 (tuned with various mirror bias levels) from each output are superimposed to demonstrate the wavelength switching capacity of the device

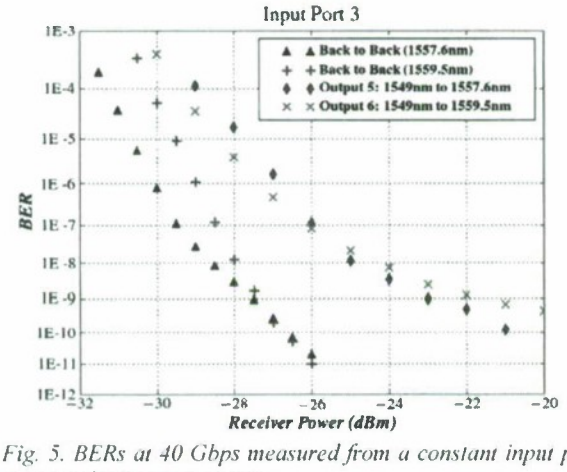


Fig. 5. BERs at 40 Gbps measured from a constant input port using multiple output ports

V. Conclusion

Using an integration strategy that emphasized simplicity for the sake of yield, we have demonstrated one of the most complex LS-PICs to date. Our strategy combines epitaxial techniques such as QWI and simple blanket regrowths with aggressive waveguide fabrication techniques. Notably, our device employed only one p-type InP regrowth step. Because the doping profile of the cladding region was designed for active components, steps were devised to reduce optical loss in passive regions. We now leave an InP implant buffer layer (used previously only for QWI) above the waveguide in passive regions to separate the optical mode from the p-type dopant in the cladding without additional regrowth steps. We have also demonstrated multiple waveguide architectures on a single-chip in order to optimize components with different optical properties. The execution of this integration strategy has led to a successful demonstration of single-channel wavelength conversion and routing of data at 40 Gbps.

Acknowledgements

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A Monolithic Wavelength-Routing Switch using Double-Ring-Resonator-Coupled Tunable Lasers with Highly Reflective Mirrors

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Abstract

We report a monolithically integrated 8x8 wavelength-routing switch with semiconductor-optical-amplifier-based wavelength converters and double-ring-resonator-coupled tunable lasers incorporated with highly reflective cavity mirrors. The dry-etched mirror coated with Au enables flexibility in device layout. It allows highly reflective mirrors in a chip and antireflective coating on both the input and output facets of the wavelength converters. A 1x8 high-speed wavelength routing operation of a non-return-to-zero signal at 10 Gbit/s is demonstrated.

I. Introduction

With the steady growth of the optical communications networks due to the Internet and Internet-related services, there is a need for large-capacity and low-power-consumption nodes with flexible traffic-engineering capability for high-level services. A potential solution is optical packet switching (OPS) which maximizes the flexibility and throughput of the network because of its packet-level data granularity [1,2]. However, OPS requires optical routers that surpass current electrical routers in throughput, power consumption, latency, and size. An NxN optical switch operating on a packet-by-packet basis is a key device for realizing optical routers since it can maintain data in the optical packet format [3].

Although a variety of optical switch technologies have been proposed for use in OPS, wavelength-routing switches (WRSs) based on tunable wavelength converters (TWCs) and an arrayed-waveguide grating (AWG) are the most promising ones due to their potential low power consumption and high scalability for larger throughput. We have developed a monolithic 4x4 WRS with double-ring-resonator-coupled tunable lasers (DRR TLs) [4] and semiconductor-optical-amplifier (SOA)-based wavelength converters (WCs) [5], and a high-speed wavelength routing operation of a non-return-to-zero (NRZ) signal at 2.5 Gbit/s has been demonstrated [6].

In order to further enhance the applicability to the optical routers, we need to increase the port count and signal line rate for higher throughput of the WRS, and to achieve higher output power. In the previous WRS, the same cleaved facet served as both the back mirror of the DRR TL, which requires high reflectivity, and the input facet of the SOA-based WC, which must have low reflectivity. The non-optimized facet reflectivity (R = ~30%) was insufficient for high output power of the DRR TL, which therefore led to unstable operation of the SOAs at high current density. In this work, we developed a monolithically integrated 8x8 WRS with dry-etched mirrors

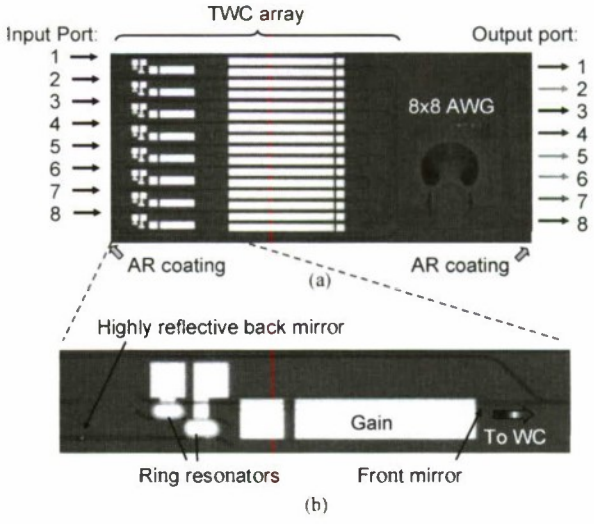

Fig. 1. (a) Photograph of the fabricated WRS. (b) Enlarged view of the DRR TL.

coated with Au. Each mirror is separated from the cleaved facet and serves as a high-reflection cavity mirror of the DRR TL. Therefore, an antireflection film can be coated on both the input and output facets of the WC to improve the performance of the WC. We also demonstrate a 1x8 high-speed wavelength routing operation of a NRZ signal at 10 Gbit/s.

II. Device structure and fabrication

Figure 1(a) shows a photograph of the fabricated WRS, consisting of an array of eight TWCs and an 8x8 AWG. The device size is 2.1 mm x 4.8 mm, which is less than one-sixth of the size of an 8x8 monolithic optical switch previously reported [7]. Connections between the eight input and eight output ports are accomplished by changing the TWC output wavelength.

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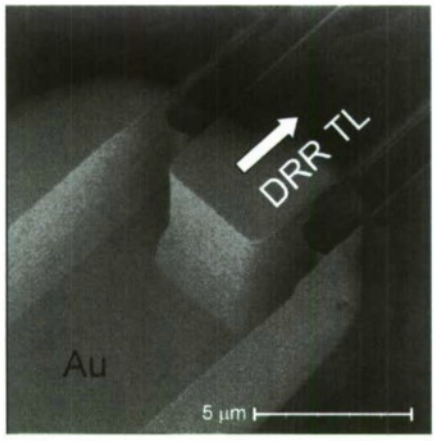

Fig. 2. SEM image of the highly reflective back mirror coated with Au.

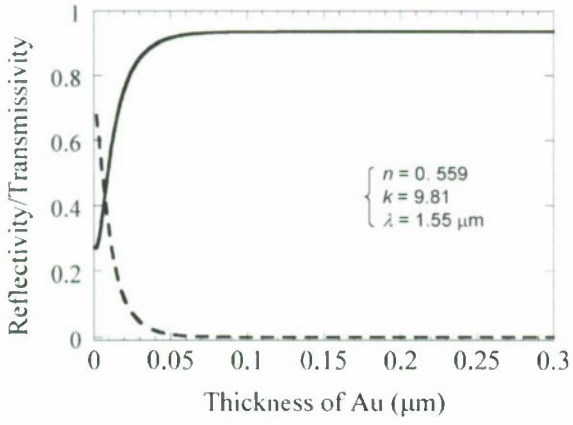

Fig. 3. Calculated reflectivity (solid line) and transmissivity (dashed line) of the mirror at a wavelength of 1.55 μm.

The TWC consists of the DRR TL and the WC with a parallel amplifier structure (PAS) [8]. The DRR TL features low-tuning-current operation, which allows rapid and stable tuning [4]. Compared with the sampled-grating distributed Bragg reflector (SG DBR) often employed in tunable lasers, the ring-resonator filters employed within the cavity of the DRR TL offer superior filter characteristics as well as a compact structure. These characteristics include a narrower transmission bandwidth with a Lorentzian-type filter response and an infinite number of resonant peaks. When the Vernier tuning mechanism is used, the maximum injection current required for tuning can be reduced by reducing the free-spectral ranges (FSRs) of the filters. The ring-resonator filter enables reduction of the FSR while it expands the tuning range, resulting in low tuning current operation. The low tuning current operation is critical for reducing wavelength drift due to thermal transients [4]. The small wavelength drift is highly advantageous for high-speed and stable switching operation of the WRS, as the wavelength drift exhibits a much longer response time (millisecond order) than the mechanism employed for fast tuning and will cause loss and crosstalk in the WRS.

The FSRs of the ring resonators were set to 400 and 444 GHz, respectively, and the total FSR of the two ring resonators is 4 THz as a result. Wavelength conversion is performed by modulating the CW light from the DRR TL with cross-gain modulation (XGM) caused by the input signal injected into the WC. The WC with the PAS is a symmetric Mach-Zehnder interferometer (MZI), which consists of two 3-dB multimode interference (MMI) couplers and an SOA in each arm. Since the MZI is set in the cross state by injecting the same amount of current into both SOAs, the input signal after the XGM and the converted signal are fed to different output ports of the MZI automatically. Therefore, the input optical signal is removed before the AWG with the PAS (filter-free operation) [8].

For the device, a stack-layer structure was used, which enables fabrication with only a single regrowth step. In this structure, a compressively strained multi quantum well (MQW) layer for the active section is grown on top of a 0.3 μm-thick InGaAsP layer (λ_g = 1.4 μm). The active layer and 1.4Q passive layer are separated by a 10-nm-thick InP etch stop layer to allow the removal of the active layer in the passive section by selective wet etching. A 1.5 μm-thick p-InP cladding layer and a p-InGaAsP contact layer were grown over the entire surface after the wet etching process. The gain sections of the DRR TL and the SOA sections have a shallow-ridge waveguide structure, whereas the ring resonators and the AWG have a deep-ridge waveguide structure. The deep-ridge waveguide has a very large refractive index difference in the lateral direction, which minimizes the allowable bending radius and makes the device compact. The deep-ridge waveguide structure was formed by Cl_2-based inductively coupled plasma reactive ion etching (ICP-RIE) with only a lithography step. This simplifies the fabrication process of the WRS. The lengths of the gain and SOA sections are 400 and 1200 μm, respectively.

The laser cavity of the DRR TL is defined by an etched-gap front mirror [5] and a newly developed highly reflective back mirror. Figure 2 shows a scanning electron micrograph (SEM) image of the fabricated back mirror coated with Au. The back mirror was integrated with the DRR TL, in which a dry-etched facet was coated with Au. The mirror provides high reflectivity with a simple fabrication process and allows antireflective coating on both the input and output facets of the WCs. Figure 3 show the calculated reflectivity and transmissivity of the mirror at a wavelength of 1.55 μm. In this calculation, the values of the refractive index n and extinction coefficient k were assumed to be 0.559 and 9.81, respectively [9]. The maximum reflectivity of the mirror is expected to exceed 93 % for around 100-nm-thick Au. The dry-etched structure was fabricated in the same ICP-RIE step

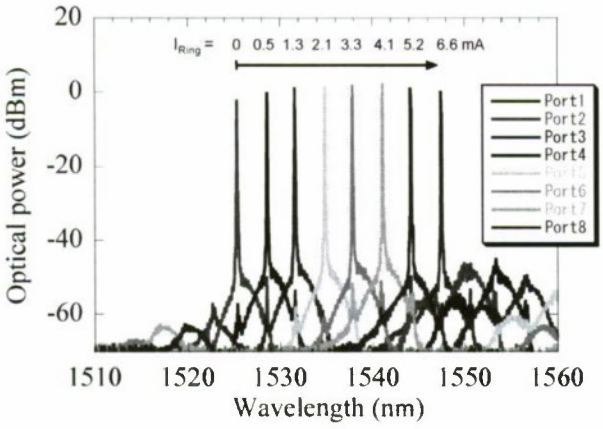

Fig. 4. Superimposed output spectra of the WRS for every output port when using the fifth TWC.

with the deep-ridge waveguide structure. Then, Au was deposited to a thickness of 300 nm by using a liftoff process in which electron-beam evaporation was employed with angled rotation to improve sidewall coverage over the structure.

III. Experiments

The first results are related to the static routing characteristics of the fabricated WRS. Figure 4 shows superimposed spectra of the WRS for every output port when using the fifth DRR TL. The injection current for the ring resonator with an FSR of 444 GHz was changed from 0 to 6.6 mA, whereas the currents for the gain and both SOAs sections were kept constant at 100 and 200 mA, respectively. By changing the injection current for only a single ring resonator, output ports can be easily selected [6]. The output power is increased from the -15 dBm of the WRS in [6] to a few dBm.

Figure 5 shows the wavelength-converted eye diagrams for every output port of the WRS. In this experiment, only a single input port was tested. The 10-Gbit/s NRZ input optical signal had a wavelength of 1545 nm with a pseudo-random bit sequence (PRBS) of length 2^{31}-1. The signal was fed into input port 5 with an average power of 10 dBm. The wavelength of the converted signal was tuned so that the converted signal was output at one of eight output ports. The currents for the gain section, both SOAs, and the other ring resonator of the TWC were kept constant at 100, 250, and 0 mA, respectively. A clear eye opening was observed for every output port, confirming the 1x8 wavelength routing operation of the NRZ signal at 10 Gbit/s.

The third results are related to the high-speed wavelength routing operation of the WRS. Figure 6 shows signal waveforms from every output port of the WRS when the input signal was fed into input port 5. The 10-Gbps NRZ input signal had a wavelength of 1545 nm with a power of 13 dBm. Dynamic switching between the eight output ports was performed by changing the injection current for only a single

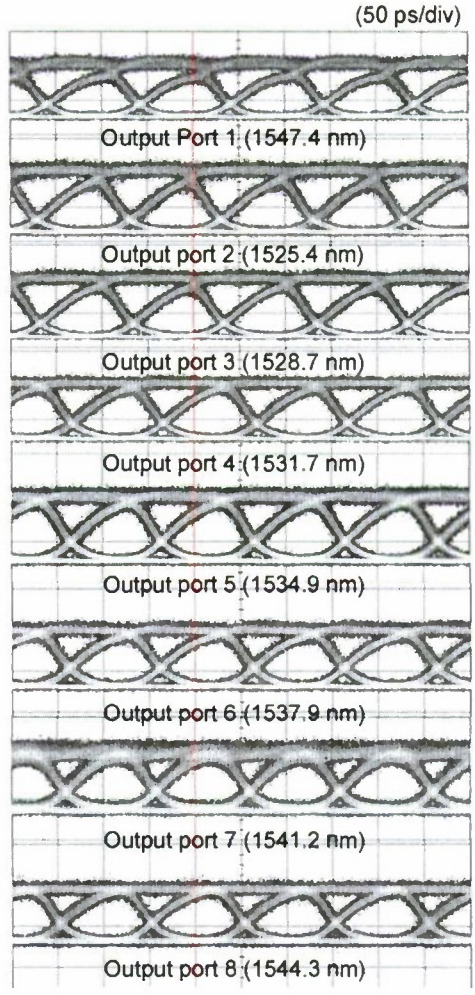

Fig. 5. Wavelength converted eye diagrams for every output port of the WRS.

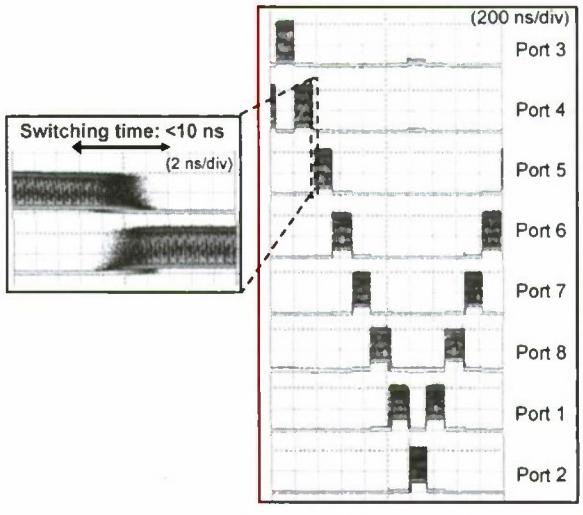

Fig. 6. Waveforms for the eight output ports of the WRS.

ring resonator with a period of 160 ns. High-speed and stable wavelength routing with a switching time of less than 10 ns was achieved. The capability of stable switching between multiple ports is attributed to the improved characteristics of the WC based on the dry-etched mirrors.

IV. Conclusion

We have fabricated an ultra-compact WRS using DRR TLs with dry-etched mirrors coated with Au. The highly reflective mirror enables us to coat both the input facet and the output facet with an antireflection film and thereby improve the performance of the WRS. We demonstrated 1x8 high-speed wavelength routing operation of an NRZ signal at 10 Gbit/s. These characteristics make the device very promising for use in OPS.

Acknowledgments

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MONOLITHICALLY-INTEGRATED 8:1 SOA GATE SWITCH WITH SMALL GAIN DEVIATION AND LARGE INPUT POWER DYNAMIC RANGE FOR WDM SIGNALS

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Abstract

We developed a highly uniform monolithically integrated 8-input and 1-output (8:1) SOA gate switch for a large-scale high-speed switching system. The gain fluctuation due to an internal interference was suppressed with a low loss 8:1 tapered MMI coupler. The device exhibited a very small gain deviation of <2.0 dB for all wavelengths in the C-band, together with a high extinction ratio of >50 dB and an ON-state gain of >10 dB. We also demonstrated a penalty-free amplification of 8×10 Gb/s WDM signals with a large input power dynamic range of >9.8 dB

I. INTRODUCTION

A high-speed optical switching system is a key technology to realize a highly efficient and flexible photonic network using an optical packet or burst signal. A semiconductor optical amplifier (SOA) gate is a very promising candidate for the switching engine in these systems, because of its fast gain dynamics of nanoseconds. Recently, large-scale, high-speed switching systems have been proposed using a large number of SOA gates in multi-stage configuration [1-2]. Monolithic integration of multiple SOA gates and passive components is an attractive approach for reducing the size and power consumption of these switching systems. However, in large-scale switching systems that use monolithically integrated SOA gate switches, the inter-port gain deviation and polarization dependent gain (PDG) of each integrated device randomly accumulate at each path. Thus, in the worst case, the total deviation at received power levels becomes large. This large deviation in received power is a critical issue when we consider a small input power dynamic range of a high-speed packet or burst mode receiver. To overcome this difficulty, we must keep the gain deviation and PDG of the monolithically integrated devices at a very low level. In addition, when the switching systems handle a broadband wavelength-division multiplexing (WDM) optical packet or burst signal, the device must realize a small gain deviation and PDG for all the wavelengths where the WDM signal are arranged.

To date, monolithic SOA gate switches have been reported on a scale of 8:1[3,4] and 16:16[5]. These devices demonstrated a fast switching time and a penalty-free operation for high bit-rate signals. However, a monolithically integrated SOA gate switch which has a sufficiently small gain deviation over a wide wavelength range is yet to be investigated. In this paper, we report on a monolithically integrated 8:1 SOA gate switch which has a very small gain deviation and PDG over the entire wavelength of the C-band. This device also exhibited a large input power dynamic range (IPDR) of >9.8 dB for an 8 × 10 Gb/s WDM signal owing to both a high saturation output power and a low noise figure (NF) in SOA gates.

II. DEVICE STRUCTURE

In order to reduce the gain deviation of monolithically integrated SOA gate switches, a very high uniformity is required for SOA gates, passive waveguide, and couplers. In addition, excess losses at passive waveguides and couplers must be carefully reduced to suppress any stray light that propagates through the chip. This stray light may cause an unfavorable interference between the signal light, resulting in an unexpected wavelength dependence of the device. In this study, therefore, we adopted an 8:1 tapered multi-mode interference (MMI) coupler in place of the former 8:1 field flattened coupler (FFC) [6]. Because a tapered MMI coupler utilizes self-imaging based on mode interference, the excess loss of a tapered MMI coupler can be smaller than an FFC by a factor of about 0.63 [7]. Moreover, the tapered MMI coupler can be made smaller than a conventional MMI, and thus we can maintain a compact coupler size of 275 μm, which is almost the same as that of the FFC.

A schematic structure of our 8:1 SOA gate switch is illustrated in Fig. 1. The device comprises an 8ch SOA gate array, an 8:1 tapered MMI coupler, passive waveguides, and a 1ch SOA gate. These components are integrated on an n-InP substrate using butt-joint re-growth technology. Each SOA gate of 800-μm length has a strained MQW active layer which can realize a small PDG and high saturation output power over a wide wavelength range [3]. The port spacing of the 8ch SOA gate array was set to 60 μm to reduce the size of the 8-ch fan-out waveguides. Although the spacing of the 8-ch SOA gate was narrow, we can efficiently couple the signal lights from a fiber array by using a

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collective lens coupling scheme [8]. All of the waveguides in the SOA gates and passive section were buried with an Fe-doped semi-insulating InP layer which has a small electrostatic capacitance and a high current blocking efficiency. The total device size was 3.0 × 1.0 mm.

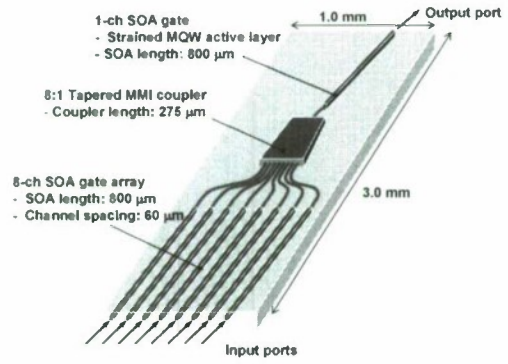

Figure 1. Schematic structure of 8:1 SOA gate

III. Device Characteristics For CW Signal

The characteristics of the 8:1 SOA gate switch were measured over the C-band wavelength. The signal light was individually coupled to the ports using fiber-pigtailed lens modules. A selected port from an 8-ch SOA gate and a 1-ch SOA gate were simultaneously biased to the ON-state (300 mA). Figure 2 (a) shows 8-ch superimposed gain spectrums of the newly developed 8:1 SOA gate switch with a tapered MMI coupler. The device exhibited smooth and uniform gain spectrums. In the C-band wavelength (1525–1565 nm), a large ON-state gain of >10.0 dB and a small PDG of <1.0 dB were obtained. On the other hand, Fig. 2 (b) shows 8-ch superimposed gain spectrums of the previous 8:1 SOA gate with a FFC coupler. Each gain spectrum has a non-periodic fluctuation with an amplitude of about 2 dB, and the fluctuations of each port show almost no correlation with each other. These fluctuations in gain spectrums are attributed to the internal interference between the signal light and stray light. By comparing the gain spectrums of these devices, we confirmed that adopting a tapered MMI coupler clearly suppressed the fluctuations in gain spectrum. We think this is because the lower excess loss in the tapered MMI coupler reduced the intensity of stray light. Figure 3 shows the wavelength dependences of total 8-ch gain deviation including the PDG for each device. In our previous device, the total gain deviation had been deteriorated by a fluctuation in gain spectrum which can been seen in Fig. 2(b), and it varied in the range of 3 to 5 dB with a large wavelength dependence. However, in our new device, the amplitude of the gain fluctuation was improved and the device exhibited a much smaller total gain deviation of <2.0 dB for all wavelengths in the C-band. In addition, the total NF of the 8:1 device was 7.6 to 10.4 dB in the C-band, which was also better than the former device due to a small excess loss at a coupler. The chip-out 3-dB saturation output power of each SOA gate was > +16.8 dBm at 1550 nm. Figure 4 (a) shows the 8-ch superimposed switching characteristics measured at 1550 nm. The currents for a 1-ch SOA and an 8-ch SOA gate were synchronously swept between 0 and 300 mA.

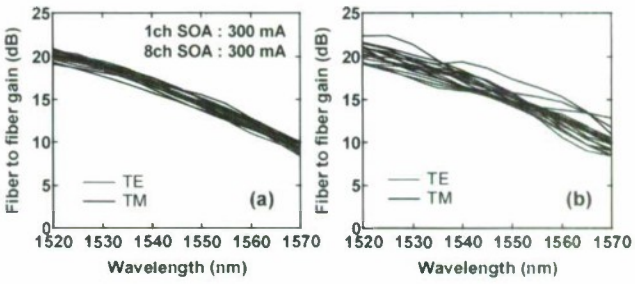

Figure 2. 8-ch superimposed gain spectrum of 8:1 SOA gate with (a) tapered MMI coupler (b) FFC coupler

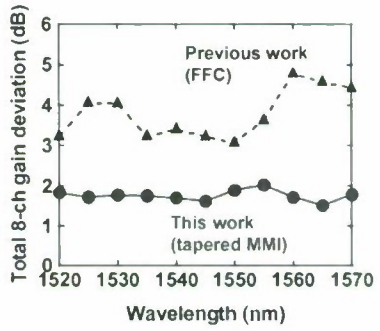

Figure 3. Wavelength dependences of total 8-ch gain deviation

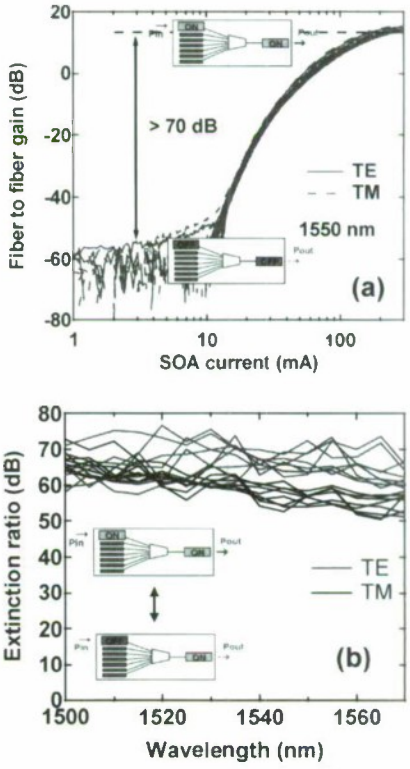

Figure 4. (a) Switching characteristics in synchronous sweep of SOA gates (b) Superimposed spectrum of "strict" extinction ratio (1ch SOA ON)

The device exhibited uniform switching characteristics, and a high extinction ratio of >70 dB was obtained between OFF(8ch)-OFF(1ch) and ON(8ch)-ON(1ch) states. In practical operation in a large-scale switching system, there are two types of extinction ratio for the 8:1 SOA gate. One is the extinction ratio between the OFF-OFF and ON-ON states shown in Fig. 4(a), and the other is the "strict" extinction ratio between OFF(8ch)-ON(1ch) and ON(8ch)-ON(1ch) states. The latter corresponds to the case in which one of the other ports is selected from the same 8-ch SOA gate. Both types of extinction ratio are important for keeping a low inter-port crosstalk in a large-scale switching system. Figure 4(b) shows the 8-ch superimposed spectrum of the "strict" extinction ratio. Owing to a low loss and low leakage at the passive section, the device exhibited a high extinction ratio of >50 dB for the entire wavelength range. These extinction ratios of the 8:1 SOA gate are large enough for application to a 256-port-scale switching system.

IV. Amplification Characteristics of 8 × 10 Gb/s WDM Signal

To investigate the performance of the 8:1 SOA gate switch for a WDM signal, we measured the bit error rate (BER) characteristics using an 8 × 10 Gb/s WDM signal. The experimental setup is shown in Fig. 5 (a). We used a wavelength-tunable 10 Gb/s NRZ-OOK transponder for the tested wavelength channel. The other seven wavelength channels were collectively modulated by a $LiNbO_3$ modulator, and they were multiplexed to the tested wavelength. To avoid any inter-channel crosstalk due to four-wave mixing (FWM) in the SOA gates, we used a wide channel spacing of 400 GHz ranging from 1531.1 to 1553.5 nm. All wavelength channels were modulated in PRBS of 2^{31}-1, and they were de-correlated using a dispersion shifted fiber of -170 ps/nm. The power level of each wavelength channel was equalized, and the target input power level to the 8:1 SOA gate switch was controlled with an EDFA and an attenuator (ATT). The input and output spectrums of the 8:1 SOA gate switch are shown in Fig. 5 (b). The device successfully amplified the WDM signal without a peak of the converted signal due to FWM. The tested wavelength channel of the amplified signal was sliced with a band-pass filter (BPF) of 0.9-nm FWHM. Then, the de-multiplexed signal was received with a transponder after a dispersion-compensation fiber (DCF). Figure 6(a) shows the BER characteristics measured for all wavelength channels. We measured a received power dependence of BER at port 1. The power penalty at each channel was defined as the shift in the sensitivity for the BER of 10^{-12}. The input power was set to -18 dBm/ch. We obtained a clear output waveform from the 8:1 SOA gate switch, and the device exhibited a small power penalty of <0.4 dB for all 8 wavelength channels. We also measured the input port dependence of power penalty at 194.6 THz (Fig. 6(b)). The results indicated highly uniform and small power penalties of <0.4 dB for all 8 ports. These results successfully proved that the device achieved penalty-free amplification of a 8×10 Gb/s WDM signal.

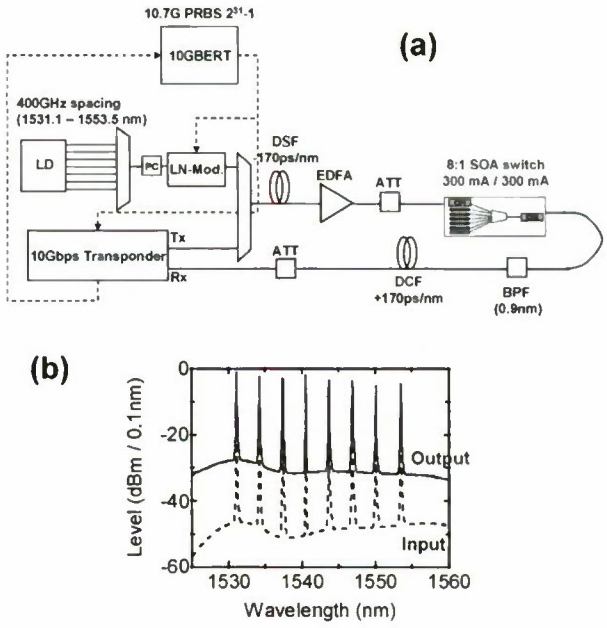

Figure 5. (a) Experimental setup for 8×10 Gb/s WDM test
(b) Input and output spectrums of 8:1 SOA gate switch

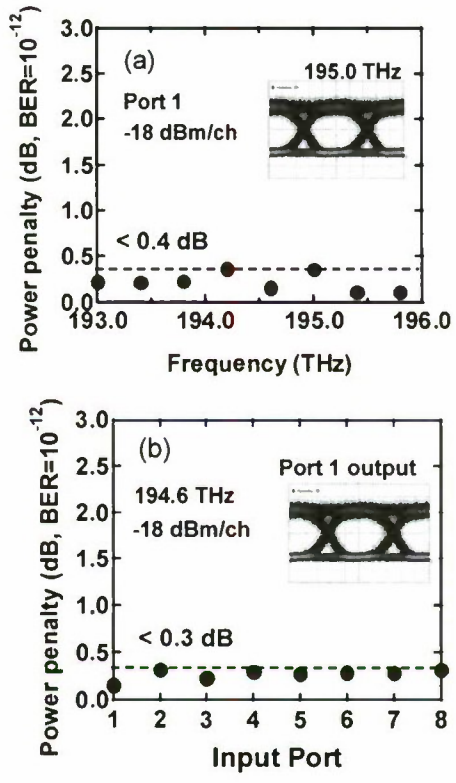

Figure 6. BER characteristics for 8 × 10 Gb/s WDM signal
(a) Wavelength channel dependence at port 1
(a) Port dependence at 194.6 THz

In a large-scale switching system, a large IPDR is required for the 8:1 SOA gate switch, because it provides sufficient power margin and scalability to the system. We, therefore, investigated the IPDRs of the 8:1 SOA gate switch for both a single channel 10 Gb/s NRZ signal and an 8 × 10 Gb/s WDM signal. Figure 7(a) shows the input power dependences of power penalty measured with single channel 10 Gb/s signals at four wavelengths over the C-band. In the higher input power regime, the shorter wavelength first exhibits a rise of power penalty because the device has a higher gain and a lower saturation output power at shorter wavelengths. In terms of the output power, the device performed a linear amplification up to a fiber-out power of +10.0 dBm. This maximum linear output power is equivalent to our discrete 1-ch SOA gate with the same structure. Meanwhile, in the lower input power regime, we obtained nearly the same curves for four wavelengths because of the small wavelength dependence in NF. When we tolerate a maximum power penalty of 1.0 dB, the device exhibited a large IPDR of 19.3 dB for all wavelengths. The IPDR tends to be larger at longer wavelengths due to a smaller gain. We also plotted the input power dependences of power penalty measured with an 8 × 10 Gb/s WDM signal in Fig. 7(b). In the lower input power regime, the device exhibited almost the same curves as that of single-channel amplification. The lower input power threshold of the 8:1 SOA gate switch is determined by the relationship between input power per channel and the NF. In the higher input power regime, however, the device exhibited lower threshold power levels as compared with that of single channel amplification. Because the power penalties in the higher input power regime are caused by the waveform distortion due to the gain saturation, the input power threshold is determined by the total output power of the device. In our investigation, by increasing the number of wavelength channels, the threshold power levels at the higher input power regime decreased by 9 to 9.5 dB. These decreases are almost consistent with the increase in total output power by wavelength multiplexing. Therefore, the result indicates that the 8:1 SOA gate switch is not much influenced by inter-wavelength channel crosstalk caused by FWM or cross-gain modulation. As a result, the device exhibited a large IPDR of > 9.8 dB for the entire wavelength channels of the 8 × 10 Gb/s WDM signal. Although the IPDR of our SOA gate switch is decreased by its high gain, the device demonstrated a large IPDR owing to the coexistence of a high saturation output power and a low NF.

V. Conclusion

A monolithically integrated 8:1 SOA gate switch was developed with a tapered MMI coupler. The low excess loss of the tapered MMI coupler improved a gain fluctuation and realized a very small total gain deviation of <2.0 dB over the C-band wavelength. The device also exhibited both a large gain of < 10.0 dB and a high extinction ratio of > 50 dB. We also successfully demonstrated a penalty-free amplification of a 8 × 10 Gb/s WDM signal with a large IPDR of > 9.8 dB. This device is suitable for use in a large-scale WDM switching system.

Acknowledgement

This work was partly supported by NICT of Japan.

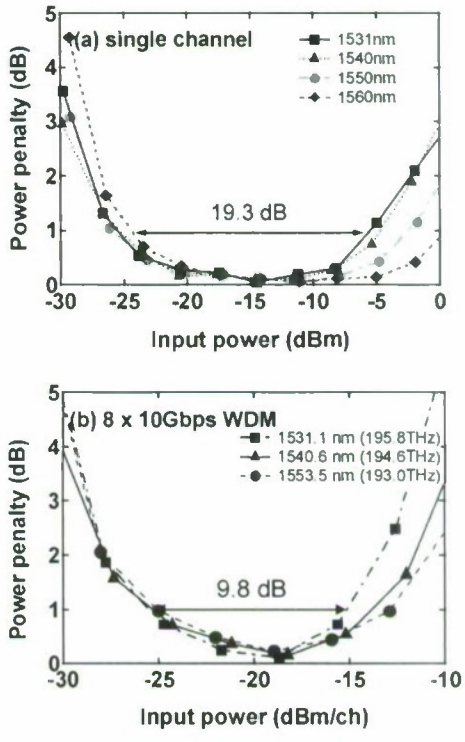

Figure 7. Input power dependences of the power penalty (a) single channel 10 Gb/s signal (b) 8 × 10 Gb/s WDM signal

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INTERSUBBAND ABSORPTION GENERATION THROUGH SILICON ION IMPLANTATION IN UNDOPED INGAAS/ALASSB COUPLED DOUBLE QUANTUM WELLS TOWARDS MONOLITHIC INTEGRATION OF INTERSUBBAND-TRANSITION-BASED ALL-OPTICAL SWITCHES

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Abstract

We demonstrated the intersubband absorption through silicon ion implantation and subsequent rapid thermal annealing in undoped InGaAs/AlAsSb coupled double quantum wells. The effective temperature region of carrier activation for the implanted silicon ions is about 470~600 °C. For the sample with a silicon implantation dose of 1e14 cm^{-2}, we obtained an actual carrier density of ~ 7.5e13 cm^{-2} (~75% activation efficiency) when it was annealed at 600 °C for 1 min. Simultaneously, a ~160-nm blueshift in interband absorption edge was observed, indicating quantum well intermixing (QWI). QWI and its non-uniformity were confirmed using SIMS and TEM measurements. This technique to generate intersubband absorption opens a route to fabricate monolithically integrated all-optical switches based on intersubband-transition induced cross-phase modulation.

I. Introduction

InGaAs/AlAsSb coupled double quantum wells (CDQWs) have been successfully used in ultrafast Mach-Zehnder interferometers (MZI) for >100Gbps all-optical switching based on the cross-phase modulation (XPM) effect which originates from the intersubband transition (ISBT) induced interband dispersion (1,2). Currently, we attempt to fabricate a compact monolithically integrated MZI based on this ISBT-XPM instead of free-space MZI packaged by bulk optics components (1) for performance enhancement. A big challenge is to selectively realize ISBT and non-ISBT waveguides on a planar chip, respectively for phase modulation and propagating. As seen in Fig. 1(a), we plan to perform ion implantation in a selective region in the undoped CDQW wafer. Then the nonlinear ISBT waveguide is expected to be achieved in the ion implantation region; while, other undoped waveguides work as the non-ISBT waveguides since they are absent from ISBT. The ISBT waveguide will absorb TM polarized control light to generate the phase shift for TE polarized signal light and other non-ISBT waveguides are transparent to both TE and TM light.

Conventionally, ion implantation and rapid thermal annealing (RTA) are post-growth techniques for achieving quantum well intermixing (QWI) in order to realize quantum well based multi-wavelength function integration (3,4) where for most cases the ion implantation aimed at realizing the bandgap adjustment. However, it is rarely reported to generate intersubband absorption through ion implantation in QWs, whereas this is important to extend such a conventional method to fabricate the integrated ISBT-XPM based photonic devices. In this study, intersubband absorption was successfully generated through silicon (Si) ion implantation and RTA in InGaAs/AlAsSb CDQWs. The coexistent QWI was experimentally clarified which greatly influences the intersubband and interband absorption spectra. This study is beneficial not only to the integration techniques, but also to understand the quantum well intermixing effects on ISBT energy shifts in CDQW systems.

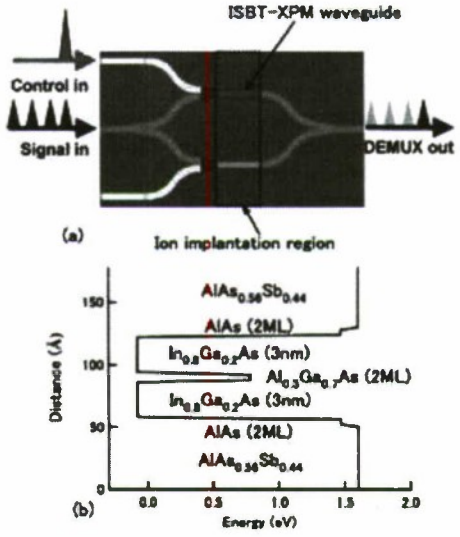

Figure 1. (a) A proposed scheme of the integrated ISBT-XPM MZI for all-optical demultiplexing. The dotted-line square is the ion implantation region to generate ISBT. ISBT: intersubband transition. XPM: cross phase modulation. DEMUX: demultiplexing. (b) CDQW parameters.

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II. Experiment

The undoped epilayer sample for Si+ ion implantation was grown on an InP substrate by molecular beam epitaxy and had a 10-nm $In_{0.52}Al_{0.48}As$ capping layer. The growth details can be found in Ref. (5). The designed CDQW structure is shown in Fig. 1(b). The AlAsSb barrier was in a latticed matched condition, while the $In_{0.8}Ga_{0.2}As$ well was compressively strained. For balancing such strain, two AlAs interfaces were introduced. The epilayer contains 60 stacks of CDQWs to guarantee measurable absorption magnitude. 250-keV Si+ ions were implanted from the surface with a 7° tilt angle to avoid channel effects. Hall measurement was carried out to check the real carrier density and Fourier transform infrared (FTIR) spectrum was performed to examine both intersubband and interband absorption which adopt a 45° edge-polished multipass scheme (6) and a normal incidence scheme with backside polished, respectively. ISBT is only allowed for *p* polarization, while the background of *p* polarized spectra have been corrected using *s* one due to the interference. Secondary ion mass spectrometry (SIMS) and transmission electron microscope (TEM) were used to characterize Si ion distribution and observe QWI, respectively. Implantation and all measurements were done at room temperature.

III. Intersubband absorption generation

The CDQW in Fig.1(b) has four confined subbands (e_i, i=1-4) in conduction band (2). The operation wavelength 1.55μm locates in the e_1-e_4 absorption region (1), while the ISBT e_1-e_4 is difficult to be measured by FTIR because of its weak dipole moment. Therefore, we study the ISBT e_1-e_2 which has much higher dipole moment than e_1-e_4. In Fig. 2(a), there are always no absorption peaks for as-grown sample, even at an enhanced annealing temperature. This means that simply annealing as-grown sample cannot generate electrons to occupy subband e_1. In contrast, a clear e_1-e_2 absorption was observed at 500°C for the implanted sample [see Fig. 2(b)] and it greatly enhances when annealed at 550°C. Evidently, implanted Si was successfully activated to generate intersubband absorption after RTA.

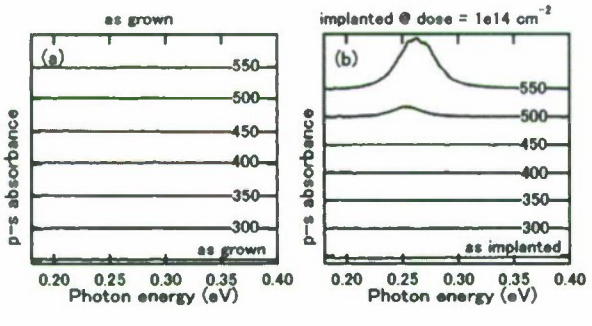

Figure 2. Intersubband absorption e_1-e_2 for (a) as-grown and (b) implanted samples annealed at each annealing temperature (°C) for 1 min. Curves are vertically offset.

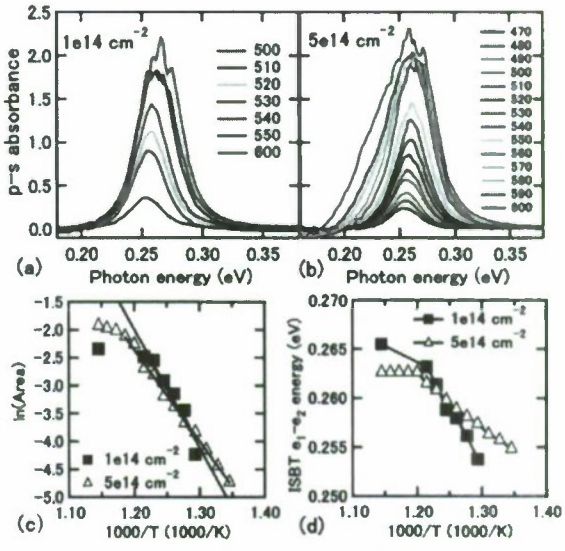

Figure 3. Annealing temperature dependences of e_1-e_2 absorption for (a) 1e14, and (b) 5e14cm^{-2}, (c) integral area, and (d) e_1-e_2 peak energy. RTA time: 1 min.

Fig. 3(a) and 3(b) further clarify the temperature evolution of e_1-e_2 absorption for 1e14 cm^{-2} and another higher dose 5e14 cm^{-2}. The corresponding integral absorption area and peak energy are given in Fig. 3(c) and 3(d), respectively. In Fig. 3(c), with increasing temperature, both doses show linear increase first, indicating the carrier density enhancement, and then a step-like saturation, indicating the near completion of carrier activation. By linearly fitting the linear part, two carrier activation energies were estimated to be 1.41 and 1.21eV respectively for 1e14 and 5e14 cm^{-2}. The small difference in these two energies may come from the difference in diffusion energy that depends on implantation dose. QWI influences both ISBT and interband transition (IBT) energies (7). As seen in Fig. 3(d), the e_1-e_2 energy first shows linear blue shift and a subsequent step-like for both doses, which comes from the near completion of QWI. Using $k \cdot p$ calculation (8), we have revealed the e_1-e_2 blueshift with QWI taken into consideration (9).

The real carrier densities were measured by Hall to be about 7.5e13 and 1e14 cm^{-2} for the samples annealed at 600°C for 1 min with the doses of 1e14 and 5e14 cm^{-2}, respectively. This illustrates the decrease in Si activation efficiency from 75% to 20% when the dose increases five times from 1e14 cm^{-2}. The carrier density cannot linearly increase with the dose because the higher dose produces the higher density of deep-level defects that will greatly trap electrons. The absorption due to mid-gap states in as-implanted samples (not shown) gave evidences. We have confirmed that with increasing RTA temperature, the defect-induced absorption can be greatly reduced and the optical loss reaches a similar level of the as-grown one. This is very important for achieving a low waveguide propagation loss in the final integrated MZI.

IV. Quantum well intermixing

Fig. 4 shows the dose dependent interband absorption spectra where a higher dose corresponds to a larger interband absorption edge (IAE) shift and a smaller IAE slope. Generally, the carrier density enhancement is another factor in addition to QWI that can result in the IAE blue shift. For carrier density effect, an increase of 2e18 cm^{-3} in the bulk density can only contribute ~20 meV shift in IAE based on our previous study as seen from Fig. 5(a) in Ref. (8). Even for the highest dose (5e14 cm^{-2}) in Fig. 4, the bulk density is only of ~1.8e18 cm^{-3} estimated from the actual Hall sheet density of 1e14 cm^{-2}. But there are ~106 (~160 nm) and 180 meV blueshifts in IAE for 1e14 and 5e14 cm^{-2}, respectively, in Fig. 4. Therefore, the experimental IAE blue shifts do not come from the carrier density enhancement.

Moreover, we observed a quick decrease in IAE slope with increasing dose. For the doses from 1e12 to 5e14 cm^{-3}, the carrier density enhancement is just <2e18 cm^{-3} which cannot cause such a large IAE slope decrease based on Fig. 2(d) and Fig. 5(a) in Ref. (8). In fact, it comes from the non-uniformity of QWI due to the inhomogenous Si ion distribution.

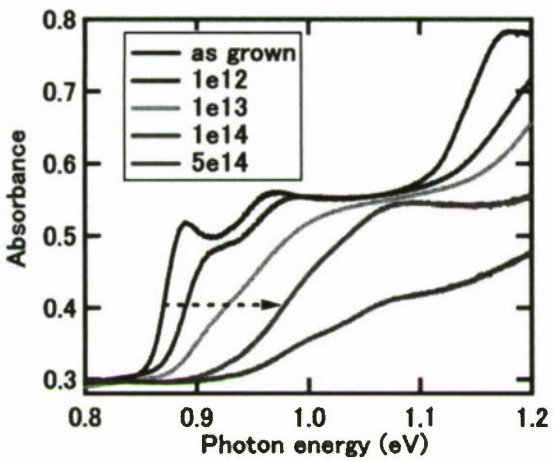

Figure 4. Interband absorption spectra for various doses (in unit of cm^{-2}) annealed at 600°C for 1 min.

In the following parts, we discuss the QWI and its non-uniformity using SIMS and TEM measurements. The Si ion distribution along 60 cycles of CDQWs was studied by SIMS for the as-implanted and annealed samples. As shown in Fig. 5, Si distributions in both samples exhibit inhomogeneity. The Si ion distribution simulated by the stopping and range of ions in matters (10) well reproduces the experimental one in the top half of epilayer, however underestimates the ion density in the bottom part. In experimental SIMS spectra, two peaks located at the surface and the interface (~600 nm) between epilayer and substrate are not true Si ion signal, both of which may come from impurity induced change in ionization efficiency. The sheet densities within the depth from ~30 to ~580 nm are ~1.06e14 and 1.11e14 cm^{-2}, respectively, for as-implanted and RTA samples. These densities are consistent with the dose of 1e14 cm^{-2}. We can obtain two conclusions from SIMS: (i) RTA does not induce big change in the overall spectral feature of Si distribution. In other words, Si ions did not become even distribution by a long distance diffusion during RTA. This is understandable because high Al composition (>=0.3) is not in favor of diffusion (7). (ii) However, a local diffusion within one or two CDQWs was observed for Si ions. Around the region B in Fig. 5, obvious density variations occurred after RTA, which gives the evidence that more Si ions moved into into well to behave as donors because Si ions continuously distributed from well to barrier in the as-implanted sample. This inhomogenous Si distribution will unavoidable result in the non-uniformity of QWI which dominates the spectral shape in Fig. 4.

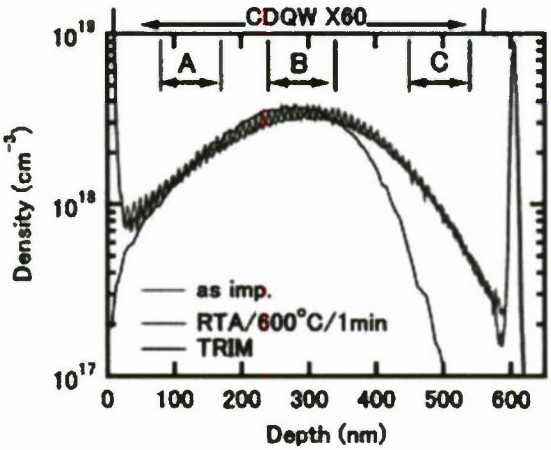

Figure 5. Depth distribution of Si measured by SIMS for the as-implanted sample (1e14 cm^{-2}) and this sample after RTA at 600°C for one minute. Si ion distribution simulated by the stopping and range of ions in matter (TRIM) [Ref. (10)] was given for comparison. Three regions are marked by A, B, and C for structural observation by TEM.

To give more visual evidence for QWI and its non-uniformity, we compare the TEM images among three depth regions marked in Fig. 5 for the as-implanted and annealed samples used for SIMS measurements as well as the as-grown sample. As shown in Fig. 6, for the as-grown sample, three regions have the same TEM images where the central AlGaAs barrier is clearly resolved. For the as-implanted sample, the contrast between the central barrier and the well gradually becomes weaker from regions C to A and region C is almost same as that of the as-grown sample. More closer to the surface the CDQW is, more stronger the disordering is because the top part undergoes much more ion bombard than the bottom which induces the higher vacancy density that is in favor of intermixing. After RTA, as seen in Fig. 6, all regions were intermixed to some degree. In regions A and B after

RTA, we cannot resolve the center barrier any more, indicating that the CDQW nearly becomes single quantum well (SQW). The well (white part) and the AlAsSb barrier (black part) in regions A and B become thicker and thinner, respectively than those in the as-grown sample, and meanwhile the interfaces between the well and barrier are not as sharp as those in the as-grown images. This gives the direct evidence for QWI. The region C after RTA was less intermixed compared to regions A and B because the well-barrier interfaces are slightly sharper and the center barrier can still be seen in the bottom even though the contrast is weaker than the as-grown and as-implanted samples. Therefore, based on the SIMS and TEM analysis, QWI and its non-uniformity are confirmed. In Fig. 3(b), the e_1-e_2 peak becomes asymmetric after 570°C which may be related to such a non-uniformity of QWI.

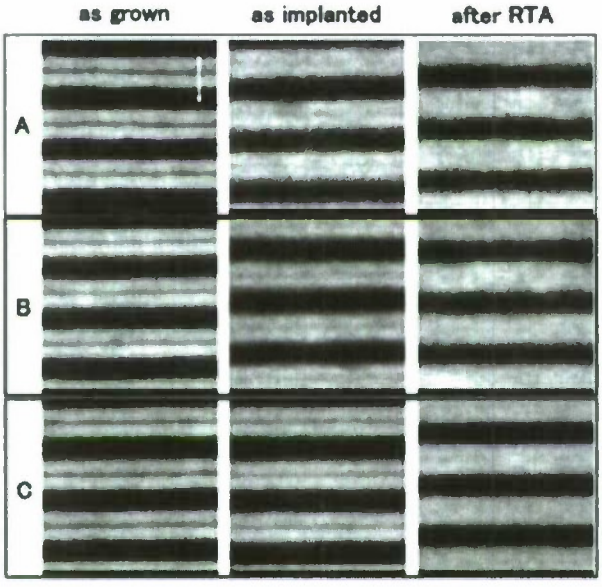

Figure 6. TEM images acquired from three regions A, B, and C denoted in Fig. 5 for three samples: as-grown sample, as-implanted sample with the dose of 1e14 cm^{-2}, and this implanted sample after RTA (600°C for one minute). A white arrow indicates one cycle of CDQW in the left-top image and all scales are 5 nm.

V. Conclusions

We generated the intersubband absorption and QWI through silicon ion implantation and rapid thermal annealing in undoped III-V CDQWs. For the sample with the dose of 1e14 cm^{-2}, we obtained the actual carrier density of ~ 7.5e13 cm^{-2} (~75% activation efficiency) and ~160 nm blueshift of IAE when it was annealed at 600°C for 1 min. The non-uniform QWI was confirmed by SIMS and TEM measurements, which dominates the interband absorption spectral shape. This controllable method to generate ISBT can be used to monolithically integrate ISBT-XPM-based photonic devices.

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ROOM TEMPERATURE PICOSECOND MODE-LOCKED PULSE GENERATION FROM A 1.55μm VECSEL WITH AN InGaAsN/GaAsN FAST SATURABLE ABSORBER MIRROR

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Abstract—**A 1.55μm VECSEL with a metal-GaAs/AlAs hybrid metamorphic mirror optimized for high power room temperature operation has been assembled with a fast saturable absorber mirror (SESAM) in a four-mirror cavity to generate mode-locked pulses at a frequency of 2 GHz. Stable pulses are obtained at room temperature avoiding the need for water cooling, with a pulsewidth < 2 ps and an average optical power at the output coupling mirror of 10 mW. The RF linewidth of the free running laser has been measured to be less than 1000 Hz.**

Keywords- *VECSEL, Bragg Mirror, Thermal Optimization, Passive mode-locking, Saturable absorber*

I. INTRODUCTION

Vertical-external-cavity surface-emitting lasers (VECSELs) are ideal sources for the generation of high power and high quality beams. The use of a semiconductor saturable absorber mirror (SESAM) allows for obtaining passively mode-locked pulses with a good intrinsic temporal stability owing to the small thickness of the active semiconductor medium and the high finesse of the cavity. Active stabilization of the cavity length has already led to obtain sub-ps temporal jitter from mode-locked VECSELs based on GaAs material in the 850 nm – 1 μm wavelength range [1]. Low-jitter pulse sources at 1.55 μm are of particular interest since they can be used as optical clock or sampling gate in optical clock recovery or sampling systems. However, the poor thermal behaviour of quaternary InP-based semiconductor compounds is detrimental to mode-locking since a high intra-cavity power is generally required to achieve an efficient saturation of the fast SESAM. A top-mounted heat spreader is an efficient solution for CW laser operation [2], and has recently been reported for operation in the mode-locked regime [3], however it may introduce an unwanted spectral selection limiting the minimum pulse-width. Moreover it is not easily compatible with electrical pumping of the ½-VCSEL structure. In another approach optimizing downward heat sinking, we have recently demonstrated high power (> 80mW) CW RT operation of an optically-pumped 1.55 μm VECSEL using a thermally optimised ½-VCSEL chip with a hybrid metal-metamorphic GaAs/AlAs mirror and bonded on a SiC substrate [4,5]. We have also shown that due to the good thermal conductivity of the metal-metamorphic mirror, the use of a CVD diamond host substrate instead of the SiC substrate can further improve the thermal resistance of the ½-VCSEL chip and reduce the thermal effects for large diameter pump spot [6]. The thermally-optimized ½-VCSEL chip is assembled in a 4-mirror cavity with a 1.55μm fast saturable absorber to generate passively mode-locked pulses.

II. VECSEL CONFIGUARTION AND CW PERFORMACES

The InP-based 2λ-thick active region grown in reverse order by metal-organic vapour-phase epitaxy includes eight strained InGaAlAs quantum wells distributed among three optical standing-wave antinode positions with a 4-2-2 distribution. Molecular beam epitaxy regrowth is then used to form a 15-pair metamorphic GaAs/AlAs semiconductor Bragg mirror [7] whose reflectivity is enhanced thanks to the deposition of a 150 nm-thick Au layer, and is calculated to be greater than 99.9% at 1550 nm. The overall structure is then mounted onto a high thermal conductivity CVD-diamond substrate thanks to an AuIn2 eutectic bonding [8]. After removal of the InP-susbtrate and of the etch–stop layer, a quarter-wavelength $SiON_x$ anti-reflecting (AR) layer at 980 nm (wavelength of the laser diode pump) is deposited on the sample surface. The thickness of the top InP layer acting as a phase layer is precisely etched, so that the position of the resonant half-cavity mode is close to the gain maximum the after AR layer deposition.

The ½-VCSEL chip has first been assembled in a plane-concave cavity (concave dielectric mirror, R ~ 99%) for the evaluation of its CW performance at room temperature (RT) under optical pumping. The RT-CW tests have also been used to identify the optimized position of the resonant half-cavity mode

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leading to the lowest threshold and highest optical output power. The L(P) characteristics obtained using a large diameter (~ 100 µm) multimode pump laser diode are reported in Fig. 1. No thermal roll-over was observed, and > 100 mW RT- CW output power ($TEM_{0,0}$ emission) at 1.55 µm could be achieved.

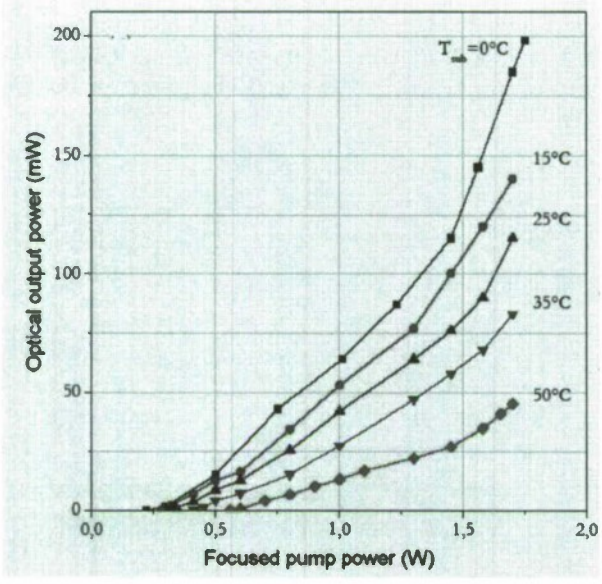

Fig. 1. : L(P) curves in plane-concave cavity configuration, using a 99% HR dielectric mirror, for different temperatures. Water cooling of the heatsink was used for T ≤ 15°C, while a TE cooler alone (no water flow) is sufficient above 20°C.

III. Mode-Locked Pulse Generation

The ½-VCSEL chip has then been assembled with a fast SESAM in a 4-mirror cavity configuration depicted in Fig. 2 with a cavity frequency of 2 GHz (cavity length of 7.5 mm). The cavity design has been chosen in order to allow for an almost independent adjustment of the mode radius on the gain and the absorber by varying the arm lengths, and for a high gain since in one cavity round trip the beam passes twice in the gain medium and just once in the SESAM. The ratio of the gain/absorber spot radii is typically greater than 5, allowing for obtaining a high power density in the absorbing region. The ½-VCSEL chip temperature was regulated thanks to a TE cooler, while the SESAM was not regulated.

The SESAM structure grown by MBE on a GaAs substrate consists of a 35-pair GaAs/AlAs Bragg mirror and a GaAs layer including the absorbing region formed by an InGaAsN quantum well surrounded by 2 GaAsN fast recombination layers. The absorption recovery time of the InGaAsN/GaAsN structure has been separately measured to be around 15 ps thanks to fast tunnelling and recombination into the GaAsN planes [9]. The GaAs cavity optical thickness has been fixed to present an anti-resonant configuration in order to minimize the absorption. It was however observed that the saturation contrast was low and did not allow for achieving mode-locking operation. A SiONx AR layer at 1550nm was thus deposited on the SESAM surface.

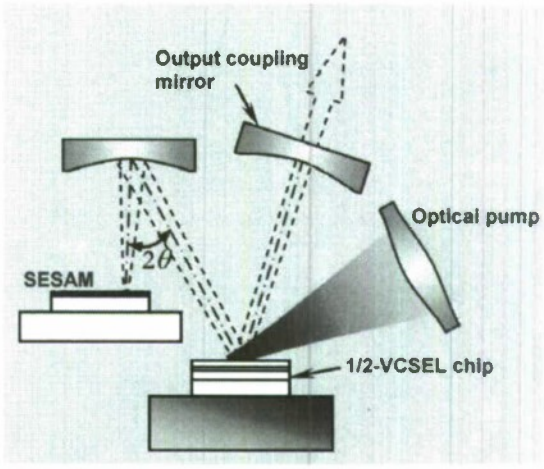

Fig. 2 : Schematics of the four-mirror cavity

Mode locking was established by tuning one arm length in order to minimize the spot size on the SESAM structure. The spectro-temporal characteristics of the pulsed emission are displayed in Fig. 3. Stable pulses are obtained at the 2 GHz fundamental repetition frequency. The pulsewidth estimated from the autocorrelation trace is of ~ 1.7 ps at T = 25 °C, and the average optical power at the output coupling mirror was measured to be ~ 10 mW. The time-bandwidth product calculated assuming a Gaussian pulse is of ~ 0.5 close to the Fourier-transform limit.

Finally the RF linewidth was measured for the fundamental frequency and the first harmonics and was estimated to be smaller than 1000 Hz for the free-running laser (see Fig. 4). This result indicates that the VECSEL cavity has the potential of producing short mode-locked pulse train with a low temporal jitter.

Acknowledgemnts

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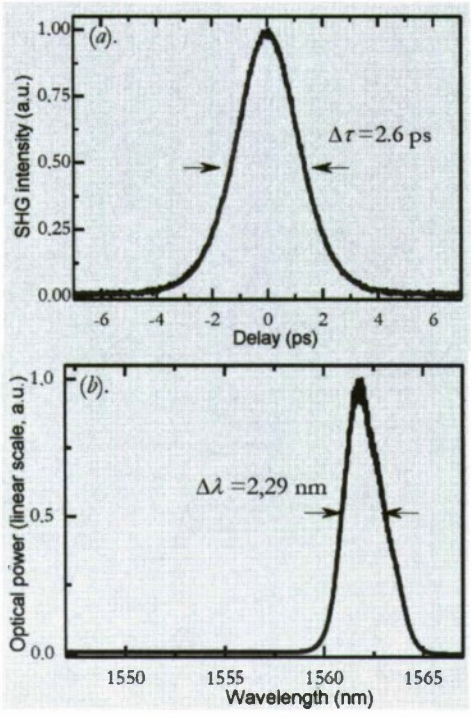

Fig. 3: (a)/ Autocorrelation trace (blue line) fitted by a Gaussian profile (red line) of the mode-locked pulses at T = 25°C. (b): corresponding time-averaged optical spectrum.

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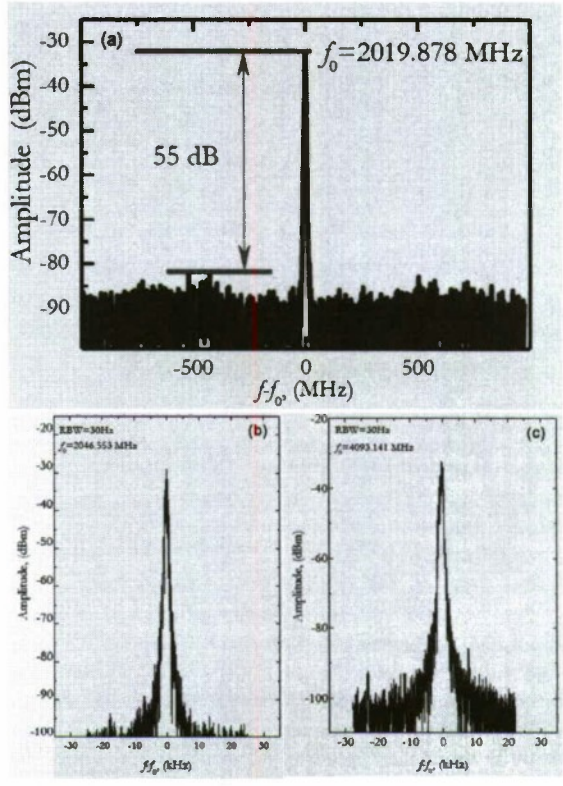

Fig. 4. : (a) RF spectrum of the pulsed signal at the fundamental frequency, corresponding to the pulse conditions of Fig. 2. (b) and (c) closer view with a 30 Hz resolution bandwidth for the fundamental (2GHz) [in (b)] and first (4GHz) [in (c)] harmonics.

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AMMONOTHERMAL TECHNOLOGY FOR BULK GALLIUM NITRIDE CRYSTALS

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ABSTRACT

The growth of bulk gallium nitride crystals can only be made from the vapor or liquid phase. The ammonothermal method is emerging as a potential alternative to the hydride vapor phase growth method. A short outline over the technology and some of the recent results from the acidic ammonothermal growth of GaN are presented.

I. INTRODUCTION

The fabrication of gallium nitride (GaN)-based high-power devices requires lattice and thermally matched substrates, which are characterized by a low crystal defect density. Consequently, GaN is the best choice and free-standing, strain-free GaN bulk crystals are required. Limited by its thermodynamic properties the crystal growth of bulk GaN under considerably modest conditions can only be done by the hydride vapor phase epitaxy (HVPE) [1] and from solution in form of the Na-flux method [2] or ammonothermal method [3]. The latter illustrates a promising path for a high-throughput technology, which has proven success in case of quartz (α-SiO_2) and more recently zinc oxide (ZnO) crystal growth [4]. Early reports on the ammonothermal growth of group-III nitride crystals, firstly AlN and followed by GaN, dating back to the early 1990s [3, 5].

The ammonothermal method for the growth of group-III nitride crystals with focus on GaN has been reviewed recently by Wang and Callahan in 2006 [6] and by Ehrentraut and Fukuda in 2010 [7]. During these 4 years, tremendous progress has been published by the few groups worldwide involved in the ammonothermal crystal growth technology. Very recently, a 1.5 size GaN wafer sliced from a bulk GaN crystal grown by the alkaline ammonothermal method had been shown and employed for the homoepitaxial growth of GaN by metal organic chemical vapor deposition (MOCVD) [8]. More achievements by the ammonothermal method are summarized in ref. [7].

The currently strong and growing involvements of industry in the research and development and the high expectations of the ammonothermal technology towards mass production of GaN bulk crystals brings along with the need to protect intellectual properties. Hence, details on experiments are often not exhaustive, however, refs. [6, 7] present a suited insight into the matter.

This paper will provide a very brief overview of the ammonothermal method for GaN crystal growth under acidic conditions with some comparison to the growth under alkaline conditions.

II. AMMONOTHERMAL METHOD

The ammonothermal method for GaN crystal growth is carried out under supercritical (SC) conditions of ammonia (NH_3), i.e., temperature and pressure well above $T > 132$°C and $p > 11.2$ MPa, respectively. SC NH_3 is knowingly a poor solvent for GaN, but a number of metal salts can be dissolved. Due to its weak reactivity alkali amides (for alkaline ammonothermal path) or ammonium halogenides (for acidic ammonothermal path), the both also named a mineralizer, is added to SC NH_3 to form the solvent. The solvent dissolves the GaN feedstock to form a SC NH_3-mineralizer solution, which is now containing metastable GaN complexes – the right species to conduct the growth process. This solution is being transported by convection to the GaN seed crystal (step I) where crystal growth (step II) is triggered through supersaturation of the solution. After depositing the dissolved GaN, the now under-saturated solution circulates back to the feedstock

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zone (step III) to continue the process of dissolution, transport, and growth. Figure 1 illustrates the simplified process. As one may guess, a closed system is used to contain the pressure. Consequently, autoclaves are being employed and their design is crucial to endure the needed pressures of 150-400 MPa at temperatures as high as 650°C, harsh conditions which are lasting several months to yield large GaN crystals.

Critical issues are the material, the inner surface, and the sealing of the autoclave. In case of the acidic ammonothermal growth method, the inner surface is tightly covered with a Pt-based alloy, which also provides the strength to resist possible plastic deformation like may be the case of the pure Pt.

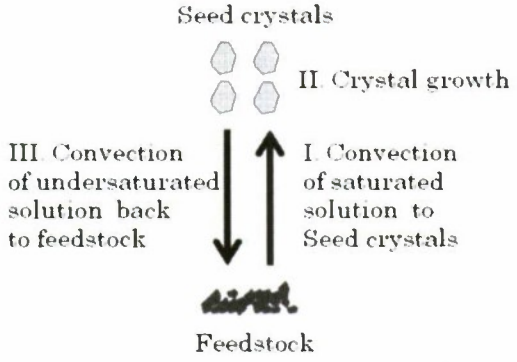

Fig. 1. Principal scheme of the ammonothermal method to grow GaN inside an autoclave.

A typical growth run starts with charging the autoclave with polycrystalline GaN (obtained from HVPE process), NH_4Cl as mineralizer, inserting a baffle to establish a suited T gradient between the zone with feedstock and seed crystals, and sealing the autoclave. After vacuuming and flushing with an inert gas, ammonia is being inserted to achieve a 50-70% fill factor. Now the temperature program can be started and crystal growth of GaN will soon after commence.

As reported earlier [9] other choices for the mineralizer comprises NH_4Br and NH_4I. The latter has shown to provide a high yield in terms of dissolved and re-crystallized GaN feedstock during similar time interval; hence, a high growth rate may be expected. On the other hand, the increase in the acidity from NH_4Cl toward NH_4I seems to favor the cubic over the hexagonal phase of GaN in case of growth without seed crystal. However, employing a hexagonal GaN seed crystal results in the growth of hexagonal GaN even when using NH_4Cl as the mineralizer [9].

The solubility of the GaN precursor is governed by the amount and type of mineralizer: acidic mineralizer cause a positive solubility coefficient whilst alkali mineralizers yield a negative solubility coefficient for the temperature range of interest. This difference requires the opposite conditions for the growth setup. The thermal design is such that GaN crystal growth must be carried out in the colder or hotter zone of the autoclave in case of acidic or alkali mineralizer, respectively. Consequently, the feedstock is placed in the hotter or colder zone in case of acidic or alkali mineralizer, respectively.

III. SOME RESULTS FROM CRYSTAL GROWTH

A great deal of the results is published in refs. [7, 9, 10]. The GaN crystals grow at relatively slow rates of maximum 50 μm per day for growth durations of up to 2-3 weeks. A higher growth temperature of 600°C favors the high growth rate. The increase of system pressure close to 200 MPa comes along with the increased growth temperature, depending on the fill factor and amount of mineralizer. It is interesting to note that the growth rates under alkaline ammonothermal conditions are very similar to those observed by us, i.e., 30-80 μm per day as combined for the Ga and N-polar face in case of the growth on (0001) GaN seed crystals [11, 12].

A major issue is the quality of the seed crystal. Only a strain-free crystal with very low bending (bending radius preferably >100 m; typical HVPE-GaN <10 m) can be used for the growth of high quality GaN. Thus far, we have been using (0001) HVPE-GaN as seed crystals. The x-ray rocking curve full-width at half-maximum (FWHM) using the (0002) reflection showed 108 and 339 arcsec for GaN grown on the (0001) and (000$\bar{1}$) polar faces, respectively. More recently, values below 100 arcsec were achieved for the Ga polar face of a sample grown at higher temperature. To compare with, a MOCVD film grown on a high quality (0001) GaN substrate prepared by the alkaline ammonothermal method reportedly exhibited a FWHM of 22-24 arcsec from the (0002) reflection [8]. It needs to be noted here that the growth of GaN by the alkaline ammonothermal method is subject to studies for quite longer time scale than is the case for the acidic ammonothermal approach.

Generally, the crystal quality is higher if the growth rate is reduced; at least under the current growth conditions. However, better control of issues like impurities and also additives is proposed to bring valuable improvements. Such effects are much better understood in case of the hydrothermal growth of ZnO [4].

An advantage of the ammonothermal growth method is the simultaneous use of a large number of seed crystals during a growth run. Up sealing has been worked out sueeessfully for ZnO [4] and the similar approach might also work for the ammonothermal method as has been shown by Dwiliński et al. [8].

Impurities are erueial to most of the physieal properties of GaN. From SIMS measurements on a couple of samples levels of transition metals of Cr, Fe, Ni of 10^{15}-10^{18}, 10^{17}-10^{20}, and 10^{17}-10^{20} em^{-3}, respeetively, and Si and O of 10^{19} and 10^{18}-10^{20} em^{-3}, respeetively, were indieated [13]. However, reeent progress in terms of purifieation of starting reaetants shows first results, whieh indicate a lowered eoneentration of O at around 10^{18} em^{-3}. Further verification is under progress.

IV. SUMMARY

The aeidie ammonothermal method provides a possibility to fabrieate bulk GaN erystals. More efforts are required to improve issues such as growth rate and eontent of impurities. The erystallinity of GaN ean be eontrolled by employing high quality seed material.

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Geometry Aspects Influencing the Growth of AlN Bulk Crystals

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Hydride Vapor Phase Epitaxy of AlN at High Temperatures on Freestanding (0001)AlN Substrates

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OBSERVATION OF BIREFRINGENCE DISTRIBUTION CAUSED BY RESIDUAL STRAIN IN BULK C-PLANE GAN SUBSTRATES

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***Abstract*— Strain-induced birefringence has been observed in bulk c-plane GaN substrates. Two-dimensional distribution of index ellipse difference $|\Delta n|$ revealed a variety of distribution such as gradual U-shape distribution with rotational symmetry and chord- and spot-like patterns with three- and/or six-fold symmetries reflecting the whole manufacturing process of substrates. Although the absolute value of the strain is not obtained yet, because of unknown photoelastic constants, the $|\Delta n|$ map is useful for qualitative evaluation of strain distribution over the whole substrate.**

Keywords- GaN, bulk substrate, residual strain, birefringence, polariscope

I. INTRODUCTION

Bulk GaN crystal is promised material as substrates of nitride based devices because it can avoid mismatch in lattice constant and thermal expansion coefficient between the substrate and the homo-epitaxial layer of device structure. It also has several self advantages such as high thermal and electric conductivity and cleavability. Therefore, commercial production of bulk GaN substrate is now on the increase. Almost commercial substrates are manufactured by hetero-epitaxial growth of GaN thick film on a starting wafer such as sapphire, followed by its separation from the starting wafer. In this case, the mismatch in lattice constant and thermal expansion coefficient between the GaN thick film and the starting wafer may cause thermal stress and strain in the cooling process. A part of them is locally frozen into the thick film as residual strain after the manufacture processes. The residual strain causes a local piezoelectric polarization, which may degrade the device performance. Furthermore, it may act as an origin of unwanted crack or breakage in the substrate during the thermal processes for device fabrication. Therefore, it is important to characterize the residual strain distribution in the bulk GaN substrates. However, as far as we have surveyed, there is no report about residual strain distribution in bulk GaN substrate.

By developing several versions of scanning infrared polariscope (SIRP) [1-3], we have studied the residual strain distribution in commercial substrates of III-V compound semiconductors such as InP, GaP and GaAs to demonstrate a feasibility of residual strain as a quality measure [4,5]. Figure 1 shows the block diagram of the SIRP. Its optical configuration is similar to the conventional linear polariscope but it is not aimed to observe the fringe pattern. The transmitted light intensities are directly analyzed as a function of the polarizer direction while rotating the polarizer and analyzer simultaneously with the crossed and paralleled condition. This sophisticated technique enables us to evaluate the index ellipse difference $|\Delta n|$ and the principal angle ψ at much less than the fringe level. Two-dimensional distribution of $|\Delta n|$ and ψ can be obtained by scanning the probing light over the whole substrate. In the case of InP, GaP and GaAs, the absolute values of in-plane strain component for (100) substrates can be quantitatively evaluated from the measured $|\Delta n|$ and ψ because the corresponding photoelastic constants p_{11}-p_{12} and p_{44} are known.

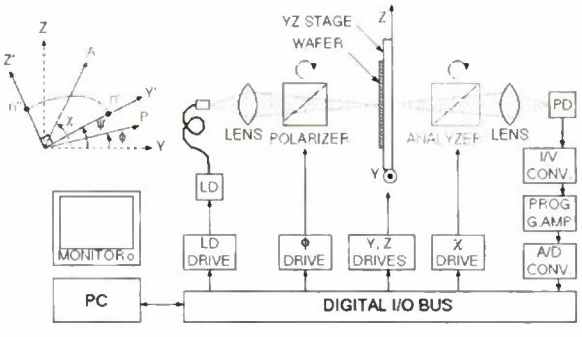

Figure 1. Block diagram of the SIRP

In this paper, we present the first study about residual strain distribution in bulk substrates of wurtzite GaN crystal. It is well known that wurtzite GaN crystal has natural birefringence. However, it does not exhibit if the probing light propagates perpendicular to the c-plane. Therefore we can observe the birefringence distribution caused by the residual strain in the c-plane substrate without compensating the natural birefringence.

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Experimental results of two-dimensional map and diametral profiles of $|\Delta n|$ are shown to demonstrate typical distribution of residual strain in bulk GaN substrates.

II. EXPERIMENTAL RESULTS

The samples observed in this study were commercially-available 2-inch (0001) substrates of wurtzite GaN crystal grown by a halogen vapor phase epitaxy (HVPE) technique. The substrate thickness was 420 μm and the surfaces were mirror-like polished on both sides. In the SIRP measurement, the substrate is arranged so that its surface is perpendieular to the probing light. It should be noted that actual c-plane GaN substrates sometimes have slight off-angle and it may cause natural birefringenee act as a uniform bias in the measurement of $|\Delta n|$. In order to estimate and minimize the off-angle effeet, the substrate was slightly tilted from the perpendicular arrangement so that the average value of $|\Delta n|$ should be minimized. The best tilts for the substrates used in this study were less than one degree.

Figure 2 shows an example of typical two-dimensional distribution of $|\Delta n|$ measured in bulk GaN substrates. The normalized value of $|\Delta n|$ is shown at the top of grayscale. The crystallographic orientations are noted as arrows at the lower left of the map. It was found that the $|\Delta n|$ was larger in the peripheral region than in the eenter region. Sueh $|\Delta n|$ increase was found in every direction of peripheral region. On the other hand, the fluctuation of $|\Delta n|$ was small in the center region. Therefore, it revealed rotational symmetry of macroscopic distribution over the whole substrate. The diametral profiles of $|\Delta n|$ along the $\langle \bar{1}100 \rangle$ and $\langle 11\bar{2}0 \rangle$ directions are also shown in Fig. 3. They revealed a gradual U-shape profile over the diameter in both directions. The maximum value of $|\Delta n|$ was about 3×10^{-5} at the edge. In addition to the U-shape profile, a small fluetuation was also found through the whole diameter.

Another example of $|\Delta n|$ distribution is shown in Fig. 4. Although the large $|\Delta n|$ was found in peripheral region, its extent was different in eaeh direetion. Furthermore, the $|\Delta n|$ was strongly varied in the center and mid regions. Especialty, it was found that three ehord-like patterns went through the mid region of the substrate. They were roughly aligned to the $\langle 11\bar{2}0 \rangle$ erystallographic orientations. The distorted spot-like patterns were also found in the mid region. Unlike the Fig.2, it revealed distorted three-fold symmetries rather than rotational one. The symmetry center did not exaetly eorrespond to the substrate center. Figure 5 shows the diametral profiles of the substrate shown in Fig.4. The peaks of $|\Delta n|$ corresponding to the chord-like patterns were indicated with black arrows. The maximum value of $|\Delta n|$ attained to 5×10^{-5} at the edge. Unlike the Fig. 3, they revealed strong fluetuation over the whole diameter. The profile was strongly varied with direction mainly because of the position of chord-like patterns.

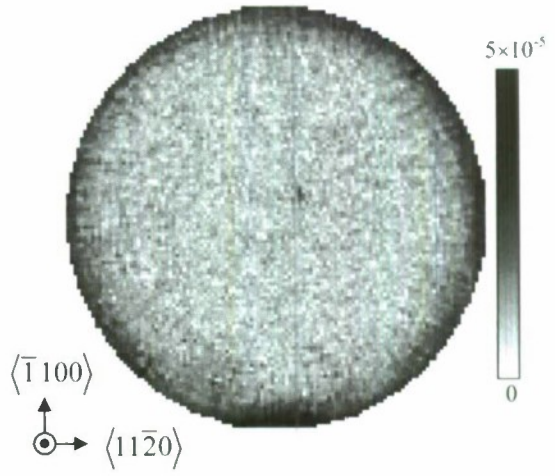

Figure 2. Two-dimensional distribution of $|\Delta n|$ in a 2-inch bulk GaN substrate

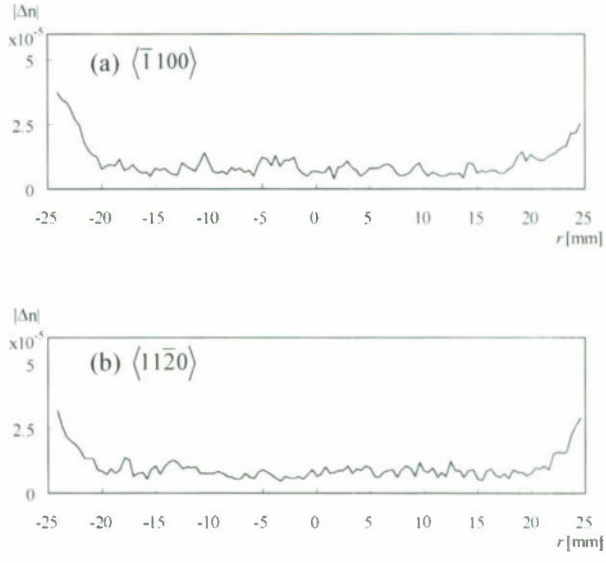

Figure 3. The diametral profiles of $|\Delta n|$ along (a) $\langle \bar{1}100 \rangle$ and (b) $\langle 11\bar{2}0 \rangle$ directions measured in the substrate shown in Fig. 2

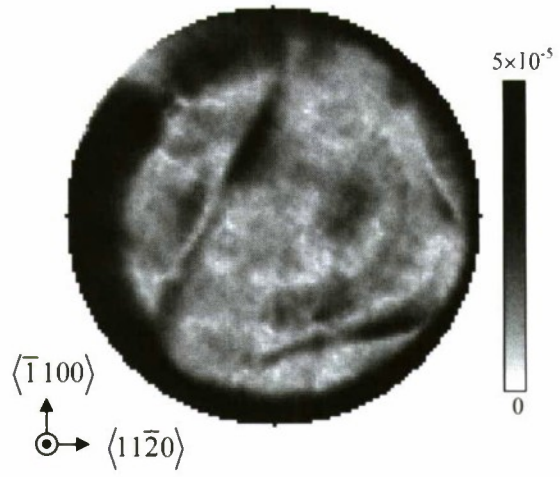

Figure 4. Two-dimensional distribution of $|\Delta n|$ in another bulk GaN substrate than that shown in Fig. 2.

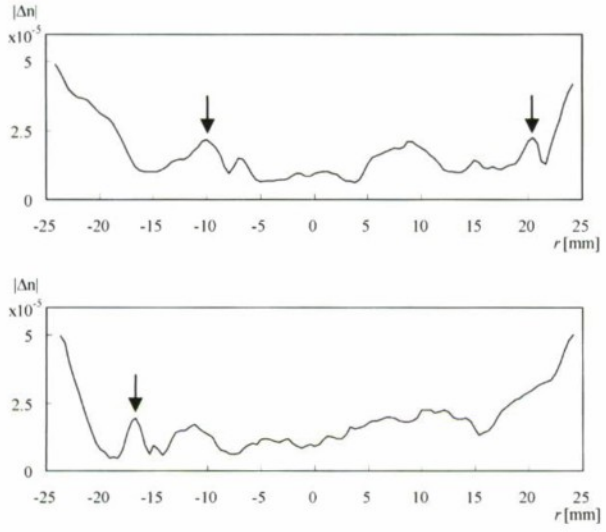

Figure 5. The diametral profiles of $|\Delta n|$ along (a) $\langle \bar{1}100 \rangle$ and (b) $\langle 11\bar{2}0 \rangle$ directions measured in the substrate shown in Fig. 4

In addition to the substrates shown in Figs. 2 and 4, we have examined several substrates. Many of them revealed the gradual U-shape distribution with rotational symmetry and a part of them revealed strong variation with three- and/or six-fold symmetries. However, their detailed distribution was different from each other. Since the $|\Delta n|$ distribution is distinctive characteristic of substrate, it should reflect the whole manufacturing process of the substrate such as growth condition of epitaxial film, structure of the buffer layer, separation technique, and so on. At the present stage, the absolute value of residual strain is not obtained yet, because the photoelastic constants are unknown. However, the SIRP measurement of $|\Delta n|$ is useful even in itself to characterize two-dimensional distribution of residual strain qualitatively over the whole substrate.

III. Conclusions

Two-dimensional distribution of strain-induced birefringence has been observed in bulk c-plane GaN substrates. They revealed a variety of distribution such as the gradual U-shape distribution with rotational symmetry and the chord- and spot-like patterns with three- and/or six-fold symmetries. Since the distribution variety should reflect the whole manufacturing process of substrates, the SIRP map of $|\Delta n|$ is useful for evaluating the process condition from the viewpoint of residual strain distribution over the whole substrate. For future quantitative evaluation of residual strain, the experimental study on elasto-optic effect is now in progress to evaluate the photoelastic constants.

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InGaAsN as Absorber in APDs for 1.3 micron Wavelength Applications

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Two issues with using InGaAsN as absorber in avalanche photodiodes (APDs) for 1310nm wavelength applications are addressed here. Firstly, we demonstrated InGaAsN p-i-n diodes with stable photoresponse around 1310nm but reverse leakage current density slightly above the acceptable limit of ~0.2mA/cm^2 at 150kV/cm. We also investigated whether or not InGaAsN as absorber is compatible with $Al_{0.8}Ga_{0.2}As$ (the proposed avalanche material in our separate-absorption-multiplication APD design) in terms of the relationship between α and β in InGaAsN. Our observations suggest $\alpha \sim \beta$ in InGaAsN, making it compatible with $Al_{0.8}Ga_{0.2}As$.

1. Introduction

Current avalanche photodiodes (APDs) for telecommunication systems operating at 1310/1550 nm use InP and $In_{0.53}Ga_{0.47}As$ in their multiplication and absorption layers, respectively. The upper limit of these APD gain-bandwidth products (~150 GHz) is mainly due to the minimum InP multiplication layer thickness required to avoid excessive band-to-band tunnelling current [1]. Although $In_{0.52}Al_{0.48}As$ (lattice-matched to InP) offers a slightly larger band gap (1.4 eV) compared to InP (1.35 eV) and hence a thinner $In_{0.52}Al_{0.48}As$ multiplication layer for the same tunnelling current level, the gain-bandwidth products of $In_{0.53}Ga_{0.47}As$ /$In_{0.52}Al_{0.48}As$ APD are still limited to ~180 GHz [2].

It is therefore desirable for a multiplication layer material to have a bandgap much larger and excess noise performance comparable to, if not better than, those of InAlAs. $Al_{0.8}Ga_{0.2}As$ (lattice-matched to GaAs) is a promising candidate because its (indirect) bandgap is 2.2eV and its excess noise characteristics exhibits low effective ionization coefficients ratio, k_{eff}, for thin avalanche layers [3]. As expected from its bandgap, $Al_{0.8}Ga_{0.2}As$ p-i-n diodes with i-region thinner than 100nm showed reverse leakage currents free from band-to-band tunnelling currents [3]. This is a much lower limit than that of InP and InAlAs, which is close to 200nm. $Al_{0.8}Ga_{0.2}As$ APDs not only promise high speed and low noise performance, but are also compatible with GaAs substrates, which are larger in size and cheaper than InP substrates.

In order to realize $Al_{0.8}Ga_{0.2}As$ APDs for 1310/1550 nm wavelength, GaInNAs with long cut-off wavelength, λ_c, in photoresponse and with acceptable reverse leakage currents [4] can be used as the absorber in Separate-Absorption-Multiplication (SAM) APDs. As dark current increases with decreasing GaInNAs bandgap [4], it is logical to achieve 1310 nm-wavelength operation first before extending to 1550 nm.

Although many GaInNAs photodiodes have been reported to show photon detection (not λ_c) beyond 1310nm, few exhibited relative constant photoresponse of ~ 1.31 μm (more specifically, 1260 to 1360 nm), which is required for APDs used in optical communication systems. None of these GaInNAs photodiodes meet the reverse leakage current density requirement for SAM APDs. The upper limit is ~0.2mA/cm^2 at 150kV/cm, corresponding to ~1nA for a 30μm diameter diode.

In designing SAM APDs, consideration should also be given to whether or not the absorber and the avalanche materials are compatible in terms of their ionization coefficients of electrons and holes, α and β, respectively. As $\alpha > \beta$ in $Al_{0.8}Ga_{0.2}As$, a compatible absorber material should not have $\alpha < \beta$ [5]. Yet, it was predicted that in GaInNAs, the electron-initiated impact ionization process may be suppressed, resulting in $\alpha << \beta$ [6]. So far, there has been no experimental report to investigate this prediction.

In this paper, we address the above two issues concerned with using GaInNAs as absorber in a SAM APD. The first is to improve the photoresponse of GaInNAs material whilst satisfying the leakage current

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limit. The second is to obtain experimental evidence for the relationship between α and β.

II. Photoresponse

In our previous work [4], a p-i-n diode wafer (wafer C in Ref [4]) that detects photons at wavelengths up to 1400 nm and satisfies the leakage current limit was demonstrated using the composition of $Ga_{0.90}In_{0.10}N_{0.038}As_{0.962}$. In this work we report a new p-i-n diode wafer with increased indium and nitrogen fractions to increase the photoresponse wavelength limit. The new wafer structure, summarized in Table 1, differs from the previous wafer only in the absence of the AlAs layer. The composition for the new wafer was nominally $Ga_{0.88}In_{0.12}N_{0.042}As_{0.958}$ to give a bandgap of 0.92eV at room temperature, based on the 0.92eV bandgap at 0K as calculated by Bellaiche [7].

X-ray diffraction curves indicated lattice-mismatch (between the GaInNAs peak and the GaAs substrate peak) ranging from -1.2×10^{-3} to $+1.3\times10^{-3}$ from the centre to the edge of the wafer. Using linear interpolation for the lattice constant of GaInNAs, the corresponding fractions for nitrogen are 4.9 and 3.7%, respectively, which are close to the 4.2% intended.

Circular mesa diodes with four different sizes were fabricated from the wafer using photolithography and wet chemical etching. Reverse dark Current-Voltage (I-V) and Capacitance-Voltage (C-V) characteristics were measured from these diodes at room temperature. Reverse dark currents of the different sized diodes scaled with diode area so bulk dark current density, J, versus bias was obtained.

C-V data were needed to deduce the unintentional doping (u.i.d.) level in the i-GaInNAs layer. Full depletion was achieved from -2V onwards. Using an abrupt 3-region Poisson solver and deduced u.i.d level ($\sim10^{16}cm^{-3}$), electric field profile was calculated at different reverse biases to yield leakage current density versus peak electric field, J-E.

The J-E results are compared to those of wafer C from Ref [4] in Fig. 1. At an electric field of 150 kV/cm, the leakage current density increases from 0.06 mA/cm^2 to 0.5 mA/cm^2, exceeding the acceptable current limit. A re-growth of structure similar to wafer C in Ref [4], except without the AlAs layer, yielded higher leakage current densities than wafer C itself, as shown in Fig. 1. This increase in leakage current density suggests that the wafer quality in the new growth is poorer than that in wafer C. Hence, there is still room for improvement in the dark currents of the $Ga_{0.88}In_{0.12}N_{0.042}As_{0.958}$ p-i-n diodes in future growth.

Since the $Ga_{0.88}In_{0.12}N_{0.042}As_{0.958}$ p-i-n diodes exceed the current density limit by a small margin, it is still worthwhile to study its photoresponse versus wavelength. Using a tungsten lamp and a monochromator, the photocurrent versus wavelength characteristics was measured on the diodes at room temperature. Due to non-uniformity in composition across the wafer, the measurements were performed on diodes from different parts of the wafer, namely centre, middle and edge.

TABLE 1: Structure details of the GaInNAs p-i-n diode wafer for photoresponse work.

Layer	Thickness(nm)
p^{++} GaAs	20
p^{+} GaAs	480
p^{+} GaInNAs	50
i GaInNAs	400
n^{+} GaInNAs	50
n^{+} GaAs	300
n^{+} GaAs substrate	

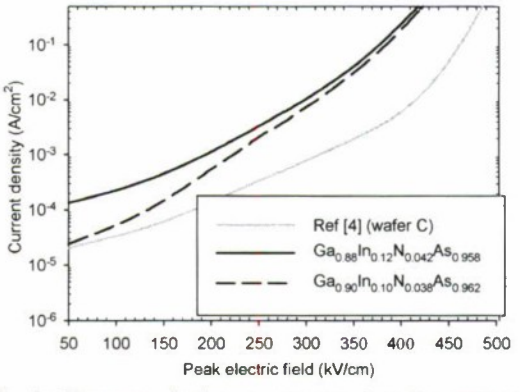

FIG. 1: Reverse leakage current density versus peak electric field of the $Ga_{0.88}In_{0.12}N_{0.042}As_{0.958}$ p-i-n diodes at room temperature. The results are compared to that of wafer C in Ref [4] for the wider bandgap $Ga_{0.90}In_{0.10}N_{0.038}As_{0.962}$.

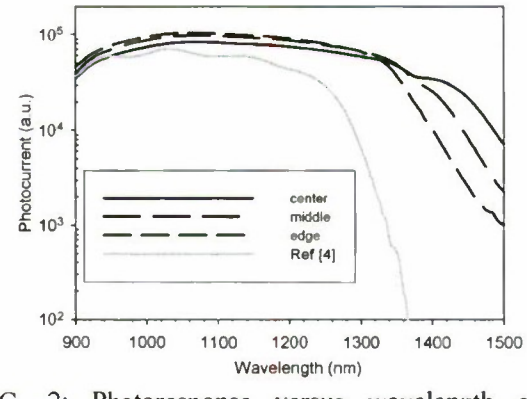

FIG. 2: Photoresponse versus wavelength of the $Ga_{0.88}In_{0.12}N_{0.042}As_{0.958}$ p-i-n diodes at -2V and room temperature, compared to the data of wafer C from Ref [4] for the wider bandgap $Ga_{0.90}In_{0.10}N_{0.038}As_{0.962}$.

Since the C-V data indicated full depletion from -2V onwards, the data for -2 V measurements are compared in Fig. 2. Again the data from wafer C in Ref [4] provide a useful reference and are included in Fig. 2. The photoresponse of the new wafer from all parts of the wafer clearly covers longer wavelengths than before, achieving a relatively constant response of ~1300nm. The lack of fringes on data from the new wafer compared to the previous wafer is due to the absence of the AlAs layer, which previously formed an optical cavity in the wafer C.

III. Relationship between α and β

For the investigation of relationship between α and β, a p-i-n diode wafer and a n-i-p diode wafer with 0.8μm i-layer were used. Their structures are described in Table 2. The composition of $Ga_{0.90}In_{0.10}N_{0.038}As_{0.962}$ (instead of $Ga_{0.88}In_{0.12}N_{0.042}As_{0.958}$) and the thicker i-layer were designed to minimize leakage currents, which could make measurements difficult. Also, the dead space effects are likely to be insignificant in 800nm-thick avalanche layers.

Again, circular mesa diodes were fabricated from these wafers. The investigation relied on the avalanche multiplication versus bias, $M(V)$, data obtained from the photomultiplication measurements of these diodes. The setup employed phase-sensitive detection through mechanically chopped laser light and a lock-in amplifier. Reverse bias to the device-under-test was provided by a Source-Measure-Unit via a small series resistor.

It is well known that, for a given diode, the measured gain is dependent on the carrier injection profile, which in turn depends on the wavelength of laser light used in the measurements. For example, in a p-i-n diode, if a short-wavelength light illuminates the p-side and is absorbed strongly within the p-cladding, then we obtain $M(V)$ data due to pure-electron injection, $M_e(V)$. Choosing a wavelength to which the p-cladding is transparent yet is absorbed in the i-layer will generate carriers within the i-layer only, resulting in mixed-carrier injection multiplication data, $M_{mix}(V)$.

In our photomultiplication measurements, lasers with wavelengths of 532nm and 1064nm were used. The 532nm laser light is strongly absorbed by the top GaAs cladding layer, giving rise to $M_e(V)$ and pure-hole multiplication, $M_h(V)$, for the p-i-n and the n-i-p diodes, respectively. Using the 1064nm light, which is not absorbed in GaAs, mixed-carrier profiles were created within the i-GaInNAs layer, with heavier weighting on electrons and holes, for the p-i-n and the n-i-p diodes, respectively.

The multiplication factor data for both p-i-n and n-i-p diodes are compared in Fig. 3. Despite the different carrier injection profiles achieved using the two different laser lights, $M_{e(h)}(V)$ and $M_{mix}(V)$ data for a given wafer were indistinguishable, indicating similar values for α and β at a given electric field. With $\alpha \sim \beta$, the GaInNAs material is compatible with $Al_{0.8}Ga_{0.2}As$ to form a SAM APD.

TABLE 2: Structure details of the GaInNAs 0.8μm p-i-n and n-i-p diode wafers for investigating relationship between α and β.

Layer		Thickness
p-i-n	n-i-p	(nm)
p^{++} GaAs	n^{++} GaAs	20
p^{+} GaAs	n^{+} GaAs	480
p^{+} GaInNAs	n^{+} GaInNAs	50
i GaInNAs	i GaInNAs	800
n^{+} GaInNAs	p^{+} GaInNAs	50
n^{+} GaAs	p^{+} GaAs	300 (p-i-n) 2000 (n-i-p)
n^{+} GaAs substrate		

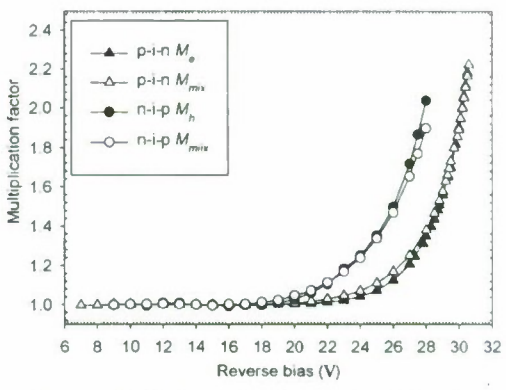

FIG. 3: $M_e(V)$ and $M_{mix}(V)$ for the 0.8μm $Ga_{0.90}In_{0.10}N_{0.038}As_{0.962}$ p-i-n and n-i-p diodes.

IV. Conclusions

A GaInNAs p-i-n diode with suitable photoresponse to cover the 1310nm optical communication wavelength is demonstrated. Although its leakage current density has exceeded the limit for applications by a small margin, it is expected that with wafer growth optimization, the GaInNAs material could soon meet the leakage current density requirement whilst retaining its desirable photoresponse properties. Also, comparison of multiplication factors suggests $\alpha \sim \beta$ in this material, satisfying the compatibility consideration when combining with the $Al_{0.8}Ga_{0.2}As$ material to form SAM APDs. Therefore, GaInNAs is suitable for use as absorber material in APDs for 1310/1550 nm wavelength applications.

Acknowledgements

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INVESTIGATION OF SiO_2 ON AlGaAs PREPARED BY LIQUID PHASE DEPOSITION

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Abstract

The liquid phase deposition (LPD) was used to deposit silicon oxide (SiO_2) layer on AlGaAs near room temperature. The LPD method is not only simple but also can obtain the SiO_2 very economically. Both the aqueous solution of hydro-fluosilicic acid (H_2SiF_6) and boric acid (H_3BO_3) were used for the LPD solution. After rapid temperature annealing (RTA) at 300℃ for 1 min, the leakage current density is ~ 4.24×10^{-7} A/cm^2 at 1 MV/cm, and the interface trap density is ~ 1.7×10^{11} cm^{-2}eV^{-1} for the LPD-SiO_2 thickness of 29 nm.

I. Introduction

It has been reported that AlGaAs/InGaAs high-electron-mobility transistor (HEMT) has promising features and good performances. However, the device has some issues such as lower gate swing voltage and higher gate leakage current. These problems can be improved by using the metal-oxide-semiconductor (MOS) structure [1-2]. SiO_2 is the most widely used insulator in semiconductor because the processes and properties are reliable. There are many methods have been successfully grown SiO_2 films such as chemical vapor deposition (CVD), plasma-enhanced chemical vapor deposition (PECVD), electron cyclotron resonance chemical vapor deposition (ECR-CVD), and liquid phase deposition (LPD) [3-6]. Comparison with other methods, LPD process has many advantages which include low cost, low temperature, selective deposition, high deposition rate, and no photo energy or plasma source needed. The technique was used for the oxide layers on Si, GaAs, and glass [7-9]; however, there is no any report about LPD-SiO_2 on AlGaAs [10].

II. Experimental

The LPD system is shown in Fig. 1. The LPD-SiO_2 films were performed in a system which is equipped with a heater, a Teflon vessel, a controlled dripper, a stirrer, a stirrer controller, a wafer holder, and a water bath. The details of the LPD growth solution and the deposition flowchart were reported earlier in [8] and [11]. The wafers were prepared by metal-organic chemical vapor deposition (MOCVD) consisting of a 20 nm-thick GaAs capping layer, a n-type 1 μm-thick $Al_{0.2}Ga_{0.8}As$ layer with carrier concentration 1 x 10^{17} cm^{-3}, a 0.1 μm-thick GaAs layer, and a n^+-GaAs substrate. The wafers were cleaned by acetone, methanol, and DI water with ultrasonic vibration for 5 min, respectively. Before immersing in the LPD growth solution, the wafers put in the mixed solution ($NH_4OH:H_2O_2:H_2O$ = 3:1:50) to remove the GaAs capping layer for 5 s and blown-dry with nitrogen. Then, the wafers were immersed in the LPD growth solution at 40℃, and the SiO_2 was deposited on the AlGaAs. The LPD-SiO_2 process utilizes supersaturated hydro-fluosilicic acid aqueous solution (H_2SiF_6) as the source liquid. The H_2SiF_6 react with DI water to generate SiO_2 by using boric acid aqueous solution (H_3BO_3) as the deposition rate controller. The chemical reaction kinetics of LPD-SiO_2 deposition can be expressed by the following two equilibrium process:

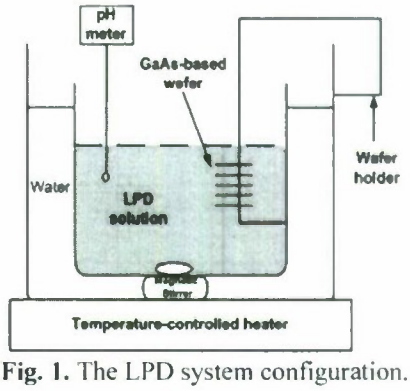


Fig. 1. The LPD system configuration.

$$H_2SiF_6 + 2H_2O \leftrightarrow 6HF + SiO_2 \downarrow \quad (1)$$

$$H_3BO_3 + 4HF \leftrightarrow BF_4^- + H_3O^+ + 2H_2O \quad (2)$$

In formula (1), hydrofluoric acid (HF) is separated by hydrofluosilicic acid with SiO_2 generation. After that, increased H_3BO_3 would consume HF and generate boron tetrafluoride ions (BF_4^-) as shown in formula (2). The decreased HF in the dipping solution will shift the formula (1) to the right side. Therefore, formula (1) shows that the DI water was added firstly to generate SiO_2 and promote the deposition of SiO_2 on AlGaAs. Then, the concentration of H_3BO_3 can be adjusted to control the oxide thickness and deposition rate. The better SiO_2 can be deposited on the GaAs while 0.4 M H_2SiF_6 and 0.01 M H_3BO_3 is mixed at 40℃ [8, 11]. Therefore, the concentrations of H_2SiF_6 and H_3BO_3 are fixed at 0.4 M and 0.01 M in the work.

The X-ray photoelectron spectroscopy (XPS) was used to investigate the elemental composition, chemical bonding structure analysis, and the depth profile of the oxide films. To characterize the electrical properties of the oxide layers, the MOS capacitors were fabricated on n-type AlGaAs using LPD-SiO_2 as insulators. The current-voltage (I-V) characteristics were measured by HP4156, and the high frequency (1 MHz) capacitance-voltage (C-V) was measured by HP4280.

III. Results and discussion

Figure 2 shows the deposition rate and the refractive index of LPD-SiO_2 on AlGaAs. The deposition rate and the refractive index of the SiO_2 were characterized by ellipsometer. The oxidation rate is ~ 70 nm/h at first hour. After 1h, the deposition rate descends mainly due to the decrease of the concentration of H_3BO_3. Before immersing in the deposition solution, the ammonia will make rich hydroxyl (OH) groups to formed GaO_x and AsO_x on the surface of the AlGaAs [12]. With the increased thickness of SiO_2, the effect of the GaO_x and AsO_x descends and results in the decrease of refractive index.

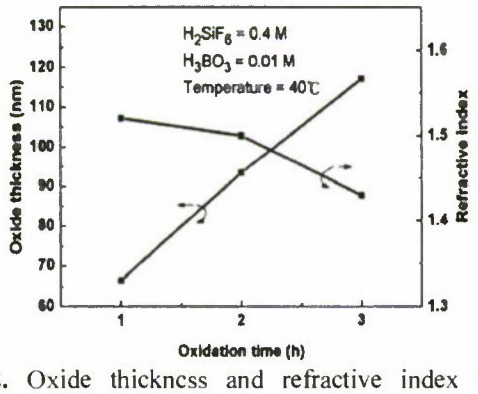
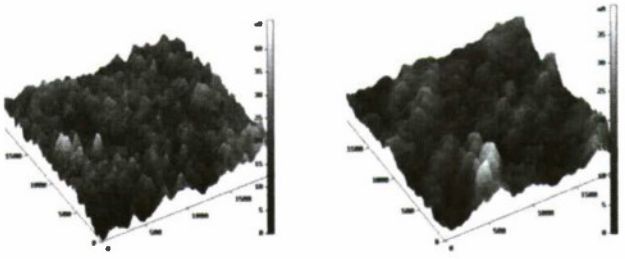


Fig. 2. Oxide thickness and refractive index versus oxidation time.

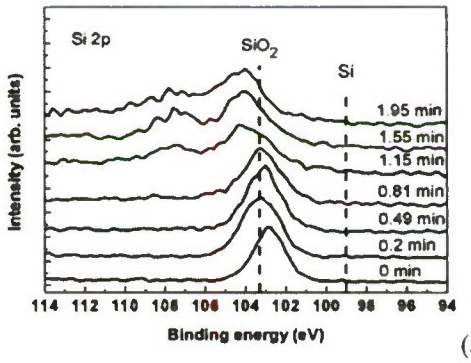
Figure 3 shows the AFM images of surface morphology. The surface before Rapid Thermal Annealing (RTA) is shown as Fig. 3(a), and the root mean square (rms) value is about 5.65. After RTA in the N_2 ambient at 350℃ for 1 min., the rms value is improved to 5.05 is shown as Figure 3(b).



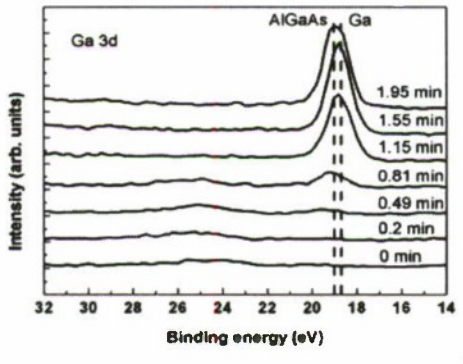
(a) (b)

Fig. 3. The AFM images of surface morphology (a) without (b) with RTA in the N_2 ambient at 350℃ for 1 min.

Figure 4(a) shows the XPS surface spectrum of the Si 2p core level by Al ion sputtering, detected at a take-off angle of 45°. The sputter etching is 50 nm/min. The main peak is the oxidized Si (103.4 eV, FWHM = 2.1 eV). We performed XPS analysis at Si 2p spectra to investigate the chemical states of the LPD-SiO_2 on AlGaAs between 0 to 1.95 min sputter etching. In Fig. 4(b), the Ga 3d core level reveals the existence of AlGaAs after 1.15 min sputter etching.



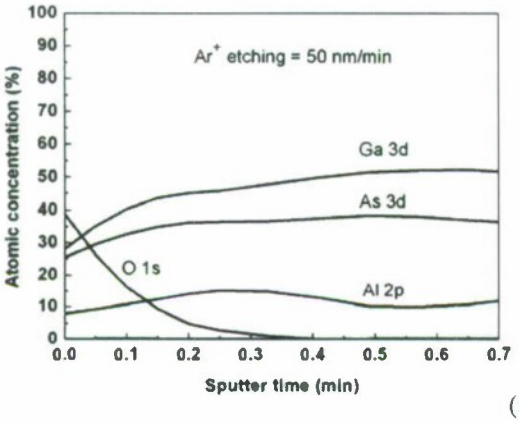
(a)



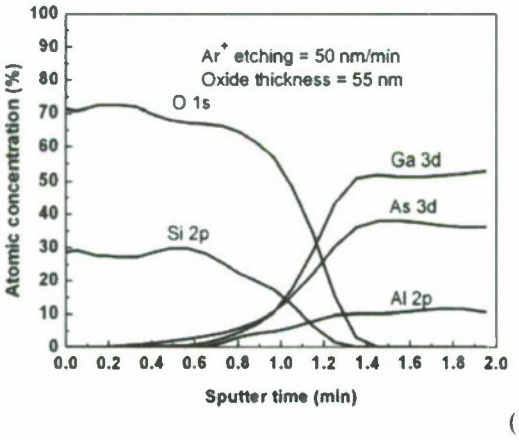
(b)

Fig. 4. (a) Si 2p and (b) Ga 3d of XPS surface spectrum of the as-deposited sample on AlGaAs.

Figures 5(a) and 5(b) show the XPS depth profile without and with LPD-SiO_2 film, respectively. The elements detected in overall depth of samples were O, Al, Ga, and As atoms except Si atoms as shown in Fig. 5(a). In Fig. 5(b), it shows a uniform of silicon and oxygen atoms near the SiO_2/AlGaAs interface. The SiO_2 thickness is about 55 nm. The XPS depth profile is confirmed according to the overlap point about 1.1 min sputter etching.



(a)



(b)

Fig. 5. The XPS depth profile (a) without and (b) with LPD-SiO_2 film.

Au and Au/Ge/Ni were used as top and bottom electrodes of the MOS capacitors, respectively, as shown in Fig. 6. Fig. 7 shows the leakage current density of the LPD-SiO_2 for the MOS capacitors with and without RTA. The leakage current density is approximately 1.21×10^{-6} A/cm^2 at 1 MV/cm. After RTA in the N_2 ambient at 300℃ for 1 min, the leakage current density can be improved to 4.24×10^{-7} A/cm^2 at 1 MV/cm. Fig. 8 shows the experimental and ideal C-V results after RTA in the N_2 ambient at 300℃ for 1 min. In order to confirm interface trap density (D_{it}), Terman method was performed. The D_{it} is ~ 1.7×10^{11} cm^{-2}eV^{-1} for the LPD-SiO_2 thickness of 29 nm on AlGaAs. The C_{hf} and C_{ox} denote the capacitance and the oxide capacitance at 1 MHz, respectively.

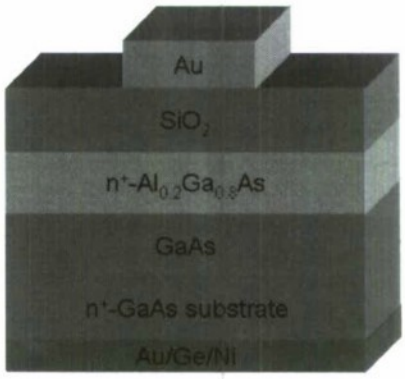


Fig. 6. A schematic structure of the MOS capacitor.

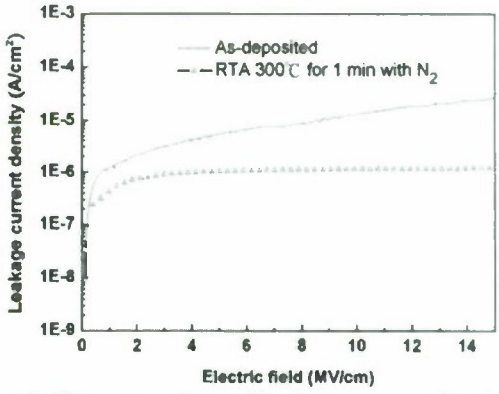


Fig. 7. The comparison of leakage current density for the MOS capacitors with and without RTA.

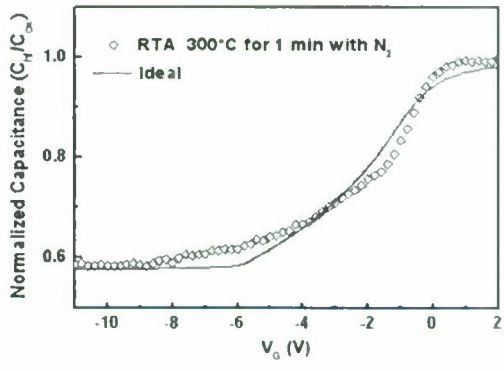


Fig. 8. The experimental and ideal C-V results of the MOS capacitors with RTA.

IV. Conclusion

The LPD-SiO_2 deposited on AlGaAs substrate has been demonstrated and characterized. The electrical properties of the LPD-SiO_2 can be improved by RTA. After RTA at 300℃ for 1 min, the leakage current density is ~ 4.24×10^{-7} A/cm^2 at 1 MV/cm, and the D_{it} is ~ 1.7×10^{11} cm^{-2} cV^{-1} for the LPD-SiO_2 thickness of 29 nm.

Acknowledgements

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COMPARISON OF THE PHOTOLUMINESCENCE SPECTRA BETWEEN QUANTUM WELL STRUCTURE AND QUANTUM DOTS STRUCTURE

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Abstract— We have compared the photoluminescence (PL) spectra of InAs/InGaAsP/InP quantum dots (QD) structures with that of InGaAs/InP quantum well (QW) structures by changing the incident angle for TE polarized excitation light. From the results, we have found the shift of the PL peak wavelength is different between QD and QW. Then, we have measured the change in the FWHM of the PL spectrum against the excitation light intensity. The increment rate of the FWHM for QD is larger than that for QW. From the above, we have supposed each QD couples electrically to form a continuous band structure and the quantum levels broaden, due to adjacent QD whose size are variant. It means the band filling effect for the bulk sample occurs in QD samples.

Keywords-component ; photoluminescence, Quantum-well, Quantum-dots

I. Introduction

The quantum structures are influential to improve the device characteristics especially of laser diodes.[1-5] We have already reported the photoluminescence (PL) spectra of quantum well structures by changing the polarization of the excitation light.[6-8] We have found the shift of the PL peak wavelength is different between the TE mode and TM mode excitation. From these results, we have estimated the strain factor of samples and the degeneracy of the quantum levels between the heavy hole band and the light hole band.[8] Here we measured the PL spectra behavior of quantum dots (QD) structures.

II. Samples and Experimental set-up

The experimental set-up is shown in Fig.1. The PL spectra measurement has been performed at room temperatures by using the YAG laser [CrystaLaser, IRCL-1W-1064] with 1064nm of the wavelength and the emitting power of 1W, the grating-type spectrometer [Jobin Yvon, Triax 320] and the PbS photodiode. The polarization of the excitation light is the TE mode. We observed the behavior of the PL spectra changing the excitation light intensity. To obtain the gradual change in the excitation light intensity, the incident angle of the excitation light was changed from 30° to 70°. As the polarization direction of TE mode is always parallel to the surface of samples, the excitation condition is the same for any incident angle.

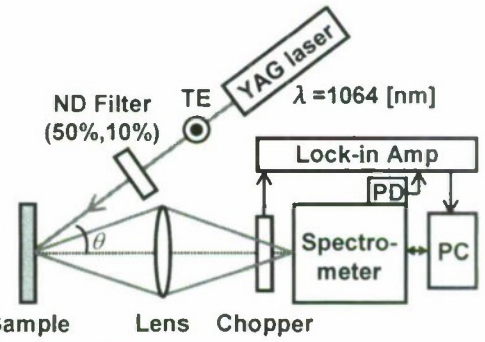

Fig.1 Experimental set-up

We have measured the absorption coefficient for 1064nm wavelength of these samples to calculate how much power of the excitation light is absorbed in the sample for each incident angle. The absorption coefficient of QW sample#1 and #2 is 5×10^4/cm, that of the other QW samples is 3×10^5/cm, and that of QD samples are 2×10^6/cm.

The schematic structure of QD samples is shown in Fig.2. We have prepared 5 samples as shown in Table 1. All layers are non-doped n type. The size of QD is mostly oval with 30nm × 40nm. The packing density of these samples is about 40%. From the above, dot density of these samples is 4.2×10^{10}/cm^2. The shape of QD-samples is a sector with 2.5cm in radius.

We have prepared QW samples as the comparison samples. The schematic structure of QW samples is shown in Fig 3, and the parameters of them are shown in Table 2. All layers

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of these samples are non-doped n types. The size of QW-samples #1 is 7mm×3mm, #4 is 2cm×2cm, and the shape of the other QW-samples is sector with 2.5cm in radius.

The parameter of the lattice mismatch is denoted as $\Delta a/a$; a is the lattice constant of the substrate and Δa is the difference in the lattice constant between the substrate and InAs for QD or InGaAs for QW. The negative $\Delta a/a$ corresponds to the expansion strain and the positive value corresponds to the compression strain.

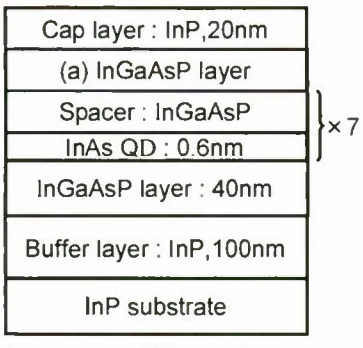

Fig.2 Schematic structure of QD samples

Table 1 Parameters of QD samples

	(a)	Spacer	$\Delta a/a$ [%]
QD-Sample #1	20nm	20nm	0
QD-Sample #2			-0.4
QD-Sample #3			-0.8
QD-Sample #4	10nm	30nm	0
QD-Sample #5			-0.4

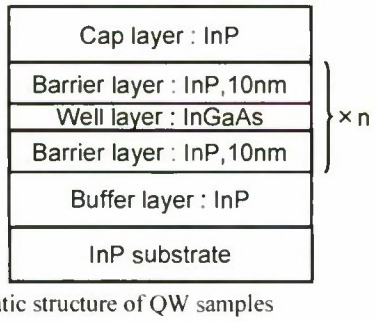

Fig.3 Schematic structure of QW samples

Table 2 Parameters of QW samples

	Cap	Well	Buffer	n	$\Delta a/a$ [%]
QW-Sample #1	10nm	15nm	500nm	20	0
QW-Sample #2					0.2
QW-Sample #3	40nm	6nm	90nm	6	1.6
QW-Sample #4					-1.56
QW-Sample #5			190nm		-1.24

III. Results and Discussions

Fig. 4(a) shows the change in the PL peak wavelength against the excitation light intensity for QD-Sample #3, and (b) shows that for QW-Sample #5. We have calculated the absorbed light power for each incident angle considering the multi reflection from the front and rear surfaces. And we normalized absorption light power dividing the absorbed light power at the each incident angle by the absorbed light power at the incident angle of 0°.

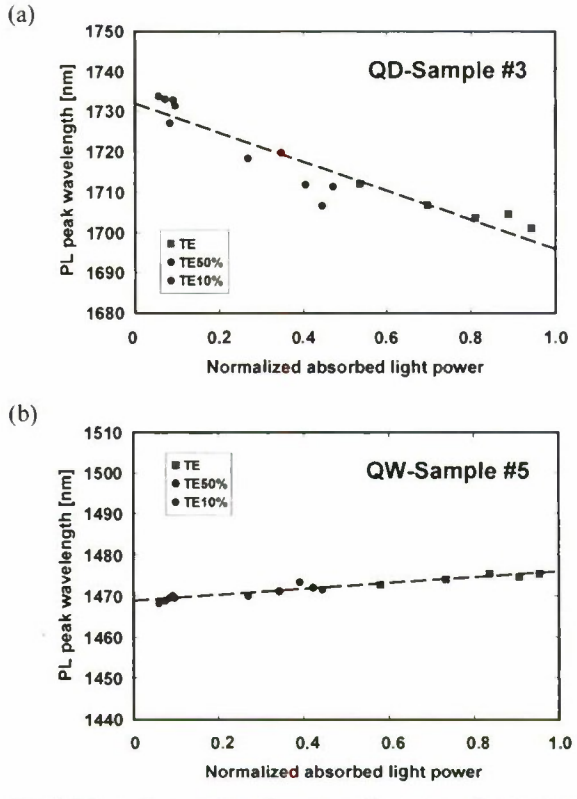

Fig.4 PL peak wavelength versus the normalized absorbed light power of excitation light. (a) is for QD-Sample #3 and (b) is for QW-Sample #5.

From these figures, for QD, it is found the PL peak wavelength shifts to the shorter wavelength corresponding to the increase in the excitation light intensity. On the other hand, PL peak wavelength of QW shifts to the longer wavelength.

We have assumed temperature rise of QW-sample caused this tendency. As the excitation light intensity increases in the PL measurement, the sample temperature increases. This means the PL peak wavelength moves to the longer wavelength. Because, the lattice constant becomes longer due to the thermal expansion, and the band gap is narrower.

This is sure to occur for QW samples. However, it is different for QD samples. Thus, we have assumed a certain effect may overcome the effect due to the temperature rise in QD samples.

Then, we measured the change in the FWHM of the PL spectrum against the excitation light intensity, and Fig. 5(a) shows the result of QD-Sample #3, and (b) shows that for QW-Sample #5.

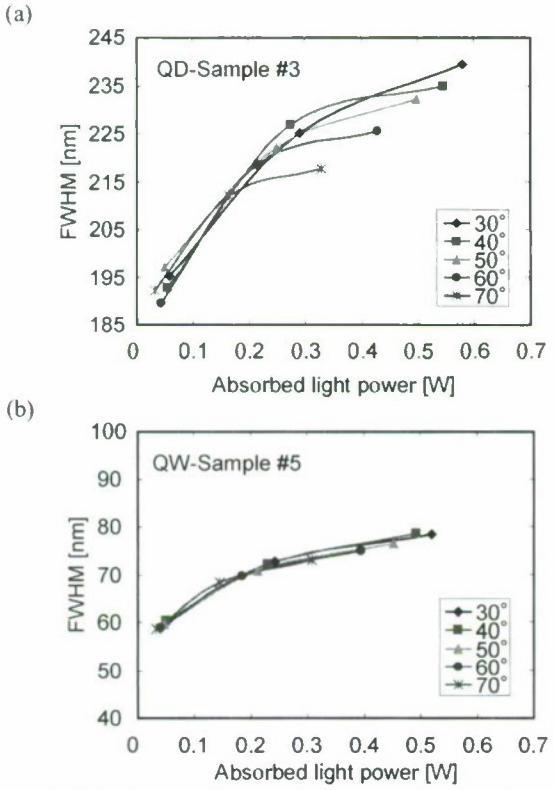

Fig.5 FWHM of the PL spectrum versus absorbed light power of excitation light. (a) is for QD-Sample #3 and (b) is for QW-Sample #5.

Both results for the QD sample and for the QW sample show the FWHM increases with the increase in the excitation light intensity. However, the FWHM and the increment rate are larger for the QD sample than for the QW sample.

We have assumed the variation in the size of the QD has influenced this tendency. The packing density of this sample is about 40～50%, and each QD couples electrically to form a continuous band structure. We suppose the quantum level broadens due to the variation of the QD sizes. It means the band-filling effect similar to the bulk sample occurs in QD samples. The fact that PL peak wavelength moves to the shorter wavelength, FWHM of PL spectra is large for QD samples and it increases largely with the increase in the excitation intensity seems to correspond to this effect. The energy distribution where the excited electrons occupy broadens to the high level with the increase of the excitation intensity due to the band-filling effect in the QD. That is why PL peak wavelength moves to the shorter wavelength. The result of the FWHM in QD shows the range the electrons are distributed.

IV. Conclusion

We have observed the PL spectra of QD structures and QW structures. The peak shifts of the PL spectrum for TE excitation are observed by changing the incident angle and intensity of the excitation light. By comparing the results of QD with that of QW, it is found the PL peak wavelength of QW shifts to the longer wavelength due to temperature rise of QW sample, but the PL peak wavelength of QD shifts to the shorter wavelength corresponding to the increase in the excitation light intensity. We measured the change in the FWHM of the PL spectrum against the excitation light intensity. We have found the FWHM and the increment rate are larger for the QD sample than that for the QW sample. From the above, we have supposed each QD couples electrically to form a continuous band structure and the quantum levels broaden due to the variation in the QD sizes. Therefore it is expected the band filling effect occurs in the QD. That is why PL peak wavelength moves to the shorter wavelength, and the FWHM and the increment rate are large.

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Synthesis of cubic-GaN nanoparticles using the Na flux method

- A novel use for the ultra-high pressure apparatus -

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Abstract

Nano-scale cubic-GaN particles were successfully synthesized using the Na flux method under about 500 atm with a belt-type ultra-high pressure apparatus. High pressure nitrogen gas of about 500 atm was sealed in the ultra-high pressure apparatus, which enabled the dissolution of pressurized nitrogen gas into a Ga-Na melt at 500°C without a compressor. In contrast, the conventional Na flux method is carried out under a pressure of 150 atm, the maximum pressure of a nitrogen gas cylinder. A characteristic feature of the process used herein is that the high-pressure reaction gas is dissolved into a flux within the ultra-high pressure apparatus. The c-GaN nanoparticles obtained by this method show excellent crystallinity and a low mixing ratio of hexagonal-GaN, and thus the method solves two common problems in the synthesis of c-GaN.

I. Introduction

Recently, GaN nanoparticles have been studied for their possible application to fluorescent materials and electronic devices that use quantum size effects.[1-3] The synthesis of not only the hexagonal-GaN (h-GaN) but also cubic-GaN (c-GaN) nanoparticles has already been studied.[4,5] However, the commingling of h-GaN with c-GaN particles and the low crystallinity of c-GaN has been unavoidable, because the c-GaN is easily structured at a lower temperature than is h-GaN.

It has been established that the Na flux method is advantageous for realizing high crystallinity in the synthesis of h-GaN. In this method, GaN single crystals can be obtained in a Ga-Na mixed metal melt by dissolving pressurized nitrogen gas of about 50 atm into the melt at 800 °C.[6-9] If a seed GaN crystal is introduced in this method, a large GaN single crystal with a size of inches can be obtained and applied to a single crystal substrate for electronic devices.[10-19] Recently, Yamane et al. reported that c-GaN can also be synthesized together with the h-GaN by the Na flux method by lowering the reaction temperature to 570 °C.[20,21] In addition, K flux has been reported to be a useful flux for the synthesis of c-GaN, enabling the synthesis of c-GaN particles with a size of several tens of microns at a relatively high temperature of 750 °C, although the mixing ratio of h-GaN was not mentioned in that study.[22]

A major problem in the synthesis of c-GaN by the Na flux method is the high mixing ratio of h-GaN. Although lowering the temperature is a favorable method for achieving a high cubic/hexagonal ratio, synthesis at a low temperature requires high nitrogen pressure because of poor nitrogen dissolution into low temperature melt, and 570°C is the lowest synthesis temperature that can be used with a conventional apparatus for the Na flux method. We previously reported the dissolution mechanism of nitrogen gas into the Ga-Na melt, which led to a method for calculating the required nitrogen pressure. The nitrogen pressure needed at 500 °C turned out to be several hundred atm.

In this research, we designed a system that can easily supply high pressure nitrogen gas of several hundred atm into a Ga-Na melt by modifying a belt-type ultra-high pressure apparatus for low temperature synthesis of c-GaN. As a result, cubic-GaN nanoparticles with low h-GaN content could be obtained at 500 atm.

In this research, high pressure reaction gas was used for synthesizing crystals inside a ultra-high pressure

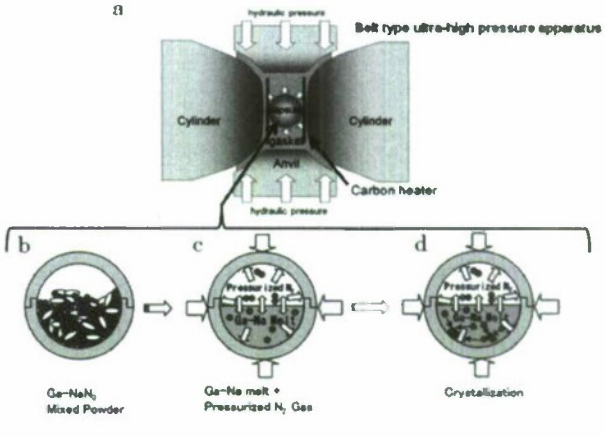

Fig.1 (a) A schematic illustration of the experimental setup and (b,c,d) the procedures of the reaction to synthesize GaN particles. (b) Sodium azide and metal-Ga are mixed in a Ni spherical capsule. (c) Sodium azide is exploded in a Ni capsule which is set in a belt-type ultra-high pressure apparatus. (d) GaN particles with a size of a few to 600 nanometers are synthesized in a Ga-Na melt with dissolution of high-pressure nitrogen gas. The concentration of nitrogen in the melt is balanced with the pressure of nitrogen gas.

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apparatus. This method that uses high-pressure gas as source material goes ahead of synthesizing new materials and will be applied under further higher pressure of GPa level.

II. Experimental

Figure 1 provides a schematic of the experimental procedures. In a nitrogen-purged glove-box, a metal-Ga powder and sodium azide (NaN_3) powder (Ga : Na = 1 : 3 (mol)) were mixed and weighed so that the total weight of reagents was 500 mg, and then transferred into a spherical nickel capsule with an outer diameter of 7 mm, as shown in Fig.1b. The Ni capsule was set in a belt-type ultra-high pressure apparatus (KOBELCO) with a gasket which functions as a pressure medium, as shown in Fig.1b. After pressurizing the reactive portion up to 1 GPa, the capsule was heated to 500 °C to 700 °C. The reaction temperature was varied according to the aims of the study. The spherical capsule was strong enough to maintain its shape under isotropic pressure of 1 GPa. Figure 1c shows the inside of the capsule after decomposition of NaN_3, resulting in the formation of a Ga-Na melt and high pressure nitrogen gas. Nitrogen gas is sealed in the Ni capsule because the external pressure is considerably higher than the pressure inside the capsule. Successively, GaN particles were formed during a synthesis duration of 2 hrs in the Ga-Na melt with dissolution of nitrogen gas as shown in Fig.1d. After the reaction, the temperature was cooled down to room temperature, and then the capsule was resealed. The GaN powder formed in the melt was collected after breaking the capsule and pouring water over the capsule to flush out the Na metal. During this flushing procedure, careful handling is needed because the Na metal is highly flammable and can ignite.

III. Results and Discussion

Figure 2 indicates the XRD profiles obtained at various reaction temperatures. The cubic/hexagonal ratio was increased as the reaction temperature was lowered. The specific main peaks attributable to c-GaN and h-GaN were c-(200) and h-(100), h-(101), h-(102) and h-(103),

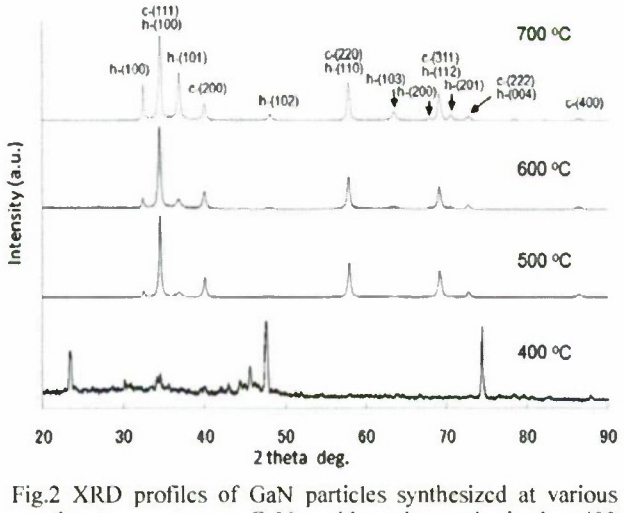

Fig.2 XRD profiles of GaN particles synthesized at various reaction temperatures. GaN could not be synthesized at 400 °C because of the phase splitting of the Ga-Na melt.

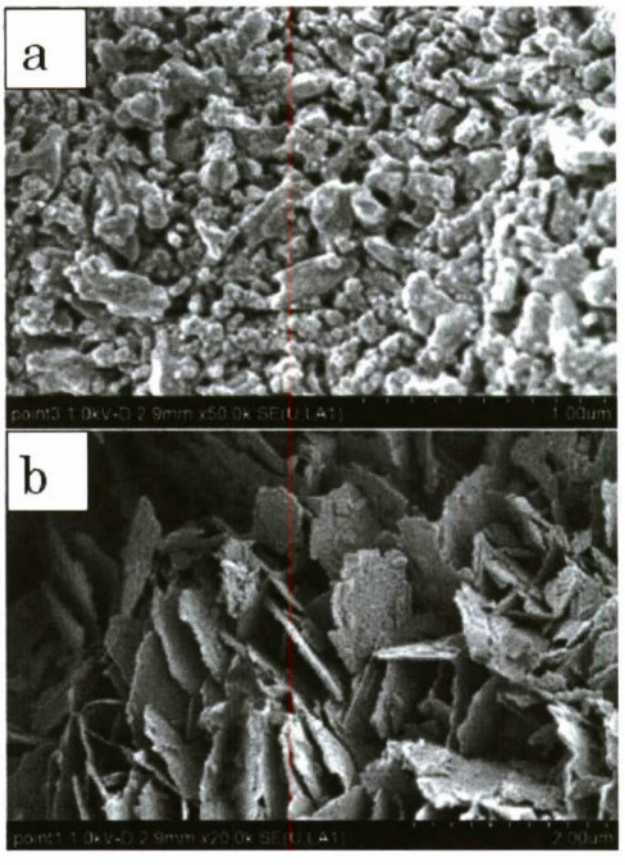

Fig.3 SEM photographs of c-GaN particles. (a) Major component of obtained particles. (b) Flaky crystals of GaN which were synthesized with c-GaN nano particles, which are localized at specific area.

respectively. At 500 °C, the peaks of c-GaN overwhelmed those of h-GaN. GaN could not be synthesized at 400 °C because the metal Ga and Na were not mixed and existed separately. The peaks found at 400 °C were probably intermetallic compounds. In addition to the high ratio of c-GaN, a characteristic feature in Fig.2 was the good crystallinity of c-GaN particles. As compared with the previously reported data on the synthesis of c-GaN by other synthesis methods, the XRD peaks in the present experiments were quite sharp. The high crystallinity, which is one of the advantages of the Na flux method, was maintained even at an extremely low synthesis temperature.

Figure 3 shows the scanning electron microscope (SEM) images synthesized at 500 °C. Although dispersed nanoparticles with a size of a few to 6 hundred nanometers were confirmed in most of the areas examined, as shown in Fig. 3a, some flaky crystals with a thickness of several tens of nanometers were also found. It is known that lowering the temperature and increasing the nitrogen pressure in the Na flux method accelerates the nucleation frequency, resulting in a reduction of the crystal size of grown GaN.[23] Although, based on the synthesis conditions of this research, it is reasonable to speculate that atomization occurred, the reason for the generation of flaky crystals could not be specified and warrants further study.

Figure 4 shows the results of the cathode luminescence (CL) measurement. The difference in CL

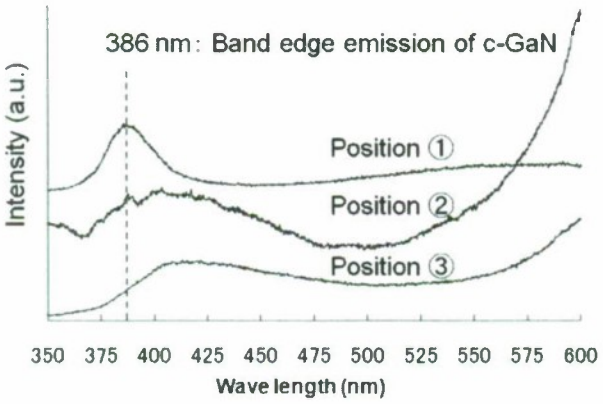

Fig.4 Cathode luminescence profiles of c-GaN particles synthesized at 500 °C. Some types of profiles are found: ① Clear band-edge emission is observed. ② Band-edge emission exists with broadened peak. ③ Only broadened peak is found around 410 nm.

profiles among the measured positions was remarkable. Typical CL profiles could be classified into three patterns as indicated in the figure: ① A clearly confirmed band-edge emission at 386 nm. ② A clearly confirmed band-edge emission at 386 nm plus a broadened peak around 410 nm. ③ A broadened peak at around 410 nm, but no band-edge emission. Although no clear reason for these differences was apparent, they might be attributable to the successive changes in the Ga/Na ratio that occurred during the synthesis of GaN, which could not be avoided because of consumption of Ga might cause defects and change the property of the obtained crystals.

The merits of this research were not only the successful synthesis of c-GaN nanoparticles but also the development of a new synthesis process employing an ultra-high pressure apparatus. The introduction of a spherical capsule which can seal a high-pressure gas source enabled flux growth by a high-pressure gas source. In particular, the evaporation of the Na element, the prevention of oxidization and the further pressurization of nitrogen gas were made easier by the Na flux method. In the Na flux method, dissolving a nitrogen gas in a Na-X melt (where X is an additional metal element added to the Na flux) enables the formation of nitride of the X element, because the Na works as a catalyst in the dissolution of nitrogen, even though the Na does not form sodium nitride at high temperature.[24,25] A belt-type ultra-high pressure apparatus can pressurize to about 10 GPa, which means that it will be possible to further pressurize the nitrogen gas source in this method by developing capsules with strong pressure tolerance. We will attempt to form various nitride compounds with various structures by using this method under Gpa-level nitrogen pressure.

IV. Conclusions

1. A method of flux growth using a high-pressure gas source with a belt-type ultra-high pressure apparatus was developed.
2. Cubic-GaN nanoparticles were successfully synthesized at 500 °C under 500 atm.
3. The mixing of h-GaN into c-GaN was minimal.
4. C-GaN particles synthesized by the Na flux method showed a band-edge emission at 386 nm in the CL measurement.

Acknowledgement

The authors would like to thank O. Tsuda, a researcher of the National Institute for Materials Science (NIMS), for the measurement of cathode luminescence.

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ALN BULK SINGLE CRYSTAL GROWTH ON SIC AND ALN SUBSTRATES BY SUBLIMATION METHOD

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Aluminum nitride (AlN) bulk single crystals up to 45 mm in diameter and 10 mm in thickness have been successfully grown on 6H-SiC (0001) substrates by the sublimation method. Moreover, high growth rate of 200μm/h has been achieved by high temperature homo-epitaxial AlN growth on AlN(0001) substrate. The Raman spectrum indicates that the polytype of the grown AlN single crystals is a Wurtzite-2H type structure, and the crystals do not include any impurity phases. In both the hetero- and homo-epitaxial AlN bulk single crystal growth, the quality at the top of the crystal improves as the crystal thickness increases along the <0001> direction during the growth: low etch pit density 7×10^4 cm^{-2} and 1×10^4 cm^{-2} have been achieved at a thickness of 8 mm and 2 mm in the hetero- and homo-epitaxial growth, respectively.

I. Introduction

Aluminum nitride (AlN) is a most promising substrate material for III-V nitrides based UV-optoelectronic and high-power high-frequency devises because this nitride has wide direct band gap 6.2 eV, high thermal conductivity, high thermal stability and small lattice mismatch for III-V nitrides. AlN bulk crystals have been grown by sublimation growth using graphite [1,2], boron nitride(BN) [3], tantalum carbide(TaC) [4-7], tungsten(W) [5,7-10] crucibles. Recently, TaC and W crucibles have been well used for the growth because these crucibles have high corrosion resistance to the gas sublimed from the AlN source. Concerning seeding growth, SiC(0001) and AlN are typically used as the seed crystal. However, both crystal size and quality of the AlN crystals grown by sublimation method are not sufficient for substrate of the III-V nitrides based devise.

In this study, we report hetero- and homo-epitaxial AlN bulk single crystal growth by sublimation method on SiC and AlN substrates, respectively.: (a) large and thick (up to 45 mm in diameters, 10 mm in thickness) AlN bulk single crystal growth on SiC(0001) substrate (b)high speed (200μm/h) AlN bulk single crystal growth on AlN(0001) substrate.

II. Experimental

AlN bulk single crystals were grown by sublimation method in N_2 atmosphere using RF-heated furnace as shown in Fig.1. A double-crucible (Inner crucible: TaC, Outer crucible: graphite) covered with graphite insulator was placed in the furnace. TaC crucibles were obtained by pre-carbonized treatments of Ta crucibles using graphite powder at 1900-2100 °C with Ar-gas flowing. A specially made 6H-SiC(0001) (AlN(0001)) substrate was held on a TaC crucible cap. AlN sources were prepared from AlN powder by sintering at 1900 °C in a N_2 atmosphere. In the growth, the temperature of the graphite crucible cap was controlled by an upper

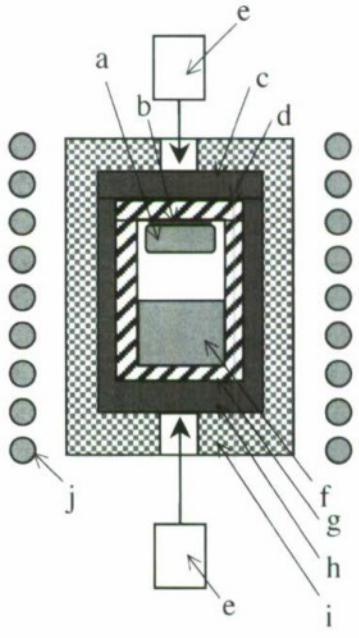

Fig. 1 Schematic illustration of AlN crystal growth equipment: **a**. AlN single crystal, **b**.SiC or AlN substrate, **c**. graphite cap, **d**. TaC cap, **e**. pyrometers, **f**. AlN source, **g**.TaC crucible, **h**.graphite crucible, **i**.graphite insulation, **j**. RF coil.

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pyrometer to keep in the rage of 1700-2000 °C and 2100 °C for the growth on SiC and AlN, respectively. N_2 pressure in the furnace was kept at 100-700 torr during the growth. The crystal qualities were evaluated by Raman scattering spectroscopy, etch pit observation and x-ray rocking curve (XRC) measurements using the AlN(0001) plate-like polished specimens with ~700μm-thick, which have been sliced from top and bottom parts of an AlN crystal.

III. Results and discussion

A. AlN bulk single crystal growth on SiC substrates

Figure 2 shows an AlN bulk single crystal with 45mm in diameter and 10 mm in thickness grown on SiC(0001). The crystals have been grown with growth rate about 30-50 μm/h. The grown crystal

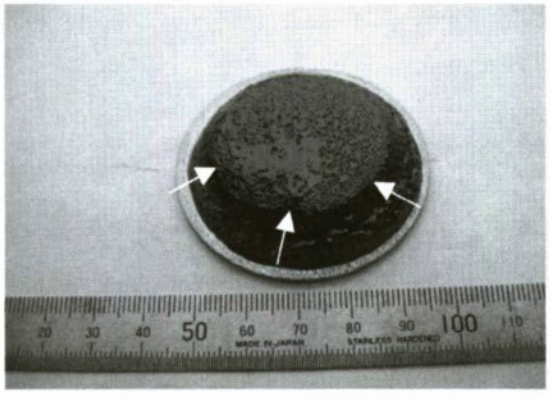

Fig. 2 Photograph of an AlN bulk single crystal with 45 mm in diameter and 10 mm in thickness grown on a SiC(0001) substrate. The white arrows indicate (10-1N) facets.

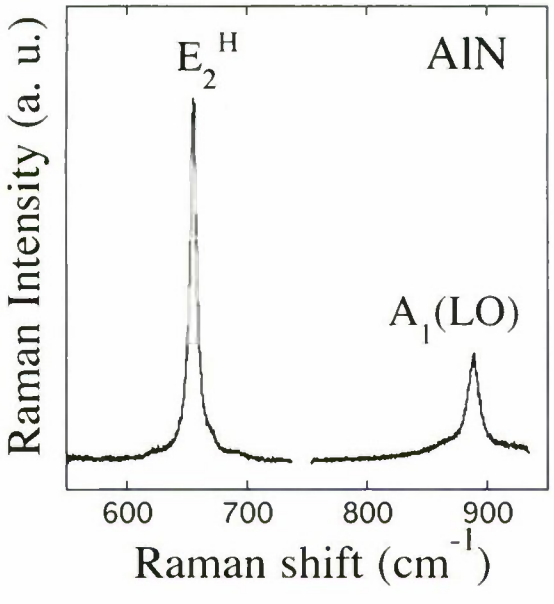

Fig. 3 Raman spectrum of a grown AlN single crystal, which shows Wurtzite-2H type structure. No impurity phase Raman mode was detected in the specimens.

is enlarged from 35mm to 45mm in diameter during the growth in spite of a short growth length of about 7 mm in height. Large (10-1N) facets with six-fold symmetry were observed clearly on the surface of lateral side of the crystals, which implies that the AlN single crystals grow along <0001> direction.

The Raman spectrum indicates sharp peaks of E_2^H and A_1(LO) modes derived from 2H polytype of AlN, and shows no polytype inclusion in the crystal as shown in Fig. 3. Figure 4 exhibits a cross-section transmitted optical microscopy image of the grown AlN single crystal. Although a large number of cracks were generated near the AlN/SiC interface, only a few cracks were observed near the top of the crystal. The decrease in the crack with increasing thickness implies that the stress arising at interface between SiC and AlN relaxes gradually during the growth.

The etch pit density (EPD) and the full width at half maximum (FWHM) of XRC 0002 for two typical AlN(0001) specimens cut from (i)an AlN crystal near the SiC substrate and from (ii) the top of an AlN crystal are summarized in Table 1.

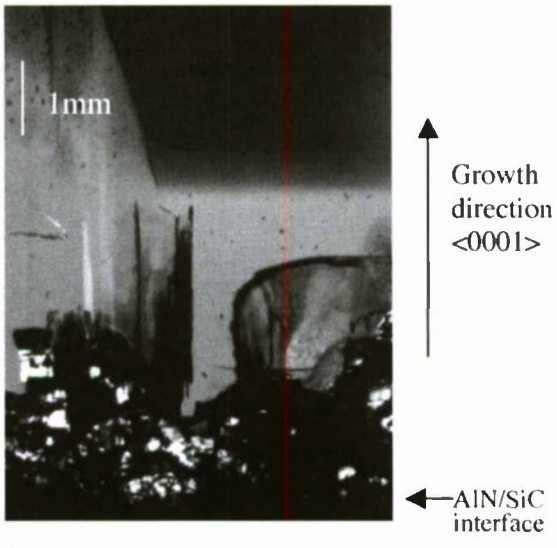

Fig. 4 Cross-section transmitted optical microscopy image of the AlN layer grown on 6H-SiC substrate. Extremely many cracks are observed at near AlN/SiC interface. These cracks occur due to strain relaxation arising from the lattice mismatch between AlN and SiC.

Table 1 The EPD and FWHM of 0002 XRC for typical two AlN specimens cut from (i) an AlN crystal near the SiC substrate and from (ii) the top of an grown AlN crystal, in the hetero-epitaxial AlN bulk single crystal. The data indicate that the crystal quality of the latter is higher than that of the former.

	EPD	FWHM of 0002 XRC
near SiC substrate	$>10^6$ cm^{-2}	183 arcsec
top	10^4 -10^5 cm^{-2}	58 arcsec

Hetero-epitaxial AlN growth on 6H-SiC(0001) with increased crystal thickness along <0001> direction is quite effective in improvement of the crystal quality based on the following two experimental results: (i)the etch pit density for the AlN specimen taken from the crystal near the AlN/SiC interface is several 100 times as high as that taken from the top of the crystal, indicating that low etch pit density (7.4×10^4 cm^{-2}) is achieved at 8 mm in thickness as shown in Fig. 5. (ii)the AlN specimen taken from the crystal near the interface tend to show the rocking curve with wider FWHM and split peaks in comparison with that taken from top of the crystal, which is derived from the stress arising at interface between SiC and AlN. A specially made freestanding AlN substrate with 35 mm in diameter, which was produced through cutting from top of the grown AlN crystal and then polishing, is shown in Fig. 6.

B. AlN bulk single crystal growth on AlN substrates

Figure 7 shows an AlN bulk single crystal with 35mm in diameter grown on AlN(0001). The crystal has been successfully grown with 2mm thick for 10 hours with high growth rate about 200 μm/h, which is 4-6 times as high as that of the hetero-epitaxial AlN crystal growth on SiC(0001). In contrast to the AlN single crystal grown on SiC, no large (10-1N) facet was observed on the surface of lateral side of the crystal. The Raman spectrum indicates sharp peaks of E_2^H and A_1(LO) modes of 2H polytype of AlN, and shows no polytype inclusion in the crystal.

The EPD and FWHM of XRC 0002 for two typical AlN(0001) specimens which were cut from (i)a grown AlN single crystal and from (ii)the AlN substrate are summarized in Table 2.

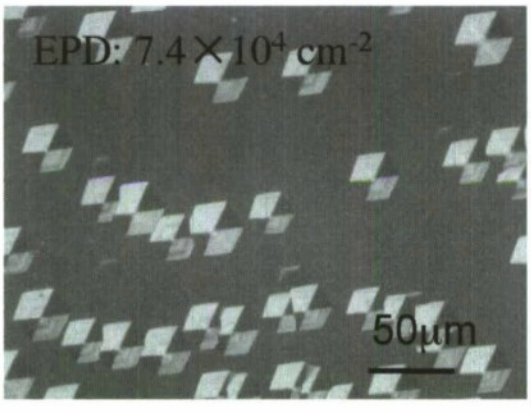

Fig. 5 Micrograph of etch pit by molten alkali treatment appeared on the AlN(0001) specimen taken from the top of the AlN crystal grown on SiC(0001). The etch pit density of the specimen taken from the AlN crystal near AlN/SiC interface is several 100 times as high as that taken from the top of the crystal.

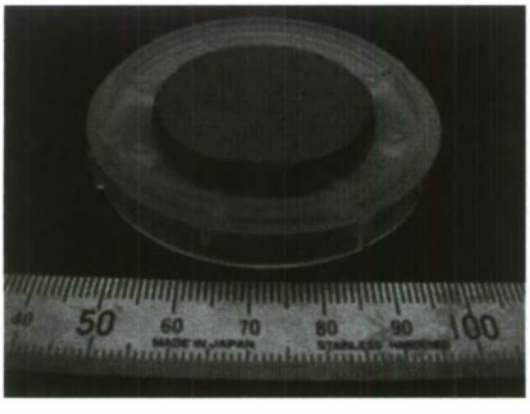

Fig. 6 Freestanding 35 mm diameter AlN(0001) substrate produced from an AlN bulk single crystal grown on SiC(0001).

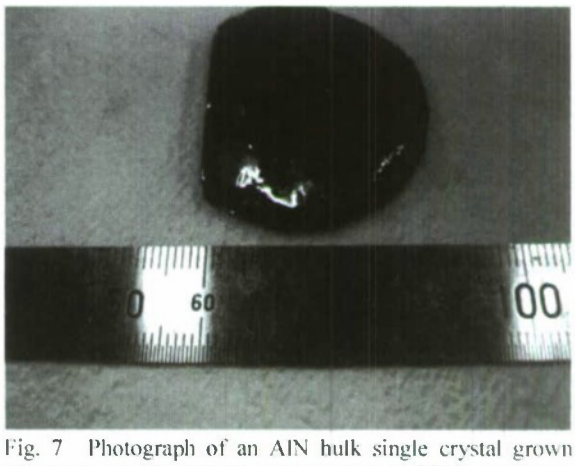

Fig. 7 Photograph of an AlN bulk single crystal grown with high growth rate 200 μm/h on an AlN(0001) substrate.

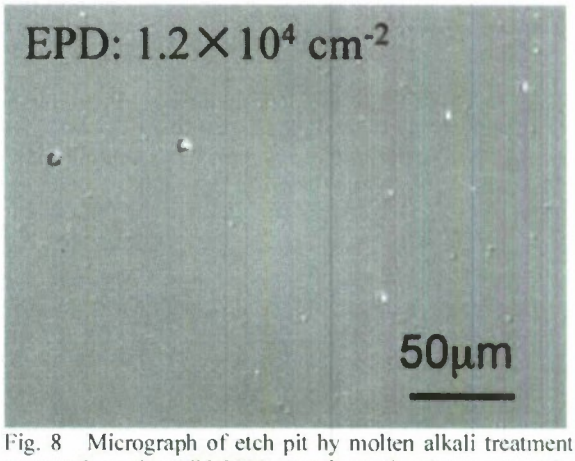

Fig. 8 Micrograph of etch pit by molten alkali treatment appeared on the AlN(0001) specimen for the grown AlN crystal. The etch pit density of the specimen for the substrate is 10 times as high as that for the grown crystal.

Table 2 The EPD and FWHM of 0002 XRC for typical AlN specimens cut from (i) an AlN substrate (ii) a grown AlN crystal, in the homo-epitaxial AlN bulk single crystal. The data indicate that the crystal quality of the latter is higher than that of the former.

	EPD	FWHM of 0002 XRC
AlN substrate	10^5 -10^6 cm^{-2}	440 arcsec
grown AlN crystal	10^4 -10^5 cm^{-2}	202 arcsec

The crystal quality of the grown AlN crystal tends to be higher than that of the substrate from following two results: (i)the etch pit density of the specimen taken from the AlN substrate is approximately10 times as high as that taken from the grown AlN crystal, indicating that low etch pit density (1.2×10^4 cm^{-2}) is achieved at 2 mm in thickness as shown in Fig. 8. (ii)the specimens for the grown AlN crystal tend to show the rocking curve with smaller FWHM in comparison with that for the grown AlN crystal.

IV. Conclusion

We have succeeded in enlargement and high seed AlN single crystal growth on SiC(0001) and AlN(0001) substrate, respectively. In both the hetero- and homo-epitaxial AlN bulk single crystal growth, etch pit density and x-ray rocking curve for the grown AlN single crystals suggest that the crystal quality at the top of the grown AlN crystal tends to be improved when crystal thickness increases along <0001> direction during the growth.

Acknowledgements

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CARBON-DOPED $In_xGa_{1-x}As_{1-y}Sb_y$ ON InP GROWN BY METAL-ORGANIC CHEMICAL VAPOR DEPOSITION

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Abstract

This paper reports metal-organic chemical vapor deposition (MOCVD) growth of undoped and C-doped $In_xGa_{1-x}As_{1-y}Sb_y$ on (001) InP substrates for the first time. We investigated the relationship between the $In_xGa_{1-x}As_{1-y}Sb_y$ alloy composition and molar flow ratio of group-III and group-V precursors in both undoped and C-doped $In_xGa_{1-x}As_{1-y}Sb_y$ and found a characteristic etching effect caused by the decomposition of carbon tetrabromide (CBr_4). C-doped InGaAsSb films with high hole concentrations of over 2×10^{19} cm^{-3} were obtained for the In composition of less or equal to 0.10. The effect of hydrogen passivation of C-acceptors in C-doped InGaAsSb was negligibly small and similar to that in C-doped GaAsSb.

I. INTRODUCTION

GaAsSb/InP double hetero-junction bipolar transistors (DHBTs) have been attracting a great deal of interest over the last decade because the type-II band alignment at the base-collector (B-C) hetero-interface eliminates the current blocking effect and is beneficial for integrated circuits requiring both ultra-high-speed performance and high breakdown voltages [1, 2]. Recently, the device performance of Sb-based DHBTs has been improved by using a GaAsSb/InGaAsSb or AlGaAsSb graded base [3, 4], and the electron pile-up at the emitter-base (E-B) junction has been suppressed by using an As-rich GaAsSb base and/or wide-bandgap emitters [5, 6]. The use of an InGaAsSb base layer is advantageous for lowing the turn-on voltage of DHBTs because both the type-II band offset between the emitter and the base and the band gap of the base layer should be effectively reduced by controlling quaternary alloy composition. Very recently, InP/InGaAsSb/InGaAs DHBTs with a low tern-on voltage have been demonstrated by using a Be-doped InGaAsSb base grown by molecular beam epitaxy [7]. On the other hand, there have been few reports on the metal-organic chemical vapor deposition (MOCVD) growth of InGaAsSb.

In this paper, we report the MOCVD growth of undoped and carbon (C)- doped InGaAsSb on InP. We discuss the relationship between alloy composition and molar flow ratio of group-III and group-V precursors in both undoped and C-doped materials. The electric properties of the C-doped InGaAsSb and their relation to alloy composition are described. The influence of hydrogen passivation of carbon acceptors [8] on the electrical properties of the C-doped InGaAsSb is also described.

II. EXPERIMENT

Undoped and C-doped $In_xGa_{1-x}As_{1-y}Sb_y$ films were grown on Fe-doped (001) InP substrates in a low-pressure vertical MOCVD reactor. The carrier gas was hydrogen. The precursors were triethylgallium (TEGa), trimethylindium (TMIn) for group-III elements, arsine (AsH_3) and trimethylantimony (TMSb) for group-V elements, and carbon tetrabromide (CBr_4) for carbon dopant. All samples were grown at the same temperature. The flow rate of CBr_4 during C-doped InGaAsSb growth was the same among the samples. In order to change the alloy composition of samples, the molar flow ratio of precursors were varied. The molar flow ratios of the group-III and V precursors are given by the following equations.

$$R_{III} \equiv [TMIn]/([TMIn]+[TEGa]) \quad (1)$$

$$R_V \equiv [AsH_3]/([TMSb]+[AsH_3]) \quad (2)$$

The total molar flow of the group-III precursors was constant among the samples. Undoped and C-doped GaAsSb films were prepared under similar growth conditions. The total thicknesses of undoped and C-doped InGaAsSb films were 200 nm and around 140 to 180 nm, respectively.

X-ray diffraction (XRD) was used to evaluate the quality of the films. Alloy compositions were determined by inductivity coupled plasma atomic emission spectroscopy (ICP-AES) [9] and also checked by XRD measurements. The van der Pauw method was

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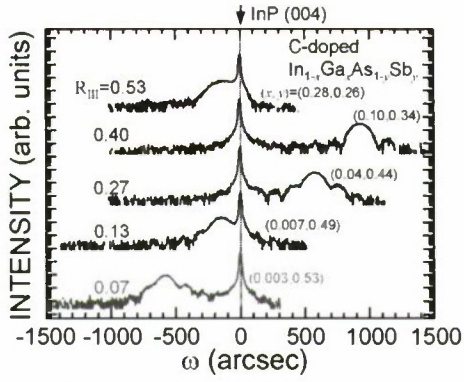

Fig. 1. XRD patterns of C-doped InGaAsSb.

used to measure the hole concentration and mobility in the samples. The influence of hydrogen passivation of carbon acceptors was investigated by annealing samples in nitrogen ambient. Secondary ion mass spectroscopy (SIMS) was used to investigate the differences in carbon and hydrogen concentration between the as-grown and after annealed samples.

III. RESULTS AND DISCUSSION

A. Relationship between alloy composition and molar flow ratio of precursors

We obtained mirror-like smooth surfaces successfully in all the InGaAsSb samples. Figure 1 shows the (004) ω-2θ XRD profiles of the C-doped samples. The pronounced diffraction peaks with Pendellösung fringes indicate the excellent quality of the films. The systematic change of diffraction-peak position with R_{III} was observed and well simulated by the calculation of XRD profiles based on the alloy compositions determined by ICP-AES measurements.

Figures 2(a) and (b) summarizes the relationship between the molar flow ratio of the group-III and group-V precursors and the alloy compositions of undoped and C-doped InGaAsSb. In Fig. 2(a), the In composition x of undoped InGaAsSb is proportional to R_{III}. Such behavior is similar to that reported in the MOCVD growth of typical III-V alloy materials [10]. On the other hand, the x of C-doped InGaAsSb increased nonlinearly with increasing R_{III}. The maximum In content of C-doped sample reached around 0.28. As we discuss later, the nonlinear dependence of In composition on R_{III} in C-doped samples is due to the etching effect caused by CBr_4 decomposition during growth.

Figure 3 shows the effective growth rate of undoped and C-doped samples as a function of R_{III}. The growth rates of undoped samples were approximately constant around 10 nm/min. In contrast, the growth rates of C-doped samples were smaller than that of undoped samples. As shown by gray squares in Fig. 3, the growth rate of C-doped samples decreased

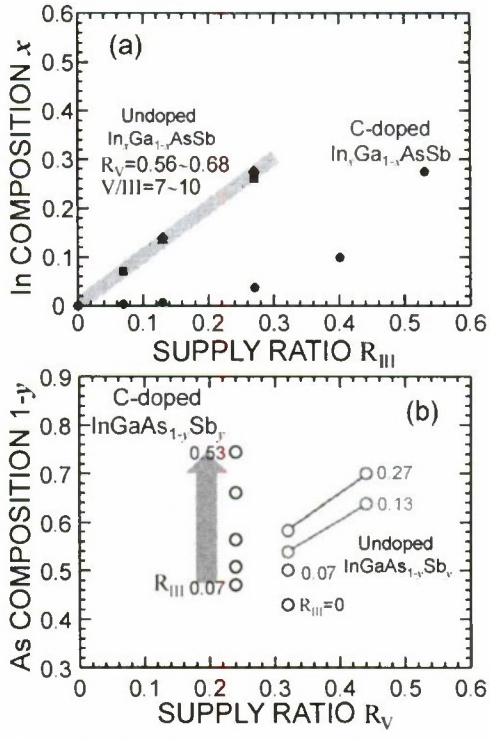

Fig. 2. (a) Molar flow ratio R_{III} vs. In composition x, and (b) molar flow ratio R_V vs. As composition 1-y.

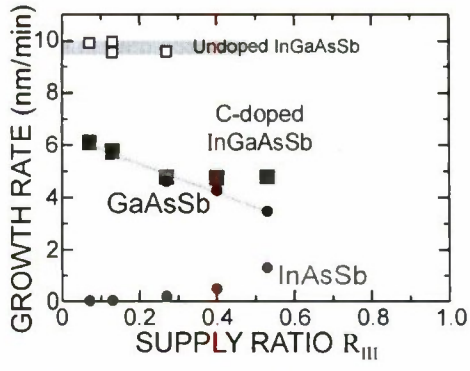

Fig. 3. Molar flow ratio R_{III} vs. growth rate of C-doped InGaAsSb. The growth rates of the GaAsSb and InAsSb components of C-doped InGaAsSb are also plotted. The range of the typical growth rate of undoped InGaAsSb is indicated.

with the increase of R_{III} from 0.07 to 0.27. Then, it became constant in the R_{III} range from 0.27 to 0.53. To discuss the characteristic behavior of the growth rates of C-doped InGaAsSb, we separated the growth rates into GaAsSb and InAsSb components, which are plotted in Fig. 3. The InAsSb components were nearly equal to zero at comparatively low R_{III} of 0 to 0.13, and then increased at R_{III} of 0.13 to 0.27. On the other hand, the GaAsSb components decreased linearly with increasing R_{III}.

One of the possible causes of the decreasing InGaAsSb growth rate at lower R_{III} of 0 to 0.13 is the effect of chemical etching due to hydrobromic acid

(HBr) produced by CBr_4 decomposition. It has been reported that the decomposition of CBr_4 during the growth of C-doped films in H_2 carrier gas and AsH_3 produces CBr_z (z<4) and HBr [11]. The HBr can be adsorbed on the InGaAsSb surface and cause chemical reactions. The possible surface reactions are given by

$$In(ad) + HBr(g) \leftrightarrow InBr(g) + 1/2H_2(g) \quad (3)$$

$$Ga(ad) + HBr(g) \leftrightarrow GaBr(g) + 1/2H_2(g). \quad (4)$$

The volatile InBr and GaBr produced in reactions (3) and (4) are not incorporated in the InGaAsSb layer. Therefore, the growth rate of C-doped InGaAsSb decreases compared with undoped InGaAsSb. The equilibrium constants of reactions (3) and (4) at the InGaAsSb-growth temperature are 1.5×10^{11} and 3.2×10^{12}, respectively [11] and large enough for them to progress. The etching rates of ternary and quaternary alloys are dominated by the volatility of III-Br and the binding energy of group-III and group-V (III-V) bonds [12]. Since the bonding energy of Ga-V bonds is stronger than that of In-V bonds, the etching rate of the In component would be larger than that of the Ga component. Indeed, the etching rate differences between the In and Ga components of III-V quaternary alloys have been reported [11, 12]. Tateno *et al.* [11] have reported that the etching rate of the In component in C-doped InGaAsP is three times as large as that of the Ga component. Arakawa *et al.* [12] have reported that InP and In-containing alloys are easily etched by CBr_4. The effective InAsSb-component growth rate of around zero in the comparatively low R_{III} region in Fig. 2(a) is probably due to the etching rate of the InAsSb component exceeding the InAsSb growth rate. The increase of InAsSb growth rate in the higher R_{III} region probably indicates that the growth rate exceeds the etching rate in that R_{III} region.

The vapor phase reaction between metal-organic precursors and CBr_z might also affect the growth rate but probably to a smaller extent than the etching effects described by reactions (3) and (4). In any case, further quantitative analyses of the reaction are required in order to clarify the growth mechanism.

In Fig. 2(b), the As composition of undoped samples increased with increasing R_V. It should be noted that it increased with increasing R_{III} in both undoped and C-doped samples. The As composition probably increased because InAsSb has a stronger preference for As incorporation than GaAsSb. It has been reported that III-As is incorporated preferentially in MOCVD growth under high V/III ratios [13-17]. The thermodynamic calculation of MOCVD growth of InGaAsSb has also indicated that InAsSb has a stronger preference for As incorporation than GaAsSb [13].

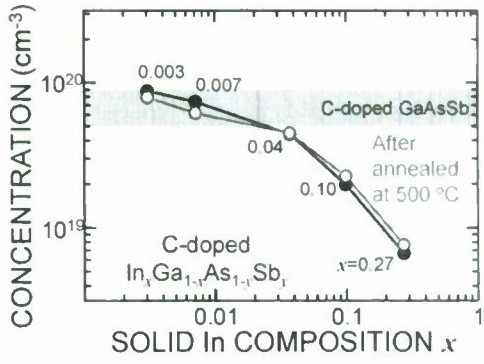

Fig. 4. Indium composition vs. hole concentration of as-grown and annealed C-doped InGaAsSb (closed and open circles).The range of the typical hole concentration of C-doped GaAsSb grown under a similar condition is also indicated.

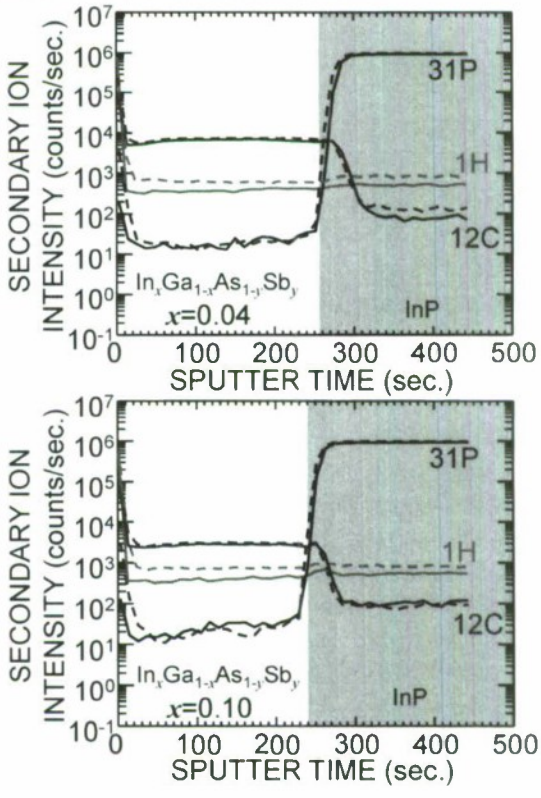

Fig. 5. SIMS profiles of carbon (12C), hydrogen (1H) and phosphorous (31P) of as-grown (solid line) and annealed (dashed line) C-doped InGaAsSb/InP.

These previous studies support the increase of As composition with increasing R_{III}.

B. Effects of hydrogen passivation of acceptors in C-doped InGaAsSb

Figure 4 shows the In-composition dependence of hole concentration of as-grown and annealed C-doped InGaAsSb films. Here, the CBr_4 flow rate was the same among the samples during the growth. The range of typical hole concentrations in C-doped

GaAsSb grown under similar conditions is also indicated. Hole concentrations of over 2×10^{19} cm^{-3} were successfully obtained in as-grown InGaAsSb at In composition of less or equal to 0.10. The reduction of hole concentration with increasing In composition probably reflects the In composition dependence of doping efficiency. We found that hole concentrations in the samples with comparatively high In composition of over 0.10 were hardly changed by nitrogen-ambient annealing. The increase in hole concentration was not so significant and similar to that in C-doped GaAsSb [8]. Compared with MOCVD-grown C-doped InGaAs, hydrogen passivation of carbon seems to be quite suppressed in the InGaAsSb samples. Figure 5 shows the SIMS profiles of carbon and hydrogen in the as-grown and annealed C-doped InGaAsSb films with the In composition of 0.04 to 0.10. Secondary ion intensities of hydrogen were at the background level of the SIMS analysis for all samples. There are no significant differences between as-grown and annealed C-doped InGaAsSb films, as shown in Fig. 5. These results also suggest that the effect of hydrogen passivation on C-acceptors is eliminated in C-doped InGaAsSb, which is similar to the case of C-doped GaAsSb [8].

C. Hole concentration and mobility of C-doped InGaAsSb

Figure 6 shows the relation between the hole concentration and mobility of C-doped InGaAsSb and GaAsSb. The hole mobility of the samples with comparatively low In composition was around 35 cm^2/Vs and almost similar to that of the GaAsSb samples. In contrast, it decreased with increasing In composition of over 0.10. The alloy scattering might be enhanced in the samples with higher In composition and affect the mobility. Further systematic investigations are expected to clarify the growth mechanism, which will enable us to further improve the crystal quality and electronic properties of C-doped InGaAsSb.

IV. CONCLUSION

MOCVD growth of undoped and heavily C-doped InGaAsSb was performed. The relationship between quaternary alloy composition and molar flow ratio of precursors was investigated. The introduction of CBr_4 for carbon doping caused nonlinear dependence of In composition on the molar flow ratio R_{III}, which can be explained by the difference in the etching behavior between the In and Ga components of InGaAsSb. The Sb composition of undoped and C-doped InGaAsSb films decreased with increasing R_{III}. Such behavior is probably due to preferential As incorporation into InAsSb, which has been reported in the literature. C-doped InGaAsSb layers with high hole concentrations of over 2×10^{19} cm^{-3} was obtained for comparatively low In composition. The impact of hydrogen passivation of C-acceptors in C-doped InGaAsSb was almost negligible and similar to that in C-doped GaAsSb under the same growth condition.

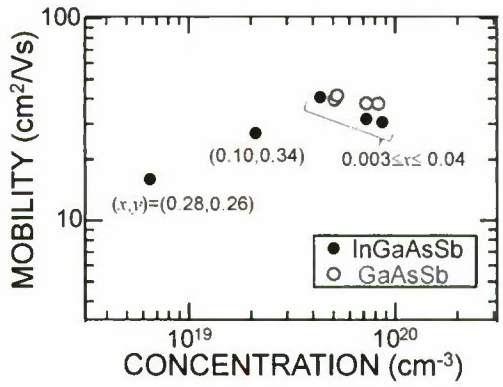

Fig. 6. Correlation between hole concentration and mobility of C-doped GaAsSb and InGaAsSb.

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The Combination For Thermodynamic Model And Precursor State Used In GaAsSb/GaAs Multiple Quantum Wells Grown By Gas Source Molecular Beam Epitaxy

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Abstract

The competition behavior between two Group V atoms is significant in the epitaxy growth of III-V-V compounds. We have developed a combination for the precursor state and the associated thermodynamic model in order to describe the competition behavior between Sb and As atoms during the pseudomorphic growth of GaAsSb/GaAs multiple quantum wells (MQWs) on GaAs (100) substrates by gas-source molecular-beam epitaxy (GSMBE). The strain-induced incorporation coefficient due to lattice mismatch between the growing film and substrate is also taken into account.

I. Introduction

Molecular beam epitaxy (MBE) is developed to use for the growth of GaAsSb/GaAs heterostructure alloy extensively, because of its type-II band alignment provides an excellent opportunity to improve the performance of optoelectronic devices.[1] The different incorporation behavior between As and Sb atoms results in that there is no linear dependence of composition on the ratio between As and Sb element fluxes. Competition in two group V atoms play a important role on the growth surface during incorporation.[2] Presumably, the competition could result such that it is difficult for atoms to join into the lattice, which could promote desorption of extra atoms that have escaped from among incident molecules in the precursor state. Additionally, some researchers have also implied that a thermodynamic approach is less valid without considering the effect of desorption at lower substrate temperature.[3]

In previous publications on thermodynamic model[4]-[5] used in the epitaxy growth of III-V-V compounds, the two group V elements was considered to be independent for two parallel reactions at the beginning; competitive behavior between two group V atoms was neglected and nor were changes in chemical potential of the primary reactants. So, the trend of curve fitting is not good agreement with some reported data[6]-[7] for the primitive thermodynamic model.[5] Thus far, no studies have focused on the incorporation behavior of Sb and As during pseudomorphic growth in GaAsSb/GaAs multiple quantum wells by gas source molecular beam epitaxy (GSMBE) using a non-equilibrium thermodynamic model.

In this paper, a precursor state for non-equilibrium thermodynamic model is investigated and the effect of strain due to lattice mismatch between the growing film and substrate was taken into account.[8] Strain induced incorporation coefficient variation was defined by an additive elastic strain term in the Gibbs free energy.[9]

II. Experiment

Growth of GaAsSb/GaAs multiple quantum wells (MQWs) were carried out on semi-insulating GaAs (100) substrates by using a VG V-80MKII gas source molecular beam epitaxy (GSMBE) apparatus. The As_2 source was cracked from the AsH_3 gas cell, and the Sb_2 source was supplied via an EPI Model 175 standard cracker K cell.

Substrates were attached to MO heater blocks. Before growth, surface oxidation of the substrate was desorbed by treatment with As_2-rich flux at 600°C and verified by observing reflection high energy electron diffraction (RHEED) patterns. An undoped 1000 Å GaAs buffer layer was grown at 580 °C, first to prepare a smooth growth surface and then with growth interruption for the substrate feed at different temperatures, 400 °C, 430 °C, 460 °C, 490 °C, 520 °C, and 550 °C, for growth of multiple quantum wells that contain five periods of GaAs (300 Å)/GaAsSb (50Å). A final growth interruption occurred for the substrates feed at 580 °C for growth of a 1000Å GaAs cap layer. The growth rate for all samples determined by the arrival rates of Ga element is near $1\ \mu m/hour$. All temperature values were measured with a thermocouple surveyed by an infrared pyrometer.

Sb/As beam equivalent pressure (BEP) ratios were measured by ion gauge. Composition of antimony in the GaAsSb/GaAs MQW was determined by double crystal X-ray diffraction (XRD) measurement. XRD analysis was carried out using the $CuK\alpha_1$ line of wavelength $\lambda = 0.154nm$ generated by a Bede diffractometer. The solid compositions of Sb in the GaAsSb alloy at different temperature are shown in Table 1.

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Table 1. Flux ratio (F_{Sb}/F_{As}) and Sb composition of samples at different substrate temperatures.

Sample	Substrate temperature (℃)	F_{Sb}/F_{As}	Sb Composition
1	400	0.099	0.348
2	400	0.091	0.320
3	400	0.110	0.350
4	430	0.099	0.310
5	460	0.257	0.320
6	460	0.340	0.358
7	460	0.222	0.310
8	460	0.121	0.260
9	460	0.104	0.240
10	490	0.099	0.220
11	520	0.099	0.203
12	550	0.088	0.155
13	550	0.099	0.149

III. Theory

Competition between two Group V atoms plays a important role on the growth surface during epitaxy.[2] It is attributable to atoms with disparate incorporation rates and the characteristics of atoms themselves. It is well-known that because of the segregation effect of the Sb atom, Sb content in GaAsSb would vary seriously along the growth direction, especially for MQW epitaxy.[10] It is also reasonably to hypothesize that the segregation effect results in desorption of atoms form some of the incident molecules.[10] There are previous reports of an available process to lower substrate temperature in order to reduce the segregation effect during epitaxial growth.[11] However, some researchers have also implied that a thermodynamic approach is less valid without considering the effect of desorption at lower substrate temperature.[3]

At the start of the model, MBE growth is assumed to be a non-equilibrium process with chemical potential change between gas and solid phases under Group V-rich conditions. Formation of $GaAs_{1-y}Sb_y$ alloy is based on homogeneous mixture reactions of GaAs and GaSb binaries.

During epitaxial growth, incident fluxes of Ga, As_2, and Sb_2 in the gas phase first physisorb on the growth surface in a so-called precursor state. Those incident fluxes satisfy the equations presented below.[12]

$$\begin{cases} \frac{\partial N_{Ga}}{\partial t} = -G - \frac{N_{Ga}}{\tau_{Ga}} + F_{Ga} \\ \frac{\partial N_{As_2}}{\partial t} = \frac{-G(1-y)}{2} - \frac{N_{As_2}}{\tau_{As_2}} + F_{As_2} \\ \frac{\partial N_{Sb_2}}{\partial t} = \frac{-Gy}{2} - \frac{N_{Sb_2}}{\tau_{Sb_2}} + F_{Sb_2} \end{cases}$$

, where N_i is the number of corresponding molecules in the precursor state, τ_i is the lifctimes of corresponding molecules in the precursor state, G is the incorporation rate of GaAsSb, and F_{Ga} , F_{As_2} , F_{Sb_2} are the incident flux.

Two formation reactions of binaries $GaAs$ and $GaSb$ are thought to proceed in parallel:

$$\begin{cases} Ga_{(g)} + \frac{1}{2}As_{2(g)} \rightarrow GaAs_{(s)} \\ Ga_{(g)} + \frac{1}{2}Sb_{2(g)} \rightarrow GaSb_{(s)} \end{cases}$$

, where the gas phase and solid phase are marked by g and s, respectively. The differences in chemical potentials for the corresponding reactions are as follows:[5]

$$\Delta\mu_{GaAs} = K_B T \ln\left(\frac{N_{Ga}}{N_{Ga}^{eq}}\right) + \frac{1}{2}K_B T \ln\left(\frac{N_{As_2}}{N_{As_2}^{eq}}\right) - \left(K_B T \ln a_{GaAs} + (1-y)\Delta G_{GaAs}^{str}\right)$$

$$\Delta\mu_{GaSb} = K_B T \ln\left(\frac{N_{Ga}}{N_{Ga}^{eq}}\right) + \frac{1}{2}K_B T \ln\left(\frac{N_{Sb_2}}{N_{Sb_2}^{eq}}\right) - \left(K_B T \ln a_{GaSb} + y\Delta G_{GaSb}^{str}\right)$$

, where K_B and T are Boltzmann constant and substrate temperature, N_i^{eq} is the number of molecules for the corresponding equilibrium flux of substance i. a_{GaAs} and a_{GaSb} are the activities of GaAs and GaSb in $GaAs_{1-y}Sb_y$ and may be expressed as follow:[13]

$$a_{GaAs} = (1-y)\exp\left[\frac{y^2\Omega}{K_B T}\right] \quad , \quad a_{GaSb} = y\exp\left[\frac{(1-y)^2\Omega}{K_B T}\right]$$

, where Ω is an interaction parameter between the GaAs and GaSb compounds in the ternary alloy, which can be obtained from the delta lattice parameter (DLP) model.[14]

ΔG^{str} is the Gibbs energy due to the strain induced by the lattice mismatch between the substrate and the corresponding binary component, which can be expressed as follows:[9]

$$\Delta G^{str} = C_{44}\frac{1+\nu}{1-\nu}V_m\left(\frac{\Delta a}{a}\right)^2$$

, where C_{44} is the elastic coefficient, ν is the Poisson ratio, V_m is the molar volume and $\frac{\Delta a}{a}$ is the lattice mismatch between the unstrained layer and substrate.

By combining chemical potential change of two homogeneous reactions for GaAsSb, we get the following expression:

$$\Delta\mu_{GaAsSb} = (1-y)\Delta\mu_{GaAs} + y\Delta\mu_{GaSb}$$

The steady-state equation is generated and expressed as follows:

$$\frac{\partial\Delta\mu_{GaAsSb}}{\partial y} = 0 \, , \, \frac{\partial N_{Ga}}{\partial t} = 0 \, , \, \frac{\partial N_{As_2}}{\partial t} = 0 \text{ and } \frac{\partial N_{Sb_2}}{\partial t} = 0$$

It is assumed that $\tau_{Ga} \rightarrow \infty$ and no desorption for Ga fluxes due to the sticking coefficient of Ga atom is closed to unity. Combing all equations of above results in an equation while the epitaxy growth is in steady-state, shown as follows:

$$\left(\frac{\frac{F_{As_2}}{F_{Ga}} - \frac{1-y}{2}}{\frac{F_{Sb_2}}{F_{Ga}} - \frac{y}{2}}\right)^2 = \frac{\tau_{As_2}N_{Sb_2}^{eq}}{\tau_{Sb_2}N_{As_2}^{eq}}\left[\frac{y}{1-y}\exp\left(\frac{\Omega(1-2y) + \left((2\nu-2)\Delta G_{GaAs}^{str} + 2\nu\Delta G_{GaSb}^{str}\right)}{K_B T}\right)\right]^2$$

Finally, it is derived the relation $\frac{F_{Sb_2}}{F_{As_2}}$ vs. y.

IV. Results and discussions

The results of calculation for GaAsSb at different growth

temperatures are shown in Fig. 1. The only unknown value is $\left(\frac{\tau_{As_2} N_{Sb_2}^{eq}}{\tau_{Sb_2} N_{As_2}^{eq}}\right)$, and it is taken a fitting parameter in this model. Because there have been no reports about the details of $\left(\frac{\tau_{As_2} N_{Sb_2}^{eq}}{\tau_{Sb_2} N_{As_2}^{eq}}\right)$ until now, it is available to prove that $log\left(\frac{\tau_{As_2} N_{Sb_2}^{eq}}{\tau_{Sb_2} N_{As_2}^{eq}}\right)$ vs. (1000/T) is a linear relation, as shown in Fig. 2.

Additionally, the slope of the linear line is consistent with the difference of desorption energy for both As and Sh atoms.[15]-[16]

Fig. 1 clearly shows that the Sb atom has a higher priority than As to incorporate into the growth surface at a relatively low flux ratio (F_{Sb} / F_{As}),[6] especially at a lower growth temperature, because of competition between As and Sh atoms for finite incorporation sites.[2] For a relatively high flux ratio (F_{Sb} / F_{As}), Sb incorporation exhibits saturation, which is attributable to competition between Sb atoms for the same incorporation sites.[2] It is also apparent that the saturation effect is more evident at a higher growth temperature, we can infer that the segregation effect of Sb atoms plays a major role at higher temperatures.

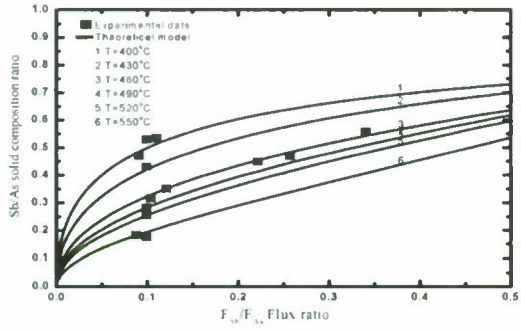

Fig. 1. Sb/As solid composition as a function of flux ratio (F_{Sb} / F_{As}) at different substrate temperatures.

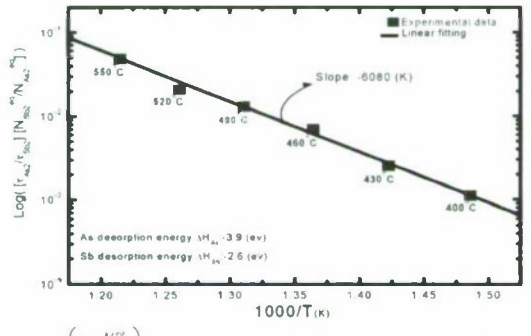

Fig. 2. $log\left(\frac{\tau_{As_2} N_{Sb_2}^{eq}}{\tau_{Sb_2} N_{As_2}^{eq}}\right)$ vs. (1000/T) at different substrate temperatures

V. Conclusion

We have successfully proposed a combination of thermodynamic model and precursor state in order to describe the desorption phenomenon that is attributable to competition between two Group V atoms; the calculated results are in good agreement with experimental data obtained for GaAsSh/GaAs MQWs during pseudomorphic growth. We also prove that the only fitting parameter $\left(\frac{\tau_{As_2} N_{Sb_2}^{eq}}{\tau_{Sb_2} N_{As_2}^{eq}}\right)$ has a linear relationship with respect to (1000/T) and the slope of the line is consistent with the difference of desorption energy for both As and Sh atoms.

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Investigation of the origin of InAs dot formation at the growth interrupted AlGaInAs hetero-interface grown by MOVPE

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Abstract

In the growth of AlGaInAs/InP material system by metal organic vapor phase epitaxy (MOVPE), there are many hillocks on the wafer in some growth conditions. We analyzed the hillocks by TEM and EDX and found that the origin of the hillocks is InAs dots on growth interrupted interface. In addition, we investigated the growth condition dependence of hillock distribution in details, and revealed the origin and the mechanism of the formation of InAs dots.

I. Introduction

AlGaInAs materials are preferable to the conventional InGaAsP materials in optical device application, because the AlGaInAs material systems have the large conduction band discontinuities and the small inter valence band absorption in comparison with those of the InGaAsP systems. Owing to these superior properties, higher modulation speed and higher operation temperature have been realized by AlGaInAs-based optical device on InP substrates.

However, the incorporation of oxygen into crystal is a problem for the growth of AlGaInAs by metal-organic vapor phase epitaxy (MOVPE). To avoid the incorporation of oxygen, the growth temperature of AlGaInAs is generally set to be higher than that of InP or InGaAsP [1,2]. Therefore, the changing process of the growth temperature between AlGaInAs and InP is necessary for the growth of AlGaInAs/InP material system. The optimization of the growth sequence of the hetero-interface is important to the quality of the epitaxial layer, which relates the character of the optical device.

In this work, we investigate anomalous morphology, which is appeared in the periphery of the wafer, in the growth of AlGaInAs/InP material system. We reveal that this anomalous morphology consists of many hillocks, which originated from InAs dots on the hetero-interface of AlGaInAs layers. And the formation of these dots is affected by the growth parameters of the MOVPE. Moreover, we considered the mechanism of the formation of InAs dots from the dependence on the growth parameters, and obtained a new knowledge concerning the growth interruption of AlGaInAs/InP material system.

II. Experimental

The AlGaInAs epitaxial layers were grown by MOVPE apparatus on an InP (100) substrate. The reactor pressure was 100 hPa and the total hydrogen flow was 25 slm. TMIn, TMGa and TMAl were used as the group-III source, PH_3 and AsH_3 were used as the group-V source. Figure 1 shows a schematic drawing of the epitaxial layers and the growth temperature of each layer. The growth procedure is as follows; a 1.8 μm-thick InP buffer layer was grown at 600 °C on a 2"ϕ InP (100) substrate, and then growth temperature was elevated to 680 °C in PH_3 atmosphere. After that, the 20 nm-thick AlGaInAs layer-(a) was grown at 680 °C in AsH_3 atmosphere. Then, growth temperature was elevated to 720°C in AsH_3 atmosphere within 3 minutes and stabilized 2 minutes, and the AlGaInAs layer-(b) was grown at 720 °C. Although AlGaInAs layers should be grown at 720 °C to avoid the incorporation of oxygen, such a high temperature is not suitable for the growth of InP because its surface is damaged by the desorption of phosphorus. Thus, in the growth from InP layer to AlGaInAs layer, we applied the two-step raising sequence of the growth temperature shown in Fig. 1.

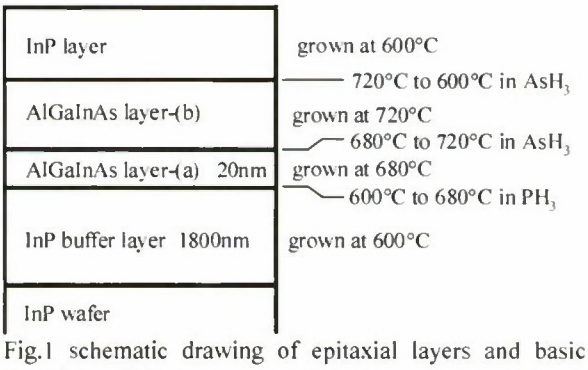

Fig.1 schematic drawing of epitaxial layers and basic growth condition

Several samples were made and investigated those morphology by varying the growth parameters; thickness of InP buffer layer, that of AlGaInAs layer, the time of the growth

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interruption during raising the temperature, and the growth temperature.

The morphology was analyzed by differential interference contrast microscope, transmission electron microscope (TEM), and energy dispersive X-ray spectroscopy (EDX).

III. Results & Discussion

Figure 2 shows a surface morphology of the anomalous growth area. There are many hillocks in the area within a few millimeters width from the periphery of the wafer. The density

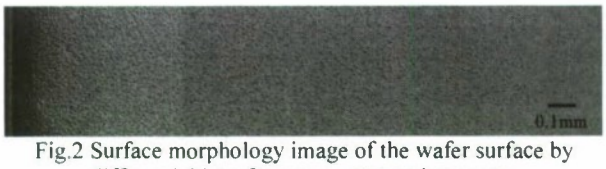

Fig.2 Surface morphology image of the wafer surface by differential interference contrast microscopy. The wafer rim is left side of this figure.

of the hillocks is high near the periphery, and it decreases towards the inside of the wafer. Figure 3 shows the cross-sectional TEM image of the hillock. It shows that hundreds-nm-high dot exist under the hillock, and this dot is grown near the interface of InP and AlGaInAs layer. Figure 4 shows the TEM-EDX spectrum at the point in Fig. 3. The EDX peaks correspond to In, As and Si. On the other hand, the peaks which corresponding to Al, Ga and P are not detected. These results indicate that the hillocks are originated from InAs dot.

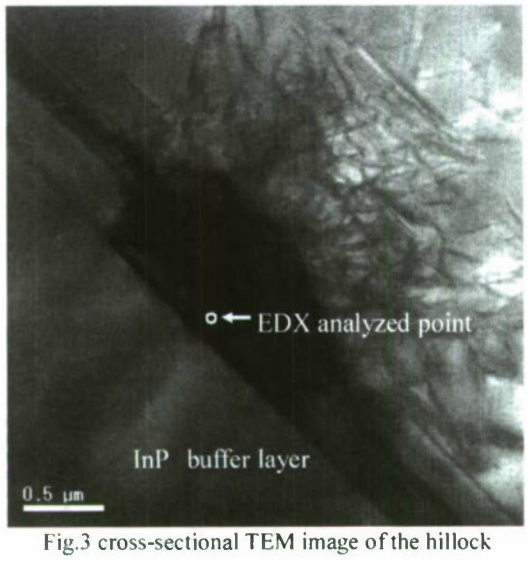

Fig.3 cross-sectional TEM image of the hillock

The width of this anomalous growth area and the density of the hillocks depend on the sample structure as follows:

1) When the thickness of InP buffer layer is increased, the density of the hillocks increase (the correlation between the thickness of buffer layer and the density of the hillocks is shown in Fig. 5).

(2) When the thickness of the first AlGaInAs layer (a) is increased from 20 nm to 1500 nm, the hillocks disappear.

(3) When the interruption time between the AlGaInAs layers (a) and (b) is increased from 5 minutes to 20 minutes, the hillocks increase several times in density and area.

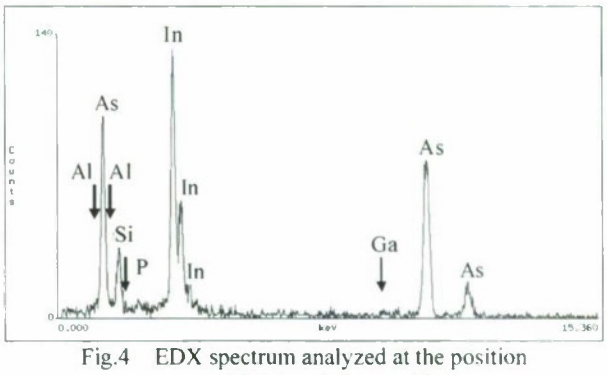

Fig.4 EDX spectrum analyzed at the position which is pointing on Fig.3.

As for the result (2), it suggests that the InAs dots are not formed during the growth of AlGaInAs. In other words, the compositional modulation by segregation of InAs phase during the growth of the AlGaInAs layer is not occurred. Though both indium and arsenide source is necessary for the formation of InAs dots, AsH_3 is not supplied during the growth of the buffer layer on the result (1). And TMIn is not supplied during the growth interruption on the result (3). Considering the above discussion together, the only possible mechanism is as follows; at first, indium absorbs on the susceptor during the growth of the InP buffer layer. And then it desorbs from the susceptor during the growth interruption for raising the growth temperature in AsH_3 atmosphere. This model is supported by the results that the anomalous morphology exists only in the periphery of the wafer. In the following discussions, we clarify the validity of this model.

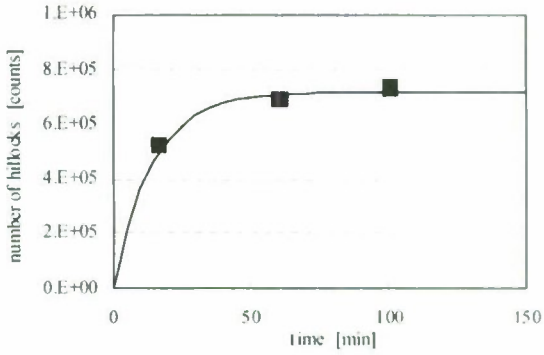

Fig.5 the number of hillocks in periphery of wafer surface as a function of the growth time of the InP buffer layer.

Figure 5 shows the total number of the hillocks on the wafer surface as a function of the growth time of the InP buffer layer. The data points show our experimental result. As is shown in Fig. 5, the number of the hillocks increases in the

growth time of the InP buffer layer. In order to explain this behavior, we consider the adsorption and desorption processes of indium during the growth of InP buffer layer.

The adsorption and desorption processes can be expressed by the following equation (1):

$$\frac{\partial N_{sus}}{\partial t_{buff}} = a - bN_{sus} \qquad (1)$$

where N_{sus} is the density of indium molecules on the susceptor and t_{buf} is the growth time of the InP buffer layer, that is, the time which indium is supplied on the susceptor. Equation (1) indicates that indium molecules constantly adsorbed and desorbed proportional to the density of indium molecules N_{sus}. Because the indium which desorbed from the susceptor is assumed to be incorporated into the wafer surface by a certain fixed ratio, the total number of the hillocks N_h is proportional to N_{sus} ($N_h = kN_{sus}$). Thus, equation (1) can be rewritten as:

$$\frac{\partial N_h}{\partial t_{buff}} = a \cdot k - bN_h \qquad (2)$$

By solving this equation, equation (3) is obtained.

$$N_h = A\{1 - \exp(-b\, t_{buff})\} \qquad (3)$$

In this equation, we replace $A = ak/b$. The solid line in Fig. 5 is a fitting line by using equation (3). As can be seen in Fig. 5, this line agrees with the experimental data. This result also supports our model for the formation mechanism of the InAs dots. The fact that a function such as equation (3) fits the experimental data means the presence of adsorption and desorption process of indium molecules on the wafer susceptor.

Next, in order to clarify how indium molecules desorb from the susceptor, we focus on the relation between the density of the hillocks and the reached temperature during the growth interruption between AlGaInAs layer-(a) and -(b). Figure 6 shows the density of the hillocks appearing in the edge of the wafer as a function of the growth temperature of AlGaInAs layer (b). In Fig. 6, the growth temperature "600 °C" means that the growth temperature of AlGaInAs layers and that of InP buffer layer (600 °C) are the same, and only the growth interruption is applied between AlGaInAs layers. In this sample, no hillocks were observed on the edge of the wafer by microscope (It means that the density of the hillocks was <1E+4 counts/cm^2). According to the above model that indium supplies from the susceptor to the wafer, the indium supplied from the susceptor is not sufficient to form hillocks at 600 °C.

As for the process about the desorption of indium molecules, following two process can be assumed. The first model is that indium molecule is supplied by the resolution of InP polycrystal on the susceptor. The second model is that indium molecule is originated from the unresolved TMIn which is supplied during the growth of the InP buffer layer [3]. In the case of the second model, we assumed that TMIn diffuses onto the wafer and the distribution of TMIn vapor on the wafer

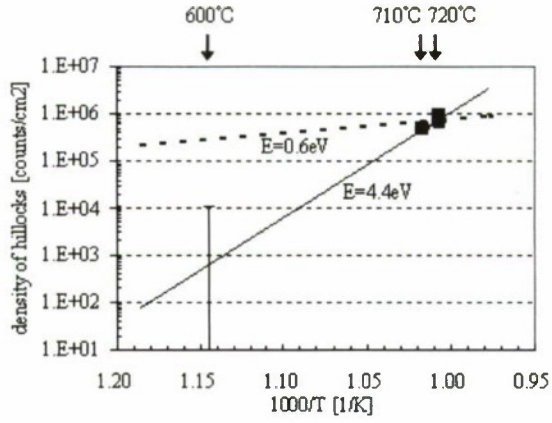

Fig.6 The density of hillocks in the rim of wafer surface as a function of the growth temperature of AlGaInAs layer (b) growth interruption.

causes the hillocks on the periphery of the wafer. However, the latter model is not able to explain the experimental results discussed previously: the hillocks disappeared when the thickness of the AlGaInAs layer changed from 20 nm to 1500 nm. In this case, if indium molecules for InAs dots are supplied by unresolved TMIn, the hillocks should be increased because the same flow of TMIn was supplied during the growth of both AlGaInAs layer and InP buffer layer.

Next, we consider these two models from a different point of view. The desorption rate of the indium molecules from the susceptor is proportional to exp(-Ea/kT); Ea is the activation energy for the desorption of indium molecule, k is Boltzmann constant, T is the temperature of the susceptor. In the case where InP polycrystal on the susceptor resolves, the activation energy Ea is assumed to be as 4.4 eV which is the equilibrium constant of the equilibrium reaction (InP $\leftrightarrow$ In + 1/4P_4) [4]. The solid line in Fig. 6 shows the temperature dependence of the density of the hillocks by using the activation energy Ea = 4.4 eV. In this model, the density of the hillocks is <1E+4 counts/cm^2 where the growth temperature is 600 ℃. On the other hand, in the case of the desorption of the unresolved TMIn on the susceptor, the activation energy Ea is calculated as 0.6 eV from the temperature dependence of the vapor pressure of TMIn [5]. The dashed line in Fig. 6 is the estimation from the activation energy Ea = 0.6 eV. As can be seen in Fig. 6, this dashed line can not explain our experimental data. Thus, we conclude that the indium molecules are supplied by the resolution of InP polycrystal on the susceptor.

Next, we discuss the diffusion process of the indium molecules which desorbs from the susceptor. We assumed the following two processes about the diffusion of indium molecules. The first process is that indium vapor diffuses after the InP polycrystal resolves. The second process is that indium adatom which is supplied from the susceptor, diffuses on the wafer surface. In order to examine the validity of these process quantitatively, we considered the diffusion coefficient of both

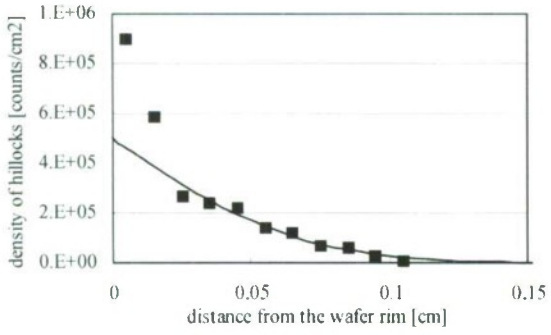

Fig.7 The distribution of the density of the hillocks near the edge of the wafer grown under the condition as shown in Fig.1.

the processes. The diffusion coefficient of indium vapor is calculated as 45 cm^2/sec at 720 °C by using the kinetic theory of gas and the Lennard-Jones potential of the carrier gas (hydrogen and indium). On the other hand, while the diffusion coefficient of surface migration is affected by condition of the wafer surface, we can estimate it roughly at 1E-5 cm^2/sec [6]

Figure 7 shows the dependence of the density of hillocks on the distance from the edge of the wafer grown under the condition shown in Fig. 1 The solid line in Fig. 7 indicates the equation (4) which is obtained from the diffusion equation (5).

$$N_{waf} = erfc\left(\frac{x}{\sqrt{Dt_{int}}}\right) \qquad (4)$$

$$\frac{\partial N_{waf}}{\partial t_{int}} = -D\frac{\partial N_{waf}}{\partial x} \qquad (5)$$

N_{waf} is the density of indium molecules adsorbed on the wafer, x is the distance from the edge of the wafer, D is the diffusion constant and t_{int} is the period of the interruption of growth between AlGaInAs layer-(a) and -(b). In these equations, both diffusion coefficient and boundary condition N_{waf} (x=0) are constant against time. In the case that t_{int} and D are set on 2 minutes and 1.1E-5 cm^2/sec, respectively, there is good agreement between the calculated curve and the experiment except for the nearest two data from the edge (these two values lie in the distance of 0.2 mm from the edge, and so these are affected by the beveling of the wafer). The value of diffusion constant, 1.1E-5 cm^2/sec, means that distribution of the density of hillocks is governed by the surface migration of indium adatoms.

On the other hand, the value of the diffusion coefficient of indium vapor (45 cm^2/sec) is too large to explain the distribution of the hillocks density. Therefore, the indium vapor diffusion does not relate the anomalous growth in the periphery of the wafer.

IV .Conclusion

In conclusion, we investigated the anomalous growth observed in AlGaInAs/InP material system grown by MOVPE. From the analysis of the anomalous growth by using cross-sectional TEM and EDX, we found that the InAs dots exist on the hetero-interface of between AlGaInAs and InP, where coincidence with the interface applying the growth interruption. Furthermore, by analyzing the dependence of the density of the hillocks on the growth condition and the sample structure, we cleared the mechanism of the formation of InAs dots. Indium molecules which are originate from the resolution of the InP polycrystal on the susceptor, are supplied to wafer surface during the growth interruption. Then, indium adatoms migrate on the wafer surface, and the InAs dots are formed in AsH_3 atmosphere.

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Comparative Study of Spacer Layers for InAs Quantum Dot Stacks

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Quantum Dot Density Studies for Quantum Dot Intermediate Band Solar Cells

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MOVPE GROWTH OF InPN FILMS ON InP(001) SUBSTRATES

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Abstract—Dilute-nitride alloy InPN films have been grown by metalorganic vapor phase epitaxy (MOVPE), and the N incorporation behavior is investigated by varying the major growth parameters. The grown-surface morphologies show that the 2-dimensional (2D) growth with atomically flat surfaces is obtained at 460-500°C with relatively high P supplies. The XRD analyses show that the N incorporation increases for lower growth temperatures and higher N/P ratios, and the N concentration up to 0.18% has been attained. The 150-170 nm-thick InPN films are coherently grown on InP(001) without lattice relaxation.

I. Introduction

The InPN alloy is a potential material for infrared optoelectronics applications of the wavelengths around 0.9 μm or longer. As commonly found in III-V-N type alloys [1-3], a significant bandgap reduction with N incorporation due to the huge bandgap bowing is expected in InPN. Bi and Tu reported a bowing parameter in the range as large as 13-17 eV [4] by studying the N-incorporated InP films grown by gas-source MBE. However, the studies of InPN have been limited to the N concentrations much less than 1% by MBE [4] and LPE [5] due to the extremely low N solid solubility. In fact, the N solubility in InP is as low as 1.2×10^{-5} at 600°C equilibrium as estimated using the interaction parameter Ω=82.2 kJ/mol based on the delta lattice parameter (DLP) model [6]. In this work, the growth of InPN films has been attempted by MOVPE. The N incorporation behavior is investigated by varying the major growth parameters.

II. Experimental

For the MOVPE growth of InPN films, trimethyindium (TMIn), tertiarybutylposphine (TBP) and dimethylhydrazine (DMHy) are used as the In, P and N precursors, respectively. An rf-heated horizontal-type reactor which is designed so as to avoid parasitic reactions between TMIn and DMHy by separately supplying the two precursors onto the susceptor region [7]. With this reactor, DMHy is fed through a capillary extending to the vicinity of the substrate, while TMIn and TBP are introduced to the reactor from the inlet at the up-stream region. The reactor pressure was 60 Torr, and an N_2 carrier was used to enhance N incorporation [8]. After the growth of an InP buffer layer (~120 nm) on a Fe-doped semi-insulating InP(001) substrate at 500°C for 15 min, the InPN layer was grown for 20 min at the temperature range of 460-520°C. During the growth of InPN, the TMIn and DMHy supplies were maintained at 8.71 and 1000 μmol/min, respectively, while the [TBP]/[TMIn] ratio was varied from 20 to 50. The InPN layer thickness was around 150-170 nm. The grown-surface morphologies were evaluated with a scanning electron microscope (SEM) and an atomic force microscope (AFM). The N concentrations of the grown films were estimated from fitting the 2θ-ω (004) high-resolution X-ray diffraction (HRXRD) profiles with a dynamic simulation. In order to evaluate the lattice relaxation, the XRD reciprocal space mappings of the asymmetrical (115) reflection were carried out.

III. Results and Discussion

Fig. 1 collects the SEM images showing the surface morphology of the InPN films grown at

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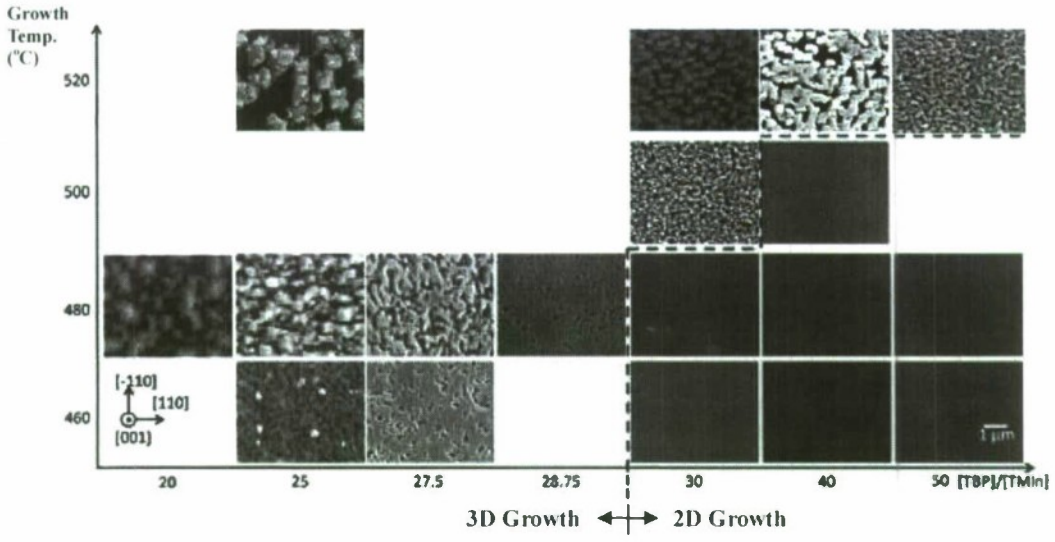

Fig. 1 SEM images showing the surfaee morphology of the InPN films grown on InP (001) substrates at 460-520°C with different [TBP]/[TMIn] ratios between 20 and 50. The boundary of 2D/3D growth is shown.

Table 1 RMS roughness (nm) of the InPN surfaees as estimated from the AFM observations.

Growth Temp.	[TBP]/[TMIn]= 20	25	27.5	28.75	30	40	50
520 °C		220			93	79	34
500 °C					52	0.3	
480 °C	102	38	46	8.6	0.6	0.3	0.3
460 °C		47	19		0.7	0.3	0.3

different temperatures and [TBP]/[TMIn] ratios. It is observed that the 3-dimensional (3D) growth resulting rough surfaces dominates for the InPN films under lower (<30 at 460 and 480°C, and <40 at 500°C) [TBP]/[TMIn] ratios, while the 2-dimensional (2D) growth with a fairly flat surfaee is attained under higher [TBP]/[TMIn] ratios at 460-500 °C. The boundary of 2D/3D growth shifts to higher [TBP]/[TMIn] ratios for higher growth temperatures as expeeted from the enhaneed desorption of P atoms from the growing surfaee leading to a rough surfaee. The root-mean-square (RMS) roughness values of the InPN film surfaees as estimated from the AFM observations are listed in Table 1. The RMS roughness values are below 0.7 nm and typically 0.3 nm within the 2D-growth regime indieating atomieally flat surfaees, while they are much over 10 nm for the rough surfaees within the 3D-growth regime.

Fig. 2 (a) and (b) show the 20-ω (004) HRXRD profiles of the InPN films grown at different temperatures and [TBP]/[TMIn] ratios, respeetively. The diffraction from the InPN film is nearly discernible at the higher angle side beside the main peak of InP(004) from the InP buffer layer, and it shifts to higher diffraction angles with decreasing growth temperature and [TBP]/[TMIn] (*i.e.* higher N/P) ratio indicating the enhaneed N ineorporation in the film. The clearly observed Pendellösung fringes indicate the growth of a flat and uniform InPN film and interface, and faeilitate the estimation of the InPN film thickness of 150-170 nm. The film thiekness is almost independent of the TBP flow rate and mostly determined by the TMIn supply

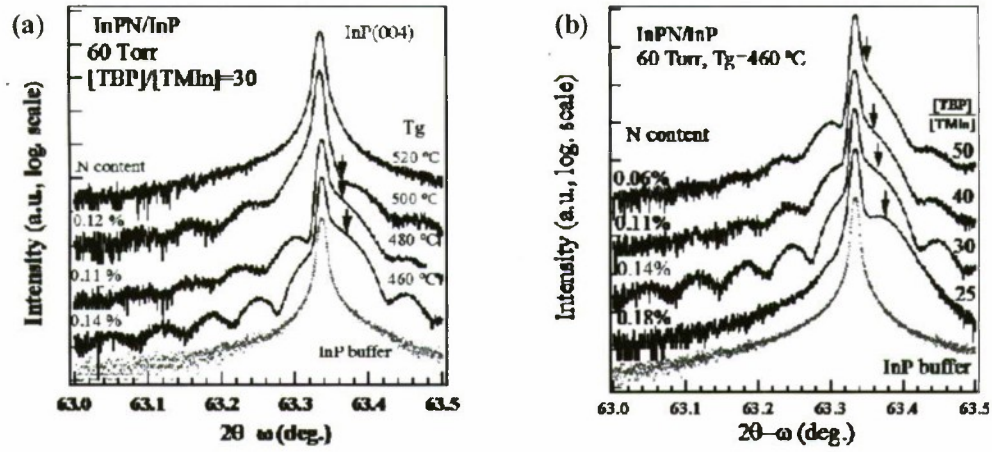

Fig. 2 (004) 2θ-ω HR-XRD profiles for the InPN films on InP (001) substrates grown at (a) different growth temperatures 460-520 °C with the fixed [TBP]/[TMIn] ratio of 30, and at (b) 460 °C with different [TBP]/[TMIn] ratios 25-50. The diffraction from the InPN films is designated with arrows.

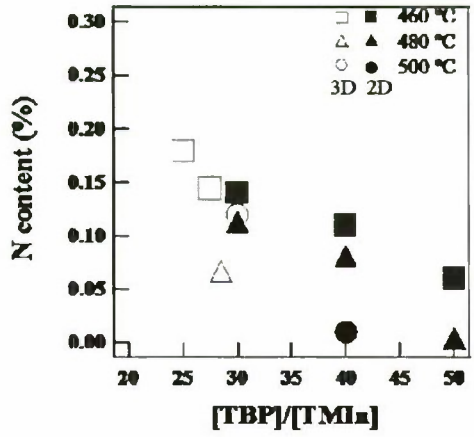

Fig. 3 N concentrations in the InPN films as dependent on the [TBP]/[TMIn] ratio and the growth temperature, estimated from fitting the 2θ-ω (004) HRXRD profiles with the dynamic simulation .

indicating the In transport limited growth. The estimated N concentrations are as low as below 0.2% from fitting the XRD profiles with those calculated by the dynamic simulation. The effects of the [TBP]/[TMIn] ratio and the growth temperature on the N incorporation are collectively shown in Fig. 3. The highest N concentration is 0.18% with the growth temperature of 460°C and the [TBP]/[TMIn] ratio of 25, though it is attained in the 3D growth regime. Within the 2D growth regime, the highest N concentration is 0.14% with the growth temperature of 460°C and the [TBP]/[TMIn] ratio of 30. The whole N incorporation behavior suggests that a lower growth temperature and an optimum [TBP]/[TMIn] ratio are the key factors for obtaining the higher N concentrations in the InPN films.

Fig. 4 shows the (115) XRD reciprocal space mappings of the InP(001) substrate and the InPN films with different N concentrations grown at 460°C with respective [TBP]/[TMIn] ratios. The zeros of Δ2θ-ω and Δω are taken at the (115) diffraction peak from the substrate. The dashed lines through the (115) diffraction peak and shoulder which inclines against the Δ2θ-ω axis indicate that the InPN films are coherently grown without lattice relaxation irrespective of 2D or 3D growth. The estimated N concentrations are consistent with those from the XRD dynamic simulation.

IV. Conclusions

Dilute-nitride alloy InPN films have been grown by MOVPE. The 2D growths with atomically flat surfaces are obtained at 460-500°C with relatively high P supplies with fixed In and N supplies. The N incorporation increases for lower growth temperatures and higher N/P ratios. The N concentrations up to 0.14% have been obtained within the 2D growth regime. The maximum N concentration of 0.18% has been attained within the 3D growth regime. The 150-170 nm-thick InPN

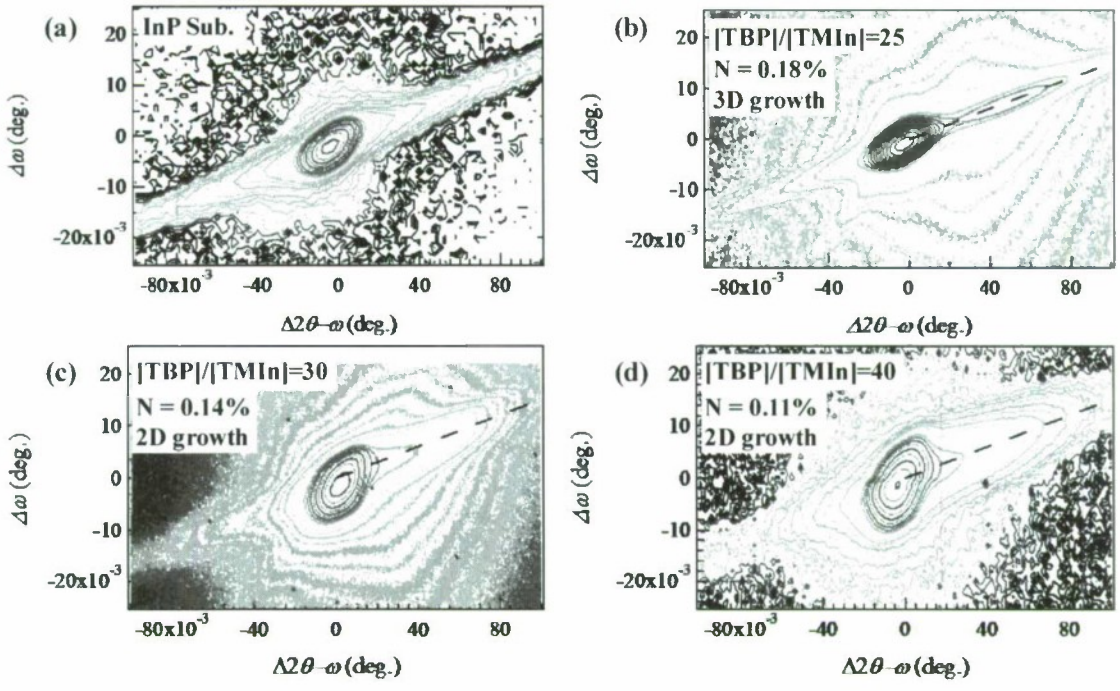

Fig. 4 (115) XRD reciprocal space mappings of (a) InP (001) substrates, and (b), (c), (d) InPN films with different N concentrations grown with respective [TBP]/[TMIn] supply ratios.

films are coherently grown on InP(001) without lattice relaxation irrespective of 2D or 3D growth.

Acknowlegment

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Reduction of Surface Roughness of GaP on Si Substrate using Strained GaInP Interlayer by MOCVD

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Abstract

Epitaxial growth of GaP on a Si substrate with a GaInP interlayer by a low-pressure metalorganic chemical vapor deposition were investigated using the atomic force microscopy. The surface roughness Ra was decreased from 2.7 nm to 1.3 nm by only inserting the GaInP interlayer under the 600°C. The GaP layer using the GaInP interlayer was optimized under various growth temperature between 500°C and 650°C. The surface roughness Ra was drastically decreased to 0.5 nm when both the GaP and the GaInP interlayer was grown at 550°C.

I. INTRODUCTION

Photonic devices on Si substrates have been attracting much interest, because they will become a key technology of the optical interconnection for achieving high speed information processing, and of realization of high functional sensing system. Efficient emission from light sources on Si is highly demanded to realize such advanced photonic systems. Since Si is unsuitable as an active emitting material due to its indirect bandgap, it is important to form high quality III-V based devices on the Si substrate. The best solution is direct growth of III-V- materials on Si for both efficient fabrication process and easy development of various applications. Whereas there have been numerous studies on the growth of GaAs and InP on Si, high density threading dislocations which were induced due to the large lattice mismatch were critical problem. Thus a lattice-matched GaPN on a Si substrate is attractive for making photonic devices [1]. A GaP layer on the Si substrate is needed as a buffer layer to avoid formation of a large number of defects which appears in case of the direct growth of a GaPN layer on Si [2]. Thus the detailed investigation of the epitaxial growth of the GaP layer on Si is remarkably important.

In this study, MOCVD grown GaP buffer layers on Si with a thin GaInP interlayer were investigated to achieve a small roughness of the GaP surface, focusing on the dependence on the indium composition, the number of the GaInP interlayer, and the growth temperature.

II. EXPERIMENT

All samples were grown on an n-Si (100) 4° off to (011) direction substrate using a low pressure MOCVD. Tertiarybutylphosphine (TBP), triethylgallium (TEGa) and trimethylindium (TMIn) were used as source precursors. The surface of Si was etched by BHF solutions under room temperature and then the Si substrate was loaded into the MOCVD chamber. After thermal cleaning at 750°C under the TBP supply, at first a 15-nm-thick low-temperature GaP buffer layer was grown under the growth temperature of 400°C, the growth rate of 1.5 μm/h, and the V/III ratio of 36. Following it, a 20-nm-thick high-temperature GaP buffer layer was grown under the growth temperature of 600°C. These growth conditions of GaP layers were optimized from preliminary studies of using only GaP materials. A 3-nm-thick GaInP interlayer was grown on the high-temperature GaP layer under the same growth temperature. The indium compositions of GaInP were from 3% to 20% and the numbers of GaInP interlayer were from 1 to 3. In case of the multilayer GaInP, 10-nm-thick GaP layers were grown between GaInP layers. Lastly, a 200-nm-thick high-temperature GaP layer was grown for clear observation of the surface morphology by atomic-force-microscopy (AFM), though the total thickness was exceeding a critical thickness of GaP on Si. Figure 1 shows a schematic structure of the GaP buffer layer with a GaInP interlayer on a Si substrate. The surface morphology of the GaP buffer layer is important because the smooth

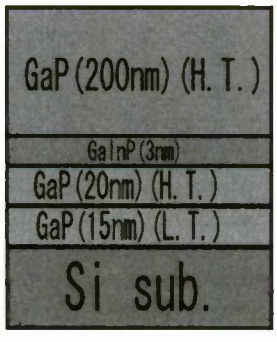

Fig. 1 Grown structure of the GaP buffer layer with a GaInP interlayer on a Si substrate.

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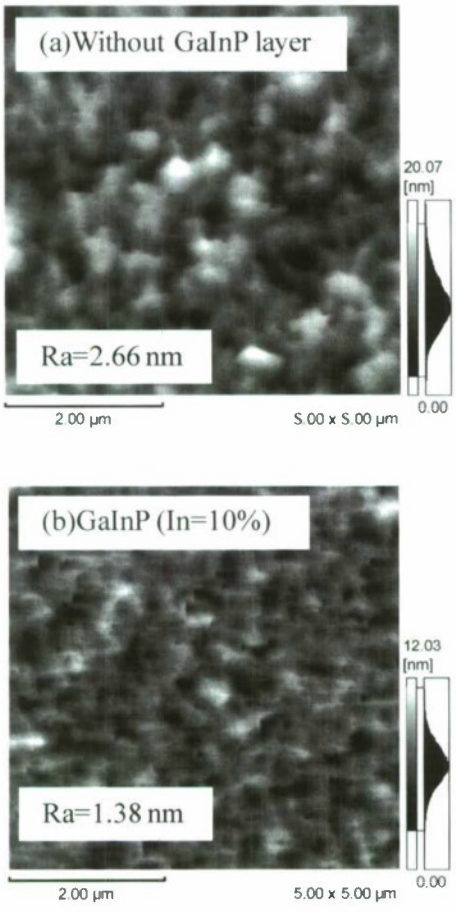

Fig. 2 AFM images of GaP (a) without a GaInP layer and (b) with a GaInP interlayer of In=10%.

surface of the GaP buffer layer is needed for smooth growth in the following GaNP layer. The AFM measurements for examining the surface roughness as the arithmetical mean roughness Ra were carried out.

III. RESULTS AND DISCUSSION

A. Dependence on indium composition of GaInP interlayer

The growth of GaP buffer layer with GaInP interlayer on a Si substrate is discussed. Figures 2 shows 5μm square area of the surface morphology of the GaP layer with and without the GaInP interlayer. From the Fig. 2(a) for the GaP layer without a GaInP interlayer, the roughness Ra was 2.7 nm. This roughness was observed by the result of optimization of the growth conditions for 2-layer structure which consists of both the bottom low growth temperature GaP and upper high growth temperature GaP structure. Figure 2(b) shows the surface morphology of GaP with a GaInP interlayer with the indium composition of 10%. The Ra was reduced to 1.3 nm which is almost half of optimized result for a sample without GaInP. This result shows that the insertion of a thin GaInP interlayer was effective to decrease the surface roughness of the GaP buffer layer on the Si substrate. The large roughness of GaP without the GaInP interlayer is mainly due to the antiphase domain and the deep pits

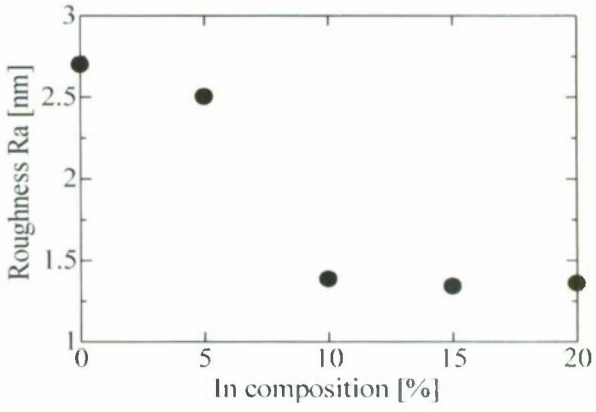

Fig. 3 Roughness Ra dependence on indium composition of GaInP interlayer. The thickness of GaInP was fixed at 3 nm.

generated from the Si-GaP interface confirmed by the TEM image (not shown in this paper). The improvement using the GaInP interlayer might be caused by the superlattice buffer and strained layer buffer effect. Both the existence of the interface and the strain of the layer changed the growth mode slightly and it broadened the area of the specific phase and buried the pits.

Figure 3 shows the Ra dependence on the indium composition of the GaInP interlayer. The In composition of the GaInP interlayer was from 5% to 20% and the thickness of GaInP was fixed at 3 nm. Decrease in the Ra from 2.5 nm to 1.3 nm was observed by increasing the indium composition. However the effect of planarization was saturated by increasing In composition. In case of the indium composition of 10% or more, the Ra was almost constant at 1.3 nm.

B. Dependence on the number of GaInP interlayer

Figures 4 show the surface morphology of GaP with multi GaInP layers. Figure 4(a) shows the surface morphology of GaP with the three-layer GaInP interlayer of indium composition of 3%. The Ra was decreased to 1.3 nm in comparison with that of a single GaInP layer as shown in Fig. 3. This result shows that the multilayer GaInP was effective to decrease the surface roughness of the GaP buffer layer on the Si substrate. Figure 4(b) shows the surface morphology of GaP with the three-layer GaInP interlayer of indium composition of 10%. Large 3-dimensinal structures appeared, and the Ra was increased to 37 nm. The In composition of 10% was enough to reduce down to the saturation Ra for a single GaInP layer. Thus, the result for the multilayer sample is attributed to the strain accumulation induced 3-dimensional growth.

Figure 5 shows the summary of the surface roughness dependence on the indium composition and on the number of the GaInP interlayer. The Ra for a single GaInP interlayer is the same data as Fig. 3. In case of the small indium composition of 3% and 5%, the Ra was down to 1.3 nm by using the multilayer GaInP. This Ra is almost equal to the case of single GaInP interlayer of In=10%, 15%, and 20%. The improvement effect of the multi GaInP interlayer is

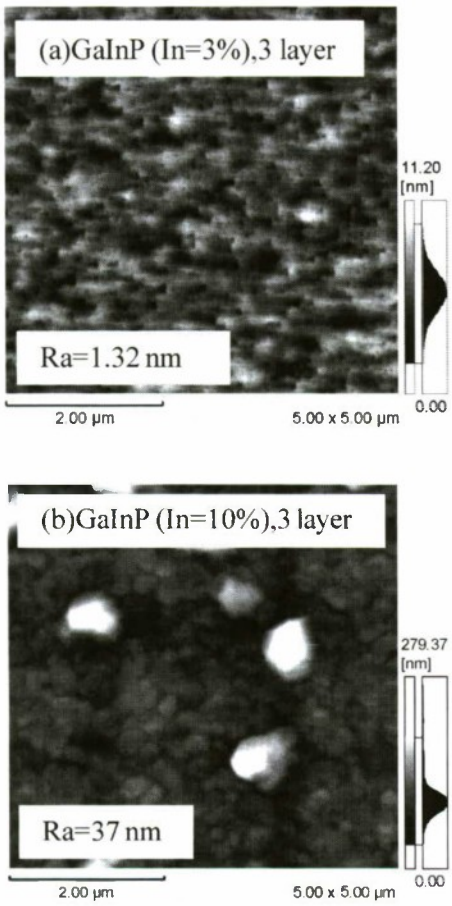

Fig. 4 AFM images of GaP with 3-layer GaInP interlayer with indium composition of (a) 3% and (b) 10%.

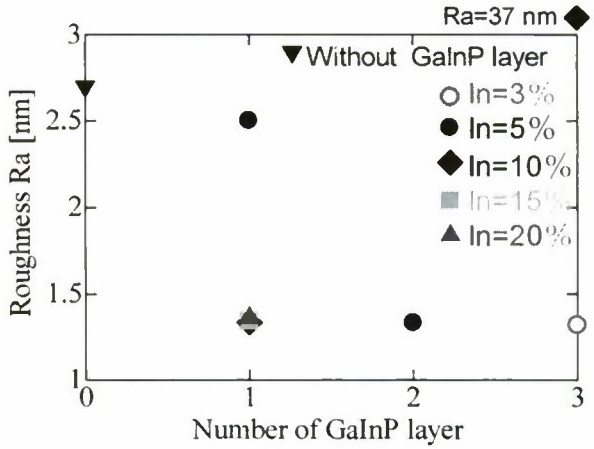

Fig. 5 Ra dependence on numbers of the GaInP interlayer.

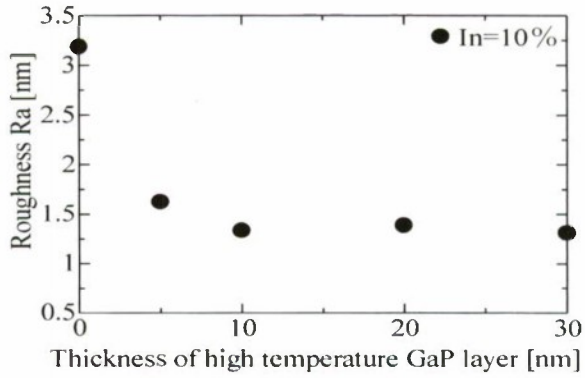

Fig. 6 Ra dependence on thickness of the high temperature GaP layer.

certainly confirmed from the Fig. 4 in case of In=5%, however the effect was almost the same as as optimized single GaInP layer.

C. Dependence on thickness of high temperature GaP layer under the GaInP interlayer

The samples discussed above had the 20 nm thick high temperature layer GaP below the GaInP layer. The thickness was varied from 0 nm to 30 nm to confirm the influence of the thickness below the GaInP layer. Figure 6 shows the relationship between the roughness Ra and the thickness of the high temperature GaP layer below the GaInP layer. As a result of this experiment, the surface roughness Ra was almost constant value of 1.5nm in the case of the thickness of the high temperature GaP layer from 5 nm to 30 nm. It was confirmed that the influence on the surface roughness of the GaP thickness below the GaInP layer was small. As a result, we obtained almost equal roughness Ra with thinner thickness of a high temperature GaP layer. However, in the case of the thickness of the high temperature GaP layer of 0 nm, the Ra was increased to 3.2 nm.

D. Dependence on growth temperature of Ga(In)P layer

Above samples were grown under the fixed temperature of 600°C which was optimized for the GaP structure without GaInP. In next, The growth temperature of both the high temperature GaP layer and the GaInP interlayer were varied from 500°C to 650°C. The last 200nm GaInP layer was grown under the same growth temperature of GaInP.

Figures 7 show the surface morphology of GaP grown under the different temperatures of 500°C and 550°C. The In composition of the GaInP interlayer was 5%. The surface roughness Ra was 8.95 nm and 0.51 nm, respectively.

Figure 8 shows the relationship between the roughness Ra of the GaP layer and the growth temperature of the high temperature GaP layer and GaInP interlayer. From the figure, the minimum Ra of 0.5 nm was achieved at the growth temperature of 550°C. In contrast, the roughness Ra at 500°C increased to 8 nm. It might be because that 3-dimensional growth was enhanced by suppressed adatom migration on the rough surface of the low temperature GaP layer. On the other hand, in the case of 650°C, roughness Ra increased to 6 nm. It might be because that 3-dimensional growth of the strained GaInP layer was progressed by enhanced migration of adatoms. From these result, the smallest surface roughness Ra of 0.5 nm was achieved by optimization of the growth temperature of high temperature GaP layer and GaInP interlayer.

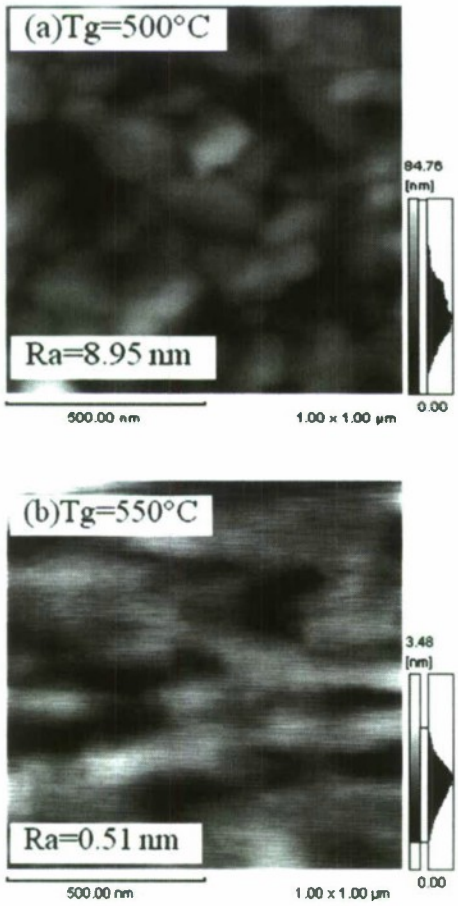

Fig. 7 AFM images of GaP with GaInP interlayer grown under the temperature of (a) 500°C and (b) 550°C.

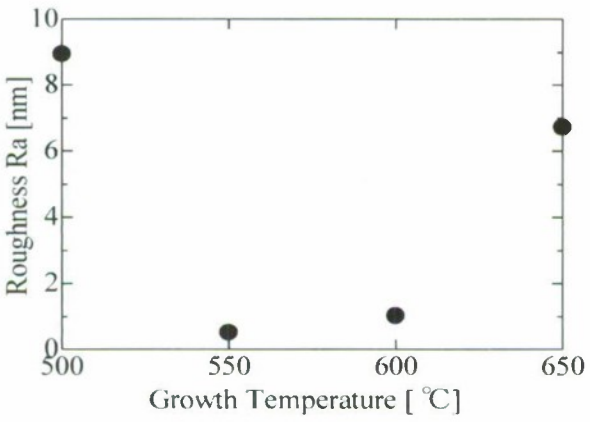

Fig. 8 Dependence of growth temperature both of GaP and GaInP layer.

In this experiment, the growth temperature was kept through the growth of the high temperature GaP , GaInP, and top GaP layers. Thus it is unclear which layer improves the roughness by the optimization of growth temperature. The detailed study will improve the surface roughness further.

IV. CONCLUSION

In conclusion, we investigated the GaP growth on a Si substrate using a thin GaInP interlayer by the MOCVD. The surface roughness was decreased from 2.7 nm to 1.3 nm using the GaInP interlayer under 600C. It is shown that the GaInP interlayer is effective to decrease the surface roughness. Furthermore, the smallest surface roughness Ra of 0.5 nm was achieved by optimization of the growth temperature. The small roughness of the GaP buffer layer with a thin layer thickness is helpful to grow a high quality GaNP lattice matching layer to the Si and effective for various design of photonic devices.

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SELECTIVE AREA GROWTH OF InP ON NANO-PATTERNED SiO_2/Si(100) SUBSTRATES BY MOLECULAR BEAM EPITAXY

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Abstract

We have investigated the selective area growth of InP on nano-patterned Si substrates with SiO_2 mask by molecular beam epitaxy. By optimizing the growth conditions, the growth of one separate InP single crystallite for each Si opening has been accomplished. It is found that when single crystallites coalesced into larger grains beyond Si openings, lattice strains were introduced in the grains because of the difference in thermal expansion coefficient between Si and InP. This clearly shows that the growth of one InP single crystallite for each Si opening is indispensable for growing stress- and defect-free InP regions on SiO_2 towards the application to next generation MOSFETs as the channel materials.

I. Introduction

Recently, research works aimed at the improvement of the drift mobility in CMOS channel part have actively been carried out. In this regard, *n*-MOSFETs having III-V materials in the channel part are gaining much attention owing to their higher electron mobility, as compared to Si [1]. The crystalline growth of III-V compound semiconductors on SiO_2 is essential for this issue. It is, however, difficult to grow III-V materials directly on SiO_2 hence selective area growth is being employed. In the selective area growth, the growth area is limited by using SiO_2 as mask and growing up the desired III-V material on Si selectively. After that, growth extends over the mask edges as epitaxial lateral overgrowth.

Among III-V compound semiconductors, InP is one of the most promising materials for high-speed electronic and optical devices for optical communications. There are, however, serious problems to overcome, such as large mismatches in lattice constant and thermal expansion coefficient with Si. It has been reported that successful heteroepitaxy of InP on Si has usually been achieved by inserting thin GaAs [2], InP/GaAs [3] or InAsP/InP superlattice [4] layer as an intermediate buffer layer. Especially, lattice strain increases with increasing growth area in the heteroepitaxy [5].

From the viewpoint of achieving defect-free III–V semiconductors on Si substrates, the selective area growth followed by lateral overgrowth is also one of promising methods since reducing growth area of III–V semiconductors effectively decreases lattice strain due to large mismatch in lattice constant and thermal expansion coefficient between Si and III-V materials [6]. Based on the viewpoint, we have investigated the selective area growth of InP on Si(100) substrates with SiO_2 mask by molecular-beam epitaxy (MBE).

In this presentation, we will report on the growth of one separate InP single crystallite for each Si opening by reducing the size of Si openings of substrates.

II. Experimental procedure

Two types of patterned Si substrates were used in this study: one is a nano-patterned substrate and the other a micro-patterned one. The nano-patterned substrates consisting of Si openings (400 nm square) and SiO_2 masks were fabricated on SiO_2/Si(100) substrates by using nanoimprint lithography, reactive ion etching (RIE), and wet etching techniques. At the first step of fabricating the nano-patterned SiO_2/Si(100) substrates, nano-sized resist pillars (400 nm square spaced 400 nm) were made on Si(100) substrates covered with SiO_2 400 nm thick by nanoimprint lithography, and SiO_2 was deposited by electron beam deposition. The nano-pillars were removed by acetone, and the resultant nano-patterns of SiO_2 were formed on the substrates. At the second step, Si oxide etching was performed on the substrates by CHF_3 RIE to reduce the thickness of SiO_2 layers. Finally, the remaining SiO_2 around 10 nm thick was wet-etched by a dilute HF solution to form Si openings (400 nm square). This process is important to fabricate damage-free Si openings. The micro-patterned substrates consisting of Si openings (10 μm square spaced 10μm) and SiO_2 masks were fabricated on SiO_2/Si(100) substrates by conventional photolithography, RIE and wet etching techniques mentioned above.

MBE growth of InP was carried out on the nano-

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and micro-patterned substrates using thermally cracked PH_3 and elemental In as group V and III sources, respectively. Prior to MBE growth, HF wet etching was carried out to remove the native silicon oxides on the Si opening surfaces and to leave H-terminated surfaces.

III. Results and discussion

Figure 1 shows scanning electron microscopy (SEM) images of InP grown on the micro-patterned substrates (10 μm square spaced 10 μm; sample A) and nano-patterned substrates (400 nm square spaced 400 nm; samples B and C) at the growth temperature of 515 °C. It can be seen that at this growth temperature, InP does not grow on the SiO_2 masks while InP does grow on the Si openings for all the three samples. This means that the selective area growth of InP can be achieved regardless of the size of the patterned areas. For the micro-patterned substrates (sample A), however, a lot of InP crystallites are grown in every micro-patterned Si opening (Fig. 1(a)). As a result, most of crystallites coalesce to form much larger grains. On the other hand, it is found that for the nano-patterned substrates, one single crystallite for each nano-patterned opening is grown as shown in Fig. 1(b) (hereafter indicated sample B). This result is readily understood in terms of the result that InP crystallites are around 400 nm in diameter at the present growth condition regardless of the size of Si openings (see Figs. 1(a) and 1(b)). With increasing the coverage of InP (sample C), the crystallites become large and some crystallites coalesce into much larger grains over the SiO_2 mask region, as shown in Fig. 1(c).

The coalescence of InP single crystallites neighbored on each other can introduce some strain in the grains after the MBE growth due to the difference in thermal expansion coefficient between Si and InP. Figures 2 (a) and (b) show high-resolution X-ray diffraction (HR-XRD) ω-2θ profiles for sample B consisting of individual InP single crystallites and sample C consisting of much larger InP grains formed by the coalescence of single crystallites neighbored on each other, respectively. From the (400) peaks, values of the spacing between the (400) planes for samples B and C are calculated as 1.4681 Å and 1.4648 Å, respectively. Compared with the corresponding value of bulk InP (1.4672 Å), it can be seen that individual InP single crystallites formed in sample B, as shown in Fig. 1(b), have almost the same spacing between the (400) planes as bulk InP has. In contrast, much larger InP grains formed by the coalescence of single crystallites (sample C), as shown in Fig. 1(c), have smaller spacing between (400) planes than that of bulk InP, indicating the presence of tensile strains in the grains. Judging both from the occurrence of the coalescence and from the difference in thermal expansion coefficient between Si (2.4×10^{-6} K^{-1}) and InP (4.5×10^{-6} K^{-1}), the tensile stress is considered to be caused by lowering the substrate

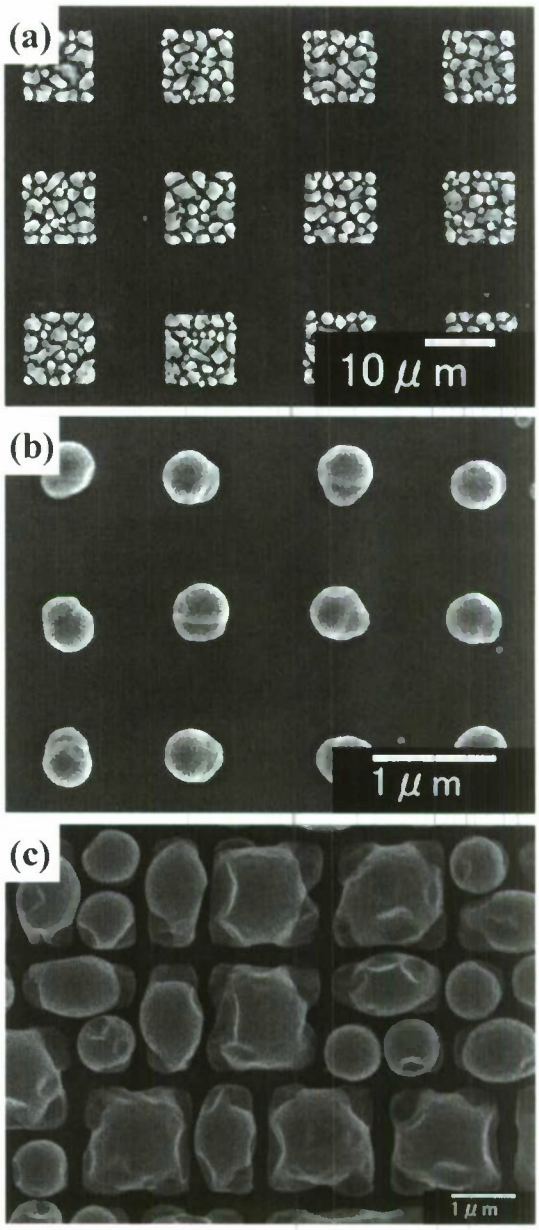

Fig.1. SEM images of InP grown on patterned Si substrates with SiO_2 mask regions. (a) micro-patterned (10 μm x 10 μm) SiO_2/Si substrate. (b) and (c) nano-patterned (400 nm x 400 nm) SiO_2/Si substrates. In (c), some srystallites coalesce into larger grains over Si openings.

temperature after the growth. We also notice that the (400) peak of sample C is much broader than that of sample B. This result is consistent with the SEM observation revealing that sample C contains not only separate single crystallites but larger grains formed by the coalescence of two or four single crystallites neighbored on each other, as shown in Fig. 1(c). It is considered that tensile strain in the grains produced by the thermal expansion coefficient difference depends on the size of grains. The (400) diffraction peak becomes broader as a result of the variation of the lattice spacing

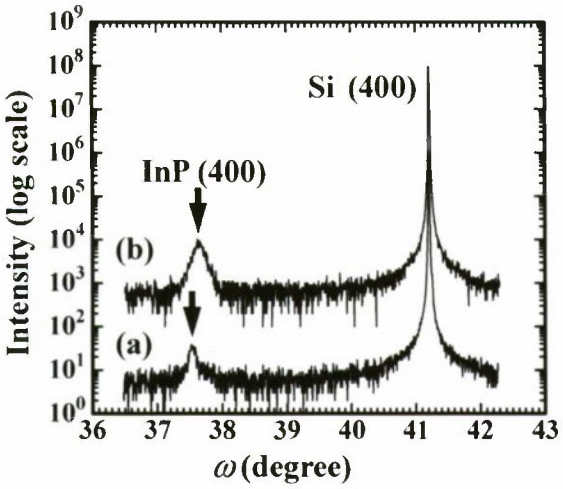

Fig. 2. HR-XRD ω-2θ profiles for InP grown on nano-patterned (400 x 400 nm^2) SiO_2/Si substrates. (a) No coalescence beyond openings takes place (Fig. 1(b)). (b) Some single crystallites coalesce into larger grains over Si openings (Fig. 1(c)).

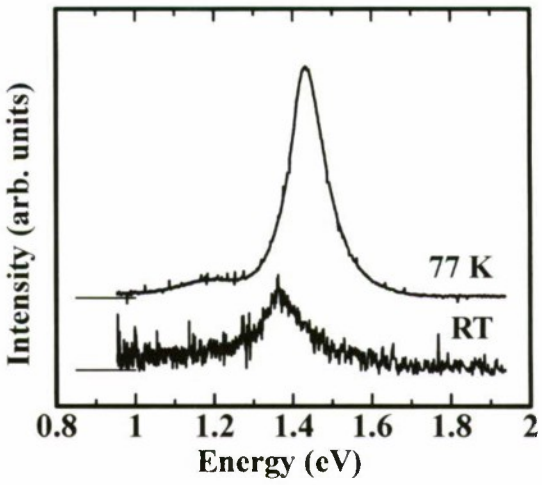

Fig. 3. Photoluminescence spectra taken for the sample consisting of separate single crystallites formed in Si openings (Fig. 1(b)).

in the grains. This clearly shows that the growth of one InP single crystallite for each Si opening is indispensable for growing stress- and defect-free InP regions on SiO_2.

Next, photoluminescence (PL) measurement for samples A and B was carried out. For sample A, i.e. InP grains grown on the micro-patterned substrate, no PL emission was observed. In contrast, for separate InP single crystallites grown on the nano-patterned substrate (sample B), PL emission lines are observed even at RT as shown in Fig. 3. The PL peaks at RT and 77 K are considered to be due to a band-to-band (B-B) transition [8]. The RT PL spectrum exhibits a broad peak located slightly above the intrinsic bandgap energy (1.35 eV) [9]. The value of the full width at half maximum (FWHM) of the peak is around 120 meV. When decreasing temperature to 77 K, a broad and strong luminescence line is observed at around 1.433 eV although the FWHM becomes slightly narrow compared with the FWHM at RT. The peak energy of 1.433 eV at 77 K is also larger than the intrinsic bandgap energy of 1.412 eV. This dominant feature of the PL spectra, *i.e.* the broadening of the B-B transition peak and the accompanying blue shift, is explained in terms of the Burstein-Moss effect. Figure 4 shows μ-PL spectra taken for different separate single crystallites of sample B at RT. The PL peaks are located in energy above the intrinsic bandgap (1.35 eV) and are still rather broad although the values of their FWHM (~ 80 meV) are slightly smaller than that for the macro-PL peak. These results provide the evidence that separate single crystallites of sample B exhibit PL emission lines with peak energy above the intrinsic bandgap and broad FWHM because of the Burstein-Moss effect. From the values of FWHM of the μ-PL peaks, we can estimate the carrier concentration as ~$3x10^{18}$ cm^{-3} [9]. It is thought that such high carrier concentration comes from auto-doping of Si from Si substrate during high

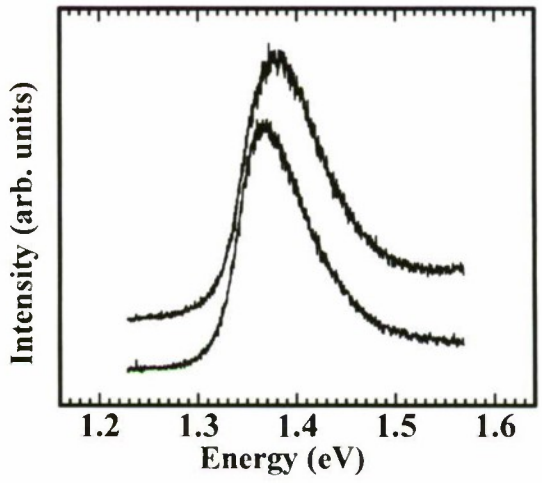

Fig. 4. Micro-photoluminescence spectra taken from different separate single crystallites of sample B.

temperature growth of InP on Si.

Finally, we have investigated the lateral overgrowth of InP on the SiO_2 mask region using separate single crystallites formed in the Si openings. A preliminary result indicates that it is possible to grow InP laterally on the SiO_2 mask region. Unfortunately, since the spacing between the Si openings of the patterned substrates used in this study is narrow, InP regions formed by lateral overgrowth coalesce and the resultant larger grains contain many defects. To avoid such coalescence, lateral overgrowth of InP on nano-patterned substrates with larger spacing between Si openings is in progress.

IV. Summary

We have investigated the selective area growth of

InP on nano-patterned Si substrates with SiO_2 mask. By optimizing the growth conditions, the growth of one separate InP single crystallite for each Si opening was accomplished. It was found that when InP single crystallites coalesced into larger grains, lattice strains were introduced in the grains because of the difference in thermal expansion coefficient between Si and InP. This clearly shows that the growth of one separate InP single crystallite for each Si opening is indispensable for growing stress- and defect-free InP regions on SiO_2 towards the application to next generation MOSFETs as the channel materials.

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Heteroepitaxial Growth of Indium Phosphide from Nano-openings Made by Masking on a Si(001) Wafer

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We investigate nano-cptiaxial lateral overgrowth (NELOG) of InP from the nano-sized openings on a seed layer on the silicon wafer, by Hydride Vapor Phase Epitaxy (HVPE). The grown layers were analyzed by cathodoluminescence (CL) *in situ* a scanning electron microscope (SEM) and transmission electron microscopy (TEM). The results from InP:S growth shows that the boundary plane of the grown layer has a major impact on the luminescence, indicating preferential orientation-dependent doping. Moreover, although there is clear evidence that most of the threading dislocations originating in the InP seed layer/Si interface are blocked by the mask, it appears that new dislocations are generated. Some of these dislocations are bounding planar defects such as stacking faults, possibly generated by unevenness in the mask. Finally, patterns where coalescence takes place at higher thickness seem to result in a rougher surface.

Key words:- ELOG, heteroepitaxy, HVPE, CL, TEM, InP/Si, dislocations.

I. Introduction

Integrating III-V materials on silicon and silicon-on-insulator for realization of optical interconnects, integration with microelectronics, optical networking, imaging and disposable photonics for medical applications remains equally interesting and challenging. Advances in photonic materials, structures and technologies are main ingredients of this pursuit. The growth of III-V heteroepitaxial layers on silicon substrate is attractive because of its possible application for monolithically integrated electronic and optoelectronic devices. On one hand, active optical devices are feasible with III–V compound semiconductors. On the other hand, silicon-based complementary metal oxide (CMOS) technology has been continuously advancing in the pursuit of low-cost, high-performance electronic devices (1) but is soon facing the physical limitation of metallic electrical interconnects in terms of transmission capacity and energy dissipation. One of the proposed solutions is the merging of electronics and photonics into an integrated platform using the existing silicon infrastructure which in essence is the goal of silicon photonics (2).

The InP(001)/Si(001) system represents a particularly interesting candidate for silicon photonics. Heteroepitaxial growth of InP on silicon is, however, associated with a number of challenges due to its large lattice mismatch (8%) and large difference in thermal expansion coefficient (~50%) (3) with the Si. Selective epitaxy and epitaxy on patterned substrates offer new possibilities to modify the structural, optical and electrical properties of epitaxial layers, in particular in the case of hetroepitaxy (4). This option for InP/Si is proved to be successful through the use of epitaxial lateral overgrowth (ELOG) by hydride vapor phase epitaxy (HVPE) in our group (5). In this work, ELOG of InP/Si on patterns consisting of net-type and line openings was conducted. Cathodoluminescence (CL), atomic force microscopy (AFM) and transmission electron microscopy (TEM) studies have been made on the grown layer, to study the effect of boundary plane and the formation of defects in the region of coalescence.

II. Experimental

Two samples (A and B) of n-Si(100) misoriented 4° off toward [111] with a thin (~1.5 μm) seed layer of InP were used in the ELOG experiments. Line and net type openings on Sample A and only net type openings on sample B were then made on ~40 nm thick SiO_2 mask deposited by plasma enhanced chemical vapor deposition with e-beam lithography and conventional dry etching techniques (5). The samples have patterns as shown in Fig. 1. Their description and growth parameters are summarized in Table 1. The patterns were contained in the fields of different sizes. The regions outside the fields were covered with silicon dioxide. Sulphur-doped and unintentionally doped InP was grown on sample A and sample B, respectively in an Aixtron HVPE system with PH_3 and InCl as precursors at a total pressure of 20 mbar. More growth details are described in Table 1.

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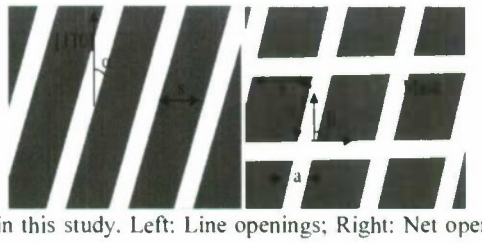

Figure 1. Schematic of the patterns used in this study. Left: Line openings; Right: Net openings. Their details are given in Table 1.

Table 1. Summary of sample description and growth parameters

Sample	Temperature (^{0}C)	Opening type, orientation (deg) and separation between the openings (s)	Field size (x 10^4 μm^2)	Doping	III/V	Growth time (min:sec)
A	610	Lines with α =15 and 30 s = 3 μm	4, 8, 12, 16	Sulphur (nominal conc. = 2 x 10^{18} cm^{-3})	5 (InCl = 0.56 mbar)	9:00
		Net openings with α = 15, β = 105 & α = 15, β = 120 s = 3 μm	4, 8, 12, 16			
B	615	Net openings with α = 15, β = 105 & α = 15, β = 120 s = 3 μm	4, 8, 12, 16	Unintentional (~1 x 10^{15} cm^{-3})	10 (InCl = 0.28 mbar)	2:15

III. Results and discussion

The thickness of the InP epitaxial layer grown over the oxide mask was measured for each of the field sizes on sample A for both types of patterns using a profilometer and the results are displayed in the form of growth rate vs. field size in Fig. 2. For the line openings, the growth rate of the layer shows a decreasing tendency with respect to the field size (the area over which the openings lay) irrespective of the orientation of the openings. However, the growth rate of the layer grown from line openings which are oriented at $\alpha = 15^0$ is larger than the ones at $\alpha = 30^0$ regardless of the field size. On the contrary, the growth rate of the overgrown layer from the net opening patterns seems to increase with the field size mostly for the sizes beyond 8 x 10^4 μm^2 regardless of β. While comparing the two types of openings, net type openings exhibit larger growth rate regardless of the orientation and the field size. This is because in the latter case, coalescence occurs from four corners, which is absent in the patterns of line openings. In the case of net openings, coalescence occurs rapidly from four corners corresponding to the junction points of the net openings that constitute the pattern unit cell. In this case, no typical boundary planes are formed before coalescence takes place, and after coalescence the surface of the layer generally becomes parallel to the (001) plane. This, however, is not the case with the line openings where the slow growing low index boundary planes of the formed islands do not lead to quick planarization. The reason for the decrease in the growth rate in the case of line openings and increase in the net type openings as the field size increases is not fully understood and needs further investigation.

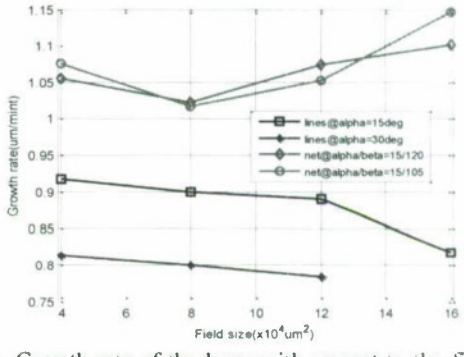

Fig. 2. Growth rate of the layer with respect to the field size of the patterns on sample A for different orientations of the line and net type openings with respect to the [110] direction.

The surface morphology of the grown layer was characterized by AFM from a 45 x 45 μm^2 scan window. The root mean square (RMS) roughness was obtained (Table 2). The results show that the net type openings result in a better surface morphology of the grown layer. The surface morphology of an ELOG layer depends to some extent on how thick the sample is, confirming results from previous studies (6). The AFM characterization was done for all the field sizes on sample A and there is little difference on the surface roughness of the respective grown layer as the field size varies.

Cathodoluminescence studies of the epitaxial layer were made at room temperature with an acceleration voltage of 9 kV. Figure 3 summarizes the CL and SEM results. Fig. 3a shows the panchromatic image of the immaturely grown islands

along the line openings of sample A; Fig. 3b that of the coalesced region; Fig. 3c is the CL spectra for the regions marked 1 and 2 in Fig. 3a and 3 in Fig. 3b. Fig. 3d is the SEM view of the sample of Fig. 3a after subjecting it to Hubert's etchant ($1HBr:2H_3PO_4$) (7) for 20 s at room temperature. In places where less mature growth was obtained, the CL mapping (Fig. 3a) showed that the growth starts by forming small islands along the line openings, which later on will coalesce and form the layer. These islands give strong CL intensity compared to the fully coalesced region (Fig. 3b). This indicates that coalescence may generate certain defects. The contrast in the CL image (see Fig. 3b,) is governed by the ratio between the radiative to nonradiative recombination rates. The "dark" spot areas in the CL images correspond to areas where the non-radiative recombination, usually around an extended defect, is dominant over the radiative recombination. These spots are threading dislocations as reported in literature (8) . They were quantified by counting the black spots and dividing the number by the total scan area. Although there is a one- to- one correspondence between black spots and the threading dislocations, as the dislocations tend to cluster, it is difficult to assess the exact number of dislocations in a broader dark area. However, the analysis was made by assuming that a dislocation corresponds to a dark spot with a diameter of ca 1 μm. Since the hole diffusion constant is 5 cm^2s^{-1} and the measured minority carrier life time in our material is ~0.2 x 10^{-9} s, the diffusion length is ~ (1 x 10^{-9} $cm^2)^{1/2}$, which is ~0.3 μm. This value is within the radius of the spot considered here. There is no larger difference in dislocation density with respect to the pattern, but the dislocation density is slightly lower in layers grown from line openings than in those grown from net openings. The coalesced regions from both types of patterns give threading dislocation density of the same order of magnitude. Table 2 summarizes the results from the CL measurement and AFM surface characterization.

Table 2. Threading dislocation density of the ELOG layer of both net type and line openings of sample A estimated from the CL panchromatic image and RMS surface roughness obtained from AFM.

Patterns of sample A	Threading dislocation density (cm^{-2})	RMS Surface roughness (nm)
Net, α =15°, β =105°	3.9 x 10^7	35
Net, α =15°, β =120°	3.4 x 10^7	48
Lines α = 15°,	2.3 x 10^7	106
Lines α = 30°,	2.6 x 10^7	93

The line defects that are probably threading dislocations can be seen lying in the boundary plane of the islands, and in the se of the smaller island, it appears that the threading dislocation lie at the edge of a planar defect that could be a stacking fault or microtwin (Fig. 3d). While considering the CL spectra (Fig. 3c), which is the intensity at the three specified regions as mentioned above, the intensity of region 2 is very weak compared to those of regions 1 and 3. There is a slight shift in the peak of the CL spectrum from the region 1 compared to those at 2 and 3, the side wall of the island and where the complete coalescence has occurred, respectively, towards a shorter wavelength. This shift could be due to unrelaxed strain, or it could be due to the Burstein- Moss effect, which occurs in doped semiconductors due to the filling of states at the bottom of the band minima as the doping level increases. Since the thermal expansion coefficient of the silicon dioxide mask is smaller than that of InP, the grown ELOG InP would experience a tensile strain. If this strain is operative, it would introduce a shift to longer rather than shorter wavelengths. It thus seems more likely that the shift is due to the Burstein-Moss effect caused by doping enrichment. This also explains why some boundary planes of the islands appear dark, since the boundary plane direction is known to influence doping concentration. Orientation dependent doping has resulted in lower intensity for region 2 (9).

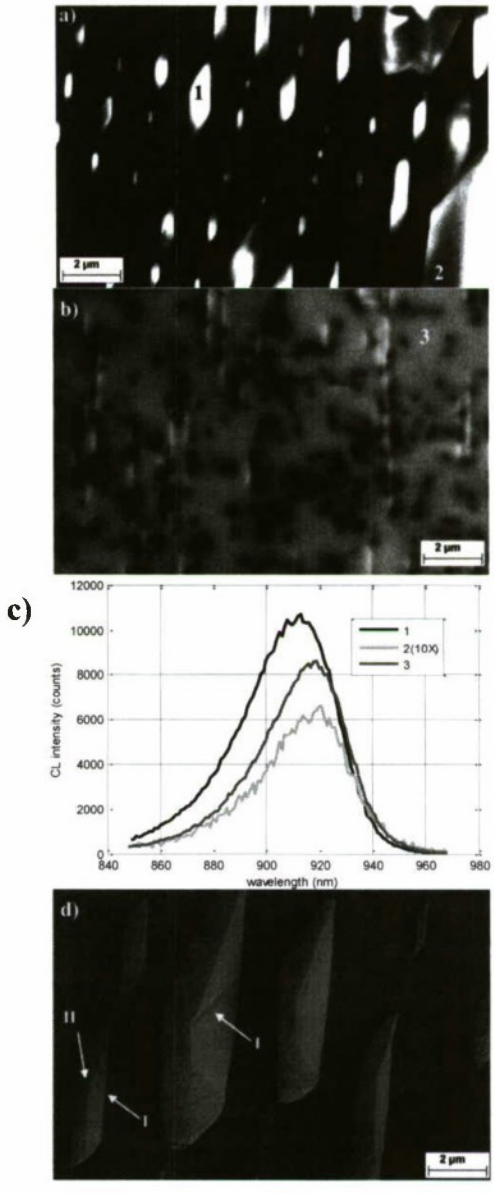

Fig. 3. a) Panchromatic CL image over the spectrum 400 – 1000 nm from a less mature growth region of patterns with line openings; b) the same for the fully grown region; c), the CL spectra of an island 1 in (a), a side facet of island 2 in (a) and a coalesced region 3 in (b); d) SEM view of islands of (a) after Hubert's etching where line defects (I) and planar defects (II) are revealed. In the case of the small island, the planar defect, which has an edge component in the (001) plane, appears to be bounded by a line defect (I).

Figure 4 shows a cross sectional TEM image from the net type openings with α and β = 15^0 and 105^0 of sample B. At the interface between the substrate and the seed layer, a large amount of dislocations close to the substrate can be seen. The TEM image clearly reveals that the dislocations are blocked by the mask. F. Olsson et. al. (10) studied the defect filtering mechanism inside the opening in ELOG of InP on silicon. Studies show that the large filtering of defects can be achieved in a region above smaller size openings. This can be explained by a theory of local strain field, which may bend the dislocation near the openings. However, stacking faults found in the grown layer are most likely not related to the underlying substrate. Improving the surface morphology of the mask and optimization with respect to growth temperature may decrease the intensity of these stacking faults since the generation of stacking can be reduced by decreasing the growth temperature (10).

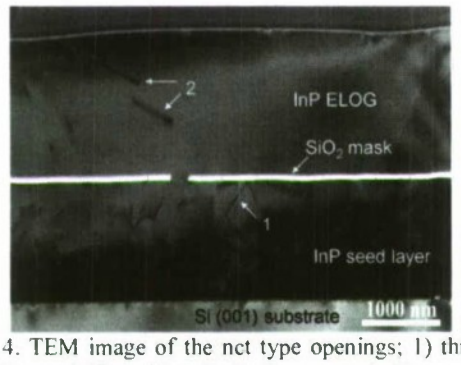

Figure 4. TEM image of the net type openings; 1) threading dislocation and 2) stacking faults from sample B, grown at a temperature of 615 ^{0}C for 2 min and 15 s.

IV. Conclusions

ELOG of InP on silicon from nano-sized line and net-type openings has been carried out and characterized by CL, TEM and AFM. It is shown by TEM that filtering of dislocations that are originally present in the InP seed layer and those originating in interface between the InP seed layer and the silicon substrate can be achieved to a large extent, but defects like stacking faults may arise during lateral growth across the mask, and possibly during coalescence as well. The net type openings give a thicker layer with better surface morphology than the line openings under the same growth conditions. The growth boundary plane seems to have an impact on the luminescence of the grown InP layer, which is due to the orientation-dependent dopant incorporation. Thus, the surface morphology of the mask and the coalescence mechanisms need further attention in order to achieve a layer with good quality.

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High Temperature Operation and Reduced Thresholds in Ring-Based Quantum Cascade Lasers

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MOVPE REGROWTH STEPS FOR HIGH POWER QUANTUM CASCADE LASERS.

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Abstract: we report on the realization of both Distributed Feedback (DFB) and Fabry-Pérot (FP) Quantum Cascade Lasers (QCLs) at Alcatel Thales III-V Lab, involving MOVPE regrowth steps for the realization of the upper cladding and buried ridge structures. We present our results on both device types. Optimization of the planarization process as well as reduction of the thermal resistance achieved using semi-insulating InP:Fe for regrowth is shown and performance perspectives using these building blocks are addressed.

I. Introduction

The interest for efficient and/or high power, single and multi-mode QCLs emitters for applications such as gas sensing or mid IR counter measures has increased in the past years, following the fast development of the devices performances (1-3). We have developed at III-V Lab a full technological process for the realization of both FP and DFB edge emitting ridge waveguide lasers. The AlInAs/GaInAs active region of the laser epitaxial structures is grown on InP substrates using a solid source, multi-wafer Riber 49 MBE system. Subsequent InP based upper cladding and planarization steps are performed using Aixtron Aix 200 MOVPE reactors. In-house technological facilities such as e-beam lithography or ICP for grating realization and ridge etching are used for the fabrication steps.

II. DFB lasers fabrication and performances

We present first the realization of continuous wave (CW) room temperature DFB QCLs using metal grating which opens the possibility of low cost highly versatile fabrication. Our approach is based on the coupling of surface waves and guided waves and is not loss-coupled but index-coupled (4-5). The coupling efficiency of the grating κ=5 cm^{-1} was chosen for designing L=2mm long cavities in order to reach κL close to unity. The upper cladding is etched with a depth $\lambda_{eff}/4$, λ_{eff} being the effective wavelength along the waveguide. The final surface grating defined by e-beam lithography and etched using ICP process on a 7.4µm emitting laser is shown in figure 1 on which the homogeneous metallic deposition is clearly visible along the grating facets. This design provides an index coupling and thus no additional losses are introduced through the feedback and the losses in the waveguide remain low. Continuous wave room temperature single mode QCLs with 30 dB side mode suppression ratio are demonstrated over a 4-8 µm wavelength range with an output power of tens of mW (figure 2).

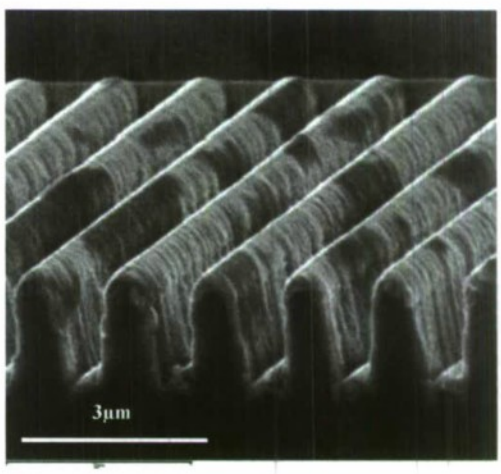

Figure 1: SEM picture of the surface grating realized on top of the ridge waveguide of a DFB QCL.

This process is fully compatible with the subsequent InP:Fe regrowth step which is presented in the third paragraph of this paper. The combination of both

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technological steps should provide a key improvement of the thermal management, leading to higher achievable output power of the devices.

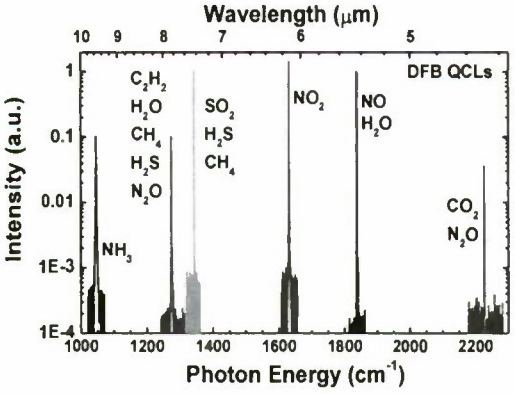

Figure 2: DFB QCL wavelength emissions in the range of 4-8 μm and related molecules for spectroscopy applications.

III. High power ridge FP lasers fabrication and performances.

We have in parallel developed AlInAs/GaInAs QCLs on InP for high power emission. A 850 mW output power has been reached at room temperature in CW operation with a wall plug efficiency of 6.5% using a standard ridge processing and a High Reflectivity (HR) coating. Figures 3 and 4 show the output power and wall plug efficiency obtained for 4mm long ridge waveguides of various widths on a 4.6μm emitting structure.

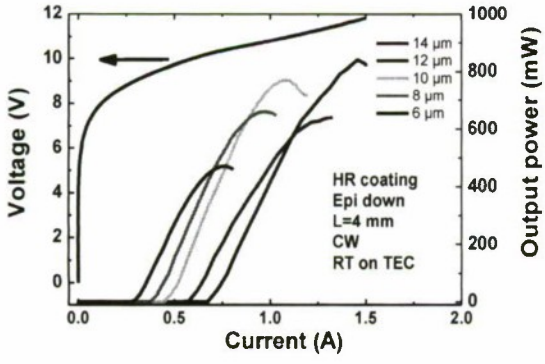

Figure3: room temperature V(I) and P(I) characteristics for 4mm long ridge waveguides of various widths from 6 to 14μm.

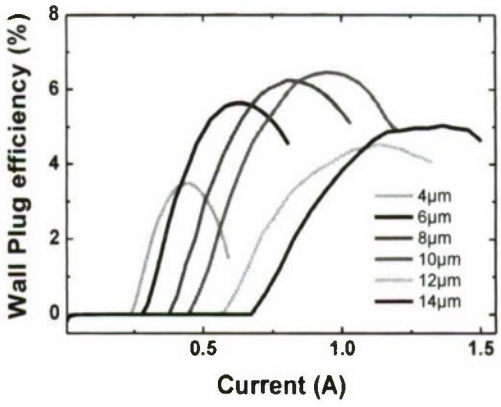

Figure 4: wall plug efficiency for 4mm long ridge waveguides of various widths

The beam divergence is measured using a slit scan at the beam waist behind a telescope for the near field part and a standard far field measurement. It gives a beam quality factor M^2 of 1.15 and 1.22 in the fast and slow axes respectively. The gaussian behavior of the lateral far field is illustrated in figure 5.

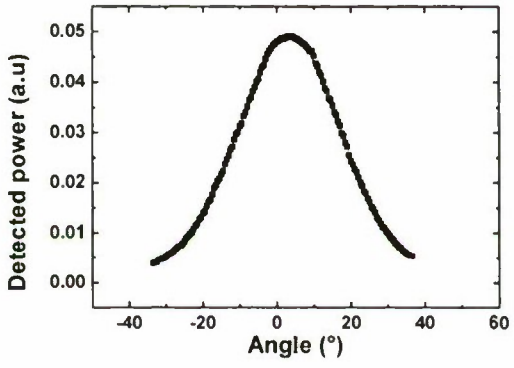

Figure 5: lateral far field of a ridge FP laser emitting @ 4.6μm < 40° (1/e)

IV. InP:Fe regrowth step optimization

This part concerns the development of the semi-insulating InP:Fe MOVPE regrowth process. Figures 6a and 6b show SEM pictures of a conventional selective MOVPE process on dielectric masked ridge waveguides. Large parasitic InP overgrowth is clearly visible at the vicinity of the masked area. This is due to indium precursors adsorption and diffusion on the mask surface

as well as in the vapor phase and this is enhanced by the anisotropic growth rates along the various crystallographic directions.

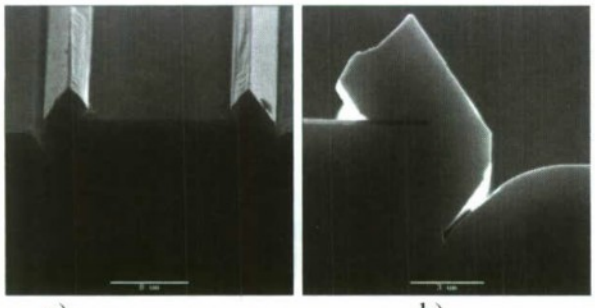

Figure 6: SEM pictures of tilted (a) and cross section (b) views of the InP conventional selective regrowth process.

We have developed a specific regrowth process using in-situ Cl-assisted epitaxy, which allows a perfect selectivity over the whole SiO_2 masked area. The excellent planarization obtained with a 7µm ridge depth and perfect growth along the high Al containing layers of the active region is shown in figure 7 and figure 8 respectively. Fe incorporation in the range of 10^{17} at.cm^{-3} leading to high resistivity up to 10^9 ohm.cm has been achieved.

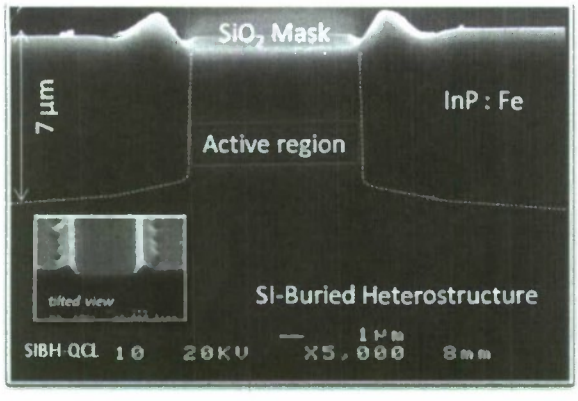

Figure 7: SEM picture of a planarized 7µm deep ridge waveguide.

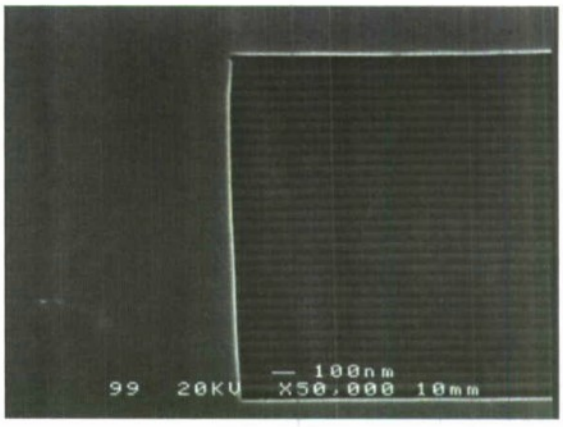

Figure 8: SEM picture of a detail of the regrown InP:Fe along the GaInAs/AlInAs QW active region.

Once all the technological steps – such as ICP etching and growth conditions optimization - achieved and optimized, a full process has been performed on a non optimized laser structure. Figure 9 shows the V(I) and P(I) characteristics of this 5.5µm emitting laser with one HR-coated facet. The thermal resistance of the devices has been determined and exhibits a drastic decrease from 15 K.W^{-1} to 7.5 K.W^{-1} compared to the standard ridge process.

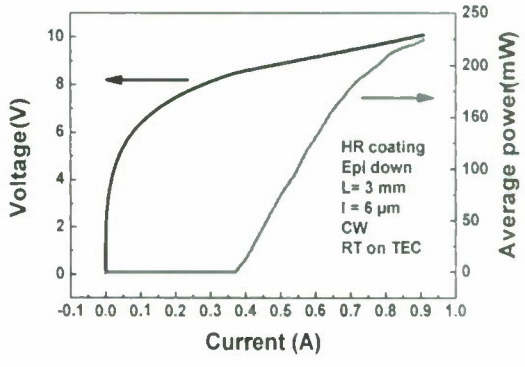

Figure 9: room temperature V(I) and P(I) characteristics for 3mm long, 6µm wide buried ridge waveguide laser emitting at 5.5µm.

V. Conclusion

We have developed AlInAs/GaInAs based QCL structures using MBE and MOVPE epitaxial steps. We have achieved top grating index coupled single mode DFB lasers operating in the in the 4µm to 8µm range and developed the technological process – ridge FP structures and SI-InP:Fe regrowth steps - for the realization of high power buried FP lasers. Using this, we will move the output power from 500mW to 1W while keeping good beam quality.

Aknowledgment

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Proposal of InAlGaAs/InAlAs/InP 1×2 Cross-point Optical Switch with Mode-Spot Modulation MMI Waveguide and 45° TIR Mirror

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***Abstract*—We proposed and analyzed the 1×2 cross-point optical switch with mode-spot modulation in multi-mode interference (MMI) waveguide and 45° total internal reflection (TIR) mirror. It is suitable for crossbar switch fabric and expected some significant switching characteristics for large scale interconnection. As a result, 90° redirection switching is confirmed using FDTD method.**

Keyword; optical switch, optical cross-point switch (OXS), multi-mode interference (MMI)

I. INTRODUCTION

Optical packet switching (OPS) is expected in the in-future new-generation photonic network, and in this system high-speed optical switches are key devices and required to operate with low power consumption, low crosstalk, polarization independent, and multi-port cascade connection, etc. Many kinds of optical switches have been proposed with various materials such as lithium niobate (LN) [1], polymers [2], silicon [3], and compound semiconductors [4][5]. Some of advantages of compound semiconductors are relatively large refractive index change by carrier injection and short carrier lifetime. Therefore, carrier-injection-type optical switches are suitable for low power consumption and high-speed operation. We have fabricated InAlGaAs-InAlAs-InP Mach-Zehnder Interferometer(MZI)-type photonic switch and realized the low crosstalk, polarization independent and low power consumption characteristics [6].

On the other hand, a crossbar-type switch configuration which consists of cross-point switches is attractive because of wide-sense non-blocking operation, crosstalk, and power consumption characteristics [7][8]. The nonblocking switching in wide-sense can be realized to connect between arbitrary input and output ports if they are not busy, without disturbing any other exiting connection. For the crossbar-type switch fabric, it is enough for specific connection that only one cross-point switch is ON per one input light [2], so its control algorithm is very simple and the low power consumption characteristic is expected. For 90° redirection at a cross-point optical switch, the total internal reflection (TIR) mirror with large refractive index difference between semiconductor and air is effective [5].

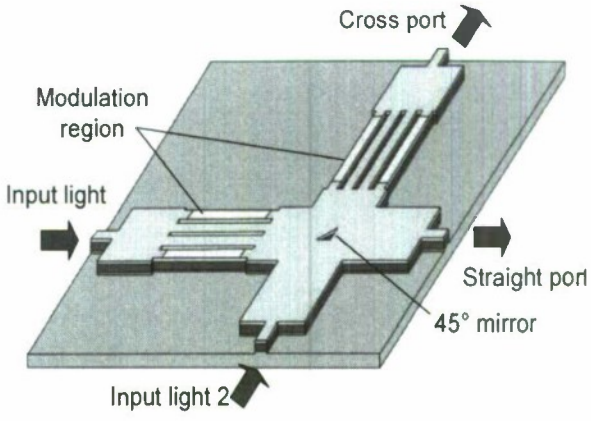

Figure 1. The schematic of a proposed 1×2 cross-point optical switch with mode-spot modulation MMI waveguide and 45° TIR mirror.

Therefore, we proposed a 1×2 cross-point optical switch with mode-spot modulated MMI waveguide and 45° TIR mirror which is suitable for the crossbar switch.

II. STRUCTURE AND DESIGNING

The schematic of a 1×2 cross-point optical switch with mode-spot modulated MMI waveguide and 45° TIR mirror is shown in Figure 1.

This switch consists of two symmetric MMI waveguides, two arrayed phase shifter waveguides, and 45° TIR mirror at the cross-point. The total length of an MMI waveguide is $3L_\pi/4$, the TIR mirror is set at the position of $3L_\pi/8$, where L_π is the beat length given by $L_\pi=4n_{MMI}W_e^2/3\lambda_0$ with an effective MMI width of W_e and an equivalent refractive

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TABLE I. THE RELATIVE PHASE DIFFERENCE OF EACH SPOT

z	Spot	Relative Phase Difference			
$3L_\pi/16$	4	$-\pi/2$	0	0	$-\pi/2$
$3L_\pi/8$	2	0		0	
$9L_\pi/16$	4	$\pi/2$	0	0	$\pi/2$
$3L_\pi/4$	1	0			

index of n_{MMI} [9]. For a symmetrie MMI, the input light is split into four spots at $3L_\pi/16$ and $9L_\pi/16$, and two spots at $3L_\pi/8$, and they are converged in one spot at $3L_\pi/4$.

At OFF state, the input light is split into two spots and they pass by the TIR mirror without strike and go straight ahead, so the output light passes into the straight port. On the other hand, at ON state, the refractive index of modulation regions is decreased by carrier injection, and the input light is not split but is converged at one spot at the center at $3L_\pi/8$ and reflected by the TIR mirror, so the output light emits from the eross port. On the other hand, the input light 2 passes by the mirror and goes into the cross port without the phase modulation.

The spot number and relative phase differenees are shown in TABLE 1. Four spots appear at $3L_\pi/16$ and $9L_\pi/16$, and their relative phase differences turn over. When the relative phase differences of four spots are $(-\pi/2, 0, 0, -\pi/2)$, the two spots appear at $3L_\pi/8$. On the other hand, when the relative phase differenees of four spots are $(\pi/2, 0, 0, \pi/2)$, the one spot appears at $3L_\pi/8$. Thus, the number of mode at the cross point and the output light can be switched by the relative phase differences of four mode spots at $3L_\pi/16$. In order to switch the output port, the arrayed phase shifters are set at $3L_\pi/16$ so that the first MMI waveguide is functioned as a 1×4 splitter [10], and the phases of two outer spots of four spots are modulated by π at ON state.

The light propagation analysis of 1×4 MMI waveguide splitter and arrayed phase shifter waveguides are shown in Figure 2: (a) there is no phase modulation and the input light is split into two spots at $3L_\pi/8$, and (b) there is π phase modulation at two outer spots of four spots in arrayed phase shifter waveguides, and the light is converged at one spot at the center at $3L_\pi/8$.

We analyzed the light propagation of the cross-point switch using FDTD method, and the results are shown in Figure 3: (a) at OFF state and (b) at ON state. The widths of

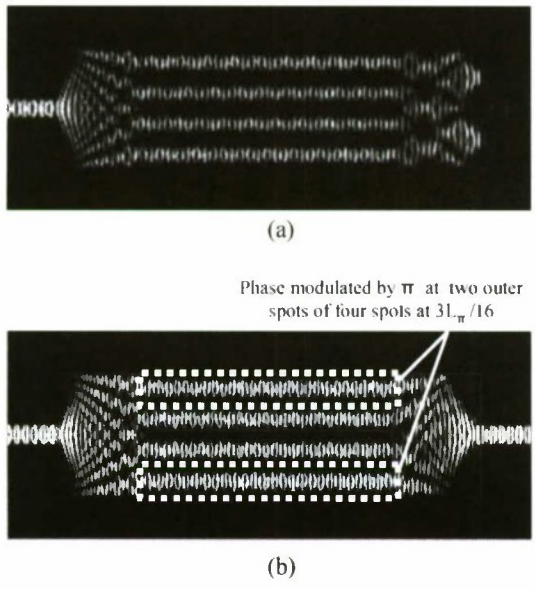

Figure 2. The light propagation analysis of MMI waveguide with four arrayed waveguides: (a) at OFF state and (b) at ON state

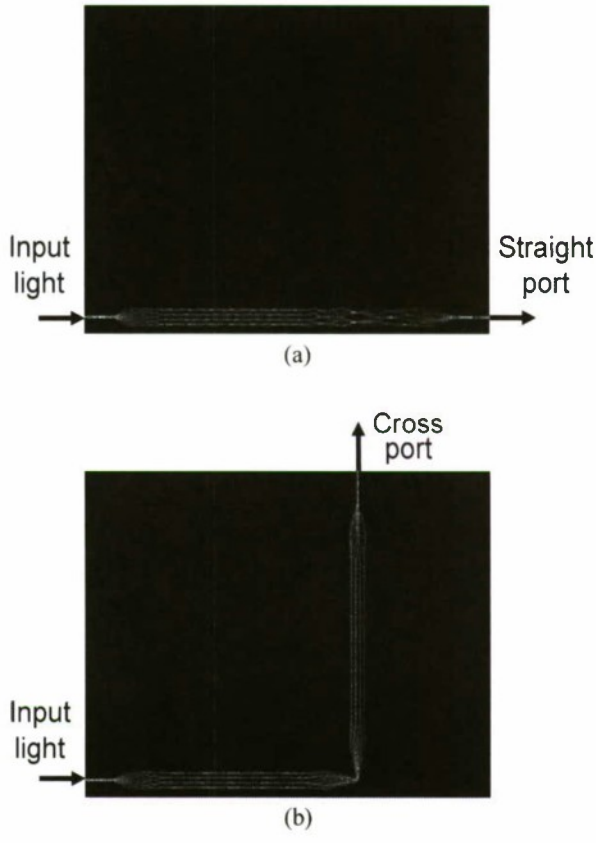

Figure 3. The light propagation analysis of the cross-point optical switch using FDTD: (a) at OFF state and (b) at ON state.

MMI and access waveguides are W_{MMI}=6.0μm and W_{ACC}=1.0μm, respectively, the length of phase shifters L_{phase} is 50μm, and the total length is 142μm. We will actually fabricate the cross-point switch which has a larger MMI width W_{MMI} than that used in the analysis. At OFF state, the light comes out from the straight port and the crosstalk is less than -30dB. At ON state, the refractive index change of each phase shifter is Δn=0.54%, the light comes out from the cross port, and the crosstalk is less than -15dB. The phase modulation at the second arrayed phase shifter waveguides at the side of the cross port waveguide is also necessary at ON state.

The switching characteristic of the cross-point switch for λ_0=1.55μm and TE-mode is shown in Figure 4. The output power from the cross port is the lowest and the crosstalk is less than -35dB when Δn=0.1%. This is caused by that the 1×4 MMI waveguide splitter is not optimal length for this analysis by FDTD method, and the relative phase difference of the four light spots is not ideal at $3L_\pi/16$ when Δn=0%. The output power from the straight port is the lowest and the output power from the cross port is the maximum when Δn=0.54%. At ON state, the propagation loss is 4.0dB, and this propagation loss seems to be caused by the scattering of the reflected light between the MMI waveguide and the second arrayed phase shifter waveguides. To reduce this propagation loss, the precise designing of the curvature of the reflection facet of the mirror and the coupling efficiency between the MMI waveguide and the second arrayed phase shifter waveguides are necessary. The phase change Δφ is given by $k_0\Delta nL_{phase}$, so the refractive index change for a certain Δn is inversely proportional to the phase shifter length L_{phase}. The required refractive index modulation for switching can be reduced down to Δn=0.14%, when the phase shifter length is 200μm, which is good for lower power consumption.

The crosstalk is dependent on the relationship between the size of the TIR mirror and the widths of the access

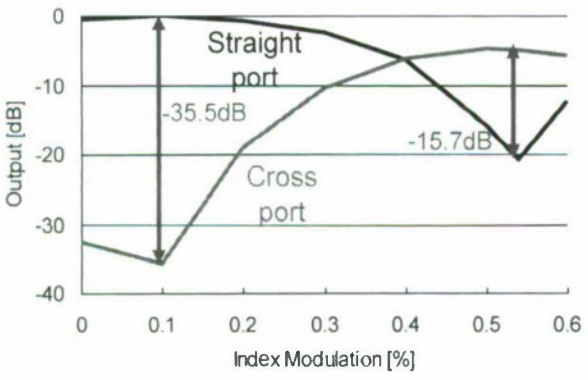

Figure 4. The switching characteristic of the cross-point switch for λ_0=1.55μm and TE-mode.

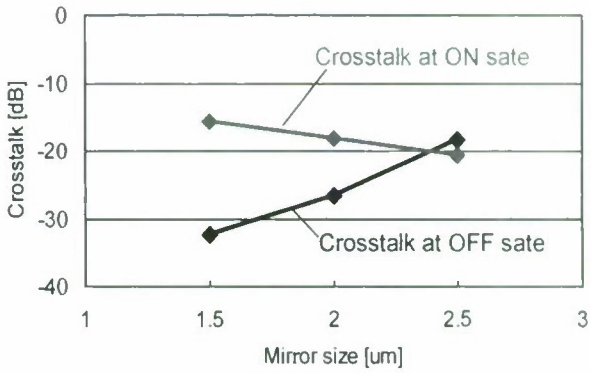

Figure 5. The crosstalk dependence on the reflection mirror size when W_{MMI}=6.0μm and W_{ACC}=1.0μm.

waveguide and the MMI waveguide. The crosstalk dependence on the reflection mirror size is shown in Figure 5, when W_{ACC}=1.0μm and W_{MMI}=6.0μm. The crosstalk at OFF state becomes lower but that at ON state larger, when the mirror size becomes smaller. Reversely, the crosstalk at OFF state becomes larger but that at ON state lower, when the mirror size becomes larger. About the mirror size, the crosstalk characteristics at ON and OFF states are in the trade-off relationship. Considering the actual operation of the crossbar switch, the total crosstalk is critically determined by the crosstalk at OFF state than the crosstalk at ON state, because the input light passes one switch at ON state and other switches at OFF state. Therefore, the mirror size should be smaller and 1.5μm is optimal when W_{MMI}=6.0μm and W_{ACC}=1.0μm.

The crosstalks at OFF and ON states for TM-mode are less than -30dB and -10dB, respectively. The crosstalks at OFF and ON states are in low polarization and wavelength dependence.

III. CONCLUSION

We proposed the 1×2 cross-point optical switch with mode-spot modulation MMI waveguide and 45° TIR mirror which is suitable for the crossbar switch. Crosstalks are less than -30dB and -15dB at OFF and ON states, respectively, by FDTD analysis. The crosstalks at ON and OFF state are low polarization and wavelength dependence.

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Switching Characteristics in Variable Refractive-Index Waveguide Array by Carrier Injection

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Abstract

We have demonstrated a carrier-injection-type wavelength switch composed of the straight waveguide array using GaInAs/InP MQW with linearly varying refractive index distribution fabricated by selective MOVPE.

I. Introduction

In wavelength division multiplexing (WDM) networks, the key components are wavelength demultiplexers, wavelength switches, and wavelength-selective switches (WSSes). The WSSes can be obtained by combining wavelength demultiplexers and wavelength switches; thus, they connect arbitrary input wavelength signals to arbitrary output. Various WSSes have been proposed and reported, with components based on micro-optic techniques already commercially available, such as planar lightwave circuits (PLCs), micro-electro-mechanical systems (MEMS), III-V semiconductors, PLZT, and lithium niobate ($LiNbO_3$).

We have proposed a wavelength demultiplexer/switch using arrayed waveguide with linearly varying refractive-index distribution based on GaInAs/InP MQW fabricated by selective metal-organic vapor phase epitaxy (MOVPE) growth. The conventional AWGs are designed so that phase differences between adjacent waveguides are obtained by gradually varying waveguide length. In the proposed design, however, phase differences between adjacent waveguides are achieved by varying the waveguide thickness which is the refractive indices of the waveguides. In the previous work, we have shown the wavelength demultiplexing [1-3], wavelength switching [4] using thermo-optic (TO) effect [5, 6]. In this report, we show the successful demonstration of wavelength switching by controlling the refractive index using carrier injection.

II. Design and principle of operation

A schematic of the wavelength switch is shown in Fig. 1. This device consists of a star coupler, a waveguide array, and input/output waveguides. The refractive index varies gradually across the waveguide array because of differences in waveguide thickness realized by MOVPE selective area growth.

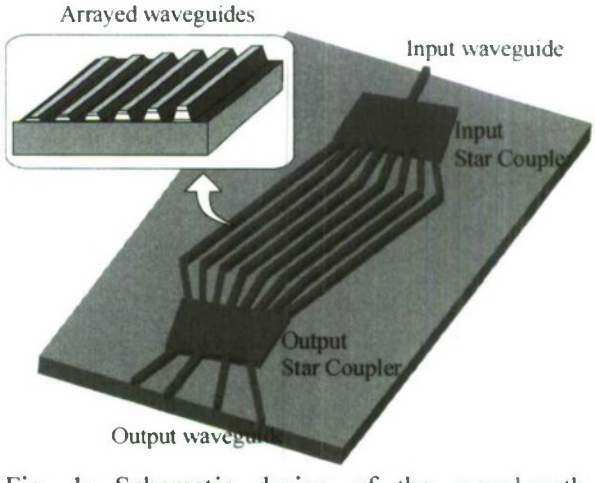

Fig. 1: Schematic design of the wavelength switch using variable refractive-index waveguide array.

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To focus each wavelength of light, the waveguide arrays and input/output waveguides use a Rowland circle mounting. All the arrayed waveguides between the input and output star couplers are of equal length, and the straight arrayed waveguides and star couplers are joined with curved waveguides. The switch contains 16 arrayed waveguides, each 3-μm wide and 10,000-μm long; the waveguide spacing is 3 μm. The equivalent refractive-index difference between the two sides of the array is 1.4%, and the refractive index modulation region is 4000-μm long. The length of the star coupler is 1250 μm; there are four output waveguides with a 10.2-μm separation. In the variable-refractive-index waveguide array, different wavelengths of light undergo different phase shifts in the waveguides, resulting in diffraction peaks in different positions for different wavelengths of light, allowing the proposed design to act as a wavelength demultiplexer. Moreover, the device could be applied to wavelength switching, because the refractive indices of the waveguides in the array can be controlled dynamically, e.g., by carrier injection, quantum-confined Stark effect (QCSE), and TO effect.

III. Fabrication

In the selective MOVPE, an asymmetric SiO_2 mask, where there was a wide width SiO_2 mask in one side of the array shown in Fig. 2(a), was used and the waveguides with different thickness were formed [7,8]. The arrayed waveguides having varying waveguide thickness could be fabricated in a single growth step, resulting in the formation of an arrayed waveguide with gradually varying refractive index across the array. The arrayed waveguides consisted of an n-InP buffer layer, a 40-period i-GaInAs/InP MQW, a i-InP Zn-difussion stop layer, a p-InP cladding layer, a p^+-GaInAs contact layer along the [011] direction on the (100)-oriented n-InP substrate, as shown in Fig. 2(b). The waveguide oriented parallel to the [011] direction had a trapezoidal profile that narrowed in the vertical direction and was bound by sidewalls of highly smooth well-defined (111)B planes. Selective MOVPE growth was performed in a vertical reactor at a growth pressure of 100 Torr and a temperature of 640 °C.

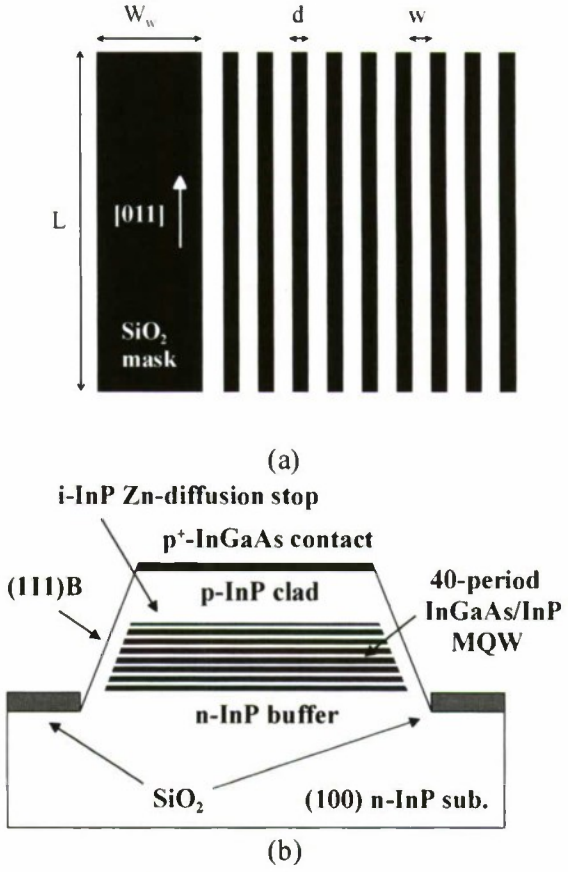


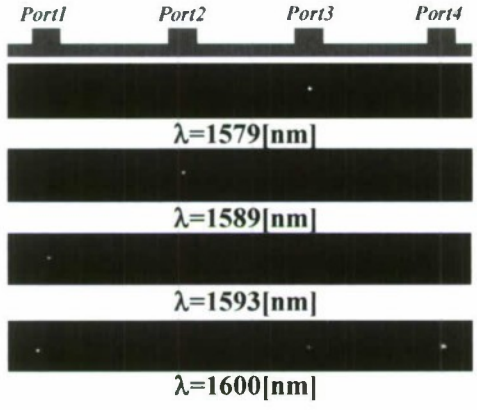
Fig. 2: (a) SiO_2 mask pattern used in selective MOVPE growth. (b) Cross-sectional schematic diagram of the p-i-n GaInAs/InP MQW waveguide.

IV. Wavelength switching

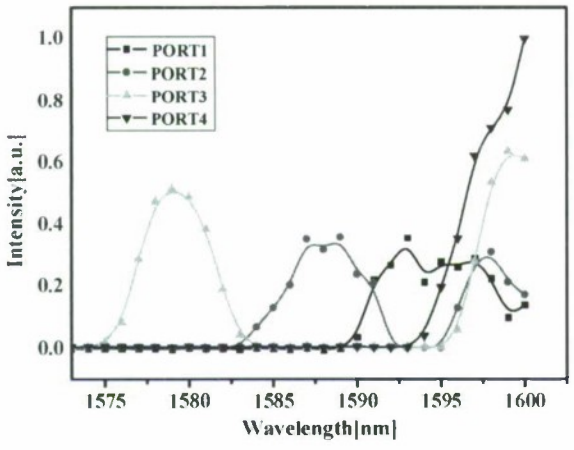
First, we show the wavelength demultiplex characteristics of this device. Fig. 3(a) shows the near-field pattern (NFP) of the output ports with various wavelength light. The input light was successfully demultiplexed where the input light wavelength was between 1575 nm and 1600 nm, however the crosstalk between channels was lowered longer than 1600 nm wavelength. Fig. 3(b) shows the relation between normalized output power and the input light wavelength in each output port. The crosstalk was -20.9 dB, -17.8 dB, -19.4 dB, and -2.1 dB at 1579 nm, 1589 nm, 1593 nm and 1600 nm, respectively.

Successful wavelength switching was demonstrated by refractive index change through carrier injection in this device. Fig. 4(a) shows the NFP of the output ports with various injected currents where the input light wavelength was 1579 nm. By increasing the injected current into

the device, the output light shifted from Port3 to Port2. Fig. 4(b) shows the relation between normalized output power and the injected current in each output port. The switching current and current density was 300 mA and 0.156 kA/cm^2, respectively. The extinction ratio was 27.6 dB at Port2 and 16.0 dB at Port3. The channel crosstalk was −18.4 dB and −12.6 dB at an injected current of 0 mA and 300 mA, respectively.

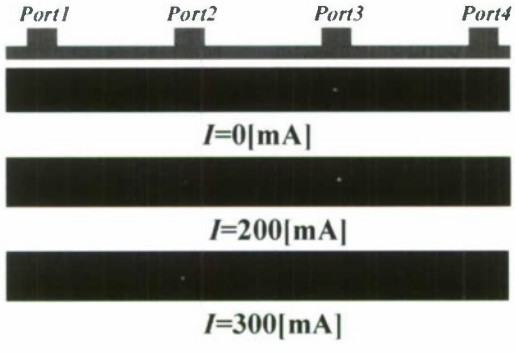


(a)

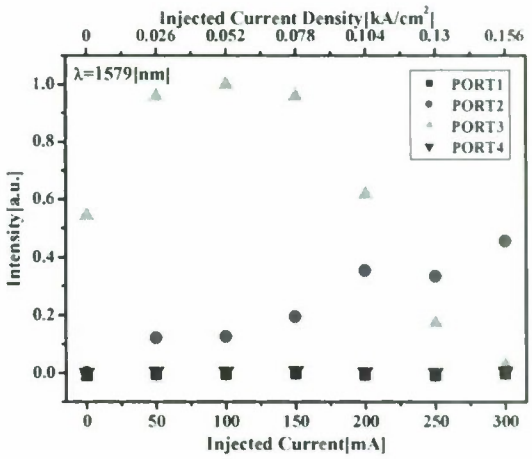


(b)

Fig. 3: (a) NFP of the output ports with various wavelength light. (b) Wavelength dependence on the normalized output port intensity.



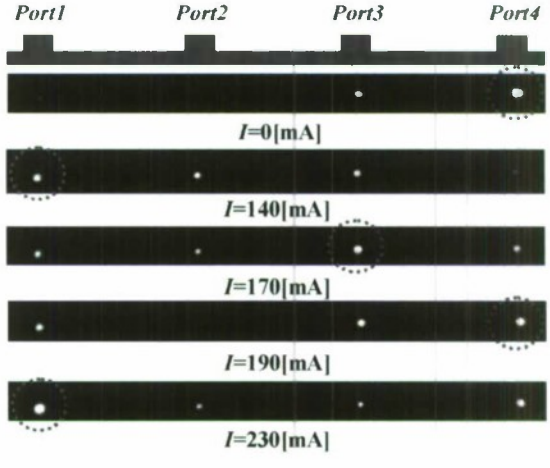
(a)



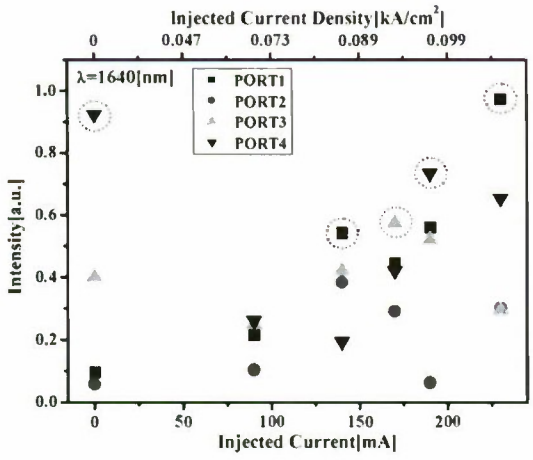
(b)

Fig. 4: (a) NFP of the output ports with various current for input lights of 1579nm. (b) Output ports intensity vs. injected current of λ=1579nm wavelength of light.

Fig. 5(a) shows the NFP of the output ports with various injected currents where input light wavelength was 1640 nm. By increasing the injected current into the device, the output light was shifted from Port4 to Port1, Port3, Port4, and Port1. Fig. 5(b) shows that the relation between normalized output power and the injected current in each output port. As can be seen from these figures the light was shifted to the output ports in order except Port2. The extinction ratio was 10.0 dB, 8.3 dB, 3.7 dB, and 6.8 dB at Port1, Port2, Port3, and Port4, respectively. The channel crosstalk was -3.6 dB, -4.5 dB, -1.1 dB, -1.2 dB, and -1.7 dB at an injected current of 0 mA, 140 mA, 170 mA, 190 mA, and 230 mA, respectively.



(a)



(b)

Fig. 5: (a) NFP of the output ports with various current for input lights of 1640nm. (b) Output ports intensity vs. injected current of λ=1640nm wavelength of light.

The low channel crosstalk was caused by the phase difference error between the arrayed waveguides resulting from the nonuniform thickness of the arrayed waveguides and the structure of the star coupler. This low crosstalk will be improved by optimizing the selective growth process and the star coupler design. These experimental results prove that this device structure is useful for a carrier-injection-type wavelength switch.

V. Conclusion

The carrier-injection-type wavelength switch using arrayed waveguides with linearly varying refractive-index distribution based on GaInAs/InP MQW fabricated by selective MOVPE growth. Successful wavelength switching was experimentally demonstrated by the refractive index change through the carrier injection in this device with input light 1579nm in wavelength. Increasing the injected current into the device shifted the output port from Port3 to Port2. The switching current and current density were 300 mA and 0.156 kA/cm^2, respectively. The extinction ratio was 27.6 dB at Port2 and 16.0 dB at Port 3. The Channel crosstalk was -18.4 dB and -12.6 dB at an injected current of 0mA and 300 mA, respectively. These experimental results prove that this device structure is useful for carrier-injection-type wavelength switch.

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All-optical switch using InAs quantum dots in a vertical cavity

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Abstract—We have investigated at the first time an all-optical switch using self-assembled InAs/GaAs quantum dots (QDs) within a vertical cavity structure. The optical nonlinearity of the QD switch has been optimized by an asymmetric cavity to achieve the maximum differential reflectivity. Optical switching via QD excited states exhibits a fast decay with a time constant down to 23 ps and a wavelength tunability over 30 nm. By compared to the theoretical design, the absorption strength of QD layers within the cavity has been determined.

I. INTRODUCTION

Ultrafast photonic devices, such as femtosecond light sources and all-optical switches, are essential components for the future optical communication system with high-speed of 100 Gb/s~1 TGb/s.[1] Optical nonlinear properties are demanded to realize the all-optical switching. However, to access to the nonlinear operation region of photonic materials, very high excitation power is usually required for optical switching devices, which becomes a well-known problem as the "power/speed trade-off". In that sense, nano-scale materials such as self-assembled quantum dots (QDs) are particularly attractive due to their novel characteristics as three-dimensional confined semiconductor structures. Atom-like states in quantum dots with extremely-high differential gain/absorption parameters are anticipated to realize ultra-low power operation of ultrafast all-optical switches.

The use of nonlinear absorption dynamics of QDs has been proposed to construct an optical phase shifter in a Mach-Zehnder (MZ) configuration.[2] However, the low volume of QDs requires a very long waveguide structure to fulfill the interaction between QDs and the light. This makes the lateral geometry of the MZ interferometer relatively large. Alternatively, a vertical-cavity QD switch has been proposed based on the optical Kerr effect inside QDs.[3] Such a vertical geometry could potentially provide low-power, polarization-insensitive and micro-meter-size switching devices based on QD materials.[4]

In this work, we investigate the design principle of a vertical-geometry switch by considering the QD/cavity nonlinearity. The relation between the distributed Bragg reflectors (DBRs) and the QD absorption strength has been derived analytically. An all-optical switch based on the optical transition of excited-QD states (ES) has been fabricated, and characterized. Our results show that QD materials are potentially suitable for compact all-optical switches in the future optical communication system.

II. THE MAXIMUM DIFFERENTIAL REFLECTIVITY

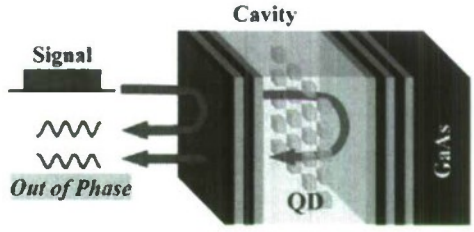

Figure 1. Schematic diagram of an all-optical switch using QDs as an optical nonlinear source.

Figure 1 describes the operation principle of a vertical-cavity QD switch. The cavity consists of two DBR mirrors, which further includes multiple periods of alternating high- and low-index layers. At a certain condition, the light reflected by the front mirror is fully cancelled by the effective reflection from the back mirror at the cavity resonant mode. This condition is so-called the zero reflectivity condition, which requires,

$$R_F = R_B e^{-2\Gamma}, \qquad (1)$$

where R_F and R_B present the reflectivity of the front and back mirrors, respectively, $\Gamma = 2\int \alpha(l)dl$ is the total absorption strength, and $\alpha(l)$ is the absorption coefficient inside the cavity.

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Figure 2 presents a typical reflectivity spectrum from a vertical cavity at the zero reflectivity condition. A photonic bandgap region can be observed with a very high reflectivity close to 100%. When strong optical pumping occurs at the cavity resonant mode, the absorption strength of QDs saturates. This results in a violation of the zero reflectivity condition and hence fulfills the all-optical switching process. Efficient switching requires a high differential reflectivity between two operation conditions with and without optical pumping. To achieve the high differential reflectivity, the cavity should be operated at

$$R_F = \left(\frac{\sqrt{3} R_B^{1/2} e^{-\Gamma} - 1}{\sqrt{3} - R_B^{1/2} e^{-\Gamma}} \right)^2 < R_B e^{-2\Gamma}. \qquad (2)$$

Equation (2) described the maximum differential reflectivity condition, which gives a front mirror reflectivity close to but less than the zero reflectivity condition--Equation (1). Both equations (1) and (2) suggest an asymmetric cavity structure. For the QW or bulk material, large absorption exists for the all-optical switching. Hence, very small reflectivity is required for the front mirror, which corresponds to a low-finesses cavity. However, the Γ value is usually at the order of 10^{-4} in QD materials, which is extremely small compared to the QW and bulk materials. Hence, a relatively large-finesses design needs to be addressed in the case of QDs.

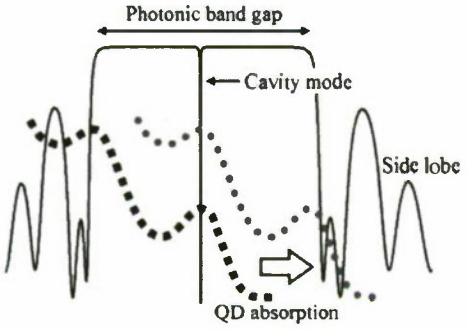

Figure 2. The cavity reflectivity spectrum with a zero reflectivity at the cavity resonant mode (solid curve). QD absorption spectra are plotted with ground state (solid squares) and excited states (solid circles) transitions matching at the cavity mode.

To study the mirror design of the vertical cavity, the relation between the front and back mirror periods is fixed at the maximum differential reflectivity condition, as expressed in Equation (2). The optical nonlinearity of the QD/cavity structure is investigated by changing the period number of the back DBR mirror, with regarding only the absorption saturation process inside QDs. In Figure 3, the cavity reflectivity with different periods of the back mirror is calculated. When the period of the back mirror increases, the reflectivity of the back mirror is significantly enhanced. After exceeding 20 periods, the differential reflectivity of the cavity

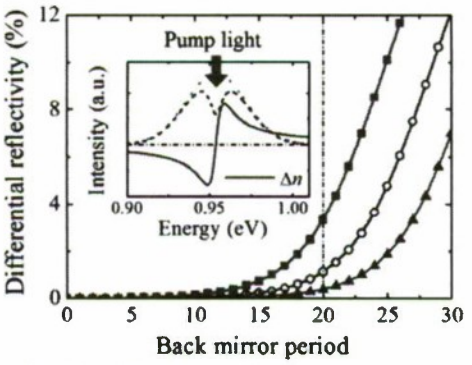

Figure 3. The QD/cavity nonlinearity represented by the reflectivity of back mirror (solid curve) and the differential reflectivity of the cavity with $\Gamma = 1\times10^{-4}$ (solid triangles), 3×10^{-4} (hollow circles) and 1×10^{-3} (solid squares), respectively. The inset shows the refractive index change according to the Kramers-Kronig relation.

increases rapidly. Three test values of Γ are used in the figure with $\Gamma = 1\times10^{-4}$ (open triangles), 3×10^{-4} (open circles) and 1×10^{-3} (solid squares), respectively. 20-30 periods of the back mirror present a high nonlinear region, where we focused for the design of QD switches.

The refractive index change due to the Kramers-Krönig relation is usually considered as another optical nonlinear mechanism induced by the absorption dynamics, which can be described as,

$$\Delta n(\omega) = \frac{c}{\pi} P \int_0^\infty \frac{\Delta\alpha(\omega')}{\omega'^2 - \omega^2} d\omega' \qquad (3)$$

where ω is the optical frequency, and n is the refractive index. With considering a light beam injected into a large-finesses vertical cavity, the absorption linewidth is mainly determined by the homogenous broadening of QD materials. By this consideration, the refractive index change of QDs inside cavity is calculated using equation (3), as shown in the inset of Figure 3.The refractive index change would cause a phase shift inside cavity, which further helps the optical switching.

III. Experimental Results

The QD switch sample has been grown on an undoped GaAs (110) substrate by molecular beam epitaxy (MBE). QD layers were prepared using Stranski-Krastanow growth mode by depositing 2.6 ML InAs per layer at 480 °C. 9 layers of InAs QDs within 3 stacks were placed at the anti-node position of the optical field. Both the wavelength of QD emission and the cavity resonant mode has been carefully adjusted to match each other.

High energy states in QDs can be employed to enhance the switching dynamics. Figure 4 shows edge emission PL spectra from the QD switching sample. It gives emission peaks with the ground state (GS) emission at 1298 nm and the ES emission at 1220 nm (solid curve). The ES transition is close to the cavity mode at 1230 nm.

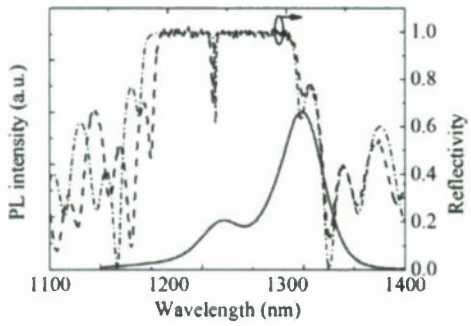

Figure 4. Edge emission PL (solid curve) and the cavity reflectivity spectra (dashed curve).

Conventional pump-probe measurements were carried out at room temperature to study the switching dynamics. Orthogonally polarized pump and probe beams were generated by an optical parametric oscillator (OPO), which provided ~130 fs optical pulses with an 80 MHz repetition rate. The pump power was typically has a power density of ~10 fJ/μm^2 (per pulse) with a bandwidth of ~20 nm, which is much broader than the linewidth of the cavity mode. With the pump beam exciting the front cavity mirror at the wavelength of cavity mode, the differential reflectivity was traced by the probe signal beam with a power approximately one hundredth of that of the pump power. The absorption of the ES becomes saturated when an ultra-fast optical pulse pumps at the ES wavelength. After the pump pulse is removed, a fast relaxation of carriers into the GS takes place, which recovers the absorption at the ES. This ES switching sample shows a fast switching dynamics with 32 ps decay time, as shown in the inset of Figure.5.

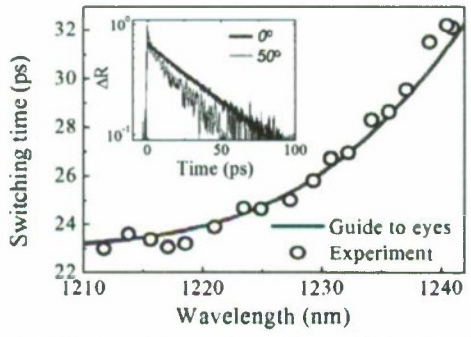

Figure 5. Wavelength dependence of the switching time from measurement (open circles) and simulation (dashed curve). The inset gives two examples of switching curves with operation wavelength at 1240 and 1219 nm, which correspond to the incident angles of 0 and 50°, respectively.

Because the cavity resonant mode determines the operation wavelength of the device, this QD switch can only work in a very narrow wavelength region. To overcome this drawback, we have investigated the incident angle dependence of the switching performance. By changing the incident angle of the optical pulses from 0 to 50 degrees, the operation wavelength is varied near the ES emission peak from 1240 to 1210 nm. This degree of tuning is certainly possible because the inhomogeneous broadening of QD absorption spectra is usually over a range of 40~50 nm. As shown in Figure 5, the angle-dependent switching time (open circles) decreases when the operation wavelength is going to shorter. A minimum switching time of 23 ps is reached using this configuration near the QD ES emission. For wavelengths shorter than 1220 nm, the switching time almost keeps constant. The inset in Figure 5 presents two switching dynamics curves with operation wavelength at 1240 and 1219 nm. The present QD switch using the ES has been shown to operate over a wavelength range of 30 nm with a 23-32 ps switching time.

IV. Comparision with the Design

In the characteristics of this switching device, a differential reflectivity in this measurement shows 2-3% variation of the cavity reflectivity, e.g. $\Delta R/R \approx$ 2-3%. By comparing with the simulation, it corresponds to a value of $\Gamma \approx 2.3\text{-}3.5 \times 10^{-4}$, which equals to one of the test values set in Figure 3 (hollow-circle curve). Based on the experimental value of the absorption strength, the period of the frond mirror should be optimized to be 16 to achieve the maximum differential reflectivity. Additionally, with increased absorption strength, a differential reflectivity value of ~10% could be expected ($\Gamma = 1\times10^{-3}$ in solid-square curve), which requires higher number of QD layers.

V. Summary

We have proposed an all-optical switch device based on self-assembled InAs QDs within a GaAs/AlGaAs vertical cavity structure. The optical nonlinearity of QDs can be significantly enhanced with optimizing the cavity structure. Pump-probe measurement has shown a switching time down to 23 ps via QD ES and a tunable wavelength region of 30 nm. These results support QD materials to be suitable for compact ultra-fast all-optical switches and would finally provide cheaper, faster, and reduced power consumption devices for future high-bit-rate telecommunication systems.

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LOW DRIVING VOLTAGE SPATIAL LIGHT MODULATOR FABRICATED BY ULTRAHIGH-PURITY GaAs

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Abstract

Highly efficient surface normal spatial light modulators (SLMs) using ultrahigh purity GaAs layers (30 μm thick) grown on (100) - oriented n^+- GaAs substrate by liquid phase epitaxy (LPE) method have been realized. The extinction ratio of 25 dB has been demonstrated with a low - driving voltage (32 V) at 895 nm, based on electroabsorption (EA) effect. Very large depletion length over 150 μm is confirmed by analyzing the extinction ratio and capacitance- voltage (C-V) measurements. The calculated value of impurity concentration is low ($\approx 10^{12}$ cm^{-3}) and indicates donor and accepter in the device are highly compensated.

I. INTRODUCTION

Optically addressed spatial light modulators (SLMs) are key components in optical processing systems. A liquid-crystal light valve is usually used; however, it has a low contrast ratio and low speed. High contrast and high speed SLMs using 400 μm thick semi-insulating (SI) GaAs have been reported [1] with the extinction ratio of 20 dB at 2.4 kV based on EA effect.

Recently we have succeeded in growing the highest purity GaAs epilayers, as represented by 77 K electron concentration as low as 5.84×10^{12} cm^{-3} and Hall mobility as high as 312,000 $cm^2 V^{-1} s^{-1}$ using LPE method. The epilayers were grown inside a quartz tube, utilizing a conventional sliding boat under a palladium-purified hydrogen carrier gas ambient [2]. GaAs epilayers with high mobility and low carrier concentration have low transmission loss and large depletion region because a sharp excition absorption can be observed even at room temperature. These properties enable us to fabricate various devices [3-5]. The high purity with low carrier concentration makes it possible to widen the depletion region, resulting in enhancing the extinction ratio and reducing operating voltage of devices [6]. Thus, it is possible to fabricate highly efficient SLMs.

In this paper, we will report fabrication process of SLM along with its voltage dependent optical transmission characteristic. The extinction ratio of 25 dB at low driving voltage of 32V is also reported here.

II. DEVICE FABRICATION

In this work, we have studied two different samples of high purity GaAs ($n < 10^{13}$ cm^{-3}). One consists of 30 μm thick i-GaAs and n^+-GaAs substrate and the other consist of 13 μm thick i-GaAs only. The sample made from the former was used for the fabrication of SLMs, while the latter were used for measuring the absorption coefficient at room temperature.

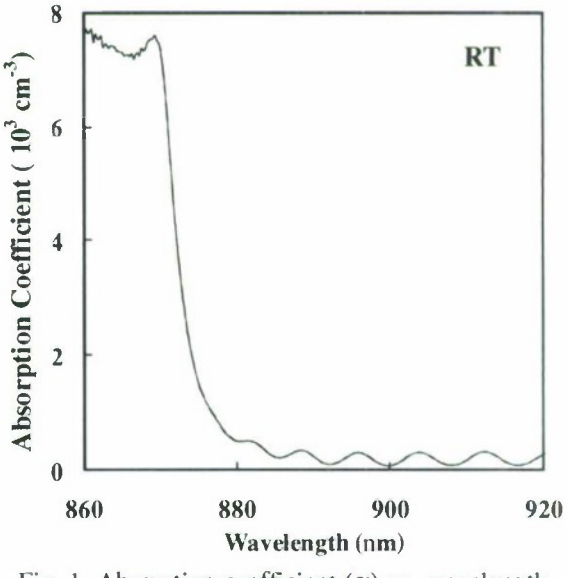

Fig. 1. Absorption coefficient (α) vs. wavelength (λ) measured at the room temperature.

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In order to measure the absorption coefficient the substrate was etched chemically and then epilayer was polished to be about 13 μm thick with Br-ethanol mechano-chemical etching to the required size. The sample was supported on a glass.

The optical transmission of 13 μm thick epilayer was measured using halogen light source (ANDO AQ4303B). The incident light was perpendicular to epilayer surface and transmitted light was detected from the sample backside. Transmitted light through the sample was coupled to a standard single mode fiber (SMF), and detected by optical spectrum analyzer (ANDO AQ6317B). The sample and fibers was set in a XYZ manipulator. The ends of both fibers were hemi-spherical shaped to improve the coupling efficiency between the sample and the fibers.

A clear exciton absorption peak was observed at 869 nm even at room temperature, as shown in Fig. 1. The absorption coefficient for the exciton resonance peak is estimated to be 8×10^{3} cm^{-1} by analysing the optical transmission. The absorption coefficient decreases sharply from 869 nm. It also indicates that the grown epilayer is high purity.

A clear Fabry-Perot interference mode was also observed over 880 nm wavelength, from which the thickness and transmission loss of epilayer is estimated to be 12.8 μm and 4.6 cm^{-1} at 897 nm, respectively [7]. The calculated value of transmission loss is little higher than those reported by Stillman et al. [3] for the waveguide structure. This higher value in our case may be due to coupling loss ambiguity.

The SLMs were fabricated by growing high purity epilayers on (100)-oriented n^{+}- GaAs substrate doped with Si concentration of $3\sim5\times10^{18}$ cm^{-3} using liquid phase epitaxy (LPE). The growth parameters of the sample used in this work are shown in Table 1.

Table 1. Growth parameters of the sample:

1	Purification time	25 Hours
2	Crystal growth time	45 Minutes
3	Temperature	800 °C
3	Environment	Hydrogen gas

In order to purify epilayers we used recyclic growth method [2]. Before fabricating device, epilayer was grown on semi-insulating (SI) GaAs substrate and the purity of Ga solution was measured by Hall measurement. Then, the same Ga solution was used for the fabrication of SLM. The mobility and carrier concentration was 2.43×10^{5} $cm^{2}V^{-1}s^{-1}$ and 7.49×10^{12} cm^{-3} at 77 K under light, being similar to the highest value reported by Amano et al [8]. The detail of the LPE system used here is reported in ref. 2.

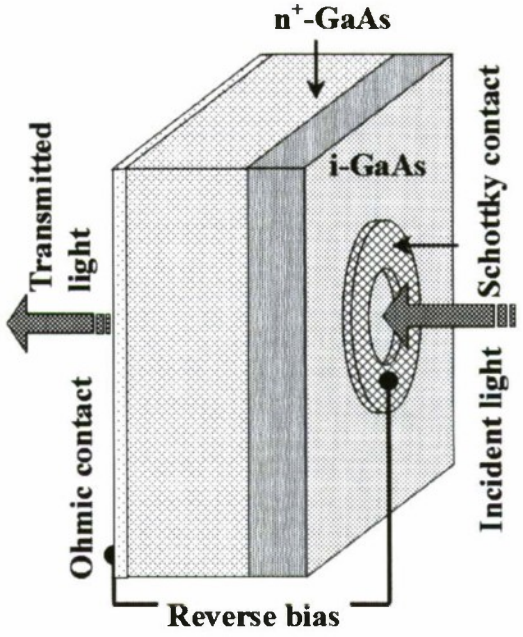

Fig. 2. Schematic diagram of SLM

The Schottky and the Ohmic contacts were formed by depositing an Au and Au/Ge/Ni on GaAs epilayer and the substrate, respectively by thermal evaporator. Then the contact was annealed at 400°C for 4 min in H_2 gas flow. The device contacts have a small window with 300 μm diameter in each contact in order to transmit an incident light. The sample configuration of SLM is shown in Fig. 2.

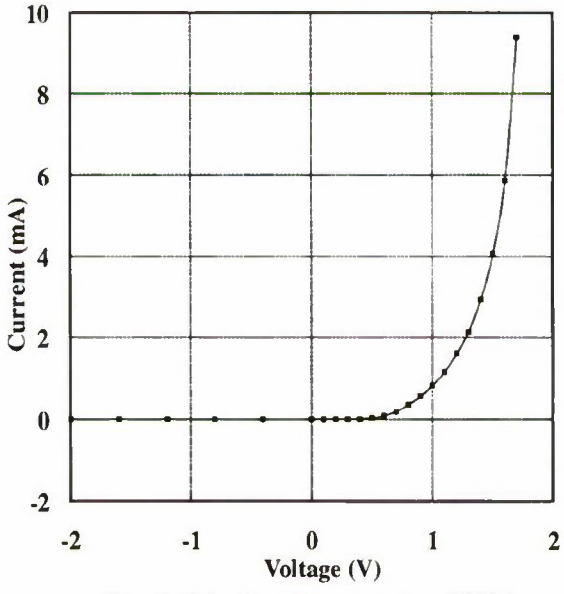

Fig. 3. Schottky characteristic of SLM

The Schottky characteristic and reverse bias characteristic of SLM are shown in Figs. 3. and 4, respectively. The built-in voltage for SLM is about 0.8 V. SLM has low leakage current of 112 μA at 19.6 V and high breakdown voltage (over 40 V). This figure was obtained under light.

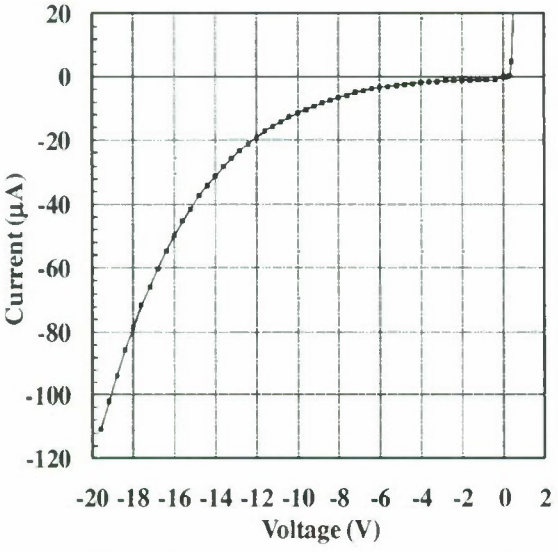

Fig. 4. Reverse bias characteristic of SLM

The voltage dependent optical transmission of SLM was measured using a laser diode operating at 897 nm. The emitted light was coupled to a standard SMF with a lens and launched perpendicularly to epilayer surface. Then, the transmitted light was coupled from the sample backside using a standard SMF and detected by optical spectrum analyzer. The experimental conditions are same as explained in paragraph 3 of section II.

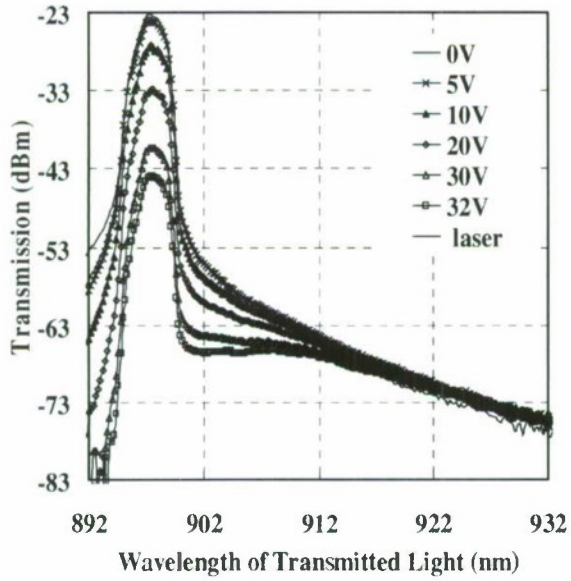

Fig. 5. Transmission characteristics of SLM

Figure 5 shows transmitted spectra for SLM as a function of reverse bias. It is clear that the laser transmitted light is nonsymmetrical (i.e. for a wavelength slightly shorter than 897 nm the absorption is large, while for longer wavelength it is small as wavelength increases) because of EA effect.

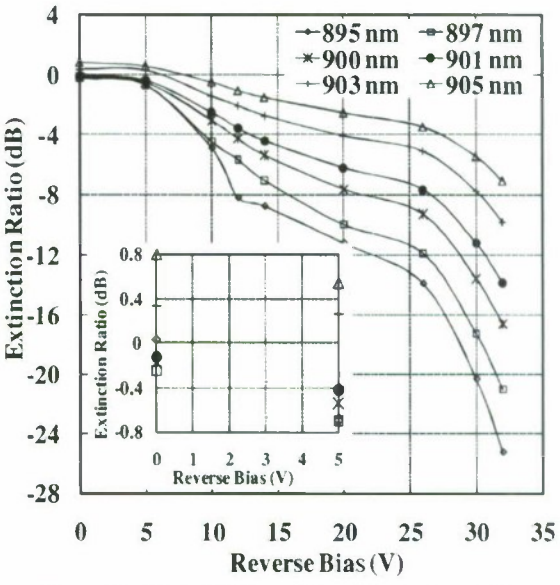

Fig. 6. Extinction ratio vs. reverse bias voltage at different wavelength

Extinction ratio vs. reverse bias for the wavelength from 895 to 905 nm is shown in Fig. 6, which is calculated from Fig. 5 for the wavelengths 895, 897, 900, 901, 903 and 905 nm. Very little extinction ratios change upto 5 V and then increase gradually. Upto 25 V some change has been observed with applied voltage, while after 25 V the light intensity abrupty decreases. Extinction ratio of 25 dB for the voltage of 32 V at wavelength 895 nm was obtained under the detuning energy of 40 meV. This is relatively low voltage ever reported. The inset figure shows magnification of the same figure at 0 and 5 V.

The two bumps observed in Fig. 6 can be due to two factors. The first one may be due to effect of the electric field on the depletion layer, and another is due to Franz-Kedysh effect [9][10] which shifts absorption edge to longer wavelength. The widening of the depletion region starts after 6 V and the reach-through takes place at 25 V as the electric field increases.

III. DISCUSSION

The SLM has 300 μm windows. We will discuss electric field intensity distribution in the i-layer and the depletion width based on Fig. 6. as the

following. The depletion width is estimated to be over 150 μm at the applied voltage of 26 V because the window diameter is 300 μm.

Using the relationship between depletion width and impurity concentration [11], impurity concentration is estimated to be 2.32×10^{12} cm^{-3} and 7.09×10^{11} cm^{-3} under reverse voltage 33 and 10 V, respectively. Therefore, we assume depletion width to be 150 μm at 26 V. Net carrier concentration calculated from capacitance-voltage (C-V) measurement gives similar value. The low impurity concentration of device indicates donor and acceptor are highly compensated to each other.

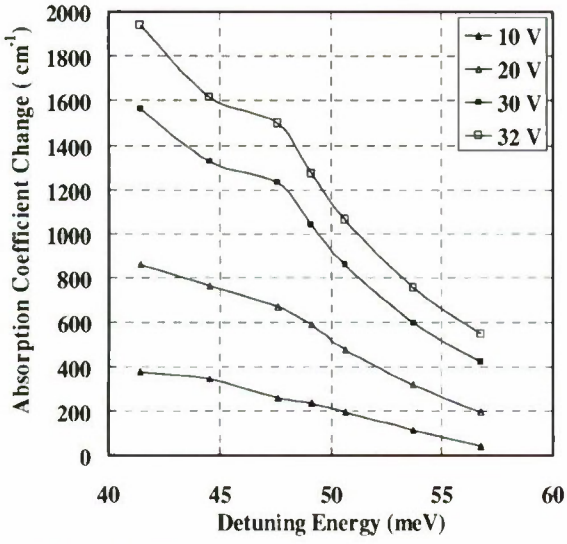

Fig. 7. Absorption coefficient vs. detuning energy

The absorption coefficient change vs. detuning energy is shown in Fig. 7, which is obtained from Fig. 6. The detuning energy (△E) can be defined as the energy difference between exciton peak and incident light wavelength. The smaller the detuning energy, the larger the absorption coefficient change. The driving voltage of the device can be reduced by using shorter wavelength light source.

The device capacitance is 20 pF as given from C-V measurement. When we assume the drive impedance to be 50 Ω, we obtain time constant (RC) of 1 ns.

IV. CONCLUSION

We were able to fabricate SLM using ultrahigh purity and 30 μm thick GaAs epilayer. The extinction ratio of 25 dB is obtained at operating voltage of 32 V at 895 nm. Calculated value of impurity concentration indicates donor and accepter are of the device are highly compensated. The device capacitance is estimated to be 20 pF, which will be reduced by optimizing the size. The speed is limited by RC time constant. Therefore, we are now investigating high-speed operation as well as integration of many devices.

Acknowledgements

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Enhanced TE/TM electro-optic effect in vertically coupled InGaAs quantum dots

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Abstract

We have investigated the electro-optic effect for the vertically coupled InGaAs quantum dots. In addition to large TE-polarized electro-optic coefficient, TM-polarized electro-optic effect is observed. The linear and quadratic electro-optic coefficients are larger than GaAs-base multiple quantum well structures.

I. Introductions

Self-assembled InGaAs quantum dots (QDs) provide a new platform for the study of semieonduetor photonies. The three-dimensional carrier confinement and the intrinsic strain field are combined for the investigation of device applications. The quantum confinement of electrons and holes has interesting effeet on electro-optie deviees. Beeause of low dimensional quantum confined structures are expeeted to enhanced electro-optic properties [1]. The major ehange is the parabolic density of states in bulk to delta density of states in QDs. And, the lowly dimensional structures increase the binding energy of electron-hole pairs. It will promote the eleetro-optieal eoeffieients.

Conventionally, eombinations of compressive- and tensile-strained multiple quantum wells have been demonstrated to aehieve the polarization insensitivity. For self-assembled InGaAs QDs grown on (001) GaAs substrates, the island structures are under biaxially compressive strain individually. Therefore, transverse-electric (TE) mode [i.e., polarization along the in-plane direetion] is expeeted for the fundamental transition between heavy-hole and eleetron subbands [2]. To inerease the transverse–magnetic (TM) eomponent [i.e., polarization along the growth direction] for the fundamental transition, vertically coupled QDs layers are investigated to relax the strain deformation potential [3,4], and/or to inerease the mixing of heavy-hole (hh) and light-hole (lh) subbands in the ground state [5-7]. Therefore, to eontrol the thiekness of GaAs spacer between QDs layers obtained the vertically eoupled QDs, which can change the quantum eonfinement direetion.

In general, for TE polarization, the index ehange depends on the applied electric field, but, we eould not observe the electrorefraction for TM polarization. Beeause of the eleetrorefraetion of typical structures for TM polarization are no significant dependence on the propagation direction [8]. Here, we measure structure of the vertically coupling InGaAs QDs, use the TE/TM transmission through Fabry-Perot resonators at 1515 nm to determine the electro-optical coefficients.

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II. Experiment

In this paper, we report the study of electro-optic effects both of TE- and TM-polarizations for a vertically coupled InGaAs QDs. The pin structures of triple-layer QDs were grown by MBE on (100) n^+-GaAs substrates, as shown in Fig. 1. The active region consists of triple stacked self-assembled $In_{0.75}Ga_{0.25}As$ QDs were of 3.4 ML coverage at a growth rate of 0.1μm/hr. After the growth of QDs at a substrate temperature (T_s) of 510°C, a 10-nm $In_{0.1}Ga_{0.9}As$ layer was directly grown on the QDs at the same T_s. Then, the T_s was raised to 580°C for the growth of GaAs spacer layer. Each QD layers is separated by 5nm GaAs spacer layer. Vertically aligned QDs of 5-nm GaAs spacer was directly revealed in transmission electron microscopy (TEM) image [9]. The density of each layer of InGaAs QDs is $3x10^{10}/cm^2$. The structure cavity is clad by $Al_{0.5}Ga_{0.5}As$. On the top and substrate side is p-doped and n-doped GaAs, respectively.

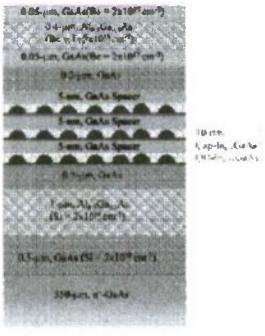

Fig. 1 Schematic structure of triple-layer QDs

Ridge waveguides are fabricated by dry etching in $SiCl_4$: Cl_2:CH_4= 10 : 3 : 6 down to 1μm. Deposition of 300 nm thick SiO_2 protect waveguides. The p-contact (Cr/Au) is formed by thermal evaporation and lift-off. After p-contact deposition, the substrate is thinned down to 150μm and the n-contact (Au/Ge/Au) is deposited on the substrate side. Fabry-Perot measurement at 1515 nm was carried out by a TE/TM polarized light from a tunable laser through the fiber polarization controller [10]. The end of 1.52 mm long waveguide is collected light with lens fiber. The applied electric field by DC voltage is perpendicular to the epitaxy layers. The phase retardation of the output light from another facet propagating through the ridge waveguidc was measurement with InGaAs detector and power meter.

III. Result and Discussion

Experimental results are shown in Fig. 2. Firstly, we measured Fabry-Perot resonances by TE polarized light, as shown in Fig. 2 (a). Through the Fabry-Perot transmission equation, we can calculated the TE mode effective index (n_{eff}= 3.367). Voltage-dependent spectral shift is observed for TM polarization, as shown in Fig. 2 (b). And the TM mode effective index (n_{eff}) is 3.355. In Fig. 2(a), it reveals that on/off modulation is possible using 5V.

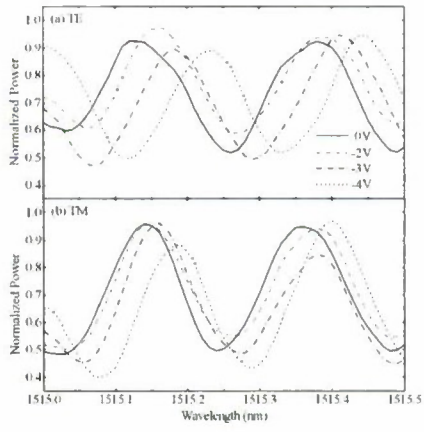

Fig. 2 Voltage dependent shift of Fabry-Perot resonances is observed for (a) TE and (b) TM polarization.

We simulated the structure mode profile by Fimmwave. The confinement factor (Γ) is the overlap optical mode intensity. For the Γ values of the TE and TM polarization are 0.07, and 0.061, respectively. And the simulated results for TE and TM index is 3.27and 3.26, respectively. We measured the shift in the Fabry-Perot resonance under reverse-bias voltages. The index

change is related to the phase shift [8]. The phase retardation and refractive index change as a function of reverse bias, as shown in Fig. 3. In order to obtained the linear and quadratic electro-optic coefficients by fitting the measured phase retardation with the relation [11]. The relation is

$$\Delta\phi = \pi L n_0^3 \lambda^{-1} (\Gamma r E + \Gamma s E^2), \qquad (1)$$

Where L is the waveguide length, n_0 is the effective refractive index in the active region, E is the electric field in the intrinsic region, r and s are the linear and quadratic electro-optic coefficients, respectively, Γ is the confinement factor.

For TE polarization shown in Fig. 3 (a), the linear (r) and quadratic (s) electro-optic coefficient are $2.99\text{x}10^{-12}$ m/V and $4.10\text{x}10^{-18}$ m^2/V^2, respectively. Another, TM polarization shown in Fig. 3 (b), the quadratic (s) electro-optic coefficient is $3.52\text{x}10^{-18}$ m^2/V^2. The electro-optic coefficients are larger than GaAs bulk and GaAs-base quantum well [11-14]. Because of the low-dimensional quantum confined structures enhanced oscillator strengths [1].

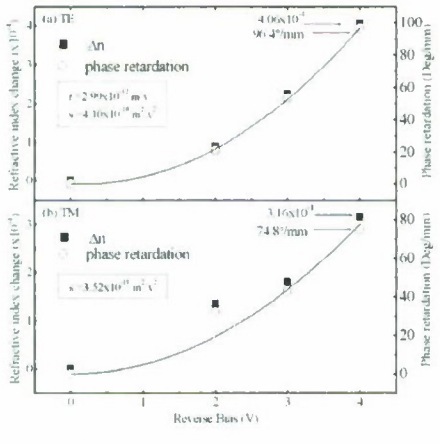

Fig. 3 Refractive index change and phase retardation as a function of reverse bias for (a) TE and (b) TM polarization. The curve is a fit to the measured data of phase retardation.

IV. Conclusion

In conclusion, the triple vertically coupled quantum dot structures can clearly observe voltage-dependent spectra shift for TE and TM polarization. And the electro-optic coefficients of InGaAs quantum dot larger than GaAs bulk. It is provided a chance for polarization-insensitive electro-optic devices.

V. Acknowledgement

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DEPENDENCE OF THRESHOLD CURRENT DENSITY ON QUANTUM WELL COMPOSITION FOR COMPRESSIVE STRAINED-LAYER $Al_xGa_yIn_{1-x-y}As$ LASERS

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Abstract

Separate confinement AlGaInAs/InP compressive strained quantum well lasers especially in the wavelength range of 1.55 μm and 1.3 μm with 7.6 nm well thick have been studied. Threshold current density and emission wavelengths have been calculated as a function of well composition. A minimum of threshold current density of 146 Acm^{-2} was obtained for the devices with $Al_{0.1}Ga_{0.16}In_{0.74}As$ well which is the lowest value ever reported at this well composition.

I. Introduction

At present, the thermoelectric cooler is essential in most of the modules using the InGaAsP-InP lasers because these lasers generally show too weak temperature characteristic. It has been generally well known that the poor temperature characteristics of the InGaAsP-InP multiple quantum well lasers are due to the small conduction band offset (ΔE_c = 0.4 ΔE_g), which causes the poor electron confinement in quantum wells. Recent years, another material system such as AlGaInAs-InP has been attracting much attention because it has a larger conduction band offset (ΔE_c = 0.72 ΔE_g) showing the strong electron confinement in the wells. Since superior characteristic has been proposed by Zah et al.[1] for 1.3 μm AlGaInAs-InP lasers with compressive and tensile strain. The main cause of low characteristic temperature is due to the leakage carrier from the active layer into the cladding layer which has been reported as [2].

In this paper we have studied the effects of well composition on threshold current density operating at 1.55 μm and 1.3 μm for AlGaInAs-InP compressively strained single quantum well lasers. We also have reported the lower threshold current density for 1.3 μm with slightly higher electron confinement energy than that of reported as [1]. As for 1.55 μm, we have obtained the lower threshold current density and higher electron confinement energy than those of reported as [2] which is the lowest value ever reported at this wavelength.

II. Calculation Method

A) Optical gain

Due to intraband relaxation process such as electron–electron collision etc., broadening occurs in the gain spectrum of semiconductor lasers. The linear gain for bulk lasers is given as [3] by taking into account of the intraband relaxation time and for quantum well laser it is written as

$$g(\omega) = \omega\sqrt{\mu/\varepsilon}\, R_{ch}^2 \int_0^\infty \frac{(f_c - f_v)(\hbar/\tau_{in})}{(E_{ch} - \hbar w)^2 + (\hbar/\tau_{in})^2} \frac{kdk}{\pi d} \tag{2.1}$$

Where, ω is an angular frequency, μ is permeability, ε is dielectric constant, R^2_{ch} is the dipole moment between conduction band and valence band for quantum well, $\hbar$ is reduced Plank constant, τ_{in} is intraband relaxation time, k is wave vector, E_{ch} is a transition energy between the conduction band and valence band, d is well thickness and f_c and f_v is Fermi distribution function of conduction band and valence band, respectively which is given by

$$f_c = \left[1 + exp\{(E_{cn} - E_{fc})/KT\}\right]^{-1} \tag{2.2}$$

$$f_v = \left[1 + exp\{(E_{hn} - E_{fv})/KT\}\right]^{-1} \tag{2.3}$$

In Eqs. (2.1), (2.2) and (2.3), we have supposed that the electron and hole in the well are in equilibrium determined by the quasi-Fermi levels E_{fc} and E_{fv} respectively.

E_{fc} and E_{fv} are related to the electron and hole densities injected into the well as

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$$N = \frac{m_c^* KT}{\pi\hbar^2} \sum_n ln\left[1 + exp\left\{ E_{fc} - \varepsilon_{cn} \right) / KT \right\}\right] \quad (2.4)$$

$$P \approx \frac{m_v^* KT}{\pi\hbar^2} \sum_n ln\left[1 + exp\left\{ E_{fv} - \varepsilon_{hn} \right) / KT \right\}\right] \quad (2.5)$$

In Eqs. (2.1), (2.4), and (2.5) we have assumed the transition from the conduction band to the heavy hole valence band because the density of states of light hole band is smaller that that of the heavy hole band.

The compressively strained band gap of $Al_xGa_yIn_{1-x-y}As$ material has been calculated as [4]

$$E_g(Al_xGa_yIn_{1-x-y}As) = 0.572 + 1.517x$$

$$(1\text{-}x\text{-}y = 0.74) \quad (2.6).$$

Where x is aluminium composition in well, y is gallium composition of well and $1\text{-}x\text{-}y$ is indium composition of well. In order to find the right material composition of quantum well for 1.55 μm and 1.3 μm, we have calculated the lasing wavelength as a function of well composition (x) as shown in Fig. 1.

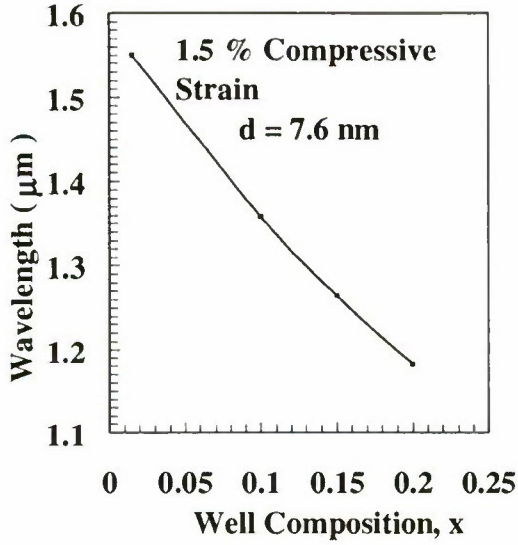

Fig. 1 Calculated lasing wavelength as a function of aluminium composition in well.

The dependence of conduction band effective mass on aluminium composition of $Al_xGa_yIn_{1-x-y}As$ material can be written as [5].

$$m^* = 0.0427 + 0.683x \quad (2.7)$$

B) Threshold currenty density

The threshold carrier density is calculated with the following equation

$$N_{th} = \frac{L}{\Gamma a L_c} + N_{tr} \quad (2.8)$$

Where L is total loss, Γ is optical confinement factor, a is differential gain, L_c is cavity length and N_{tr} is transparency carrier density.

The threshold currenty density using threshold carrier density (N_{th}) is written as [6].

$$J_{th} = \frac{qdN_w N_{th}}{\tau_s} \quad (2.9)$$

Where q is electron charge, N_w is the numbers of wells and τ_s is carrier life time. Here we have condidered as single quantum so that N_w=1.

III. Results and Discussion

We have calculated the lasing wavelength as a function of well composition with 1.5 % of compressive strain by fixing electron confinment energy of 259 meV and 156meV, respectively as shown in Fig. 1. The electron confinement energy is defined as the energy between first quantised level and the top of the barrier layer. This energy depends on the barrier composition, conduction band off-set, well composition and well thickness.

The electron confinment energy for different well composition is shown in Fig. 2. In Table 1, we have showed the electron confinement energy for 1.3 μm lasing wavelength (λ) about 165 meV which is slightly larger to that of reported as[1]. In this study we have taken band gap for barrier of 1.16 eV.

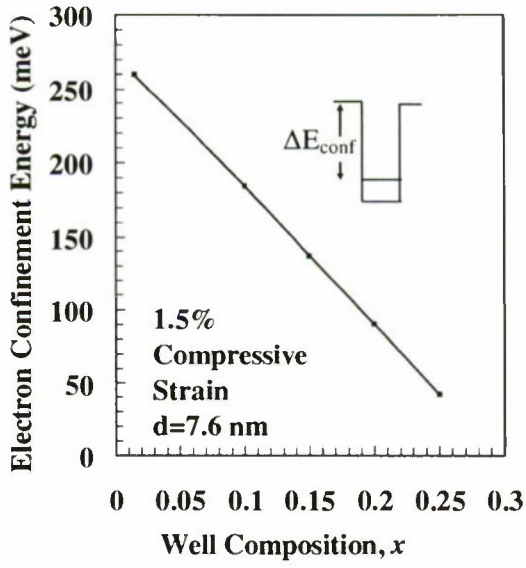

Fig. 2. Calculation of electron confinement energy as a function of well composition with 1.5% compressive strain.

We have calculated the threshold current density for $Al_xGa_yIn_{1-x-y}As$ as a function of well composition at different values of well thickness by using Eq. (2.8). The minimum of threshold current density (J_{th}) at an aluminium mole fraction of 0.1 as shown in Fig. 3, is explained by taking into account of two effects. For high aluminium fraction in well, the carriers are poorly confined, while for low fraction, the effect of strain results in increase in J_{th}. These two effects are shown in Fig. 3.

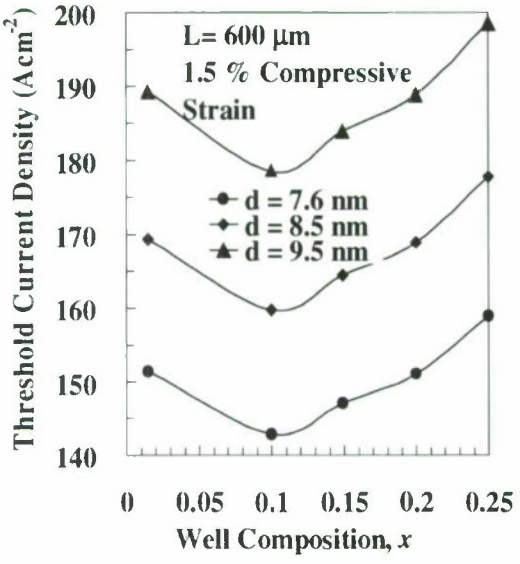

Fig. 3. Calculated threshold current density as a function of well composition at different well thickness.

For high aluminum fraction in well, the confining energy ΔE_{conf} between the conduction band and the barrier is small. ΔE_{conf} have been calculated as the same method as the wavelengths of Fig. 1. From the basic principle concerning carrier distribution, it can simply say that a confining energy of at least a few times more than KT (90 meV) is necessary to obtain good carrier confinement in the well. Smaller confinement energy results in a significant part of electron population in the active region having energies greater than the barrier height, and a corresponding higher density of electrons in the barrier. Similar assumption can apply to the confinement of holes in the valence band.

The electrons are weakly confined for devices having aluminum composition of 0.25 in the well because ΔE_{conf} (~ 42 meV) is only of the order of KT. For this device, J_{th} is high compared with J_{th} for devices with 0.2 composition in the well. The threshold current density decreases as the aluminum fraction in the well decreases, since the well is made deeper and the electron bound state is better confined. In this study J_{th} tends to decrease as aluminum content reaches to 0.1. Then the strain begins to adversely influence the performance of laser after below the aluminum content of 0.1. Since under compressive strain, effective mass of hole in parallel to junction plane decreases to a value close to effective mass of electron, then transparency carrier density reduces. As a result, we can obtain higher differential gain.

Figure 4 shows the inverse relationship between the differential gain and composition of aluminum in the well. Therefore J_{th} slightly increases upto the aluminum composition of 0.015 and sharply increases below aluminum composition of 0.015. The lowest value of threshold current density was obtained for aluminum composition of 0.1 with 7.6 nm thick well. The combination of well composition and thickness for the device in this study is such that electrons are sufficiently confined in the well (ΔE_{conf} ~ 183 meV).

In all devices with aluminium composition in the range from 0.015 to 0.2, where ΔE_{conf} is greater than 90 meV so that the performance of devices in this range will be optimized and otherwise J_{th} is increased. We emphasize that there are more options in the choice of well composition and well thickness that will give low threshold current density, high efficiency at the required lasing wavelength. The lower threshold currenty density was obtained for 7.6 nm thick well of 15 % compressive strain with 0.13 aluminium mole in the well. This lower value of J_{th} is smaller than that of 1.3 μm reported as [1] because of high electron confinement energy. For 1.55 μm, J_{th} is estimated to be smaller than that of the reported as [2] with aluminium composition of 0.015 with optimum higher electron confinement energy as shown in Table 2.

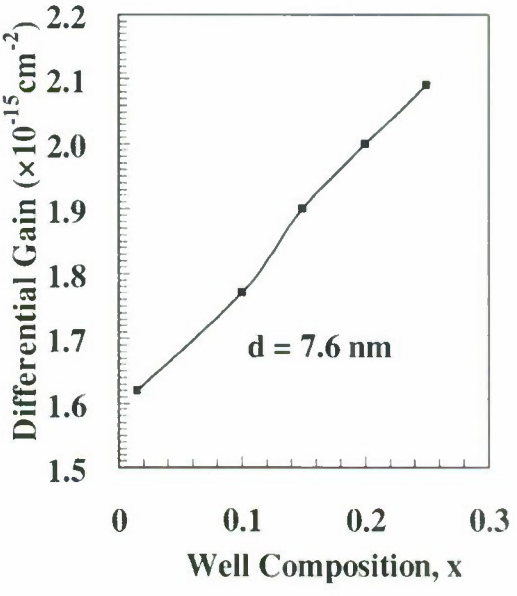

Fig. 4 Calculated differential gain as a function of well composition with well thickness of 7.6 nm.

The variation of J_{th} with cavity length for device with $Al_{0.015}Ga_{0.245}In_{0.74}As$ well is shown in Fig. 5. These devices show the usual decrease in the J_{th} as increasing of cavity length as a result of proportionally decreasing of mirror loss remaning the constant mirror reflectivity. One can see that the intervalence band absorption loss reduces the characteristic temperature of all lasers. To minimise the temperature sensitivity of the threshold current either increasing more quantum well or reducing the mirror loss. Here we have studied about the single quantum so that

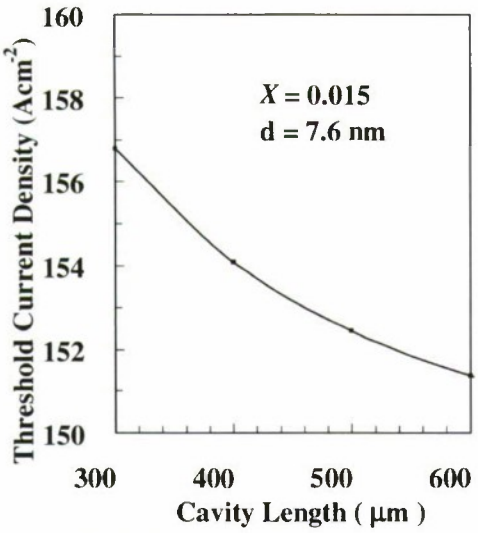

Fig. 5 Calculation of threshold currrent density as a function of cavity length

Table 1: Parameters used in calculation for λ =1.3 μm

Parameter	Value	Units
m_c	0.0449	m_o
m_v	0.08	m_o
E_g	0.594	eV
ΔE_c	0.4	eV
ΔE_v	0.158	eV
x	0.015	mole

Table 2: Parameters used in calculation for λ =1.55 μm

Parameter	Value	Units
m_c	0.05	m_o
m_v	0.08	m_o
E_g	0.75	eV
ΔE_c	0.292	eV
ΔE_v	0.11	eV
x	0.12	mole

it is possible only by reducing the mirror loss. For this we have used 600 μm as a cavity length for 1.55μm and 1.3 μm lasing wavelength to minimize the temperature sensitivity of threshold current density.

IV. Summary

We have reported the results of different characteristic of strained layer $Al_xGa_yIn_{1-x-y}As$ single quantum well lasers by calculating of 1.5 % compressive strained single quantum well with 7.6 nm thick and aluminium mole fraction between 0.015 to 0.15. The emission wavelengths ranged from 1.2 to 1.55 μm have low threshold currenty density. The higher differential gain due to 1.5 % of compressive strained well have been shown in this study. The threshold current density was obtained for devices at 1.3 μm and 1.55 μm having aluminium mole fraction of 0.13 and 0.015 in well which is smaller than that of reported results. We also concluded that the electron should be confined by at least 90 meV in the conduction band and the devices having the well composition between 0.015 and 0.2 can operate with low threshold current density. We also obtained absolute low value of 146 Acm^{-2} with alumonium composition of 0.1 with 7.6 nm thick well. The parameters support to design criteria for low threshold operation of strained layer $Al_xGa_yIn_{1-x-y}As$ for lasing wavelength of 1.55 μm and 1.3 μm have been reported.

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Thermal Performance of 1.55μm InGaAlAs Quantum Well Buried Heterostructure Lasers

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***Abstract*— We have investigated the threshold current I_{th} and differential quantum efficiency as the function of temperature in InGaAlAs/InP multiple quantum well (MQWs) buried heterostructure (BH) lasers. We find that the temperature sensitivity of I_{th} is due to non-radiative recombination which accounts for up to ~80% of J_{th} at room temperature. Analysis of spontaneous emission emitted from the devices show that the dominant non-radiative recombination process is consistent with Auger recombination. We further show that the above threshold differential internal quantum efficiency, η_i, is ~80% at 20°C remaining stable up to 80°C . In contrast, the internal optical loss, α_i, increases from 15 cm^{-1} at 20°C to 22 cm^{-1} at 80°C, consistent with inter-valence band absorption (IVBA). This suggests that the decrease in power output at elevated temperatures is associated with both Auger recombination and IVBA.**

I. Introduction

Uncooled InGaAlAs based multiple quantum well buried heterostructure (BH) lasers show great promise for low power-consumption operation data communication links [1]. Recently 1.3 μm InGaAlAs BH lasers have shown good temperature characteristics for uncooled operations [2]. There are, however, relatively few reports on 1.55 μm InGaAlAs BH lasers [3-6]. Semiconductor lasers emitting at 1.55 μm are the most desired light sources for high speed optical transmission due to the lowest loss window region of silica-based fiber optics occurring around this wavelength [7].

Conventional InGaAsP/InP based QW lasers are inefficient as at these wavelengths their characteristics have relatively high temperature sensitivity. Therefore such lasers require the use of expensive cooling devices to stabilise the laser operation temperature [4]. Due to the larger potential conduction band offset ratio of the InGaAlAs/InP material system of around $\Delta E_c = 0.7\Delta E_g$ compared to $\Delta E_c = 0.4\Delta E_g$ for the InGaAsP/InP heterostructures, the former material system has stronger electron confinement, reduced Auger recombination and reduced threshold current [1-5]. Hence InGaAlAs lasers have better temperature characteristics at wavelengths between 1.3μm and 1.55μm. However, a concern with processing of the Al-containing layers has limited progress in the development of BH lasers based upon this material system.

II. Theory

The current I flowing through a semiconductor laser can be simply written as

$$I = eV(An + Bn^2 + Cn^3) + I_{leak} \qquad (1)$$

where e is the electron charge, V is the volume of the active region, and n is the carrier density (assuming that the electron and hole densities are equal). The An term corresponds to the current associated with carrier recombination at defects and impurities in the material. In high quality devices it can be assumed negligible [8]. The Bn^2 term corresponds to spontaneous emission in which an electron and a hole recombine to give out a photon, hence forming the radiative current I_{rad}. The Cn^3 term corresponds to non-radiative Auger recombination whereby a third carrier is excited higher into its respective band, the carrier subsequently relaxes through phonon emission and is therefore a non-radiative process resulting in heat. I_{leak} describes the current due to leakage of carriers from the quantum wells and subsequently recombine radiatively or non-radiatively. Carrier leakage depends on the thermal spread of the carriers at the operation temperature and the height of the potential barrier.

As first proposed in [9], we can approximate equation (1) as $I \propto n^z$ where z depends on the dominant recombination process. If the current is dominated by radiative recombination then z=2 while if Auger recombination is dominant then z=3. Intermediate values of z can indicate the influence of more than one process. Since the integrated spontaneous emission rate, L, is directly proportional to the radiative current I_{rad}, one may write that $L \propto I_{rad} \propto n^2$ and hence write $I \propto (L^{1/2})^z$. The z-value can then be obtained from the gradient of a graph of $ln(I)$ versus $ln(L^{1/2})$, evaluated using the following expression:

$$z = \frac{d\ln(I)}{d\ln(L^{1/2})} \qquad (2)$$

In this analysis we assume that the recombination coefficient B is independent of n. The method used agrees with theoretical calculations over the temperature range covered in this investigation [10]. The temperature sensitivity of the threshold current of the semiconductor laser may be described as

$$\frac{1}{T_o(I_{th})} = \frac{1}{I_{th}}\frac{dI_{th}}{dT} = \frac{d\ln(I_{th})}{dT} \qquad (3)$$

From equation (3) we can deduce that a high $T_o(I_{th})$ indicates low temperature sensitivity and vice versa. In an ideal laser, the radiative current at lasing threshold saturates due to the pinning of the carrier density caused by stimulated emission [10]. In an ideal QW, at threshold, the radiative recombination coefficient is inversely proportional to temperature ($B \propto T^{-1}$) and the carrier density, $n_{th} \propto T$ [11].

From the equation (3) we can deduce T_0 parameter for the radiative component of the threshold current, $T_o(I_{rad})$, to be

$$T_0(I_{rad}) = T \qquad (4).$$

For the Auger current, the temperature sensitivity $T_o(I_{non\text{-}rad})$, assuming that the Auger coefficient, C, is independent of temperature, the temperature sensitivity for the Auger recombination process can be approximated as

$$T_0(I_{Auger}) = \frac{T}{3}. \qquad (5)$$

We note that these are effectively upper limits on $T_0(I_{rad})$ and $T_0(I_{non\text{-}rad})$.

III. Experiment

The samples used were InGaAlAs multiple quantum well buried heterostructures lasers grown on InP substrates using

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MOVPE technology. These were then fabricated into BH lasers and used a reverse biased p-n current blocking layer to minimize current leakage. The BH is the most common lateral wave-guiding structure exhibiting a strong index step and current confinement which results in a low threshold current for lasers [12]. The samples used were 1.55 μm lasers consisting of 9 compressively strained (1.6%) InGaAlAs quantum wells contained within unstrained InGaAlAs barriers and separate confinement layers grown on an n-doped InP substrate.

The lasers were cleaved into cavity lengths ranging from 350μm to 1000μm. The BH mesa width was measured to be 1.57 μm. The devices were measured as-cleaved. CW current was used for measurements from 80K to 240K and pulsed current (500ns pulse width at 10 kHz repetition rate) was used from 260K to 370K to avoid self heating effects.

Pure spontaneous emission measurements were carried out by collecting light from a window created in the laser substrate contact using an ion-beam milling technique. The windows were approximately 200 μm by 50 μm in size. The lasers threshold currents were measured before and after milling to ensure that the milling has not damaged the devices or introduced changes in the active region. A multimode optical fiber was used to collect the light. This fiber was connected to an Optical Spectrum Analyser (OSA). The temperature was controlled using a gas-exchange cryostat from 80K up to 370K.

IV: RESULTS AND DISCUSSION

A. Pinning effect, Radiative and Non-radiative current

Fig. 1 shows integrated spontaneous emission L as a function of current. Fig. 1 demonstrates the devices excellent pinning behaviour of the spontaneous emission above laser threshold. This indicates that the carrier density is well pinned in the structure, and suggests that the lateral current blocking structure in the BH is effective.

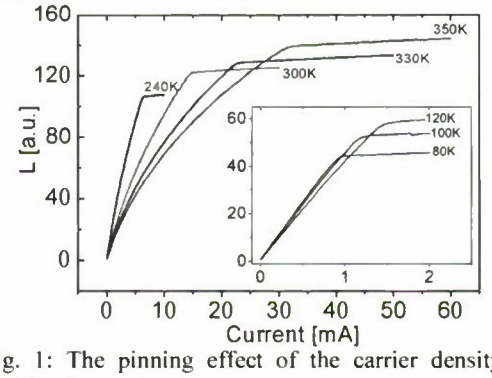

Fig. 1: The pinning effect of the carrier density at lasing threshold current.

Fig. 3 shows the temperature dependence of the threshold current (squares) and its radiative component (circles). The radiative component, I_{rad}, is determined from the pinning level of the spontaneous emission (since $L \propto I_{rad}$ and where we assume that $I_{th}=I_{rad}$ at low temperature).

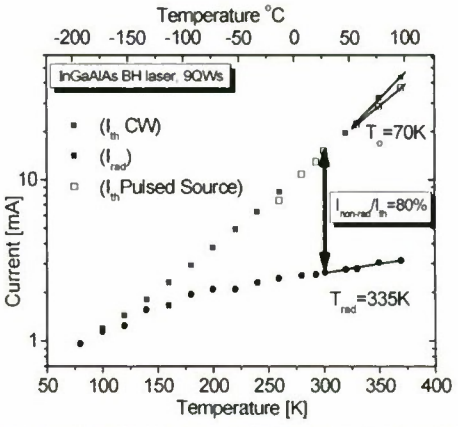

Fig. 3: Temperature dependence of the lasing threshold current and its radiative component I_{rad} for InGaAlAs MQWs BH lasers.

It can be observed that at 300K, I_{rad} forms approximately 20% of the threshold current and is much less temperature sensitive than the threshold current. This represents a maximum estimate for I_{rad} assuming that the defect related recombination and carrier leakage are negligible in our devices at low temperature. This assumption is supported by the results from z-analysis (shown later in this paper).j Around RT, the T_0 for the threshold current of these devices is ~70K. Whilst this is better than typical InGaAsP lasers (~50K) [11], we note that it is still much lower than the T_o of the radiative component of the threshold current, for which $T_o(I_{rad})$=335K over the same temperature range. This suggests that the temperature dependence of the gain is relatively stable and that the overall temperature sensitivity of the threshold current must be due to a non-radiative process.

B. Z-Analysis

To further understand the nature of the non-radiative recombination process we employed z-analysis method to determine the carrier density dependence of I_{th} as described in section II. By analyzing the slope of a graph of $ln(I)$ versus $ln(L^{1/z})$ just below threshold current. In Fig. 4 we plot z-values obtained at different temperatures.

It can be observed from Fig. 4, that z-value is ~2 from 80K to 140K, indicating that the current is dominated by radiative recombination ($\propto n^2$). From 150K to 350K, the measured z-value increases with increasing temperature stabilizing around ~3 at RT. This indicates that the dominant non-radiative recombination process is Auger recombination ($\propto n^3$) which becomes dominant above 250K. It is known that in longer wavelength lasers Auger recombination process becomes much more significant because its rate increases strongly as the band gap decreases [13].

We note that a z-value of 3 could also be a signature of leakage, since the leakage current has an approximately exponential dependence on n which can effectively give rise to any value of n, since the exponential can be expanded as a power series in n.

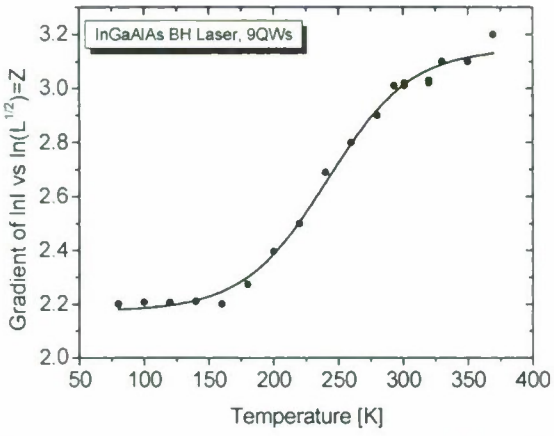

Fig. 4. Variation of z –value with temperature from 80K to 350K for 1.55μm InGaAlAs BH lasers

However, the fact that z stabilizes around 3 suggests that this is not the case, and that Auger recombination is, in fact, dominant.

C. Differential Quantum Efficiency

The variation in the differential quantum (slope) efficiency with temperature can also lead to a strong dependence of the laser output power on temperature and can be influenced by a number of factors. The same samples were used to investigate the external differential quantum efficiency η_d as a function of temperature. The differential quantum efficiency is obtained from the slope above threshold of the graph of optical output power from the laser facet, P_{out}, versus current, I, as

$$\eta_d = \frac{2e}{h\nu}\frac{dP_{out}}{dI} \qquad (6)$$

where $h\nu$ is the photon energy of the laser light. In Fig. 5 we show the variation of the differential quantum efficiency with temperature for these devices (quantified via the T_1 parameter, as defined in the inset). The measurements show that the devices exhibit a sharp drop in η_d at temperatures above 260K as shown in Fig. 5. From Fig. 3, we note that the non-radiative process becomes important from around 150K so the sharp drop in η_d above 260K is likely to have a different underlying cause. Since we know that the carrier density pinning is well behaved with temperature, this suggests that this is due to either an increase in internal loss with increasing temperature or a decrease in the internal differential quantum efficiency, η_i, with increasing temperature.

To identify the key factors responsible for the strong temperature sensitivity of η_d, we undertook a study of the cavity length dependence of the slope efficiency. Since only a fraction of the stimulated emission is reflected by the mirrors (assuming mirrors have constant power reflectivity, R, and are confined within the laser), η_d, will be less than η_i [14].

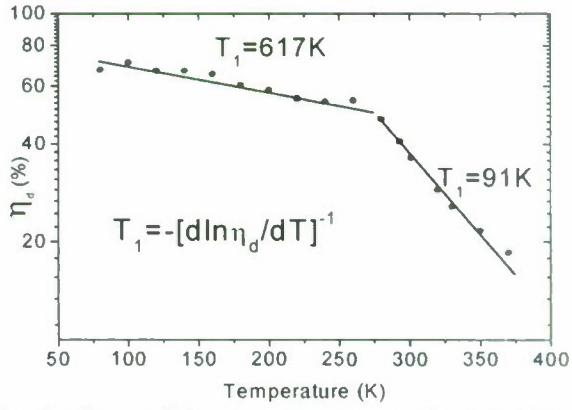

Fig. 5: Slope efficiency vs temperature for InGaAlAs BH lasers

η_d can be related to laser cavity length L_{cav}, and η_i by [15]:

$$\frac{1}{\eta_d} = \frac{1}{\eta_i}\left[\frac{\alpha_i L_{cav}}{\ln\left(\frac{1}{R}\right)} + 1\right] \qquad (7)$$

where α_i is the internal optical loss. The internal optical loss is mainly due to scattering losses, free carrier absorption and inter valence band absorption (IVBA) which affects the differential quantum efficiency [10, 12]. Assuming R=0.3 and using the plot of $1/\eta_d$ versus cavity length L_{cav} we can obtain values for internal differential quantum efficiency, η_i, and internal optical loss, α_i [16]. This method assumes that internal differential quantum efficiency η_i, and internal optical loss, α_i, does not depend on the cavity length of the lasers and carrier density pins above threshold, as we verified in Fig. 1. The internal differential quantum efficiency, η_i, can be defined as the ratio of stimulated photons produced to carriers injected. The value of η_i is consistent with previous work on InGaAlAs devices [8] and better than typical values for InGaAsP BH lasers [16]. By repeating this analysis over a wide temperature range we determine the variation of the internal differential efficiency η_i(T) and internal loss α_i(T).

The internal differential quantum efficiency is found to be almost constant (within uncertainty) over this temperature range and hence cannot be responsible for the decrease in slope efficiency with increasing temperature. This also provides further evidence that a thermally activated carrier leakage mechanism is not the cause of the temperature sensitivity of the threshold current [13].

In contrast, the internal optical loss exhibits a superlinear increase above RT as shown in Fig. 6 (b). This has previously been observed for InGaAsP lasers. The increase in internal optical loss with temperature is most likely attributed to Inter-Valence-Band-Absorption (IVBA) [11]. The effect of

increasing internal loss on external differential efficiency can be seen in Fig. 5 where a sharp drop in efficiency is observed between 260K and 350K. We note that the increase in internal loss with increasing temperature will lead to an increase in n_{th} with temperature and a stronger increase in the Auger current at threshold ($\propto n_{th}^3$) further decreasing T_o, as previous reported for 1.55μm InGaAsP lasers [18].

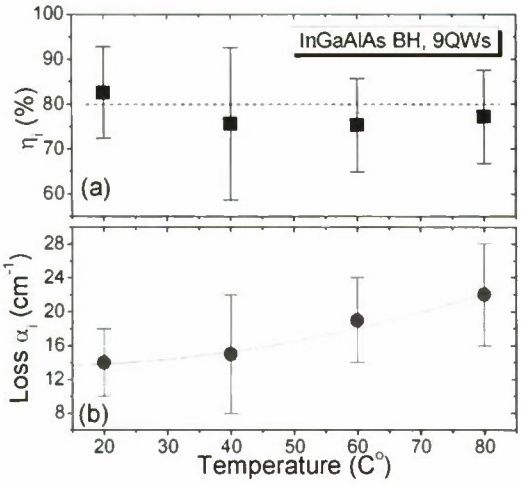

Fig. 6: (a) Internal differential quantum efficiency and (b) internal optical loss as a function of temperature for 1.55μm InGaAlAs BH lasers

V: CONCLUSION

We have analysed temperature dependence of the threshold current and slope efficiency of 1.55μm InGaAlAs/InP BH lasers in terms of radiative and non-radiative currents, internal differential quantum efficiency and internal optical losses. We find that the carrier density is effectively pinned in the lasers, suggesting that the BH blocking is effective. The investigation also confirms the presence of Auger recombination which dominates under ambient conditions. Above room temperature, the internal optical losses showed a superlinear dependence on temperature causing a strong decrease in the slope efficiency. Since internal optical losses are coupled to Auger recombination process, special emphasis in laser design should be placed on reducing internal optical losses to minimize the threshold current and to improve the temperature stability of the devices, allowing for uncooled operation.

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Investigation of Regrowth Interface Quality of AlGaInAs/InP Buried Heterostructure Lasers

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Abstract

1.3-μm AlGaInAs/InP buried heterostructure lasers were prepared by a low-pressure organo-metallic vapor-phase-epitaxy with *in-situ* thermal cleaning. The regrowth interface quality dependence on thermal cleaning time has been investigated from their lasing properties as well as electroluminescence property below the threshold. As the results, under condition of PH_3 atmosphere in the organo-metallic vapor-phase-epitaxy (OMVPE) reactor at a fixed temperature of 450 °C for 60 min cleaning time, successful operation with the internal quantum efficiency of around 81 % and the differential quantum efficiency of 63 % were obtained for the cavity length of 500 μm with cleaved facets.

Keywords: AlGaInAs/InP, Buried-Heterostructure, OMVPE, Thermal Cleaning.

I. INTRODUCTION

To achieve low-cost and low-power consumption semiconductor laser modules for optical communication, AlGaInAs/InP alloy system has been extensively studied [1,2]. Since this alloy system has a lager conduction band offset (ΔE_c = 0.75 ΔE_g) than GaInAsP/InP system (ΔE_c = 0.40 ΔE_g) [3], electrons are well confined even at high temperature operation range and good operation characteristics can be maintained without expensive thermoelectric coolers. On the other hand in optical fiber communication applications, buried-heterostructure (BH) lasers have been used for advantages of low operation current, a stable output beam pattern, high-speed operation, and so on, as compared with a ridge structure [4-6].

However, it is difficult to realize BH lasers based on AlGaInAs/InP system since Al-containing layers are easily oxidized during the fabrication processes and it prevents high quality crystal growth during the embedding growth, resulting in not only poor lasing characteristics but also poor reliability [7].

Therefore, avoiding the oxidation of the Al-containing layer or a removal process of the oxidized Al-containing layer is needed and various methods have been investigated, for example, improvement about the cleaning before regrowth [4,5] and reform the organo-metallic vapor-phase-epitaxy (OMVPE) technique [6,7]. Using these methods, portions of companies dealing with semiconductor lasers have established high quality characteristics [8-10]. However, quantitative studies of regrowth interface quality and lasing characteristics of BH lasers based on AlGaInAs/InP system have not been reported. Accordingly, it is useful to study about cleaning before the regrowth for BH of AlGaInAs/InP system and confirm good condition of that.

In this paper, we would like to report the influence of *in-situ* thermal cleaning in a growth reactor to regrowth interface quality by the estimation of surface recombination rate using spontaneous emission below the threshold current.

II. DEVICE STRUCTURE AND FABRICATION

The fabricated device structure of an AlGaInAs/InP BH laser is shown in Fig. 1. The initial wafer was grown on (100) n-InP substrate by OMVPE technique. It consists of (i) a 500-nm-thick n-InP cladding layer, (ii) a 30-nm-thick n-AlInAs layer, (iii) a 100-nm-thick n-AlGaInAs graded-index separate-confinement-heterostructure (GRIN-SCH) layer, (iv) five fully strain compensated $Al_{0.15}Ga_{0.12}In_{0.73}As$ quantum-wells (QWs)/ $Al_{0.25}Ga_{0.32}In_{0.43}As$ barriers with the corresponding emission wavelength of 1300 nm, (v) a 100-nm-thick p-AlGaInAs GRIN-SCH layer, (vi) a 30-nm-thick p-AlInAs layer, (vii) a 30-nm-thick p-InP layer and (viii) a 30-nm-thick GaInAs layer.

Then various width mesas (2 μm, 3 μm, 5 μm, 7 μm, 10 μm, 20 μm, and 50 μm) were formed by wet and dry etchings using a SiO_2 mask. Firstly, the GaInAs and the Al containing layers (about 450-nm-thick) were etched by a bromomethane solution (Br_2:CH_3OH = 1:1000) to reach n-InP cladding layer. The actual

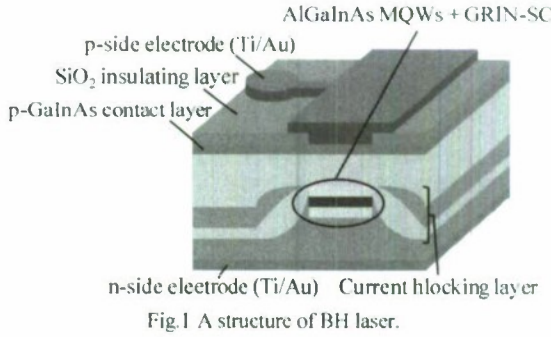

Fig.1 A structure of BH laser.

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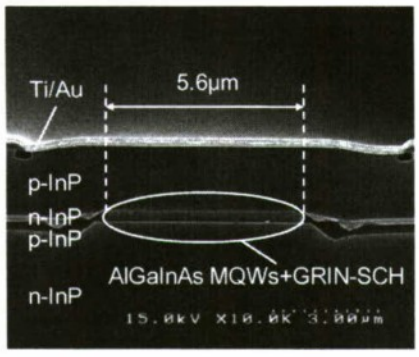

Fig.2 The cross sectional SEM view of 5.6μm wide stripe

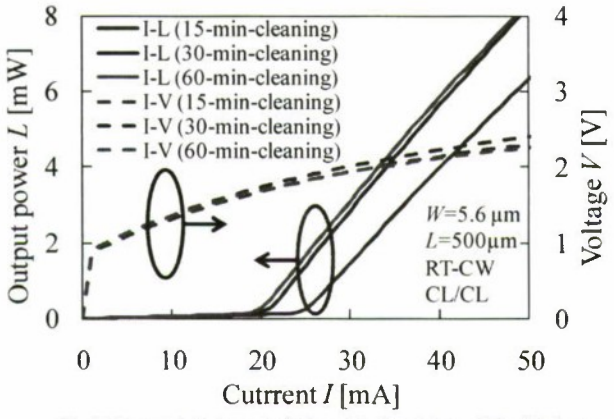

Fig.3 *I-L* and *I-V* characteristics with the stripe width of 5.6 μm

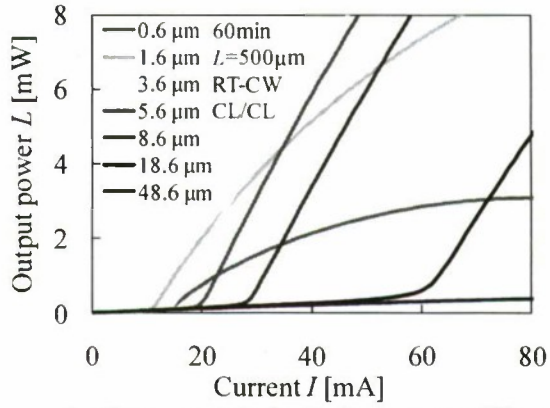

Fig.4 *I-L* characteristics for 60-min-cleaning-L = 500 μm

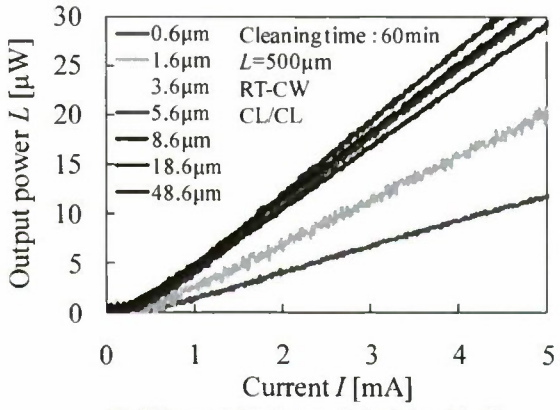

Fig.5 Zoomed *I-L* characteristics below 30 μW for 60-min-cleaning-L = 500 μm

mesa stripe width after this etching was shrieked by about 1.4 μm narrower than from the original mask width since the etching is isotropic. Secondly, CH_4/H_2 reactive-ion-etching (RIE) was done to give 300-nm additional mesa heights. Next, two-step wet cleaning process was employed, i.e. weak bromomethane (Br_2:CH_3OH = 1:40000) which cleans the surface and a mixture of H_2SO_4:H_2O_2:H_2O = 1:1:40 which cleans the Al containing region, and 1% BHF which removes the oxidized layer just before the regrowth.

Then the wafer underwent a thermal cleaning process with a PH_3 atmosphere in the OMVPE reactor to expose fresh regrowth surface prior to the growth of current blocking layers. The reactor temperature was fixed at 450 °C since this temperature had the best characteristics among 250 °C, 450 °C, and 650 °C according to our previous experiment. And the cleaning time was varied for (a) 15 min., (b) 30 min., and (c) 60 min.. The current blocking layers consisting of 100-nm-thick n-InP, 200-nm-thick p-InP, and 200-nm-thick n-InP were selectively grown to bury the mesa stripes. After removing the SiO_2 mask, the wafer underwent the growth of a 2000-nm-thick p-InP cladding layer and a 50-nm-thick p^+-GaInAs contact layer. Ti/Au electrodes were evaporated and laser cavities with the lengths of L = 500 μm, 750 μm, and 1000 μm were made by cleavage.

III. Experimental Results

Due to an undercut during the wet etching, the actual stripe widths confirmed by SEM were 0.6 μm, 1.6 μm, 3.6 μm, 5.6 μm, 8.6 μm, 18.6 μm, and 48.6 μm. The cross sectional SEM view of the device with 5.6 μm wide stripe is shown in Fig.2.

Figure 3 shows *I-L* and *I-V* characteristics of devices with the stripe width of 5.6 μm for the cleaning time of 15min., 30min. and 60 min., respectively. Although *I-V* characteristics were similar to each other, *I-L* characteristics of 15-min-cleaning device were inferior to others in terms of external differential quantum efficiency η_d and threshold current I_{th}. We investigated the reason for these results in terms of the internal quantum efficiency attributed to non-radiative surface recombinations at the regrowth interface.

Figures 4 and 5 show *I-L* characteristics and zoomed *I-L* characteristics below an output of 30 μW, respectively for 60-min-cleaning devices. Dependences on stripe width of threshold current, threshold current density J_{th} and external differential quantum efficiency are listed in Table.1. The device of the stripe width of 48.6 μm didn't operate under CW condition because devices were not die bonded on heatsinks. A minimum threshold current density of 632 A/cm^2 and maximum external differential quantum efficiency η_d of 63 % for 5QWs were achieved at the stripe width of 18.6 μm and 5.6 μm, respectively. J_{th} steeply

Table 1. Dependences on stripe width of threshold currents, threshold current densities and external differential quantum efficiencies.
(60-min-cleaning-L = 500 μm)

Stripe width W [μm]	Threshold current I_{th} [mA]	Threshold current density J_{th} [A/cm²]	External differential quantum efficiency η_d [%]
0.6	12.9	4300	22
1.6	9.5	1188	39
3.6	13.9	772	55
5.6	19.3	689	63
8.6	27.7	644	58
18.6	58.8	632	48

increased and η_d drastically reduced in devices with the stripe width narrower than 1.6 μm. Since the reason for this tendency may be due to non-radiative surface recombinations at the regrowth interface, we evaluated, firstly, the sidewall recombination velocity, denoted by S, from the following relation [11, 12]:

$$\frac{\eta_{sponBH}}{\eta_{sponBH0}} = \frac{1}{1+\frac{2\cdot S\cdot \tau}{W-2W_d}} \qquad (1)$$

where $\eta_{spon,BH}$, is the spontaneous emission efficiency (measured from Fig. 5) under low injection current level, which is 1 mA span of from I = 0.9 mA ($\leq 0.1I_{th}$) to 1.9 mA, and $\eta_{spon,BH0}$ is that of the 48.6 μm wide stripe BH laser with 60-min-cleaning, τ is the carrier life time of the BH structure when S = 0, W is the stripe width and W_d is the so-called "dead layer thickness" but we assume it is negligible in this paper as $W >> W_d$. If there are no defects or non-radiative recombination centers at the regrowth interface, normalized spontaneous emission efficiency $\eta_{spon,BH}/\eta_{spon,BH0}$ should be 1 even at narrow stripe width, which corresponds to smaller $S\cdot\tau$ product.

Figure 6 shows the normalized spontaneous emission efficiency $\eta_{spon,BH}/\eta_{spon,BH0}$ of BH lasers with the cavity length of L = 500 μm as a function of a stripe width. From these data and Eq. (1), $S\cdot\tau$ product was estimated by the least-square method to be 481 nm (not fit well), 331 nm, and 341 nm for the cleaning time of 15min., 30min., and 60 min., respectively. The case of the 15-min-cleanning, $\eta_{spon,BH}/\eta_{spon,BH0}$ didn't reach $\eta_{spon,BH}/\eta_{spon,BH0}$ = 1 even for wide stripe samples. This may indicate quite large non-radiative recombination components not only at the side walls of the stripe. Thus clear improvement was observed for longer thermal cleaning time. Then we compared the $S\cdot\tau$ product for AlGaInAs/InP alloy system with that of GaInAsP/InP system after the same cleaning process (60-min-cleaning) as shown in Fig. 7. The $S\cdot\tau$ product of GaInAsP/InP system was estimated to be 80 nm, which is close to previously reported value of 62 nm [12]. Therefore the $S\cdot\tau$ product of the present AlGaInAs/InP BH structure is still 5 times larger than that of GaInAsP/InP system, there is plenty of room for further reduction of the surface recombinations at the regrowth interface.

Figure 8 shows the cavity length dependence of the inverse of the external differential quantum efficiency η_d (both facets) of lasers with the stripe width of 5.6 μm. The internal quantum efficiency η_i and the waveguide loss α_{WG} were estimated from extrapolated value at L = 0 and the slope and listed in Table. 2. It is noteworthy that η_d = 63 % and η_i = 81 % were obtained for L = 500 μm. These values show improvement of characteristics by

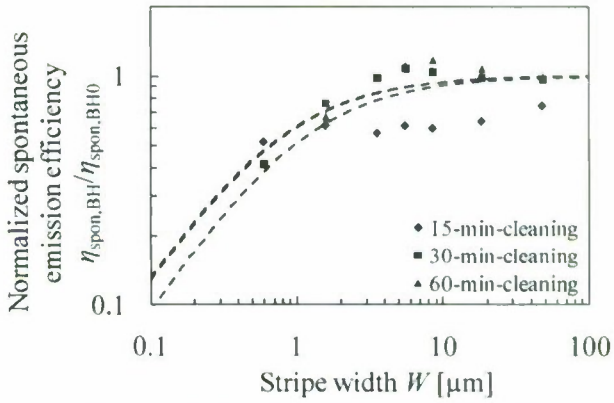

Fig.6 Stripe width dependence of the normalized spontaneous emission efficiency.

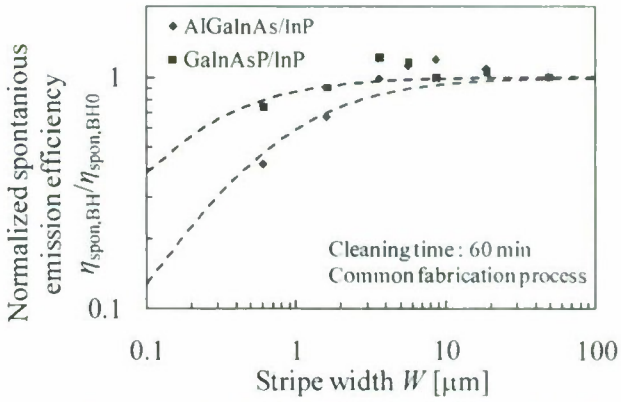

Fig.7 Comparison of S·τ products for AlGaInAs with GaInAsP

increase of thermal cleaning time and this result agrees with the results used for evaluation of $S\cdot\tau$ products mentioned above.

These results indicate that the thermal cleaning is effective for reduction of the sidewall recombination velocity for the embedding growth of AlGaInAs/InP BH lasers. Furthermore, quantitative studies of regrowth interface quality by $S\cdot\tau$ products are effective for not only GaInAsP/InP alloy system, but also AlGaInAs/InP alloy system. But there is still a room for further improvement and S·τ product should be further reduced.

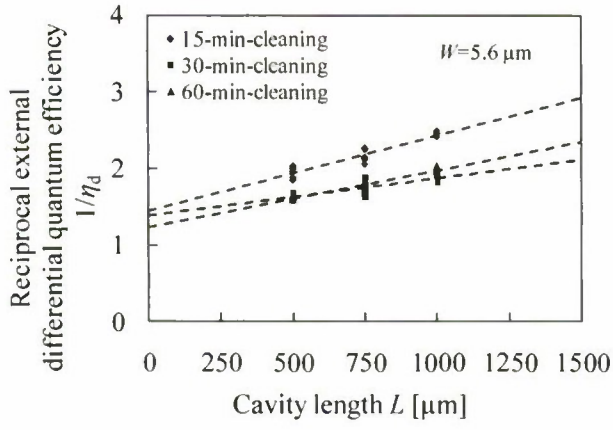

Fig.8 External quantum efficiency as function of cavity length.

Table 2. Internal quantum efficiency and waveguide loss.(W = 5.6μm)

Cleaning time [min.]	η_i [%]	α_{WG} [cm^{-1}]
15	69	8
30	72	4
60	81	7

IV. Conclusion

AlGaInAs/InP BH lasers with moderately high differential quantum efficiency were obtained by a combination of wet cleaning and thermal cleaning under PH_3 ambient gas prior to the embedding growth in OMVPE. The quantitative study of regrowth interface revealed proper thermal cleaning is notably effective and internal quantum efficiency as high as η_i = 81 % and the waveguide loss α_{WG} = 7 cm^{-1} were achieved.

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Investigation of Bonding Strength and Photoluminescence Properties of InP/Si Surface Activated Bonding

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Abstract

A low-temperature direct wafer bonding technique has been researched by using plasma treatment. Si-to-Si direct bonding strength was 1.6 MPa by using plasma pretreatment prior to the heating and weighting. 1.4 MPa of InP/Si bonding strength was obtained by improving chemical cleaning process. On the other hand, photoluminescence properties of GaInAs/InP quantum wells bonded on Si substrate were investigated. An introduction of a 30-nm-thick superlattice buffer on the top of the wafer greatly suppressed photoluminescence intensity degradation near the bonded interface.

Keywords: Surface Activated Bonding, Direct Bonding, Superlattice Buffer, InP on Silicon

I. Introduction

The speed of the large scale integration (LSI) is getting higher and higher by the miniaturization of device sizes. However, LSI technology will soon hit the interconnect bottleneck such as joule heating and signal delay due to the metal lines [1]. One way to solve the problems is replacing global metal lines with optical lines [2-4]. Optical circuit based on Si or silicon on insurator (SOI) is very attractive to be able to use the complementary metal oxide semiconductor (CMOS) process. The Si material is available for waveguide because it transmits near-infrared light wavelength such as 1.3-μm and 1.55-μm, and has the advantage of high index contrast between Si and oxide.

Recently, a lot of research activities related to optical devices on Si or SOI substrates have been reported [5-8]. However, a Si material has indirect bandgap property that is hard to contribute to the light emission and amplification. Previously, some silicon active devices were reported [9-11]. On the other hand, the lasers and the photodetectors made from InP based materials can realize high efficiency and low threshold oscillation. Conventional long wavelength lasers are manufactured on a InP substrate by using the organometalic vapor phase eptaxity (OMVPE) method. However, it is difficult to deposit long wavelength active layers such as GaInAsP quantum-wells to a Si or SOI substrate because of the difference of the lattice constants between Si and InP. Therefore, the hybrid integration of optical III-V compounds based devices on Si or SOI substrates became a very important technology. The surface activated bonding (SAB) technique [12] is expected to have advantages of low process temperature and high bonding strength than plasma assisted bonding [13, 14]. The integration of the LD chip on Si substrate was achieved by using Au-Au surface plasma-activated bonding, with no significant degradation of the optoelectronic characteristic after bonding [15].

However, for the optical coupling between the III-V laser and the Si optical circuit, a direct bonding of III-V compounds on Si and SOI is advantageous. By the direct bonding, hybrid silicon evanescent lasers were reported [16, 17]. In the future, an ultra low power consumption hybrid laser is requisite for optical interconnection on a Si-LSI. So-called membrane structures, which have higher optical confinement by high index contrast between polymer/SiO_2 and a thin III-V core layer, can realize such low power consumption lasers. Thus, the investigation of the influence of the SAB process is helpful to obtain the membrane InP on the Si optical circuit.

In this paper, we would like to report the bonding strength between InP and Si wafer by using the SAB technique and photoluminescence (PL) intensity degradations of GaInAs/InP quantum-wells. The PL intensity was greatly improved by inserting a thin (30-nm) GaInAsP superlattice at the interface.

II. Wafer Bonding

Figure 1 shows an outline of the SAB processes employed in our experiments. Si and InP substrate thicknesses were 700 μm and 350 μm, respectively, with the sizes of 2 x 2 cm^2. In order to reveal active surfaces, the surface of two wafers were exposed to plasma in high vacuum chamber. The species which can be used in our SAB machine are nitrogen, oxygen and argon. Plasma system we used in the equipment is conventional parallel plate type. Subsequently, two clean surfaces were bonded by heating and weighting at relatively low temperature (<150 °C) (Table.1). High precision to align is necessary between two wafers to manufacture a hybrid laser. The 1.6μm alignment accuracy of the Si/Si bonding could be obtained with this equipment.

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Fig. 1 Surface activated bonding processes.

Table I Bonding condition

Name	Value
Plasma irradiation process	
Plasma precursor	N_2,O_2,Ar
Plasma intensity	100 - 700 W
Pressure	1.2×10^{2} Pa
Weight and Heating process	
Bonding weight	50 - 1000 kgf
Heater temperature	R.T. - 500°C
Pressure	$<1.0\times10^{-5}$ Pa

At a first step, the plasma precursor dependence of bonding strength was investigated by Si/Si wafer bonding. The Si wafers ware cleaned by ultra sonic cleaning followed by organic solvent, H_2SO_4, BHF, and Standard Cleaning 1 (SC1) solution (NH_3:H_2O_2:H_2O=1:4:20 @ 70 °C). Figure 2 shows the Si/Si bonding dependence of the bonding strength by the plasma precursor and the plasma intensity measured by a tension tester (IMADA Co., Ltd., ZP-500N). The bonding condition is 1.25-MPa pressure (bonding strength and bonding weight were normalized by the contact area) at R.T. for 3 minutes and the plasma intensity is 200, 400 and 750 W, respectively. The reason why this experiment set at R.T. is to remove influence of the heating from energy to contribute to the bonding. The bonding strength was enhanced with increasing plasma intensity for nitrogen and oxygen gases. However, argon gas gave no adhesion for intensities above 400W. We believe this is because the surface roughness increases when argon plasma is irradiated to a wafer for long time [18]. On other hand, oxygen plasma causes bad influence to III-V layers and Si waveguides due to oxidation. Therefore, as for the plasma precursor dependence, nitrogen gas may be suited for surface activated bonding.

Figure 3 shows the bonding strength dependence on the bonding pressure. We adopted a plasma irradiation using nitrogen gas and the bonding was carried out by using the fixed conditions of the sample holder temperature of 150 °C and the bonding period of 2 hours in high vacuum. The bonding strength was enhanced with increasing bonding pressure for both Si/Si (solid line) and InP/Si (dashed line) bondings. In the case of the cleaning process without SC1 solution, the bonding strength higher than 1.0 MPa was obtained for Si/Si bonding, but not for InP/Si. Since this poor bonding property of InP/Si was considered to be attributed to residual particles on the InP wafer surface after a dicing process due to cleaning processes different from Si wafer. The InP wafer was cleaned by only organic solvent, H_2SO_4, and BHF. To avoid this problem, the

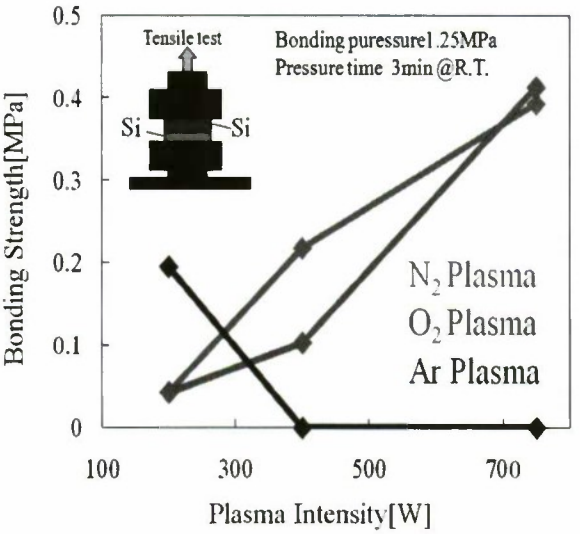


Fig. 2 Plasma precursor dependence.

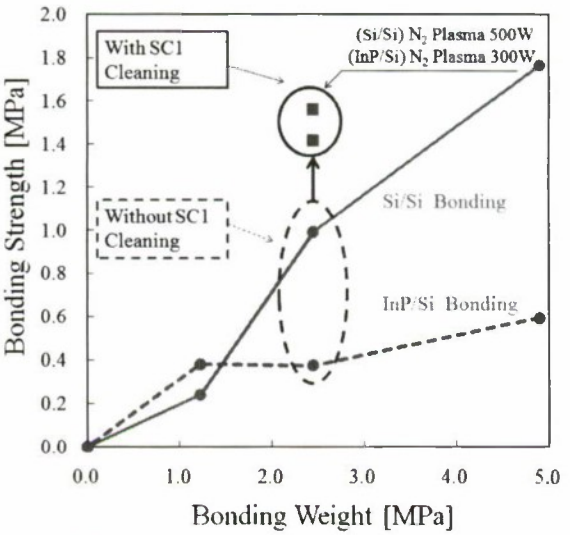


Fig. 3 Bonding strength characteristics.

Si and InP wafer surfaces were covered with SiO_2 (300 nm thick) deposited by plasma enhanced CVD before the dicing. .After removing this SiO_2 film with BHF, the same SC1 cleaning process was carried for both Si and InP wafers. This modification improved the InP/Si bonding strength to 1.4 MPa, which is similar to the bonding strength of Si/Si (1.6 MPa), as indicated by an arrow in Fig. 3. In addition, the Si/Si bonding strength was also increased from 1.0 MPa to 1.6 MPa at a 2.5-MPa bonding pressure point by SiO_2 cover for dicing. These results showed that the thermal expansion difference effect for bonding strength was suppressed in this process temperature.

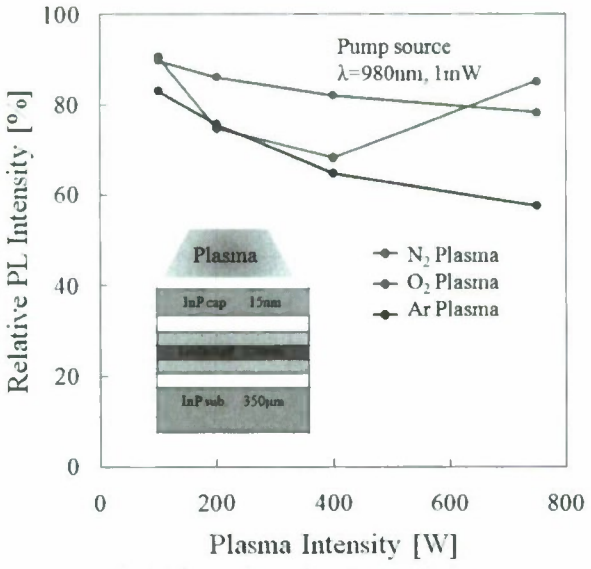
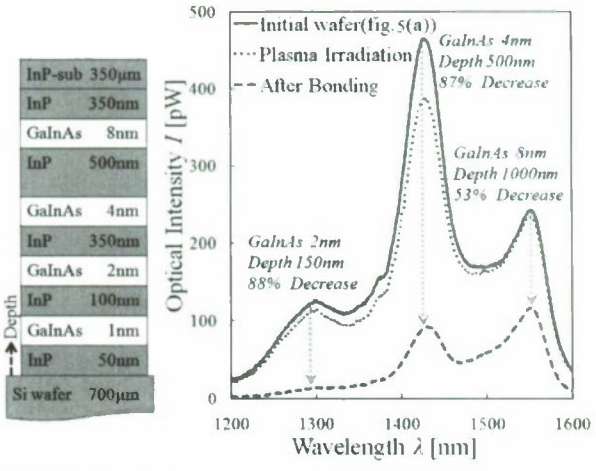


Fig. 4 Plasma intensity characteristics.

III. PHOTOLUMINESCENCE PROPERTY

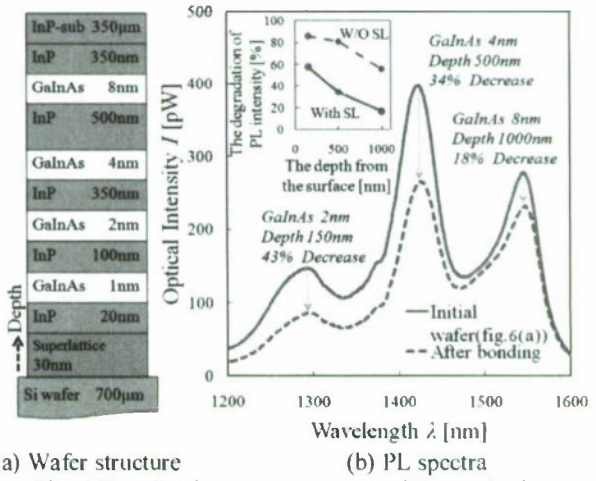
In this section, effects of the SAB processes to active layers were investigated by PL measurements. The plasma irradiation process is necessary to obtain high quality bonding as shown in Fig. 1. However, the optical characteristic of quantum wells might deteriorate by plasma irradiation similar to the reactive ion etching (RIE) process [19]. The inset of Fig. 4 shows wafer structure to check the plasma-irradiated effects, which consisted of a InP cap layer and a single GaInAsP quantum well layer whose the emission of light wavelength is 1.55 μm. The PL intensity was measured by using 980-nm light source after plasma irradiation. The relative PL intensity was degraded with increasing of plasma intensity for oxygen and argon gases. On the other hand, the degradation of the relative PL intensity was small for 700W by using nitrogen gas. Dropping near 400W may be due to ion generation in the plasma.

Next, the depth dependence of PL intensity degradation was investigated. Figure 5 (a) shows an initial wafer structure including GaInAs quantum-wells and Fig. 5 (b) shows its PL spectra measured at R.T. (solid line), after the nitrogen plasma irradiation (dotted line) and after the SAB process with 2.5 MPa pressure (dashed line). The initial wafer consists of 4 GaInAs quantum-wells with the thickness of 1, 2, 4, and 8-nm located at 50, 150, 500, and 1000-nm from the bonded surface, respectively. As can be seen in Fig. 5 (b), emission peak wavelengths of 1300, 1425, and 1550-nm correspond to the quantum-well thicknesses of 2, 4, and 8 nm, respectively, while that for 1-nm thick quantum well was not observed in this spectral range at R.T. The degradation of PL intensity after the bonding process was much larger than that after the plasma irradiation, and the degradation was larger for the quantum-well close to the bonding interface. The amount of degradation for quantum-well thicknesses of 2, 4 and 8 nm were 88, 87 and 53-%, respectively. Since this fact was considered to be attributed to a propagation of crystal degradation at the bonding interface due to large difference between thermal expansion



(a) Wafer structure (b) PL spectra

Fig. 5 Photoluminescence property without superlattice.



(a) Wafer structure (b) PL spectra

Fig. 6 Photoluminescence property with superlattice.

coefficients of Si and InP. In order to reduce internal stress at the bonded interface, two pairs of lattice matched superlattices consisting of $Ga_{0.22}In_{0.78}As_{0.47}P_{0.53}$ (7.5-nm) and InP (7.5-nm) were inserted as shown in Fig. 6 (a) [20]. Figure 6 (b) shows its PL spectra of the initial wafer (solid line) and after the bonding process (dashed line). The degradation of PL intensity after the bonding was reduced to approximately 1/2 to 1/3 of that without the superlattices. The inset in Fig. 6 (b) indicates the degradation of PL intensity normalized by that of the initial wafer (with the superlattices (solid line) and without that (dashed line)) as a function of the depth of the quantum-well from the bonding interface. The degradation of PL intensity was held down to about 20% in the layer that is deeper than 500 nm. This improvement of the PL intensity was considered to be relaxed the internal stress between Si and InP wafers because of inserting superlattices in the bonding interface.

IV. Conclusion

A successful bonding of InP on Si by the surface activated bonding technique was demonstrated. The bonding strength of >1 MPa was realized. An introduction of thin superlattices was found to be very effective to eliminate nonradiative components generated from the bonding interface. This technology is promising for realizations of high performance photonic devices directly bonded on Si and SOI.

Acknowledgment

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SELECTIVE ETCHING AND POLYMER DEPOSITION ON InP SURFACE IN CH_4/H_2-RIE

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Abstract

We conducted a preliminary study of selective etching and polymer deposition for fabricating Bragg gratings with varied depths in InP by using reactive ion etching (RIE) with methane (CH_4). We obtained selectivity in a submicrometer-pitch grating: the InP was etched in the window of the grating in the region with a thick layer, while it was not etched and polymer was deposited in the region without the thick layer. We also found that the selectivity depends on the plasma pressure in RIE.

I. Introduction

In the fabrication of InP-based optical and optoelectronic devices, selective etching, which can etch to varied depths with just one process, is promising because it allows us to keep the etching process simple and reproducible for enhancing the device characteristics. One of the effective applications of selective etching in the device fabrication process is to form Bragg gratings with varied depths (appodized gratings), because the depth variation, that is, the variation in the coupling-coefficient, can suppress sidelobes in the grating response [1]. Selective area etching by gas in a metal organic vapor phase epitaxy (MOVPE) reactor has been reported [2, 3], but not for submicrometer structures. On the other hand, reactive ion etching (RIE), one of the plasma etching techniques, has been used in the fabrication of InP-based optical and optoelectronic devices owing to its ability to accurately form structures with sidewalls perpendicular to the surface plane. RIE based on hydrocarbon gases, such as methane and ethane, has attracted much attention because it can provide smooth surface morphology and good anisotropy [4-9], and it has been applied to the device fabrication process [10-13].

In a previous work, we showed that the InP window is selectively etched in a patterned surface (surface with a SiO_2-patterned mask) by RIE with a mixture of methane and hydrogen, but that it is not etched and polymer is deposited on the InP surface in an unpatterned surface (surface without a SiO_2-patterned mask) [14]. The mechanism of the selective etching and polymer deposition can be explained by the loading effect for hydrogen plasma as follows [14]. In the plasma of methane and hydrogen, the primary reactants responsible for In volatilization are organic plasma, such as methyl, whereas the reactants for P are hydrogen plasma [6]. Here, plasma means plasma-excited atoms including ions and radicals. When the hydrogen plasma concentration is low, polymer is deposited on the unpatterned surface [Fig. 1(a)]. For the patterned surface, the methane and hydrogen plasmas can not react with the SiO_2 on the mask [upper diagram in Fig. 1(b)]. The organic plasmas therefore react only with each other to deposit a polymer film, and hydrogen plasma, which is not consumed as much on the mask, diffuses from the mask to the InP window [middle diagram in Fig. 1(b)]. Then, the InP surface is loaded with hydrogen plasma to a concentration sufficient for etching the InP and the InP is etched [bottom diagram in Fig. 1(b)].

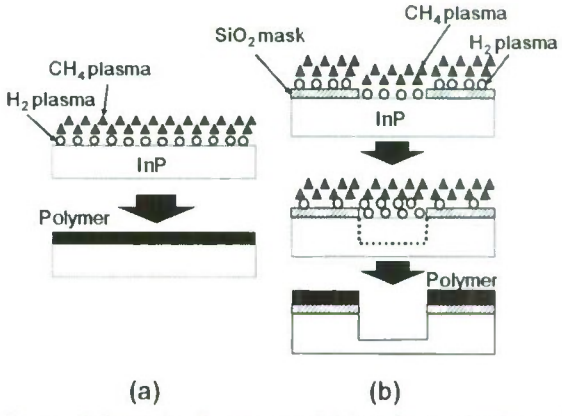

Fig. 1. Schematic diagrams explaining the mechanisms of selective etching and polymer deposition for the (a) unpatterned and (b) patterned surfaces (Ref. 14)

In this work, we study the application of the selective etching and polymer deposition to the fabrication of submicrometer pitch gratings and examine the dependence of the selectivity, i. e., selective etching or polymer deposition, on the plasma condition in the RIE.

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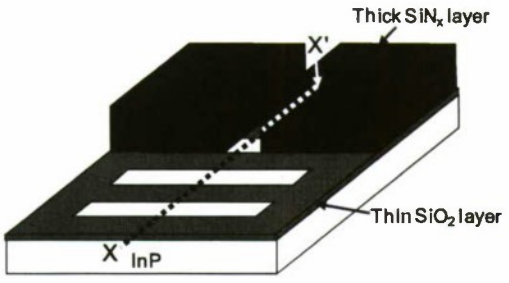

Fig. 2. Schematic diagram of the sample structure with a mask consisting of a thick SiN_X layer (1-μm thick) with a 1.5-μm-wide stripe space on a thin SiO_2 layer (30-nm thick) with about a 0.2-μm-pitch grating.

II. Experimental

We prepared samples with patterned mask as shown in Fig. 2. The mask structure consists of a thick SiN_X layer (1-μm-thick) with a 1.5-μm-wide stripe space on a thin SiO_2 layer (30-nm-thick) with about a 0.2-μm-pitch grating. In the mask structure, the thin region allows us to easily fabricate a submicrometer-pitch grating because the aspect ratio (mask thickness/grating pitch) of the mask is low, and the thick layer supplies the hydrogen plasma to the InP window of the grating, which contributes to the etching of the InP. The details are described in the next section.

The mask structure was fabricated as follows. First, 30-nm-thick SiO_2 film was deposited by plasma-enhanced chemical vapor deposition (CVD) as the thin layer. The SiO_2 layer was also patterned into the grating with the line/space of 0.11 μm/0.11 μm by electron-beam lithography. Next, the 1-μm-thick SiN_x layer was deposited by plasma-enhanced CVD on the patterned SiO_2 layer. A resist pattern with 1.5-μm-wide stripe spaces was formed on the SiN_X layer by conventional photolithography. Then, the SiN_X layers were etched by RIE with C_2F_6 using the resist as masks to the vicinity of the interface between the SiN_X and SiO_2. The RIE was performed at a C_2F_6 flow rate of 40 sccm, a plasma power of 50 W, and pressure of 2.0 Pa. SiN_X was further etched by RIE at a SF_6 flow rate of 30 sccm, plasma power of 50 W, and pressure of 20 Pa. Under this plasma condition, SiN_X is selectively etched and the SiO_2 is little etched. Finally, the resist was removed by oxygen plasma exposure.

The samples were exposed to a plasma of methane (CH_4), and etched at a plasma power of 100 W and pressure of 10 Pa for 1 min. During the etching, the flow rate of methane was kept constant at 40 sccm.

III. Results and Discussion

A. Selective etching and polymer deposition in submicrometer structure

Figure 3 shows SEM cross-sectional images of the grating in the regions with and without the thick layers. Polymer was

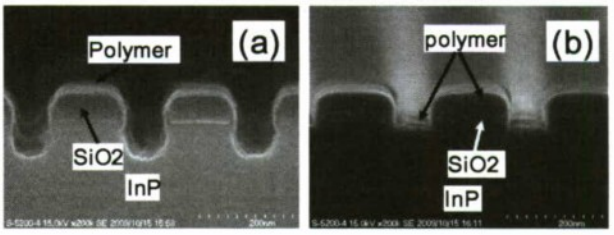

Fig. 3. SEM cross-sectional images of the etched gratings in the regions (a) with and (b) without the thick layers.

deposited on the InP surface in the window of the grating in the region without the thick layer to a thickness of 20 nm, and the InP was not etched. On the other hand, the InP was etched to a depth of 90 nm in the window of the grating in the region with the thick layer. Thus, for the submicrometer pitch grating, selective etching and polymer deposition was obtained by using the mask structure. Here, polymer was deposited to about 30 nm on the masks (thin layers) of the grating in the regions both with and without the thick layer.

The mask-thickness dependence of selective etching and polymer deposition, in addition to the loading effect for hydrogen plasma, can explain the selectivity. The selective etching is obtained with the thick layer but not with the thin layer [15]. This is because the thick layer can supply enough hydrogen plasma to etch InP while the thin layer cannot. In the mask structure, the hydrogen plasma decomposed from methane is not consumed as much on the mask (thick or thin layer), and it diffuses from the mask to the InP window. In the region with the thick layer, the thick SiNx layer supplies enough hydrogen plasma to etch the InP. The hydrogen plasma diffuses from the layer to the window of the grating in the stripe space. Therefore, the InP window surface is loaded with hydrogen plasma to a concentration sufficient for etching the InP and the InP is etched. On the other hand, in the region without the thick layer, the thin SiO_2 layer (mask) cannot supply enough hydrogen plasma to etch the InP. Therefore, polymer is deposited on the InP window surface of the grating. Thus, the selectivity is obtained due to the hydrogen plasma supply from the thick layer to the window of the grating in the direction across the grating (Y-direction).

B. Process for fabrication of appodized gratings

Utilizing the above-mentioned selective etching and polymer deposition, we propose an idea for fabricating gratings with varied depths, such as the appodized gratings. If we can vary the widths of selectively etched windows by varying the plasma conditions in RIE, we can vary the etching depths of the windows of the grating as follows.

First, a sample is prepared with a mask with different grating pattern widths [Fig. 4(a)]. Then, a first RIE is performed [Fig. 4(b)]. After the first RIE, the narrowest InP windows (W1) are etched, while polymer is deposited in the second narrowest windows (W2) and unmasked region [Fig. 4(c)]. Next, the sample is exposed to oxygen plasma to

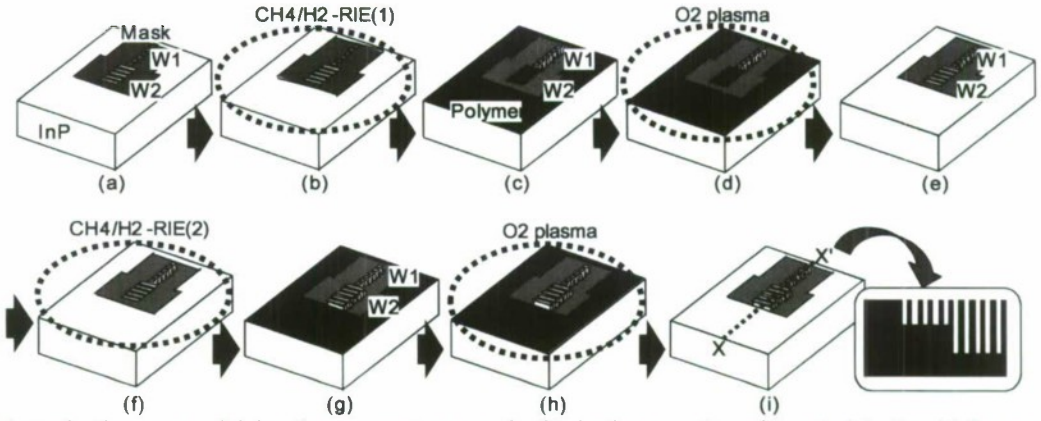

Fig. 4. Schematic diagrams explaining the proposed process for fabricating a grating with varied depths. (a) Prepared sample, (b) first RIE, (c) after first RIE, (d) oxygen plasma exposure, (e) after oxygen plasma exposure, (f) second RIE, (g) after second RIE, (h) oxygen plasma exposure, (i) after oxygen plasma exposure. A schematic cross-sectional diagram of the grating with varied depths is also shown.

remove the polymer [Fig. 4(d) and (e)]. Then, a second RIE is performed [Fig. 4(f)]. After the second RIE, the narrowest (W1) and the second narrowest InP windows (W2) are etched, while polymer is deposited in the unmasked region [Fig. 4(g)]. Here, the narrowest window (W1) is etched by both the first and the second RIEs, while the second narrowest window (W2) is etched by only the second RIE. This can bring the narrowest window (W1) deeper than the second narrowest window (W2). Finally, the sample is exposed to oxygen plasma to remove the polymer [Fig. 4(h) and (i)]. By repeating the above process steps (f) through (i), a grating with varied depths can be fabricated.

Thus, to fabricate the grating with varied depths, it is necessary to vary the width of the etched region in the window of the grating by varying the plasma conditions in the RIE. Therefore, we conducted a preliminary study of the dependence of selective etching and polymer deposition on the plasma condition in RIE.

C. Plasma-pressure dependence of selective etching

We examined the plasma-pressure dependence of the selectivity. Figure 5 shows SEM cross-sectional images of the InP surface in the gratings with and without the thick layer after RIE at 5, 10, and 20 Pa. At 5 Pa, selectivity was not obtained; the InP window surfaces with and without the thick layer were etched to a depth of about 90 nm. At 10 Pa, selectivity was obtained, the same as shown in Fig. 3. When the pressure was increased to 20 Pa, both surfaces were not

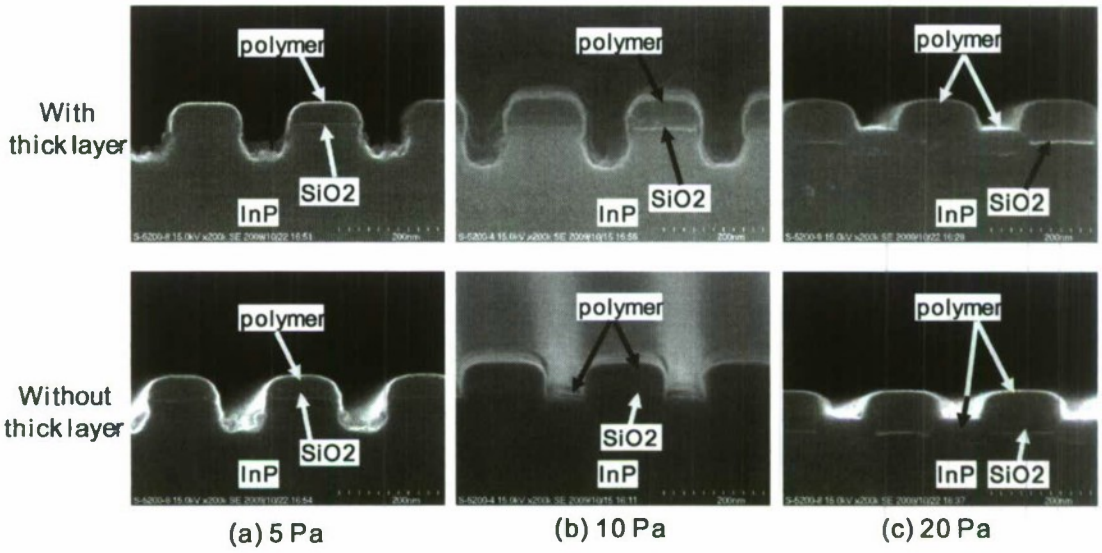

Fig. 5. Cross-sectional SEM images of the gratings etched at pressures of (a) 5 , (b) 10, and (c) 15 Pa. The upper and lower views were obtained for gratings in the regions with and without the thick layers, respectively.

etched and polymer was deposited. Thus, we found that the InP tends to be etched at low pressures, while polymer tends to be deposited on the InP in the window of the grating at high pressures. This might be because the pressure variation affects the hydrogen plasma diffusion or the self-bias voltage. We think that the hydrogen plasma reaches the center of the window in the Y direction and contributes to the etching of the InP window because of the increased diffusion length of the hydrogen plasma at low pressures, but that it does not contribute to the etching because of the shorter diffusion length at high pressures. We also think that the hydrogen plasma is accelerated because of the high self-bias voltage and contributes to the etching at low pressures, but that it is less accelerated because of the low self-bias voltage and contributes less to the etching at high pressures.

IV. Conclusion

We conducted a preliminary study of selective etching and polymer deposition of InP in submicrometer-pitch gratings by CH_4-RIE. Using a mask structure consisting of a thin layer and a thick layer, we obtained the selectivity at a CH_4 flow rate of 40 sccm, a pressure of 10 Pa, and a power of 100 W. The InP was etched in the window of the grating in the region with the thick layer, while it was not etched and polymer was deposited in the region without the thick layer. Furthermore, we found that the selectivity depends on the pressure in RIE. At high pressures, selectivity was not obtained and there was enhanced polymer deposition on the InP. At low pressures, it was not obtained and the etching of the InP was enhanced.

Acknowledgments

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Characterization on the 1064 nm InGaAs/GaAs Quantum-Well Laser Diode with Thermal Vias

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Abstract—We made the characterization on the 1064 nm quantum-well laser diode with thermal vias, which can be used for green-light generation combined with sceond-harmonie generation crystal. Due to the simplicity of the configuration and high reliability, large merits in terms of size, cost, and power consumption would arise. Furthermorc, direct modulation is possible in the laser diodes, which would lead to a highly compact pulsed laser sourcc with good heat dissipation.

Keywords-InGaAs/GaAs; laser diodes; MOCVD; quantum-well lasers; thermal vias

I. Introduction

In this paper, the InGaAs/GaAs quantum-well as well as the AlGaAs/GaAs and the GaAsP/GaAs super-lattice material systems have been used to develop 1064 nm quantum-well laser diodes, including epitaxial growth and device fabrication technologies. The semiconductor-type seed laser can be used in the pulsed optical-fiber system. Extensive research efforts [1-6] have been made to generate blue and green light directly from semiconductor laser diodes because of their various advantages such as low noise, high-frequency modulation capability, wavelength tunability, compactness, and easy integration. Because the low-cost GaAs substrate was adopted, it is expected that the manufacturing expense of the optical communication network will be reduced as well as the lasing performance will be excellent, and it is very helpful for the future global optical-fiber platform implementation.

II. Experimental

The 1064 multi-quantum-well and super-lattice laser diodes were grown by the low-pressure MOCVD system [7], and TBAs was used as the source of As. In this work, we adjusted flow-rate ratios and the growth timc of quantum wells to achieve the composition and the thickness needed for emitting the 1064 nm lasers. To optimize the growth conditions, different V/III flow-rate ratios, including 5.2, 10.3, and 20.6, were used, and different epi-layer growth rate, including 0.93, 1.03, and 1.13 Å/s, were tested. Through a series of experiments on the parameter of InGaAs/GaAs structures, we found that the growth temperature around 510°C and the V/III ratio about 10 resulted in better epi-layer quality.

III. Results

Expanding previous work on InGaAs/GaAs quantum wells [8], we fabricated samples 994, 995, and 996 to examine the composition and thickness of the structure. HR XRD rocking curves and PL diagrams for these samples are as shown in Figs. 1 and 2, respectively. By using the curve-fitting method, the Indium composition and its thickness can be obtained.

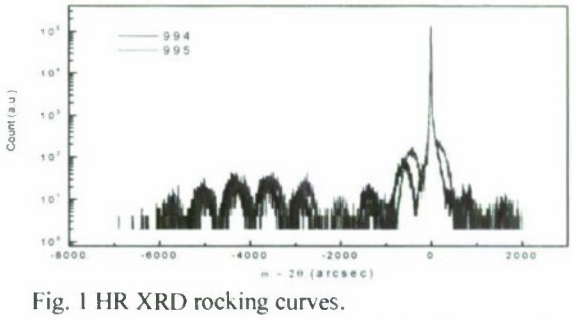

Fig. 1 HR XRD rocking curves.

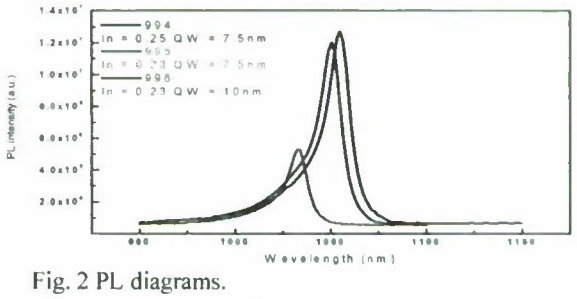

Fig. 2 PL diagrams.

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In order to produce high-power lasers, we engaged in the fabrieation process of wide-area semiconductor-type lasers, which can lead to higher output power. A variety of quantum-well and super-lattiee structure wcre grown for this study. The demonstrated room-temperature L-I curves, and lasing speetra for different samples L1 to L6 are shown in Figs. 3 ~ 6, respectively. All of the laser diodes were measured in the pulsed mode, and the pulse time was 0.5 μs/20 μs. From the lasing speetra, we observed that the lasing wavelength was less than1064 nm, which might be eaused by less Indium contents or thin quantum-well thieknesses.

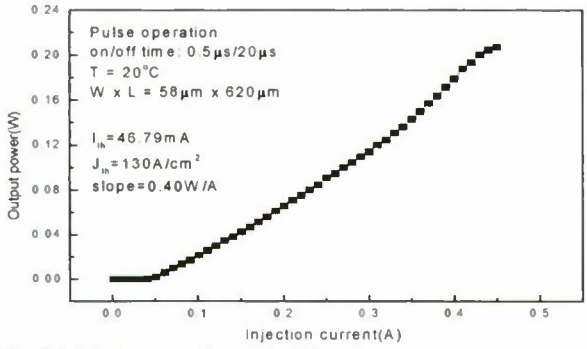

Fig. 3 (a) L-I eurve of sample L1.

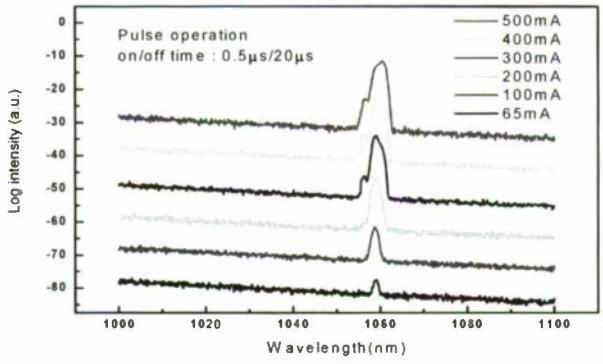

Fig. 3 (b) Lasing spectra of sample L1.

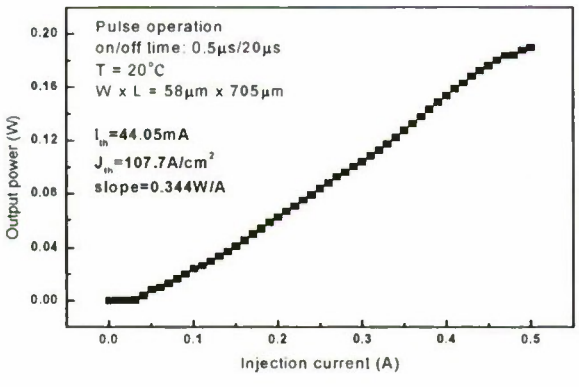

Fig. 4 (a) L-I eurve of sample L2.

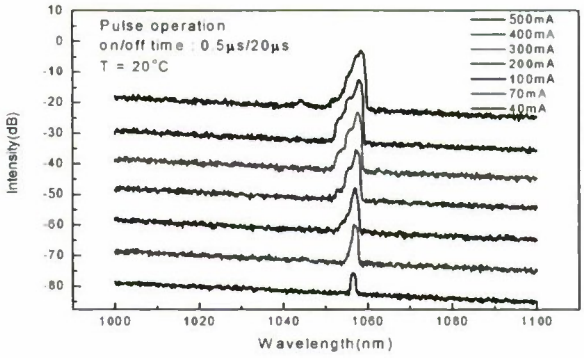

Fig. 4 (b) Lasing spectra of sample L2.

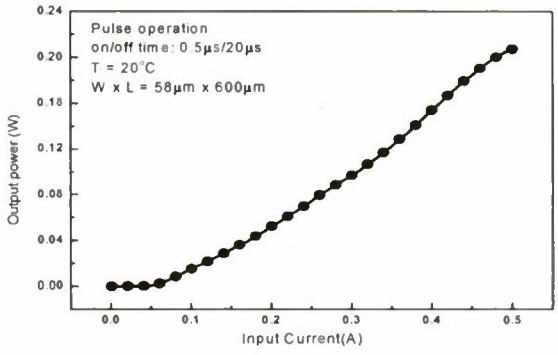

Fig. 5 (a) L-I curve of sample L3.

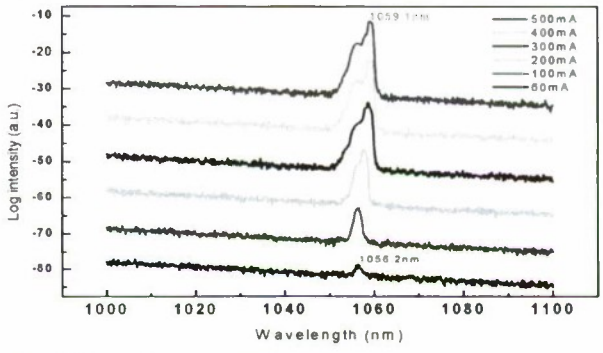

Fig. 5 (b) Lasing spectra of sample L3.

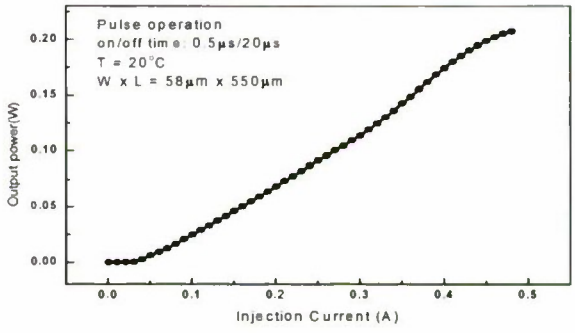

Fig. 6 (a) L-I curve of sample L4.

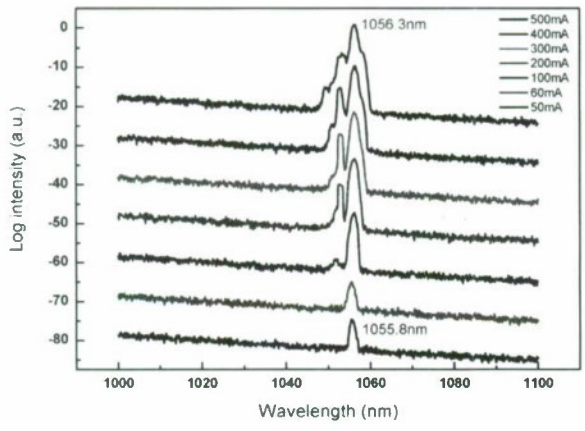

Fig. 6 (c) Lasing spectra of L4.

Under high-power operations, a number of carriers injected into the active region, and the band-filling effect resulted in the carrier distribution to high-energy levels, so that carriers could easily jump off quantum wells. Using super-lattice structures as potential barriers, as illustrated in Fig. 7, we can additionally support higher potential barriers, and subsequently improve the carrier-confinement capability.

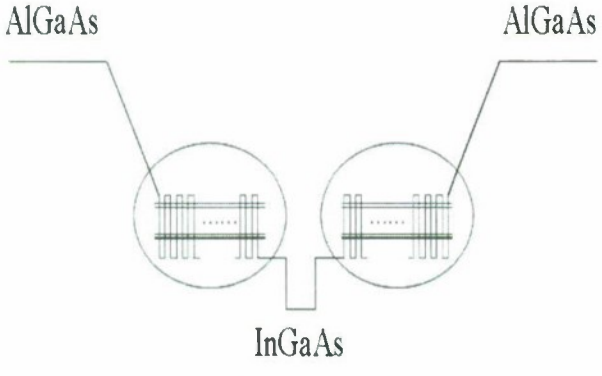

Fig. 7 A typical schematic diagram of the superlattice laser structure.

In general, AlGaAs, which is easily lattice matched to the GaAs substrate, and GaAsP, which induces tensile strain to the GaAs substrate, are used as super-lattice materials; however, the InGaAs quantum-well induces compressive strain to the GaAs substrate, so that the use of GaAsP as the super-lattice material could lead to strain-compensation effects. Therefore, the AlGaAs/GaAs and the GaAsP/GaAs material systems were utilized to grow super-lattice structures. The demonstrated results for the AlGaAs/GaAs (sample L5) and the GaAsP/GaAs (sample L6) super-lattices are shown in Figs. 8 and 9, respectively.

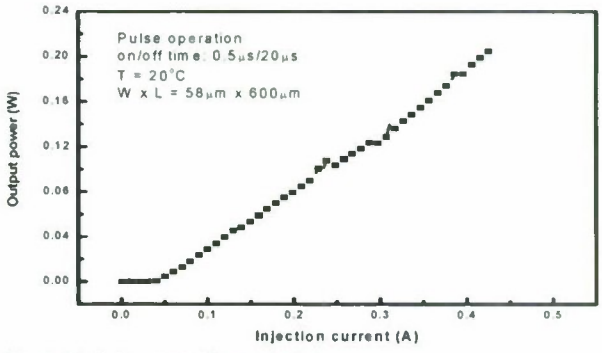

Fig. 8 (a) L-I curve of sample L5.

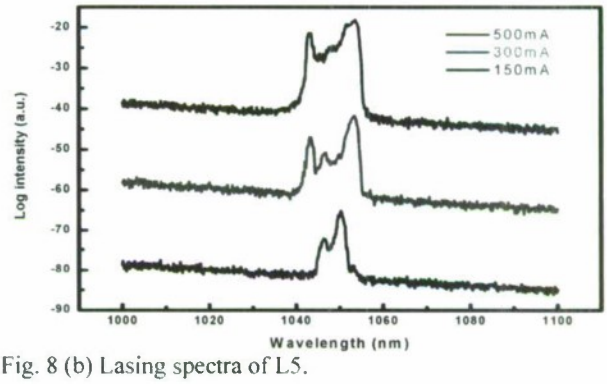

Fig. 8 (b) Lasing spectra of L5.

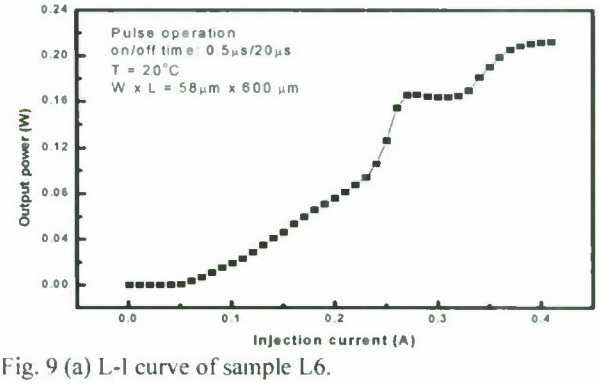

Fig. 9 (a) L-I curve of sample L6.

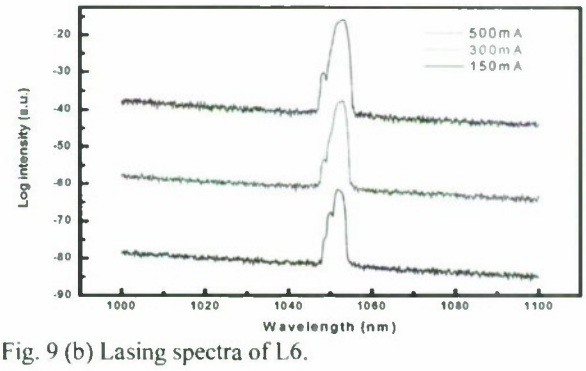

Fig. 9 (b) Lasing spectra of L6.

A detailed comparison among the characteristics of samples L1 to L6 is clearly articulated in Table 1. For sample L1 and sample L2, no obvious difference was observed and as expected that the increase in the thickness of isolation layer effectively reduced the accumulation of strains, and consequently improved the epi-layer quality of sample L2. However, sample L3 with thick isolation layer exhibited different effects, which might attributed to the lower optical confinement efficiency, and hence the increase in the threshold current.

From the exploration of different cladding-layer compositions, we found that the 60 % Aluminum content of the AlGaAs greatly improved the lasing efficiency. As to sample L5, we noticed that better carrier confinement resulted in higher efficiency. In sample L6, we found that its emitting efficiency is higher than that of sample L5.

Table 1 Characteristics of sample L1 ~ L6

	QW period	I_{th} (mA)	Slope (W/A)	Wavelength @100mA (nm)	Pulse operation	Note
L1	2	47mA	0.40	1058.7	0.5μs/ 20μs	Barrier = 15nm
L2	1	44mA	0.34	1056.9	0.5μs/ 20μs	Al = 0.3
L3	2	67mA	0.41	1056.4	0.5μs/ 20μs	Barrier = 30nm
L4	1	44mA	0.44	1056.2	0.5μs/ 20μs	Al = 0.6
L5	1	44mA	0.51	1050.3	0.5μs/ 20μs	AlGaAs/GaAs Super-lattice Structure
L6	1	63mA	0.54	1052.0	0.5μs/ 20μs	GaAsP/GaAs Super-lattice Structure

IV. Conclusions

The InGaAs/GaAs multi-quantum-well as well as the AlGaAs/GaAs and the GaAsP/GaAs super-lattice laser diodes were successfully fabricated by low-pressure MOCVD system, and a number of novel structures, including the thermal vias, were explored in this systematic investigation. The strain-relief effect and the composition of cladding layers were analyzed. In comparison with a series of experiments, we concluded that better lasing efficiency and the minimum threshold current could be obtained from the sample made up of the AlGaAs/GaAs structure combined with the 60% Aluminum content of the AlGaAs cladding layer.

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NEW APPROACH BASED ON LINEAR SPECTROGRAM TO MEASURE OPTICAL DELAYS IN SEMICONDUCTOR OPTICAL AMPLIFIERS

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Abstract

We show for the first time the potential of the linear spectrogram method for the extraction of phase shifts induced by slow and fast light in an InGaAsP/InP semiconductor optical amplifier. Optical filtering using this technique exhibits a 6-fold improvement of the optical delay at 10 GHz and an enhanced slow-light related effect bandwidth.

I. Introduction: group velocity control in semiconductor optical amplifiers

Controllable optical delays based on group index modification in guided wave devices have recently received much attention [1, 2, 3]. Indeed, slow and fast light are attractive for many applications such as optical buffers for telecommunication [1, 4, 5], control of optically carried microwave signals. Slow light schemes are based on the modification of the waveguide and/or material dispersion [1]. The former method can be implemented using periodic structures like two dimensional photonic crystals or Fabry-Perot resonators. Material dispersion can be changed using various methods such as the electromagnetic induced transparency, non linear effects in optical fibers like stimulated Brillouin scattering, or by changing the gain or the absorption spectrum of semiconductor devices via wave mixing [1, 3].

Although the maximum achievable delays via wave mixing are modest for optical buffer applications [6,1], these compact delay lines exhibit a great potential for microwave photonics applications where signal processing of radio-frequency signals is performed in the optical domains. Slow and fast light have indeed been used for phased array antennas [7], where the direction of a beam can be steered [8] without introducing beam distortion and without resorting to mechanical means that limit the speed of the system; tuneable microwave notch filter at 20 GHz for broad band access networks [9]; and optoelectronic processing functions for defense applications [10, 11].

Control of the group-velocity in guided wave devices is achieved by exploiting wave mixing in semiconductor optical amplifiers, i.e. coherent population oscillation (CPO) [12]. CPO and FWM arises from the beating of a intense pump with a weak probe beam (or with a modulation sideband) within the semiconductor nonlinear material that generates a carrier density pulsation [12, 1], which in turn modifies the refractive index seen by the optical beam. Population pulsation is also responsible for four wave mixing: the temporal index variation generates two conjugate wave and a four wave mixing signals [12,13], i.e. FWM signal 1 and FWM signal 2 [12,13]. The interaction modifies the non linear susceptibility of the material thereby altering the dispersion relationship experienced by the light [1].

Modification of the material dispersion is of paramount importance since strong carrier confinement in low dimensional material systems can allow the achievement of compact optical delay lines at room temperature.

It has been shown that it is possible to modify the group velocity in quantum well (QW) semiconductor optical amplifiers [14, 15, 16, 17]. FWM and CPO were successfully used in 1.3 µm quantum well (QW) semiconductor optical amplifiers [14], yielding optical variable delays up to 160 ps at a 1 GHz bandwidth. To evaluate the potential of a slow light approach, it is customary to use the time delay-bandwidth (DBP) product as a figure of merit [5,1,18]. The results published in [14] leads to a delay-bandwidth product DBP of 160 ps·GHz. Besides, slow light was also demonstrated in QW based electro-absorbers [19] where a change in the absorption spectrum is responsible for group velocity change. Moreover, investigation of monolithic integration of QW based semiconductor optical amplifiers (SOAs) and electro-absorption modulators allowed to demonstrate the feasibility of achieving large true-time delay of ~ 61 ps at 5 GHz bandwidth [20], thus leading to a DBP of about 300 ps·GHz.

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The methods traditionally used to measure a phase shift in SOAs are either based on the so-called "phase shift experiment" that resorts to a network analyzer, or to a high speed photodiode coupled with an oscilloscope [7, 21, 22]. Recently, slow light in a bulk SOA was enhanced by means of optical filtering of red-shifted sideband before detection using fiber Bragg grating based notch filter [23]. Optical filtering using this method has proven successful to enhance both the optical delay as well as the slow light bandwidth. Phase shift as high as ~ 150° at 19 GHz have been obtained, resulting in an optical delay of 22 ps, which implies a DBP of 418 ps•GHz.

In this paper, we introduce a new method based on linear spectrogram method that permits to measure optical delays created by group index modification in SOAs. This new technique allows to extract both the amplitude and the phase of the complex electric field at the output of an SOA. A phase shift of 135° is obtained at 10 GHz for a bulk InGaAsP/InP SOA, in agreement with results published in reference [23].

II. Linear and non linear optical properties of bulk semiconductor optical amplifier

The SCH structure is grown by gas source molecular beam epitaxy on a (100) InP n+-oriented substrate and consists of a 0.2 μm thick tensile-strained-bulk active layer embedded between two 0.1 μm thick quaternary layers (λ_c= 1.18 μm) [24]. The active layer was processed into buried ridge stripe (BRS) single mode waveguides. The waveguide tilted with a 7° angle and facets were AR coated leading to a residual reflectivity of about 10^{-4}. Input and output tapers ensure reduced coupling losses between the waveguide and specific lensed fibers. The length of the device is 1 mm [24].

Description of the experimental set-up used to determine the gain and four wave mixing efficiency can be found in reference [22]. The current is adjusted to obtain the maximum gain. The unsaturated fiber to fiber gain is 29 dB for a bias current of 250 mA (J ~ 20 kA/cm2). The FWM efficiency theoretically determines the efficiency of slow light in a SOA. We therefore measured the conversion efficiency of the conjugate FWM. The bias currents are adjusted so as to obtain the maximum gain, which is actually at 1540 nm. The input probe power is fixed at – 16 dBm while the pump power is adjusted (between -20 dBm and 0 dBm) using a variable attenuator, the pump-probe detuning being about 100 GHz. The FWM efficiency varies with the total output power and exhibit a maximum corresponding approximately to the output saturation power. For a negative detuning Δf, the decrease of FWM efficiency follows a slope of – 13 dB/dec (Fig. 1). The decrease of FWM efficiency with the detuning is consistent with values published in previous works [25].

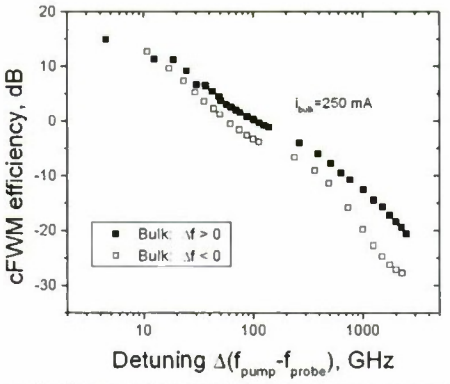

Fig. 1: FWM efficiency of the FWM signal I versus pump-probe detuning for optimum powers of P_{pump} ~ - 5 dBm et P_{probe} ~ -16 dBm.

III. New approach based on linear spectrogram to measure optical delays in semiconductor optical amplifiers

We mentioned in the introduction that optical filtering has been found to enhance both the maximum attainable phase shift as well as the bandwidth of slow light induced effects [23]. Following these results, we introduce here a new method based on linear spectrogram [26, 27, 28] that allows to measure the complex electric field, i.e. the phase as well as the amplitude, using a simple configuration that requires neither a high speed photodiode nor a network analyzer. This technique based on the linear spectrogram method use a time-dependent element to gate the input signal then spectrally resolve the input signal. This method builds a time-frequency distribution of the input signal from which the original complex electric field is obtained. The functional form of a spectrogram is given by:

$$S(\omega,\tau) = \int_{-\infty}^{+\infty} E(t)G(t-\tau)\exp(-i\omega t)dt \qquad (1)$$

E(t) is the complex electric field at the output of the SOA and $G(t-\tau)$ relates to the delayed gate function. This approach offers a direct mean to rapidly evaluate the potential, in terms of optical group delays, of various SOAs based on different type of active layers. The linear spectrogram method can also allow the extraction of the phase amplitude coupling factor of SOA [29] that remains a critical parameter in the slow and fast light effects [30]. The linear spectrogram method allows to select the best SOAs before the implementation of the experiment using a fiber Bragg grating as the optical filter.

The experimental set-up is illustrated on Fig. 2. An external tunable cavity laser plays the role of the pump at 1.55 μm. A $LiNbO_3$ based Mach-Zehnder modulator (MZM) is driven with a 10 GHz modulation frequency and generates two sidebands in the frequency domain that act as probe beams. The complex electric field *E(t)* at the output of the SOA is gated through a gate function $G(t-\tau)$, where τ is a

relative programmable delay. The gate function is determined by an electro-optic phase modulator that exhibits the advantage of a large operating wavelength range compared to an electroabsorption modulator [27, 28]. It also has a much simpler transfer function, i.e. a pure phase modulated signal, that allows for a faster convergence of the algorithm compared to an electro-optic Mach-Zehnder modulator that contains both amplitude and phase modulation [27, 28]. The variable attenuator allows to adjust the input optical power in the input fiber (fiber before the SOA) from – 30 dBm up to 0 dBm.

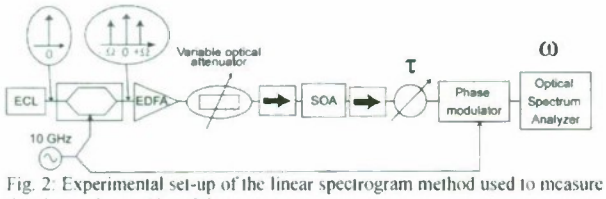

Fig. 2: Experimental set-up of the linear spectrogram method used to measure the phase advance/time delay.

Moreover, optical filtering is implemented through digital filter in the algorithm calculation which avoids the need of a very narrow band notch filter. The radio frequency source used to control the EOPM is the same as for the MZM.

The bulk SOA previously studied bias current is fixed at 200 mA to obtain a fiber to fiber peak gain of about 27 dB at 1.55 μm. When no optical filtering is used, the transmitted signal through the SOA experiences a negative delay, i.e. a phase advance which is representative of fast light (Fig. 3). Blocking of the red shifted sideband is found to enhance the optical delay by a factor of 6 in a bulk SOA compared to the unfiltered scheme when the input power increases from -30 dBm up to 0 dBm (Fig. 3), demonstrating phase delay of 135 ° at 10 GHz, close to the seven fold improvement measured in a bulk SOA using a network analyzer and a fiber Bragg grating [23].

This method exhibits the advantages of offering a powerful mean to investigate the potential of SOAs based on different type of active layers prior to the physical implementation of the optical filter.

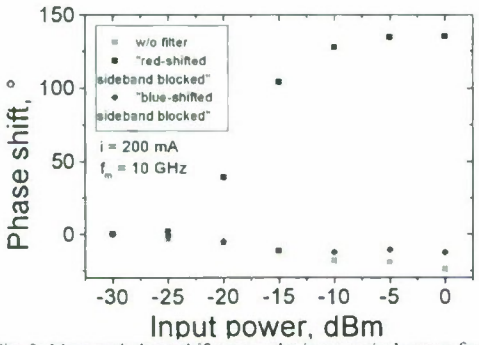

Fig. 3: Measured phase shift versus the input optical power for 10 GHz modulation frequency extracted from the linear spectrogram method.

IV. Conclusion

A new method based on linear spectrogram method allowed to measure the complex electrical field at the output of an SOA, i.e. both the phase and the amplitude. Optical filtering using signal processing in our method is found to enhance both the slow light related effect phase shift and the optical bandwidth, in agreement with experiments using fiber Bragg grating as an optical filter [23].

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Floating-base InGaP/GaAs Heterojunction Phototransistors with Low Doped Extrincsic Base

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Abstract

Floating-basc InGaP/GaAs heterojunction phototransistors (HPTs) with low doped extrinsic base region arc demonstrated. Electrieal and optieal characteristics of thc fabricated HPTs with and without SiN_x passivation are investigated. Moreover, the optieal gain of these HPTs is compared in terms of variation of the emitter size. The SiN_x passivated HPTs with 50×50 μm^2 of emitter size showed the superior high optical gain. The devices exhibited very high optieal gain of 159 at optical power of 100 nW under 635 nm illumination.

Keywords-InGaP/GaAs, phototransistors, SiN_x passivation, optical gain, emitter size effect.

I. INTRODUCTION

Very high optoelectronic conversion gain is required for the photodetectors (PDs) in the applications such as nano-bio sensor system, optical coherence tomography and quantum information processing systems because the PDs in these applications should be able to detect ultra-low optical power levels. Although the photodetectors such as PIN photodiodes (PIN-PDs) and Avalanche photodiodes (APDs) havc been commonly used for the photo-detection, PIN-PDs have no internal optical gain (G_{opt}) and APDs suffer from high operating voltage and excess noise from avalanche multiplication. Accordingly, heterojunction phototransistors (HPTs) with large G_{opt} under thc low bias voltage arc promising PDs in the above mentioned applications. InGaP/GaAs HPTs have been extensively studied as detectors for short wavelength applications.

There have been several works to enhance G_{opt} of InGaP/GaAs HPTs [1-4]. Three-terminal InGaP/GaAs HPTs (3T-HPTs) with the dc current source have been studied to obtain the higher G_{opt} [1-2]. However, these devices have physical structure which interferes with incident light and suffer from an additional fabrication process and power consumption. The recently reported InGaP/GaAs 2T-HPTs (emitter area: 75×60 μm^2, absorption area: 10.9×10^4 μm^2) with sulfur treatment demonstrated G_{opt} of 20.3 at optical power of 107.6 nW, V_{CE} = 1 V under 635 nm illumination [3], but the sulfur treatment as surface passivation technique does not become permanent [5]. We already reported the G_{opt} of the 2T-HPTs with extrinsic base region is high compared to that of the conventional 2T-HPTs with base contact metal [4]. In addition,

n^+-$In_{0.5}Ga_{0.5}As$	$>1\times10^{19}$	50 nm	Cap
n^+-$In_xGa_{1-x}As$ (x=0→0.5)	$>1\times10^{19}$	50 nm	Graded
n^+-GaAs	4×10^{18}	50 nm	Subemitter 2
n^+-$In_{0.5}Ga_{0.5}P$	2×10^{18}	50 nm	Subemitter 1
n-$In_{0.5}Ga_{0.5}P$	5×10^{17}	50 nm	Emitter
p^+-GaAs	4×10^{18}	80 nm	Base
n^--GaAs	1×10^{16}	800 nm	Collector
n^+-$In_{0.5}Ga_{0.5}P$	2×10^{18}	20 nm	Etch stop
n^+-GaAs	4×10^{18}	600 nm	Subcollector
N^+ GaAs substrate			

Figure 1. Device heterostructure of InGaP/GaAs HPTs

a fabrication of thc 2T-HPTs with extrinsic base region is simpler than that of the standard HPTs. Thc SiN_x passivated 2T-HPTs with low doped extrinsic base region (SP-HPTs) are suggested to improve their electrical and optical characteristics for this paper. During the diffusion process in the extrinsic base region, the collected holes can be annihilated by a recombination process at the SiN_x/GaAs or metal/GaAs interfaces. The surface recombination velocity at the SiN_x/GaAs interface of the base of HPT is lower than that at the metal/GaAs interface [6-7] Moreover, the low doped base region causes the reduction of the emitter-base built-in potential barrier and the longer minority lifetime in the base. Therefore, the G_{opt} can be enhanced because the lower base recombination current and built-in potential barrier facilitates the electron injection from the emitter to the collector.

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In this paper, SiNx passivated InGaP/GaAs 2T-HPTs with extrinsic base mesa fabricated and characterized. The electrical and optical characteristics of the fabricated SP-HPTs are compared with those of the non-passivated HPTs (NP-HPTs). The influence of emitter size of the HPTs on the G_{opt} is also investigated.

II. EXPERIMENT

The InGaP/GaAs HPT structure was grown by metal organic chemical vapor deposition (MOCVD) on an n^+-GaAs substrate oriented in the [100] direction, as shown in Figure 1. The epitaxial layer consists of a 600-nm-thick n^+-GaAs subcollector, a 20-nm-thick n^+-InGaP etch stop layer, a 800-nm-thick n^--GaAs collector, a 80-nm-thick p-GaAs base (C doped at 4×10^{18} cm^{-3}), a 50-nm-thick n-$In_{0.5}Ga_{0.5}P$ emitter, a 50-nm-thick n^+-InGaP subemitter 1, a 50-nm-thick n^+-GaAs subemitter 2, a 50-nm-thick n^+-$In_xGa_{1-x}As$ (x=0~0.5) graded layer and a 50-nm-thick n^+-$In_{0.5}Ga_{0.5}As$ cap layer from the bottom to the top. Multilayer Ni/Au/Ge/Ni/Au (20/100/50/30/200 nm) metal was deposited by electron beam evaporation method on the backside of substrate for the collector contact, which was followed by annealing process at 410°C for 40 sec in N_2 ambient. Ti/Pt/Au (20/30/200 nm) metallizations were evaporated for non-alloyed emitter. The emitter metal was used as an etching mask to form the emitter mesa by using selective wet etching method. The base and isolation mesa etching was performed down to the half of n-GaAs collector. A SiN_x film was deposited for the passivation and antireflection coating. The exposed extrinsic base layer of the fabricated HPTs was employed as the optical window. Their emitter sizes are 140×50, 110×50, 80×50 and 50×50 μm^2, respectively. Isolation mesa size is 166×171 μm^2. The peak wavelength of a single laser source for the optical illumination is 636.8 nm, which was measured by using and optical spectrum analyzer. The incident optical power was measured by using an HP 81530A optical power sensor. The spot size of the illuminated light through the lensed optical fiber is less than 50 μm. Dark current and photocurrent was measured using an HP 4155A semiconductor analyzer.

III. RESULT AND DISCUSSION

The collector dark currents (I_{Cdark}'s) of the fabricated SP-HPTs and NP-HPTs are presented in the Figure 2. The SP-HPTs and NP-HPTs with 50×50 μm^2 of emitter size exhibited I_{Cdark} of 110 and 290 fA at V_{CE} of 1 V, respectively. The I_{Cdark}'s of the SP-HPTs were lower than those of the NP-HPTs because of the reduced the surface conducting current along the exposed base region and sidewall of the mesa. Both SP-HPTs and NP-HPTs showed that the I_{Cdark} decrease as the emitter size decreases. This can be ascribed to the base leakage currents. The base leakage currents consist of bulk recombination current (I_{bulk}), space charge recombination current (I_{scr}), surface recombination current (I_{surf}), and contact recombination current (I_{cont}). The I_{bulk} and I_{scr} are proportional to the emitter area while the I_{surf} and I_{cont} are dependent on the device layout. Considering that the layout of the SP-HPTs and NP-HPTs, I_{cont} is imperceptible. The SiN_x passivation also results in the I_{surf}

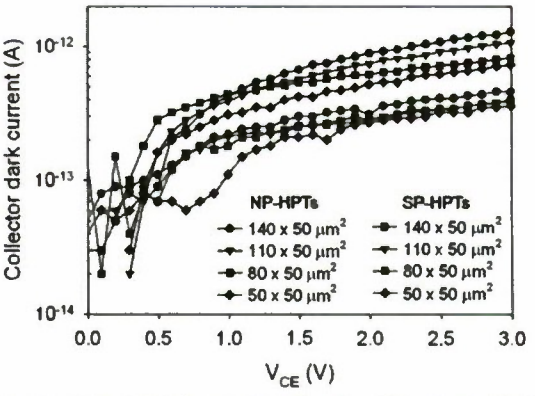
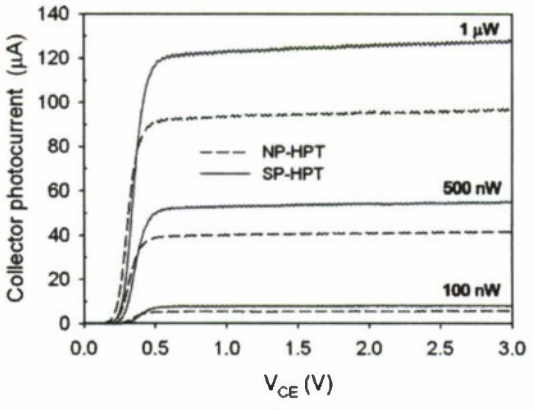
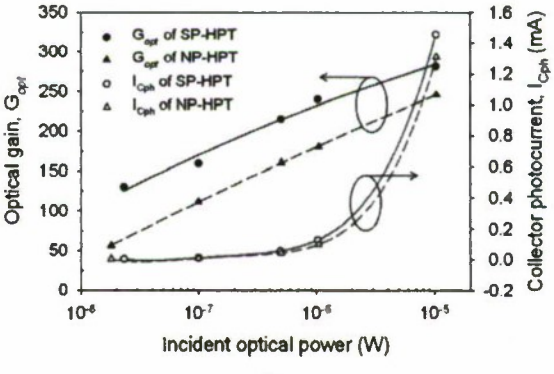


Figure 2. Collector dark current as a function of V_{CE} for the SP-HPTs and NP-HPTs with various emitter sizes.



(a)



(b)

Figure 3. (a) Common emitter characteristics and (b) optical gain and collector photocurrent at V_{CE} = 2 V as a function of incident optical power for the SP-HPTs and NP-HPTs having 50×50 μm^2 emitter size.

TABLE I. OPTICAL GAIN OF THE NP-HPT AND SP-HPT UNDER VRIOUS INCIDENT OPTICAL POWERS

P_{in}	10 μW	1 μW	500 nW	100 nW	20 nW
G_{opt} of NP-HPT	245.6	180.2	160.1	111.3	56.1
G_{opt} of SP-HPT	280.9	239.8	214.6	159.0	129.6

becoming insignificant in comparison to the I_{bulk} and I_{scr} [6]. The base region is low doped so that the minority carrier lifetime is quite long. The fabricated HBTs, which was fabricated using the same epitaxial structure as shown in Figure 1, exhibited the base current ideality factor of 1.77. Thus, the dominant component of the overall base current is the I_{scr}. As a result, one cause of the decrease in the I_{Cdark}'s of both devices may be the increase of the base recombination current with the emitter-base junction area due to the additional I_{scr}.

The optical characteristics of the SP-HPT and NP-HPT with floating base were measured under the illumination of 635 nm laser light with various optical powers. The electron-hole pairs are generated in the base and collector region when the light is incident on the base surface of a base-floated HPT. Not only did the deposited SiN_x film passivate the device surface, it functioned as an antireflection coating. The responsivity of the non-passivated and passivated HPTs-WB in p-i-n mode was 0.28 and 0.40 A/W, respectively. Therefore, the number of absorbed photons is greater in the SP-HPTs than in the NP-HPTs. The photo-generated holes in the collector are swept into the base due to the electric field established in the collector. These holes take a role as holes supplied from base electrode in HBTs. Thus, the photocurrent is amplified by dc current gain, resulting in the collector photocurrent (I_{Cph}). As the optical power increases, so does the photocurrent, as shown in Fig 3 (a). The optical gain, G_{opt}, was measured with respect to the variable incident optical power as shown in Figure 3 (b). The G_{opt} was defined to be $G_{opt} = h\nu\Delta I_c/qP_o$, where $h\nu$ is the energy of the incident photon and ΔI_c is the increment of the collector photocurrent due to the incident optical power, P_o. The obtained G_{opt} values of the SP-HPT (NP-HPT) at V_{CE} = 1 V are shown in Table I. The G_{opt} of the SP-HPT (NP-HPT) is 280.9 (245.6) and 129.6 (56.1) under the P_{in} of 10 μW and 20 nW, respectively. The SP-HPTs demonstrated much higher optical gain than NP-HPTs due to the difference of the generated photocurrent in the base and collector region. A further enhanced G_{opt} is expected in the 800–850-nm wavelength range due to the higher photocurrent at the same optical power levels [9].

The Figure 4 shows the dependence of the optical gain of the SP-HPTs on the emitter size and the illuminated optical power level. The measured G_{opt} values of all devices increase as the optical power increases. It was observed that the higher G_{opt} was measured for the devices with the smaller emitter size. A larger number of holes will be lost by recombination with larger emitter area because the base leakage current is dominated by the area dependent I_{scr}. Therefore, the density of accumulated holes at the base region contributing to G_{opt} will

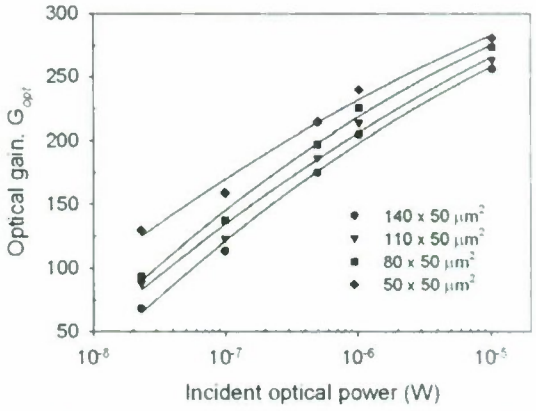


Figure 4. Optical gain as a function of incident optical power for the SP-HPTs with 50×50, 80×50, 110×50 and 140×50 μm² emitter sizes.

be reduced. Considering that higher G_{opt} was observed for the devices with smaller emitter area, further scaling in the emitter area may help to improve the G_{opt} of the devices.

IV. CONCLUSION

The SiN_x passivated floating-base InGaP/GaAs HPTs with low doped extrinsic base region were successfully fabricated and characterized. Both SP-HPT and NP-HPT showed very low I_{Cdark}. And it can be ascertained that the recombination currents in the base region are responsible for the I_{Cdark} of NP-HPT being larger than that of SP-HPT and for the G_{opt} of SP-HPT increasing with a decrease in the emitter size. The experimental results show that the fabricated SP-HPT is a promising two-terminal photodetector operating at short wavelengths (600–850-nm).

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OPTICAL CONTROL OF InP-BASED HEMT 60GHz OSCILLATORS WITH SUB-HARMONIC INJECTION LOCKING

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***Abstract*— Optical control and sub-harmonic-injection-locking of a 60GHz millimeter-wave oscillator using InP-based HEMTs are reported. The oscillation frequency locking by the injection of several order sub-harmonic signals was clearly observed. In addition, the modulation of the frequency-locked 60GHz signals by the illumination of a tightly focused laser beam with intensity modulation was also demonstrated. This oscillator can lead to a key device for the base station in millimeter-wave wireless systems with optical fiber links.**

Keywords: HEMT, opto-electronic mixing, sub-harmonic locking

I. INTRODUCTION

The High-Electron-Mobility Transistor (HEMT) is a promising device for converting high-speed lightwave signals to millimeter-wave signals due to its excellent millimeter-wave characteristics and light absorption characteristics. Many studies on interactions between lightwaves and micro-/millimeter-waves using HEMTs have been reported [1]-[6].

We have also studied optical responses of the InP-based HEMT and have reported its potential for applications to radio-on-fiber (ROF) systems [7], [8].

In this paper, the optical control of a 60GHz MMIC oscillator using an InP-based HEMT is reported.

II. OPTICAL RESPONSE OF HEMT

An InP-based InAlAs/InGaAs ultra-fast HEMT of f_t=170GHz and f_{max}=350GHz, developed at NTT photonics laboratories [9], was used in this study. Firstly, the basic optical response of the HEMT was measured in detail. The HEMT was fixed on a precisely-controllable X-Y mechanical stage and this was installed into a microscope. DC power supplies for Gate and Drain bias voltages and a microwave network analyzer/spectrum analyzer were connected to the HEMT by use of two precise microwave probes and bias-Tees. An optical beam from a 635nm FP laser was tightly focused with a spot size of ~10μm using a microscope. This was repeated using a 1550nm DFB laser. The spot position was observed by use of an IR camera and precisely controlled by use of the X-Y stage.

The increases in the small signal gain and the Gate capacitance in microwave and millimeter-wave ranges were observed by the illumination of the tightly focused CW laser beam when the beam spot was set to the position between the Drain and Source electrodes. However, the decrease in the gain was observed when the beam spot was set to the side-gating position [7], [8].

III. MMIC OSCILLATOR

Based on the basic measured optical response in the HEMT, we designed and fabricated an optically controllable millimeter-wave oscillator using the HEMT. Figure 1 shows an equivalent circuit for an optically controllable MMIC oscillator composed of two HEMTs; HEMT-1 is used as an active transistor with an appropriate DC Drain bias voltage for generating appropriate gain at the designed frequency range for MMW oscillation. HEMT-2 is used as an optically controlled variable capacitor with a negative Gate bias voltage. The bias and feedback circuits for HEMT-1 are composed of HEMT-2, Z_1, and Z_2. Detailed CPW parameters were determined using circuit design software.

The oscillation frequency can be controlled by the laser beam illumination to the Gate electrode of HEMT-2, since the increase in the Gate capacitance by the laser beam causes a change in the MMW oscillation frequency determined by $f_{osc} = 1/2\pi\sqrt{LC}$.

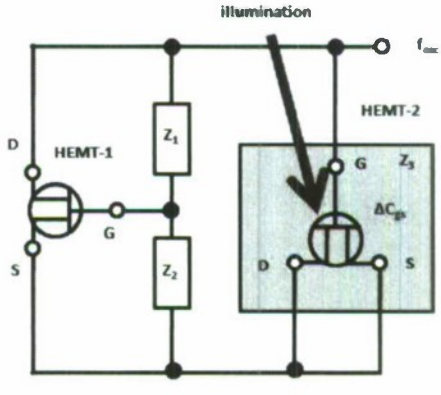

Figure 1. An equivalent circuit of a designed optically controlled 60GHz oscillator.

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Figure 2 shows examples of the measured 60GHz signal spectra from the fabricated MMIC oscillator with/without a local 30GHz signal for injection locking. By injecting the local microwave signals to the MMIC oscillator from the injection port, oscillation frequency locking to the integer multiple value of the local frequency was also clearly observed over a 10MHz locking frequency range. Figure 3 shows the measured output power lever versus the oscillation frequency under the injection locking. The injection locking by use of 10/12/15/20/30GHz signals were also observed clearly.

Finally, an amplitude modulated laser beam was also focused onto HEMT-2 under the frequency locking condition by the local signal injection. An example of the modulated 60GHz signal spectrum is shown in Fig. 4. The frequency-locked 60GHz signal was modulated by the illumination of a ~1MHz modulated laser beam. This characteristic is useful for converting optical ASK signals to MMW FSK signals.

IV. Conclusion

The optical control of the injection-locked 60GHz signal was demonstrated experimentally. It leads to a key-device for compact base-stations for down-links in millimeter-wave wireless systems with optical fiber links.

Acknowledgment

Authors would like to thank Prof. T. Nagatsuma and Dr. H. Shiomi for their valuable comments and discussions. This work was supported in part by the Grants-in-Aid for Scientific Research from the Ministry of Education, Science, Sports and Culture, Japan.

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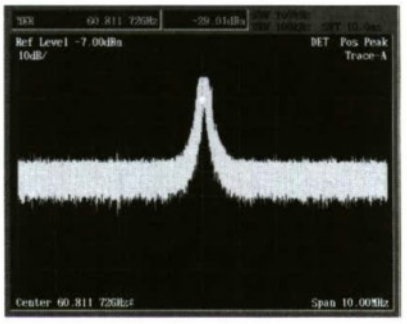
(a)



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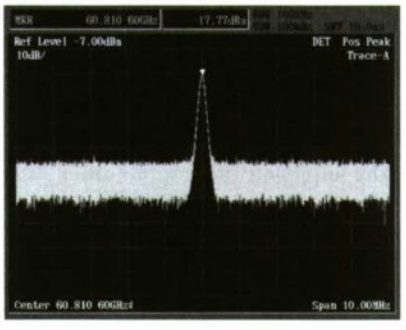

Figure 2. Measured 60GHz signal spectra under free-running (a) and with the injection of a 30GHz local signal. (HEMT-1:V_{ds}=0.4V)

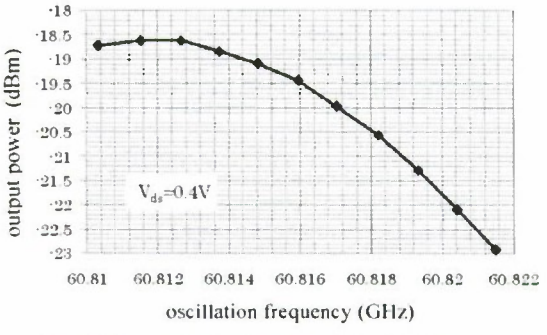

Figure 3. Measured output power vs. the locking frequency. (Injection power -10dBm, HEMT-1:V_{ds}=0.4V)

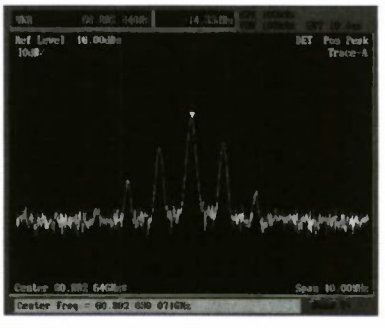

Figure 4. Measured frequency-locked 60GHz signal spectrum with the illumination of the 1MHz amplitude modulated laser beam. (Injection power -10dBm, HEMT-1:V_{ds}=0.4V)

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OPTICAL GENERATION OF MICROWAVE CARRIER WITH HIGH SPECTRAL PURITY USING INTEGRATED DUAL WAVELENGTH SEMICONDUCTOR LASER DIODE

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Abstract

The design and fabrication of an integrated dual wavelength laser diode is reported for optical generation of microwave signal. Microwave carrier with high spectral purity has been generated based on modulation sideband injection locking.

I. Introduction

Microwave and millimeter (mm) wave signal generation by optical means is attractive for future wireless communication systems due to its low cost and wide tuning range [1, 2]. In such applications, microwave carrier with high spectral purity is desired.

Microwave carrier at a particular frequency can be obtained by heterodyning two light waves with the proper frequency difference at a high-speed photodetector (PD). However, owning to the uncorrelated phase variation, heterodyning two free-running semiconductor laser diodes (LDs) would result in a Lorentzian shaped microwave signal with a RF power spectral linewidth the sum of the linewidth of each LD [3]. The key issue in generating microwave carrier with high spectral purity is to secure correlation between the heterodyning light waves, which can be realized by external modulation [4], mode-locked laser [5], optical phase locked loop, and sideband injection locking [6, 7].

In this paper, we report optical generation of microwave signal with low phase noise based on sideband injection by using an integrated dual wavelength laser diode. The advantages of adopting integrated LD in place of discrete LDs will be discussed.

II. Device Design and Fabrication

Figure 1 shows the schematic of our integrated dual wavelength laser diode, which consists of two distributed feedback (DFB) lasers and one Y-branch coupler monolithically integrated on the same AlGaInAs multiple quantum well (MQW) active layer. The angle between the two DFB lasers is 4°, and the curvature radius of the transition waveguide in the Y-branch section is designed to be 11.46 mm to minimize the propagation loss. In order to avoid undesirable mode coupling between the two DFB LDs, the minimum distance between them is designed to be 14 μm.

The epitaxial structure of the device is completed with a two-step metal organic vapor phase deposition (MOCVD) growth. Standard ridge waveguide structure with a ridge width of 2 μm and a ridge height of 1.5 μm is adopted for both the DFB lasers and the Y-branch coupler. The lengths of the DFB laser section and the Y-branch section are 420 and 400 μm, respectively.

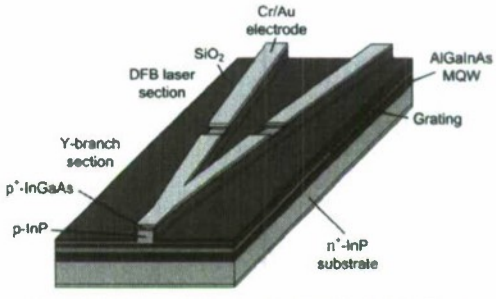

Fig. 1 Integrated dual wavelength laser diode

The typical threshold current of the DFB lasers is around 17 mA. Figure 2 depicts the optical spectrum of the integrated device measured at the Y-branch section facet. By varying the injection currents into the DFB LDs, the wavelength difference between the two lasing modes can be adjusted.

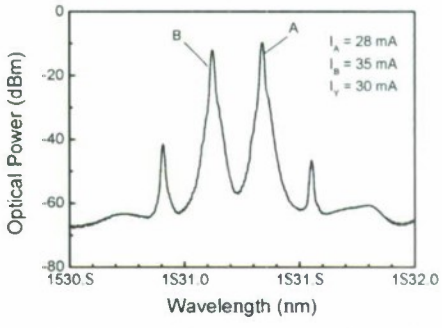

Fig. 2 Optical spectrum of the integrated dual wavelength LD

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III. Microwave Carrier Generation Based on External Injection Locking

Firstly, the experimental setup shown in Fig. 3 is adopted, which is similar to the one reported in Ref. [8], only that the integrated dual wavelength LD is used in place of two discrete slave LDs. A tunable laser works as the master laser (ML), whose output is modulated by a $LiNbO_3$ modulator biased at its half-wave voltage V_π. A circulator is used to couple the output of the $LiNbO_3$ modulator into the integrated dual wavelength laser, which works as two slave lasers (SLs). Light coming out of the integrated LD is fed into a high-speed PD through the circulator, and the microwave beating signal is recorded by an electric spectrum analyzer (ESA). Meanwhile, the spectrum of the light is monitored by an optical spectrum analyzer (OSA).

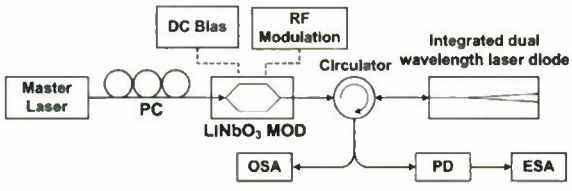

Fig. 3 Microwave generation by external injection locking

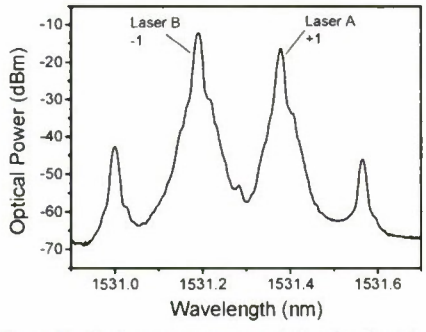

Fig. 4 Optical spectrum upon injection locking

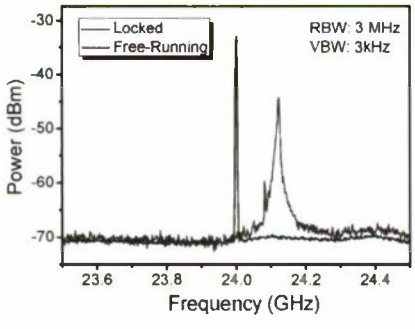

Fig. 5 Electrical spectra of beating signal

During our experiment, a 12 GHz RF modulation signal of 25 dBm is applied to the $LiNbO_3$ modulator. By adjusting the dc bias currents, the two DFB LDs are injection locked to the +1st and −1st order modulation sidebands of the ML, respectively. The optical spectrum upon injection locking is shown in Fig. 4. The electrical spectrum of the 24 GHz beating signal generated by the 12 GHz modulation signal is plotted in Fig. 5. Upon injection locking, microwave carrier with high spectral purity is generated due to correlation between the two heterodyning lights.

In optical microwave generation system based on discrete LDs, the spectral purity of the generated microwave carrier suffers from decorrelation due to optical path difference between the two beating lights [8, 9]. By replacing discrete SLs with monolithically integrated dual wavelength LD, the optical path difference can be made negligible, resulting in improved phase noise performances, as shown in Fig. 6. Meanwhile, monolithically integrated device also greatly reduces the system complexity and cost.

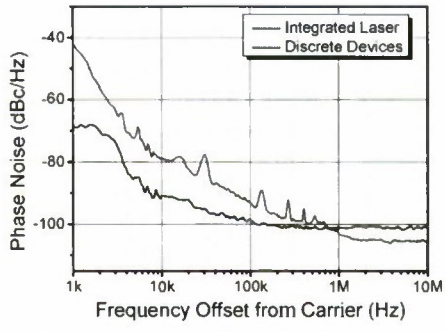

Fig. 6 Phase noise of the 24 GHz microwave carrier

IV. Microwave Carrier Generation Based on Self Injection Locking

To eliminate the need for a $LiNbO_3$ modulator, experimental setup shown in Fig. 7 is then adopted [10]. In this configuration, one of the DFB laser works as the ML and is directly modulated, while the other DFB laser works as the SL and its current is tuned so that it is injection locked to one of the high order modulation sidebands of the ML. Optical injection between the two LDs is realized by reflection at the end facet of the Y-branch section.

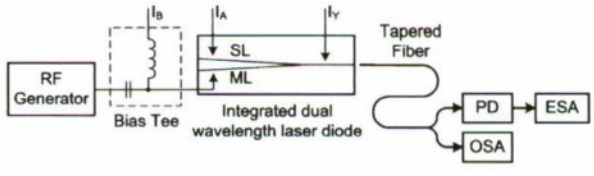

Fig. 7 Microwave generation by self injection locking

To obtain high frequency mm-wave carrier from low frequency modulation signal, it is important to generated high order modulation sidebands. This is accomplished by taking advantages of the enhanced amplitude and frequency modulation response of the LD around its relaxation resonance frequency [11]. In our experiment, the ML is modulated at 5.25 GHz, close to its relaxation frequency of 5.95 GHz. Figure 8 shows the optical spectrum when the SL is injection locked to one of the high order sidebands of the ML.

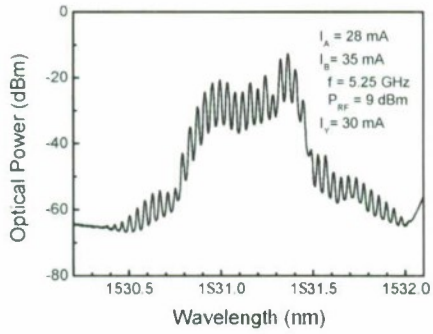

Fig. 8 Optical spectrum of the integrated dual wavelength LD

Figure 9 depicts the measured heterodyne spectra. Peaks at multiples of modulation frequency can be observed due to the enhanced amplitude and frequency modulation response of the ML at around its relaxation frequency. However, the intensity of the peaks at higher frequency decreases rapidly when the SL is unbiased. On the other hand, mm-wave carrier with significant intensity is recorded when the SL is injection locked to one of the high order sideband of the ML.

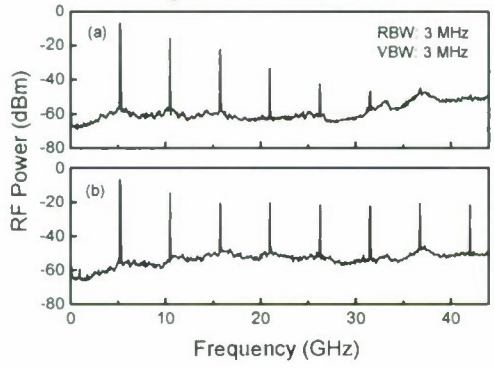

Fig. 9 Electrical spectra (a) w/o and (b) with injection locking

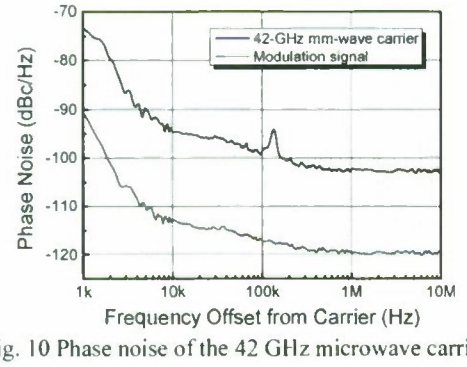

Fig. 10 Phase noise of the 42 GHz microwave carrier

In our experiment, 42 GHz mm-wave carrier is generated from a 5.25 GHz modulation signal, corresponding to eight-fold frequency multiplication. The measured phase noise performance of the 42 GHz mm-wave carrier is shown in Fig. 10, and the phase noise is as low as –94.6 dBc/Hz at 10 kHz offset. The phase noise of the 5.25 GHz modulation signal is also plotted in the figure for comparison. It is seen that there is no additional phase noise degradation apart from the 18 dB degradation corresponding to the eight-fold frequency multiplication.

In a practical wireless communication system, correlated light waves are generated at the central station (CS), whereas heterodyne at the high-speed PD is performed at the base station (BS), which is connected to CS through fiber link [12]. To test its potential in such a wireless system, the output of the integrated dual wavelength diode is sent into single-mode fiber (SMF) with a length of 20 km, and the phase noise of the 42 GHz mm-wave carrier obtained after transmission is shown in Fig. 11. About 10 dB degradation is observed compared with the back-to-back result, which is attributed to the optical path difference between the two beating lights brought about by the dispersion of the SMF [13]. Nevertheless, the phase noise after 20 km SMF fiber transmission is still better than –80 dBc/Hz at 10 kHz offset, showing great promise for applications in future mobile mm-wave communications.

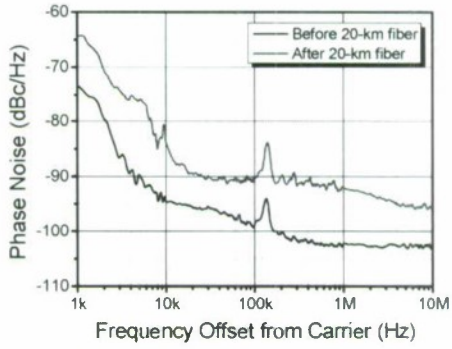

Fig. 11 Phase noise after 20 km SMF transmission

IV. Conclusion

Integrated dual wavelength laser diode has been designed and fabricated for low phase noise microwave carrier generation. Microwave carrier with high spectral purity has been generated by adopting either external or self injection locking scheme. Improved phase noise performance has been verified by adopting the integrated device in place of discrete LDs. The device is believed to have great potential in future mm-wave mobile communication systems.

Acknowledgements

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PROPOSAL OF MULTI-WAVELENGTH INTEGRATION OF ATHERMAL GAAS VCSEL ARRAY WITH THERMALLY ACTUATED CANTILEVER STRUCTURE

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Abstract

We propose a multi-wavelength and athermal VCSEL array with thermally-actuated cantilevers. The lithography-defined cantilever structure enables on-chip multi-wavelength integration. The experiment shows the wavelength spacing of 20 nm for 2-ch VCSEL array with different cantilever lengths.

I. Introduction

Vertical cavity surface-emitting lasers (VCSELs) have been attracting great interest for optical interconnects because of their low power consumption and small footprint. For further increase in data rates even for short reach links, wavelength division multiplexing (WDM) should be one candidate for ultrahigh capacity optical interconnects. However, the temperature dependence of semiconductor lasers, which is typically 0.1 nm/K for single-mode lasers, which is a remaining problem to be solved. The elimination of costly and bulky thermoelectric controllers is needed for use in low cost WDM optical interconnects. Tunable VCSELs with micro-electric mechanical system (MEMS) have been studied [1]-[6]. We reported the athermal operation of 1550 nm VCSELs [7] and 850nm VCSEL [8] with a thermally actuated cantilever based on the bimorph effect.

In this paper, we propose a multi-wavelength and athermal VCSEL array with thermally-actuated cantilevers. An optimal design of cantilever structures enables 10-channel athermal VCSEL array. In addition, a preliminary experiment shows a possibility of the wavelength integration of over 20 nm wavelength span.

II. Design of multi-wavelength athermal VCSELs

Figure 1 shows the schematic structure of a multi-wavelength and athermal VCSEL array we proposed. The side view is shown in Fig. 2. The device consists of a top AlGaAs MEMS mirror, an active region including three GaAs/AlGaAs quantum wells and an AlGaAs bottom p-DBR including an oxide aperture, which provides optical and electrical confinement. The top MEMS mirror is a freely suspended cantilever-shaped AlGaAs n-DBR including a 4 λ (1.1 μ m) thick $Al_{0.85}Ga_{0.15}As$ thermal stress control layer at the bottom. Because of different thermal expansion coefficients in different AlGaAs compositions, we are able to obtain the thermal actuation of the cantilever for compensating the temperature dependence of wavelength. In addition, the cantilever displacement is dependent on the cantilever length, and thus the resonant wavelength can be controlled by changing the cantilever length, which can be lithography defined.

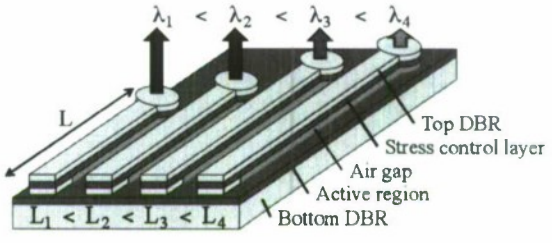

Fig. 1 Schematic structure of multi-wavelength and athermal VCSEL array with different cantilever lengths.

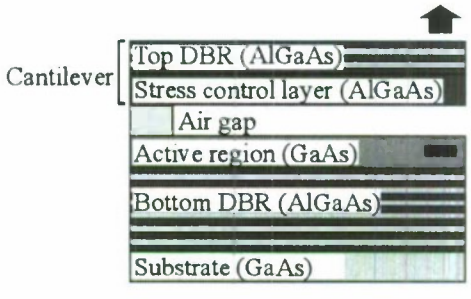

Fig. 2 Schematic structure of athermal VCSEL with a thermally actuated cantilever structure.

We carried out the design of athermal 850 nm VCSELs with a cantilever. The top DBR is 19.5 pair $Al_{0.85}Ga_{0.15}As$ / $Al_{0.2}Ga_{0.8}As$ whose reflectivity is 99.5%. The calculated

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temperature coefficient of wavelength as a function of the cantilever length is shown in Fig. 3 for different stress control layer ($Al_{0.85}Ga_{0.15}As$) thicknesses. We are able to realize the athermal operation for the stress control thickness of $\lambda/2$ (0.137μm) and the cantilever length of 202 μm. The resonant wavelength can be controlled by changing the cantilever length. The cantilever length dependence of wavelength change for different stress control layer thicknesses is shown in Fig. 4.

We have to note that both the athermal condition and the wavelength deviation are dependent on the cantilever length. Therefore, there may be some limitations for making athermal and multi-wavelength VCSEL array. Figure 5 shows the temperature dependence of 10-channels multi-wavelength VCSEL array. When the cantilever length is changed by 3 μm step for each channel, we are able to form 10 channel multi-wavelength VCSEL array in 20 nm wavelength span with avoiding the overlap of lasing wavelength for wide temperature range of -40 ~ 80 ℃. Even without a temperature controller, we are able to lock the lasing wavelength of multi-wavelength VCSEL array.

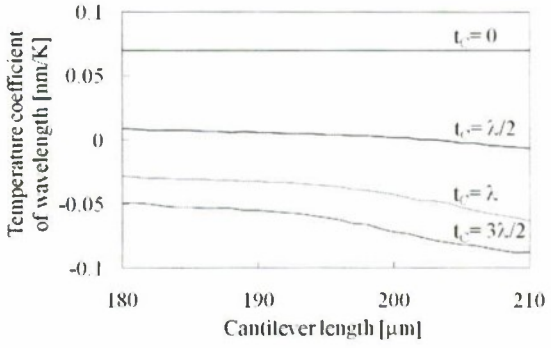

Fig. 3 The cantilever length dependence of temperature coefficient of wavelength for different stress control layer thicknesses.

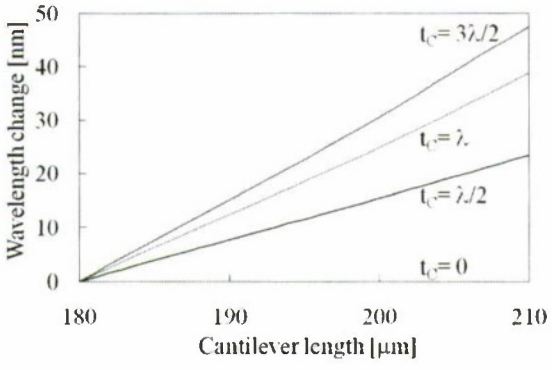

Fig. 4 The cantilever length dependence of wavelength change for different stress control layer thickness.

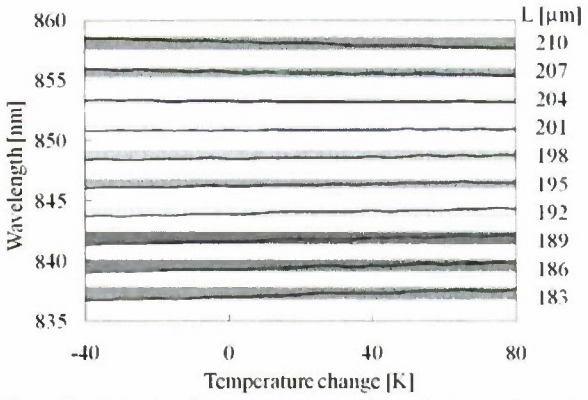

Fig. 5 Calculated temperature dependence of lasing wavelength for 10-ch multi-wavelength, athermal VCSEL array.

III. Fabrication of multi-wavelength VCSEL array

We fabricated a multi-wavelength VCSEL array with different cantilever lengths as shown in Fig. 6. The process includes the formation of a cantilever structure, VCSEL mesa etching, the oxidation process which forms oxide confinement and anti-reflection layer, metal deposition and finally cantilever release by selective etching using citric acid. The air gap is formed by highly selective citric-acid-based chemical etching of a GaAs sacrificial layer underneath the cantilever [9, 10]. The cantilever lengths are 120, 130, and 140 μm. The top electrode is Ni/Au/Ge and the bottom electrode is Au/Zn/Au. The top view of the fabricated array is shown in Fig. 6 (a). The SEM image of the fabricated cantilever structure is shown in Fig. 6(b). The cantilever structure can be freely suspended as shown in the figure.

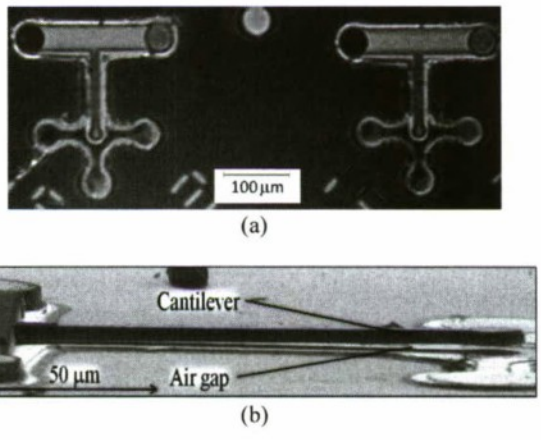

Fig. 6 (a) SEM top view and (b) side view of fabricated multi-wavelength VCSEL array with different cantilever lengths.

We measured the cantilever displacement along the cantilever for different cantilever lengths by using a laser microscope as shown in Fig. 7. The measured result is in agreement with calculations shown in the solid line. Thus we are able to control the cantilever displacement by the cantilever length.

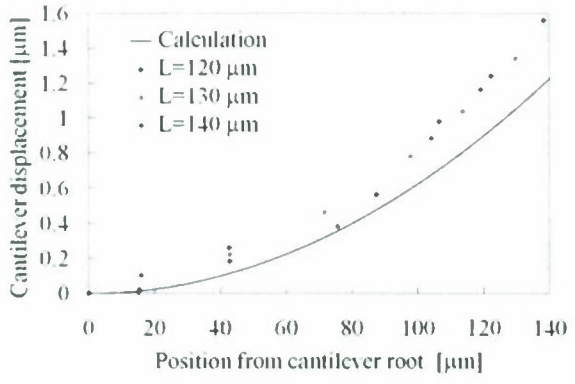

Fig. 7 Measured cantilever displacement along the cantilever position for different cantilever lengths.

Figure 8 shows I/V and I/L characteristics of a fabricated VCSEL with a 10 μm-diameter oxide aperture. Figure 9 shows the lasing spectra of 2-ch VCSEL array with two different cantilever lengths. The cantilever lengths are 120 μm and 130 μm, respectively. Although the device operates in multi-transverse modes, we can see the wavelength separation of 20 nm by changing the cantilever length. We are able to realize single-mode operation just by reducing the oxide aperture. The design of the cantilever structure is different from that of Fig. 5. More precise allocation of wavelengths can be expected.

We measured the lasing wavelength for several VCSEL arrays. In order to avoid the on-wafer fluctuations of layer

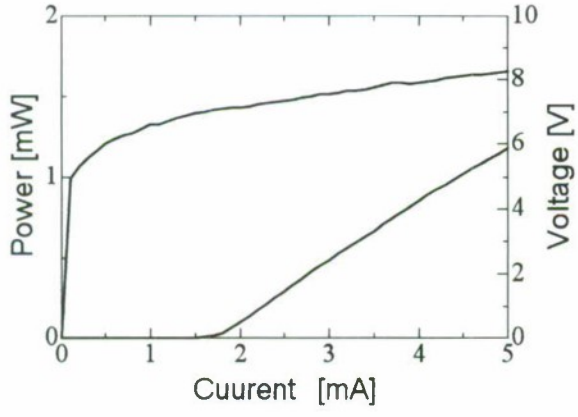

Fig. 8 L/I and V/I characteristics of a fabricated MEMS VCSEL with 10 μm-diameter oxide aperture.

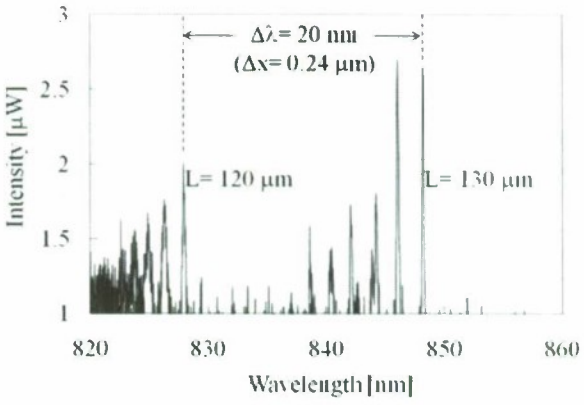

Fig. 9 Lasing spectra of 2-ch multi-wavelength VCSEL array with a lithography-defined cantilever structure having a different length.

thickness and fabrication process, we tested neighboring VCSEL arrays in a 5 mm x 5 mm area. Also, we looked at the wavelength of the same longitudinal mode. The measured lasing separation of neighboring arrays is show as a function of a measured cantilever displacement difference in Fig. 10. The measured result is almost in agreement with the calculation, while we see some scattering of lasing wavelengths due to thickness fluctuations over the wafer. The result shows the precise control of the cantilever displacement enables us to realize the highly controlled multi-wavelength integration of VCSELs.

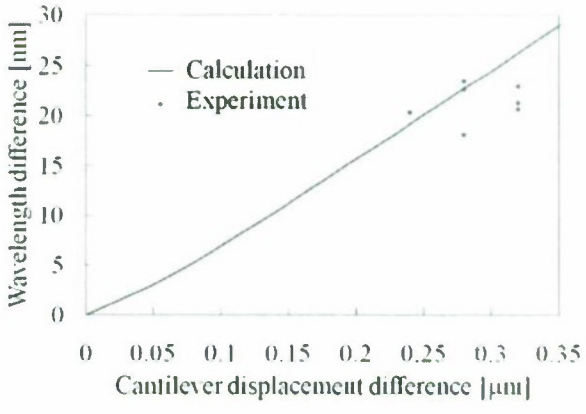

Fig. 10 The measured lasing separation of neighboring arrays is show as a function of a measured cantilever displacement difference.

VI. Conclusion

We proposed the novel multi-wavelength integration of athermal VCSEL arrays with a thermally actuated cantilever structure. The lithography-defined cantilever structure enables on-chip multi-wavelength integration. We expect 10-ch multi-wavelength integration to avoid the overlap with neighboring channels for wide temperature ranges of -40 ~ 80 ℃. We fabricated the VCSEL array with different cantilever lengths. We obtained 20 nm wavelength spacing between neighboring integrated VCSELs with different cantilever lengths. The structure is simple and athermal operation can be expected at the same time. The proposed structure could be useful for future ultra-high capacity optical link technologies with low power consumption. We expect the scalability of multi-wavelength integration by precise control of stress-induced cantilever displacement. The proposed concept may open up the potential of precise manipulation of wavelength in VCSEL arrays.

Acknowledgement

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Light Enhancement in a Microdisk of Composition-Tailored InGaAs Quantum Dots-in-a-Well Structure

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AIR-BRIDGE CONTACT FABRICATION FOR IN-PLANE ACTIVE PHOTONIC CRYSTAL DEVICES

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The fabrication of air-bridge contacts for in-plane active photonic crystal devices is presented. The technology allows to access waveguides as narrow as 200nm. The main fabrication challenges described in detail are surface planarization and formation of isolation layers for contact pads. The issue of surface damage effects on dry-etched sidewalls is addressed and current measurements on narrow contacts were performed.

I. Introduction

The unique properties of photonic crystals (PhCs) have stimulated a lot of ideas and activities in the direction of dense photonic integrated circuits (PICs). Waveguides and numerous other passive devices have been studied and implemented theoretically and experimentally. Many of the most successful experiments were performed in silicon-based membrane-type PhCs (1,2). This is due to the readily available silicon fabrication technology and to the fact that membrane-type devices suffer from lower out-of-plane propagation losses than substrate-type (low refractive index contrast) devices do. However, for PICs, it will eventually be inevitable to implement electrically pumped active devices for light generation/amplification. Due to an indirect bandgap transition, many active functionalities are hard to realize in silicon. Moreover, the membrane-type approach loses its principal advantage of low loss when it comes to adding lossy metal contacts close to the optical mode. Therefore, we choose a substrate-type material system like InP/InGaAsP/InP. A PIN layer structure is grown on an n-doped indium phosphide (InP) substrate for electrical current injection, and planar PhCs are formed by deep etching of holes in a triangular lattice array (3). Using this configuration, electrically pumped PhC waveguide lasers have already been demonstrated (4,5). As a step further, we present a fabrication scheme optimized for the exploitation of unique PhC properties like slow light or the active control of high-Q cavities. For such experiments it is vital that PhC properties be not affected by the metal contact or by an electrically isolating layer which is sometimes used to planarize the PhC device surface. Such layers can shrink and shift the bandgap (6,7) and, for sophisticated PhC functionalities, the accurate device modelling becomes very challenging. Therefore, we developed an air-bridge contacting technique which can access PhC structures like waveguides or waveguide cavities down to a feature size of <200nm.

II. Fabrication

The fabrication of electrical contacts for vertical current injection into narrow PhC waveguides faces a number of challenges. In Fig.1, the proposed process flow is depicted schematically. The first challenge is to find a suitable material to planarize the PhC holes (step (c) in Fig.1). At the same time, that material has to provide the possibility to reliably define narrow contact openings (step (d)), and it has to serve as a sacrificial layer for the formation of the air-bridge (step (f)). The second challenge is to form electrically isolating contact pads. At first sight this might seem trivial, but the choice of an adequate material can be strongly limited by the fabrication steps associated with planarization and air-bridge formation.

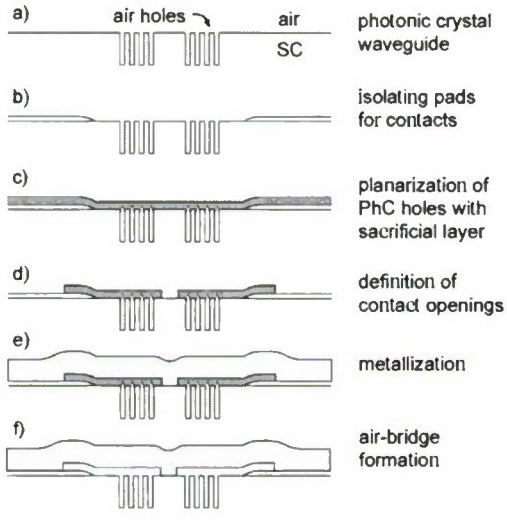

Fig.1: Schematic cross-sectional representation of process flow for air-bridge contact fabrication. In our specific case, the semiconductor (SC) is an InP-based PIN junction.

A. SACRIFICIAL LAYER

All the above-mentioned requirements on the material for the sacrificial layer can be fulfilled by silicon nitride (SiN_x). Firstly, planarization can be achieved by iterative deposition and dry-etching of the material. If the deposition step is more

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isotropic than the etching step, planarization is possible. Therefore, a highly directional etching process has to be chosen. To etch SiN_x, using CHF_3 as a feedgas generally provides good anisotropy. For an increased etching rate, careful additions of O_2 can be considered, which inhibits the formation of a fluorocarbon film on the SiN_x surface (8). However, lateral etching will rapidly set in for too large O_2 contents. Fig.2 shows the planarization of a 900nm wide trench in InP by three cycles of etching and deposition of 300nm of SiN_x. Three cycles are needed to fully close the gap. For PhC holes of less than 300nm diameter, only one etching step is required, as can be deduced from Fig.3, which shows the planarization of a 300nm wide trench. Commercial tools from Oxford Instruments (9) were used for deposition of SiN_x layers (Plasmalab System80Plus PECVD) as well as for dry-etching (Plasmalab System80Plus RIE). The feedgas ratio for the etching step is CHF_3:O_2 = 11:1. The plasma is operated at a pressure of 45mTorr and a self-bias voltage of 380V.

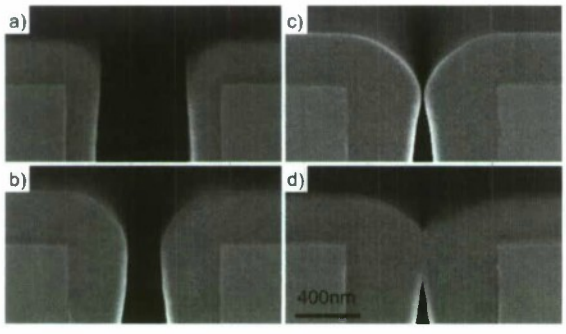

Fig.2: Planarization of a 900nm wide trench etched in InP. 300nm of SiN_x are deposited and dry-etched in alternating steps. (a) single deposition step; (b) one etching cycle; (c) two etching cycles; (d) three etching cycles.

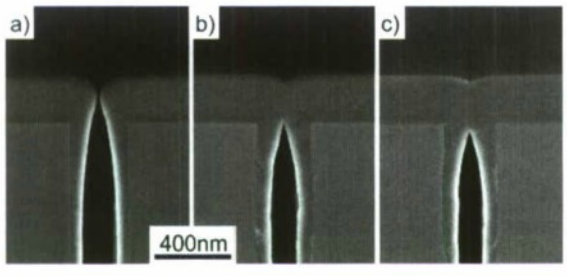

Fig.3: Planarization of a 300nm wide trench in InP using the same procedure as in Fig.2. For a sacrificial layer thickness of 100nm, one cycle of etching is sufficient. This corresponds to panel (b).

The second requirement to be fulfilled by the sacrificial layer material is the possibility to define narrow contact openings. Using a dry-etching process similar to the one for the planarization step, this can easily be achieved by means of an electron beam lithography (EBL) mask. Here, the most critical issue is the alignment with the PhC waveguide, which, depending on the application, can exceed the millimeter length range. Using a Raith150 system (10), we achieve an alignment accuracy below 50nm.

Finally, the removal of the sacrificial planarization layer is performed by wet-etching in hydrofluoric acid (HF). For long waveguides, openings in the metal layer have to be provided for the acid to penetrate. HF removes the SiN_x layer, including sidewall depositions in the PhC holes, very effectively. The removal of SiN_x from sidewalls is crucial to avoid partial filling of holes, which would have effects on PhC properties that are very challenging to predict accurately (cf. Fig.4).

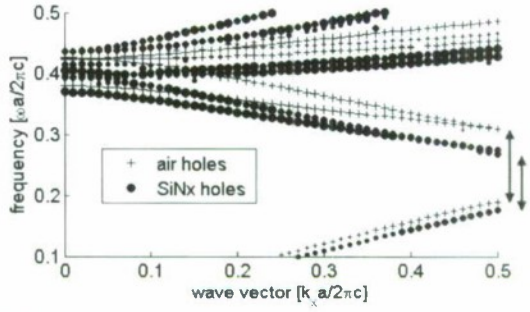

Fig.4: 3D simulation (plane wave expansion method) of TE modes of a triangular lattice PhC in InP. The size of the markers scales with the energy density in the core layer of the corresponding modes. Completely filling the air holes with SiN_x shrinks the bandgap and shifts it slightly (indicated by arrows). The effect of partial filling as in Fig.3 would be challenging to predict accurately.

B. CONTACT PADS

Given the choice of SiN_x for the sacrificial layer and all involved fabrication steps, high demands are set on the isolating material for the contact pads. It must be resistant to high temperatures (SiN_x deposition, contact annealing), insoluble in acetone (metal lift-off), resistant to HF etching (air-bridge formation), and there has to be a way to structure thin layers (~200nm) on indium phosphide (InP) surfaces without interfering with PhC holes (e.g., permanent filling of holes).

Promising material candidates to electrically isolate the contact pads are the Cyclotene™ resins from the Dow Chemical Company (11). In particular, the photosensitive 4000-series (Photo BCB) is attractive for its potential as a negative resist for both photolithography (11) and EBL (12). In the following, the properties of Photo BCB are addressed with respect to the requirements set by the air-bridge fabrication process.

1) Patterning of Photo BCB by EBL

Upon dilution in mesitylene, the thickness of spin-cast Photo BCB layers can be well controlled. Thicknesses of around 200nm are desired to keep the surface clear of protruding features. This can be obtained, e.g., by diluting one

part (weight) of Cyclotene 4022-35 in three parts of mesitylene.

Thin layers of unexposed Photo BCB are very sensitive to ambient light and must be handled with care. Exposed to an electron beam (30kV acceleration voltage), cross-linking sets in at very low doses. However, the contrast value of 0.28±0.02 obtained upon development in DS3000 at 35°C is very low. All feature heights were measured after hard curing of the samples for two hours at 250°C. Since, for the application presented here, sharply defined edges are not of particular interest, no further efforts were spent on finding optimized process conditions for a lower contrast.

During spin-coating of Photo BCB, the resin penetrates into PhC holes and, depending on the exact process parameters, fills them up to a certain level. It was verified by cross-sectional SEM inspection that, if not exposed during EBL, this material is removed completely from the holes during development.

2) Adhesion on InP and resistance to HF etching

Diluted Photo BCB, as described above, offers reasonably good adhesion when spin-cast on InP substrates. Chip sizes of 12mm × 12mm or smaller were used for all experiments. Adhesion was tested both with AP3000 adhesion promoter and without any adhesion promoter. No significant difference was observed.

After EBL exposure, development and hard curing, the resistance of Photo BCB features to HF etching and their adhesion to the InP substrate during that process was tested. A 1:5 dilution of 40% HF in DI water was used for the experiments. It was observed that for the samples which where coated without adhesion promoter, delamination of Photo BCB structures sets in after several minutes. The sample for which the adhesion promoter AP3000 was used was still intact after roughly one hour of HF etching.

3) Temperature stability

Depending on the details of how the process in Fig.1 is implemented, the sample will be subjected to elevated temperatures that must be compatible with all materials present. In the proposed process flow, the Photo BCB pads are added at an early stage and have to withstand all subsequent processing steps. Assuming 30 minutes of PECVD deposition at 300°C and a contact annealing of 2 minutes at 370°C, hard-cured Photo BCB patterns were tested accordingly. Optical inspection revealed no detrimental effects such as cracking, bubbles, or other deformations.

C. DEMONSTRATOR DEVICE

Fig.5 shows an SEM micrograph of a metal air-bridge contact to a W3 waveguide (triangular PhC lattice with three omitted rows of holes), fabricated according to the process flow depicted in Fig.1. It is a Pt/Ti/Pt/Au ohmic contact for an InP-based PIN diode structure, suspended in air and laterally supported by Photo BCB isolating pads. The design is symmetric for stability reasons. The bridge is formed using a SiN_x sacrificial layer. After metallization and contact annealing, the SiN_x layer was removed by HF wet etching for 20 minutes.

Fig.5: SEM image of a metal air-bridge contact (~200nm width) to a W3 PhC waveguide in InP. It is suspended in air and supported by Photo BCB isolating pads. The pattern on the gold layer is a replication of shallow dimples present on the sacrificial layer after planarization of the PhC holes.

III. Further Considerations

A. SIDEWALL EFFECTS

The presented air-bridge contacts are designed to access active PhC waveguide devices. They can be used to form contacts on waveguides as narrow as 200nm. However, as waveguides get increasingly narrow, efficiency of current injection becomes an important issue (e.g., for lasers or SOAs). The etched sidewall surfaces are in close proximity to the active layers of the PIN structure and form a narrow channel for the carriers to pass through. A surface damage layer can affect the final current density and carrier lifetime. Moreover, carriers can move between PhC holes and laterally diffuse out of the interesting regions without crossing the active injection area.

In order to estimate the effect of surface damage, we assume a surface depletion layer as in Ref.13 and, using horizontal current injection through PhC pads of varying filling factor, we measure the relation between conductivity and inter-hole distance (13), as shown in Fig.6. A linear extrapolation to the zero-intercept of conductance yields an estimate of the depth of the defect zone. For our dry-etching process we obtain a value of 50±2nm, measured on n-doped layers ($4.5e17m^{-3}$) of several thicknesses (0.5µm, 1µm, 2µm). A similar procedure was applied for deep trenches to find a surface depletion layer of 59±3nm. The higher value can be attributed to more severe sidewall roughness on etched trench sidewalls as compared to PhC holes, which can be confirmed qualitatively by SEM inspection. Although the depletion depends on a number of factors, such as type of material, doping concentration, and etching process, the obtained values give a first quantitative indication.

Fig.7 shows an example of a V-I characteristic for vertical current injection into an InP/InGaAsP/InP PIN diode. The

contacts are 200µm long and 200nm wide, enclosed in 300µm long deep trench waveguides separated by 220nm. A current of 100mA corresponds to a current density of more than 200kA/cm^2.

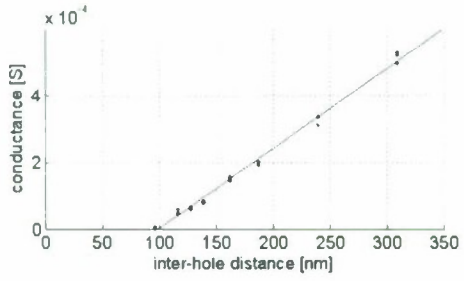

Fig.6: Conductance through 40µm long PhC pads in 10µm wide channels as a function of inter-hole distance. The data (dots) corresponds to a conductive sheet thickness of 0.5µm. Similar behaviour is observed for thicknesses of 1µm and 2µm. The intercept at zero conductance of a linear fit (solid line) occurs where the separation between two holes equals twice the width of the surface depletion zone.

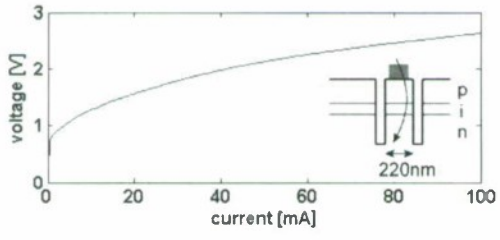

Fig.7: Typical diode characteristics of a PIN junction contacted between deeply etched (~3.5µm) trenches of 220nm separation distance.

B. RESISTANCE VERSUS CONTACT WIDTH

Narrow contacts of 200µm length were formed on an n-doped InP substrate (3.7e18cm^{-3}, no highly-doped cap layer), and voltages were applied across the substrate. Resistances of the contacts were measured at a current density of 10kA/cm^2, which is a typical value for laser diodes and SOAs. Fig.8 confirms an inverse dependency on contact width down to very small feature sizes without unexpected size effects.

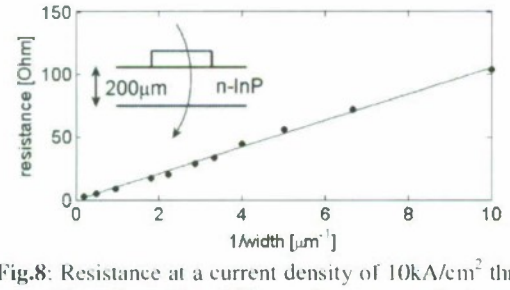

Fig.8: Resistance at a current density of 10kA/cm^2 through contacts of varying width (100nm - 5µm) versus the inverse of the contact width. By use of a highly doped InGaAs cap layer, further reductions are expected.

IV. Conclusions

We presented a fabrication process for air-bridge contacts to access narrow PhC waveguides without interfering with PhC properties by covering or filling the air holes. Considering only technological limitations of the fabrication (dry-etching, EBL alignment precision), active waveguide devices as narrow as 200nm, or even less, can be realized. However, additional limitations arise from the need for efficient current injection. Dry-etched sidewalls present surface damage with sites for carrier recombination. A depletion zone of several tens of nanometers width, depending on the etching process, can be deduced from current measurements through perforated horizontal channels.

In order to directly exploit the unique properties of PhCs in active devices, single-mode operation would be required, which, for an operation wavelength of 1550nm, corresponds to a W1 waveguide width on the order of 500nm. A successful implementation of such a device relies on well-optimized optical and electrical performance. In terms of optics, this can be achieved by addressing the PhC hole shape and sidewall smoothness using advanced dry-etching technology; in terms of electronics, the sidewall damage can be reduced either during etching or by using sidewall passivation techniques.

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InP DHBTs having Simultaneously Deposited Base and Emitter Contacts

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Characterization of InAlAs/$In_{0.25}Ga_{0.75}As_{0.72}Sb_{0.28}$/InGaAs Double Heterojunction Bipolar Transistors

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Abstract

We report on the characterization of InP-based heterojunction bipolar transistors (HBTs) with low turn-on voltage and high current gain by using InGaAsSb as the base layer. The low turn-on voltage of 0.43 V is attributed to the smaller band gap of the $In_{0.25}Ga_{0.75}As_{0.72}Sb_{0.28}$ material. High current gain of 74 is observed despite a heavily Be-doped (9.0×10^{19} cm^{-3}) base is used, suggesting a long minority carrier lifetime (τ_n) in the InGaAsSb material. Moreover, low specific contact resistivity of 5×10^{-8} Ω-cm^2 is also demonstrated on separate $In_{0.25}Ga_{0.75}As_{0.72}Sb_{0.28}$ samples

I. Introduction

Recently, InP/GaAsSb/InP double heterojunction bipolar transistor (DHBT) has attracted great attention because of its superior dc and microwave characteristics, such as high breakdown voltage, high saturation velocity as well as high current gain cut-off frequency. Its type-II base-collector (B/C) junction reduces the current blocking effect, thus increases the operation current density [1,2]. However, electron pile-up often occurs at the type-II InP/GaAsSb emitter-base (E/B) junction and results in a tunneling recombination current that deteriorates current gain (β) at low current regime. Several device structures have been proposed to improve the β of the GaAsSb base DHBTs, such as InGaP/GaAsSb, InAlP/GaAsSb and InAlGaAs/AlGaAsSb E/B junctions [3,4,5]. These emitter junctions are primarily designed to be of type-I lineup to alleviate the electron pile-up issue while increasing β. In this study, an InAlAs/InGaAsSb/InGaAs DHBT with an $In_{0.25}Ga_{0.75}As_{0.72}Sb_{0.28}$ base is proposed for the same purpose. Meanwhile, the $In_{0.25}Ga_{0.75}As_{0.72}Sb_{0.28}$/$In_{0.53}Ga_{0.47}As$ B/C junction maintains its type-II lineup and high current capability as the aforementioned DHBTs. The schematic band diagram of the InGaAsSb base DHBT is shown in Fig. 1. The band gap of the $In_{0.25}Ga_{0.75}As_{0.72}Sb_{0.28}$ material is measured to be 0.67 eV, which is close to the lowest band gap region among the entire composition range of $In_xGa_{1-x}As_{1-y}Sb_y$ material lattice-matched to InP [6]. The valance band discontinuity (ΔE_V) at the $In_{0.52}Al_{0.48}As$/$In_{0.25}Ga_{0.75}As_{0.72}Sb_{0.28}$ junction is estimated to be 0.52 eV. The large ΔE_V prevents the back-injection of holes from the InGaAsSb base to the InAlAs emitter. Therefore, high current gain and low turn-on voltage can be realized simultaneously on the $In_{0.25}Ga_{0.75}As_{0.72}Sb_{0.28}$ base DHBT.

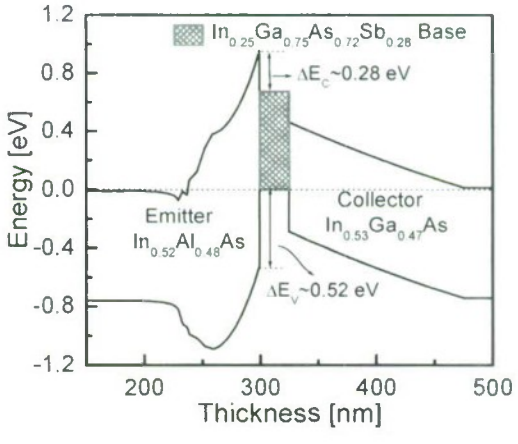

Fig. 1. Schematic band diagram of the $In_{0.52}Al_{0.48}As$/$In_{0.25}Ga_{0.75}As_{0.72}Sb_{0.28}$/$In_{0.53}Ga_{0.47}As$ DHBT.

II. Material Growth and Layer Structure Design

The samples investigated in this work were grown on semi-insulating (100) InP substrates in a Riber 32P solid-source molecular beam epitaxy (MBE) system. The group V elements, i.e. arsenic (As) and antimony (Sb), were delivered using valved cracker cells. Beryllium and Silicon were the p-type and n-type dopants, respectively.

As listed in Table I, the DHBT sample consisted of a 150 nm n-type $In_{0.53}Ga_{0.47}As$ collector doped to 1.0×10^{16} cm^{-3}, a 30

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nm p-type $In_{0.25}Ga_{0.75}As_{0.72}Sb_{0.28}$ base layer doped to 9.0×10^{19} cm^{-3}, and a 40 nm n-type $In_{0.52}Al_{0.48}As$ emitter layer doped to 8.0×10^{17} cm^{-3}. To reduce the emitter resistance, a 25 nm-thick n-type InAlGaAs quaternary graded layer was inserted between the InAs cap layer and the InAlAs emitter.

Large area devices with an emitter size of 75×75 μm^2 were fabricated by using the triple mesa wet etching process. Electron-beam evaporated Pt/Ti/Pt/Au was used for all the electrodes. The dc characteristics of the devices were measured by an HP4156A semiconductor parameter analyzer.

Table 1. Epitaxial layer structure of InGaAsSb base DHBT.

Emitter cap	InAs:Si	5 nm ($\sim8\times10^{19}$ cm^{-3})
E.C. graded	InAlGaAs:Si	25 nm ($\sim8\times10^{18}$ cm^{-3})
Emitter	$In_{0.52}Al_{0.48}As$:Si	40 nm ($\sim8\times0^{17}$ cm^{-3})
Base	**$In_{0.25}Ga_{0.75}As_{0.72}Sb_{0.28}$:Be**	**30 nm ($+9\times10^{19}$ cm^{-3})**
Collector	$In_{0.53}Ga_{0.47}As$:Si	150 nm ($\sim1\times10^{16}$ cm^{-3})
Sub-collector	$In_{0.53}Ga_{0.47}As$:Si	400 nm ($\sim1\times10^{19}$ cm^{-3})
Substrate	InP	Semi-insulating

III. Results and Discussion

Fig. 2(a) illustrates the typical room-temperature forward Gummel plot of the $In_{0.25}Ga_{0.75}As_{0.72}Sb_{0.28}$ base DHBT. The collector turn-on voltage of the DHBT is 0.43 V at current density of 1 A/cm^2. This low turn-on voltage value is comparable to that of the reported GaAsSb base DHBTs [3,4,5,8] It seems that the large conduction band discontinuity (ΔE_C~0.28 eV) at the InAlAs/$In_{0.25}Ga_{0.75}As_{0.72}Sb_{0.28}$ E/B junction does not contribute to the turn-on voltage of the present $In_{0.25}Ga_{0.75}As_{0.72}Sb_{0.28}$ base DHBT. Further investigations on the near unity ideality factor of collector current (η_C~1.09), and the small voltage difference between the forward-mode collector current (I_C) and the reverse-mode emitter current (I_E) confirm that carrier transport in the $In_{0.25}Ga_{0.75}As_{0.72}Sb_{0.28}$ base DHBT is mainly limited by base diffusion instead of the spike at the conduction band discontinuity as shown in Fig. 2(b) [9]. In Fig. 2(a), a high β value of 74 is observed at the collector current density of 1 kA/cm^2 in spite of the use of a thick and heavily doped InGaAsSb base layer.

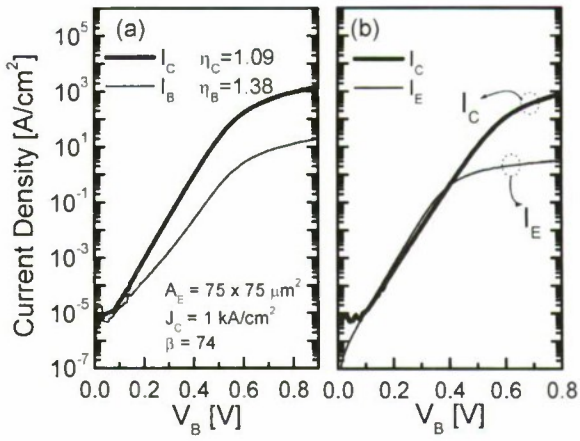

Fig. 2. Room-temperature Gummel plots in the (a) forward-active mode and (b) forward-active and reverse-active modes for the HBT.

In addition to the type-I E/B structure, the high current gain may also be resulted from a long minority carrier lifetime (τ_n) in the InGaAsSb base. Time-resolved excitation correlation (EC) spectroscopy is performed on separate InGaAsSb layers grown on InP substrate. A τ_n as high as 12.5 ps is measured on an $In_{0.25}Ga_{0.75}As_{0.72}Sb_{0.28}$ (N_B=9.0×10^{19} cm^{-3}) sample as shown in Fig. 3. This is in good agreement with the observed current-voltage characteristics and the conclusion that current transport in the InGaAsSb base DHBT is dominated by the base diffusion. Therefore, the long τ_n in InGaAsSb leads to a high current gain.

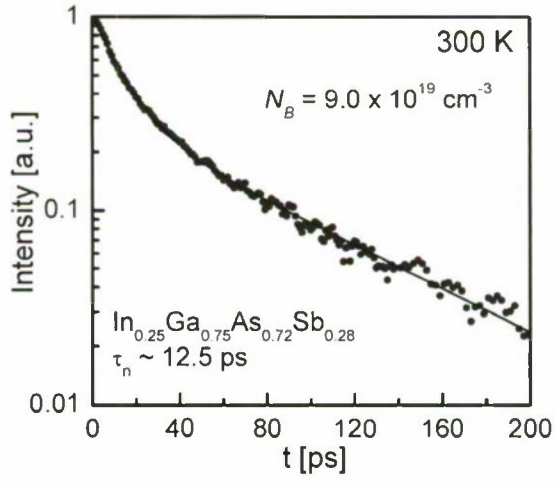

Fig. 3. Electron lifetime is extracted by the time-resolved excitation correlation spectroscopy of the $In_{0.25}Ga_{0.75}As_{0.72}Sb_{0.28}$ bulk layer.

To investigate the effects of the carrier concentration on minority carrier lifetime, $In_{0.25}Ga_{0.75}As_{0.72}Sb_{0.28}$ bulk layer samples (73 nm-thick) are grown with different p-type concentrations under the same growth conditions. The detailed parameters of these bulk samples are listed in Table II. Instead of following the inverse quadratic relation, the τ_n value shows weak dependence on base doping concentration, implying that Auger process is not the major dominant factor of lifetime degradation. Such a long τ_n is beneficial for further increase in base doping concentration (N_B) while maintaining a reasonable current gain.

Table II. Electrical properties and measured minority carrier lifetimes of the InGaAsSb material.

	In (%)	Sb (%)	Rsh Obm/sq	N_B (cm^{-3})	τ_n (ps)
InGaAsSb separate samples (73 nm-thick)	25	28	741	9.0×10^{19}	12.5
			1173	5.9×10^{19}	16.4
			2206	3.5×10^{19}	27.5
			3786	2.9×10^{19}	34.3

For probing the contact issue further, Pt/Ti/Pt/Au ohmic contacts on the four $In_{0.25}Ga_{0.75}As_{072}Sb_{0.28}$ bulk samples with different N_B are fabricated and characterized. The specific contact resistivity (ρ_C) of the contacts determined by transmission line method is shown in Fig. 4. The specific contact resistivity reduces from 2×10^{-6} Ω-cm^2 to 5×10^{-8} Ω-cm^2 as the doping concentration of $In_{0.25}Ga_{0.75}As_{0.72}Sb_{0.28}$ is increased from 2.9×10^{19} cm^{-3} to 9.0×10^{19} cm^{-3}. This result is encouraging for the realization of THz InGaAsSb base DHBTs.

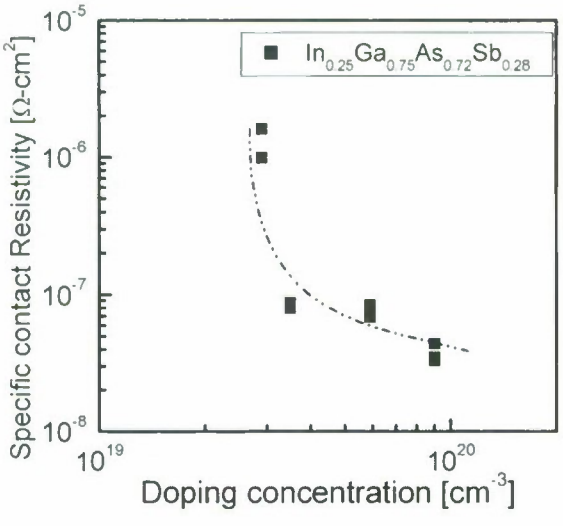

Fig. 4. Specific contact resistivity as a function of doping concentration.

IV. Conclusions

DC characteristics of an InAlAs/$In_{0.25}Ga_{0.75}As_{0.72}Sb_{0.28}$/InGaAs DHBTs are investigated. The low band gap InGaAsSb base leads to low turn-on voltage in the DHBT. A high current gain of 74 is observed despite the use of a thick and heavily doped InGaAsSb base layer. The observed high current gain is attributed to the long minority carrier lifetime in the $In_{0.25}Ga_{0.75}As_{0.72}Sb_{0.28}$ base material. Moreover, a low specific contact resistivity (5×10^{-8} Ω-cm^2) has been achieved on heavily Be-doped $In_{0.25}Ga_{0.75}As_{0.72}Sb_{0.28}$ bulk samples. These characteristics show that the InGaAsSb base DHBT has great potential for THz devices.

Acknowledgments

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Electron Transport through an Abrupt InP/GaInAs DHBT

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Analytical Studies on Temperature Dependence of DC characteristics of InP/GaAsSb Double Heterojunction Bipolar Transistors

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Abstract - In this work, an analytic study of DC characteristics based on the drift-diffusion approach has been performed for the InP/GaAsSb DHBTs. The current transport of InP/GaAsSb/InP DHBTs has been investigated focusing the device temperature dependence. Our simulation results show that, at room temperature, the DC characteristics of the InP/GaAsSb/InP DHBTs is similar to the conventional InP-based HBT using InGaAs as the base layer although a type-II energy band alignment is presented in the InP/GaAsSb HBT. However, due to different mechanisms for the electron injection from the emitter induced by the different conduction band alignments, the InP/GaAsSb HBTs may present a different temperature dependent behavior in term of device current gain as compared to the conventional InP/InGaAs HBTs. Higher current gain could be achieved by the InP/GaAsSb HBTs at elevated temperature.

I. Introduction

InP/GaAsSb/InP double heterojunction bipolar transistors (HBT's) have been proposed and extensively studied in the past years [1] as a new alternative for InP-based DHBT's. Although InP/GaAsSb/InP DHBTs with excellent microwave performance have been demonstrated, detailed analysis the temperature dependent current transport mechanism in NpN InP/$GaAs_{0.51}Sb_{0.49}$/InP DHBT and its impact on the device performance is still limited. Understanding on the temperature dependence of device performance will not only provide a better insight to the device structure design but also practical device applications.

In this work, an analytic study of DC characteristics based on the drift-diffusion approach has been performed for the InP/GaAsSb DHBTs. The current transport of InP/GaAsSb/InP DHBTs has been investigated focusing the device temperature dependence. Our simulation results show that, at room temperature, the DC characteristics of the InP/GaAsSb/InP DHBTs is similar to the conventional InP-based HBT using InGaAs as the base layer although a type-II energy band alignment is presented in the InP/GaAsSb HBT. However, due to different mechanisms for the electron injection from the emitter induced by the different conduction band alignments, the InP/GaAsSb HBTs may present a different temperature dependent behavior in term of device current gain as compared to the conventional InP/InGaAs HBTs. Higher current gain could be achieved by the InP/GaAsSb HBTs at elevated temperatures.

II. Physical Model for Simulation

The device layer structure used for simulation is given in table I. The major difference between the two structures is the base-emitter (B-E) energy band alignment. InP/InGaAs forms a type-I heterojunction while InP/GaAsSb forms the type-II staggered heterojunction. Therefore, the conduction band spike at B-E junction interface seen in the InP/InGaAs is not present in the InP/GaAsSb HBT. To model the carrier transport in the devices, the drift-diffusion formulation is applied with the Possion's equation , which is similar to the approach given in reference [2].

Table I DHBT device structure used in our calculation

Layer	Doping (cm^{-3})	Material	Thickness (μm)
Emitter	n-type 3×10^{17}	InP	0.1
Base	p-type 2×10^{19}	GaAsSb or InGaAs	0.05
Collector	n-type 5×10^{16}	InP	0.4
Subcollector	n-type 5×10^{18}	InP	0.2

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For the InP/GaAsSb structure, the injection of electrons crossing the E-B heterojunction is purely determined by thermionic emission. Also, injection of electron from the base into collector can be achieved under zero electronic field conditions. Based on the thermionic current density expression for the metal-semiconductor system, the electron or hole injection current at B-E heterojunction interface is given by [3] and [4]. The thermionic emission current includes two components: the thermionic emission and thermionic field emission (tunneling), and is given as:

$$J_{ther} = A^* T^2 (1 + P_t) \exp\left(-\frac{V_{barrier}}{kT}\right)\left[\exp\left(\frac{V_a}{kT}\right) - 1\right], \qquad (1)$$

where V_a is applied voltage at the hetero-interface and A^* is the effective Richardson's constant as $A^* = 4\pi q k^2 m^* / h^3$. P_t is the tunneling probability for electron to across the conduction band spike by tunneling[3]. In InP/GaAsSb, due to the absence of the conduction band spike, only thermionic emission is considered by setting P_t=0 during the simulation. Both of the thermionic emission and thermionic field emission (tunneling) are included for the calculation of the InP/InGaAs DHBTs

III. Results and Discussion

Fig.1 shows the base current J_B (sum of bulk base current and surface recombination current) and surface recombination current J_{surf}, in InP/GaAsSb/InP DHBT versus V_{BE} calculated at different temperatures in the range of 100 to 400 K. The surface recombination velocity v_{surf} is set to 10 cm/s during the calculation. As the temperature is lowered from 400 K to 100 K, the increase of GaAsSb band gap reduces the base bulk current components such as radiative recombination and Auger recombination thus bulk J_B. Also, the reduction of intrinsic carrier concentration of GaAsSb in conjunction with the increase of band gap reduces the surface recombination. Combining these two aspects presents a significant reduction of the base current with decrease of the temperature. Notice that, with the decease of temperature, the surface recombination tends to more contribution to the total base current. This is consistent with the experimental observation on the InP-based HBTs [5].

The Gummel plots of InP/GaAsSb/InP DHBT at different temperatures are given in Fig.2. Besides the decrease of the base current with the decrease of the temperature, the collector currents are also reduced. This could be attributed to the increase of GaAsSb band gap at the low temperature, which causes the increase of the conduction band discontinuity at InP/GaAsSb B-E junction. The electron thermionic emission form the emitter into the base is thus limited, reducing the collector current. As the temperature decreases from 400K to 100K, the base-emitter turn-on voltage is increased more than 0.4 V. Similar results are obtained in referenced InP/InGaAs/InP DHBT which was confirmed by the experiments [4].

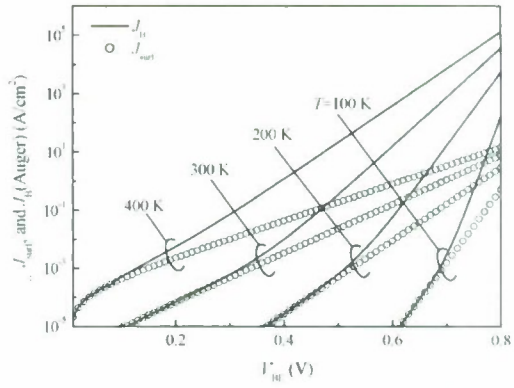

Fig. 1 Base J_B and base surface recombination component J_{surf} versus V_{BE} in an InP/GaAsSb DHBT at different temperatures.

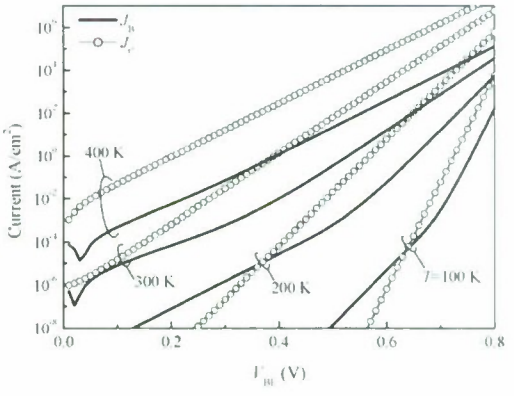

Fig.2 Gummel plots of an InP/GaAsSb DHBT at different temperatures.

The β versus J_c at different temperatures for InP/GaAsSb/InP and InP/InGaAs/InP DHBTs are shown in Fig.3. The temperature is varied from 100 K to 450 K with a step of 50 K. Besides the decrease of the base current with the decrease of the temperature, the collector currents are also reduced. This could be attributed to the increase of GaAsSb band gap at the low temperature, which causes the increase of the conduction band discontinuity at InP/GaAsSb B-E junction. The electron thermionic emission form the emitter into the base is thus limited, reducing the collector current. As the temperature decreases from 400 K to 100 K, the base-emitter turn-on voltage is increased more than 0.4 V. Similar results are obtained in referenced InP/InGaAs/InP DHBT. It can be seen that the β of InP/GaAsSb DHBT is more sensitive to temperature.

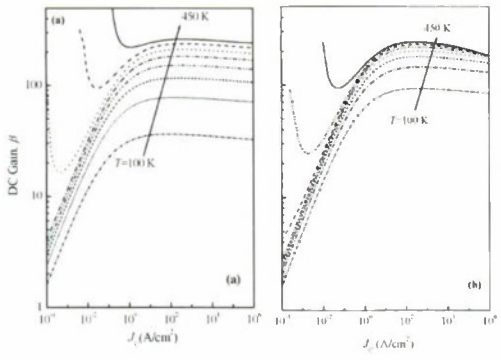

Fig.3 DC gain β versus J_C for (a) InP/GaAsSb and (b) InP/InGaAs DHBTs calculated in the temperature range from 100 to 450 K with a step of 50 K.

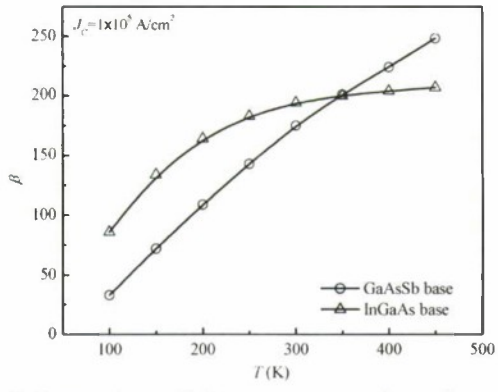

Fig. 4 Comparison of the temperature dependence of β between InP/GaAsSb and InP/InGaAs DHBTs at $J_C=10^5 A/cm^2$.

For the given structures, it can be seen in Fig.4 that the DHBT with a GaAsSb base show a smaller DC gain at low temperature. It can be seen that the β of InP/GaAsSb DHBT is more sensitive to temperature. For the given structures, the DHBT with a GaAsSb base show a smaller DC at low temperature as compared to the referenced InP/InGaAs HBT. However, with the increase of temperature, the β for the InP/GaAsSb HBT is increased almost monotonously, while β for the InP/InGaAs HBT shows a saturation behavior at high temperature. A higher β is observed on the InP/GaAsSb HBT if the temperature is higher than 350 K. The different trend for the temperature dependence of β obtained in the two structures is due to the difference of electron injection from the emitter. In InP/GaAsSb structure, the electron injection from emitter to base is solely determined by thermionic emission. The emitter current injection and thereby the collector current is related to the Equation (1) with P_t=0. By setting the P_t to 0, plotting the temperature-dependent J_{ther} gives a monotonously increasing trend with the increase of temperature. Therefore, the β for InP/GaAsSb HBT shows a more sensitive (positive) temperature-dependence. However, in InP/InGaAs HBTs, the thermionic-field emission plays a more important role than thermionic emission in determining the electron injection. Therefore, the temperature dependence of tunneling probability P_t should provide an important contribution and significantly affect the temperature dependence of the collector current. As shown in reference [3], P_t reduces with the increase of the temperature and tends to saturate at high temperature region. This is believed to be the major course of the saturation of β at elevated temperatures observed in referenced InP/InGaAs device.

IV. Conclusion

In conclusion, an analytic study of DC characteristics based on the drift-diffusion approach has been performed for the InP/GaAsSb DHBTs. The current transport of InP/GaAsSb/InP DHBTs has been investigated focusing the device temperature dependence. Our simulation results show that, at room temperature, the DC characteristics of the InP/GaAsSb/InP DHBTs is similar to the conventional InP-based HBT using InGaAs as the base layer although a type-II energy band alignment is presented in the InP/GaAsSb HBT. However, due to different mechanisms for the electron injection from the emitter induced by the different conduction band alignments, the InP/GaAsSb HBTs may present a different temperature dependent behavior in term of device current gain as compared to the conventional InP/InGaAs HBTs. Higher current gain could be achieved by the InP/GaAsSb HBTs at elevated temperature, which could be important for power applications.

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HIGH LINEARITY 2-BIT CURRENT STEERING InP/GaInAs DHBT DIGITAL-TO-ANALOG CONVERTER

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Abstract

We present a high linearity 2-bit digital-to-analog converter (*DAC*) implemented in an InP/GaInAs DHBT technology. The DAC is based upon the current steering architecture. Cascode structure and layout techniques, i.e. static shuffling and dummy devices, have been used to enhance the linearity. The DAC exhibits static integral/differential nonlinearities of 5.5×10^{-3} LSB, equivalent to a resolution of 9.2 bits. Dynamic measurements qualitatively show proper behavior at 6 GS/s, while simulations with typical on-chip load exhibit sufficiently fast settling at 20 GS/s.

I. Introduction

Analog-to-digital converters (*ADCs*) based upon HBT technologies have reached record breaking sampling rates (1-4). However, the existing technologies set strict limitation on the maximum number of transistors that can be incorporated in a single circuit. As a result, HBT-based ADCs usually rely upon the flash and delta-sigma ($\Delta\Sigma$) architectures. Digital-to-analog converters (*DACs*) embedded in standard

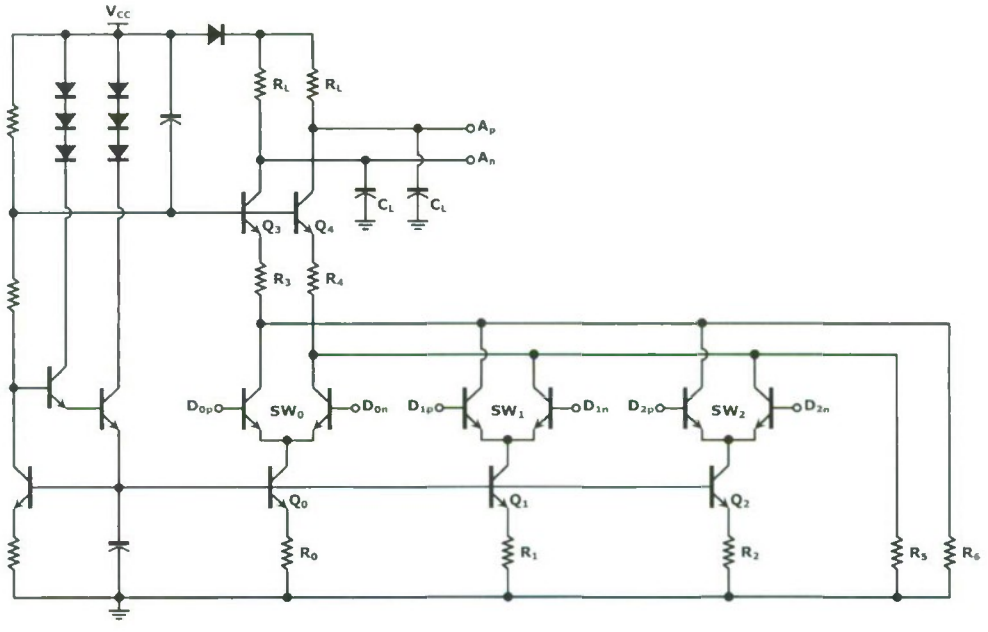

Fig. 1. Schematic circuit diagram of the DAC

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CMOS ΔΣ ADCs are typically of low resolution, namely 1 to 3 bits. Nevertheless, the linearity of the embedded DAC must be sufficiently high to support the final resolution of the ΔΣ ADC (5). The resolution of HBT-based low over-sampling ΔΣ ADCs may be as high as 8 bits, (6, 7), and since digital methods of nonlinearity correction are too complex for HBT technologies, all HBT-based ΔΣ ADCs known to us incorporated a single-bit DAC, which is linear by definition (6, 8). Here, we present a high linearity current steering two-bit DAC implemented in an InP/GaInAs HBT technology. A two-bit DAC can significantly improve the resolution of a ΔΣ ADC, compared to a single-bit ΔΣ ADC of the same complexity and sampling rate.

II. DAC Design

The DAC is based on the standard differential current steering architecture (9) with a common-base output stage in the cascode configuration, as shown in Fig. 1. Each input bit (D_0-D_2) switches the current between the outputs of a differential pair (SW_0-SW_2). The digital input is provided in the thermometer coding format; hence, the switched current sources (Q_0-Q_2) are identical. A common base output stage (Q_3-Q_4) is used to increase the output resistance. Additional resistors (R_5-R_6) maintain the common base stage in the active mode, in case all the bits are "1"s or "0"s. Finally, the resistors R_3-R_4 and the capacitors C_L filter out the output overshoots caused by sharp input transients.

The layout of the circuit is shown in Fig. 2. The switches SW_0-SW_2, the transistor pair Q_3-Q_4, and the resistor pairs R_3-R_4 and R_5-R_6, are all matched in common centroid structures. The resistors R_0-R_2 and the current sources, Q_0-Q_2, are shuffled in a manner that each device consists of 3 parallel devices. To enhance device uniformity, two rows of dummy transistors provide uniform metal density around the current source transistors during the etching of the transistor layers. Fig. 3 illustrates this method.

The DAC was fabricated by the Fraunhofer Institute for Applied Solid State Physics (*IAF*) using their InP/GaInAs DHBT technology (10). A microphotograph of the chip is shown in Fig. 4. Total die area is 1x0.75 mm^2.

III. DAC Performance

The static (DC) transfer function of the DAC, shown in Fig. 5, exhibits a least-significant bit (*LSB*) voltage of 241.67 mV and offset of 7.5 mV. The integral and differential nonlinearities (*INL* and *DNL*) were smaller than 0.0055·LSB, indicating a spurious free dynamic range (*SFDR*) of 57.2 dB, i.e. 9.2 effective bits (see Fig. 6). The total power consumption was 90 mW, using a supply voltage of 6 V.

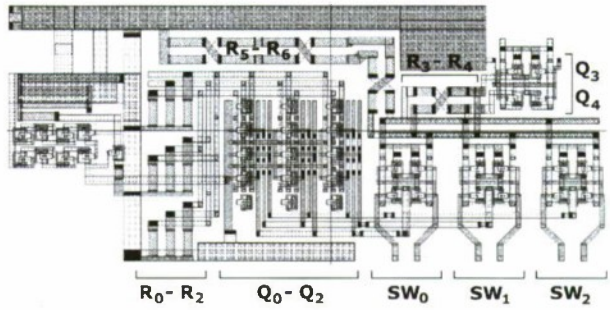

Fig. 2. Layout of the DAC

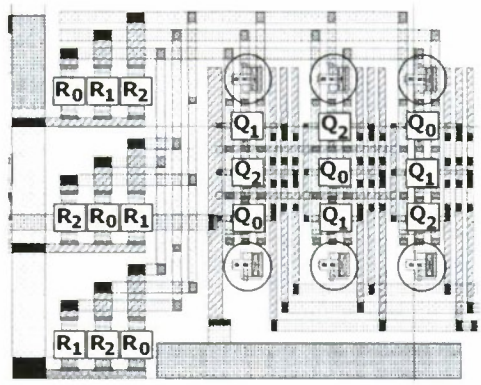

Fig. 3. Close up of the layout of transistors Q_0–Q_2 and resistors R_0–R_2, showing the static shuffling. Each element consists of three devices connected in parallel. Encircled are the dummy transistors

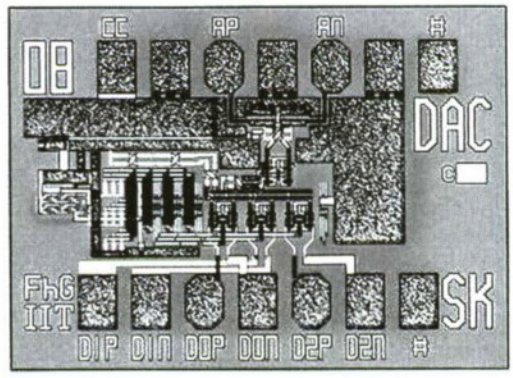

Fig. 4. Microphotograph of the circuit

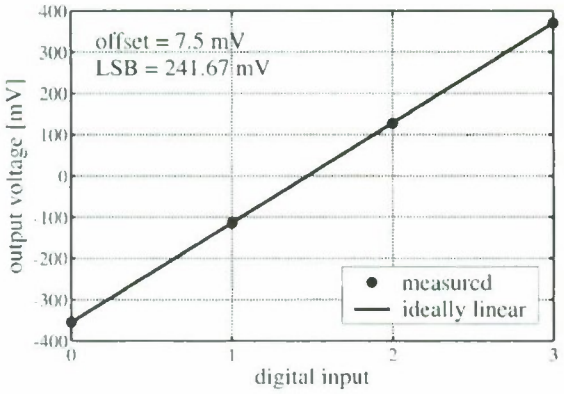

Fig. 5. DC transfer function of the DAC

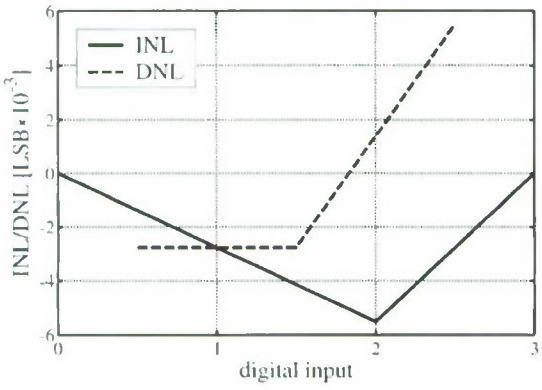

Fig. 6. Integral and differential nonlinearities of the DAC. Obtained SFDR is 57.2 dB (9.2 effective bits) indicating that multibit ΔΣ ADCs are feasible in InP HBT

For the dynamic test one bit was toggled at 6 Gb/s, and the differential output was sampled by an oscilloscope. The oscilloscope output is shown in Fig. 7. Since we have no data on cable attenuation and mismatch at the oscilloscope inputs, the waveforms provide only qualitative information on the behavior of the DAC at high frequencies. The attempts to measure at a higher sample rate were unsuccessful most probably due to output mismatch. Circuit performance was simulated, however, while loaded by a differential integrator with 200 Ω resistors. The simulated response at 20 GS/s is shown in Fig. 8. The simulated output settles to a 0.0055·LSB band in less than a half period.

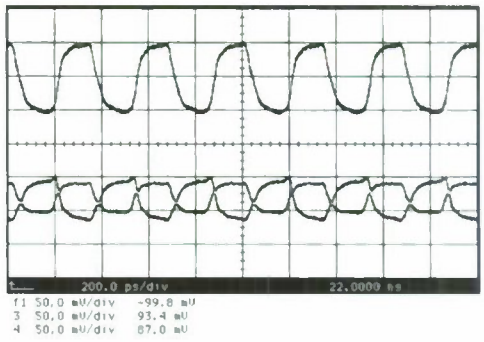

Fig. 7. Measured waveforms of the DAC output (one bit is toggling at 6 Gb/s): differential (top) and single ended (bottom)

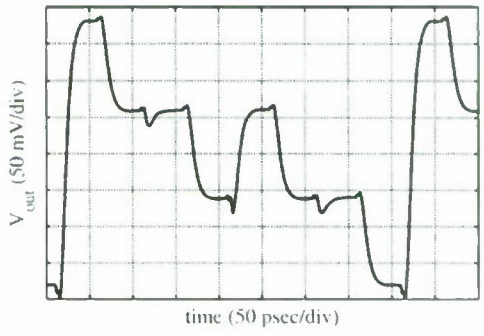

Fig. 8. Simulated waveform of the DAC output at 20 GS/s. The input sequence was 3-2-2-1-2-1-1-0-3.

IV. Conclusion

An InP DHBT-based current steering 2-bit DAC with static linearity of 9.2 bits was presented. Simulated output settles to a 0.0055·LSB band in less than 25 psec, but experimental performance was demonstrated only up to 6 GHz due to output mismatch. This circuit demonstrates that high speed multibit ΔΣ ADCs can be implemented using the InP HBT technology.

Acknowledgement

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DC and RF cryogenic behaviour of InAs/AlSb HEMTs

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Abstract

DC and RF properties are reported for InAs/AlSb HEMTs operating under cryogenic conditions (6 K) for a drain source bias up to 0.3 V. Compared to room temperature (300 K), a large improvement in device properties was observed: lower R_{on}, lower g_{ds}, a more distinct knee in the I_{ds} (V_{ds}) characteristics, increased f_t and a reduction of the gate leakage current of more than two orders of magnitude. This makes InAs/AlSb HEMT technology of large interest in cryogenic low-noise amplifier designs with high constraints on power dissipation.

I Introduction

The combination of high electron mobility, high peak velocity and elevated concentration of electrons in the InAs channel makes the InAs/AlSb HEMT suitable for operation in high speed applications. Furthermore, the InAs/AlSb HEMT can operate at one tenth of the power dissipation of conventional InAlAs/InGaAs/InP HEMTs exhibiting similar RF performances [1]. This makes the InAs/AlSb HEMT a very promising device for applications such as space or mobile microwave/millimetre-wave communications systems where high speed must be combined with very low power dissipation [2]. The cryogenic properties of InAs/AlSb HEMTs have however not been extensively documented. We earlier investigated DC device properties of 110 nm gate-length InAs/AlSb HEMTs at 30 K [3]. We here report both DC and RF properties for 80 nm and 110 nm gate-length InAs/AlSb HEMTs operating at 6 K.

II Experimental

The InAs/AlSb HEMT heterostrueture was grown by molecular beam epitaxy in a Riber 21 TM chamber on two-inch semi-insulating InP substrates. The epitaxial strueture of the InAs/AlSb HEMT is described in detail in Ref. [4]. Shallow mesa isolation was performed by dry etching (Cl_2/Ar) into the metamorphic buffer. Pt/Pd/Au ohmic contacts with a source-drain distance of 2 µm were deposited and subsequently annealed for 15 minutes at 275 °C. Ti/Pt/Au T-shaped gates were defined by electron-beam lithography with two different gate lengths, 110 nm or 80 nm. Prior to gate metallization, a 9 nm deep gate-recess was etched through the cap layer by a pH-adjusted citric acid/H_2O_2. A contact resistance R_c of 0.03 Ω·mm and a sheet resistance R_{sh} of 120 Ω/□ was measured at 300 K using on-wafer transmission line model (TLM) test structures. Hall measurements performed at 300 K showed a sheet carrier density of 3×10^{12} cm^{-2} and an electron mobility of 15000 cm^2/Vs. The devices were characterized by DC and small-signal RF measurements at room- and cryogenic temperature. The cryogenic measurements were carried out at 6 K in a LakeShore probestation using an HP 4156B parameter analyzer and a 67 GHz Agilent 8361A PNA.

III Results and discussion

The electrical measurements were performed on HEMTs with widths of 2x20 µm. The drain-source current I_{ds} as a function of the drain-source voltage V_{ds} was first measured at 300 K. The gate voltage V_{gs} was swept between 0 V and -1.4 V in steps of 0.2 V; See Fig. 1(a). As expected the 80 nm gate length device showed a slightly higher drain current compared to the 110 nm device due to the lower gate length. Furthermore, the 80 nm device exhibited a higher output conductance g_{ds} (350 mS/mm at V_{ds} = 0.2 V and V_{gs} = 0 V) and worse current pinch-off compared to the 110 nm device. This is mainly due to a non-optimized gate length/gate-to-channel distance ratio. The two gate lengths exhibited no current saturation and high g_{ds}, especially for low V_{gs}, due to the accumulation of holes in the $Al_{0.8}Ga_{0.2}Sb$ metamorphic buffer caused by the well known impact ionization effect [5]. The measured on-resistance R_{on} was 0.52 Ω·mm and 0.56 Ω·mm for the 80 nm and 110 nm gate-length device, respectively, at 300 K.

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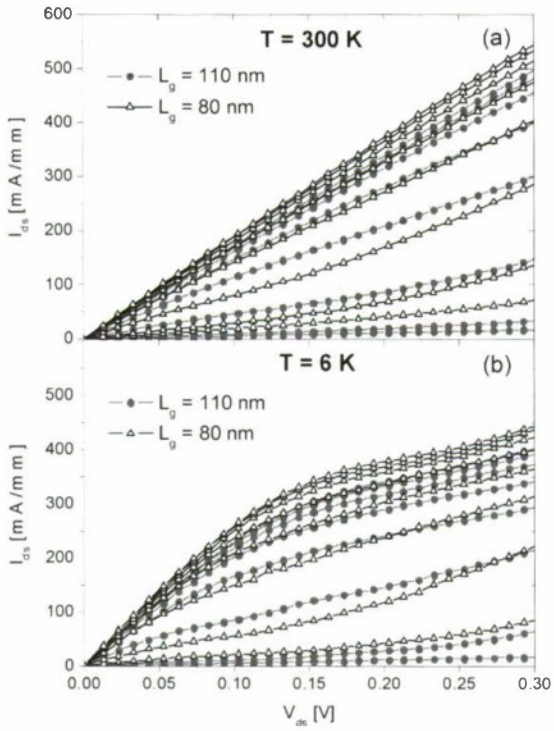

Fig. 1: $I_{ds}(V_{ds})$ with V_{gs} swept from 0 V to -1.4 V in steps of 0.2 V for a 110 nm (black triangles) and a 80 nm (red circles) gate length InAs/AlSb HEMTs at 300 K (a) and 6 K (b).

When measured at 6 K, it was observed that the InAs/AlSb HEMTs exhibited a much improved dc behaviour compared to 300 K. In Fig. 1(b), the I-V curve shows a pronounced well-behaved knee characteristic with a much lower g_{ds} (about 110 mS/mm at V_{ds} = 0.2 V and V_{gs} = 0 V) and lower R_{on} of 0.36 Ω·mm and 0.40 Ω·mm for the 80 nm and 110 nm gate length device respectively; See Fig. 2.

The I_{ds} as a function of the gate voltage V_{gs} and the extrinsic dc transconductance g_m at 300 K and V_{ds} = 0.3 V are shown in Fig. 2(a). At 300 K, the 80 nm device had a peak g_m of 809 mS/mm at V_{gs} = -1.05 V while the 110 nm device exhibited a peak g_m of 865 mS/mm shifted by 100 mV (V_{gs} = -0.95 V). As shown in Fig. 2(b), at 6 K, the g_m peak was 798 mS/mm at V_{gs} = -1.3 V for the 80 nm device and 852 mS/mm at V_{gs}= -1.15 V for the 110 nm device; the V_{gs} shift of the peak g_m was 150 mV for this gate length. This unexpected behaviour of slightly lower (8 %) g_m upon reducing the gate length was also confirmed by Monte Carlo simulations at 300 K. This is due to, first, that the gate length has been scaled with no reduction of the gate-channel distance, and second, that the electron transport is already ballistic under the gate for the 110 nm device at 300 K. Hence the electron velocity is not improved neither when reducing the gate length [6] nor when lowering the temperature. Furthermore, at 6 K, g_m has a sharper profile for both gate lengths due to an improved accumulation of electrons near the top heterojunction of the channel.

The gate leakage current I_g at 300 K is shown in Fig. 3(a). The gate current is composed of the sum of (i) the monotonically increasing electron current due to thermionic injection over the metal Schottky-barrier and (ii) the bell-shaped hole current which results from holes generated due to impact ionization mechanisms which exit the device through the gate electrode [7]. The signature of impact ionization is clearly observed at 300 K and 6 K for both 80 nm and 110 nm gate lengths. At 300 K, the impact ionization component of the gate current exhibited a peak of about 10 μA in the 80 nm device and 11 μA in the 110 nm device but with a 100 mV shift toward higher negative gate voltage for the 80 nm gate-length device. This shift is due to the different gate length/gate-to-channel distance ratio for the two devices. The Schottky component of I_g at V_{gs} = -1.4 V was about 14 μA in the 80 nm device and above 20 μA for the 110 nm device due to the larger gate area. The gate current density is 437 A/cm^2 for the 80 nm gate length and 454 A/cm^2 for the 110 nm gate length. When the devices were cooled down to 6 K, both the impact ionization component and the Schottky component were strongly reduced; See Fig. 3(b) The impact ionization peak was reduced to 4 μA in the 80 nm device and to 5.5 μA in the 110 nm device respectively. The lower impact ionization effect in the channel under cryogenic operation is directly related to the reduction of g_{ds} in the $I_{ds}(V_{ds})$. This strong improvement cannot be associated with reduced impact ionization, since the thermal energy of electrons constitutes an insignificant fraction of the total energy of electrons for V_{ds}=0.3 V at 6 K.

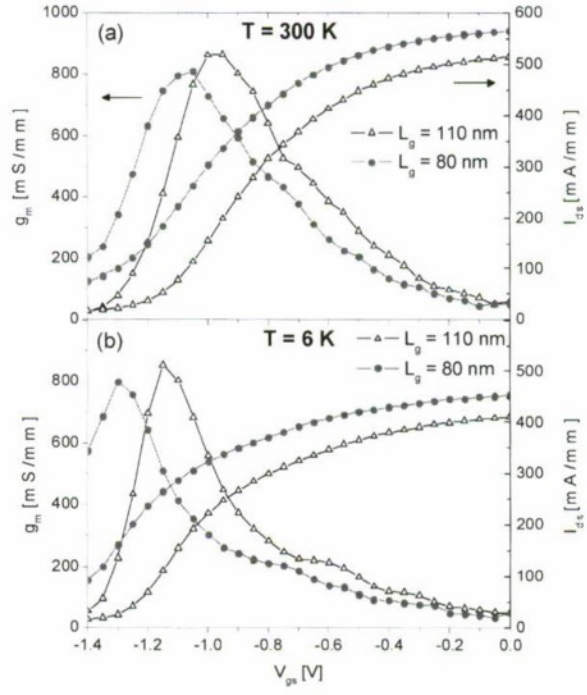

Fig. 2: I_{ds} and g_m versus V_{gs} at V_{ds} = 0.3 V for a 110 nm (black triangles) and a 80 nm (red circles) gate length InAs/AlSb HEMTs at 300 K (a) and 6 K (b).

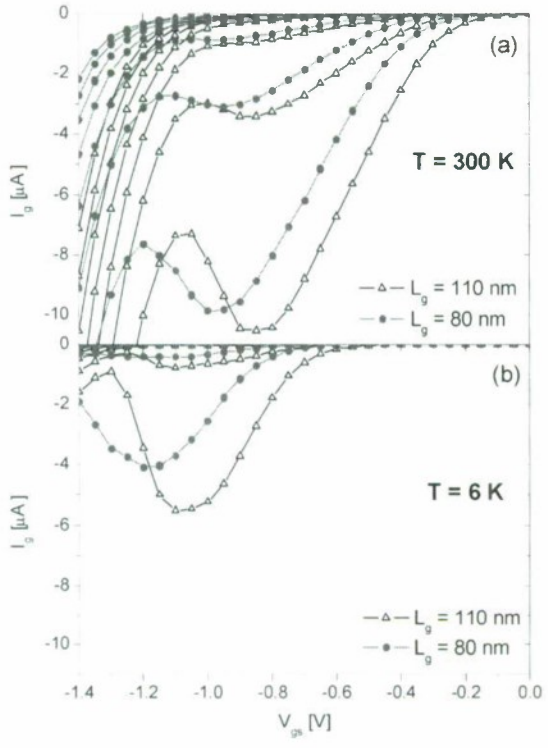

Fig.3: I_g (V_{gs}) with V_{ds} swept from 0 V to 0.3 V in steps of 50 mV for a 110 nm (black triangles) and a 80 nm (red circles) gate length InAs/AlSb HEMTs at 300 K (a) and 6 K (b).

Rather a variation in the hole dynamics involving hole accumulation under the gate may be the origin of the weakened influence from impact ionization at low temperature. At 6 K, the Schottky component of I_g at V_{gs} = -1.4 V is also reduced to less than 2 μA in the 110 nm gate length device. For the 80 nm HEMT it was not even possible to distinguish the Schottky component in the $I_g(V_{gs})$. The gate leakage I_g was also measured at V_{gs} = -1 V and V_{ds} = 0 V sweeping the temperature from 300 K to 6 K; See Fig. 4. At this particular bias point, the main contribution to the gate current leakage is due to the Schottky component. In the 80 nm device, the I_g decreased from 105 nA at 300 K to 393 pA at 6 K. The 110 nm device behaved similarly showing an I_g reduction from 158 nA at 300 K to 420 pA at 6 K. The gate leakage current at 6 K is hence more than two orders of magnitude lower than the value at 300 K. The sharp reduction follows an exponential dependence with temperature and could be due to the exponential temperature dependence of the thermionic emission processes.

RF small-signal measurements were performed in the frequency range between 100 MHz and 67 GHz at 300 K and 6 K after a standard line-reflect-match calibration. The small-signal measurements have been conducted for a drain-source bias of 0.2 V, i.e for a bias point where the impact ionization is not dominating as observed in Fig. 3. At 300 K, the cut-off frequency f_T, extrapolated with a -20 dB/dec slope, was 102 GHz and 105 GHz in the 80 nm and 110 nm HEMT, respectively. The power consumption, calculated as the product $V_{ds} \times I_{ds}$, was 37 mW/mm and 26 mW/mm for the 80 nm and 110 nm HEMT, respectively. At 6 K, f_T increased to 128 GHz in the 80 nm device and up to 139 GHz in the 110 nm HEMT mainly due to the reduction of the output conductance g_{ds} as well as to the reduced access resistances related to a transport improvement in the channel when reducing the temperature. The power consumption was 36 mW/mm and 28 mW/mm for the 80 nm and 110 nm HEMT, respectively.

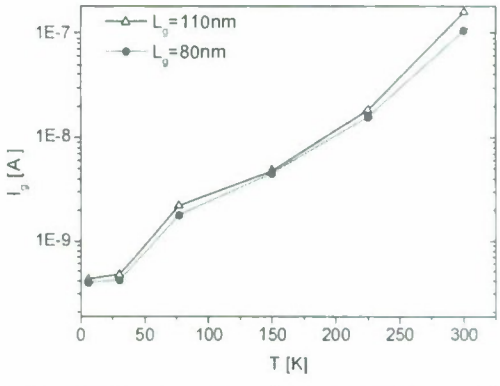

Fig.4: I_g as a function of temperature for V_{ds} = 0 V and V_{gs} = -1 V in the 110 nm (black line) and 80 nm (red line) gate length InAs/AlSb HEMTs.

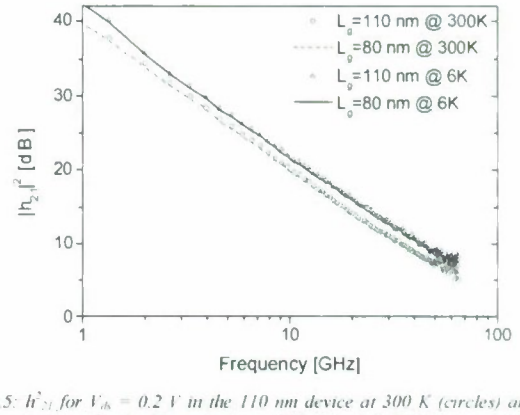

Fig.5: h_{21} for V_{ds} = 0.2 V in the 110 nm device at 300 K (circles) and 6 K (triangles) and for the 80 nm device at 300 K (red dashed line) and 6 K (blue line).

IV Conclusions

DC and RF properties at or below 0.3 V for InAs/AlSb HEMTs were clearly improved when reducing the operating temperature from 300 K to 6 K such as lower R_{on}, reduced gate current leakage, and higher f_T. The peak g_m was observed to shift towards more negative V_{gs}. Reducing the gate length from 110 to 80 nm suggested a slight shift in V_{th} and peak g_m,

higher $I_{ds,max}$, and lower gate leakage current. The observed improvement of the dynamic performance of InAs/AlSb HEMTs at 6 K compared to 300 K makes this a promising technology candidate for integrated microwave cryogenic designs operating at very low power dissipation.

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An 80 nm $In_{0.7}Ga_{0.3}As$ MHEMT with Flip-Chip Packaging for W-Band Low Noise Applications

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Abstract— **The fabrication process of an 80 nm $In_{0.7}Ga_{0.3}As$ MHEMT device with flip-chip packaging on Al_2O_3 substrate is presented. The flip-chip packaged device exhibited good dc characteristics with high I_{DS} = 425 mA/mm and high g_m = 970 mS/mm at V_{DS} = 1.5 V. Besides, the RF performances revealed high gain of 10 dB at 50 GHz and low minimum noise figure (NF_{min})below 2 dB at 60 GHz, showing the feasibility of flip-chip packaged $In_{0.7}Ga_{0.3}As$ MHEMT device for low noise applications at W-band.**

Keywords- $In_xGa_{1-x}As$-channel, HEMTs, Flip-chip

I. INTRODUCTION

With the deployment of millimeter-wave systems, the high gain, low noise and low power consumption characteristics are the main considerations for high frequency applications. In order to realize these systems, one of the most important components is the low noise amplifier (LNA) which can amplify the received signal and suppress the noise. Among all the possible device technologies, III-V compound semiconductor is the best candidate which delivers high gain and low noise at low power consumption levels due to the high electron mobility and saturation velocities. Specifically, indium-rich $In_xGa_{1-x}As$ channel high electron mobility transistors (HEMTs) have attracted more attentions due to its excellent electrical performances [1], [2].

In terms of practical implantation scenarios, packaging is the most critical issue to guarantee device performance because it should provide reliable transmission path for signal transmission without introducing too much parasitic effect to degrade device performance. Wire-bonding is usually adopted as interconnection in conventional packaging configurations which may cause significant degradations in performance at high frequencies. Thus, the use of flip-chip technology is more suitable for interconnection in millimeter-wave package because it provides smaller package size, good thermal management, short interconnects length and better mechanical reliability [3-7].

In this study, the in-house fabrication process of 80 nm $In_{0.7}Ga_{0.3}As$ MHEMT devices and Al_2O_3 substrate is demonstrated. The DC and RF performance of the fabricated $In_{0.7}Ga_{0.3}As$ MHEMT devices with flip-chip assembly were characterized up to 60 GHz. In addition, the noise characteristics were also measured ranging from 22 GHz to 60 GHz. Measurement results clarified the feasibility of the flip-chip packaged structure for millimeter-wave LNA applications.

II. FABRICATION AND FLIP-CHIP PACKAGE PROCESS

In this study, the in-house fabricated 80-nm $In_{0.7}Ga_{0.3}As$-channel MHEMT devices with Pt-buried gate was employed. The epitaxial layer was grown on 3-inch semi-insulating GaAs substrate by molecular beam epitaxy (MBE). The epitaxial structure is shown in Fig. 1. The indium-rich heavily-doped $In_{0.65}Ga_{0.36}As$ cap layer was used resulting in the enhancement of the tunneling current between source or drain ohmic contacts. As a result, a low ohmic contact resistance of 0.05 Ω·mm was achieved.

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n+ Cap	InGaAs, x = 0.65	30 nm, $2x10^{18}$
Etch stop	InP	4 nm
Barrier	InAlAs, x = 0.52	8 nm
δ-doping	Si	$5x10^{12}$
Spacer	InAlAs, x = 0.52	4 nm
Channel	InGaAs, x = 0.7	12 nm
Buffer	InAlAs, x = 0.52	100 nm
3 Inch S. I. GaAs Substrate		

Fig. 1 Epitaxial layer structure of the $In_{0.7}Ga_{0.3}As$ high electron mobility transistors (HEMTs).

The device fabrication closely follows our previous process flow [8]. T-shaped Pt/Ti/Pt/Au Schottky gate were fabricated by EB lithography and a standard lift-off technique. Following, a Pt-buried gate was performed to improve device performances. After finishing the device process, the wafer was thinned down to 100 μm and diced into discrete MHEMT dies. The image of the fabricated 80nm $In_{0.7}Ga_{0.3}As$ MHEMT device is shown in the Fig. 3 (a).

Fig.2 illustrates the in-house fabrication procedure of the flip-chip packaged Al_2O_3 substrate with electroplated Au micro bump transitions. For the demonstrated interconnect structure, the material of the substrate was Al_2O_3 due to good electrical properties, i.e. dielectric constant of 9.8 and tangent loss of 0.0006. Firstly, the seed layers of titanium (Ti) and gold (Au) metal (300 Å and 500 Å) were deposited on Al_2O_3 substrate by E-gun evaporator. The Ti metal layer was chosen to improve adhesion between Au metal layer and Al_2O_3 substrate. Then the thin photoresist was patterned to the following electroplating Au CPW transmission lines with the thickness of 3 μm. The characteristic impedance of the CPW transmission line with optimum dimensions was equal to 50 ohm. After electroplating the circuit, the thick photoresist from TOK Company was then patterned for the Au bump electroplating. The required bump height of micro Au bumps was achieved after optimization of the electroplating current density, temperature and time. Finally, the thick photoresist and seed layers were removed.

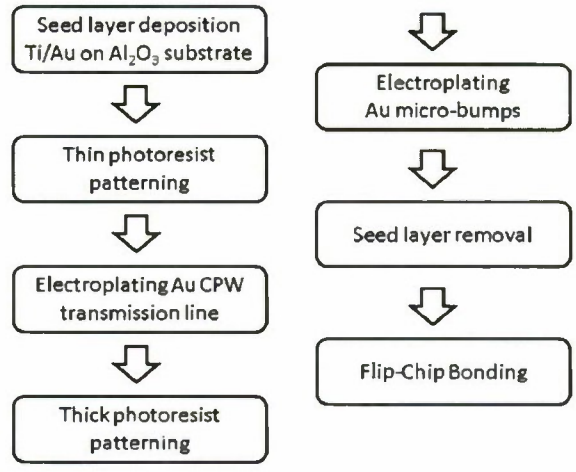

Fig. 2 In-house process flow of the alumina (Al_2O_3) substrate for flip-chip packaging structure

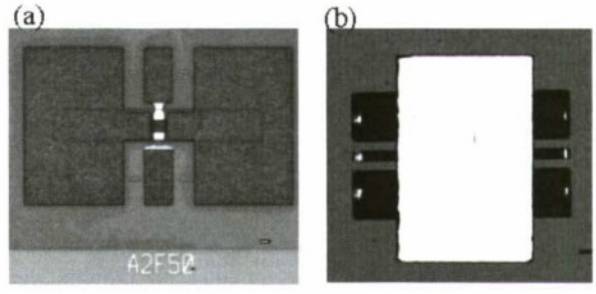

Fig. 3 Images of (a) 80nm gate $In_{0.7}Ga_{0.3}As$ MHEMT device, (b) flip-chip packaged $In_{0.7}Ga_{0.3}As$ MHEMT device on Al_2O_3 substrate.

Finally, the $In_{0.7}Ga_{0.3}As$ MHEMT devices and Al_2O_3 substrate were flip-chip assembled together by using Laurier Inc. M9 flip-chip bonder. The thermo-compression bonding process with optimized bonding conditions such as bonding force, time, and temperature was employed. The image of the flip-chip packaged 80-nm $In_{0.7}Ga_{0.3}As$ MHEMT on Al_2O_3 substrate is shown in Fig. 3 (b).

III. Results and Disscusion

Fig. 4 shows the characteristics of drain current (I_{DS}) versus drain voltage (V_{DS}) with various gate voltage (V_G) of the 80-nm $In_{0.7}Ga_{0.3}As$ MHEMT device after flip-chip assembly. A high drain current density of 425 mA/mm was observed at a V_{DS} of 1.5 V. The transconductance (gm) and the drain source current (I_{DS}) as a function of gate-source voltage

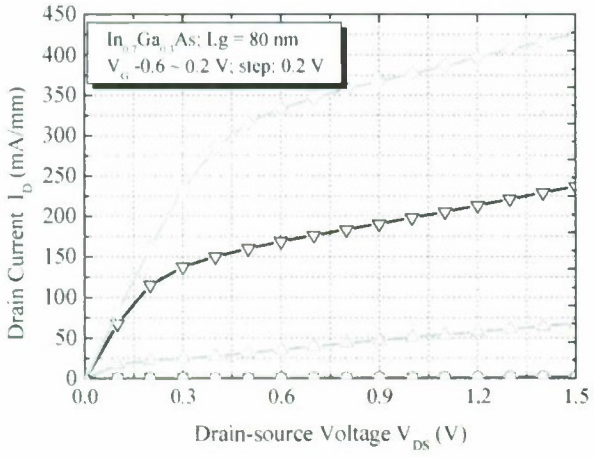

Fig. 4 Drain-source current (I_D) versus drain-source voltage (V_{DS}) curve with various gate voltage (V_G) of $In_{0.7}Ga_{0.3}As$ MHEMT device with flip-chip packaging

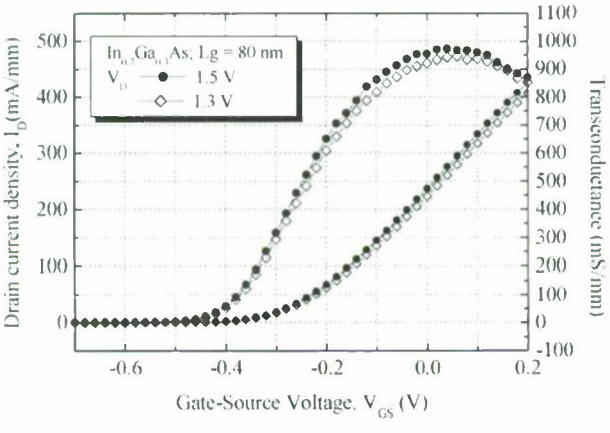

Fig. 5 Drain current density (I_D) and transconductance (gm) as a function of gate-source voltage (V_{GS}) of $In_{0.7}Ga_{0.3}As$ MHEMT device with flip-chip packaging.

(V_{GS}) with various V_{DS} are shown in Fig. 5. The maximum g_m peak of the devices at a V_{DS} of 1.5 V was 970 mS/mm. This high transconductance is due to the superior electron transport properties in the $In_{0.7}Ga_{0.3}As$ channel and low ohmic contact resistance. This MHEMT device can be well pinched off with a threshold voltage (V_T) of -0.45 V.

The RF characteristics of the flip-chip packaged $In_{0.7}Ga_{0.3}As$ MHEMT device were measured up to W-band frequencies by using on-wafer probing measurement system with the Agilent vector network analyzer 8510XF. The Short-Open-Load-Thru (SOLT) calibration was

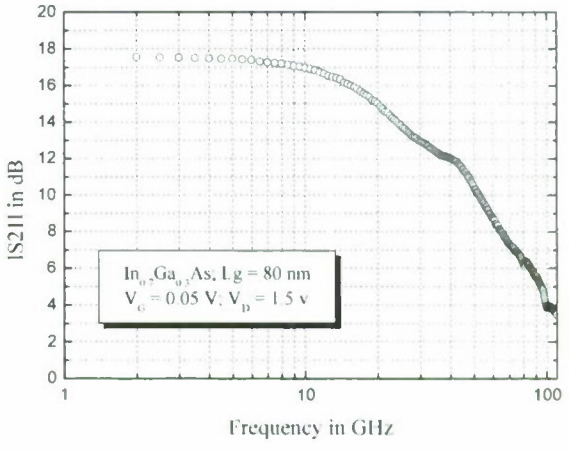

Fig. 6 Insertion gain (S21)) of $In_{0.7}Ga_{0.3}As$ MHEMT devices with flip-chip packaging.

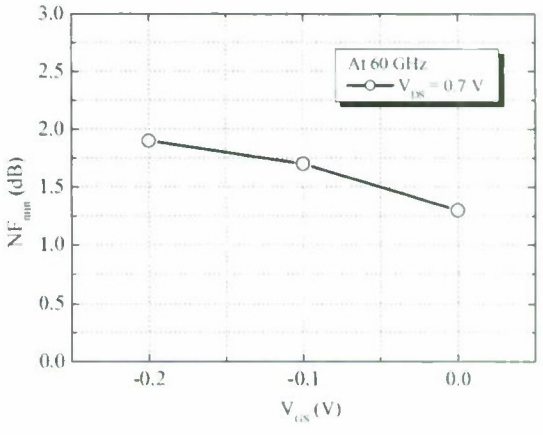

Fig. 7 The minimum noise figure (NF_{min}) of $In_{0.7}Ga_{0.3}As$ MHEMT devices with flip-chip packaging at 60 GHz.

used to calibrate the measurement system. Fig.6 shows the measured gain with 50 Ohm terminations both at input and output ports. It is clear that the device exhibited better than 10dB gain up to 50 GHz. This superior performance evidenced the very high quality of the interface between the chip and gold bumps which did not introduce additional loss even at very high frequencies.

The minimum noise figure (NF_{min}) of the flip-chip packaged $In_{0.7}Ga_{0.3}As$ MHEMT device was also characterized at 60 GHz, as shown in Fig.7. The NF_{min} was as low as 1.3 dB at V_D of 0.7 V and V_G of 0 V. Clearly, less than 2dB NF_{min} was achieved at all the biases. These superior

performances at 60 GHz clearly proved the feasibility of adopting flip-chip packaging technology for W-band low noise applications.

IV. CONCLUSION

In this study, a flip-chip packaging structure of 80 nm gate $In_{0.7}Ga_{0.3}As$ MHEMT device is successfully demonstrated on Al_2O_3 substrate. After flip-chip packaging, this structure exhibits high I_{DS} = 425 mA/mm, high g_m= 970 mS/mm at V_{DS}= 1.5 V, and high gain of 10 dB at 50 GHz. Besides, the NF_{min} is less than 2 dB at 60 GHz with different gate voltage. These state-of-the-art results exhibit the potential of InGaAs MHEMT with flip-chip package for W-band LNA applications.

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N+-InGaAs/InAlAs Recessed Gates for InAs/AlSb HFET Development

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Abstract

In this work, N+-InGaAs/InAlAs recessed gates for InAs/AlSb HFET development are presented. Highly doped N+-InGaAs cap layers are used to decrease the parasitic resistances in contact and access regions. As-grown modulation-doped epitaxy materials exhibit a Hall mobility of 14,200 cm^2/V s and a sheet density of 6.15 $\times 10^{12}$ cm^{-2}, while a mobility of 14,600 cm^2/V s and a sheet density of 5.61×10^{12} cm^{-2} are shown after removal of the N+-InGaAs cap. Benefiting the energy band lowering using the highly doped cap layers, a low contact resistance of 0.06 Ω-mm is achieved. DC performances of I_{DSS}=862mA/mm and $g_{m,peak}$=927mS/mm and RF performanees of f_T=24GHz and f_{max}=51GHz are demonstrated in a 2.1 μm-gate-length device. An f_T-L_g product is as high as 51 GH-μm.

Keywords-InAs, recessed gate, HFET

I. INTRODUCTION

InAs quantum wells with nearly lattice-matched AlSb barriers feature very high room-temperature electron mobility of 30,000 cm^2/V s at a sheet density of 1.5×10^{12} cm^{-2} and a large Γ-L valley separation of ~0.9 eV that enable very high peak velocity of 3.5×10^7 cm/s [1][2]. However, a drawback of the technology is the low breakdown voltage associated with the relatively narrow band-gap of the InAs channel layer. Added with staggered band lineup at InAs/AlSb heterojunctions, the generated holes from the breakdown cannot be confined in the channel and result in significant impacts on device performance. Typically, applied drain bias range is limited below 0.4V, which is roughly the effective energy bandgap of the InAs channel. The InAs HFETs are thus suitable for low-voltage and high-frequency applications. The use of double caps, which consist of heavily doped and intrinsic layers, for recessed-gate development is widely recognized as an effective approach for reducing source resistance in the device structures of conventional HFETs [3][4]. Utilizing an N+-cap layer at the device surface of n-channel HFETs, reduced parasitic resistances in both device contact and access regions can be achieved. Moreover, the recessed gate technology can help control the electric field between gate and drain for higher breakdown voltage and provide surface protection during device fabrication. A 200nm-gate-length n+-InAs/InAlAs recessed-gate HFET with f_t =162 GHz and f_{max} =137 GHz has been demonstrated [5]. This work studies a novel combination of N+-InGaAs and i-InAlAs double caps for developing the recessed-gate InAs/AlSb HFETs. Epitaxy growth, device fabrication and electric characterization are included.

II. GROWTH AND DEVICE FABRICATION

The InAs/AlSb HFET materials were grown by solid-source molecular beam epitaxy (MBE) on a semi-insulating (001) GaAs substrate. Growth was initiated with a 1.5μm-thick AlSb buffer layer which serves primarily to reduce the high density of threading dislocations to be below 10^8 cm^{-2}. Following a 0.3μm $Al_{0.7}Ga_{0.3}Sb$ mesa floor layer, the active layers of HFET devices were grown. The active layers consisted of a 10nm AlSb bottom barrier layer, a 13nm InAs channel layer, and an 11.3nm AlSb top barrier layer. A planar Te modulation doping sheet was inserted in the AlSb top barrier and 5 nm above the InAs channel layer. Finally, a 0.6nm GaSb, a 5nm InAlAs, and a 30nm N+-InGaAs layers were capped at epitaxy surface. Figure 1 shows the layer structure. The lattice constants of InAlAs and InGaAs layers were both lattice-matched to those of InP materials. Figure 2 shows the calculated energy band diagrams of two layer structures, one of which is with and another is without the N+-InGaAs cap. Assisted by the lowering of energy bands at device surface, the structure with the N+-InGaAs cap layer yields a higher carrier concentration in the channel than the one without the N+-InGaAs cap layer. Hall measurement

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revealed a mobility of 14,600 cm^2/V s and a sheet concentration of 5.61×10^{12} cm^{-2} after removal of the N^+-InGaAs cap layer.

N^+-InGaAs	300Å
InAlAs	50 Å
GaSb	6 Å
Te --------AlSb---------	110 Å
InAs	130 Å
AlSb	100 Å
$Al_{0.3}Ga_{0.7}Sb$	3000 Å
AlSb	15000 Å
S. I. GaAs substrate	

Fig. 1 Layer structure of the InAs/AlSb HFET

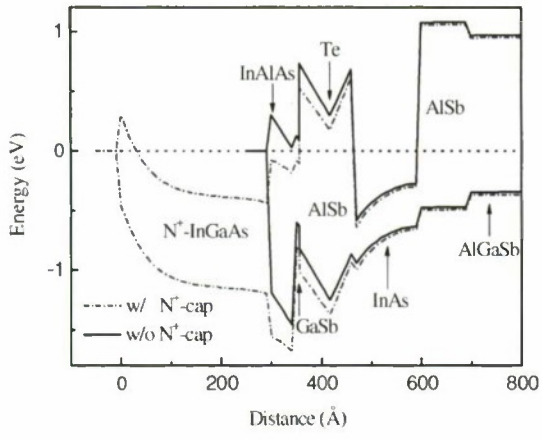

Fig. 2 Calculated energy band diagrams for the InAs/ AlSb HFETs w/ and w/o N^+-cap.

The HEFTs were fabricated using a conventional mesa process. First, Pd/Ti/Pt/Au ohmic contacts were formed using a 300℃ RTA annealing. After defining the mesa by a wet etch, Ti/Pt/Au recessed Schottky gates were fabricated. Citric acid was used for selectively removing the N^+-InGaAs and stopping in the InAlAs layer. Finally, Ti/Au probing pads were made. Figure 3 is the cross-sectional schematic of N^+-InGaAs/InAlAs recessed-gate HFETs. Figure 4 shows a study of ohmic contacts based on the two InAs/AlSb HFET structures of N^+-InGaAs/ InAlAs double caps and an InAlAs single cap. A lower contact resistance of 0.06 Ω-mm in the structure of the N^+-InGaAs/ InAlAs double caps than that of 0.1 Ω-mm in the structure of the InAlAs single cap was achieved, and primarily contributed to the use of the N^+-InGaAs cap layer, which lowered the energy barrier for the electrons in the contact regions.

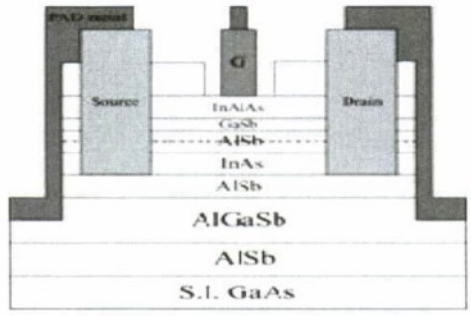

Fig. 3 Cross-sectional schematic of an N^+-InGaAs/InAlAs recessed-gate HFET.

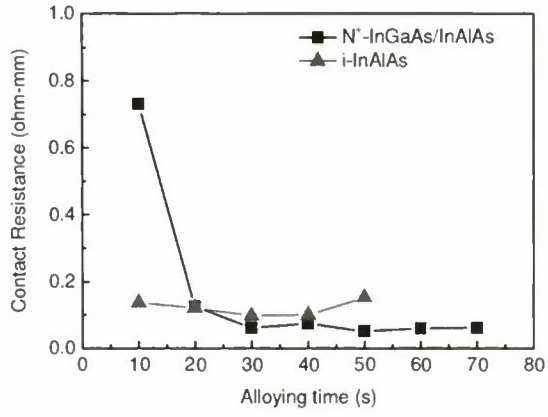

Fig. 4 Contact resistances as function of alloying time. Annealing temperature is 300 ℃.

III. RESULTS AND DISCUSSIONS

Figure 5 and 6 show the I-V and transfer characteristics of an N^+-InGaAs/InAlAs recessed-gate HFET with a gate length of 2.1 μm and a gate width of 50×2 μm, respectively. A high drain current of 863 mA/mm and a transconductance of 929 mS/mm at a drain voltage of 0.5 V are obtained. Threshold voltage is -1.8V at drain voltages below 0.3 V and shifts to more negative values at higher drain voltages. The shift of threshold voltages at high drain voltages is primarily due to the large kink currents generated by impact ionization effect. Figure 7 shows subthreshold gate and drain characteristics. An I_{on}/I_{off} ratio of 30 and a subthreshold slope of 440 mV/dec at a drain voltage of 0.5V are obtained. The consistency of gate and drain currents in deep subthreshold region indicates that the poor subthreshold behavior is primarily due to large gate leakages. Two possible leakage paths are suspected: one exists at the device surface between the N^+-InGaAs cap layer and the gate metals because of a small recess depth of 0.1 μ m [6]. The recess depth may not be enough to prevent a large conduction between the gate metals and the source/drain electrodes. Another leakage path may exist in the epiatxy materials between the channel layer and the gate

metals through the defects generated by a large mismatch between the caps and antimonide-based epitaxial layers (Fig. 8). Though the increased roughness which partly results from the mismatched cap layers are reduced by removing the N^+-InGaAs cap, many micro-cracks still exist at the InAlAs cap surface. The micro-cracks provide the potential paths for the gate leakage.

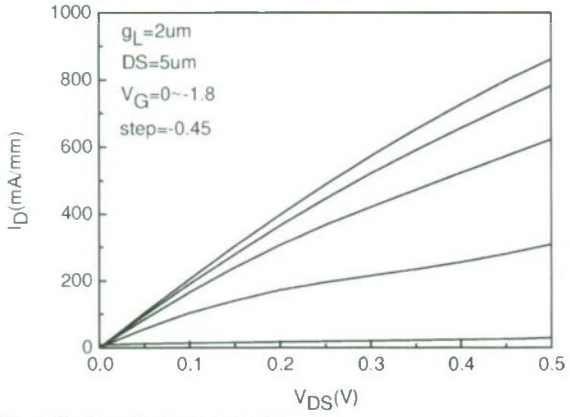

Fig. 5 Drain I-V characteristics

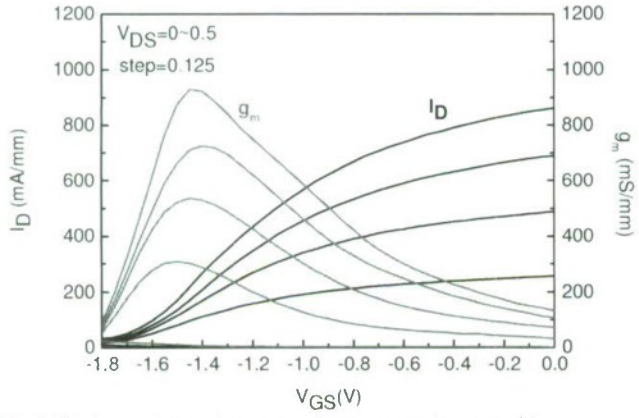

Fig. 6 Drain current and transconductance against gate bias.

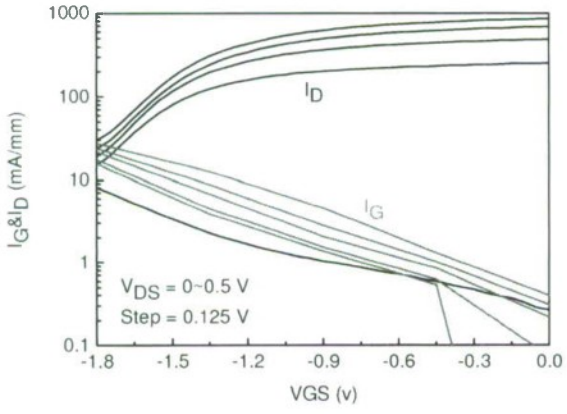

Fig. 7 Subthresbold gate and drain bebaviors as function of gate bias.

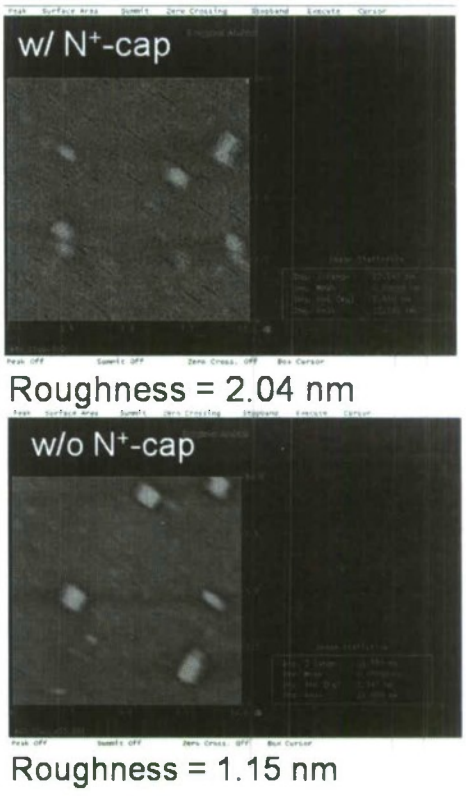

Fig. 8 AFM pictures for the epitaxies w/ and w/o an N^+-cap layer.

On-wafer S-parameter measurements from 50 MHz to 20.05 GHz yielded an f_T of 24.2 GHz and an f_{max} of 36.9 GHz at a drain voltage of 0.5 V and gate voltage of –1.5 V (Fig. 9). These values are obtained by extrapolating the short-circuit current gain (h_{21}) and the unilateral power gain (U) curves to 0 dB, respectively, using -20 dB/decade slopes. An f_T-Lg product as high as 51 GHz-μm was achieved. A gate length of 2.1 μm was determined by SEM (Fig. 10).

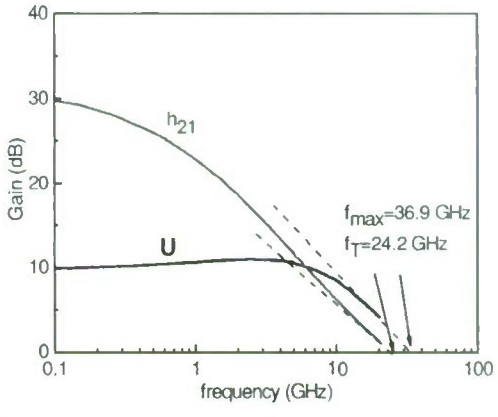

Fig. 9 Current and power gains as function of frequency

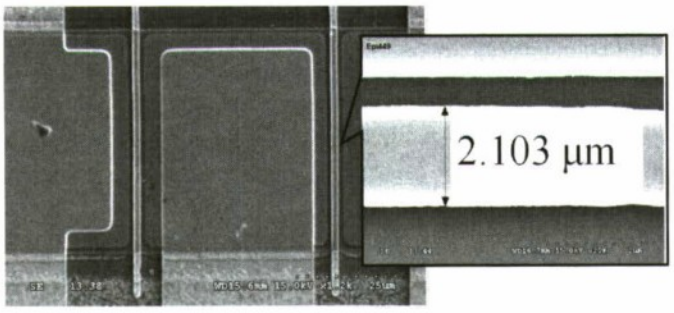

Fig. 10 Device SEM pictures.

IV. CONCLUSIONS

This work successfully demonstrated the InAs/AlSb HFETs with N^+-InGaAs/InAlAs recessed-gate structures. The N^+-InGaAs cap was used to decrease the parasitic resistances from contact and access areas. The contact resistance was reduced from 0.1 Ω-mm to 0.06 Ω-mm in the TLM measurements. An f_T-Lg product as high as 51 GHz-μm was achieved. Small gate recess depths and micro-cracks at the epitaxy surface were strongly suspected as the high gate leakages in the current devices. To optimize the recess depths and to improve epitaxy quality will be our future works.

ACKNOWLEDGMENT

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Isolated-gate InAs/AlSb HEMTs: A Monte Carlo study

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Abstract

In this work we present a Monte Carlo study of the influence of the presence of a native oxide which isolates the gate in InAs/AlSb high electron mobility transistors (HEMTs) on their dc and ac performance. A good agreement between simulations and experimental results of *I-V* curves and small signal equivalent circuit parameters has been found for low V_{DS}, where impact ionization is not of importance. The comparison between intrinsic MC simulation results for isolated-gate and Schottky-gate HEMTs reveals a strong influence of the native oxide on the dynamic behavior of the devices, mainly on C_{gs}, g_m and f_c.

I. Introduction

InAs/AlSb HEMTs, due to the huge mobility of InAs and an improved electron confinement in the channel (as a result of the large energy barrier imposed by the AlSb layers), have become an interesting option in the demanding market of high frequency, low-noise and low-power applications (1, 2). However, two main problems have been found in the development of the Sb-based HEMT technology: the very fast oxidation of AlSb, and the excessive gate leakage current. Technological developments such as the use of an isolated gate by means of a native oxide, which naturally appears after the recess etch process (3), have allowed to decrease such undesired leakage current. In this work a comparative study of conventional Schottky-gate (SG) and isolated-gate (IG) Sb HEMTs is performed by means of Monte Carlo (MC) simulations and experimental data.

Because of the very high mobility of InAs, electron transport can easily turn into ballistic or at least quasiballistic in the channel, so that the MC method becomes the most adequate simulation technique to reproduce not only static results but also the dynamic behaviour of these devices. MC results provide useful information for the optimization of the transistors, offering the possibility of studying the differences between SG and IG Sb-HEMTs from a physical point of view.

II. Monte Carlo Model

In order to compare the behaviour of SG and IG Sb-HEMTs we have used a semi-classical ensemble MC simulator self-consistently coupled with a 2D Poisson solver (4, 5), adequately modified to properly model such narrow band-gap HEMTs (6). We will focus on biases lower than 0.3 V, where the dynamic behaviour of the transistors is expected to be optimal. Therefore, impact ionization mechanisms are not considered in the simulations; however, as will be observed in the experimental measurements, impact ionization becomes very important for drain bias above V_{DS}=0.3 V.

The simulated InAs/AlSb HEMTs have the same topology as the fabricated ones (3), using the following epitaxial layer: an AlSb buffer of 800 nm followed by a InAs channel of 15 nm and a 15 nm thick AlSb barrier, a 4 nm protection layer of $In_{0.5}Al_{0.5}As$, and a 5 nm highly Si doped (N_D=5x10^{18} cm^{-3}) InAs layer on top. Electrons are provided by means of a δ-doping of δ=4.5x10^{12} cm^{-2}, 5 nm far from the channel. The recess etch stops at a depth of 9 nm (the top of the AlSb Schottky layer), and extends 50 nm at each side of the 225 nm gate.

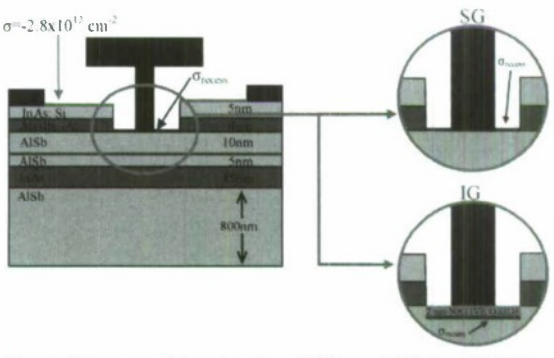

Fig. 1 Scheme of the simulated SG- and IG-Sb-HEMTs.

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After the recess etch process, no oxide removing has been performed before depositing the gate contact, so that a native oxide is presumably formed between the semiconductor and the gate metal. In order to study the influence of the native oxide under the gate two different cases have been simulated (Fig. 1). In the case of the SG-HEMT the gate contact is directly placed onto the AlSb Schottky layer, while for the IG-HEMT a thin oxide layer has been considered to be formed within the AlSb. The oxidation process of AlSb is very complex (7), thus being difficult to precisely know how deep the oxidation is and which is the exact composition of the resulting native oxide. We have checked several values for the thickness and dielectric constant of the oxide, finding a good agreement with experimental results in the case of a 2 nm thick oxide with a relative dielectric constant of 2.2 (corresponding to aluminium hydroxide).

In order to correctly reproduce with the MC calculations the experimental sheet electron density in the channel, n_S=2.1x10^{12} cm^{-2}, a surface charge density is placed at the top of the cap layer with a value of σ = -2.8x10^{12} cm^{-2}. At the recess interface the surface charge can be different (8), and we have initially used a value of σ_{recess}= -1.2x10^{12} cm^{-2}.

III. Results

A. Static results

DC MC results for IG-HEMTs are compared with the experimental measurements performed in real HEMTs in Fig. 2. The intrinsic values obtained from the simulations have been modified in order to incorporate the influence of the source and drain contact resistances (1.3x10^{-4} Ω/cm and 3.8x10^{-4} Ω/cm, respectively, in good agreement with the experimental values of the contact access resistances). As shown in the figure, for low V_{DS} (up to 0.2-0.3 V), when impact ionization mechanisms are not of importance, the agreement between the experimental and MC results is quite good. For higher V_{DS} a strong kink appears in the experimental output I-V curves, Fig. 2(a), jointly with a threshold voltage shift, Fig. 2(b), due to the generation of electron-hole pairs (not reproduced by MC simulations since impact ionization is not considered). These results confirm the importance of impact ionization in Sb-HEMTs due to the very small band gap of InAs.

To study the influence of the native oxide in the device behaviour we have compared the intrinsic results obtained on the simulations of the IG-HEMTs with those of a traditional SG device. Fig. 3 shows the intrinsic MC results for g_m and I_D vs. V_{GS} at V_{DS}=0.2 V for the SG- and IG-HEMTs. In the case of the SG-HEMT, the Schottky barrier height has not been included in the simulations (that involves a positive shift of the V_{GS} values). In order to reproduce the experimental results for the threshold voltage obtained in the real isolated-gate HEMTs, an unphysical negative value of the Schottky barrier height should be added to the SG simulations. This result confirms that the oxide layer is actually present in between the gate and the semiconductor. On the other hand in the IG-HEMT

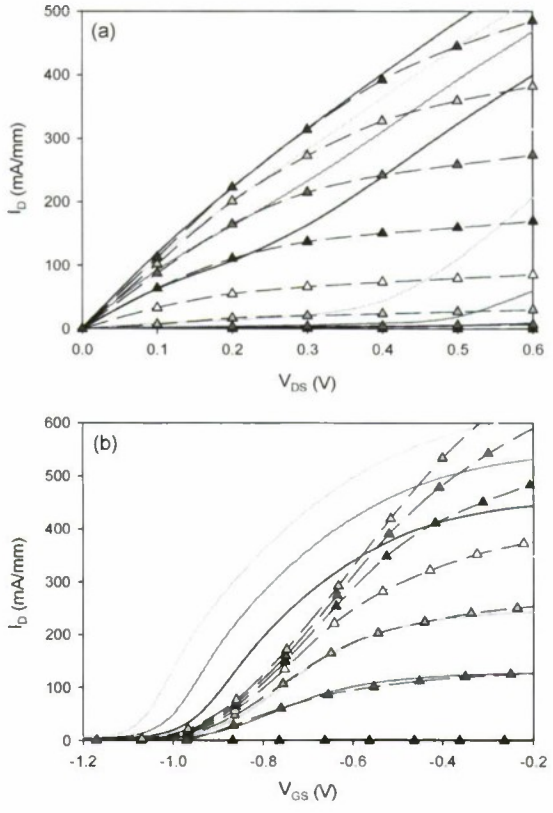

Fig. 2: Comparison of the experimental (coloured solid lines) and MC (triangles, dashed black lines) characteristics of the IG-HEMT. (a) I_D-V_{DS} from V_{GS}=-0.45 V to -1.15 V, step 0.1 V and (b) I_D-V_{GS} from V_{DS}=0.0 V to 0.6 V, step 0.1 V.

simulations, the possible V_{GS} shift (positive or negative) associated with the presence of charges in the oxide has not been considered either. Fig. 3 shows that, as expected, due to a

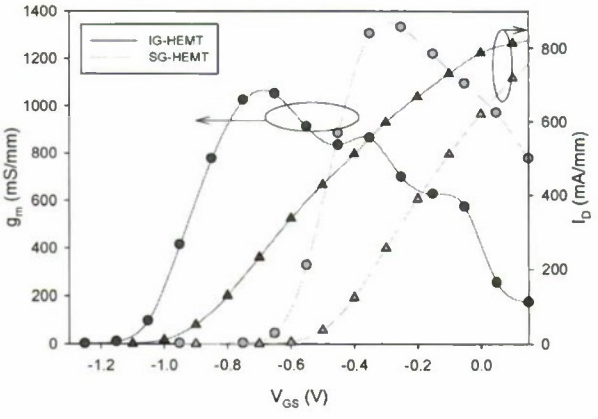

Fig. 3: Intrinsic g_m (circles) and I_D (triangles) as a function of V_{GS} for the SG- (dashed green lines) and IG-HEMT (solid red lines) calculated with MC simulations for V_{DS}=0.2V.

lower gate control, g_m decreases when the native oxide is considered, and the threshold voltage is shifted to more negative values of V_{GS}.

B. Dynamic results

The intrinsic small-signal equivalent circuit parameters have been obtained with MC simulations through the calculation of the admittance parameters of the transistors, extracted by Fourier transform of the currents response to voltage steps applied to the gate and drain electrodes (9). Three extrinsic capacitances have been added to reproduce the effects associated with the layout of the devices not taken into account in the 2D intrinsic simulation (C_{ds}^{ext}=2.17 fF/mm, C_{gd}^{ext}=1.36 fF/mm, C_{gs}^{ext}=1.04 fF/mm) (9). These values have been obtained by fitting the experimental data at zero current, where only the effect of the geometric capacitances remains, and they are independent of the bias. The intrinsic equivalent circuit obtained from the MC simulation including the C^{ext} corresponds to the intrinsic experimental small-signal equivalent circuit from the point of view of experimental measurements.

The main small-signal equivalent circuit parameters extracted from MC simulations for the IG- and SG-HEMTs are compared with the experimental results for V_{DS}=0.2 V in Fig. 4. A reasonably good agreement is found for C_{gs} and C_{gd} [Figs. 4 (a) and (b)] for both the simulated IG-and SG-HEMTs. However, as expected, the presence of the oxide slightly decreases the values of the gate capacitances of the IG- with respect to the SG-HEMT. In the case of C_{ds}, probably because of the existence of some holes in the buffer (generated by impact ionization even for such small drain bias), a disagreement between experimental data and MC simulations is found, Fig. 4 (c). This also leads to an important frequency dispersion in the measurements of C_{ds} and g_d, the two dynamic parameters that are more affected by the behaviour of the buffer. As a consequence, a significant disagreement between measurements and simulations is found for the case of g_d, Fig. 5(b), independently of the presence or not of the gate oxide. Moreover, Fig. 5(a) shows a strong decrease in g_m associated with the presence of the oxide. Due to the influence of g_d in the

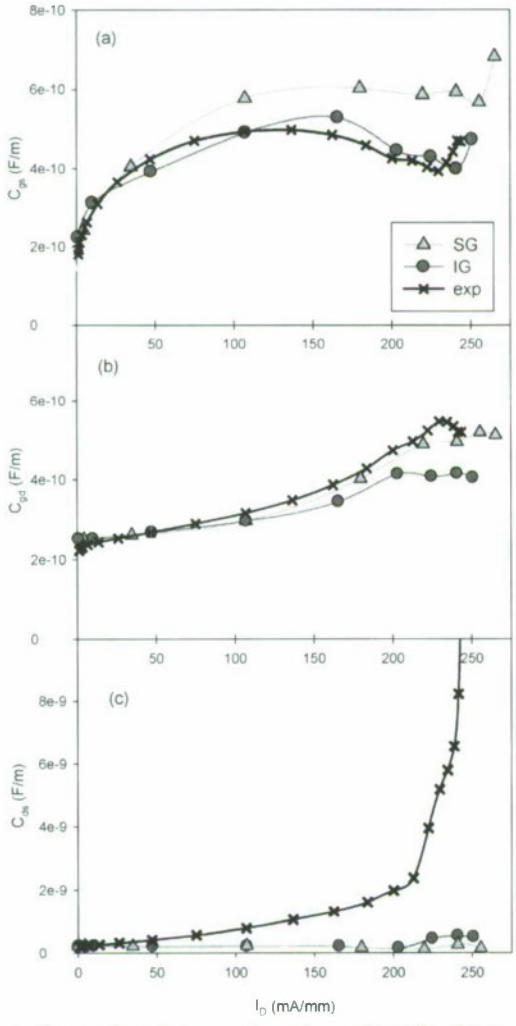

Fig. 4: Comparison between the values of (a) C_{gs}, (b) C_{gd}, and (c) C_{ds}, measured in the fabricated IG-HEMT (black crosses) and obtained by MC simulations in the SG- (red circles) and IG-HEMTs (green triangles) as a function of I_D for V_{DS}=0.2V.

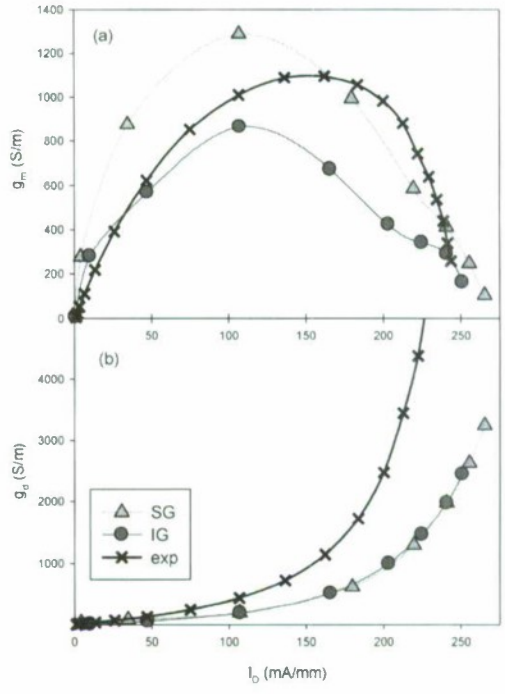

Fig. 5: (a) g_m, and (b) g_d measured in the fabricated IG-HEMT (black crosses) as compared with the values obtained from the simulated SG- (red circles) and IG-HEMTs (green triangles) as a function of I_D for V_{DS}=0.2V.

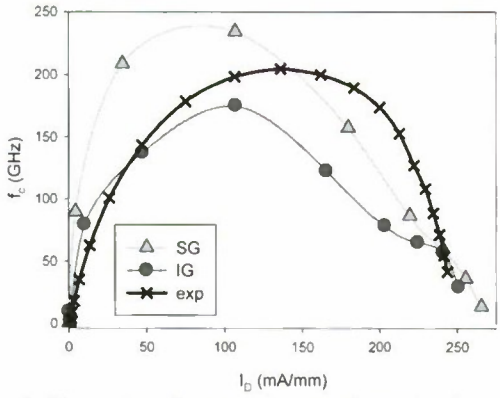

Fig. 6: Comparison between the experimental values of f_c in the IG-HEMT (black crosses) and the simulated ones in the SG- (red circles) and IG-HEMTs (green triangles) as a function of I_D for V_{DS}=0.2V.

relation between intrinsic and extrinsic g_m:

$$g_m^{extr} = \frac{g_m^{intr}}{(1+g_m^{intr}R_S)\left[1+g_d^{intr}(R_S+R_d)\right]}, \qquad (1)$$

the observed disagreement between MC and measured g_d (Fig. 5(b)), leads also to differences in the values obtained for the intrinsic g_m, Fig. 5(a) [even if the extrinsic g_m is well reproduced, Fig. 2(b)].

The values of the intrinsic cut off frequency, f_c, calculated as $g_m/2\pi(C_{gs}+C_{gd})$, are shown in Fig. 6. A reasonable agreement with the experimental results has been achieved for the IG-HEMT for low drain current, while for higher values of I_D the disagreement with experimental results is due to the discrepancies in the dynamic g_m explained before. Interestingly, the presence of the native oxide leads to a strong decrease of f_c, thus reducing the benefits of the isolated-gate technology.

IV. Conclusions

Dc behavior and small signal circuit for InAs/AlSb isolated-gate HEMTs have been studied by means of MC simulations, and compared with experimental results. A reasonable agreement has been achieved in both static and dynamic behavior. Comparing intrinsic IG and SG simulation results, with and without oxide under the gate respectivily, a decrease in g_m, C_{gs} and f_c has been observed because of the presence of the oxide.

Acknowledgement

This work has been partially supported by the European Commission through the ROOTHz Project ICT-2009-243845 and the MC2ACCESS Project, by the Dirección General de Investigación (MEC) and FEDER through Project TEC2007-61259/MIC and the Acción Integrada HF2007-0014, by the Consejería de Educación, Junta de Castilla y León through Projects SA019A08 and GR270 and by the Swedish Research Council (VR).

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TCAD optimization of field-plated InAlAs-InGaAs HEMTs

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High-voltage InGaAs-InAlAs HEMTs featuring optimized field-plate structures are being developed. A TCAD approach has been adopted for their design. Two-dimensional device simulations have preliminarily been calibrated by comparison with DC and RF measurements from the baseline InP HEMT technology into which the field plate is being incorporated. Simulations have then been used to design field-plate structures with optimal length and passivation thickness.

I. Introduction

InAlAs-InGaAs HEMTs have demonstrated the best high-frequency and low-noise performance of any transistor technology to date. This comes however at the cost of a fundamental drawback, i.e. the low breakdown voltage resulting from the small critical electric field of the InGaAs channel. On the other hand, high-voltage operation is the most desirable solution for achieving high-power-density, high-efficiency power amplifiers (PAs). High-voltage capability is advantageous also for low-noise amplifiers (LNA), enabling more robust receivers with minimal protection circuitry. In order to achieve high-voltage operation, Field Plate (FP) structures can be adopted. The FP has recently been developed and used with success in both GaAs and GaN HEMT technologies [1-4]. It consists of an extension of the gate electrode on top of a dielectric or lightly-doped semiconductor layer towards the drain contact. The FP effectively reduces the magnitude of the electric field at the drain side of the gate edge. The resulting improvement in maximum operating voltage must however be traded off with the decrease in RF performance associated with the additional gate-drain capacitance introduced by the FP.

In this paper, we report on a work aimed at developing high-voltage InGaAs-InAlAs HEMTs featuring optimized FP structures. 2D numerical device simulations have preliminarily been compared with DC and RF measurements from non-FP devices fabricated with the baseline InP HEMT technology into which the field plate is being incorporated. Simulations have then been used to design FP structures with optimal geometrical parameters.

II. Simulation of baseline HEMTs

The baseline InP-HEMT technology into which the FP is being incorporated is described elsewhere [5,6]. Two-dimensional (2D) device simulations have been carried out with the program Dessis8.0 (Synopsys Inc.) by adopting the hydrodynamic transport model. A sketch of the simulation domain is shown in Fig. 1. The simulator has preliminarily been calibrated by comparison with measurements from non-FP HEMTs. To this regard, Fig. 2 shows experimental and simulated drain-current (I_D) vs gate-source-voltage (V_{GS}) characteristics of a non-FP HEMT. As can be noted, a good agreement between simulated and measured characteristics has been achieved from pinch-off up to $V_{GS}\approx$-0.2 V. For higher V_{GS} values, simulations slightly overestimate I_D. Possible reasons for this discrepancy are channel mobility degradation at high 2DEG densities and self-heating effects (both neglected in the simulations).

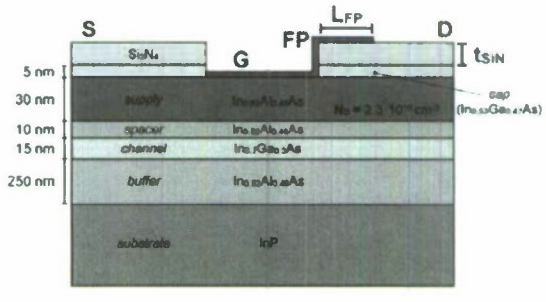

Fig. 1. Schematic cross section of devices under study. Gate length is 1 μm. Gate-source and gate-drain spacings are 2 μm.

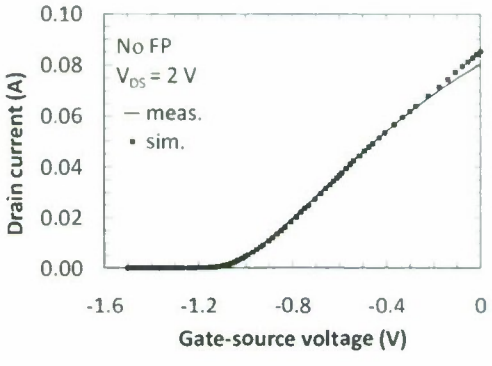

Fig. 2. Experimental (line) and simulated (symbols) drain-current vs gate-source-voltage characteristics for a HEMT without FP. Gate width (W_G) is 300 μm.

Experimental off-state breakdown characteristics for several non-FP HEMTs of same gate width are plotted in Fig. 3, while the corresponding simulated curve is included in Figs.

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4 and 5. To simulate breakdown, both channel impact ionization and gate electron injection (field emission) have been accounted for. Impact-ionization coefficients have been set in agreement with literature [7], whereas parameters of the gate tunneling model have been adjusted to obtain an off-state breakdown voltage in the 14-15 V range.

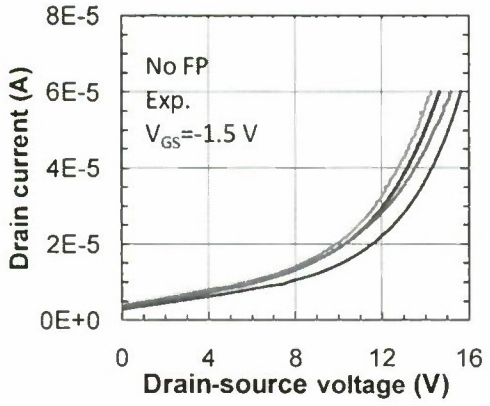

Fig. 3. Experimental off-state breakdown characteristics for HEMTs without FP. Gate width (W_G) is 300 μm.

III. Field-plate design

The calibrated simulator has been used to design field plates with optimal length (L_{FP}, see Fig. 1) and passivation thickness (t_{SiN}, see Fig. 1). Figures 4 and 5 shows simulated off-state breakdown characteristics of FP HEMTs for different values of t_{SiN} and L_{FP}, respectively. As can be noted, a maximum off-state drain-source breakdown voltage of about 24 V is predicted for a FP structure having L_{FP}=0.7 μm and t_{SiN}= 100 nm, with a 60% improvement over the non-FP device value. The effect of the FP is clearly illustrated by Fig. 6, showing the longitudinal electric field profile along the device channel for the non-FP device and for FP devices having different t_{SiN} (and same L_{FP}). The electric-field peak under the drain-end of the gate (located at x=3 μm) is reduced while a second electric-field peak is created under the FP edge (x=3.7 μm). Maximum breakdown voltage is achieved by field plates making these two peaks equal (100 nm<t_{SiN}<200 nm).

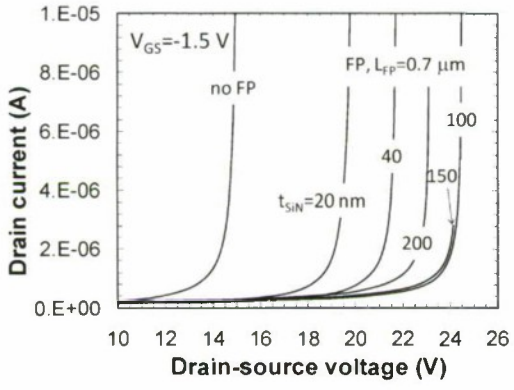

Fig. 4. Simulated off-state breakdown characteristics of FP HEMTs having different passivation thicknesses (t_{SiN}) and same FP length (L_{FP}= 0.7 μm). The curve for the HEMT without FP is included as a reference. Gate width (W_G) is 300 μm.

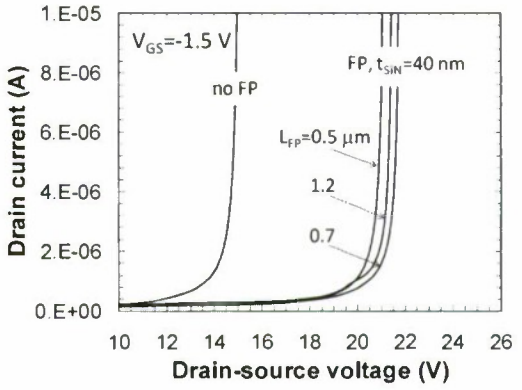

Fig. 5. Simulated off-state breakdown characteristics of FP HEMTs having different FP lengths (L_{FP}) and same passivation thickness (t_{SiN}= 40 nm). The curve for the HEMT without FP is included as a reference. Gate width (W_G) is 300 μm.

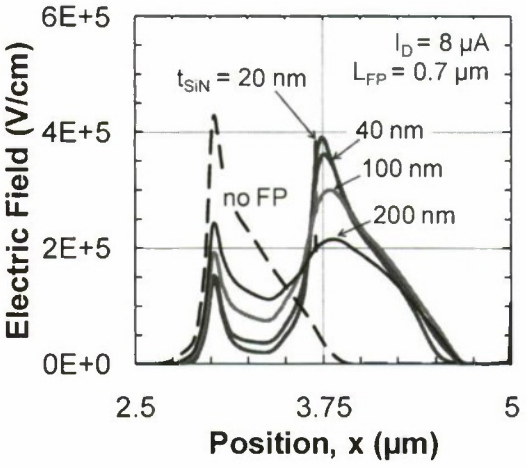

Fig. 6. Electric-field profiles along the device channel for different passivation thicknesses (t_{SiN}) and same FP length (L_{FP}= 0.7 μm). The curve for the HEMT without FP is included as a reference.

The price to pay to obtain high-voltage-operation capability is the extra gate-drain capacitance associated with the FP, leading to reduced f_T and f_{max}. This is illustrated by Figs. 7 and 8, showing the simulated unilateral power gain (G_u) as a function of frequency at a V_{DS} of 2 V and a V_{GS} of -0.8 V for FP HEMTs having different passivation thicknesses (t_{SiN}) and a FP length (L_{FP}) of 0.7 μm and 0.5 μm, respectively. G_u is obtained by solving the linearized version of the transport equations (small-signal, AC analysis). A lumped gate resistance was included in the simulations. Its value was set to 1.5 Ω, in agreement with RF measurements. Experimental and simulated curves for the HEMT without FP are included as a reference in both Figs. 7 and 8. For L_{FP}=0.7 μm and t_{SiN}=100 nm (achieving the highest breakdown voltage in Fig. 4), the decrease in f_{max} induced by the FP introduction is predicted to be of a factor of ≈2 (with respect to the non-FP device). As shown in Fig. 8, f_{max} worsening can be reduced to less than 35% by adopting sub-optimal FP parameters like t_{SiN}=200 nm and L_{FP}= 0.5 μm.

It is however important to note that, at higher V_{DS}, the detrimental effect of the FP on RF device performance is

expected to be strongly attenuated as a result of the reduced impact of the gate-drain capacitance. This is confirmed by our simulations, indicating that, at a V_{DS} of 9 V, f_{max} should show a negligible dependence on FP parameters within the assumed variability range, see Fig. 9.

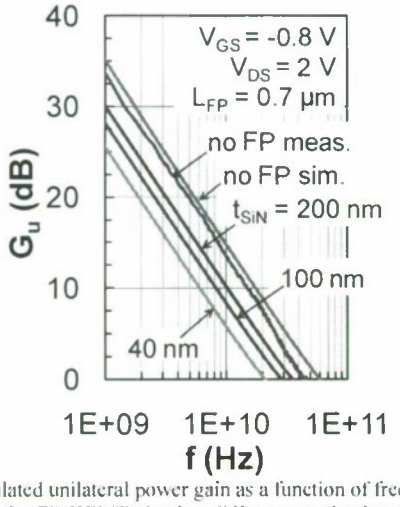

Fig. 7. Simulated unilateral power gain as a function of frequency at a V_{DS} of 2 V for FP HEMTs having different passivation thicknesses (t_{SiN}) and a FP length (L_{FP}) of 0.7 µm. Experimental and simulated curves for the HEMT without FP are included for reference.

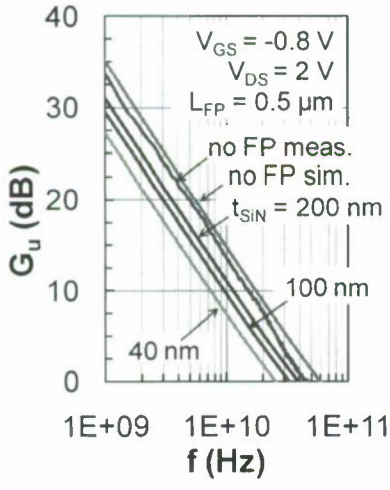

Fig. 8. Simulated unilateral power gain as a function of frequency at a V_{DS} of 2 V for FP HEMTs having different passivation thicknesses (t_{SiN}) and a FP length (L_{FP}) of 0.5 µm. Experimental and simulated curves for the HEMT without FP are included for reference.

IV. Conclusions

High-voltage InGaAs-InAlAs HEMTs featuring optimized field-plate structures have been designed by means of 2D hydrodynamic device simulations and are currently being fabricated. Device simulations have preliminarily been calibrated by comparison with DC and RF measurements from the baseline InP HEMT technology into which the field plate is being incorporated. Simulations have then been used to design field-plate structures with optimal length and passivation thickness.

The additional degree of freedom in the HEMT design made available by the field plate can potentially make it feasible: (i) high voltage, high efficiency PAs at millimeter-wave band, (ii) robust LNAs with simplified protection circuitry, (iii) integrated RF transceiver, including (onto the same chip) optimized devices for low-noise receivers and high-power devices for the transmitter PA.

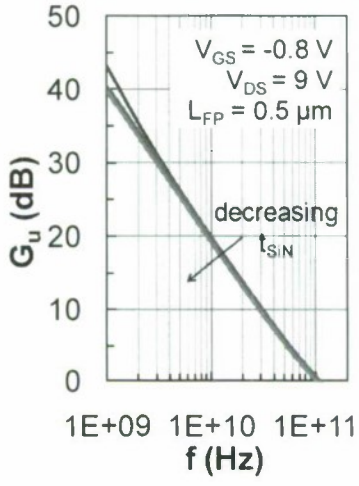

Fig. 9. Simulated unilateral power gain as a function of frequency at a V_{DS} of 9 V for FP HEMTs having different passivation thicknesses (t_{SiN}) and a FP length (L_{FP}) of 0.5 µm.

Acknowledgment

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An Optoelectronic Mixer Based on Composite Transparent Gate InAlAs/InGaAs Metamorphic HEMT

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Abstract—In this work, we have fabricated the first transparent gate using sputtered ITO/Au/ITO composite films InAlAs/InGaAs metamorphic HEMT (CTG-MHEMT) on GaAs substrate. The CTG-MHEMT has been demonstrated to increase front side optical coupling efficiency as an optoelectronic mixer. By optimizing the bias condition, the optoelectronic mixing efficiency can be enhanced. The photodetection mechanism of CTG-MHEMT is clarified by investigating the internal photovoltaic gain (G_{pv}) and photoconductance gain (G_{pc}). For comparison of the optical characteristics, the transparent gate MHEMT (TG-MHEMT) has been fabricated. The CTG-MHEMT as an optoelectronic mixer is a promising candidate that can simplify the base station architecture in fiber-optic microwave transmission systems.

Keywords: *Mixer, photovoltaic effect, photodetector, phototransistor, metamorphic high electron mobility transistor, responsivity, indium tin oxide*

Introduction

High internal gain and the possibility of simultaneously performing photodetection and microwave signal processing is quite attractive for such applications as radio-over-fiber (ROF) systems.[1][2][3] The optical response of HEMT due to the photovoltaic effect was demonstrated as predominant at low frequencies. To obtain increase internal photodetection gain, the drain-to-source spacing of a HEMT was decreased to reduce parasitic resistance. Additionally, the 3000-4000 Å-thick metal gate reflects the incident illumination signal simultaneously. Moreover, the depletion region beneath gate terminals is a highly efficient photovoltaic region due to its high electron field. Therefore, the photodetection efficiency of the HEMT channel was limited by the small optical absorbed region. Thus, a transparent gate for a phototransistor was developed and investigated to increase the size of the optical absorbed region and to enhance optical responsivity.[4] In this work, we fabricated composite transparent gate metamorphic HEMT (CTG-MHEMT) using high-conductivity ITO/Au/ITO to improve the front-illuminated light coupling efficiency. For comparison of the optical characteristics, the transparent gate MHEMT (TG-MHEMT) has been fabricated. The optical response of the CTG and TG -MHEMT with a 1.31μm DFB laser was measured and investigated experimentally and theoretically.

Experimental

Figure 1 presents the cross-sectional photograph of the CTG-MHEMT and TG-MHEMT structure grown on GaAs substrate. The grown wafers consisted of a 1-μm thick $In_xAl_{1-x}As$ metamorphic graded buffer layer with an indium content grading of x = 0 - 40 %. Two two- dimensional electron gas channels were formed in this $In_{0.4}Ga_{0.6}As$ quantum well and electrons were transferred from the upper and lower silicon δ-doped layers through the undoped $In_{0.4}Al_{0.6}As$ spacer layers. Then the 150Å $In_{0.4}Al_{0.6}As$ schottky layer sits above the upper Si δ-doped layer to increase the Schottky barrier height, and a 100Å undoped $In_{0.52}Ga_{0.48}As$ cap layer was grown to enhance ohmic contact resistivity. The designed structure had a sheet-charge density of 3.5×10^{12} cm^{-2} and a Hall mobility of 8500 cm^2/V-sec at 300 K after the undoped $In_{0.52}Ga_{0.48}As$ cap layer was removed. For device fabrication, ohmic contacts of Ni/Ge/Au metals were deposited by thermal evaporation and patterned using a conventional lift-off procedure. A chemical etching isolation technology was utilized for mesa isolation. The drain-to-source spacing was designed at 3 μm to minimize device series resistances. Following the highly selectivity chemical gate recess process, the $2\times50\mu m^2$ dimension sputtered ITO/Au/ITO composite transparent gate and traditional ITO gate was deposited and lifted off. Finally, the CTG-MHEMT was annealed at 350°C in a N_2-rich chamber for 2 minutes to obtain a low-resistivity composite transparent gate. Table I summarizes dc and rf performance of CTG- and TG-MHEMTs. The reversed gate-to-drain breakdown voltages (V_{BR}) and gate turn-on voltage (V_{ON}), are both defined by a 1 mA/mm of gate current. For CTG-MHEMT, the maximum transconductance was 400mS/ mm at V_{GS} = -0.05V and V_{DS}= 2V. The current gain cut-off frequency (f_T) and the power gain cut-off frequency (f_{max}) extracted from S-parameter measurement were 17GHz and 18.2GHz, respectively. For TG-MHEMT, the maximum transconductance was 530mS/ mm at V_{GS} = -0.3V and V_{DS}= 2V, and f_T was 17.6GHz. However, the f_{max} was only 14.6GHz. By inserting a thin Au layer into ITO transparent gate and optimizing the annealing condition, we successfully improve the f_{max} up to 4GHz range. To further investigate slight

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Table 1. Summary of CTG- and TG-MHEMTs characteristics.

Stacks	$I_{DS,max}$ *(mA)*	Gm_{max} *(mS)*	V_{TH} *(V)*	V_{ON} *(V)*	V_{BR} *(V)*	f_T *(GHz)*	f_{max} *(GHz)*	R_g *(Ω)*
CTG	45	39.75	-0.5	1.6	-10.7	17	18.2	190.26
TG	55	53	-0.75	1.7	-11.5	17.6	14.6	370

improvement in ITO/Au/ITO film resistivity increasing its f_{max}, we extracted the small signal model elements for both devices. For the component extraction of the small-signal equivalent circuit model, as well known, the parameters can be extracted by the Yang-Long method and cold-FET method. Through these two methods, we can obtain R_g for CTG- and TG-MHEMT. The extracted R_g of CTG-MHEMT is 190.26Ω, and this value of TG-MHEMT is 370Ω. The large improvement in gate resistance is the reason for increasing f_{max} which is beneficial for improving the output power of optical mixing signals.

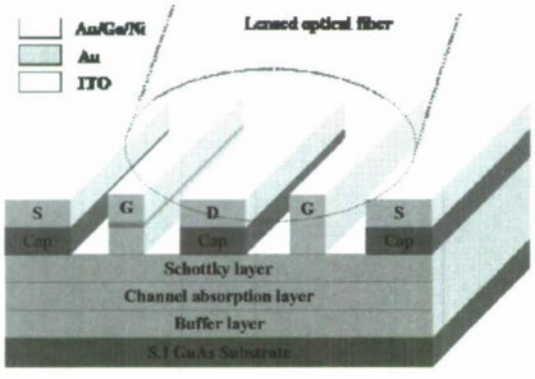


Fig. 1. The cross-sectional structure of fabricated CTG and TG-MHEMTs.

Results and disscusion

The CTG- and TG-MHEMTs were characterized by HP4142B (semiconductor parameter analyzer) and a 1.3μm wavelength DFB laser diode for optical measurements. The laser-beam illumination spot has a diameter of 25 μm as determined by the single mode lens optical fiber and projected on the two gate fingers. Figure 2(a) shows the measured I_{DS}-V_{GS} curves of the CTG- and TG-MHEMTs with various incident optical powers. The solid lines represent drain current in the dark and the dash lines represent drain current under illumination. Obviously, the I_{DS} increased with the intensity of the incident optical powers. Figure 2(b) compares the I_{DS} variation of CTG- and TG-MHEMTs at various V_{GS} bias points. The I_{DS} enhancement with 9dBm optical power illumination is conspicuous compared with that in darkness environment. Due to a better transmittance of the gate region, the TG-MHEMT exhibited a better optical response than that in CTG-MHEMT. The threshold voltages of the CTG- and TG-MHEMTs were -0.5V and -0.75V, respectively; and these values shifted to -0.61V and -0.99V with a 9dBm optical power illumination.

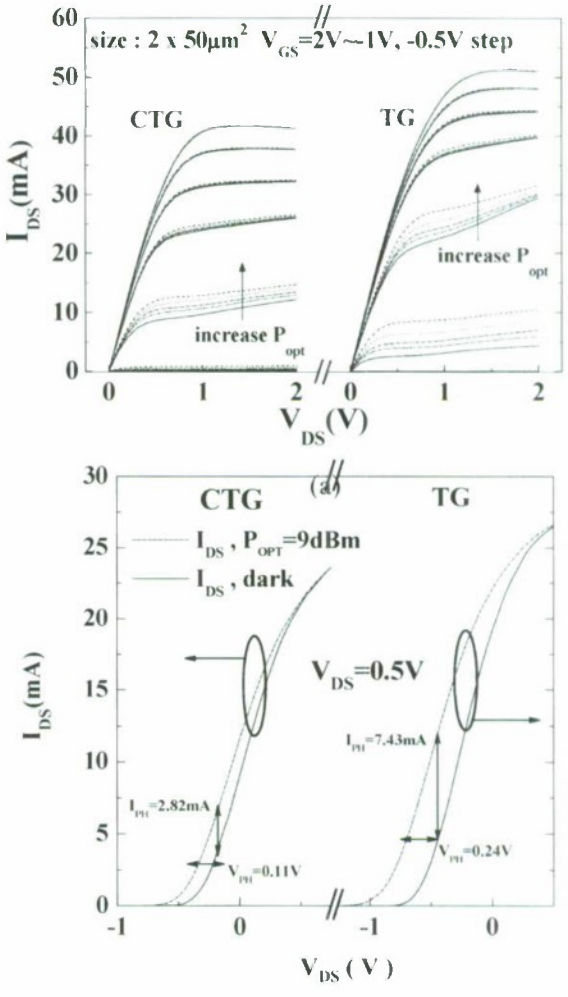
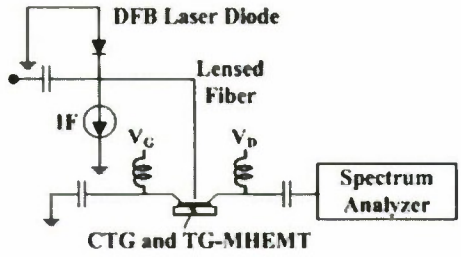
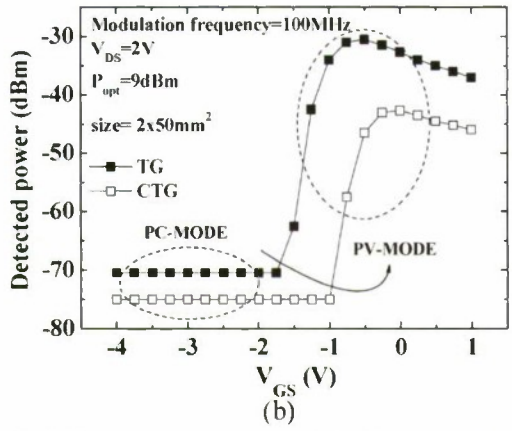


Fig. 2. (a)(b)DC I-V curve comparison between of CTG-MHEMT and TG -MHEMTs under illumination with 1.31um light.

In order to optimize the bias conditions for investigating the G_{pv} and G_{pc}, experiments were first carried out in IF frequency (100MHz). Figure 3(a) shows the experimental arrangement. The device was performed in the common-source configuration by using synthesizer as an IF source. The DC voltage source was connected through a bias-T to the gate and drain ports. The RF output from drain port was measured by a spectrum analyzer. The incident light with power of 9 dBm was modulated by a 100MHz 10dBm sine wave signal. Various gate bias conditions versus detected powers were shown in Fig 3(b). It can be seen that detected powers strongly depend on V_{GS} conditions. At photoconductance mode (turn-off condition), the detected power is quite small and roughly a constant. The non-linearity of curves for the



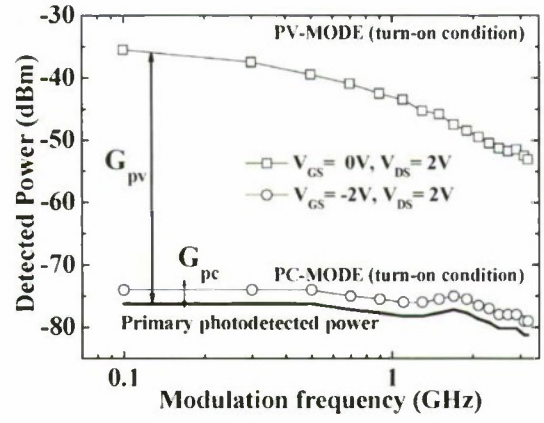
(a)



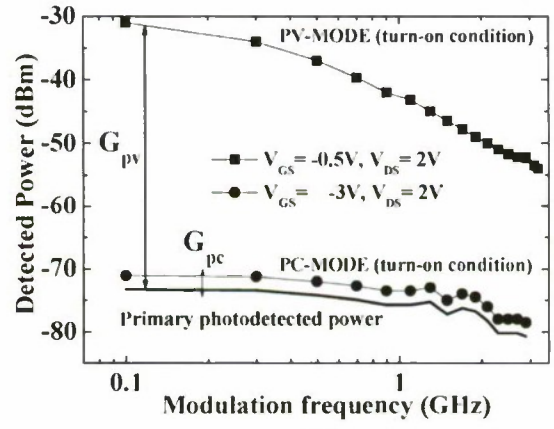
(b)

Fig. 3 (a)Experimental set-up. (b) Various gate bias conditions versus detected powers of CTG- and TG-MHEMTs. The IF frequency is 100MHz, power is 10dBm P_{opt} is 9dBm, drain bias is fixed to 2V.

photodetected signals of CTG- and TG-MHEMTs can be selectively enhanced by setting optimum V_{GS} condition. The condition was set as CTG- and TG-MHEMT biased at V_{GS}= 0V and -0.5V, respectively, with fixed V_{DS}= 2V. From which we can get the highest responsivity. By optimized gate bias points, photodetection mechanism with modulated light can be investigated for these two different cases under the fixed gate and drain voltage. Various frequencies versus detected powers were shown in Figs. 4(a) and (b). With primary photodetected powers (we had calculated above), G_{pv} and G_{pc} can be determined as shown, the difference between photodetected powers (turned-on condition) and the primary photodetected powers is the phototransistor internal gain. The optical modulation response with turned-off condition provided by the photoconductance effect was small but degraded very fast. [5] The -3dB electrical bandwidth due to the photoconductive effect is 2.3 GHz for CTG-MHEMT and only 1.4 GHz for TG-MHEMT. G_{pc} is dominated by short electron life time. In contrary, at turned-on condition, large photoresponse is obtained due to the internal gain provided by the photovoltaic effect, following the -3dB electrical bandwidth is 400MHz for CTG-MHEMT and 300MHz for TG-MHEMT, G_{pv} decays fast with frequency owing to long lifetime of photogenerated holes. However, the optoelectronic transferred signals are not strong in CTG- and TG-MHEMTs, this is because the thin channel layer designed for active devices is not thick enough to absorb all 1.31μm incident light, there is more than 50% light going through the devices. Comparing to photoresponese of TG-MHEMT, the photovoltaic and photoconductive gain of the CTG-MHEMT are smaller at low frequency owing to the transmittance of the composite gate region (30%), but CTG-MHEMT exhibit a wider bandwidth of detected power than TG-MHEMT. Figure 5 shows that the CTG- and TG-MHEMT exhibits large phototransistor internal gain although it decays rapidly due to the optical modulation response characteristics caused by the photovoltaic effect.[6][7]



(a)



(b)

Fig. 4 G_{pv}, G_{pc}, and primary detected power of the CTG-MHEMT and TG-MHEMT as a function of modulated frequency.

The mixing experimental arrangement for the optoelectronic up-conversion using CTG and TG-MHEMTs is shown in Fig. 6. When 10GHz LO was applied to the gate port and the incident light modulated by 100MHz IF signal illuminated to TG-MHEMT, the detected power of up-converted signal was -73.5dBm shown in Fig. 7 under the bias conditions of V_{GS}= -1.2V and V_{DS}=2V (class B) which were determined by the optimization process. In contrary, the up-converted signal of CTG-MHEMT is -64.2dBm under the bias conditions of V_{GS}= -0.8V and V_{DS}=2V which is better than TG-MHEMT. Due to the high conductive ITO/Au/ITO composite films, the gate resistance R_g is reduced to increase the high frequency performance of CTG-MHEMT.

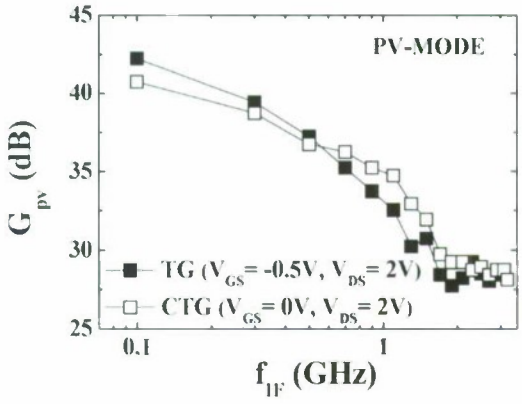


Fig. 5. G_{pv} of the CTG-MHEMT as a function of f_{IF}.

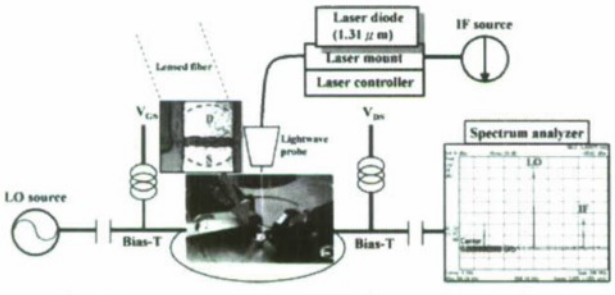


Fig. 6. 10GHz up-converted experimental set-up.

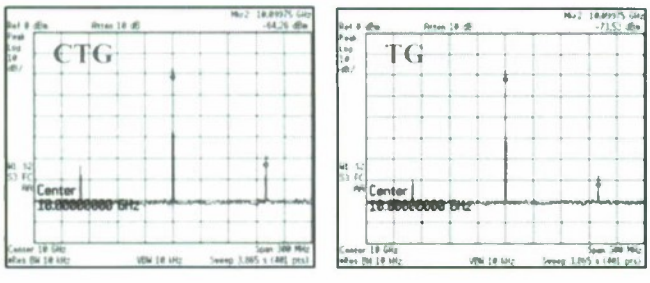


Fig. 7. 10GHz up-converted spectrum.

Conclusion

Figure. 8 shows the optoelectronic up-converted power as a function of $f_{LO}+f_{IF}$ frequency. Clearly, as these results indicating, the CTG-MHEMT as optoelectronic mixer has a wider LO frequency ranges than TG-MHEMT. Depending on radio over fiber application, the data may be an optical signal and the local oscillator an electrical signal. In this work, we proposed a CTG-MHEMT structure for 1.31μm wavelength optical response characteristics. Compared with the transparent gate MHEMT, the composite transparent gate provides a wide operating range of bandwidth and a flexible design of an epitaxial layer for integration into a MHEMT and optoelectronic mixer. The light-coupling efficiency is improved on the front side of an illuminated MHEMT. The experimental result shows that responsivity depends on incident optical power. The maximum responsivity of 1.71A/W for CTG-MHEMT and 5.97A/W for TG-MHEMT are attained at the incident optical power of -6dBm. An optimum gate-source voltage is found to maximize the level of the optoelectronic mixing component. Moreover, fabrication details, photoresponese, and mixing results are discussed for optoelectronic devices with transparent electrodes; the production of fine structures is compatible with standard lithography techniques. The proposed CTG-MHEMT features various characteristic parameters which are highly promising for the high optical response MMIC applications and simplifying the base station architecture in fiber-optic microwave transmission systems.

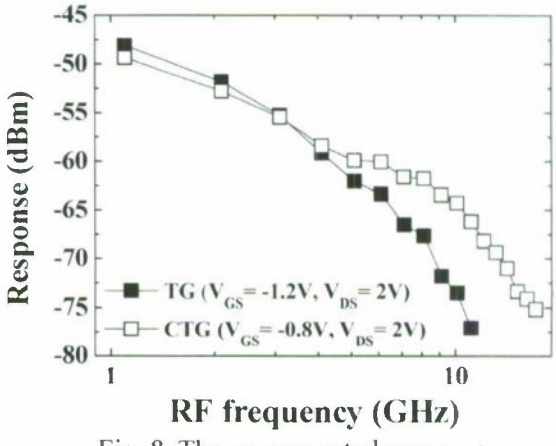


Fig. 8. The up-converted power as a function of $f_{LO}+f_{IF}$ frequency.

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Plasma-resonant THz detection with HEMTs

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Abstract

In this work, by means of Monte Carlo simulations we analyze the dependence of the DC drain current value in a 80nm-gate InAlAs/InGaAs HEMTs on the frequency of a sinusoidal signal superimposed to the DC gate bias. Interestingly, a resonant peak appears in the drain current response, which lies in the THz frequency range, in good agreement with recent experiments made on similar devices. Moreover, the frequency of the resonant peak is dependent on the length of the source-gate region, but independent of the length of the drain-gate region, thus indicating that the source-gate region acts as the plasma wave cavity leading to the resonant detection of THz radiation in HEMTs.

I. Introduction

THz radiation (also called T-rays), whose frequency range lies between microwaves and infrared light in the electromagnetic spectrum, opens the possibility for a new imaging and spectroscopic technology with a broad range of applications, from medical diagnostic (without the damage produced by ionizing radiation such as X-rays), industrial quality control or security-screening tools. The wide application area of THz science could lead to define the THz range as a specific scientific and engineering field (1, 2). In recent experiments made with InAlAs/InGaAs High Electron Mobility Transistors (HEMTs) at low temperature (3, 4), and with GaAs commercial transistors at room temperature (5), resonant THz detection as a result of plasma wave resonances has been demonstrated. However, up to now, only ideally simple theoretical models, not considering the complex real geometry of HEMTs, have been used for predicting the different types of plasma resonances that can appear in such devices (3, 6). In this work we try to explain the mechanism of plasma-resonant detection with HEMTs by means of Monte Carlo (MC) simulations self-consistently coupled with a Poisson solver (7). This technique is able to consider the real geometry and layer structure of the HEMTs and provide not only static results but also the effect of collective phenomena such as plasma oscillations.

II. Monte Carlo Simulations

Our 2D Monte Carlo simulations, based on a semi classical transport description are based on a 3-valley model (Γ-L-X nonparabolic spherical valleys for both InGaAs and AlInAs) and include ionized impurity, alloy, polar and non-polar optical phonon, acoustic phonon and intervalley scattering, and appropriate carrier injection techniques at the contacts (7). Surface charges appearing at the semiconductor interfaces with dielectrics (crucial when the size is reduced up to the nano-scale) are also self-consistently included in the simulations. More details about the model used can be found in (7).

Following Ref. (8), in order to model the THz detection mechanism, the average drain current variation is recorded when a sinusoidal signal of varying frequency is superimposed to the DC bias of the gate, V_{gs}, of a 80 nm-gate InGaAs HEMT. The geometry and layer structure of the simulated HEMT is shown in Fig. 1.

III. Results

The results for the variation of the drain current with respect to its static value, ΔI_d, as a function of the frequency of the signal superimposed to different DC values of V_{gs} are shown in Fig. 2 (the different curves have been shifted by 20 A/m each to enhance the clarity of the figure). As observed, ΔI_d shows a resonant peak (mainly for V_{gs} near pinch off) for a frequency around 2.5 THz, in good agreement with the experimental measurements (4, 5). The frequency of the peak

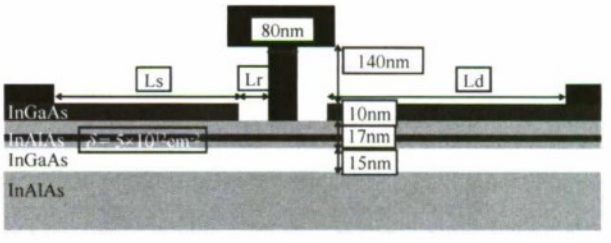

Figure 1: Sketch of the simulated HEMT

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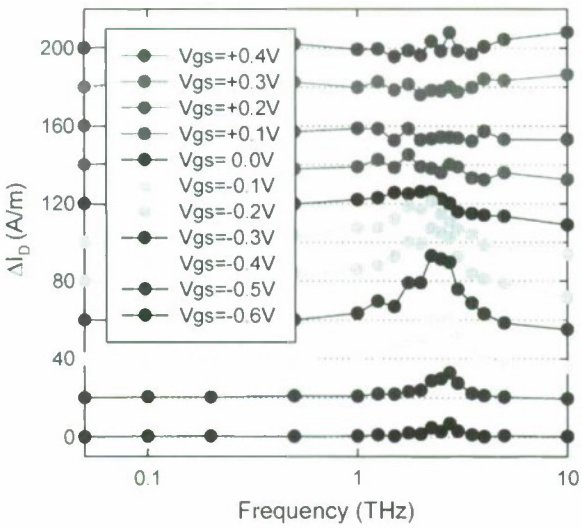

Figure 2: Average drain current variation originated by the superposition of a sinusoidal signal of 0.1 V of amplitude and varying frequency to the DC gate potential (V_{gs}) of a InAlAs/InGaAs HEMT at 300K with Ls=200 nm, Lr=100 nm and Ld=0.5 μm. The different curves have been shifted by 20 A/m each. V_{ds}=1.0 V.

slightly shifts towards lower values as V_{gs} is increased, dependence which is opposite to the experimental findings. However, as we will comment later, the conditions under which the simulations and experiments are preformed are somewhat different.

In order to understand the origin of the resonant detection we have performed simulations of HEMTs with different geometries at 300K. Fig. 3 shows the values of *Id* vs. frequency for V_{gs}=-0.3 V (optimum gate bias). In Fig. 3(a) (showing the results for the HEMT depicted in Fig. 1 compared with those of devices with a longer gate of 0.2 μm and a longer recess-drain region of 1 μm) we can observe that the frequency of the resonant peak does not depend on the gate length *Lg* nor on the recess-drain region *Ld*. On the contrary, the resonant frequency strongly depends on the lengths of the recess-source region, *Ls*, [Fig. 3(b)], and that of the source side of the recess, *Lr*, [Fig. 3(c)]. Moreover, the resonant frequency variation with *Lr* is even stronger than with *Ls*; it increases from 1.5 to more than 3 THz when reducing the value of *Lr* from 300 nm to 10 nm. These results clearly indicate that the source-gate region (including the recess) acts as the plasma wave cavity that produces the resonant detection of THz radiation in HEMTs.

It is also remarkable, that the very same characteristic frequency is also visible in the spectra of the source current noise (the comparison is shown in Fig. 4), and that of the electric potential fluctuations in the channel under the source side of the gate (the point that determines the value of *Id* since it is where the carrier injection over the potential barrier takes place).

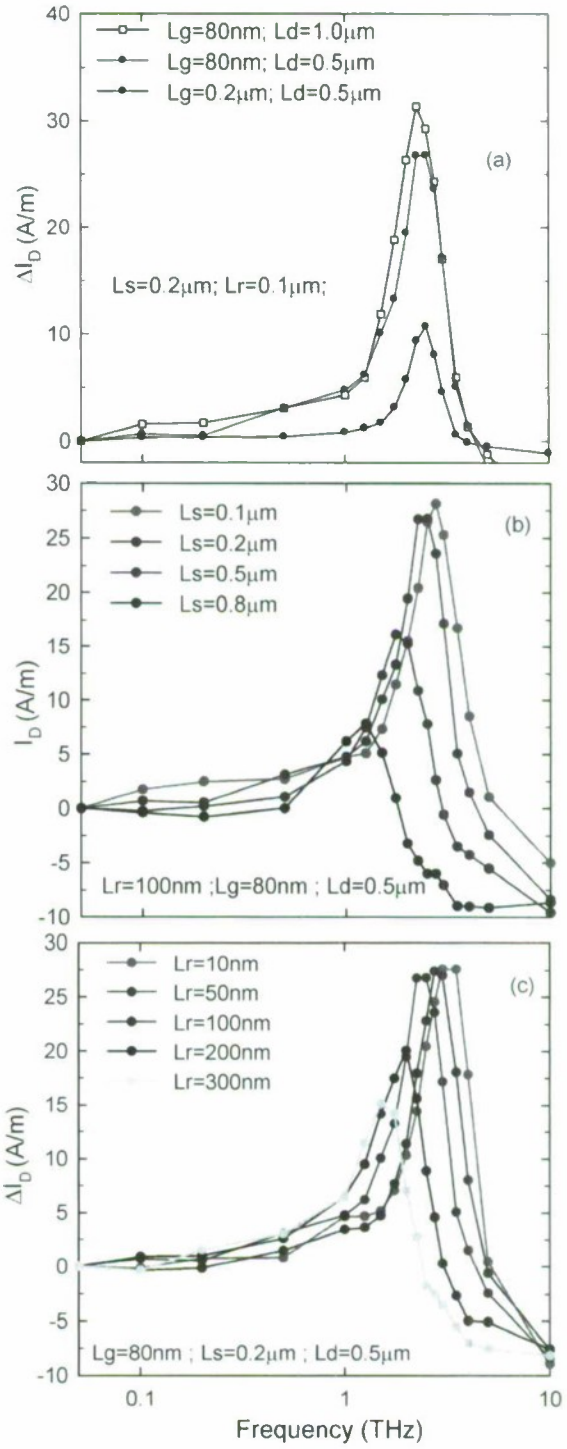

Figure 3: ΔId vs. frequency for V_{gs}=-0.3 V for different (a) Ld and Lg, (b) Ls, and (c) Lr

Dyakonov-Shur theory predicts the values of the plasma frequencies that should appear when mobile charges with

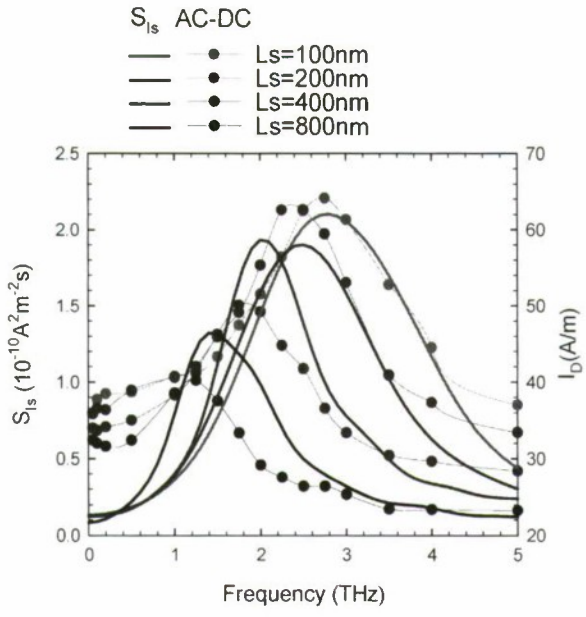

Figure 4: Comparison between the source current noise spectrum, S_{Is} and the frequency dependent drain current AC to DC conversion.

effective mass m^* are distributed in an ideally thin channel sandwiched by a dielectric material, with permittivity ε_{diel} (2D case) and when a gate contact is placed at a distance d from that surface (gated 2D case); see for example (8). Their values are, respectively:

2D plasma: $$f_p = \frac{1}{2\pi}\sqrt{\frac{e^2 n_{2D} k}{2m^* \varepsilon_{diel}}} \qquad (1)$$

Gated 2D plasma: $$f_p = \frac{1}{2\pi}\sqrt{\frac{e^2 n_{2D} d}{m^* \varepsilon_{diel}}}\,k \qquad (2)$$

$k=\pi/2L$ being the plasma wavevector, with L the length of the channel.

Due to the complex geometry of the simulated HEMT and the different plasma modes that may appear in the source-gate region (sketched in Fig. 5), there is not a unique ideal plasma model for explaining the MC results. The dependence of the resonant frequency found in the simulations when varying Ls seems to be similar to the $1/\sqrt{L}$ dependence of the 2D plasma case, while in the case of varying Lr, the dependence approaches the $1/L$ trend characteristic of the gated 2D plasma. These dependences are in agreement with the geometry of the HEMT, since the recess is covered by the gate contact while the source region is not. It is also confirmed by the fact that the resonant frequency depends on the value of the permittivity of the dielectric placed between the gate and the recess, Fig. 6. However, the values obtained in the simulations are much lower than those predicted by the ideal theory [eqs. (1) and (2)]. The only possibility to have such small values for the plasma frequencies is that the cap layer of the source region acts also as a "virtual" gate, thus providing

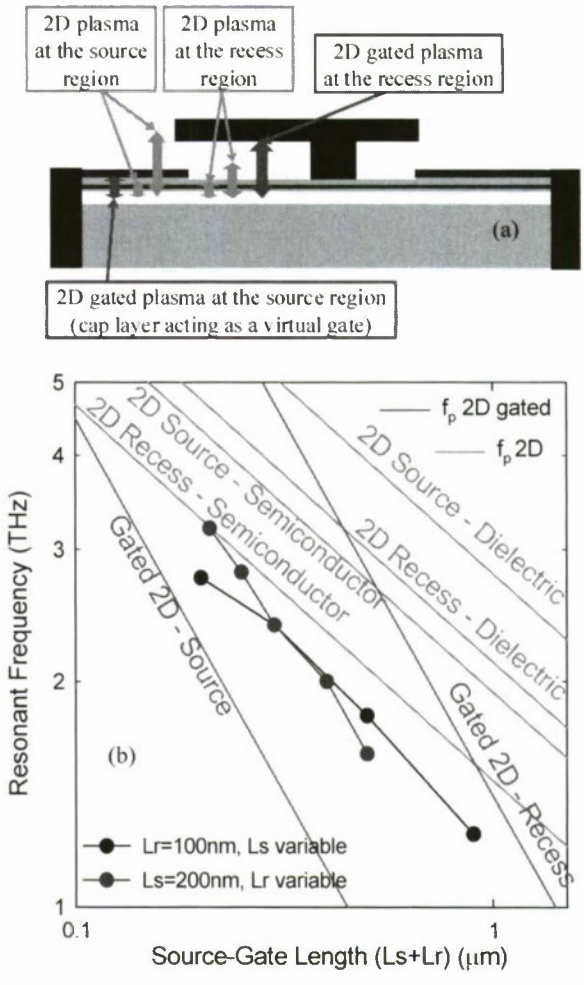

Figure 5: (a) Representation and dependence of the different possible 2D plasmas in the source-gate region of the HEMT and (b) dependence of the corresponding modes on the source-gate length as compared with the MC results.

also a possibility for a gated 2D plasma mode at that region (marked as "gated 2D source" in Fig. 5). This conclusion has also been extracted from the experimental results and the model shown in Ref. 3, even if there are some discrepancies with our findings. For example, in our case a dependence of the resonant frequency on the gate length is not clear (and also the values we obtain are much higher). However, there are important differences between the conditions imposed there and those used in our MC simulations, mainly the boundary condition at the drain contact, where the current is fixed in (3) while we enforce a constant drain voltage.

IV Conclusions

Our semiclassical Monte Carlo simulations are able to describe the mechanism for the plasma-resonant THz detection with HEMTs. Simulations show that the resonant frequency depends on the topology of the source-gate region

of the transistors and also on the dielectric used for its passivation. There exists a mechanism in the HEMTs leading to the resonant AC to DC conversion, with a characteristic frequency that also appears in the spectrum of the source current noise and in the fluctuations of the electric potential at the source region of the devices. Finally, we can conclude that the plasma-resonant THz detection observed in HEMTs is a result of a complicate combination of different modes of gated and ungated 2D plasma oscillations in the source-gate region of the devices.

Acknowledgements

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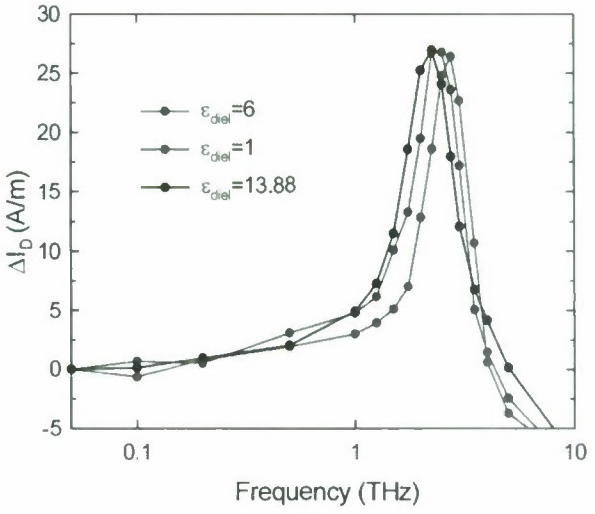

Figure 6: ΔId vs. frequency for V_{gs}=-0.3 V obtained in the HEMT with Ls=200 nm, Lr=100 nm and Ld=0.5 μm, considering different values of the permittivity of the dielectric placed at the top of the semiconductor, ε_{diel}.

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Ti- and Pt-Based Schottky Gates for InGaSb P-Channel HFET Development

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Abstract

Antimonide-based heterostructural p-channel HFET epitaxies consisting of an $In_{0.44}Ga_{0.56}Sb$ quantum well located between AlSb barriers were developed by molecular beam epitaxy. The $In_{0.44}Ga_{0.56}Sb$ channel layer was compressively strained to enhance hole mobility. Room-temperature Hall measurements to the as-grown materials exhibited a hole mobility as high as 895 cm^2/V s. Ti/Pt/Au and Pt/Ti/Pt/Au metals were utilized in Schottky gate metallization processes for evaluating their effects on the device performance. Considering the diffusivity of Pt metals, the devices with as-deposited and annealed Pt-based gates were characterized simultaneously and compared with the ones with Ti-based gates. The devices with Ti-based gates yielded superior dc and rf performances to those with Pt-based gates.

Keywords-InGaSb, p-channel, HFETs.

I. INTRODUCTION

Recently, there has been considerable interest in the potential of III-V FET materials for advanced logic applications. Sb-based HFETs are good candidates for these high-performance logic circuits owing to their high-speed and low-power potential [1]. Sb-based complementary circuits needed for this technology will require p-channel HFETs with high hole mobility. For this purpose, the $In_xGa_{1-x}Sb$ alloy system is attractive since GaSb and InSb materials have the highest bulk hole mobilities than other III-V compounds and a significant valence band barrier exists to enable quantum confinement [2][3]. Assisted by the compressive strain applied to the $In_xGa_{1-x}Sb$ channel layer, advantageous band splitting can be produced and further enhance the hole mobility as has been exploited to great effect in Si and SiGe p-MOSFETs. Furthermore, diffusion of Pt gate metals into semiconductors was a widely accepted approach to develop E-mode heterojunction field effect transistors, as applied in InAlAs/InGaAs/InP HFETs. Given annealing treatments, the continuous increases in diffusion depths of Pt metals were observed in C-V measurements. [4] The diffusivity in HFET structures not only altered the device parameters such as threshold voltage, transconductance, and gate capacitance, but also produces disadvantageous reliability issues during device operation.

II. EPITAXY GROWTH AND DEVICE FABRICATION

Figure 1 and 2 show the p-channel $In_{0.44}Ga_{0.56}Sb$/AlSb layer structure and the calculated energy band diagram, respectively. The epitaxy materials were grown by solid-source molecular beam epitaxy (MBE) on a semi-insulating (001) GaAs substrate. Growth was initiated

InAs	20 Å
$In_{0.5}Al_{0.5}As$	50 Å
AlSb (Be)	120 Å
AlSb	100 Å
$In_xGa_{1-x}Sb$	75 Å
AlSb	100 Å
$Al_{0.7}Ga_{0.3}Sb$	3000 Å
AlSb	15000 Å

Fig.1 InGaSb/AlSb epitaxy structure

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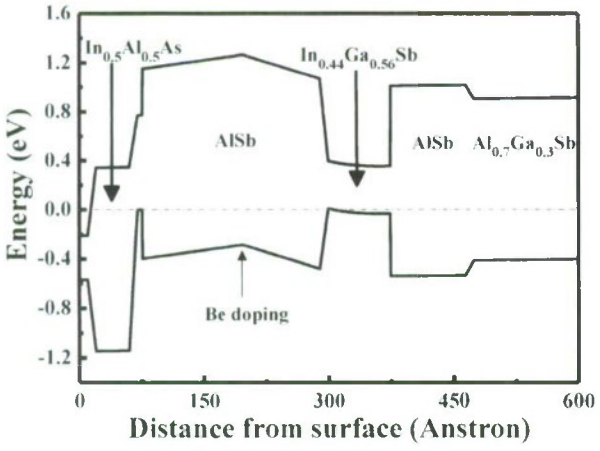

Fig. 2 Calculated InGaSb p-channel energy band diagram

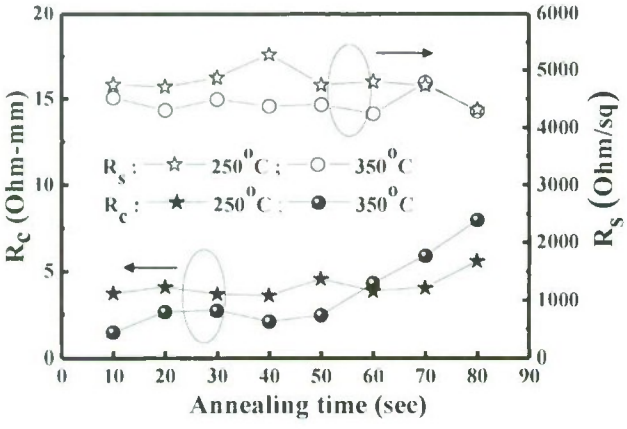

Fig. 3 Contact and sheet resistances as function of annealing time and temperature.

with a thick AlSb buffer layer. Following a 0.3μm $Al_{0.7}Ga_{0.3}Sb$ mesa floor layer, the active layers of HFET devices were grown. The active layers consisted of a 10nm AlSb bottom barrier layer, a 7.5nm $In_{0.44}Ga_{0.56}Sb$ channel layer, and a 22nm AlSb top barrier. A planar Be modulation doping sheet was inserted in the AlSb top barrier and 10nm above the InGaSb channel layer. Finally, a 0.6nm GaSb layer, a 5nm InAlAs layer, and a 2nm InAs layer were capped at epitaxy surface. The lattice constant of the InAlAs cap layer was lattice-matched to that of InP materials. Room-temperature Hall measurements to the as-grown materials exhibited a hole carrier concentration of 1.42×10^{12} cm^{-2} and a hole mobility of 895 cm^2/V-s, respectively. Implementing RTA annealing to the Pd-based ohmic contacts, the dependence of ohmic contacts on annealing temperatures and time were studied. Figure 3 shows that the minimum contact resistance of 1.8 ohm-mm is obtained at 350°C for 10s and corresponding sheet resistance is 4500 ohm/sq in TLM measurements. The HEFTs were fabricated

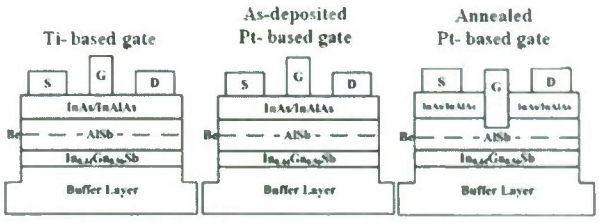

Fig.4 Cross-sectional schematics of three InGaSb p-channel HFETs.

using a conventional mesa process. Pd-based ohmic contacts were first formed using the optimized RTA annealing condition. After defining the mesa, Ti- and Pt-based Schottky gates were fabricated. Finally, Ti/Au probing pads were made. The HFETs with as-deposited and anncaled Pt-based Schottky gates were characterized simultaneously. Annealing condition is 250 °C for 30s. Figure 4 shows the cross-sectional schematics of three HFETs, which have Ti-, as-deposited Pt-, and annealed Pt-based gates, respectively.

III. Results and Discussions

Figures 5 and 6 show dc drain and transfer characteristics of the three HFETs with 2μm gate length, 50×2μm gate width, and 6μm source-to-drain spacing. The drain current and transconductance of the HFETs with as-deposited Pt- and annealed Pt-based gates are higher than those of the HFETs with Ti-based gates. The maximum drain current of 60 mA/mm and transconductance of 53 mS/mm are obtained in the HFETs with annealed Pt-based gates.

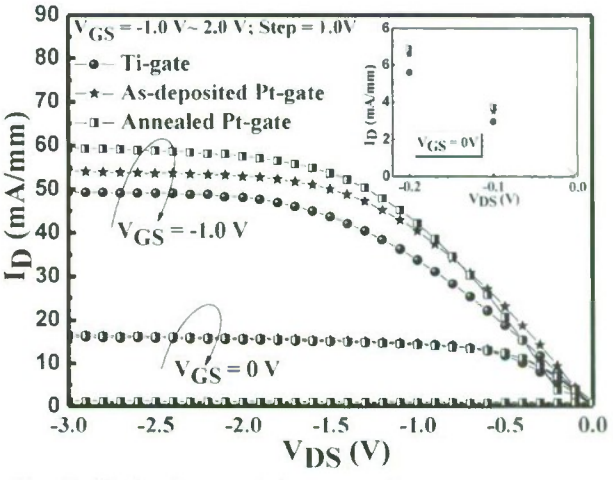

Fig. 5 Drain characteristics comparison

The threshold voltages of HFETs with as-deposited and annealed Pt-based gates are similar but slightly smaller than those of HFETs with Ti-based gates. The use of Pt metal, which can diffuse into Schottky barrier layers, results in the

decreases of threshold voltages due to reduced Schottky barrier thickness, but the decreases are partly compensated by the increased hole carrier concentration due to a larger work function of Pt than that of Ti. Figure 7 shows subthreshold drain and gate characteristics. The I_{on}/I_{off} ratio

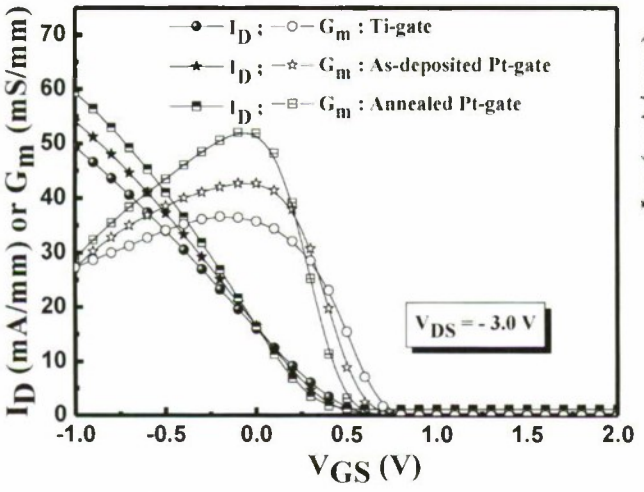

Fig. 6 Transfer characteristics

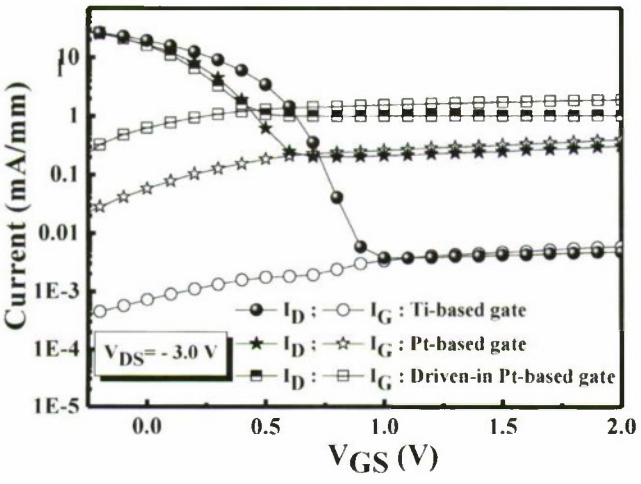

Fig. 7 Subthreshold gate and drain characteristics.

and subthreshold slope of HFETs with Ti-based gates are 9100 and 87 mV/dec, respectively, which are much better than those of HFETs with as-deposited and annealed Pt-based gates. The degraded subthreshold characteristics in the HFETs of as-deposited and annealed Pt-based gates are primarily due to the increased gate leakages generated by both reduced Schottky barrier height and thickness. Similar gate leakage behaviors are observed in the Schottky diodes (Fig. 8). Figure 9 and 10 show the frequency dependences on drain and gate biases, respectively. The maximum f_t of the three HFETs is very similar but the maximum f_{max} for the HFETs with Ti-based gates is higher than that for the HFETs with as-deposited and annealed Pt-based gates. A maximum f_t of 1.95 GHz and a maximum f_{max} of 6.75 GHz are obtained in a 2μm-gate-length HFET with Ti-based

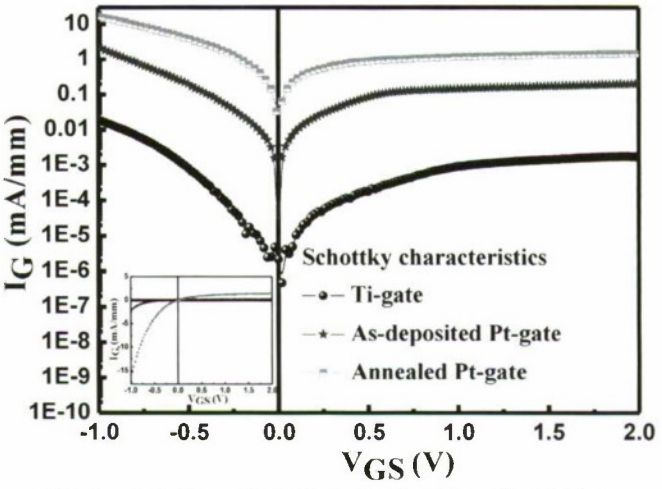

Fig. 8 Schottky gate leakages as function of gate bias

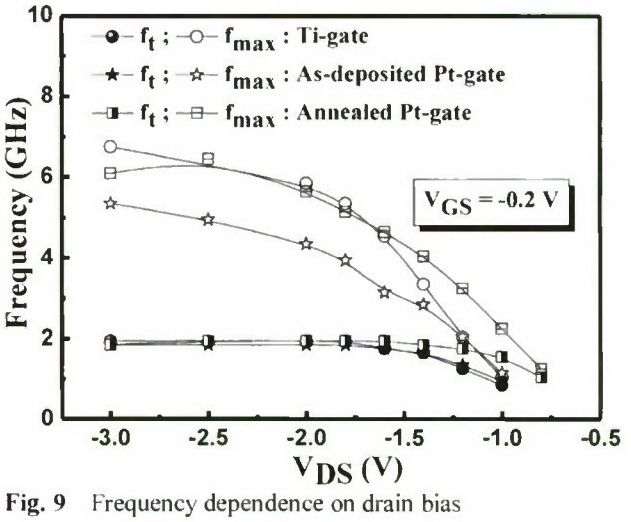

Fig. 9 Frequency dependence on drain bias

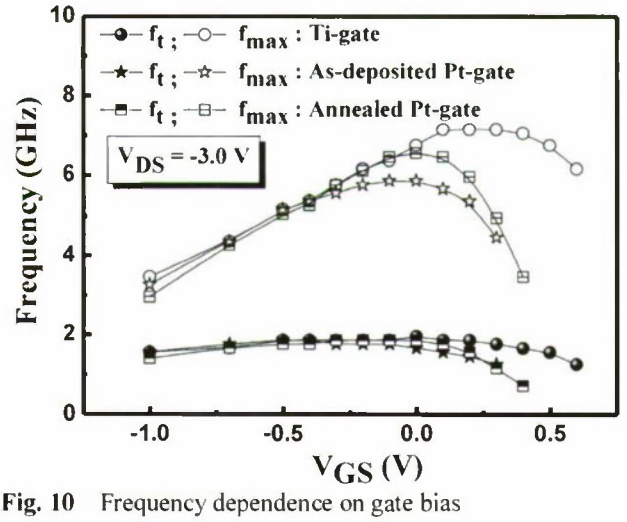

Fig. 10 Frequency dependence on gate bias

gates. This work successfully develops and characterizes the InGaSb p-channel HFETs using Ti-, as-deposited Pt-, and annealed Pt-based Schottky gates.

IV. Conclusion

In summary, high-quality InGaSb quantum-well epitaxy materials and functional p-channel HFET devices with Ti- and Pt-based Schottky gates were successfully developed and characterized. Effects of post-gate annealing on the HFETs with Pt-based gates were also evaluated. The HFETs with Ti-based gates yielded better dc and rf performance than those with Pt-based gates. This was primarily due to reduced Schottky barrier height and thickness which induced serious gate leakage issues when diffusive Pt metals were used and driven into semiconductors. A 2μm-gate-length HFET with Ti-based gates showed a maximum driving current of 50 mA/mm, a peak transconductance of 36 mS/mm, a subthreshold slope of 87 mV/dec, and an I_{on}/I_{off} ratio of 9100 in dc performances, and an $f_{t,peak}$ of 1.95 GHz and an $f_{max,peak}$ of 6.75 GHz in rf performances.

Acknowledgement

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A NEW LOW-POWER RTD-BASED 4:1 MULTIPLEXER IC USING AN InP RTD/HBT MMIC TECHNOLIGY

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Abstract

A low-power 4:1 multiplexer (MUX) IC using Resonant Tunneling Diodes (RTDs) is proposed and fabricated. The proposed 4:1 MUX topology consists of two RTD-based 2:1 MUX ICs and a 2:1 selector IC. By using the unique NDR (Negative Differential Resistance) characteristics of the RTD, the proposed IC has achieved a significantly reduced dc power consumption compared to the conventional III-V transistor-based topology. The fabricated IC shows 15 Gb/s operation with dc power consumption of 80 mW.

I. INTRODUCTION

To meet the rapidly growing demand for advances in the information infrastructure, the capacity of the digital communication systems must be expanded. In these systems, a 4:1 multiplexer (MUX), which is placed in the front end of a transmitter block, is a key component in order to achieve the required operational speed because it serializes parallel data with a low bit rate into a single data stream with the maximum transmission rate. Several 4:1 MUX circuits have been reported in a variety of conventional device technologies such as InP-based HBTs and InP-based HEMTs [1], [2].

The conventional 4:1 MUX ICs usually consume a relatively high dc power of several-hundreds milli-watts or more due to the large device count and complex interconnect lines. In order to realize power efficient systems, a 4:1 MUX IC operating at low-power consumption needs to be exploited. The negative differential resistance (NDR) digital IC technology using resonant tunneling diodes (RTDs) is one of various approaches to fulfill this requirement [3], which can drastically reduce the dc power consumption of the 4:1 MUX compared to the conventional ICs. We previously demonstrated the low-power RTD-based 2:1 MUX IC, which is a sub-block of the full 4:1 MUX IC topology [4]. In this work, we present a new low-power RTD-based 4:1 MUX IC using the InP-based RTD/HBT MMIC technology. The dc power consumption of the new 4:1 MUX IC is considerably reduced compared to the conventional III-V transistor-based 4:1 MUX topologies.

II. CIRCUIT CONFIGURATION

The schematic block diagram of the new RTD-based 4:1 MUX IC is shown in Fig. 1. The IC is composed of 2 stages, where the 1st stage consists of two RTD-based 2:1 MUXs and the 2nd stage is a 2:1 selector IC based on the conventional selector

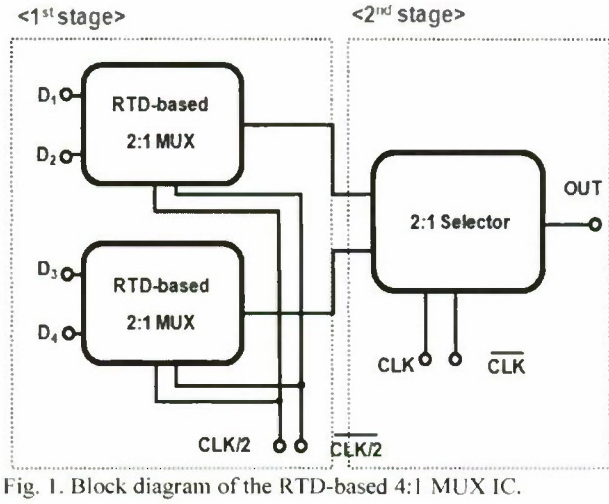

Fig. 1. Block diagram of the RTD-based 4:1 MUX IC.

topology [5]. An RTD-based 2:1 MUX is composed of two RTD CML MOBILEs (Current-Mode-Logic MOnostable-BIstable-transition-Logic-Elements) and a NOR gate which is operating as a low voltage selector IC [4]. At the 1st stage, 2:1 multiplexing operation occurs with low-power / high-speed performances by means of the NDR property of RTDs. The detailed operation is explained elsewhere [4]. At the 2nd stage, the 2:1 selector IC, which serializes data streams generated from both RTD-based 2:1 MUX ICs, enables the new RTD-based circuit to perform the 4:1 multiplexing operation. The designed RTD-based 4:1 MUX IC has the features of both the compactness and high functionality by actively utilizing the power-efficient NDR topology. Therefore, the new 4:1 MUX IC substantially reduces the dc power consumption. In addition, the total device count of the

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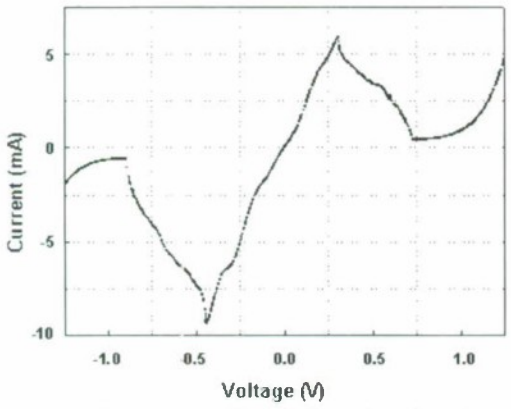

Fig. 2. Measured I-V curve of the fabricated InP-based RTD with an emitter area of 1.8 × 6.4 μm^2.

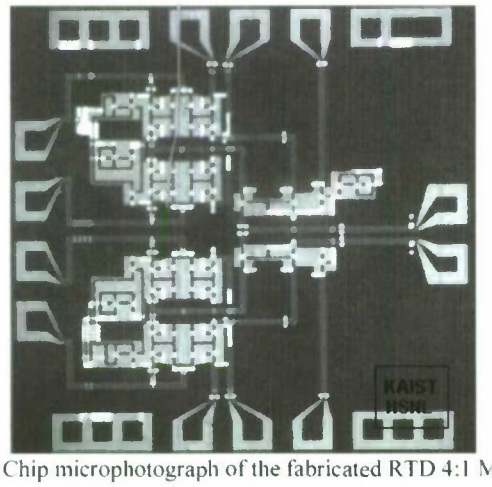

Fig. 3. Chip microphotograph of the fabricated RTD 4:1 MUX IC.

RTD-based 4:1 MUX IC is 51, less than 1/3 of that in the conventional tree-type master-slave topology.

III. Device and Fabrication Technology

The proposed RTD-based 4:1 MUX IC was fabricated by using an InP-based monolithic RTD/HBT IC technology with a minimum device feature size of 1.5 μm. The detailed layer structure and fabrication sequence have been described previously [6]. The fabricated InP-based RTD with an emitter area of 1.8 × 6.4 μm^2 has a peak voltage (V_P) of 0.30 V, a peak current density (J_P) of 60 kA/cm^2, and a peak-to-valley current ratio (PVCR) of 13.5 at room temperature, as shown in Fig. 2. The fabricated InP-based SHBT with an emitter area of 1.5 × 5.4 μm^2 shows a maximum current gain of 50, and the maximum f_T

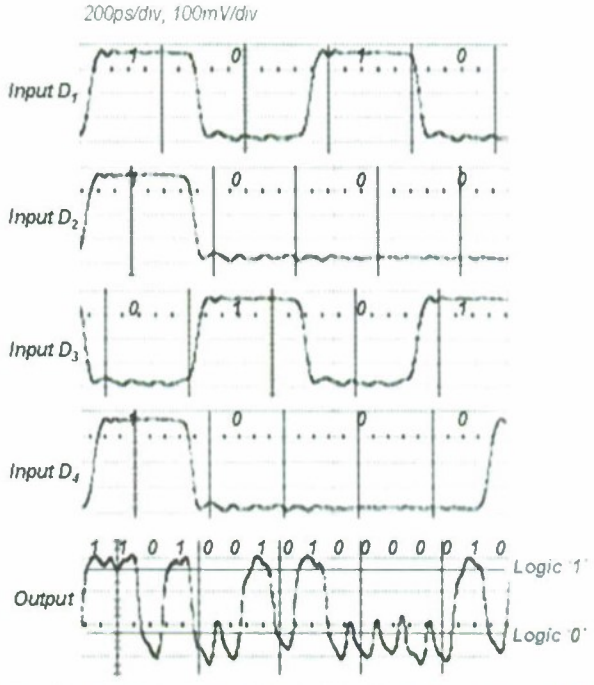

Fig. 4. Input and corresponding output waveforms measured at 15 Gb/s.

and f_{max} of 100 GHz and 100 GHz, respectively. A chip microphotograph of the fabricated 4:1 MUX IC is shown in Fig. 3.

IV. Measurement Results

The performance of the fabricated 4:1 MUX IC was characterized by on-wafer probing. In order to confirm the operational performances, time-domain measurements were performed at 15 Gb/s. Fig. 4 shows the test input data patterns (D_1 = 1010, D_2 = 1000, D_3 = 0101, D_4 = 1000) at 3.75 Gb/s and the corresponding output patterns (1101001010000010) at 15 Gb/s. Fig. 5 shows the measured output eye diagram at 15 Gb/s. The output voltage swing was 300 mV_{pp}. The operation of the fabricated RTD-based 4:1 MUX IC has been successfully confirmed up to 15 Gb/s. The operation speed will be enhanced by optimizing the device performance and IC layout. At a supply voltage of -3.3 V, the RTD-based 4:1 MUX shows extremely low dc power consumption of 80 mW. Two RTD CML MOBILE ICs and a 2:1 selector IC show dc power consumption of 45 mW and 35 mW, respectively. The obtained dc power consumption of the RTD-based 4:1 MUX IC is a considerably reduced value compared to that of the conventional III-V transistor-based 4:1 MUX ICs with a similar device feature size [7]. Table 1 summarizes the measured performances of the fabricated 4:1 multiplexer IC.

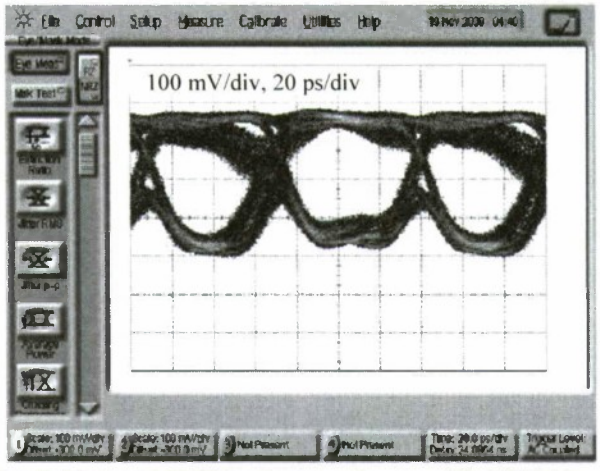

Fig. 5. Measured 15 Gb/s output eye diagram of the RTD 4:1 MUX IC.

V. Conclusion

A 4:1 MUX IC based on the InP-based RTDs has been proposed and fabricated. The proposed IC exploits the power efficient technology based on the NDR property of RTDs. The fabricated IC achieved the operating speed of 15 Gb/s with the dc power consumption of 80 mW. The obtained dc power consumption is a significantly reduced value when compared to the conventional III-V material based ICs. The results achieved in this work demonstrate the potential of the InP-based RTD/transistor monolithic IC technology for low power / high speed digital optical communication systems.

Acknowledgment

This work was supported by the National Program for Tera-level Nano-Devices of the Ministry of Education, Science and Technology in the Republic of Korea as one of the 21st - Century Frontier Programs.

TABLE I
Performance Summary

Technology	InP RTD/HBT
Output data rate	15 Gb/s
Output voltage swing	300 mV_{p-p}
Supply voltage	-3.3 V
Current consumption	37 mA
DC power consumption	80 mW

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LOW POWER K-BAND SECOND HARMONIC BALANCED VCO IC USING InP BASED RTDs

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Abstract

A K-band InP-based RTD second harmonic balanced VCO utilizing a push-push approach is presented. The fabricated RTD VCO IC shows the total dc power consumption of 136 μW, which is the lowest reported up to date in the K band.

I. Introduction

Due to the excellent quantum-effect negative differential resistance (NDR) characteristics and strong *I-V* nonlinearity, the InP-based resonant tunneling diode (RTD) has attracted a great deal of interests in microwave applications [1]. Recently, InP-based low-power microwave RTD VCOs, which are critical building blocks in microwave transceivers, have been reported exhibiting very low dc power consumption in the VCO core parts [2], [3]. However, for practical system applications, additional buffer amplifiers are usually required to isolate the VCO core from an output load, which results in a considerable increase of the total dc power consumption [4], [5].

In this work, a second harmonic balanced RTD VCO is presented based on a push-push approach in order to drive the output load directly without the buffer amplifiers, leading to low total dc power consumption. The second harmonic balanced VCO, operating in the K band, has been fabricated by using an InP-based RTD/HBT monolithic IC technology. To the best of our knowledge, the total dc power consumption of the fabricated RTD VCO is the lowest among the low power VCOs reported in the K band.

II. Device Technology and VCO Design

The RTD-based second harmonic balanced VCO has been implemented by using an InP-based RTD/HBT monolithic IC technology. The fabrication process and the detailed layer structure have been described elsewhere [2], [3]. Fig. 1 shows the measured dc *I-V* characteristic of the fabricated RTD with an emitter area of 1.2×1.2 μm^2 at room temperature. The RTD exhibits a peak voltage (V_p) of 0.29 V and a peak current (I_p) of 0.68 mA with a peak-to-valley current ratio (PVCR) of 7.2.

As shown in Fig. 2, the RTD-based second harmonic balanced VCO is basically a balanced configuration using two

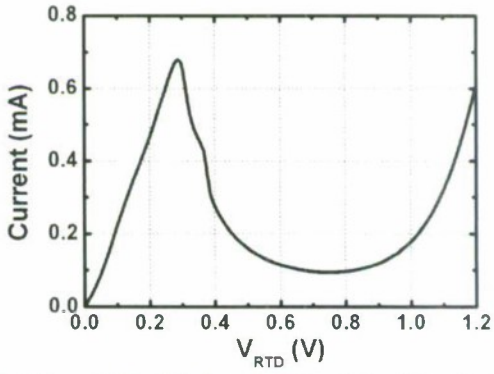

Fig. 1. Measured dc *I-V* characteristic of the fabricated RTD with an emitter area of 1.2×1.2 μm^2 at room temperature.

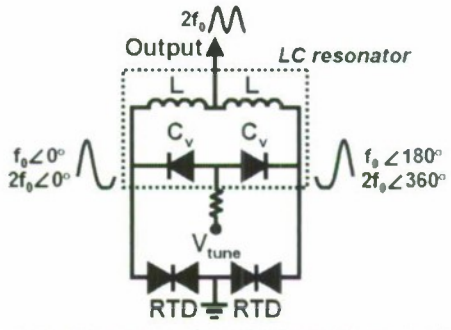

Fig. 2. Circuit schematic of the RTD-based second harmonic balanced VCO.

RTDs capacitively-coupled by the varactors, which generates the fundamental-frequency oscillating signals at the RTD terminals in the odd mode [2], [3]. At the center node between two resonator inductors, the antiphase fundamental frequency components cancel out, whereas the inphase second harmonic

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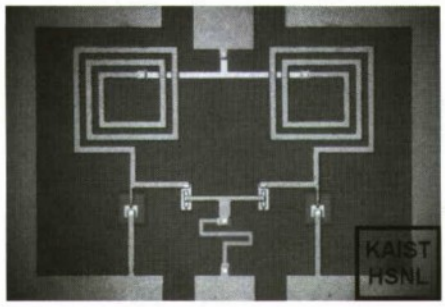

Fig. 3. Microphotograph of the fabricated RTD VCO IC.

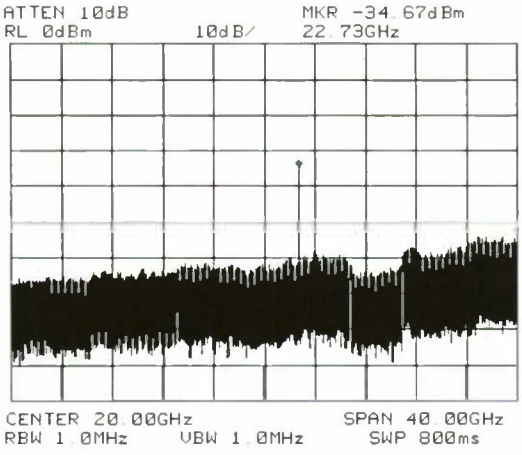

Fig. 4. Measured output spectrum of the fabricated RTD VCO IC.

components sum up being extracted to the output port, based on the push-push principle [6]. As a result, the RTD VCO enables the direct driving of an output load without the buffer amplifier for the second harmonic frequency, which arises from isolating the RTD terminals from the output load. The varactor diode has been formed by using the base-collector junction of the InP-based HBT. The capacitance of the varactor diode with a junction area of 4×24 μm^2 is 100 fF at a bias of 0 V. The inductance of the spiral inductor is 1.25 nH.

III. Measurement Results

The microphotograph of the fabricated RTD VCO IC is shown in Fig. 3. The chip area excluding the pads is 490×365 μm^2. The fabricated RTD VCO IC was characterized by on-wafer measurements using a spectrum analyzer with an input impedance of 50 Ω. The dc bias voltage of 0.62 V for the RTD

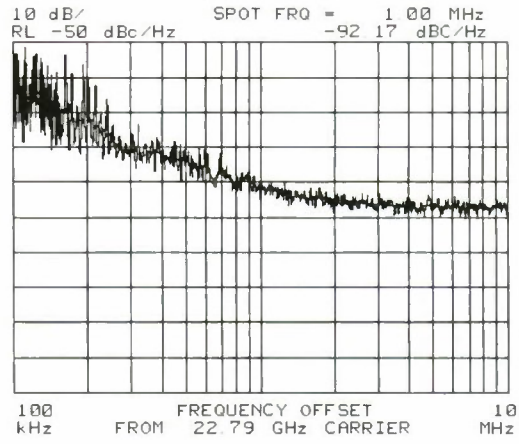

Fig. 5. Measured phase noise versus the offset frequency of the fabricated RTD VCO IC.

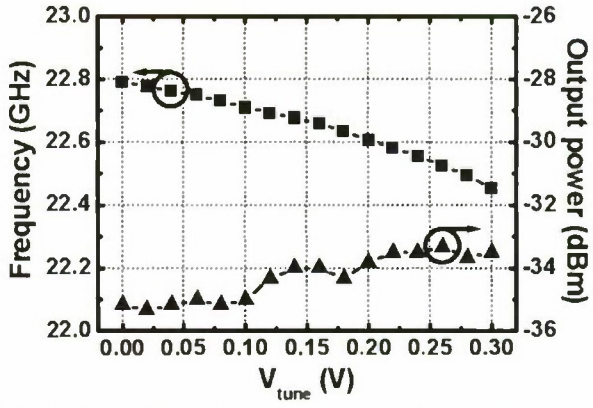

Fig. 6. Measured oscillation frequency and second harmonic output power of the fabricated RTD VCO IC as a function of the tuning voltage (V_{tune}) for the varactor diode.

VCO IC with the total bias current of 219 μA was supplied through the output port by using the bias tee [6].

Fig. 4 shows the measured output spectrum of the fabricated RTD VCO IC with an output power of −35 dBm at the second harmonic oscillation frequency of 22.7 GHz. The output power at the fundamental frequency is measured to be −63 dBm, which exhibits the fundamental rejection of 28 dB. Fig. 5 shows the measured phase noise of −92.2 dBc/Hz at 1 MHz offset frequency. The total dc power consumption of the fabricated RTD VCO IC is 136 μW. The measured oscillation frequency and the second harmonic output power are shown in Fig. 6 as a function of the tuning voltage (V_{tune}) for the varactor diode. The tuning range for the oscillation frequency

is 338 MHz. The figure-of-merit (FOM) of the fabricated RTD VCO [3] is calculated to be −188 dBc/Hz at the total dc power consumption of 136 μW. Compared to the conventional low power monolithic VCO ICs [4], [5], the fabricated RTD VCO shows the lowest total dc power consumption with the excellent FOM in the K band.

IV. Conclusion

An RTD-based second harmonic balanced VCO, which utilizes the push-push principle in order to achieve the very low total dc power consumption, has been implemented by using an InP-based monolithic IC technology. The fabricated K-band RTD-based second harmonic balanced VCO IC exhibited the lowest total dc power consumption of 136 μW with the excellent FOM in the K-band. Compared to the reported conventional low power VCOs in the K band, the RTD-based second harmonic balanced VCO can be considered to be one of the best candidates for the extremely low power practical MMIC applications.

Acknowledgment

This work was supported by the National Program for Tera-level Nano-Devices of the Ministry of Education, Science and Technology in the Republic of Korea as one of the 21st - Century Frontier Programs.

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SCALABLE HIGH-CURRENT DENSITY RTDS WITH LOW SERIES RESISTANCE

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***Abstract*—**InP-based double-barrier resonant tunnelling diodes have been optimized for high speed digital circuits. We present the scalability of high current density ($J_P \approx 150$ *kA/cm²*) resonant tunnelling diodes in the sub-micrometer electrode area range. A small signal equivalent circuit has been developed and its parameters are precisely deduced from DC and RF measurements. Based on this model the scalability has been investigated with emphasis on a low but also scalable series resistance in order to keep the peak voltage constant. A comparison of dry and wet etching methods in the device fabrication will be presented. A multiple mesa concept has been adopted to provide reliable scalability at low emitter area ($A_E < 1$ µm²).

Keywords: *Resonant tunnelling diodes, high speed logic circuits, scalability, modeling.*

I. INTRODUCTION

Resonant tunnelling diodes (RTD) are promising devices for high-speed circuit design. The negative differential resistance in their non-linear current-voltage characteristic and their fast switching speed make them suitable for a wide range of circuit applications. A well known digital circuit example is the monostable-bistable transition logic element (MOBILE) suitable for various logic gates [1, 2, 3] but also for analogue and mixed signal circuits such as oscillators [6] and pulse generators [7].

The MOBILE consists of two series connected RTDs. It is a robust high speed self-latching logic gate that requires for high speed operation both, a high peak current density and a very small emitter area, respectively. Moreover, the logic function is determined by the absolute current value and hence is very sensitive to the homogeneity and reproducibility of epitaxial growth and to the precision of emitter area definition. To increase the switching speed of the MOBILE, it is necessary to increase the current density of the RTDs [8]. However, this approach makes the device even more sensitive to epitaxial growth fluctuations [3]. To reduce the static power consumption of the MOBILE gate a very low valley current will be needed. A high peak-to-valley current ratio (PVCR) is a figure of merit for good RTDs. The series resistance is a parasitic component of the RTD, and is dominated by the ohmic contact and the resistance of the contact layer. It has to be kept low to reduce the voltage drop in high current region and to reduce the RC-delay. Moreover, the voltage drop at the parasitic series resistance and its scaling with device area are tremendous problems complicating a precise scaling of I-V data at DC and RF which is mandatory for the functionality of high speed circuits. Recently, some reports on ultra high current density devices up to $J_P \approx 1800$ *kA/cm²* [6], however a precise and scalable RTD device at very high current density data is lacking.

In this work a sophisticated processing technology is combined with a novel small signal extraction method in order to set up a scalable high current density / high PVCR ($J_P \approx 150$ *kA/cm², PVCR > 10*) small area RTD device model.

II. RTD TECHNOLOGY & DESIGN

The epitaxial growth of the heterostructure layer sequence was realised with molecular beam epitaxy (MBE) on semi-insulating InP-substrates [3]. The intrinsic RTD structure (cf. Table 1) consists of an InGaAs/InAs/InGaAs quantum well sandwiched between 1.7 nm AlAs barriers. The lattice matched InGaAs smoothes the surface after lattice-mismatched growth and reduces the valley current such that a peak-to-valley current ratio > 10 becomes feasible despite the high current density. All InGaAs layer within the RTD-structure are nominally lattice matched.

The device processing was carried out using electron beam and optical lithography, wet or dry etching, and Ti/Pt/Au lift-off contact technology. Ni is added on top if the metallisation is used as a mask for dry etching. The process started with the definition of single or multiple RTD-anode electrodes down to a nominal area 0.75² µm². Using the upper electrode as an etch mask, the RTD-layer stack was etched down to the lower contact layer. Two etching processes were compared: the inductively-coupled plasma reactive ion etching (RIE) and the wet chemical etching.

Dry etching of RTD-layer stack was performed in an Oxford Instruments PlasmaLab System 100 ICP65, in which both

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sources operate at 13.56 MHz. The well established [4] Cl2/N2 mixture with total gas loads of 40 standard cubic centimetres per minute (sccm) was injected into the reactor through mass flow controllers (MFCs) at a ratio of 4/36. During the process the temperature of the heated chuck was held at 170°C. The initial strike pressure, ICP source power and RF chuck power were 45 mTorr, 300 W and 150 W respectively. With stahle plasma conditions the parameters were ramped down within a few seconds to the desired process parameters of 10 mTorr (reactor pressure), 150 W (ICP source power) and 50 W (RF chuck power). A total etch time of 210 s leads an etch depths of approximately 425 nm, ensuring that the lower interconnection layer is reached.

Table I Layer sequence of the fabricated AlAs/InAs-RTD with InGaAs layer using respectively for contact and smoothing.

function	material	thickness [nm]	doping [10^{18}cm-3]
Contact layer	InGaAs	200	10
Grading layer	InGaAs	50	10
Contact layer	InGaAs	50	1
Spacer	InGaAs	1.17	
Barrier	AlAs	1.7	
Well, smoothing	InGaAs	1.17	
Well	InAs	1.21	n.i.d.
Well, smoothing	InGaAs	1.17	
Barrier	AlAs	1.7	
Spacer	InGaAs	1.17	
Contact layer	InGaAs	50	1
Grading layer	InGaAs	50	10
Contact layer	InGaAs	200	10
Substrate	s.i. InP		

In comparison wet chemical etching was carried out with diluted phosphoric acid (H3PO4) at room temperature. The mixture of 1:1:25 (H3PO4:H2O2:H2O) with hydrogen peroxide and water is highly selective for InGaAs with aspect to InP [5].

The dry etching via the ICP RIE process (cf. Fig. 1a) results in a precise mesa area definition with almost vertical side walls. In contrast, the wet chemical etching produces etch undercut which reduces the mesa area of the effective device area as show in Fig.1b. Especially for small active area RTD devices this etch undercut increases the process variations and fluctuation of critical parameters like peak current and peak voltage as well as the resistance of the upper ohmic contact.

After processing the top mesa, the lower RTD contact electrode is defined. Here, patterning is done using electron beam lithography which assures high alignment accuracy. The metallisation of the non-alloyed ohmic contact is done by evaporation and lift-off. The less critical lower RTD mesa was patterned and etched using optical lithography and wet chemistry (H3PO4:H2O2:H2O (1:1:25) for InGaAs contact layer, and in addition HCl:H2O (1:1) for the InP substrate surface to prevent leakage currents) respectively for both samples.

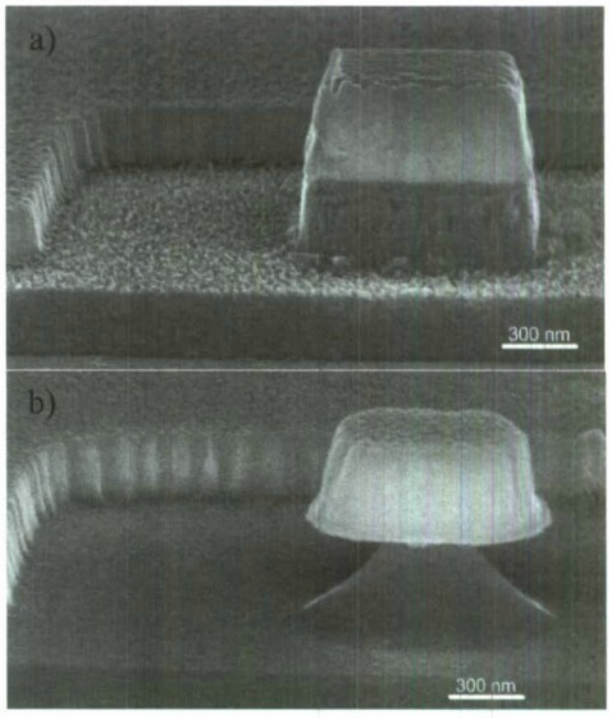

Figure 1. SEM micrograph of two RTD mesas processed by using ICP RIE dry (a) and wet chemical (b) etching, respectively.

The air bridge contact to the top electrode was fabricated by polyimide deposition combined with O_2-plasma etching just until the top metal electrode is etched free before top contact metal patterning. This process combines device passivation and electrical isolation of the top contact with the connection of the upper and lower device electrode via bridge to an on wafer GSG measurement pad configuration. The SEM micrograph of a fabricated 4-mesa device is shown in Fig. 2. A typical I-V characteristic of a fabricated RTD is given in Fig. 3 exhibiting a very high peak-to-valley current ratio (>10).

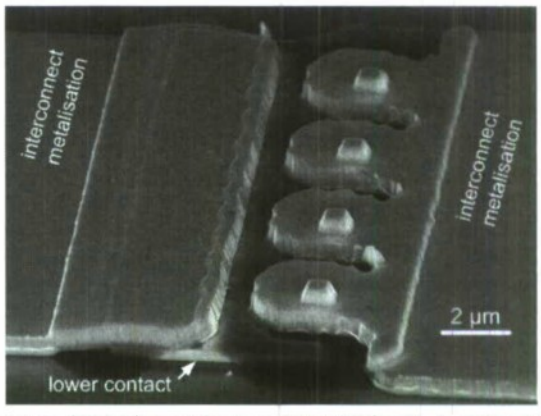

Figure 2. SEM micrograph of quad mesa RTD with 4 x 0.75 x 0.75 µm² active area.

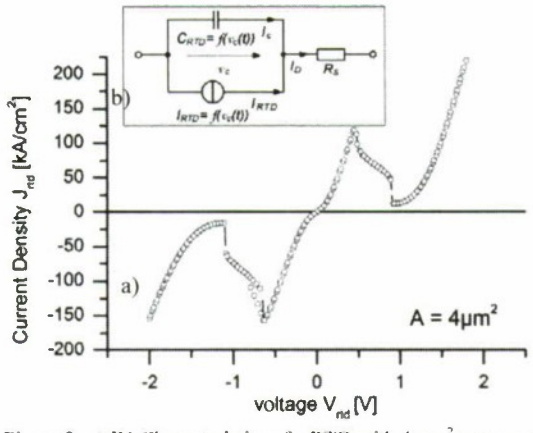

Figure 3. a) IV-Characteristics of a RTD with 4-µm² mesa area b) large signal model with bias independent series resistor Rs

III. Device Characterisation

The fabricated devices have been characterized under DC conditions to extract the peak current density from the IV-characteristics. The peak current density is defined as the device current divided by the nominal contact area. In Figure 4 the experimental peak current density for devices with a nominal contact area of 0.56 µm² up to 25 µm² are depicted for the two investigated process technologies. The wet etching results in a lower effective mesa area (cf. Fig. 1b). Hence, the nominal peak current density is always lower than in case of RIE etching. At smaller area (< 10 µm²), the undercut of wet chemical etching decreases the nominal current density down to 1/3 of the original value. The dry etched sample, however, shows a good scalability and reproductively of the nominal peak current density down to 0.75 µm² electrode area with yield higher than 90%. This technology is the best candidate for RTD manufactoring in the nanometer range.

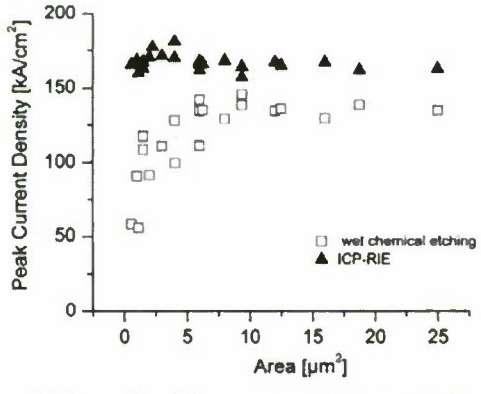

Figure 4. Measured Peak Current Density for the ICP-RIE process and wet chemical process

RTDs are unstable from DC to very high frequencies due to their high negative differential resistance. This bias dependent (negative) resistance is in series with the (positive, non-bias dependent) series resistance within a large signal equivalent Circuit model. The bias dependent negative resistance is represented by the voltage control current source within equivalent circuit in Fig. 3b. Therefore, a precise determination is very difficult in a one terminal device. Recently, a new method based on scattering parameter measurements was developed in our group, which is based on the real part of the impedance of the small signal equivalent circuit:

$$\mathrm{Re}\{\underline{Z}_{\mathrm{RTD}}\} = R_s + \frac{R_s}{1+(\omega C_d R_d)^2} \qquad (1)$$

Here C_d and R_d are the RTD capacitance and the differential resistance, respectively. When the RTD is biased in peak or valley voltage region, the differential resistance R_d becomes nearly infinite. For these bias conditions the real part of the RTD impedance converges to R_s for high frequencies. In Figure 5 the measured RTD impedance is depicted for bias voltages near the valley voltage (grey lines). When the valley voltage (solid black) is met, R_s can be extracted from the real part of the impedance for frequencies above 30 GHz. This procedure allows reliable extraction of the source resistance R_S.

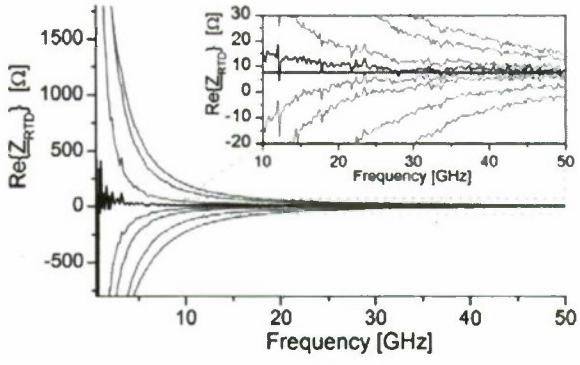

Figure 5. Real part of the RTD impedance extracted from S-parameter measurements up to 50 GHz

The series resistance for varying mesa area of RIE etched sample is shown in Figure 6 for the investigated single-mesa, double-mesa and quad-mesa design (cf. Fig.2). The wet chemical etched sample has similar series resistances for devices with nominal active area bigger than 2 µm² and up to 20% higher series resistance than the RIE etched sample for small areas devices.

To investigate the operation speed, the RTD-capacitance has to be considered additionally. In Figure 7 the extracted capacitance in the valley region is shown for the investigated devices. As can be seen, the capacitance increases nearly linear with emitter size. By using linear regression the area independent extrinsic capacitance C_{ext} was estimated to be 3.5 fF, 6.0 fF and 9.8 fF for the single, double and quad mesa design respectively. This capacitance can mainly he attributed to the overlap capacitance between upper and lower contact

metallisation (cf. Fig.2) According to Fig. 2 this overlap and so related capacitance can be further reduced considerably.

A comparison between single and quad mesa RTDs considering operation speed can be made by calculating the RC time constant of devices with the same emitter area. For 4 µm2 device area the RC-time constant can be reduced from 230 fsec to 160 fsec by splitting the active RTD area (quad mesa).This indicates that the slight increase in parasitic capacitance is overcompensated by the substantially reduced series resistance of the multiple mesa design RTDs enabling higher speed operation, especially when simultaneously reduces the overlap capacitance as discussed above.

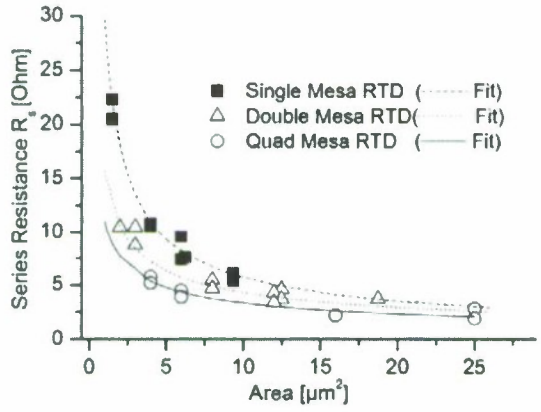

Figure 6. Series resistance for Single, Double and Quad mesa Design

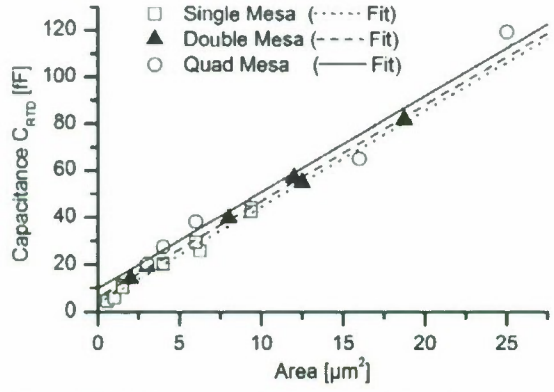

Figure 7. RTD-Capacitance for Single, Double and Quad mesa Design

IV. Conclusion

The scalability in sub-micrometer range and the reproducibility of the high current density RTD have been proven. The splitting of the RTD mesa area can be used to reduce the series resistance, which is an important factor of its speed performance. This study shows that RTDs are ready for use in very large scale integrated high speed circuits and may contribute to the development of future nanoelectronic circuits.

V. Acknowledgement

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A Traveling Wave Amplifier Based on Composite Right/Left Handed (CRLH) Transmission Lines Periodically Loaded with Resonant Tunneling Diode Pairs

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Abstract This paper proposes a traveling wave amplifier based on composite right/left handed (CRLH) transmission lines (TLs) periodically loaded with resonant tunneling diode (RTD) pairs. This TL can be regarded as a "lossy" TL with a negative loss because of the negative differential resistance of the RTD. This means that the TL can amplify signals while the signal travels along the line. One of the most important points to be investigated to realize this amplifier is the stability of the circuit. We discuss stability of the TLs periodically loaded with RTDs, and show that they can be stabilized by using CRLH TL configuration. It is demonstrated that this amplifier can have a gain for wide frequency range.

I. Introduction

Resonant tunneling diodes (RTDs) are promising quantum effect devices. Their negative differential resistance (NDR) has been demonstrated to persist up to the THz frequency range. Various applications, including analog and digital circuits, have been proposed and demonstrated using RTDs.

Recently we have proposed ultrahigh frequency traveling wave amplifiers based on active transmission lines (TLs) periodically loaded with resonant tunneling diode pairs (1). These TLs can be regarded as an conventional "lossy" transmission lines. The point is that the loss of the circuit can be negative when the RTDs are biased in the negative differential resistance region. In other words, this transmission line works as an amplifier. Owing to the ultrahigh-frequency operation of the RTDs, this amplifier is promising for THz frequency signal amplification.

One of the most important points to be investigated to realize this type of amplifier is the stability of the circuit. In this paper, we will discuss stability of the TLs periodically loaded with RTD pairs, and show that they can be stabilized by using Composite Right/Left Handed (CRLH) TL configuration. It is also demonstrated that this amplifier can have a gain for wide frequency range.

II. Active Transmission Lines Loaded with RTD Pairs

In general, negative-resistance devices can be used as amplifiers. Amplifiers based on the NDR of tunnel diodes were studied for microwave applications after its invention. The negative resistance in RTD pairs is promising for THz signal amplification owing to the high maximum frequency of oscillation. Such amplifiers need a circulator for proper signal transmission because the devices have only two terminals. Input/output isolation is impossible without it. However, in the frequency range that we are interested in (higher than 100 GHz), conventional circulators used for micro/millimeter wave applications have difficulty functioning. Optical isolators are also difficult to apply in this frequency range. To overcome these problems, we propose the application of the distributed amplifier concept with small RTD pairs for a gain unit.

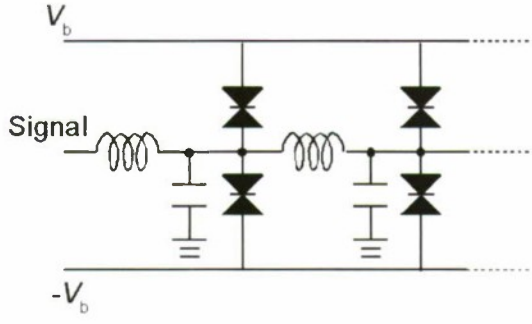

Fig. 1 Basic configuration of the active TLs periodically loaded with RTD pairs.

Figure 1 shows the basic configuration of the proposed circuits. We employ an RTD pair (2) instead of a single RTD, because the RTD pair has improved linearity than that of a single RTD. The RTD pair consists of two RTDs connected serially and is biased by voltages of the same absolute value with opposite signs (see the inset in Fig. 2). The RTD pair has unique current–voltage characteristics at the intermediate node as shown in Fig. 2; the true negative resistance appears in the low-voltage region. The linearity of this region is good owing to the symmetry of the circuit. In addition, the RTD pair circuit can be stabilized more easily than that of a single RTD.

This circuit consists of only two-terminal devices and is symmetric regarding the input and output ports. Therefore, the

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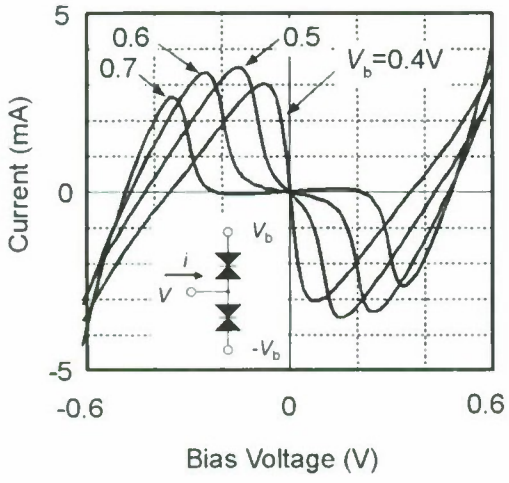

Fig. 2 *I-V* characteristics of the RTD pair.

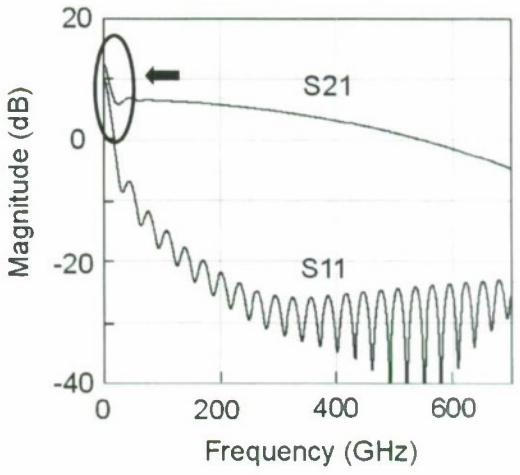

Fig. 3 Example of the simulation results. Gain (*S*21) and reflection (S11) are shown. At the low frequencies both S21 and S11 exceeds 0dB, which can make the circuit unstable.

S-parameters are also symmetric, i.e.,

$$S11 = S22$$

$$S21 = S12.$$

This means that the realization of the absolute stable condition regardless of the variations in input and load impedances is impossible for this type of circuits. Instead, we studied the stability of the circuit with standard 50 Ω impedance connected to the input and output terminals. If we can design the circuit with a small reflection coefficient and a sufficient gain, it can be used as an amplifier. Impedance matching should be satisfied to realize this condition. Although it is impossible to fulfill the wide-band impedance matching, the reflection coefficient can be satisfactorily small if the absolute value of the conductance per unit length is small. The transmission line must be sufficiently long to obtain a required gain.

With this concept RF signal amplification was demonstrated by circuit simulation in reference (1). Figure 3 shows an example of the simulation results. It shows the *S*21 and the *S*11 of the circuit as a function of the input signal frequency. As shown in the figure, a positive *S*21 of approximately 6 dB was obtained in a wide frequency range. Moreover, *S*11 was less than -10 dB in the wide frequency range. These results indicate that the RTD pair transmission line can be used as a high-frequency amplifier. The cutoff frequency depends on the unit cell size, and it is expected to exceed 1 THz with RTDs of 1 μm^2 emitter area.

III. Stabilization of the TLs loaded with RTD pairs

There remains some difficult problems; bias instability and self-oscillation. First, the RTDs must be biased in the NDR region for the proper operation. This is impossible if the total (negative) conductance of RTDs used in the circuit is larger than the some of the input and load conductances. The TLs can be

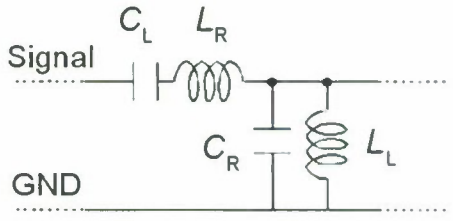

Fig. 4 Unit cell of the composite right/left handed transmission lines (CRLH-TLs).

regarded as a single negative resistor, whose conductance is a some of RTD pair's conductances at a low frequency limit. Therefore, the total (negative) conductance is limited to be less than 40mS (=1/50 x 2 mS) for 50-Ω system, which restricts the gain of the circuit less than around 6 dB. Next, spurious oscillation can occur at the frequency where the magnitude of the product *S*11 and *S*21 is larger than unity. For example, spurious oscillation can occur at very low frequencies indicated by arrows in Fig. 3. To solve these problems we employ CRLH TL configuration.

The CRLH TLs have been attracting much attention for the micro/millimeter wave passive component researchers (3). The CRLH-TLs have capacitors in the signal line, and inductors between the signal line and the ground together with the inductors and capacitors in the conventional TLs, as shown in the Fig. 4. A point is that it has two branches in the dispersion (ω-β) relation as shown in Fig. 5. The lower frequency branch is the left-handed branch based on L_L's and C_L's, where the phase

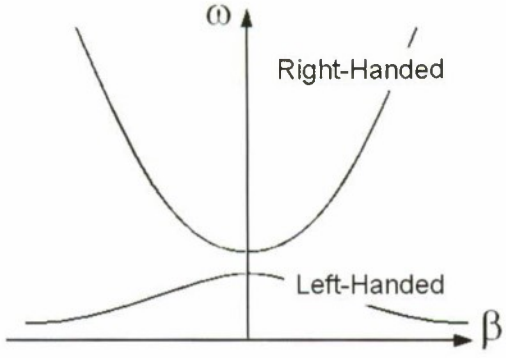

Fig. 5 Dispersion curve of the composite right/left handed transmission lines.

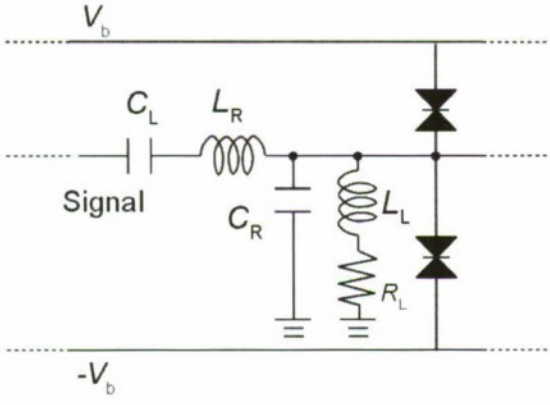

Fig. 6 Unit cell of the CRLH-TLs periodically loaded with RTD pairs.

velocity and group velocity have opposite signs. The upper branch is the ordinary right handed branch based on L_R's and C_R's.

We intentionally introduce losses in the left-handed branch by inserting a resistor between the inductor L_L's and the ground as shown in Fig. 6. This lowers the gain at the low frequencies while maintains high frequency gain. Moreover, the RTD pairs can be easily biased in the NDR region due to the existence of L_L's.

IV. Simulation Results

We carried out circuit simulations using Agilent ADS to demonstrate the signal amplification in the CRLH TLs loaded with RTD pairs. A simple RTD model consisting of a voltage-controlled current source and a capacitor connected in parallel was used in the simulations. The voltage-controlled current

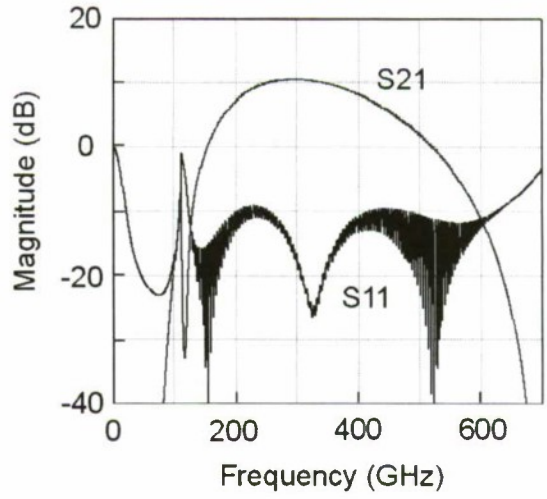

Fig. 7 Example of the simulation results for the CRLH-TLs periodically loaded with RTD pairs. Gain ($S21$) and reflection ($S11$) are shown.

Table 1 Parameters used in the Simulation

C_R (fF)	5.5
C_L (fF)	80
L_R (pH)	25
L_L (pH)	200
R_L (Ω)	20
R_S (Ω)	2.7
RTD Area (μm²)	1.5

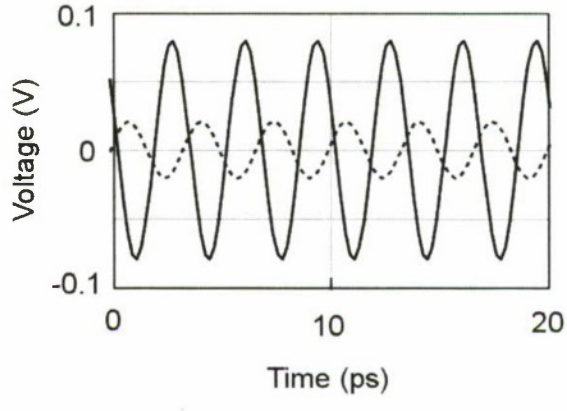

Fig. 8 Input and output waveform of the CRLH-TLs periodically loaded with RTD pairs when 300 GHz sine wave signal is fed into the circuit (Simulation result). Solid and dashed lines are the output and input waveforms, respectively.

source is based on the model of Schulman et al (4). A series resistance was also included. The parameters used for the RTD current source were the same as those shown in the reference 1, which reproduce the *I-V* curve of the RTD grown on InP substrates.

Figure 7 shows an example of the simulation results for CRLH-TLs periodically loaded with RTD pairs. The parameters used are shown in Table 1. The circuit consists of 160 unit cells. Positive *S*21 of approximately 10 dB is obtained with a low *S*11 of -10 dB or lower in a wide frequency range. A most important feature is that there is no frequency where |*S*11*S*21| is larger than unity. Consequently, the circuit is stable.

Figure 8 shows the input and output waveforms of the circuit obtained by the simulation when sinusoidal signal of 300 GHz frequency is fed. Clear amplification of about 10 dB can be seen.

These results demonstrate the possibility of the ultra wide band amplifier based on TLs periodically loaded with RTD pairs.

V. Summary

In this paper we proposed a traveling wave amplifier based on composite right/left handed transmission lines periodically loaded with resonant tunneling diode pairs. We discussed stability of the TLs loaded with RTDs, and showed that they can be stabilized by using CRLH TL configuration. It was demonstrated that this amplifier can have a gain for wide frequency range.

Acknowledgments

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AIR-GAP CAPACITANCE-VOLTAGE ANALYSIS OF P-INP SURFACES

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A novel air-gap capacitance-Voltage (C-V) method is introduced. This method is powerful tool for characterizing electrical properties of "free" or ultrathin-insulator-covered surfaces for III-V semiconductors. Air-gap C-V characteristics of p-InP surfaces with and without natural oxide are reported for the first time. Unexpectedly, the surface with natural oxide gives relatively low-density surface states. Surfaces covered with ultrathin Al_2O_3 film were also measured, indicating the importance for further investigation and optimization of surface process.

I. INTRODUCTION

III-V semiconductors have recently been recognized as candidates for realizing high-mobility n-channel metal-oxide-semiconductor (MOS) field-effect-transistors (FETs) on the Si platform.[1-3] It is very important to characterize p-type semiconductor surfaces for controlling MOS interfaces in inversion n-channel FETs. P-type InP/Al_2O_3 is one of considerable structure,[4] because of the high electron mobility and the large energy gap for InP as well as the high dielectric constant and the chemical stability for Al_2O_3. However, only a few reports indicate results focusing on the electric properties of this structure,[5,6] thus, further investigation is required.

In this paper, we applied the air-gap capacitance-voltage (C-V) technique to p-InP surfaces for the first time. Furthermore, p-InP surfaces covered with ultrathin Al_2O_3 layer (3nm) by atomic layer deposition (ALD) were characterized.

II. AIR-GAP CAPACITANCE-VOLTAGE METHOD

The schematic view of the air-gap C-V measurement system[7] is shown in Fig. 1 (a). In this system, instead of depositing a gate electrode onto the sample surface directly, C-V measurements are performed from the field electrode that is separated from the sample surface by a thin "air gap" (about 300 nm). Thus, considering the air-gap as a part of insulator, the C-V analysis of "free" surfaces or ultrathin insulator covered surfaces

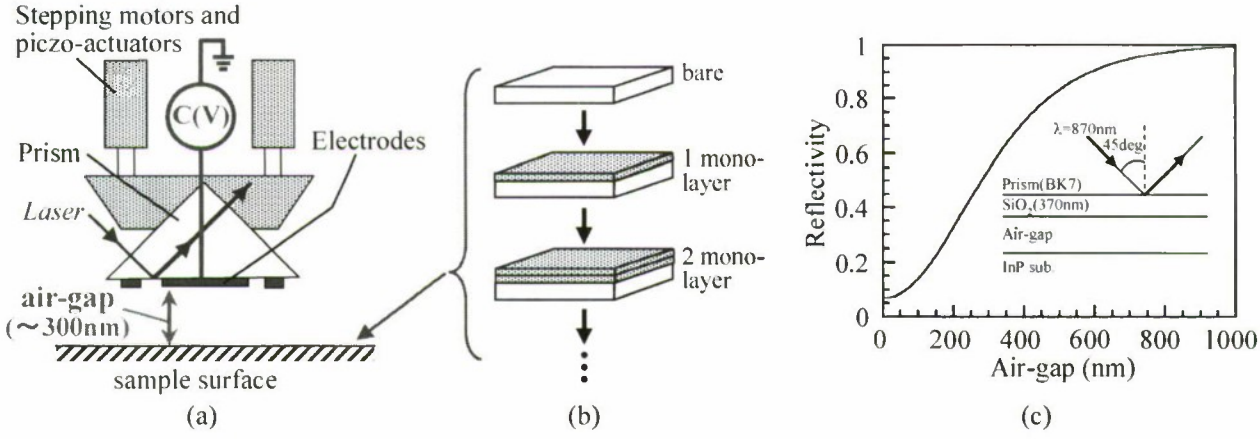

Fig. 1 (a) Schematic view of the air-gap C-V measurement system. (b) Traceability of C-V behavior in each step of monolayer growth of insulators. (b) Calculated reflectivity as a function of the air-gap distance for bare InP surface.

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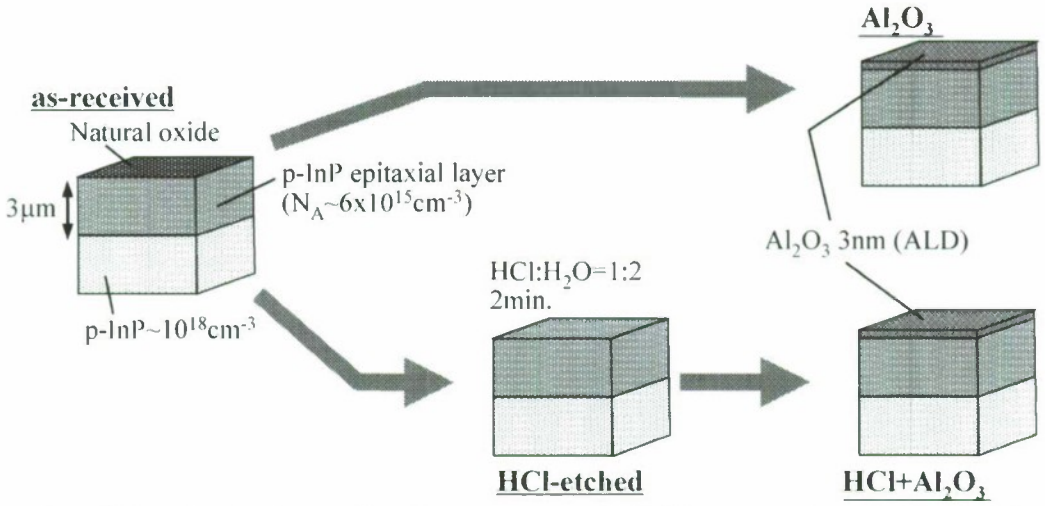

Fig. 2 Sample structure and surface processes. Al_2O_3 films were deposited by ALD technique with and without HCl-etching of natural oxide. Abbreviations are also shown; *as-received, HCl-etched, Al_2O_3 and HCl+Al_2O_3.*

becomes possible, without suffering from leakage current and generation of damages by metal deposition processes. Further applicable feature to investigating the interface formation mechanism is also shown in Fig. 1 (b). Because of the non-destructive style of C-V measurement, the variation of surface/ interface behavior can be traced using same sample in each step of monolayer growth of insulators and/or surface modification process such as dry processes.

The air-gap distance was optically determined by the variation of reflectivity of laser beam. The calculated reflectivity as a function of the air-gap distance for bare InP substrate is shown in Fig. 1 (c).

The area of the measurement electrode is 7.5 x 10^{-3} cm^{-2}.

III. EXPERIMENTAL PROCEDURE

Sample structures and surface processes are schematically shown in Fig. 2. We used p-InP epitaxial layers (N_A ~ 6x10^{15}cm^{-3}, 3μm) grown on p$^+$-InP substrate ("*as-received*" sample). One surface was immersed in dilute HCl solution (HCl : H_2O = 1 : 2) for 2 min to remove natural oxide ("*HCl-etched*" sample). Then the ultrathin Al_2O_3 layer (3 nm) was deposited on the "*as-received*" and "*HCl-etched*" surfaces using ALD module (Savannah S100, Cambridge NanoTech Inc.). For the ALD process, the alternately pulsed chemical precursors of H_2O (the oxygen precursor) and trimethylaluminium (TMA, the Al precursor) in a carrier nitrogen gas flow was used, and the sample temperature was 300 °C.

IV. RESULTS AND DISCUSSIONS

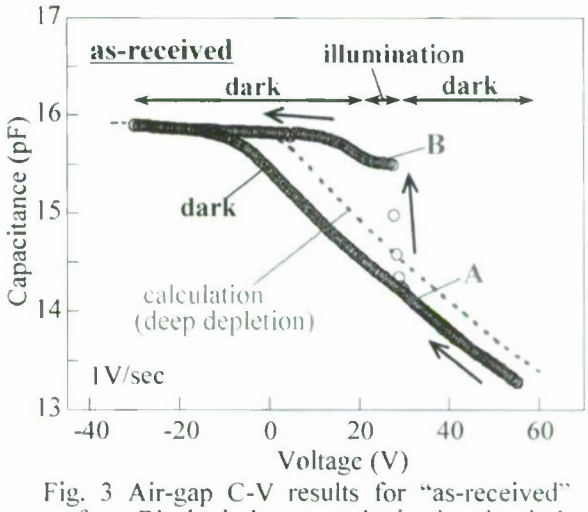

Fig. 3 Air-gap C-V results for "as-received" surface. Black circles were obtained under dark condition in whole biasing. Blue circles were obtained with illumination of a white light. Calculated capacitance behavior in deep depletion condition is also shown in dashed line.

Air-gap C-V characteristics of "*as-received*" surface is shown in Fig. 3. Under the dark condition, a large capacitance variation was observed (black circles), indicating deep-depletion behavior. In order to investigate the minority carrier response, the sample surface was illuminated by white light at the bias point A, as shown in Fig. 3. An increase in capacitance was clearly observed, and it was kept at the increased capacitance value even after switching off the light. Figure 4 shows calculated potentials from the capacitance values before and under illumination. In dark condition, the deep-depletion behavior was confirmed, whereas near inversion behavior was expected at point B due to electron accumulation at the

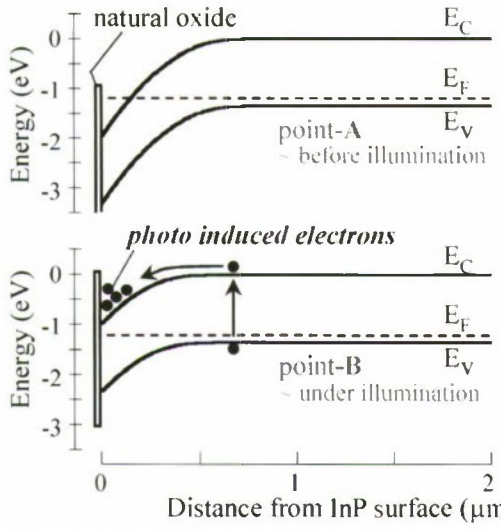

Fig. 4 Calculated band diagrams before and under illumination. Point A and B are bias points in Fig. 3, and the former is before illumination and the latter is under illumination, respectively.

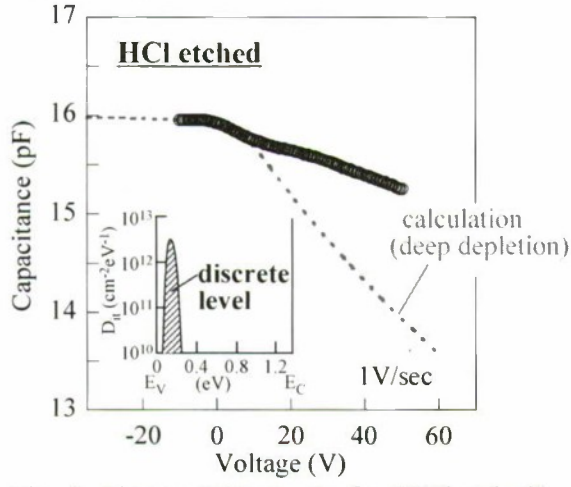

Fig. 5 Air-gap C-V results for "HCl-etched" surface. Limited capacitance variation was observed, which indicated the existence of high density of surface states as shown in the inset.

surface generated by illumination. For further investigation, air-gap C-V measurement under illumination using light with the wave length of 1000 nm, i.e. 1.24 eV < $E_{G\text{-}InP}$, was carried out (not shown here). A little increase of capacitance value was observed. These results indicate, unexpectedly, a relatively low-density surface states at the *"as-received"* p-InP surface covered with natural oxide.

On the other hand, the "*HCl-etched*" surface showed a limited capacitance variation shown in Fig. 5. The C-V slope decreased, as compared to the "*as-received*" surface. A more detailed analysis predicted the existence of a discrete surface level near E_V, as shown in the inset of Fig.5, indicating that the HCl treatment

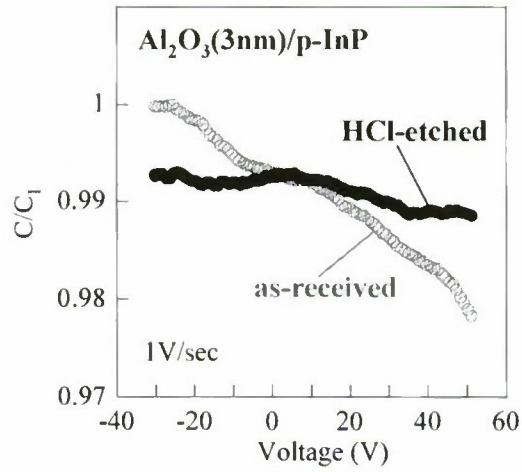

Fig. 6 Air-gap C-V results for p-InP surfaces after Al_2O_3 (3nm) deposition by ALD technique with and without HCl etching of natural oxide.

can induce some kinds of surface defects.

Figure 6 shows the air-gap C-V results on the Al_2O_3 (3nm)/p-InP structures. Both samples showed a limited capacitance variation, indicating that the surface state density increased in the initial stage of the ALD deposition of Al_2O_3. In particular, a strong Fermi level pinning was observed at the MOS interface fabricated on the HCl-etched p-InP. For controlling InP MOS interfaces, further investigation on a suitable surface process and correlation between interface states and an initial deposition condition are needed. Thus, the present air-gap C-V method is powerful tool for characterizing electrical properties of "free" or ultrathin-insulator-covered surfaces.

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THz Generation Based on Gunn Oscillations in GaN Planar Asymmetric Nanodiodes

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Abstract

By means of Monte Carlo simulations we show the feasibility of asymmetric nonlinear planar GaN nanodiodes for the development of Gunn oscillations. For channel lengths about 1 μm, oscillation frequencies around 400 GHz are predicted, reaching more than 600 GHz for 0.5 μm. The DC to AC conversion efficiency is found to be higher than 1% for the fundamental and second harmonic frequencies in GaN diodes. By simulating two diodes in parallel, we analyze the possible loss of efficiency due to the technological dispersion in channel lengths.

I. Introduction

Gunn oscillations in semiconductor diodes are typically used to produce microwave emitters. Increasing the oscillation frequency to enter the THz range is a challenging issue. Materials exhibiting negative differential mobility and high saturation velocity, like GaN, are appropriate to this end. Despite big efforts performed in the last years (1-3), continuous wave Gunn oscillations have not been experimentally observed in GaN diodes yet. Mainly vertical structures were explored so far, with little success. In this work we propose a different approach: the use of parallel arrays of planar asymmetric nanodiodes, so called self-switching diodes (SSDs) (4). The asymmetry in the channel of SSDs (geometry shown in Fig. 1) is especially appropriate for the development of Gunn oscillations (5). Heat dissipation, a technological challenge in GaN Gunn diodes, could be managed in an efficient way by a correct design of the channels and their separation thanks to their planar topology.

In this work, by means of Monte Carlo (MC) simulations, the feasibility of GaN SSDs for THz generation based on Gunn oscillations is demonstrated. The oscillation efficiency as a function of frequency is calculated. Our results indicate that oscillations at frequencies of several hundreds of GHz can be achieved with acceptable efficiencies, higher than 1%. The loss of efficiency associated with the dispersion in channel length originated in the fabrication processes is also analyzed.

II. Model Description

A semiclassical MC simulator self-consistently coupled with a 2D Poisson solver is used for the analysis. To account for the 3D nature of the diodes, a *background doping* N_{Db}=2x10^{17} cm^{-3} is considered when solving Poisson equation and a charge density σ=-0.2x10^{12} cm^{-2} is placed at the semiconductor-dielectric boundaries of the insulating trenches. Details about the model can be found in (6,7).

The non-simulated dimension Z, which allows to determine the value of the current provided by a single SSD, is estimated as $Z=n_s/N_{Db}$, taking a value 4x10^{-5} cm for n_s=8x10^{12} cm^{-2}, typical value of sheet electron density in GaN channels. All the simulations are performed at room temperature.

III. Simulated structures

We have analyzed three different structures, depicted in Fig. 2: (i) a single diode with channel length L = 900 nm and width W = 75 nm; (ii) two identical diodes placed in parallel, separated 400 nm (double symmetric structure), to check if the interaction between close channels has an influence on the oscillations; and (iii) two diodes with different channel length (900 and 900+d nm, for d=100, 200 and 300 nm) placed in parallel (douhle asymmetric structure), separated 400 nm, to detect the possible loss of efficiency originated by the dispersion in the device dimensions associated to the technological fabrication processes. The width of the vertical trenches W_v is considered to be 100 nm, while that of the horizontal trenches W_h is 50 nm. The performance of the single diode with varying L, W and W_h will also be analyzed.

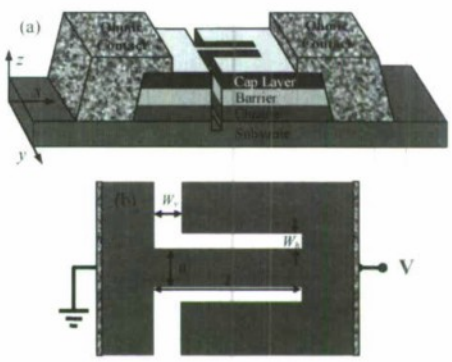

Fig. 1. (a) Three-dimensional topology of the SSD. (b) Top view of the device in the xy plane. The SSD is fabricated with just one lithographic step, by simply etching L-shaped insulating grooves onto a semiconductor layer to define a narrow channel with broken symmetry.

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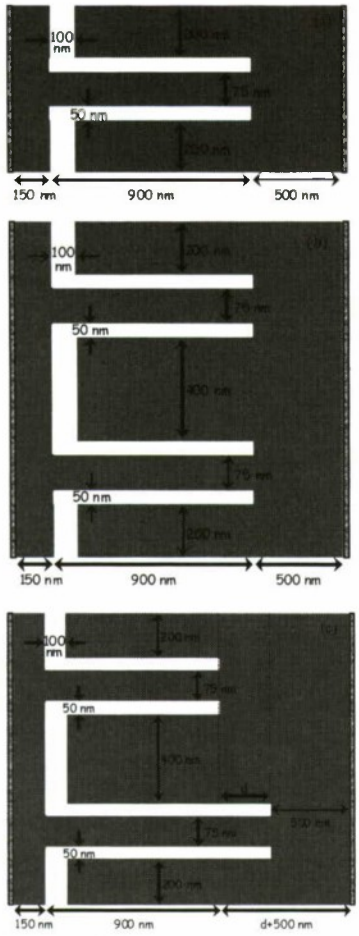

Fig. 2. Geometry of the GaN structures under analysis. (a) Single diode, (b) double symmetric structure, and (c) double asymmetric structure.

IV. Results

Fig. 3 shows the rectifying *I-V* curves obtained for the three structures. As expected, the double-diode structures provide practically the same current, twice the value obtained in the single diode. The rectifying behaviour is due to electrostatic

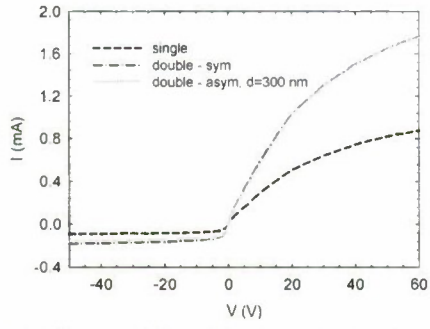

Fig. 3. I-V characteristics of the GaN simulated structures.

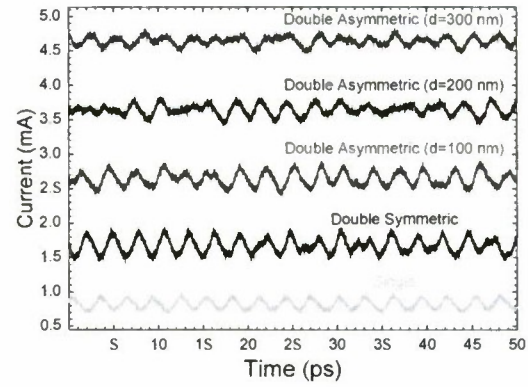

Fig. 4. Current sequences calculated in the different diodes for an applied voltage of 50 V. The current in each of the double asymmetric diodes is displaced 1 mA with respect to the previous one in order to be clearly distinguished.

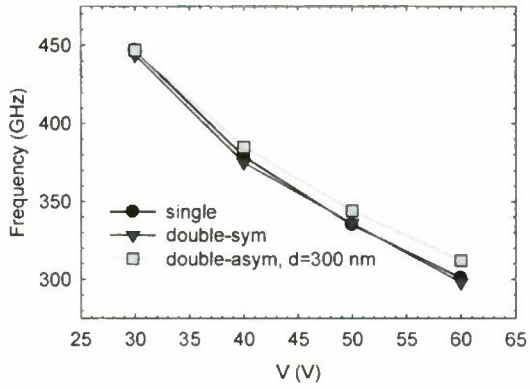

Fig. 5. Frequency of the oscillation observed in the current as a function of the applied DC voltage for the simulated diodes.

effects caused by the asymmetry of the geometry (8). When the DC bias exceeds 30 V, current oscillations appear, as observed in the time sequences of Fig. 4, calculated at an applied voltage of 50 V. The oscillations are caused by a high-field domain shifting along the channel, coinciding with an accumulation of slow electrons in the upper U-valley. As will be illustrated later, the domain is originated at the entrance of the channel, where the electric field takes high values due to the presence of the vertical trench. This feature of the SSDs architecture is especially appropriate for the development of the Gunn oscillations. The main frequency of the oscillations found in the current under DC bias is shown in Fig. 5 as a function of the applied voltage. Frequencies around 400 GHz are obtained, decreasing for higher bias due to a lower electron drift velocity.

To evaluate the DC to AC conversion efficiency ($\eta=P_{AC}/P_{DC}$) a standard procedure is used (9): a single-tone sinusoidal potential with amplitude V_{AC} is superimposed to a DC bias V_{DC}. Under such conditions, the dissipated DC power P_{DC} and the

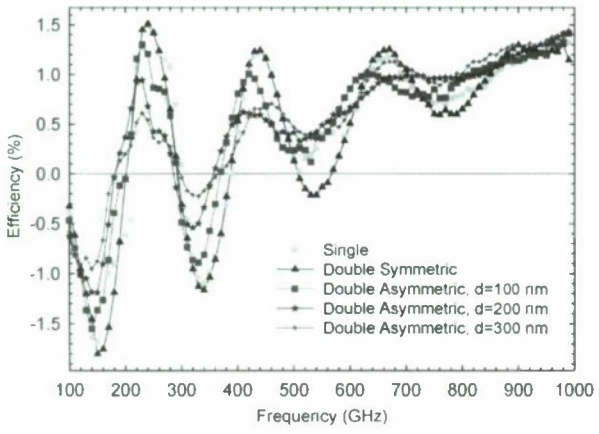

Fig. 6. DC to AC conversion efficiency η as a function of frequency for the different diodes under analysis.

time-average AC power P_{AC} are evaluated. Positive values of η correspond to resistive behavior of the diode, while negative values of η indicate AC generation from DC. For the calculations we consider V_{DC}=50 V and V_{AC}=10 V. Fig. 6 shows η as a function of the frequency of the AC excitation for the different structures under analysis. Negative values higher than 1% are achieved in the single and double symmetric structure at the frequency of the oscillation taking place when only the DC bias is present (340 GHz) and, surprisingly, also at half such a frequency. The double symmetric structure, by coupling the oscillations in both diodes, enhances the efficiency at higher frequencies (negative values around 540 GHz), while the dispersion in channel lengths originates a significant loss of efficiency for d higher than 100 nm.

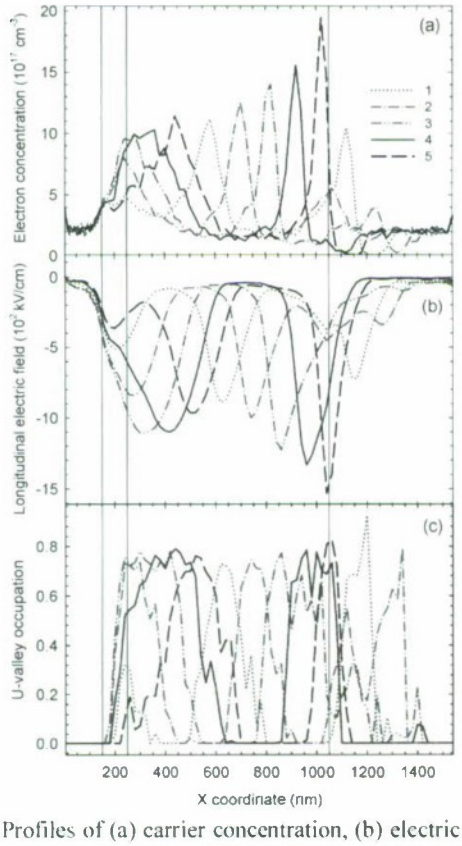

Fig. 7. Profiles of (a) carrier concentration, (b) electric field and (c) U-valley occupation along the center of the channel for V_{DC}=50 V, V_{AC}=10 V and f=340 GHz at five equidistant time moments during one period of the excitation. Vertical lines indicate the position of the vertical trench and the end of the channel.

To identify the origin of the oscillations, Fig. 7 shows profiles of several microscopic quantities along the center of the channel in the case of the single diode obtained at different time moments during one period of the AC signal for f=340 GHz. As observed, high-field domains shift along the channel, coinciding with accumulations of slow electrons in the upper U-valley. The accumulations are originated at the entrance of the channel, where the electric field takes high values due to the presence of the vertical trench. As already mentioned, this feature of the SSD geometry is especially appropriate for the development of the Gunn oscillations. At this particular frequency, two domains coexist in the structure, which indicates that the oscillations observed under DC bias, taking place at 340 GHz for 50 V (Fig. 5), correspond to the second harmonic of the fundamental frequency of the diode. Indeed, the high efficiency observed in Fig. 6 at around 150 GHz corresponds to the presence of just one domain in the diode (fundamental frequency), which, in addition to the DC bias, requires an external AC component to be excited.

To analyze which is the influence of the geometry of the diode on the oscillation performance, Fig. 8 shows the DC to AC conversion efficiency for the case of the single diode when (a) the channel length L, (b) the channel width W and (c) the width of the horizontal trench W_h are modified. In all cases V_{DC}=50 V, V_{AC}=10 V. As observed, by decreasing the length of the channel, the frequency of the oscillations increases. For L=0.5 μm, the oscillations reach frequencies around 600 GHz. While the efficiency at the fundamental frequency does not change significantly with L, at the second harmonic it decreases for lower L. The results in Fig. 8(b) indicate that the efficiency of the oscillations increases in narrower channels, while the frequency slightly decreases. Indeed, gain at the third harmonic is only present for W lower than 75 nm. However, by reducing W, the current level decreases, and also the delivered AC power. Finally, when modifying the width of the horizontal trench W_h [Fig. 8(c)], η decreases for lower W_h, except around the third harmonic, for which only the stronger control of the channel electron density achieved by a narrow trench allows the presence of oscillations.

V. Conclusions

By means of MC simulations, the suitability of planar asymmetric nanodiodes for the development of Gunn oscillations in GaN has been demonstrated. Oscillations at frequencies of

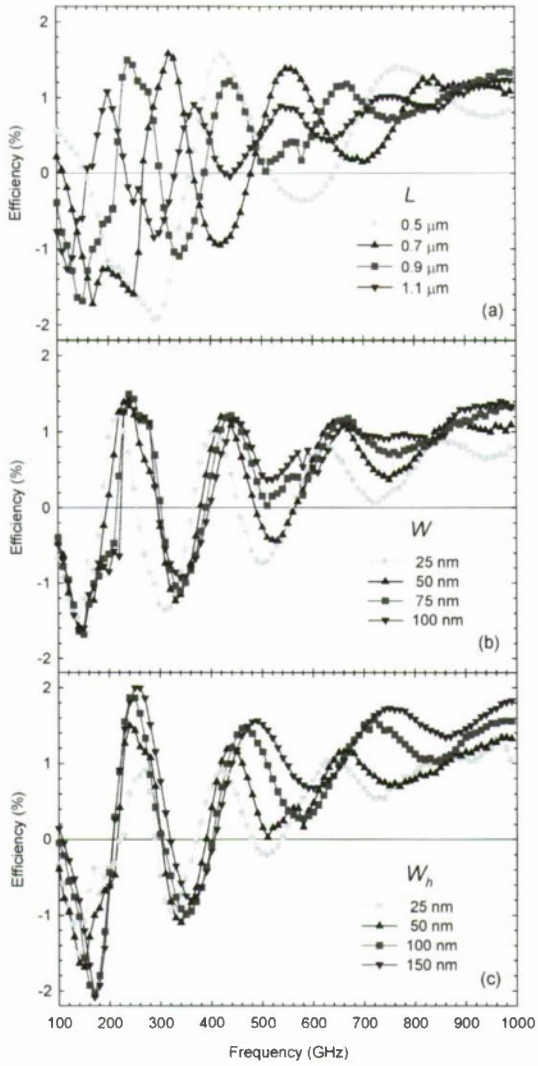

Fig. 8. DC to AC conversion efficiency η as a function of frequency in the case of the single diode of Fig. 2(a) for several values of: (a) channel length, (b) channel width and (c) width of the horizontal trenches.

several hundreds of GHz can be achieved with efficiencies higher than 1%. Moreover, arrays of SSDs in parallel can provide levels of current high enough for applications. Attention must be paid to the dispersion in channel lengths to avoid losses of efficiency. By reducing the channel length to 0.5 μm, frequencies in excess of 600 GHz can be reached.

Acknowledgments

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InAs/InGaAsP/InP(001) Nanostructures: A Cross-Sectional Scanning Tunneling Microscopy Study

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Room-Temperature Operation Type-II GaSb/GaAs Quantum-Dot Infrared Light-Emitting Diode

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Abstract

A GaSb/GaAs quantum-dot light-emitting diode (QD LED) with a single GaSb QD layer is investigated in this paper. The room-temperature photoluminescence peak blue shift with increasing excitation power densities suggests a type-II alignment of the GaSb/GaAs hetero-structures. Significant electroluminescence is observed for the device under forward biases, which suggests that pronounced dipole transitions occur at the GaSb/GaAs interfaces. With increasing forward biases, the observed EL peak blue shift confirms that the origin of luminescence is from the type-II GaSb/GaAs QD structures.

I. Introduction

Two possible transition mechanisms are adopted for Optoelectronic devices based on the InAs/GaAs quantum-dot (QD) structures, which are (a) inter-band and (b) intra-band transitions in the QD structures. The representative device for the inter-band transition is the near infrared QD laser diode (LD), while quantum-dot infrared photodetectors (QDIPs) is for the intra-band transition [1]-[4]. Although great performances have already been observed for the two devices, difficulties like longer emitting wavelengths up to 1.55 μm and 3-5 μm detections are still remained for QD LDs and QDIPs, respectively. For the long-wavelength QD LDs, attempts like InGaAs capping layers grown after InAs QDs and Sb-incorporation in the capping layers are already demonstrated [5], [6]. Although enhanced emitting wavelengths are obtained for these structures, reliable device performances are still unavailable. The main reason responsible for the emitting wavelength limitation of QD LDs is the limited choice of barriers like GaAs and InGaAs layers. Therefore, a different material system with the capacity of fabricating QD structures with high optical qualities on the GaAs substrates may provide an alternate solution to this problem. In previous reports, despite its type-II alignment, photoluminescence (PL) has already been observed for GaSb/GaAs QDs [7], [8]. The application of QD memories has also been demonstrated [9]. The main advantage of the GaSb QD structure is the wide barrier choice from GaAs to GaAsSb and even InGaP. The choice of different barriers may provide different emitting wavelengths for the devices based on this QD structure.

II. Material Growth and Layer Structure Design

The GaSb QD LED sample discussed in this paper is prepared by Riber Compact 21 solid-source molecular beam epitaxy (MBE) system. With (100)-oriented semi-insulating GaAs substrate, a single 3.0 mono-layer (ML) GaSb QD layer are embedded in the GaAs n-i-p structure. The growth procedure for the sample is (a) a 300 nm GaAs bottom contact layer p-type dopped to 2×10^{18} cm^{-3} grown at 580 °C, (b) a 200 nm undoped GaAs layer grown at 580 °C, (c) a 3.0 ML GaSb QD layer grown at 490 °C with V/III ratio ~ 1.3, (d) a 200 nm undoped GaAs layer grown at 580 °C and (e) a 300 nm GaAs top contact layer n-type dopped to 2×10^{18} cm^{-3} grown at 580 °C.

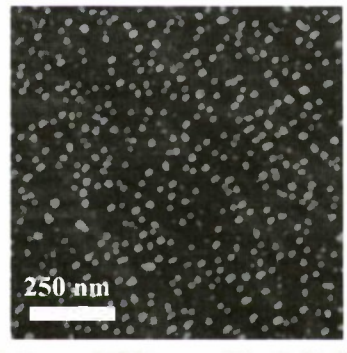

Fig. 1. The 1x1 μm AFM image of the GaSb QDs.

Since severe As/Sb exchange at the GaSb/GaAs interfaces has been reported elsewhere, Sb soaking procedures before and after

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GaSb QD growth are neeessary to proteet the GaSb QD strueture [10], [11]. The pre- and post- Sb soaking times adopted for the sample are 15 and 120 sec., respectively. Standard photolithography and wet chemical etching are adopted to fabrieate the devices with 450 × 630 μm2 mesas. For light extraction, grid top contaet is adopted. The positive and negative biases of the measurements are defined aecording to the voltages applied to the top contact of the deviees. The Keithley 6487 system is adopted to measure current-voltage (I-V) charaeteristies and aets as the voltage source. The PL and EL speetrums are observed by using Jobin Yvon's NanoLog3 system eoupled with a He-Ne laser as the pumping souree.

III. Results and Discussion

The room-temperature PL spectrums of the sample measured under different pumping power densities 0.95, 0.78, 0.59 and 0.38 W/em^2 are shown in Fig. 2. As shown in the figure, with inereasing pumping power densities, the PL peak would shift from 1.08 to 1.10 eV. The PL peak blue shift with increasing pumping powers is frequently observed for type-II hetero-struetures [12]. Due to the spatial separation of eleetron/hole eonfinements of the type-II GaSb/GaAs QDs, the aecumulation of electron/hole at the GaAs/GaSb interfaces with inereasing pumping power densities would steepen the interface band bending. In this ease, upraised confinement states in the GaAs triangular wells would result in a PL peak blue shift as shown in Fig. 2. Compared with other reports, the higher PL peak energies observed in Fig. 2 are attributed to the much larger pumping power density of the PL system compared with traditional PL systems [12].

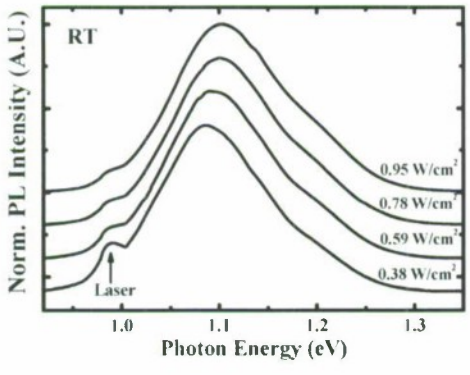
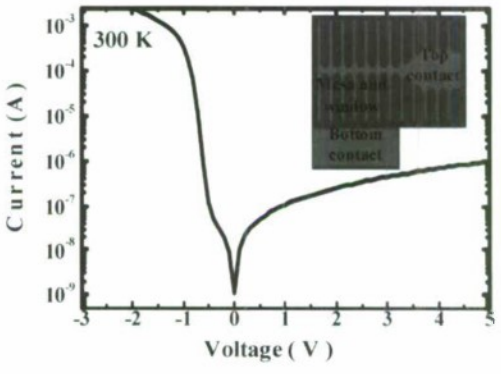
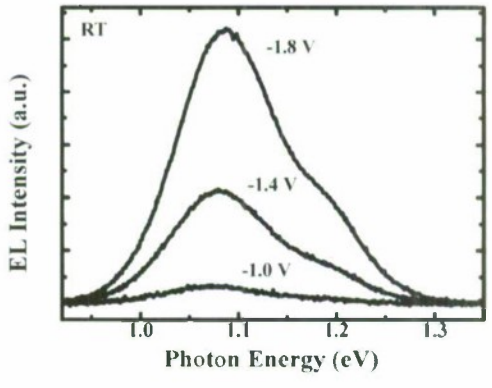


Fig. 2. The room-temperature PL speetrums of the sample measured under different pumping power densities 0.95, 0.78, 0.59 and 0.38 W/cm^2, respectively.

The I-V characteristics of the device at room temperature are shown in Fig. 2 (a). The insert in the figure shows the top view of the device. Since the device is of n-i-p struetures, the device will turn on under negative applied voltages. As shown in the figure, the leakage currents of the device under reverse biases are below 10^{-6} A, which suggests a good P-N junction is obtained. The turn-on voltage of the device is at -0.8 V. The room-temperature EL speetrums of the deviee under -1.8, -1.4 and -1.0 V are shown in Fig. 3 (b). For applied voltages lower than -1.0 V, no luminesceenee is observed for the deviee. Considering the turn-on voltage of the deviee is at -0.8 V, the results suggest that as long as the device turns on, optical recombination would take place immediately. The EL peaks of the deviee under -1.0, -1.4 and -1.8 V shown in Fig. 3 (b) are 1.072, 1.079 and 1.088 eV, respectively. The blue shift of the EL peaks with increasing forward biases suggests that the similar mechanism with the excitation-power-increasing PL would also take place with increasing electrical carrier injection. The results indicate that a type-II EL is observed for the deviee. Also observed in Fig. 3 (b) are the eloser peak energies with the PL peaks reported at other papers [12].



(a)



(b)

Fig. 3. (a) The I-V charaeteristics and (b) the (~300 K) room-temperature EL speetrums at -1.0, -1.4 and -1.8 V of the deviee.

IV. Conclusions

In eonelusion, a single GaSb QD layer with optimized growth eonditions is inserted in a GaAs n-i-p diode structure. Significant electroluminesceenee (EL) is observed for the device under forward biases, whieh suggests that pronounced dipole

transitions occur at the GaSb/GaAs interfaces. With increasing forward biases, the observed EL peak blue shift confirms that the origin of luminescence is from the type-II GaSb/GaAs QD structures. The wide barrier choices from GaAs, GaAsSb to InGaP of this material system have provided an alternate approach for infrared light-emitting devices.

Acknowledgments

This work was supported in part by the National Science Council, Taiwan under grant numbers NSC 98-2221-E-001-001 and NSC 99-2911-I-001-010.

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Optical characterization of InGaAsP/InAlAsP multiple quantum wells grown by MBE for 1 μm wavelength region

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Abstract

. InGaAsP/InAlAsP multiple quantum wells (MQWs) for 1 μm wavelength region optical modulators were proposed and were grown by molecular beam epitaxy (MBE). Optical properties, such as photoluminescence and optical absorption of InAlAsP layers, InGaAs/InAlAsP MQW layers and InGaAsP/InAlAsP MQW layers were studied in detail. A clear absorption edge was observed at about 1.06 μm for InGaAsP/InAlAsP MQW layers.

I. Introduction

The 1 μm band is very attractive for the optical fiber communication, because we can use ytterbium doped fiber amplifiers (YDFA) [1]. Also, YAG lasers operating at 1.06 μm are very important in various fields. An optical modulator using quantum confined Stark effect (QCSE) in the 1 μm wavelength region was reported by using strained InGaAs quantum wells grown on GaAs substrates [2]. However, the large lattice-mismatch related to GaAs substrates degrades the crystal quality of the epitaxial layers. In this paper, we propose InGaAsP/InAlAsP multiple quantum well (MQW) optical modulators for 1 μm wavelength region lattice-matched to InP, and report characterization of optical properties of InAlAsP layers and InGaAsP/InAlAsP MQW layers.

II. Experimentals

The epitaxial layers studied here were grown by molecular beam epitaxy (MBE) on Fe-doped (100) InP substrates. The growth temperature was 500°C, which was monitored by a calibrated infrared pyrometer. Prior to the growth, the InP substrate surface was thermally cleaned at 515°C under P vapor pressure. In, Ga and Al metals were used for group III beam sources, while As_2 and P_2 were used for group V beam sources. The growth rates of InP were 1.2μm/h and those of InGaAsP and InAlAsP were 2.3~2.5μm/h.

Photoluminescence (PL) and optical absorption were utilized to characterize the as-grown samples. PL measurements were carried out using a standard lock-in amplifier technique.

III. Results and Discussion

First, the results of InAlAsP layers are described. Figure 1 shows the PL spectra of InAlAsP layers for various Al compositions at 77K, where the PL intensity is normalized at their peak values. A YAG laser (wavelength 532 nm) was used as an excitation source. PL was detected by cooled

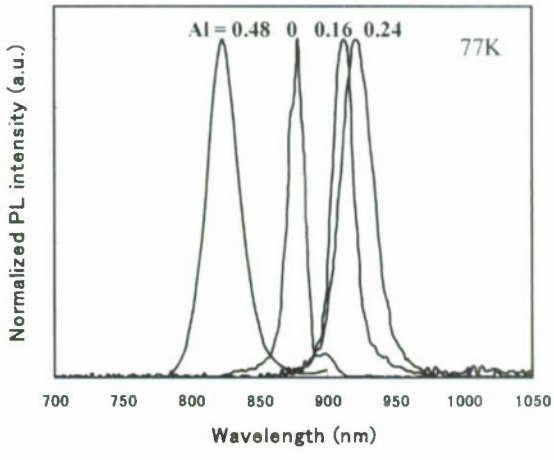

Fig. 1 PL spectra of InAlAsP layers at 77K

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photo-multiplayer. Figure 2 shows Al composition dependence of the PL peak energy of the InAlAsP layers at 77K. It is known that a marked bowing effect is observed, where the PL peak energy of the InAlAsP layers is smaller than those of InP and InAlAs layers.

Next, results for InGaAs/InAlAsP MQWs are mentioned. Figure 3 shows the inter-subband absorption spectra of the InGaAs/InAlAsP MQW layers at 300K. The intersubband absorption spectrum was measured by using Fourier-transform infrared spectrometer. The measurements were performed at

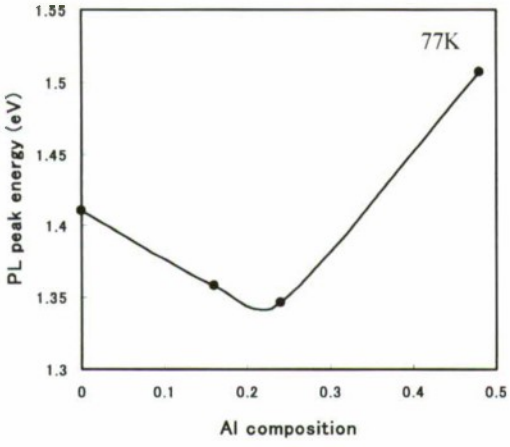

Fig. 2 Al composition dependence of PL peak energy of InAlAsP layers

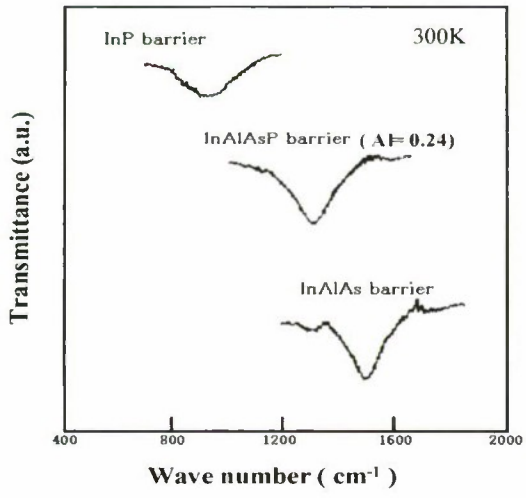

Fig. 3 Inter subband absorption spectra of InGaAs/InAlAsP MQWs at 300K

Brewster's angle (73°C) to maximize the normal component of the electric field vector and to reduce reflection. Al compositions of the barrier layers are 0 (InP barriers), 0.24 (InAlAsP barriers) and 0.48 (InAlAs barriers), respectively. All samples are Si-doped ($1x10^{18}$ cm^{-3}) to get inter-subband absorption. The InGaAs well layer thickness is 7.5 nm and the barrier layer thickness is 7 nm. It is clearly seen that the absorption peak shifts toward higher energy side with increasing the Al composition, which indicates that the conduction band discontinuity ΔEc (and the valence band discontinuity ΔEv) can be controlled by changing the Al composition of the InAlAsP barrier layers. The estimated ΔEc from the absorption peaks are 180 meV for InP barriers, 330 meV for InAlAsP barriers and 520 meV for InAlAs barriers, respectively.

We also measured the interband absorption spectrum. Figure 4 shows the absorption spectra of the undoped InGaAs/InAlAsP MQW layers at 300K, where the Al compositions of the barrier layers are 0, 0.24, and 0.48. The InGaAs well layer thickness is 8 nm for the MQWs with InP and InAlAs barriers, while that for the MQWs with InAlAsP barriers is 9 nm. The barrier layer thickness is 7 nm for all

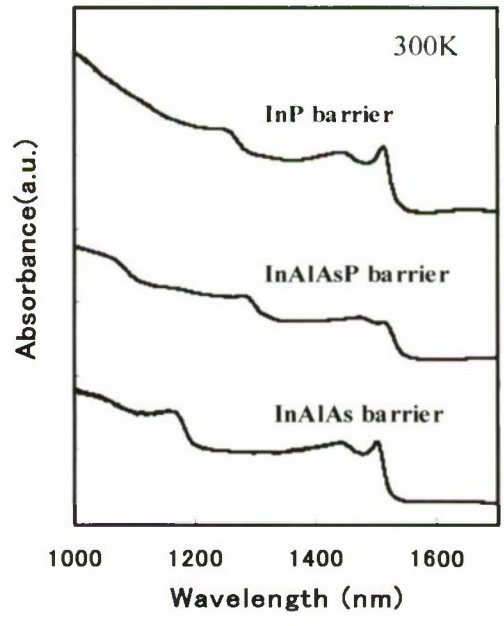

Fig. 4 Absorption spectra of undoped InGaAs/InAlAsP at 300K.

samples. It is known from the Figure that 2D-exciton peaks are very clearly observed for the MQWs with InP and InAlAs barriers, while that of the MQWs with InAlAsP barriers is not so clear comparing with other two MQWs.

In order to understand the mechanism of weak exciton peak in the MQWs with InAlAsP barriers, we measured the PL spectrum of the undoped MQW layers at 77K. PL was detected by cooled InSb photodiode. A YAG laser (wavelength 1064 nm) was used as an excitation source. Figure 5 and 6 show the barrier Al composition dependences of the PL intensity and the PL full width at half maximum (FWHM) of the undoped MQW layers. It is clearly seen that the PL intensity of the MQW with InAlAsP harriers (Al=0.24) is weak comparing with other two MQWs, which corresponds the weak 2d-exiciton peaks. However, the FWHM is also smaller than other two MQWs. This means that the weak exciton peak for the MQWs with InAlAsP harriers is not due to interface roughness. The reason of above results is not clear at present stage. Some kinds of defects are considered to exist for the MQWs with the InAlAsP harriers. Further studies are necessary to clarify the mechanism.

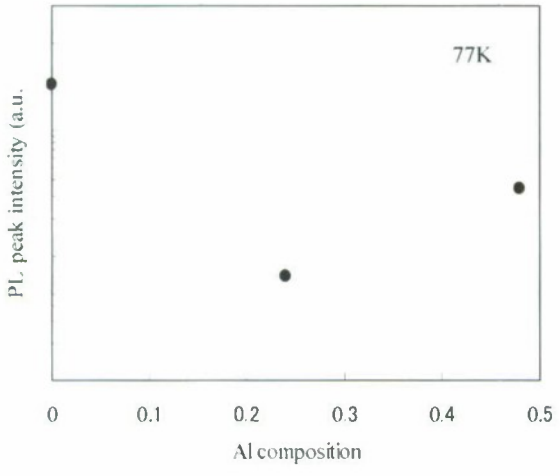

Fig. 5 Al composition dependence of PL intensity of undoped InGaAs/InAlAsP MQWs at 77K.

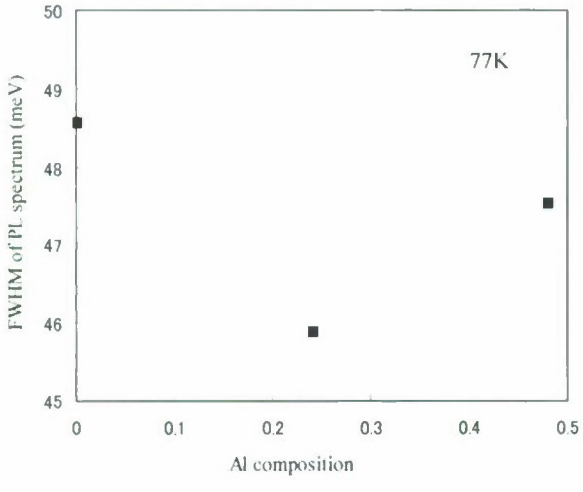

Fig. 6 Al composition dependence of PL-FWHM of undoped InGaAs/InAlAsP MQWs at 77K.

Finally, InGaAsP/InAlAsP MQW layers at 1 μm wavelength region were grown and optical absorption measurement was carried out at 300K. The MQW layers have 40 periods. The Ga composition of the InGaAsP well (9 nm) is 0.2, and the Al composition of the InAlAsP harrier (7 nm) is 0.24. Figure 7 shows the absorption spectrum of the InGaAsP/InAlAsP MQWs at 300K. A clear absorption edge is observed at about 1.06 μm. The step like structure of the absorption spectrum suggests that both of electrons and holes are confined in the quantum wells, which indicates that the InGaAsP/InAlAsP MQW layer is very promising for

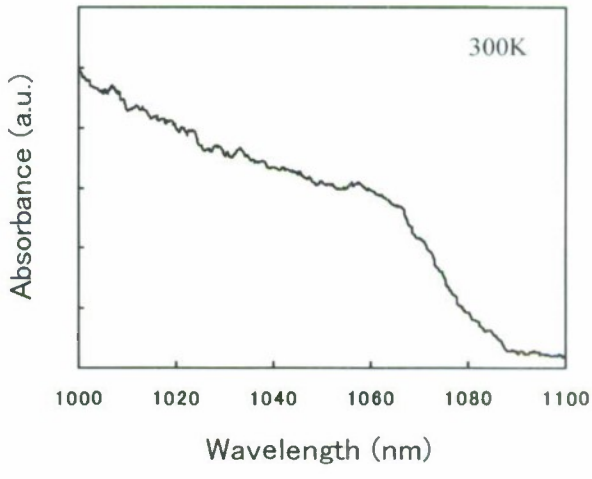

Fig. 7 Absorption spectrum of InGaAsP/InAlAsP MQWs at 300K

optical modulators using QCSE in the 1 μm wavelength region. The device fabrication is now under going.

IV. Summary

. In summary, we proposed InGaAsP/InAlAsP MQWs for QCSE type optical modulators for 1 μm wavelength region lattice-matched to InP. InGaAP/InAlAsP MQW layers, as well as InGaAs/InAlAsP MQW layers and InAlAsP layers, were grown by molecular beam epitaxy and their optical properties were studied in detail. . It became clear that the conduction band discontinuity ΔEc and the valence band discontinuity ΔEv can be controlled by changing the Al composition of the InAlAsP barrier layers. InGaAsP/InAlAsP MQWs having absorption edge of 1.06 μm were successfully obtained.

V. Acknowledgement.

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All-optical Switch Consisting of Multimode Interferometer Combined with Metamaterials: Device Design

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Abstract

We demonstrated magnetically excited magnetic resonances with negative magnetic permeability in InP-based optical waveguide with an array of gold split-ring resonators (SRRs). In transmission characteristics of the device, an incident-polarization-dependent absorption feature was clearly observed at 1575 nm. The experimental results show that the SRR array interacted with the magnetic field of the propagating light in the device, producing magnetic resonance at optical frequencies.

Keywords- Integrated optics, Meta-materials, Waveguide device, III-V semiconductor

I. Introduction

The relative permeability of every natural material is 1 at optical frequency. However, if we can break this restriction, we will be able to find a new field in optical-communication device technology. This can be achieved using the concept of left-handed materials (LHMs), or metamaterials, which have attracted growing attention in recent years [1-5]. To examine the feasibility of such LHM optical devices, we designed and made a 1.5-μm-band, all-optical switch consisting of a semiconductor waveguide with a LHM region and confirmed magnetic interaction between the LHM and light that traveled in the waveguide. The following provides the outline of the device and the experimental results.

II. Theory and Design of LHM

Figure 1 shows the proposed optical switch composed of an GaInAsP/InP 1×1 multimode-interferometer (MMI) coupler and a LHM region consisting of gold split-ring-resonator (SRR) array attached on the coupler. For input TE-mode light with a frequency equal to SRR resonance frequency, the imaginary part of the permeability of the LHM region has a large absolute value, and this causes a large propagation loss of the input light. Then, if controlling light ($\lambda < \lambda_{g,InP}$) is applied to the LHM region from above the device, a gap of each SRR is short-circuited by excited carriers in InP cladding layer, and consequently the magnetic response of the LHM region vanishes. This makes the imaginary part of the LHM permeability 0, thereby decreasing the propagation loss of the input light. In this way, the input light can be switched directly by the controlling light. (Our device can also have a function of light trapping due to a negative Goos-Hanchen shift caused by LHMs, therefore can be used as an optical memory.)

The magnetic properties of the LHM greatly depend on the conduction characteristics of metal that forms the SRRs.

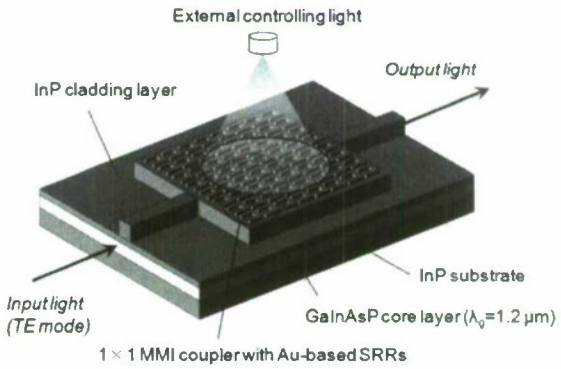

Fig. 1 All-optical waveguide switch consisting of InP-based 1×1 MMI coupler covered with LHM (array of gold SRRs).

Therefore, we first calculated the dispersion of internal impedance (the ratio of surface electric field to total current) in gold (see [6, 7] for the formula for internal impedance at optical frequencies). Figure 2 shows the result for a gold layer with a thickness larger than the penetration depth at each frequency. As frequency increases, the real part of the internal impedance first increases steeply and then saturates at the inherent frequency, about 10 THz. At frequencies more than 100 THz, the real part gradually decreases, and this dispersion property corresponds to the dielectric behavior of gold. In contrast, the imaginary part shows no saturation and has a large negative value at optical frequencies. This corresponds to ohmic loss in gold.

Using these results, we designed a SRR that had optical resonant frequency. For our device, a 4-cut single SRR (s-SRR) consisting of a gold square ring with four gaps (see left inset in Fig. 3) was used because this structure has a high resonant frequency due to its small gap capacitance [7]. From the Maxwell's equations and Biot-Savart law, we obtained equation

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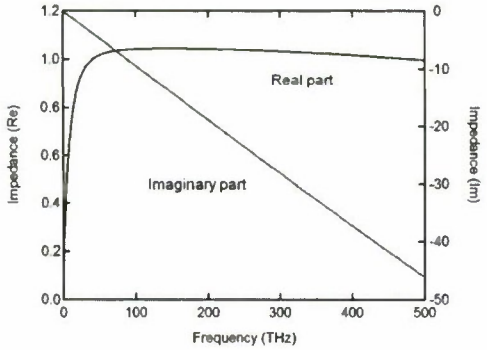


Fig 2 Internal impedance of gold as a function of frequency.

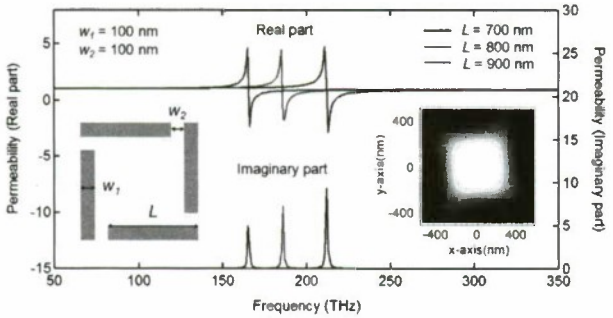


Fig 3 Complex permeability of LHM consisting of SRR array (d = 1.6 μm). (left inset) 4-cut single SRR, (right inset) magnetic field in gold SRR (L = 800 nm) at 185 THz.

$$\partial_t \int_{SRR} B d\sigma = i\omega\mu_0 \int_{SRR} \left(H_{ext} + \frac{1}{4\pi} \oint \frac{j d\mathbf{s} \times \mathbf{r}}{r^3} \right) d\sigma$$
$$= V_{ring} + 4V_{gap} = \left[Z(\tau) \cdot \frac{L}{W_1} - \frac{4W_2}{i\omega\varepsilon_0\varepsilon_m W_1 \tau} \right] j \quad (1)$$

where H_{ext} is the magnetic field of light that travel in the device, ε_m and $Z(\tau)$ are the relative permittivity and internal impedance of gold, τ is a thickness of the SRR, j is induced current in the SRR, and L, W_1 and W_2 are the dimensions of the SRR (see left inset in Fig. 3).

Using Eq. (1), the distribution of magnetic field around the SRR was calculated, as illustrated with right inset in Fig. 3. From this result, we finally obtained the complex permeability $\bar{\mu}_{zz}$ of a LHM consisting of a SRR array, using the field averaging equation [8] given by

$$\bar{\mu}_{zz} = \frac{\bar{B}_z(0,0,d)}{\bar{H}_z(0,0,d)} = \mu_0 \frac{(2d)^{-2} \int_{-d}^{d} dx \int_{-d}^{d} H_z(x,y,d) dy}{(2d)^{-1} \int_0^{2d} H_z(0,0,z) dz} \quad (2)$$

where d is the distanec between SRRs, and B_z and H_z with over-lines represent the average values of magnetic flux density and magnetic field in the unit cell that includes a SRR. Figure 3(c) shows the results, with SRR size L as a parameter. Other parameters W_1 and W_2 were set to 100 nm, distance d between SRRs was set to 1.6 μm, and thickness τ was set twice as large

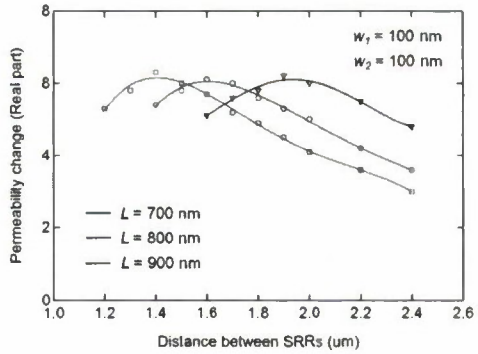


Fig 4 Permeability change as a function of distance between SRRs., calculated for 185 THz resonance.

as the penetration depth of gold at each frequency. The figure shows that SRRs with L = 700-800 nm show magnetic response at 1.5-μm-band frequencies.

The magnetic response of the LHM depends on distance d between SRRs. Figure 4 shows the intensity of magnetic response (i.e., change in permeability) as a function of d. In simulation, we considered nearest and next-nearest neighbor interaction between SRRs. There is an optimal distance that maximizes the magnetic response. For large distances, the response is weak because the surface density of SRRs is small. For small distances, magnetic field in a SRR is canceled by those of neighboring SRRs, and this weakens the total response of the SRR array.

III. Simulating Device Operation

After calculating the complex permeability of SRR-array layer, we designed a sample device and confirmed its operation with the aid of computer simulation based on the transfer-matrix method. We assumed that the device was composed of an undoped GaInAsP core layer (λ_g = 1.2 μm, n = 3.38, 200-nm thick) and an undoped InP cladding layer (n=3.16, 500-nm thick) formed on an InP substrate. A SRR array (L = 750 nm, W_1 = 100 nm, W_2 = 100 nm, d = 1.6 μm) with 1.5-μm-resonant frequency was attached on the surface of the cladding layer of the MMI region. The width and length of the MMI were set to 15 μm and 650 μm, respectively.

From Maxwell's equations, we obtained the transfer matrix with terms for permeability. Magnetic field $H_z^i(y)$ and electric field $E_x^i(y)$ in i-th layer can be given by equation

$$\begin{pmatrix} E_x^i(y) \\ H_z^i(y) \end{pmatrix} = \begin{pmatrix} \cosh[\beta_i(y-y_i)] & \frac{\mu_0\mu_i\omega}{j\beta_i}\sinh[\beta_i(y-y_i)] \\ -j\beta_i\sinh[\beta_i(y-y_i)] & \mu_0\mu_i\omega\cosh[\beta_i(y-y_i)] \end{pmatrix} \begin{pmatrix} E_x^i(y_i) \\ H_z^i(y_i) \end{pmatrix} \quad (3)$$

where y_i and μ_i are the bottom coordinate and complex permeability in i-th layer. Using Eq. (3) and boundary conditions for E_x and H_z, we can obtain the eigenvalue equation and calculate the propagation coefficient in each region of the MMI. In calculation, E_x and H_z were assumed to show exponential attenuation in the outside of the GaInAsP core layer (i.e., in air and the InP substrate).

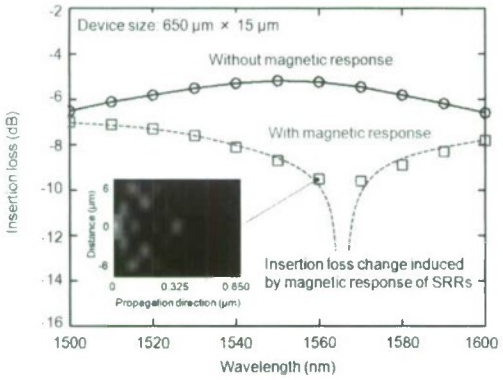


Fig. 5 Extinction ratio in sample device (L = 750 nm, W_1 = 100 nm, W_2 = 100 nm, d = 1.6 μm) as a function of wavelength. Inset shows electric field distribution in 1×1 MMI with SRR array.

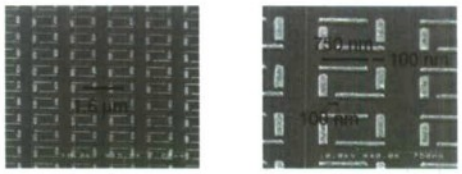
Using the propagation coefficients, we calculated the propagation loss of light in the device as a function of wavelength. Figure 5 shows the results with SRR magnetic response (with SRR gaps open) and without the response (with SRR gaps shorted). A switching change in propagation loss of 4.2 dB or larger can be expected at 1560-1570 nm wavelength (corresponding to the SRR resonance frequency). In this way, waveguide-based switching device with LHMs can be realized for optical frequency.

IV. Device Fabrication and Characteristics

To move one step closer to actual all-optical switches, we made a trial device to confirm the magnetic response of the LHM consisting of s-SRRs arrayed on a GaInAsP/InP MMI coupler. The trial device was fabricated as follows. A starting material was a semi-insulating InP(100) wafer. An undoped GaInAsP core layer (λ_g = 1.2 μm, 200-nm thick) and an undoped InP cladding layer (500-nm thick) were grown in this order with organic-metal vapor phase epitaxy (OMVPE). On the surface of the cladding layer, s-SRRs consisting of Ti (5 nm) and Au (20 nm) layers were made using electron-beam (EB) lithography and lift-off process. Figures 6 show enlarged oblique views of the fabricated SRR array. The dimensions of the SRR were set to the values we used for the simulation in the previous sections.

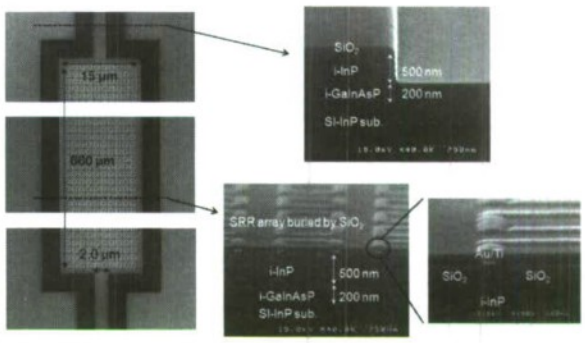
After that, to make the 1×1 MMI coupler, a SiO_2 mask (100-nm thick) was formed on the wafer, using plasma-enhanced chemical vapor deposition (PECVD) and EB lithography. Then, the MMI coupler was formed using reactive ion etching with CH_4/H_2 mixture. Figure 7 shows the optical microscope view of the entire device, and enlarged cross-section views observed with SEM.

To examine the interaction of the SRRs and light traveling in the MMI, we measured the transmission characteristics of the device. The light from a tunable laser was transferred into and out of the device through a polarization controller (see Fig. 8(a)). We first measured near field patterns at the output end of the device and confirmed that the single-mode connection was



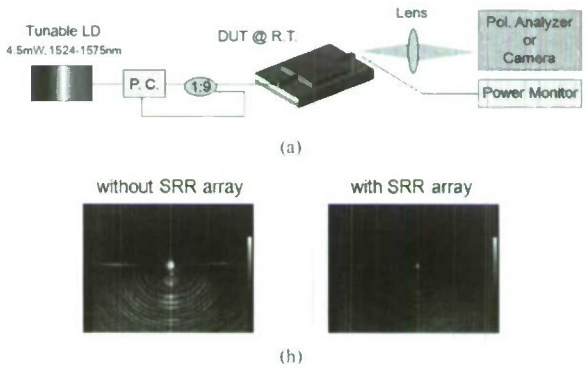
(a) (b)

Fig. 6 SEM images of gold SRR array before SiO_2 deposition, (a) wide area view, and (b) enlarged view.



(a) (b)

Fig. 7 MMI coupler with gold SRRs covered with SiO_2 layer. (a) optical microscope image, and (b) SEM cross-section images.

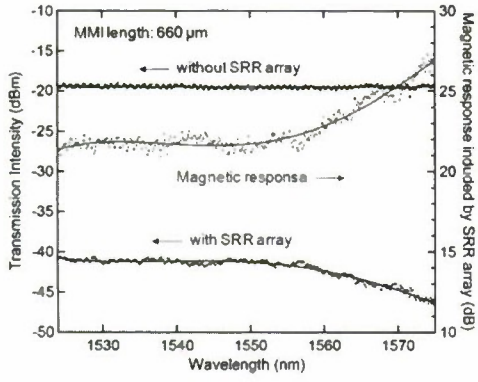


(a)

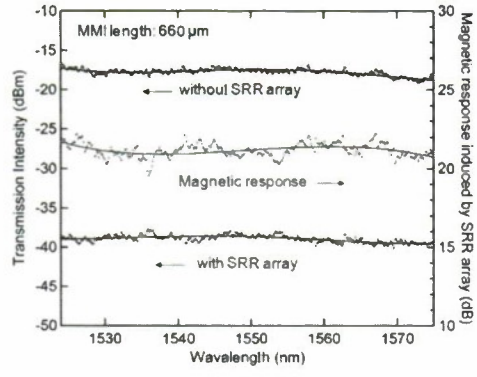
(b)

Fig. 8 (a) Measurement setup for 1×1 MMI coupler with gold SRR array. (b) Near field pattern of device with/without SRR array.

established (see Fig. 8(b)). Then, we measured the intensity of the output light, using a power meter. In this measurement, control devices without SRRs were also prepared for comparison. Figure 9 plots transmission intensity for devices with SRRs (blue curves) and without SRRs (black curves) as a function of wavelength from 1524 to 1575 nm, measured for input light of (a) TE mode and (b) TM mode. To clarify the effect of magnetic interaction between light and the SRRs, we took the difference between the transmission intensity with SRRs and that without SRRs (see red curves in the Fig. 5). As shown in Fig. 9, the magnetic interaction was observed only for TE-mode light; that is, the transmission intensity with SRRs gradually decreased with wavelength for TE mode. No decrease



(a)



(b)

Fig. 9 Transmission intensity of devices with SRR (blue lines) and without SRRs (black lines) as a function of wavelength, measured for (a) TE mode and (b) TM mode. Difference between two devices is also plotted for both modes (red lines).

in intensity was observed for TM mode. This polarization-dependent absorption is positive proof that the magnetic field of light interacted with the SRRs to produce magnetic resonance at optical frequencies. (The frequency of resonance peak in this device shifted towards a longer wavelength than we had expected and was out of the measurement range because the host material for the SRRs in the experiment was SiO_2 and different from material (i.e., air) assumed in simulation.)

In Figs. 9(a) and 9(b), the difference between the transmission intensity at 1524 nm and that at 1575 nm is an index of the magnetic response of the LHM. We measured this difference as a function of MMI length. The result is plotted in Fig. 10, showing that the magnetic response can be observed only for TE-mode light.

V. CONCLUSION

We fabricated an InP-based optical waveguide device combined with left-handed material (metamaterial) and demonstrated magnetic interaction with the metamaterial and light that traveled in the waveguide. The metamaterial consists of an array of

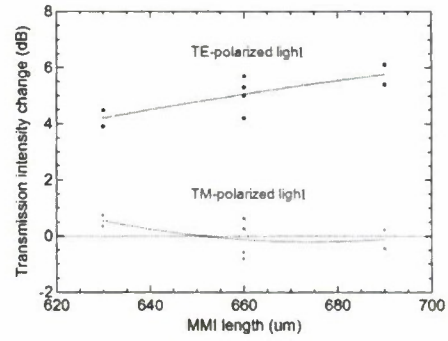


Fig. 10 Difference between 1524-nm transmission intensity and 1575-nm one as a function of MMI length, measured for TE and TM mode.

minute metal split-ring resonators (SRRs) attached on the waveguide. The operation wavelength is set to 1.5 μm. The transmission characteristics of the device strongly depend on the polarization and wavelength of input light. This shows that the SRR array interacted with the magnetic field of light and produced magnetic resonance at optical frequencies. Our result is useful to develop waveguide-based matamaterial devices for optical communication.

ACKNOWLEDGMENT

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ELECTRICAL PUMPING TO III-V LAYER FROM HIGHLY DOPED SILICON MICRO WIRE TO REALIZE LIGHT EMISSION BY PLASMA-ASSISTED BONDING TECHNOLOGY

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Abstract

The direct eurrent pumping from highly doped silicon mierowire to InP-based III-V active layer for spontaneous light emission was realized by air ambient plasma-assisted direct bonding. The semi-conductive properties of the hetero-integration and the effeets of plasma-assisted bonding process on InGaAsP multiple quantum well (MQW) were measured and discussed. The eleetrical pumping from silicon microwire to InGaAsP MQW material for spontaneous light emission was suceessfully demonstrated afterwards.

I. Introduction

Hetero-integration of III-V materials appears to be a very promising solution for silicon photonic active devices because silicon direct light emission from silicon is very inadequate due to the indirect transition. Since the lattice mismatch between silicon and III-V active materials introduces large dislocations and initial stress, the direct growth of a high-quality III-V material layer on silicon still remain very difficult. Therefore, the direct bonding method is considered to be a practical technology and has attracted considerable research interest. As a result, several breakthroughs in silicon active devices, such as the realization of a silicon evanescent hybrid laser, have been achieved. [1]-[3] However, direct current injection from silicon to the III-V material by plasma-assisted bonding for light emission still remains an open challenge. [4][5]

In this paper, we describe hetero-integration of III-V materials on highly doped silicon on insulator (SOI) microwires by plasma-assisted bonding under ambient air, mainly for the purpose of realizing the direct-current-pumped silicon hybrid laser we proposed previously. [4] The III-V compound semiconductor active layer was bonded onto an SOI platform with highly doped siliconwires as shown in Fig. 1. The silicon microwires serve as electrical contacts which provide current injection into the III-V active layer for light emission as well as an optical rib waveguide to guarantee the lateral optical confinement of the lasing light. [4] A major challenge of this type of the laser is ensuring highly efficient current injection from the silicon microwires to the III-V semiconductor material to generate photon inversion for light emission. [5] The bonding of InP-based III-V material onto the SOI platform with silicon microwires was performed, adopting the modified plasma-assisted bonding method we presented earlier. [5][6] The effects of plasma-assisted bonding process on the InGaAsP MQW photoluminescence (PL) spectrum were investigated. On the other hand, the properties of current injection properties from doped silicon to InP/InGaAsP were measured and compared in order to determine the better candidate for the interlayer of the MQW materials. Finally, we demonstrated electrical pumping from highly doped SOI microwires to the MQW materials by plasma-assisted bonding under ambient air for spontaneous emission and measured the I-V and I-L characteristics.

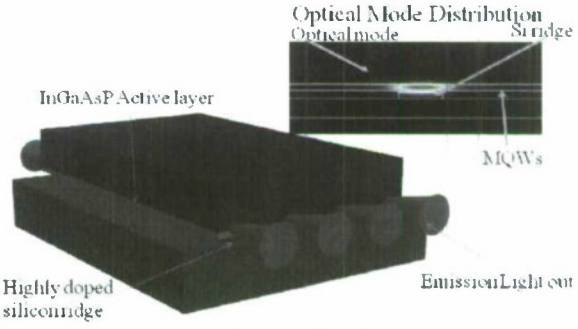

Figure 1: Schematic of silicon and III-V material active layer hetero-integration devices for light emission and FDM calculation of the TE fundamental optical mode distribution on a cross section of the device

II. Effects of plasma-assisted bonding on the InGaAsP MQW wavelength spectrum

The effects of the established plasma-assisted bonding process on III-V MQW material grown by MOVPE method had to be investigated before the current injection experiment. Therefore, a conventional epitaxial structure with 200nm Q1.25 separate confinement heterostructure (SCH) InGaAsP, six stacks of InGaAsP strained MQW material (1.56μm wavelength peak), 200nm Q1.25 SCH-InGaAsP and 200nm p-type doped InP cladding layers was grown by MOVPE on an n-type InP substrate.

Ar/oxygen plasma treatment and the pressure during bonding may be the main reasons to cause degradation of the MQW characteristics. The epitaxial chips were bonded on the highly doped silicon and detached afterwards.[5][6] The III-V chips were placed in a micro PL measurement setup to measure the PL spectra of the MQW material and compare them with the results before processing, as shown in Fig. 2. We can conclude that the bonding process does not cause an obvious wavelength shift of the MQW spectrum peak. This is because the pressure applied during the bonding process is relatively low and does not cause

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damage to the III-V layer. Another reason may be that both the InP cladding layer and InGaAsP SCH layer alleviate the initial stress between contact interfaces as well as protects the MQW from an Ar/oxygen plasma effect. However, a long time exposure of the MQW at the cleaved edge of the chip to an Ar/oxygen plasma may still be possible to degrade MQW material. As a result, it is possible to apply the plasma-assisted bonding for the current-injected light emission experiment.

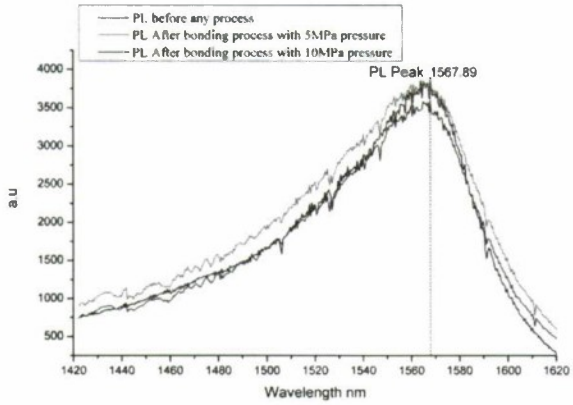

Figure 2: PL spectra of the InGaAsP MQW material before and after the bonding process (plasma processing time of 3min, at 200 ^{0}C during bonding)

III.Semi-conduetive properties of the III-V layer to p-type doped silicon mierowires

The choice of highly doped silicon or InGaAsP MQW material for hetero-integration interlayer is critical for realizing efficient current injection. Adjusting the component ratio of the InGaAsP quaternary compound provides large degree of the freedom to adjust the band gap, electron affinity, dielectric permittivity, electron/hole mobility and other semi conductive parameters to approach a better current injection condition with silicon.

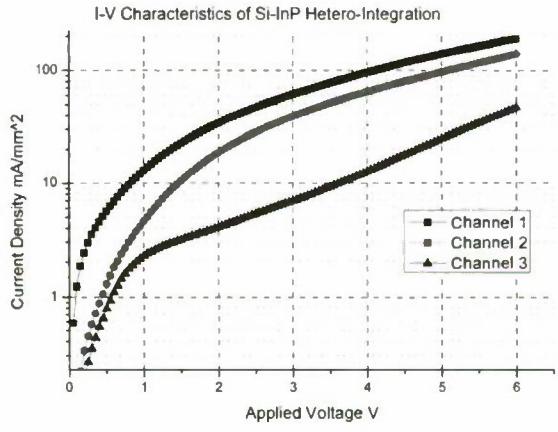

Figure 3: Current injection density vs applied voltage of p-InP bonded onto an SOI platform with 20-μm-wide p-type doped silicon microwires. I-V characteristics of three channels in the same sample were measured separately.

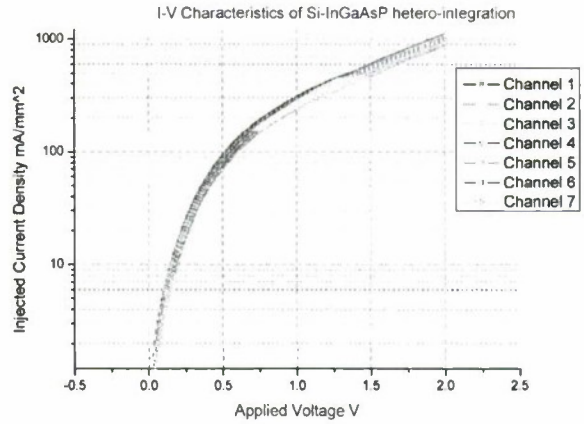

Figure 4: Current injection density vs applied voltage of InGaAsP bonded onto an SOI platform with 20-μm-wide p-type doped silicon microwires. I-V characteristics of seven channels in the same sample were measured separately

Therefore, 200-nm i-InGaAsP and 200-nm p-type doped InP for comparison were grown on n-type InP wafers by MOVPE method and bonded to the highly boron doped 10^{19} atom/cm^3 SOI platform.[6] Their current injection characteristics were measured and are compared in Figs.3 and .4, respectively. I-V curve of the silicon platform to InP shows a large junction resistance, indicating the interruption of electron/hole transportation from the highly doped silicon to the InP because of the incompatible band gap distributions of the hetero materials. Although a relatively large voltage (6 V) was applied, the injection current density was around 100 mA/mm^2 and became unstable even among channels in the same bonded chip. On the other hand, the InGaAsP/Si hetero-integration shows a rather impressive electrical contact improvement of 100 times because of their band gap matching. A 1000 mA/mm^2 injection current density was achieved under 2 V.

IV.Current-injected light emission properties of the silicon/InGaAsP MQW hetero-integration

We used the same InGaAsP MQW epitaxial chips mentioned in section 2 to bond onto the SOI platform with 5-μm-wide silicon microwire, using the process described as followed. First of all, the SOI platform with boron doped (10^{19} atoms/cm^3) microwires was fabricated by a silicon micromachining process. [6] The SOI chip was rinsed by a standard RCA process (NH_4OH:H_2O_2:H_2O=1:1:5) for 10 min at 65 ^{0}C and dried by nitrogen. Then it was dipped into the buffered hydrofluoric acid (BHF) for 2 min to remove the natural oxidation layer. This process was repeated for several times to achieved good surface contact condition. Meanwhile, the InP cladding of III-V chip was selective etched by HCl solution and was then rinsed by 96% sulfuric acid for 2 min. Both the SOI chip and III-V chip

were exposed by an Ar/oxygen plasma process. Then the SOI platform chip and III-V chip were bonded together in ambient air with 5 MPa pressure under 200 ^{0}C for 3 min. [6] Finally, the sample was annealed under N_2 at 180 ^{0}C for 12 h. [8][9]

In order to couple the emission light from the bonded chip to a single mode fiber (SMF) for further measurement, the InGaAsP MQW material was bonded onto an SOI platform utilizing an automatic precise alignment bonder. [10] The cleaved edge of the III-V chip was aligned to the edge of the SOI platform so that the SMF could approach to the cleaved facet of the InGaAsP active region, as illustrated in Fig. 1. I-V characteristics of the hetero-integrated chip were measured as shown in Fig. 5. Two channels (A4, A5) of the bonded chip were measured.

The Si/III-V hetero-integrated chip was then mounted onto a copper plate and attached to a stage with the temperature controller in the measurement setup. The current-injected spontaneous emitting light of the chip was focused by micro lens to an infrared (IR) camera to be observed as shown in Fig. 9. Then a tapered SMF was aligned with the emission position of the III-V active layer cleaved facet using piezoelectric actuator stages to couple the output of the emission light. A stepped precision current source was used to provide the injection current and the optical power was measured from the output of the SMF by an optical multimeter. The I-L characteristics of the InGaAsP MQW material's spontaneous light emission by current injection from the p-type doped silicon microwire are shown in Fig. 6. The I-L characteristics at different temperatures were compared, revealing classic parameters of current-injected spontaneous light emission. A current injection level of 150 mA seems to reach the saturation region of the photon inversion. We conclude that this is the first demonstration of current injection directly from silicon to a III-V MQW material for light emission by plasma-assisted direct bonding in ambient air. It reveals the possibility of realizing a complete direct-current-pumped silicon hybrid laser by direct bonding method for the advanced integration of SOI-based electrical and optical devices.

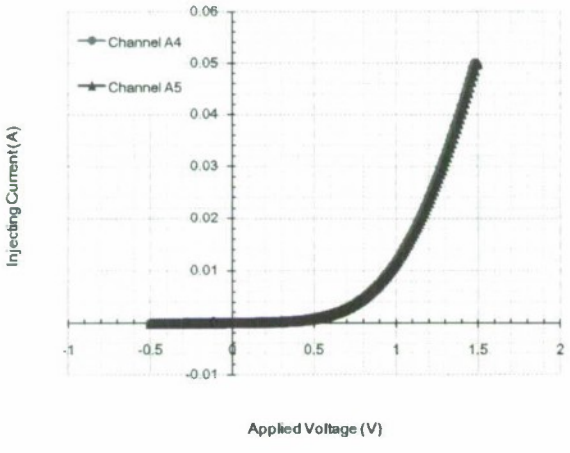

Figure 5: I-V characteristics of the hetero-integrated chip. Two channels were measured (A4, A5) by a semiconductor analyzer

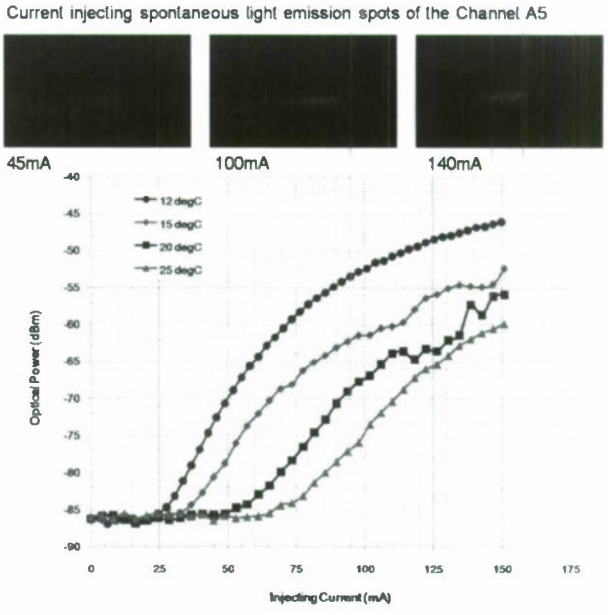

Figure 6: Spontaneous light spots observed by an IR Camera of channel A5 in hetero-integrated chip and its I-L characteristics under different temperature conditions

V. Conclusion

The plasma-assisted bonding of an InP-based active layer on highly doped silicon on insulator (SOI) microwire for realizing a direct-current-pumped light emission is presented. The plasma-assisted bonding process shows no significant effect on the InGaAsP MQW material in PL spectrum peak. The properties of current injection properties from doped silicon to InGaAsP are better than those of p-type doped InP, which indicates that InGaAsP is a better candidate for the interlayer between silicon and an MQW material. Electrical pumping from the SOI microwire to the MQW material for spontaneous emission is demonstrated.

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GaSb Based, 1.55 μm Laser Monolithically Integrated on Silicon Substrates Operating at Room Temperature

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Monolithic Integration of a 10 Gb/s Mach-Zehnder Modulator and a Widely Tunable Laser based on a 2-Ring Loop-Filter

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Abstract: A 10-Gb/s Mach-Zehnder modulator is monolithically integrated with a tunable laser source based on a 2-ring loop-filter with a small device dimension (2.5 × 0.9 mm^2). Sufficient static extinction ratio of 16.5 dB was obtained both at 1573.92 and 1595.50 nm.

Introduction

Wavelength tunable laser sources (TLSs) are key components in the evolution toward reconfigurable dense wavelength division multiplexed (DWDM) photonic network systems. They have been coming into wide use for the replacement of distributed feedback (DFB) lasers. As external optical modulators for TLSs, a Mach-Zehnder modulators (MZMs) are preferable because of their very wide wavelength working range. $LiNbO_3$ based MZMs have been widely used with hybrid integration in such optical tunable transmitters. Recently, in order to reduce footprint of the transmitters and transponders, small form factor modules (XFP, SFP, etc.) have been getting more and more attractive than those of the previous generation (300 pin MSA transponders). Therefore the optical modulators used in such modules should be miniaturized.

Semiconductor based optical modulators are more suitable for small form factors because of their compactness, lower driving voltage and easy integration with other active components [1-3]. As a tunable transmitter device, for instance, an InP-based sampled-grating distributed Bragg-reflector monolithic TLS with an integrated MZM was reported [4, 5]. The MZM was cascaded to the tunable laser section, therefore the device length reached as long as 3.4 mm. On the other hand, very compact monolithic full-band TLSs with 2-ring optical filters have been reported [6-8]. The 2-ring loop-filter based TLS, which we have previously demonstrated [8], can be one of the candidates as extremely compact tunable transmitters when MZMs are monolithically integrated.

In this paper, we demonstrate a very compact monolithic tunable transmitter device, which consists of a widely tunable laser with a 2-ring loop-filter, monolithically integrated with a 10 Gb/s MZM. For the purpose of compact size, we introduce a directional coupler (DC) based partial mirror between MZM and TLS. The total device dimension is 2.5 × 0.9 mm^2.

Monolithic Widely Tunable Laser

A schematic top view of a monolithic TLS configuration is shown in Fig. 1. The device consists of three sections: SOA, phase control (PC), and loop-filter section. The loop-filter section consists of two ring resonators and an asymmetric Mach-Zehnder interferometer (AMZI). Each ring resonator is connected to a straight waveguide from the SOA section by a 3-dB multimode interference (MMI) coupler. The light from the SOA propagates through the

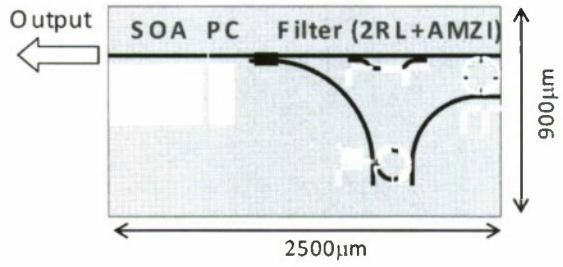

Fig. 1 Schematic top view of a monolithic TLS configuration.

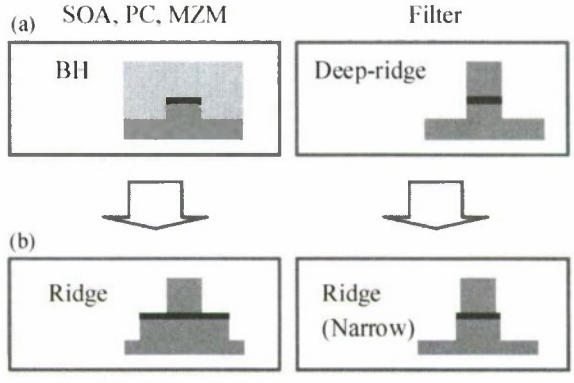

Fig. 2 Waveguide structures utilized for monolithically integrated device. (a) previous type and (b) this work.

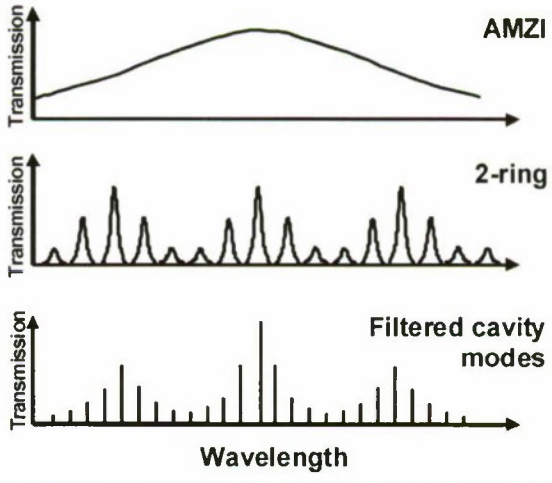

Fig. 3 Transmission spectra of AMZI and a 2-ring resonator and filtered cavity modes by loop-filter as a function of wavelength.

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MMI coupler, one of the rings, AMZI [8], the other ring, and returns to the SOA again through the MMI coupler. Both clockwise and antielockwise propagations exist in the loop-filter. This integrated chip is realized on the InP substrate. Its dimension is 2.5 × 0.9 mm^2. In order to cover wide tuning range, the wideband SOA [9] was applied. The waveguide core in the gain section consists of InGaAsP/InGaAsP based quantum wells, and those of loop-filter and PC sections are InGaAlAs based. Those QWs are butt-coupled smoothly to each other. After the epitaxial growth, all the ridge waveguides were formed by dry etching process. Thin metal heaters are formed on top of the rings and the AMZI parts [10].

In the previous report [8], two types of waveguides were formed on the device because optimized structure was different from each other waveguide. One was buried-heterostrucutre (BH) for SOA and PC sections and the other was deep-ridge waveguide formed for filter section. BH waveguide is suitable for current injected sections, such as SOA and PC, which must have an advantage for reliability. On the other hand, to prevent radiation loss, deep-ridge waveguide is suitable for the ring-resonator section. The cross sections of the waveguide were shown in figure 2 (a). However, fabrication process was too complicated when there were different waveguide structures on the device. In order to make the fabrication process as simple as possible, we unified the waveguide structures of ridge type as shown in figure 2 (b). To also prevent radiation loss in the ring-filter section, narrower base mesa was introduced for the rings than that of the other waveguides.

The principle of lasing mode selection is explained in figure 3. The two ring resonators have slightly different free spectral ranges (FSRs), which allow for extension of the tuning range to the lowest common multiple of the FSRs through the Vernier effect, as shown in Fig. 3 (2-ring). Whereas the tuning range can be extended with the small difference of the FSRs of two ring resonators, the side-mode suppression ratio (SMSR) to the next peaks decreases. Therefore, there is a trade-off relationship between tuning range and mode selectivity. The trade-off can be broken by increasing the number of rings (NR) because the finesse of the ring resonators can be enlarged. However, the insertion loss will increase as NR increases, because the loss of the semiconductor ring resonators would not be negligible. Therefore, we newly propose the structure to introduce an AMZI as a third filter instead of increasing NR. The insertion loss of an AMZI is much smaller than that of ring-filter because it is a one-pass filter with large radius. The FSR can be larger than that of ring resonators, therefore we utilize the AMZI to suppress the side modes. The concept can be explained as follows.

The transmission spectrum is shown in Fig. 3 (AMZI). As explained earlier, the Vernier transmission spectrum determined by two ring FSRs exhibits the periodic resonant peaks. At every lowest common multiple of the FSRs, there is a mode of the same transmission peak as others. Here, we can call the period of the lowest common multiple as the "lowest loss mode interval." Normally, this interval will

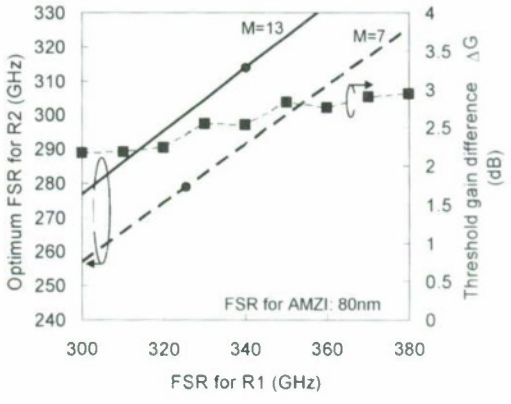

Fig. 4 Calculated optimum ring FSRs for M values, and threshold gain difference (ΔG) as a function of FSR for R1.

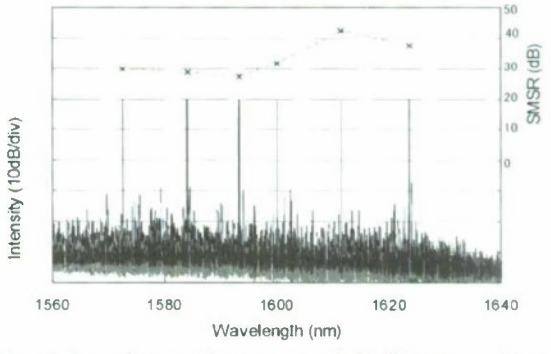

Fig. 5 Superimposed spectra and SMSRs over 51 nm range at 45 degree C.

limit the tuning range. By adding an AMZI, the other lowest loss modes can be suppressed, as shown in Fig. 3 (Filtered cavity modes), and consequently, the tuning range can be extended efficiently. Therefore, tuning algorithm does not become very complex due to additional control of the AMZI.

In Fig. 4, optimum FSR for R2 is calculated as a function of FSR for R1 to obtain as wide tuning range as possible. In the previous report [8], we obtained 39-nm tuning range with ring FSRs of 275 and 325 GHz (M=7), as shown in Fig. 4 [11]. To expand tuning range, FSRs of 314 and 340 GHz (M=13) were taken in this paper, and at least 2-dB threshold gain difference between the lasing and side modes (ΔG) is expected according to Fig. 4.

The superimposed spectra are shown in Fig. 5. The results in a tuning range of 51 nm (from 1572.6 nm to 1623.8 nm) with an SMSR of over 27 dB were obtained where the temperature of the device was stabilized at 45 degree C by a thermoelectric cooler (TEC).

Monolithic Tunable Transmitter

A schematic view of a monolithic tunable transmitter configuration is shown in Fig. 7. A 10 Gb/s MZM is monolithically integrated on the same chip of the TLS. The waveguide is connected to the TLS via a DC based partial mirror, which works as not only a partial mirror for the TLS cavity, but also an optical coupler to the MZM section. The

reflectivity can be controlled by changing the DC length. In figure 6, the reflectivity to the TLS as a function of DC mirror length was calculated for the total reflection on the facet for 1.55-μm wavelength light. Wavelength dependence would be negligible for the whole C and L bands. 38 μm long DC mirror was chosen according to the Fig. 6. Actually the end facet of the DC mirror was high-reflection (90%) coated to avoid optical excess loss. Consequently the reflectivity to the TLS was about 4%, and the rest of the optical power propagates to the MZM section. The front facet of the MZM is anti-reflection coated. The integrated device, such as tunable transmitters, can be realized on much smaller chip with this DC mirror than with the cascaded integration technology.

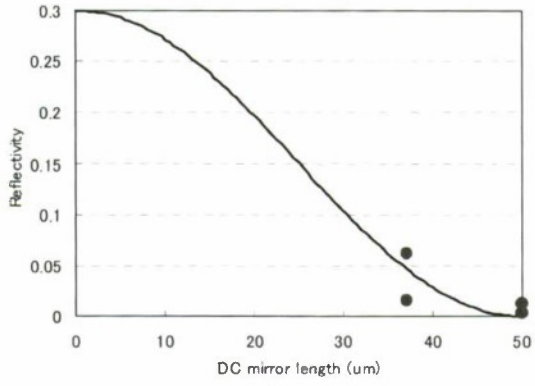

Fig. 6 The reflectivity of the DC mirror to the TLS as a function of DC mirror length. Simulation (solid curve) and experimental results (dots).

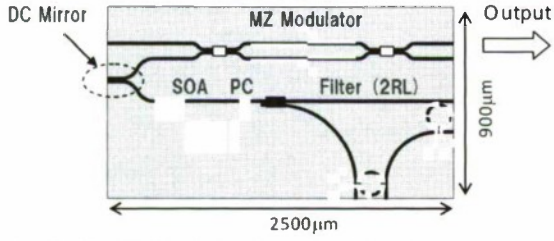

Fig. 7 Schematic top view of a tunable transmitter configuration; an MZM integrated tunable laser.

The waveguide core in the MZM section was InGaAlAs based, which was grown at the same time as the growth of other passive sections, such as loop-filter and PC. The total process including butt-joint and dry etching was completely compatible to that of the TLS structure mentioned above.

In this monolithic device structure, the AMZI filter was omitted. Alternatively, an MZM was integrated, thus the total dimension remained the same as the above mentioned TLS, i.e., the total dimension was also 2.5 × 0.9 mm^2.

Figure 8 shows the curves of normalized output power of the monolithic transmitter as a function of MZM bias voltage. The static extinction ratio was more than 16.5 dB for 1573.92 nm and 1595.50 nm, where the modulated output power of more than 2 mW was achieved at 200-mA current. The wavelength tuning range was limited for lack of the AMZI filter. For 1573.92 nm, the temperature of the device was stabilized at 20 degree C in figure 8. On the other hand, for 1595.50 nm it was measured at 50 degree C to make gain wavelength longer.

Figure 9 shows an electrically filtered back-to-back eye diagram for the tunable transmitter device at 20 degree C. The modulation conditions were as follows. The bias voltage was -6.1 V, the modulation amplitude peak-to-peak voltage (V_{pp}) was 5.39 V, the modulation speed of the non-return-to-zero (NRZ) pattern was 9.95328 Gb/s, and the word length of the pseudorandom bit sequence (PRBS) was 2^7 - 1. Clear eye opening for 1571.78 nm was obtained with a back-to-back configuration.

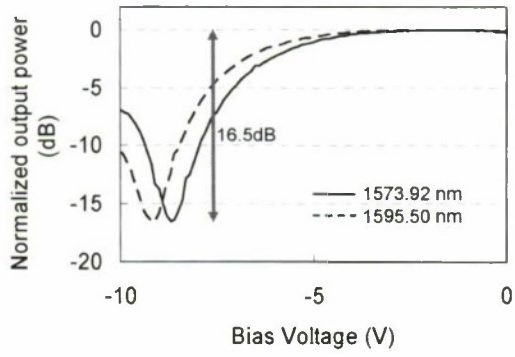

Fig. 8 Normalized output power as a function of MZM bias voltage.

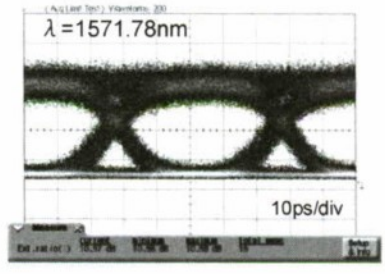

Fig. 9 10-Gb/s eye diagram at 20 degree C .

Conclusions

We have developed monolithic integration technology of an MZM and a TLS, by introducing a butt-joint and a simple dry etching process. We successfully demonstrated a wideband TLS with 51-nm tuning range, and a monolithic transmitter device, which is a 10 Gb/s MZM integrated TLS, utilizing a DC based partial mirror, with 16.5-dB extinction ratio at both 1573.92 and 1595.50 nm. Clear 10-Gb/s eye opening was also obtained.

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Fast Wavelength Switching in Interleaved Rear Reflector Laser

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***Abstract*—We present a novel tunable laser concept. The device employs an active interleaved rear mirror for wavelength selection and tuning enhancement. Rapid wavelength switching in the laser is investigated using a heterodyne method for time resolved spectral characterization. A very short transition time of 60 ps and SMSR recovery after less than 2 ns are observed.**

I. Introduction

Wavelength tunable semiconductor lasers are now widely deployed in optical telecommunication networks. Their main application today is spare inventory reduction for wavelength division multiplexed (WDM) networks. More demanding applications, including burst and packet switched networks, are the subject of active research [1]. The wavelength transition time of a laser becomes a critical parameter in scenarios where the path taken by individual bursts/packets depends on the output wavelength of a tunable source. Depending on the switching granularity of the network, reconfiguration times in the nanosecond range and below can be required.

In order to achieve wide single mode tuning, wavelength selective elements have to be used within the laser cavity. In [2] we introduced a novel integrated tunable filter concept, the interleaved rear reflector. Wavelength control is implemented by the interference between the comb reflection spectra of two electrically isolated but interleaved reflectors. Wavelength tuning is achieved by changing the injection currents in the reflector sections. In our implementation of the concept, the interleaved reflector is formed using short-cavity Fabry-Perot reflector sections realized by partially reflective slots etched into the ridge of a waveguide [3]. The approach yields a compact wavelength tunable source. Placement of the tunable wavelength filter at the rear of the laser cavity enables light emission directly from the gain section, without undesirable attenuation caused by a front reflector. This results in improved output power uniformity across the wavelength tuning range of the device.

In this paper we investigate the fast wavelength switching behavior of the interleaved rear reflector laser. A technique for time resolved spectral analysis is employed to characterize wavelength transition speed and dynamic side mode suppression ratio (SMSR) during wavelength switching events.

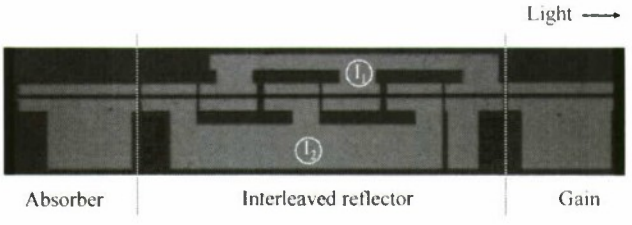

Fig. 1. Interleaved Rear Reflector laser. I_1 and I_2 denote the two interdigitated electrical contacts of the interleaved reflector.

II. Device Design

The device is based on a 5 quantum-well AlGaInAs waveguide. A 2.5 μm wide waveguide ridge provides lateral optical confinement. Slots, etched together with the ridge, provide both the reflectivity and the electrical isolation between the different sections. A photograph of the laser structure is depicted in Fig. 1, where I_1 and I_2 denote the two interdigitated electrical contacts of the interleaved reflector. The absorber section is left unconnected, so the device requires only three drive currents. The structure is based on a single epitaxial growth stage and thus the reflector waveguide is active, providing gain to compensate the loss associated with the slots. The rear reflector consists of six sections separated by the etched reflective slots. The length of the sections alternates between L_1 = 210 μm and L_2 = 219 μm. Light is emitted from the gain section of length L_g = 378 μm through an uncoated facet. The principles on which this was designed are as follows.

Consider a reflector composed of N Fabry–Pérot sections each with section length L_s and with partial reflection between each individual section having field reflectivity r. When two different section lengths are repeated in series with each other, and sections of the same length are electrically connected, one obtains an interleaved reflector. The global field reflectivity ρ_{il} of this interleaved reflector can be calculated by summing up the amplitudes and phases of the reflections from all interfaces. By neglecting all but the first-order reflections of a reflector with N/2 sections of length L_1 and N/2 sections of length L_2, the field reflectivity is

$$\rho_{il} = r \cdot \left(1 + \left(t^4 e^{-j2\beta(L_1+L_2)} + t^2 e^{-j2\beta L_1}\right) \times \frac{1 - t^{2N} e^{-jN\beta(L_1+L_2)}}{1 - t^4 e^{-j2\beta(L_1+L_2)}}\right) \quad (1)$$

with the propagation constant $\beta = 2\pi n_{eff}/\lambda$, depending on the reflector waveguide effective refractive index n_{eff}

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and wavelength of interest λ. The transmission coefficient between sections is given by $t = (1 - r^2)^{1/2}$ for lossless interfaces. Fig. 2(a) shows the calculated power reflectivity spectrum for an interleaved reflector with six sections, three of length $L_1 = 100$ μm and three of length $L_2 = 110$ μm, and a slot field reflectivity of $r = 0.01$. The interference between the two different section length spectra results in spectral modulation envelopes in the reflectivity spectrum, shown as dotted lines in the graph. The alignment of the interfering spectra is controlled by the refractive indexes n_1 and n_2 in the alternating sections and thus common-mode and differential tuning of the wavelength with maximum reflectivity can be realized by means such as current injection. The maximum achievable tuning range is determined by the modulation envelope peak repeat spacing

$$\Delta\lambda_R = \frac{\lambda_c^2}{2n_{\text{eff}}(L_1 - L_2)} \tag{2}$$

with λ_c being the center wavelength of the tuning range. In practice, the gain spectrum of the material used to generate light can also limit the tuning range, so one should match the two ranges to give maximum available tuning. The complete range can be accessed in a quasi-continuous way, if a refractive index contrast of

$$\Delta n = n_2 - n_1 > \lambda_c/(L_1 + L_2) \tag{3}$$

is achieved between the reflector sections. This allows any of the modes in Fig. 2(b) to become the dominant mode.

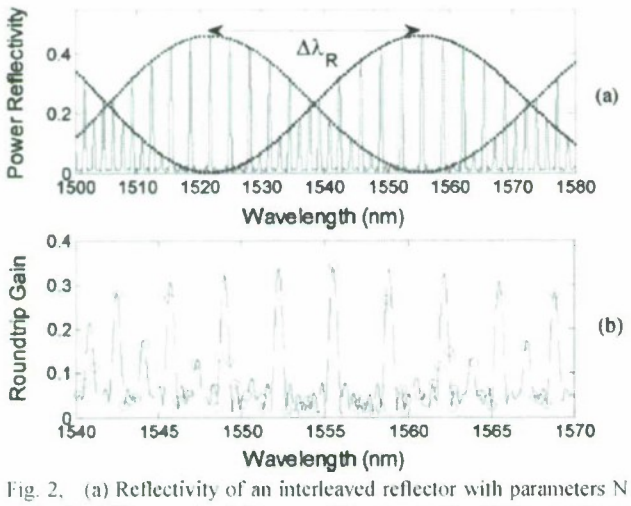

Fig. 2. (a) Reflectivity of an interleaved reflector with parameters N = 6, L_1=100 μm, L_2=110 μm. The maximum tuning range is determined by the modulation envelope repeat spacing $\Delta\lambda_R$. (b) Cold-cavity round-trip gain spectrum of an interleaved reflector laser with cavity mode positions marked with circles. Gain section length is 240 μm.

A distributed reflector has an effective length due to the reflection and attenuation of the light along its length. As light travels through the reflector, it is progressively reflected, scattered and absorbed. Thus in a serial configuration of two reflectors, the front one dominates the reflection. By interleaving the two reflectors we can ensure that both sections receive a significant fraction of the light and are within this effective length and thus contribute to the reflection and the interference effect. This is enhanced further as the sections themselves are electrically pumped and can be biased above transparency. This can compensate for the losses and further ensure that all the sections contribute to the global reflectivity.

Finally, a single-mode widely tunable laser is realized by combining the wavelength discriminating interleaved reflector with a gain section of length L_g and a cleaved output facet. Fig. 2(b) shows the "cold cavity" round-trip gain of an interleaved reflector laser with a gain section of length L_g = 240 μm and reflector section lengths L_1 and L_2 of 100 and 110 μm respectively. The round-trip gain for cavity modes which satisfy the round-trip phase condition is indicated with red circles. Due to the specific location of the modes relative to the round-trip gain, the gain separation between the strongest and all other modes is enhanced with respect to the reflectivity spectrum envelope. The positions of the cavity modes relative to the round-trip gain are also influenced by changing the refractive index of the gain section. This allows for a fine tuning of the gain separation once a desired output mode has been obtained by tuning the wavelength of the reflector using current injection.

III. Experimental Results

Figure 3 shows the SMSR under DC conditions of 37 consecutive wavelength channels on a 100 GHz grid addressable by the laser. The device covers a tuning range of 30 nm from 1546 nm to 1576 nm with SMSR greater than 30 dB.

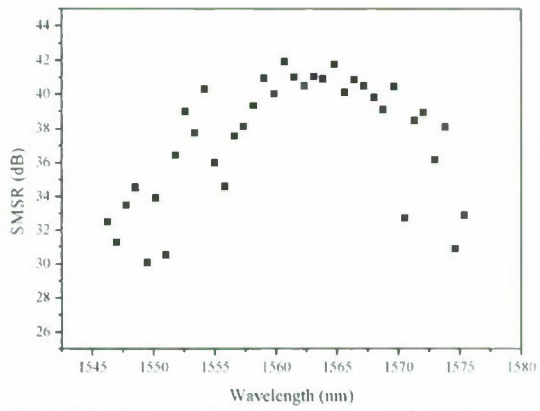

Fig. 3. SMSR of 37 wavelength channels accessible with the laser.

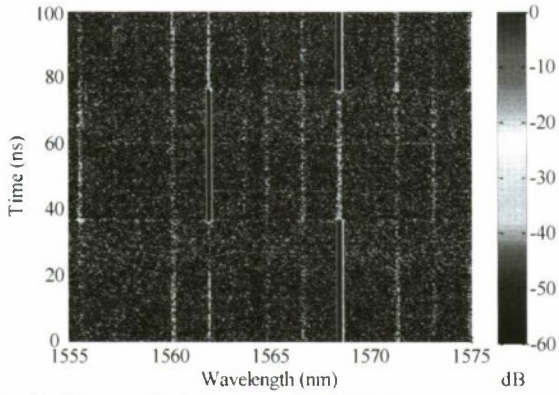

Fig. 4, Time resolved spectrum of switching between two wavelength channels. Multiple side modes are visible in the graph.

Fast wavelength switching was characterized using a heterodyne technique [4]. It is based on the measurement of the transient amplitude envelope of a beat signal between the switched laser and a wavelength tunable external cavity reference laser. By acquiring beat signal traces for different reference laser wavelengths, a time resolved spectrum of the switching event can be obtained. The high sensitivity achieved with the method allows the detection of low power side modes, and therefore the measurement of the dynamic SMSR throughout the wavelength transition.

Figure 4 shows the time resolved spectrum of a switch between two wavelength channels at 1561.4 nm and 1568.4 nm. The spectrum was acquired using a spectral bandwidth of 12 GHz. Apart from the two main channels it shows a number of low power side modes.

Figure 5 shows the transient power at the respective channel wavelengths, where the power is normalized to the steady state peak power. The graph shows the forward transition. The channel transit time is commonly measured as the time that passes between a drop from and an increase to half the steady state peak power. Using this criterion, the transit times for this channel pair is only 60 ps. The high switching speed can be associated with the dominating influence of the stimulated carrier life time in the presented all-active laser design.

Another important measure of the switching speed of a tunable laser is the time span of modal instability during and after a switching event, characterized by multi-modal emission. Horizontal cross sections through the graph in Fig. 4 represent instantaneous spectra of the laser emission. By measuring the SMSR in these instantaneous spectra for each time step the dynamic SMSR can be extracted. Figure 6 shows the resulting data. The laser resumes single mode operation after 1.85 ns and 1.65 ns respectively for the forward and backward transition.

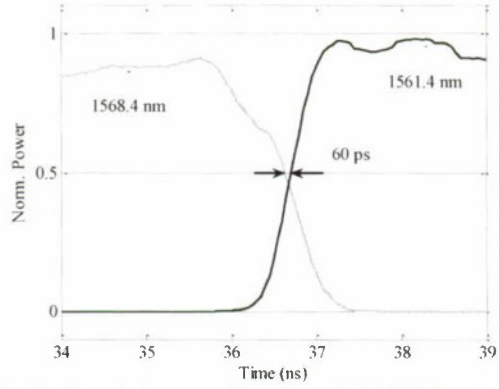

Fig. 5, Transient power of two channels at 1568.4 nm (green) and 1561.4 nm (blue). The half-power transit time is only 60 ps.

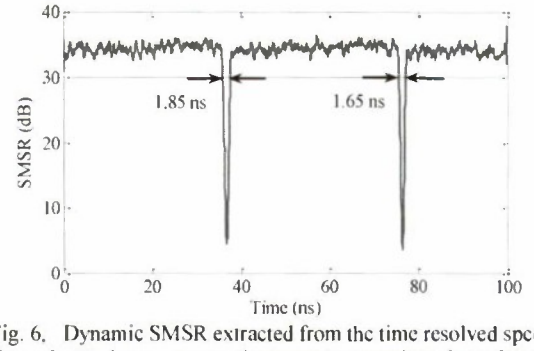

Fig. 6, Dynamic SMSR extracted from the time resolved spectrum in figure 3. The laser resumes single mode operation after 1.85 ns and 1.65 ns respectively for the forward and backward transition.

IV. Conclusion

We investigate fast wavelength switching in interleaved rear reflector lasers, a novel concept for widely wavelength tunable laser diodes. Time resolved spectral analysis of the switched laser shows channel transition times as low as 60 ps and a recovery of stable single mode emission in less than 2 ns.

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Wavelength Trimming of MEMS VCSELs for Post-process Wavelength Allocation

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Abstract

We demonstrate the wavelength trimming of MEMS VCSELs by etching the cantilever-shaped top mirror using FIB. This technique can be used for the post-process precise wavelength allocation of athermal MEMS VCSELs. Experimental results show a possibility of realizing both red-shift and blue-shift wavelength changes by choosing the etching area of the cantilever.

1. Introduction

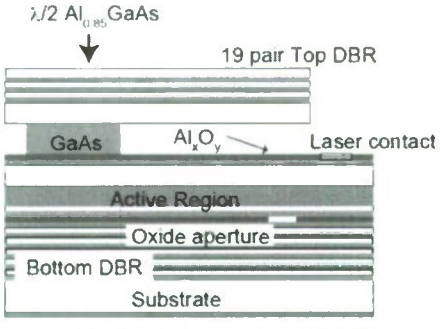
Vertical cavity surface emitting lasers (VCSELs) have been attracting great interest as light sources with low power consumption and small footprint. For further increase in transmission capacity even for short reach links, wavelength division multiplexing (WDM) should be considered. The temperature dependence of semiconductor lasers, which is typically 0.1nm/K for single-mode VCSELs, is a remaining problem to be solved. The elimination of costly thermoelectric controllers is needed for use in low cost WDM networks. If we are able to realize athermal semiconductor lasers exhibiting a fixed wavelength under temperature changes, we expect low power consumption and small packaging in WDM transmitter modules. Tunable VCSELs with micro electro mechanical system (MEMS) have been studied intensively [1-6]. We reported the athermal operation of 1550nm VCSELs with a thermally actuated cantilever based on bimorph effect [7-10]. In addition we present the first demonstration of the athermal and tunable operations of 850nm VCSELs with a newly designed MEMS cavity [11,12]. The athermal operation could be improved by inserting Al_xO_y anti-reflection layer in the cavity. We obtained the extremely low temperature dependence of 0.002nm/K.

Also, the post-process wavelength adjustment, so-called "wavelength trimming" [13], is needed in such athermal VCSELs for precise wavelength allocation. However the wavelengths of athermal VCSELs cannot be controlled with a thermoelectric controller due to their athermal nature. We would like to point out a possibility to change the wavelength by modifying MEMS structure. The cantilever-shaped top distributed Bragg reflector (DBR) can be modified by dry etching, which results in wavelength shifts even after the fabrication. This trimming technique enables the precise wavelength allocation.

In this paper, we demonstrate the wavelength trimming of micromachined GaAs-based VCSELs by post-process etching of a cantilever structure.

2. Design of Athermal MEMS VCSELs

Figure 1 shows the cross-sectional view and scanning electron microscope (SEM) image of the fabricated MEMS VCSEL. The device consists of a top AlGaAs MEMS mirror, an active region including three GaAs/AlGaAs quantum wells and an AlGaAs bottom p-type DBR including an oxide



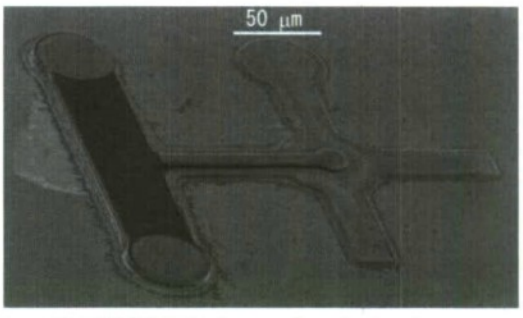


Fig. 1: The schematic and SEM image of the fabricated MEMS VCSEL for wavelength trimming

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aperture, which provides optical and electrical confinement. The top MEMS mirror is a freely suspended cantilever-shaped AlGaAs n-DBR including a 4λ-thick (1.1 μm) $Al_{0.85}Ga_{0.15}As$ stress-control layer at the bottom. The thermal expansion coefficient of the strain control layer is smaller than the average one of DBR. Because of different thermal expansion coefficients in GaAlAs compositions, we are able to obtain the thermal actuation of the cantilever for compensating the temperature dependence of wavelength. The air gap is formed (or the cantilever is released) by selective etching of a GaAs sacrificial layer underneath the cantilever. A similar concept using a stress-induced displacement of the cantilever can be used for wavelength trimming. Because there is an internal stress in the cantilever resulting from different lattice constants in different AlGaAs compositions, we are able to obtain the displacement of the cantilever when it is released. Thus, the displacement changes the air-gap length and hence the lasing wavelength. We can increase or decrease the displacement by controlling the internal stress with dry etching after forming the air-gap.

We newly inserted the Al_xO_y layer which functions as anti-reflection coating. The Al_xO_y layer was formed by using the wet oxidation of $Al_{0.98}Ga_{0.02}As$. In the case of conventional MEMS VCSELs, the wavelength control can be realized by changing the air gap. In order to enhance the tuning efficiency $\Delta\lambda/\Delta d$ (d: the length of the air gap), we found that the reflection at the interface between the air gap and the semiconductor with active region should be reduced [14]. Our proposed structure has an Al_xO_y anti-reflection layer at the interface. The refractive index of Al_xO_y is about 1.5 which is close to that of a perfect AR coating. The proposed structure leads not only the enhancement of wavelength tuning characteristics but also the increase in temperature range of athermal operations. This is because tuning efficiency $\Delta\lambda/\Delta L$ can become nearly constant against the air-gap changes by inserting the Al_xO_y layer. This characteristic also enhances the precise control of the wavelength trimming.

3. Wavelength trimming by post-process etching of the cantilever

If a GaAs sacrificial layer is selectively etched to form the air-gap, the released cantilever end shows the upward stress-induced displacement. This displacement is determined by the cantilever structure

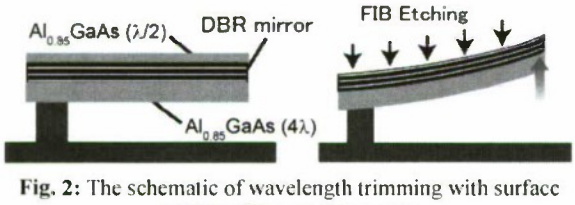

Fig. 2: The schematic of wavelength trimming with surface etching of the cantilever arm.

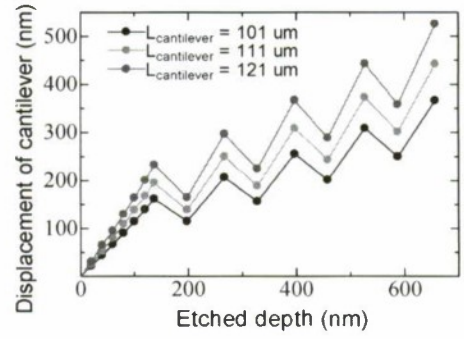

Fig. 3: Calculated displacement of the cantilever as a function of etched depth.

and is given by

$$\Delta d = \frac{3 \cdot t_{DBR} \cdot t_{scl} \cdot L_{cantilever}^{2} \cdot \varepsilon(\Delta a)}{(t_{DBR} + t_{scl})^{3}} \qquad (1)$$

where t_{DBR} is the thickness of DBR, t_{scl} is the thickness of the strain control layer, $L_{cantilever}$ is the length of the cantilever, Δa is the difference of lattice constants of DBR and the strain control layer and ε is the stress induced by lattice mismatch. The displacement can be changed by modifying the cantilever structure using the post-process FIB etching technique.

Figure 2 shows the schematic of post-process etching for "wavelength trimming". The left and right figures show the cantilever before and after FIB etching respectively. We have about 135 nm-thick $Al_{0.85}Ga_{0.15}As$ layer at the top of DBR mirror for etching protection. When the arm of a cantilever is etched to reduce the thickness of DBRs, the stress-induced displacement is increased due to the increased vertical asymmetry. The upward displacement results in the red-shift due to the increased the air-gap. We calculated the displacement of the cantilever as a function of the etched depth as shown in Fig. 3. While the top $Al_{0.85}Ga_{0.15}As$ layer is etched, the displacement is increased monotonically with the etched depth. If we continue to etch DBR layer, the displacement periodically changes with a period of one DBR pair. This is because average Al composition of DBR layer changes with the etched depth. Despite the periodic change, the figure

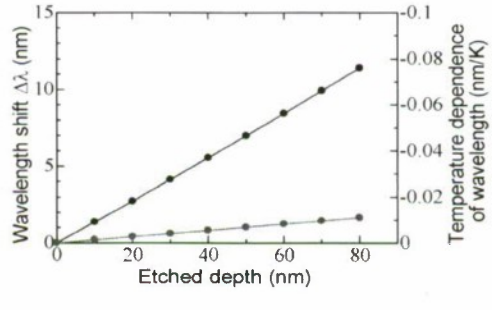

Fig. 4: Calculated wavelength shift and temperature dependence of wavelength as a function of etched depth.

indicates that we can increase the displacement of the cantilever by thinning DBR layer. An etched depth of 100 nm of DBR layer gives us a displacement of above 110 nm and a wavelength shift of about 10 nm if we assume tuning efficiency $\Delta\lambda/\Delta d$ is 0.088. The amount of this shift indicates that etching of the top $Al_{0.85}Ga_{0.15}As$ layer is sufficient for wavelength trimming that we propose.

The temperature dependence of wavelength $\Delta\lambda/\Delta T$ also should be considered when the wavelength trimming is carried out. Our proposed VCSELs with a thermally actuated cantilever enable us to control $\Delta\lambda/\Delta T$ by means of differences of thermal expansion coefficients between DBR layer and the strain control layer. Therefore $\Delta\lambda/\Delta T$ depends on the cantilever structure. If we etch DBR layer for their wavelength trimming, the displacement caused by temperature changes $\Delta d/\Delta T$ may break out the athermal condition. We calculated how the wavelength trimming effects on the athermal operation as shown in Fig. 4. We assumed a 121 μm-long cantilever for athermal operation. As the wavelength is shifted from initial one with the reduced thickness, the temperature dependence of wavelength $\Delta\lambda/\Delta T$ is increased from the athermal operation. If we allow $\Delta\lambda/\Delta T$ to be 0.007 nm/K (10 times smaller than conventional VCSELs), we can get a wavelength shift of above 7 nm with such a small $\Delta\lambda/\Delta T$.

4. Fabrication Process

Figure 5 shows the fabrication process. The process includes the formation of a cantilever structure, VCSEL mesa etching, the oxidation process which forms oxide confinement and anti-reflection layer, metal deposition and finally cantilever release by selective etching using citric acid. Cantilever structures and VCSEL mesas were formed by inductively coupled plasma (ICP) dry etching. An Al_xO_y anti-reflection layer can be formed by a lateral wet-oxidation of a 140-nm-thick epitaxial $Al_{0.98}Ga_{0.02}As$ during the formation of oxide apertures for optical and electrical confinement. No extra fabrication process is needed. The small circles, which eventually contain the base of the cantilever, are 20 μm in diameter while the larger bottom mesas are 60 μm in diameter, requiring ~25 μm of lateral oxidation. The entire $Al_{0.98}Ga_{0.02}As$ anti-reflection layer was oxidized at 480 °C leaving an unoxidized aperture (~10 μmϕ) at the center of the larger bottom mesa. We used Ni/Ge/Au as a top contact and Au/Zn/Au as a bottom contact [15]. The air-gap is formed by highly selective citric-acid-based chemical etching of a GaAs sacrificial layer underneath the cantilever [16, 17]. After removing the sacrificial layer by selective etching the wafer was dried with boiled acetone in order to avoid a stieking problem. We fabricated a freely suspended 120 x 10 μm^2 cantilever as shown in Fig. 1.

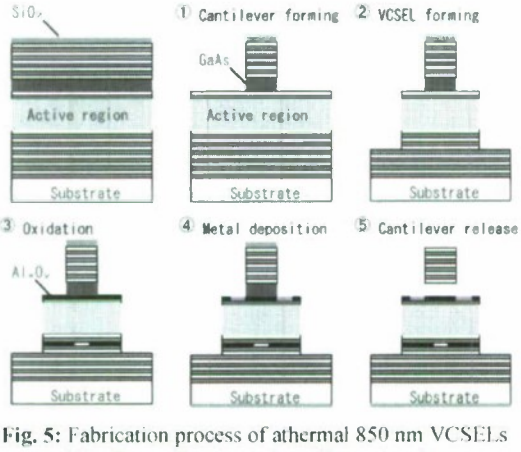

Fig. 5: Fabrication process of athermal 850 nm VCSELs with a thermally actuated cantilever structure.

5. Measurement

We carried out the post-process etching of the cantilever structure to change the displacement for "wavelength trimming". Also, we can obtain the downward displacement by etching the edge of the cantilever without the degradation of mirror reflectivity. This is because the stress relaxation along the cantilever takes place with the stress-induced bending in the perpendicular direction by etching the side of the cantilever end. As a result we can realize both the red-shifted and blue-shifted wavelength changes using the post-process etching

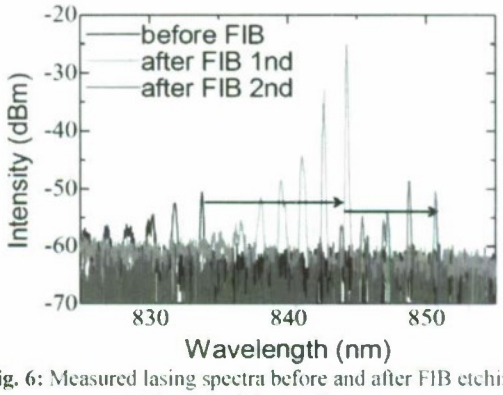

Fig. 6: Measured lasing spectra before and after FIB etching of the arm of the cantilever.

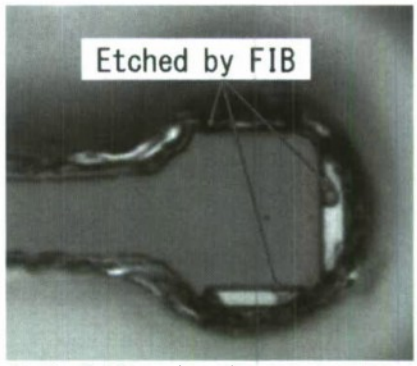

Fig. 7: The SEM top view of an etched cantilever for wavelength trimming.

technique.

We etched the arm of the cantilever by FIB, which leads to the reduction in the thickness. The post-process etching of less than 200 nm results in wavelength shifts of 15 nm. Figure 6 shows the measured spectra before and after two-steps FIB etching. This figure indicates multi-mode operations due to its large oxide aperture, but single-mode operation could be obtained by reducing the oxide aperture size. Output power was changed depending on their resonant wavelengths because its gain or reflectivity is changed. However we expect that we may avoid the changes of laser performances when the wavelength shift is a few nm in practical applications. We realized red-shifts of about 10 nm and 6 nm in the first and second step etching of the cantilever arm, respectively. We also etched the edge of a cantilever end to get blue-shifts. The SEM view of the etched cantilever is shown in Fig. 7. Etched depth was about 550 nm, which corresponds to 4.5 pairs of DBRs. As shown in Fig. 8, the lasing wavelength was blue-shifted by the post-process etching. These results indicate that we can make post-process wavelength control either with red-shift and blue-shift by choosing the etching area of the cantilever structure.

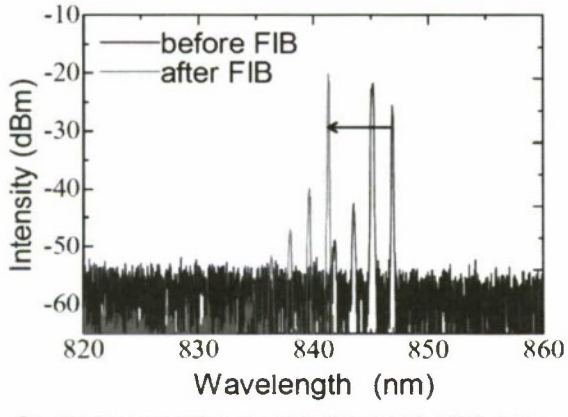

Fig. 8: Measured lasing spectra before and after FIB etching of the edge of the cantilever.

6. Conclusions

We proposed and demonstrated the wavelength trimming of MEMS VCSELs for post-process precise wavelength allocation. We realized both red-shift and blue-shift wavelength changes by choosing the etching area of the cantilever. The proposed concept would be useful for precise wavelength engineering of athermal MEMS VCSELs.

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OPTICAL COUPLING OF PLANAR III-V PIN PHOTODIODES AND SOI WAVEGUIDES USING AN INTEGRATED BCB PRISM

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Abstract

Vertical hybrid integration of photodiodes (PD) and silicon-on-insulator (SOI) waveguides has been investigated. To this end, InP-based planar detectors were used onto which a polymer prism was formed to turn the light beam into the vertical direction. The photodiodes were flip-chip mounted onto a SOI waveguide platform using thermo-compression bonding. Comparable high responsivity of around 0.75 A/W was obtained when light was coupled directly into the prism as well as via a SOI waveguide. The responsivity for SOI integrated PDs was found to depend only to a minor extent on input wavelength and polarization. PD bandwidth of up to 10 GHz was measured. The investigated optical coupling scheme proved to work well also when integrating a PD with an array of ten SOI waveguides which are combined with a star coupler.

I. Introduction

Silicon on insulator (SOI) represents a versatile integration platform for the implementation of advanced photonic integrated circuits comprising III-V compound semiconductor based optoelectronic devices such as lasers, SOAs, modulators, and detectors as active building blocks. To benefit from the advantages of both material systems when combining them by hybrid integration, an efficient yet simple method for optical coupling is necessary. In the case of photodiodes (PD) light deflection by about 90 ° represents a straightforward way to direct the output of a SOI waveguide onto a planar surface-mount pin PD. To this end turning 45° mirrors have been shown to be a viable solution in other material systems. In SOI, however, formation of such mirrors in conjunction with creating a vertical waveguide facet at low distance to the mirror is hard to achieve. In the present work, as an alternative method for turning the optical beam total reflection in a prism formed on top of the PD is exploited. The advantage of this optical coupling method is its relative simplicity compared to other methods, e.g. wafer bonding of III-V PDs on SOI or use of other sophisticated PD or SOI structures including grating couplers. In our study established PD structures have been used instead which were adapted to thermo-compression based flip-chip bonding and onto which a benzo-cyclo-butene (BCB) prism was formed to accomplish the vertical optical coupling.

Thermo-compression (TC) bonding between thin Au-pads excels other available bonding techniques regarding horizontal (±0.5 µm) and vertical (±0.1 µm) alignment accuracy, achievable without special stand-off or alignment feature requirements. Another advantage is that in principle any form and size of contact pads can be used, although some limitations may arise in practice. This method already has been successfully used to integrate lasers and SOA arrays with optical low loss onto a SOI waveguide platform using a commercial flip-chip bonder (1, 2).

In this paper we report on the technology and performance of such flip-chip mounted PDs with integrated prism. This work is part of an ongoing ESA project aiming at the realization of a 100 × 1 wavelength channel selector device, based on spatial channel redistribution by a series of periodic arrayed waveguide gratings (AWGs). The advantages of hybrid integration are evident for this proof-of-concept demonstration in that the fabrication of active components and of the waveguide platform are separated to allow for optimization of the individual devices, and faster and simpler development cycles. As the active components are integrated on a SOI chip, the technology is compatible with wafer level packaging and small-scale production.

II. Device Structure and Processing

The integration concept is depicted in ***Fig. 1***. The horizontal and vertical dimensions are not drawn to the same scale; in reality the prism is designed with a slope angle of 10 ° to 20 °.

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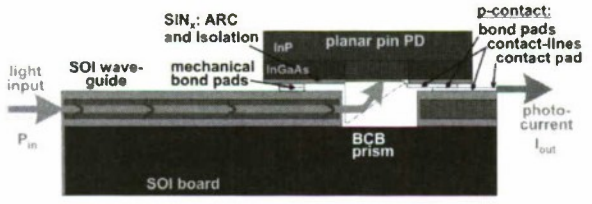

Fig. 1: The principle of optical coupling used for the integration of a planar PD onto an optical SOI platform.

A planar-type PD with a 2 µm thick InGaAs absorption layer on InP was used. The BCB prism was directly formed to the sensitive area. Light emitted by the SOI waveguide is captured by the prism and reflected upwards by total reflection at its sloped face (angle for total reflection in BCB: 41 °) and finally enters the PD absorption layer.

Layers made of BCB resins possess excellent optical quality (3), as exploited in micro-optical devices (4). The BCB prisms were fabricated by lithographic techniques: After spin-on coating of the BCB resin and curing a resist mask with thickness tapered sections is deposited on the BCB layer. The resist tapers were made by contact lithography employing a sliding mask technique (5). Subsequently the relief is transferred into the BCB layer by a dedicated RIE process utilizing an O_2 containing plasma. By controlling the movement of the lithographic mask during exposure and adjustment of the BCB layer thickness a wide range of prism parameters can be realized. This is particularly important as the design of the prism influences the polarization behaviour. A surface profiler scan over a fabricated BCB prism is depicted in ***Fig. 2***.

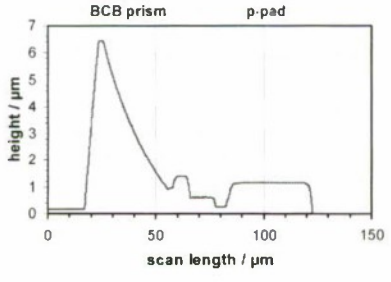

Fig. 2: Surface profiler scan across ar BCB prism and p-contact pad. The shape of the stylus distorts the slope of the prism input facet, being steeper in reality.

Due to the high refractive index difference between BCB (n = 1.54) and InGaAs (n = 3.6), respectively, an AR coating is required to reduce the reflection losses at the BCB/InGaAs interface. Furthermore, if properly designed in conjunction with an appropriate prism slope, a weak dependence on wavelength and polarization is possible. Therefore, a SiN_x layer was deposited on top of the light-sensitive area before BCB prism fabrication, reducing reflections from around 20% to practically zero. The BCB input facet was not AR-coated due to the high difficulty in realizing such a process.

A microscope image of a fabricated PD chip is shown in ***Fig. 3***. The prism appears as a dark rectangle because of an artefact from microscope illumination. The footprint of the chip is 500 × 500 µm^2 to ease handling during bonding. The actual functional area of the PD is only some 100 × 100 µm^2. Close-up SEM views of the active part of a fabricated PD including the BCB prism are depicted in ***Fig. 4***. Although some residual roughness is clearly visible on all surfaces, no significant adverse effect on optical coupling was found.

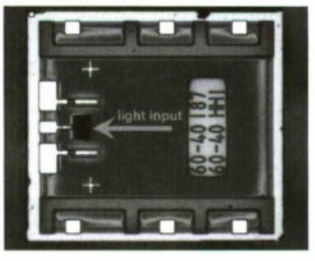

Fig. 3: Microscope view on a finished PD chip. The light-sensitive area is located directly below the dark rectangle being the BCB prism.

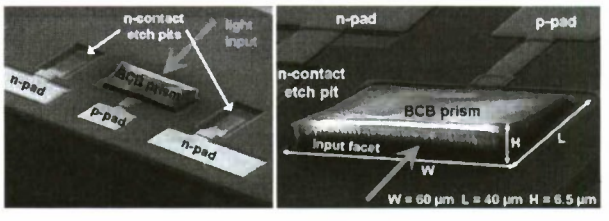

Fig. 4: SEM images of the PD's functional area (left) and the BCB prism (right). Note the different viewing directions in both pictures.

For high-speed opto-electronic devices all electrical contacts must preferably be accessible on the chip surface. For the chosen planar PD design the n-contact layer is accessed from the chip surface via etch-pits nearby the light-sensitive area and contacted via an appropriate metallization, leading to the n-contact pads on the chip surface (see ***Fig. 4***). Additional six bonding pads without electrical function ("mechanical pads") are attached at the chip edges in order to increase the reliability of mounting and optical alignment. They increase the bondable surface area and support the PD chip evenly and are located at the upper and lower chip edges as seen in ***Fig. 3***.

The PD contact pads allow on-chip RF testing of the PDs with probeheads and fit to the connection line on the SOI detector mount. Additionally, they are used as stand-offs for vertical alignment in flip-chip mounting with TC-bonding. Therefore all pad surfaces lie on the same level with high precision in order not to complicate the fabrication of their counter-parts on the SOI chip and to realize the minimum vertical alignment tolerances possible with TC bonding.

To realize the PD-on-SOI arrangement by flip-chip mounting a specially designed PD mount is necessary, realized on a

4 µm thick SOI waveguide platform. The design of the mount is adapted to the layout of the PD chip surface, including the prism.

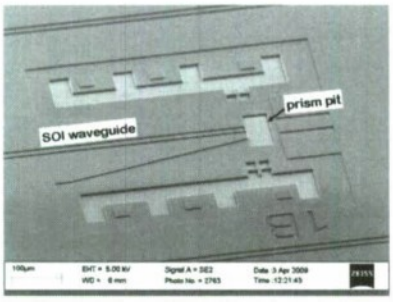

Fig. 5: SEM image of a fabricated PD mount with single SOI waveguide input, taken prior to Au sputtering.

Fig. 5 shows a SEM view on such a fabricated PD mount. Deep and shallow etch pits accommodate the PD surface topology, at the same time forming the SOI waveguide output facet with one sidewall.

Fig. 6: Layout of the investigated waveguide array/star coupler/PD mount test structure.

At the end of the future channel selector device the optical output signal is directed into one of ten adjacent waveguides, depending on the setting of the channel selector switches. Each of them has to couple its guided signal with low loss into a single PD, providing the electrical output for one output channel. To this end all waveguides in the array constituting the optical output channel are combined by means of a low-loss star coupler ***Fig. 6*** depicts the layout of the investigated waveguide array/star coupler/PD mount test structure.

The targeted bandwidth of 10 Gbit/s demands a suitably low capacitance of the space-charge region in the absorption layer. Optical coupling efficiency on the other hand requires a large light-sensitive area in order to collect most of the light emitted by the SOI waveguide(s) and deflected by the BCB prism. The footprint of the light-sensitive area is determined by the design of the BCB prism.

In order to achieve low loss optical coupling even for waveguide arrays the width of the prism has to match the size of the incoming optical beam. Based on BPM simulations, prism widths of 40 µm, 60 µm, and 90 µm were selected for fabrication. The lowest value represents the lower limit for effective coupling with the waveguide combiner output. The larger ones provide a larger acceptance width, allowing for increased tolerance in alignment and processing, however, the resulting electrically active area of the PD increases significantly and consequently the bandwidth of the PD decreases.

III. Performance

First the responsivity of discrete PDs with integrated BCB prism was measured by injecting light from a tapered fibre tip into the prism input facet, the polarization and wavelength dependence was also determined, see ***Fig. 7*** and ***Fig. 8*** for examples. The observed mean responsivity value of around 0.75 A/W represents a reasonably good value, as 0.85 A/W is expected for direct PD illumination from simulation. Deviations from this reference value mainly originate from the optical losses due to prism coupling, such as reflective loss at the BCB input facet (~5 %), absorption, scattering, insufficient collection by the prism, etc. Virtually no difference is measured for TE and TM (see ***Fig. 7***). Without AR coating and suboptimal prism shapes a difference of 20 % would be expected (according to simulation). The variation with wavelength amounts to about 6 % (see ***Fig. 8***).

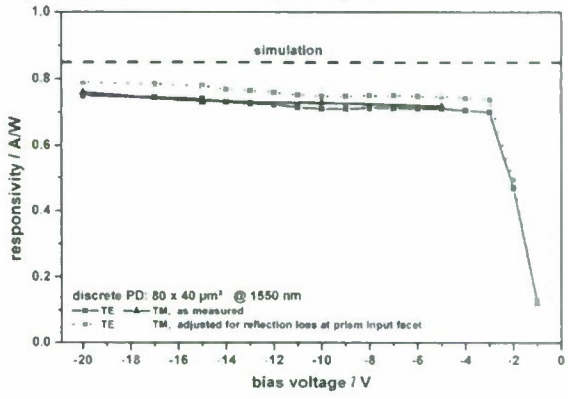

Fig. 7: Responsivity of a discrete PD with integrated BCB prism in dependence on bias voltage and polarization, measured for 1550 nm light input via the prism.

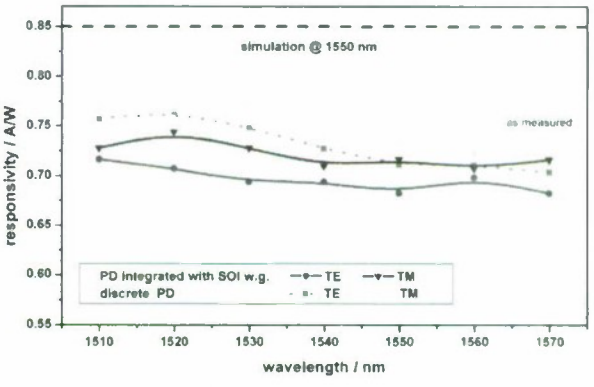

Fig. 8: Responsivity of a 40×40 µm² prism PD integrated with a single SOI waveguide, in dependence on wavelength and polarization. Also shown are the results for a discrete 60×40 µm² prism PD.

Fig. 8 additionally shows the wavelength dependent responsivity of a 40×40 µm² prism PD integrated with a single SOI waveguide. The same tapered fibre tip was used, now launching light into the AR coated SOI waveguide facet. The

observed decrease in responsivity compared to the discrete reference PD is caused by the additional optical losses due to mounting. These mainly include SOI waveguide propagation loss in this case less than 0.1 dB, coupling loss between SOI waveguide and BCB prism and the difference in fibre coupling loss for launching the light into the prism or into the SOI waveguide, respectively.

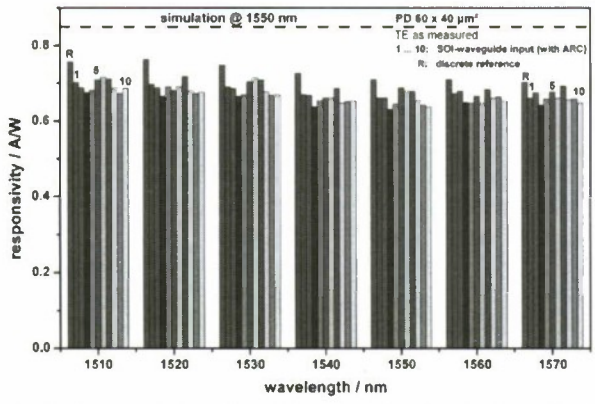

Fig. 9: Responsivity of a 60 × 40 µm² prism PD, optically coupled to an array of ten SOI waveguides.

Fig. 9 depicts the results of a 60×40 µm² PD coupled to an array of 10 SOI waveguides, measured with TE light launched into one waveguide after another. A fairly high uniformity was measured for the responsivity in this case with variations of only ± 0.06 A/W. Almost the same responsivity values are achieved as in the case of integration to a single SOI waveguide. A similar characteristic is observed for TM polarization, but at slightly increased values corresponding to the other results depicted in ***Fig. 7*** and ***Fig. 8***.

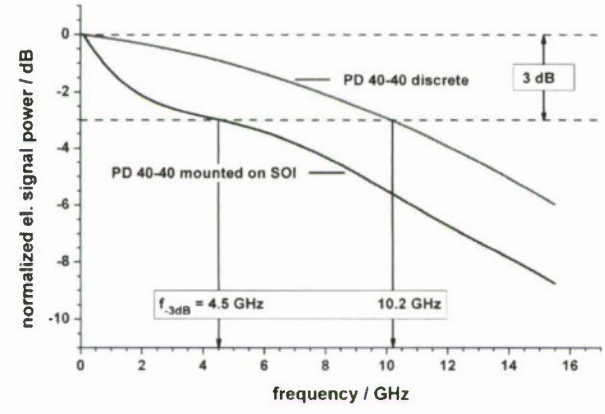

Fig. 10: RF performance of a 40 × 40 µm² prism PD, measured for a discrete and a SOI integrated device.

The RF performance of a 40×40 µm² prism PD evaluated by optical heterodyne measurements is shown in ***Fig. 10***. A -3 dB bandwidth of more than 10 GHz is measured for a discrete PD. The mounting of such a PD onto a SOI chip was found to deteriorate the -3 dB bandwidth significantly, only a bandwidth of 4.5 GHz was measured in this case. This bandwidth reduction is mainly caused by the non-optimized RF line on the SOI detector mount, being in close proximity to low resistivity silicon (10 to 20 Ωcm). This poor RF-line performance can however readily be improved by using wafers with higher resistivity of at least 100 Ωcm.

IV. Conclusion

A viable solution for integrating a SOI waveguide platform with InP-based planar PDs using prism coupling and thermocompression bonding was demonstrated. The presented results show that the prism coupling scheme works effectively, regardless of slight residual roughness of the prism surfaces and non-ideal prism shapes.

Discrete photodiodes with prism input from a tapered fibre show an almost polarization independent responsivity as high as 0.75 A/W with low variation for wavelengths between 1510 nm and 1570 nm. Integration of such a prism PD with a SOI waveguide was found to impact this performance only very slightly, even in case of an array of ten SOI waveguides combined with a star coupler placed in front of the PD. This arrangement enables a coupling efficiency almost independent from input waveguide position when using 60 × 40 µm² prism PDs.

To guarantee a bandwidth of the integrated PDs suitable for 10 Gb/s data processing SOI material with high resistivity is necessary. As prism fabrication is done on wafer-level as a separate step in the PD fabrication, no sophisticated PD or SOI structures are demanded and the PD properties are virtually not affected.

Acknowledgement

We thank Airi Weissenfelt and Miia Aitta for their great help in flip-chip bonding, and Simon Merz for his valuable support in BCB-RIE. This work has been funded by the European Space Agency (ESA) under ESTEC contract No 20174/06/NL/PM (OTUS, ARTES5).

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Lateral Junction Waveguide Type Photodiode for Membrane Photonic Circuits

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Abstract

A lateral junction type photodiode grown on a semi-insulating InP substrate was realized by 3-step OMVPE growth. The responsivity of 0.27 A/W, 3 dB bandwidth of 6 GHz and 7.5 GHz at a bias voltage of 0 V and -2 V, respectively, were obtained for the stripe width of 1.4 μm and device length of 220μm. An error free transmissions up to 6 Gbps at 0 V were confirmed.

Keywords- Photodiode, Waveguide, Lateral junction, Membrane photonic circuits.

I. Introduction

Higher computing performance has been achieved due to the progresses of device densities and operation speed by scaling down CMOS transistor size to follow Moore's law. However, further performance improvement will be limited by both power consumption due to heat generation [1] of the global metal interconnect and operation speed due to the RC delay [2]. To solve this problem, a lot of works on an optical interconnection that replaces the electric wiring have been pursued [3]-[5]. Moreover, the optical interconnection is expected to have low electromagnetic noise property.

To realize the optical interconnection on LSI, low power consumption and compact optical active devices such as lasers, amplifiers, and detectors are needed. For this demand, we have proposed a membrane distributed-feedback (DFB) laser, which consists of a thin (~ 150 nm-thick) semiconductor core layer including active regions with grating sandwiched by low-index polymer cladding layer [6]. The membrane structure has a strong optical confinement into the core layer and allows lasing operation with very low threshold. So far, a low threshold optical pump power (0.34 mW) with a stable single-mode operation was demonstrated under room-temperature continuous-wave (RT-CW) condition [7]. With the aim of realizing injection-type membrane lasers, a lateral current injection (LCI) structure [8] was adopted and RT-CW operation of LCI buried-hetero structure (BH) lasers with 400-nm-thick GaInAsP core layer grown on a semi-insulating (SI) InP substrate has been demonstrated [9],[10]. This membrane structure is also attractive for waveguide type photodiodes because the device length can be shortened due to its high optical confinement structure compared with previously reported photodetectors with a lateral junction [11], hence higher speed operation due to a feature of low capacitance will be expected.

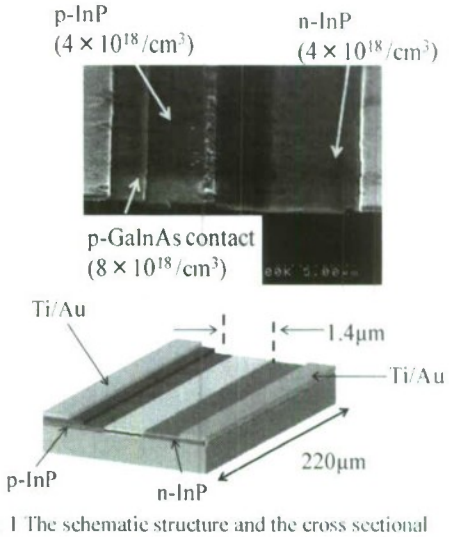

Fig. 1 The schematic structure and the cross sectional SEM view of the device.

In this paper, we would like to present fundamental properties of a lateral junction waveguide type photodiode with thin current injection layer thickness.

II. Device Structure and Fabrication

The schematic structure and the cross sectional SEM view of the fabricated device structure are shown in Fig. 1 and the fabrication process are shown in Fig. 2. An initial wafer with undoped GaInAsP core layers consisting of five quantum-wells (QWs, $Ga_{0.22}In_{0.78}As_{0.81}P_{0.19}$, 6 nm thick), barriers ($Ga_{0.26}In_{0.74}As_{0.49}P_{0.51}$, 10 nm thick) and optical confinement layers (OCLs, $Ga_{0.21}In_{0.79}As_{0.46}P_{0.54}$), were prepared by organo-

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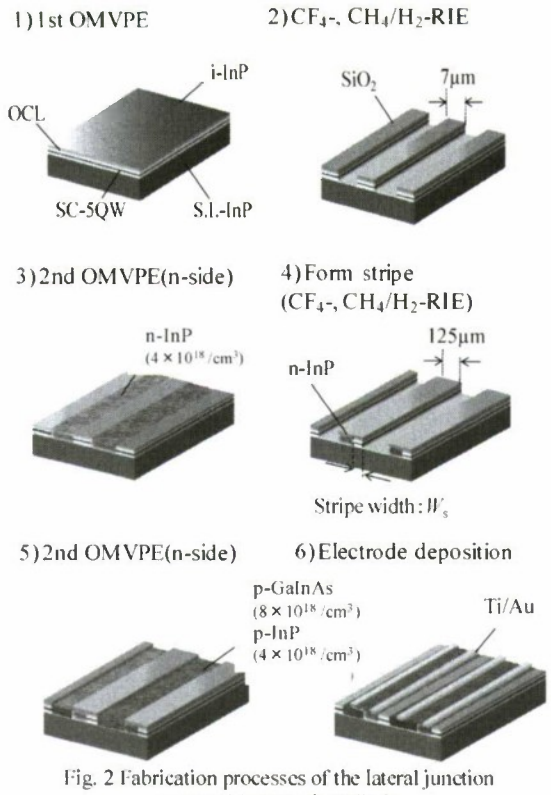

Fig. 2 Fabrication processes of the lateral junction waveguide type photodiode

metallic vapor-phase-epitaxy (OMVPE) on an Fe-doped SI-InP substrate. The total GaInAsP layer thickness was 380 nm. Then, the lateral junction structure was fabricated by reactive-ion-etching (RIE) and 2-step OMVPE selective area growth [12]. First, a mesa stripe structure with 7-μm-wide and 380-nm-high was formed with a SiO_2 mask. After removing plasma damaged sidewall by sulfuric acid based solution, n-InP ($N_D = 4 \times 10^{18}$ /cm^3) was selectively regrown at the side of the mesa as a cladding layer. Next, by etching the part of the wide mesa and the one side of the buried n-type layer in the similar way, narrow (1.4-μm-wide) stripes were formed. Then, p-InP ($N_A = 4 \times 10^{18}$ /cm^3) cladding and p-GaInAs contact layers were regrown in a similar way. After that, the part of the GaInAs contact layer near the stripe edge was removed by sulfuric acid solution to reduce optical absorption. Finally, Ti/Au electrode was deposited on both the p-GaInAs contact and the n-InP sections with spacing of 16 μm.

III. Experimental Results and Discussion

As cleaved device with the length and the stripe width of 220 μm and 1.4 μm, respectively, was used for measurements. The spectral response of the photocurrent was measured by using tunable lasers, which can be scanned from 1420 nm to 1620 nm.

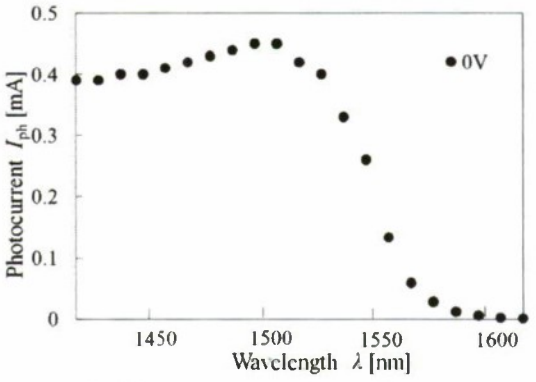

Fig. 3 Input power dependence ofphotocurrent.

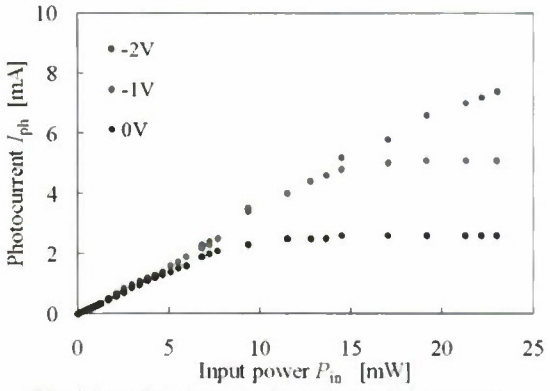

Fig. 4 Input light intensity dependence of photocurrent.

and a polarization controller to couple TE-polarized light as shown in Fig. 3. The input power coupled to the waveguide was estimated to be around 0.85 mW with consideration that the output power of 2 mW from lensed fiber and -3.7 dB coupling loss between the fiber to the device. Figure 4 shows input power dependence of photocurrent, I_{ph}, at a bias condition of 0 V, -1 V, and -2 V, where I_{ph} was obtained by subtracting the dark current from the total current. The dark current at -2 V was 660 nA which is not sufficiently low for the device size. From these values the responsivity of the device is estimated to be 0.27 A/W at the wavelength of 1550 nm, which is around 1/5 of typical GaInAs/InP photodiode [13], because the initial wafer was designed for 1.55 μm wavelength laser, hence the absorption coefficient at this wavelength is low as shown in Fig 3. Design modifications for photodiode, such as GaInAs bulk material as an absorption material instead of 1.55μm QWs or using anti-reflection coating, will be required for higher responsivity.

The frequency response of the device is shown in Fig 5. An electrical signal from a network analyzer was converted into a light signal with a network performance tester in which a LN modulator and a DFB laser were built, then the light signal was converted into an electrical signal with the lateral junction

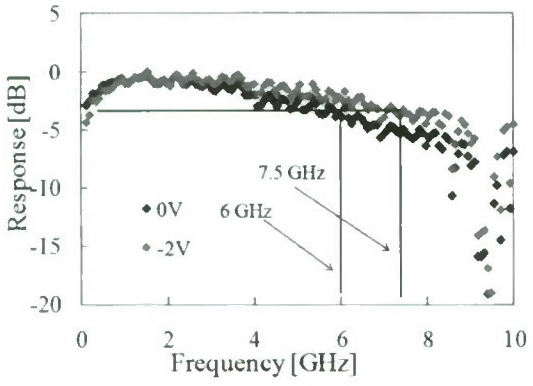

Fig. 5 Frequency response of the waveguide type lateral junction photodiode at bias voltages of 0 and -2 V.

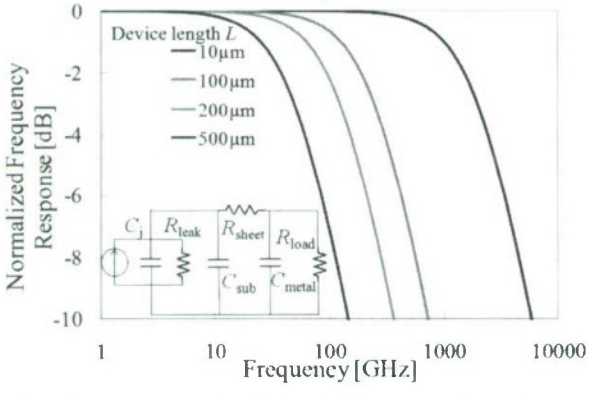

Fig. 6 Frequency response of 1 μm wide waveguide device in terms of RC limitation.

photodiode. The signal calibration of S_{21} characteristics of the network analyzer has been done under the consideration of electrical cable characteristics. Current-voltage conversion was just done by internal 50-ohm impedance in the network analyzer. The low response at low frequency side (< 1 GHz) might be due to the impedance mismatching between the device and submount. The 3dB bandwidth was observed to be 6 GHz at non-bias condition and 7.5 GHz at the bias condition of -2 V when it was measured from the peak response. The speed of the device was limited by the transit time of holes in the GaInAsP QCL or by RC time constant because of relatively long distance between electrodes and thin (380 nm) carrier transport channel.

Figure 6 shows the calculated frequency response for several device lengths limited by only the RC time constant. The intrinsic response is modeled as a current source in parallel with a junction capacitor and resistance derived from leakage current. The diode series resistance, parasitic capacitances in the substrate and metal [14], and load resistance form the external circuit. From this calculation, more than 40 GHz bandwidth is expected even for the device length longer than 500 μm. On the other hand, the

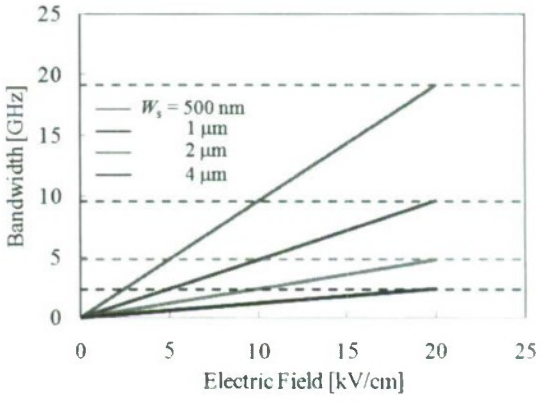

Fig. 7 Bandwidth calculated from carrier transit time under applied electric field..

bandwidth dependence on the applied electric field limited by the transit time of holes is shown in Fig. 7. Though the bandwidth can be increased by applying voltage, the carrier velocity is saturated at a point. The dashed lines show the bandwidth limitation of each waveguide width defined by the saturation velocity. In this calculation, the saturation velocity of holes in GaInAs was assumed to be 6.0×10^6 cm/s [15]. To obtain higher speed operations, one simple solution is narrowing waveguide width less than 500 nm [16]. Another solution is applying the Uni-Traveling-Carrier (UTC) structure which uses only electrons as its active carriers [17].

Figure 8 shows bit error rate (BER) measurement results and eye diagrams at 6 and 10 Gbps. Clear eye opening was obtained up to 10 Gbps when biased with -2 V. The pseudo random bit sequence (PRBS) non-return-to-zero (NRZ) signal with the word length of 2^{31}-1 from a pulse pattern generator was converted into light signals with the performance tester and input to the photodiode, then electrical signal from the device was measured by the error detector. The horizontal axis contained the coupling loss of 3.7 dB and the loss in measurement system of -4 dB, respectively. Error free back-to-back transmissions were obtained from 1 Gbps to 6 Gbps at non-bias condition. However, the averaged received power for this measurement was so high due to its poor responsivity which can be improved by adopting an appropriate design of the device.

IV. Conclusion

As a candidate for membrane photonic circuits, waveguide type lateral junction photodiode with considerably thin layer was realized on a SI-InP substrate. The responsivity of 0.27 A/W, 3dB bandwidth of 6 GHz at 0 V and 7.5 GHz at -2 V, and an error free detection up to 6 Gbps at 0 V were obtained for the stripe width of 1.4 μm and the device length of 220 μm. Further

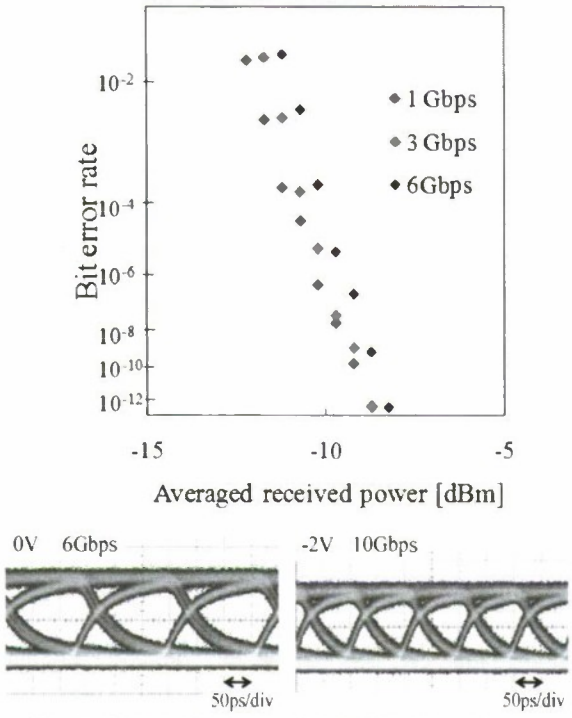

Fig. 8 BER measurements at 0Vcondition and eye patterns.

investigations for high-speed and high responsivity operation will be required.

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High Gain InAs Electron-Avalanche Photodiodes for Optical Communication

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Abstract

We report the avalanche properties of InAs avalanche photodiodes (APDs), extracted from avalanche gain and excess noise measurements performed under pure electron and pure hole injections, and from Monte Carlo simulations. For a given avalanche width electron initiated gain was found to be significantly higher than conventional InP and Si APDs. Hole initiated multiplication was negligible confirming the electron only multiplication process within the field range covered. Excess noise measurements showed the excess noise factors of less than 2, providing further evidence of the ideal avalanche properties in InAs. Monte Carlo simulations performed provided good agreement to experimental results.

I. Introduction

The explosive growth of the internet has increased the demand for highly sensitive optical detectors for high-bit-rate optical fibre communication systems. For operation at the low loss wavelength of 1.55μm InGaAs pin diodes grown on InP substrates have been the preferred choice. However at best, a pin diode can generate only one electron-hole pair per incident photon and therefore a pre-amplifier is needed for low light level detection. This limitation can be overcome by using avalanche photodiodes (APDs), in which internal detector gain is provided via avalanche multiplication. Since impact ionization is random in nature, fluctuations in the multiplication factor or gain, M, are inevitable, resulting in excess avalanche noise, characterized by the excess noise factor F and variation in the avalanche duration, D_a. At high frequencies the associated noise may still be less than that of a pre-amplifier, provided that F is small. Thus an optimized low noise APD can provide significantly higher signal to noise ratio than a pin diode-following amplifier combination. However at high gain, for example above 10, D_a can vary from a single carrier transit time, τ (when carriers fail to impact ionize) to well over 10τ (when M is large) [1] leading to low bandwidth and significant intersymbol interference (ISI) when the bit duration is comparable to D_a. Therefore an ideal APD should have $F = 1$ and small D_a.

F and D_a are predominantly determined by the electron and hole ionization coefficients, α and β respectively [2,3]. When β (or α) approaches zero $F \sim 2$ and $\tau \leq D_a \leq 2\tau$ are obtained. Unfortunately current commercial InGaAs/InP APDs have effective β/α ratio reported to be 2.5-4 [4] leading to gain-bandwidth products of 100-180GHz with a significant spread in D_a. Consequently they are suitable for bit rates up to 10Gb/s. To operate at higher bit rates while maintaining a sufficiently high value of M a material with much larger effective ionization coefficient ratio, k_{eff}, is required. InAlAs with k_{eff} = 4-6.7 [5] has been investigated as a replacement for InP multiplication region. While both the excess noise and bandwidth performance are improved over InP, InAlAs is still incapable of providing direct detection at high bit rates higher than 10Gb/s with sufficient gain.

In this work, we report the exciting avalanche properties of simple homojunction InAs APDs [6,7]. Room temperature avalanche gain measurements on improved APDs showed that large M values can be obtained at low operating bias below 10V under pure election injection conditions. New excess noise results for InAs electron avalanche photodiodes (e-APD) at 77K are presented, showing excellent noise characteristics similar to those reported at room temperature. To further advance the development of InAs APDs, we also report on the development of a 3 valley Analytical Band Monte Carlo model.

II. Experimental Results

A series of pin and nip wafers listed in Table 1 was grown using Molecular Beam Epitaxy. The growth conditions, focusing on minimisation of unintentional background doping in the i-region, are

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described in Ref [8]. Circular mesa diodes of 25, 50, 100 and 200μm radii were then fabricated by a wet etching process specifically developed to suppress surface leakage currents [8]. The doping profile and layer thickness were extracted from secondary ion mass spectroscopy and capacitance-voltage measurements at 77K. Ideality factors between 1.05 and 1.4 were extracted from forward current-voltage measurements indicating good quality wafers. Reverse current-voltage measurements on devices with different diameters confirmed predominantly bulk dominated leakage current were achieved in the best diodes.

	Intrinsic region		p cladding width (μm)	n cladding width (μm)
	width (μm)	doping ($x10^{15}$ cm^{-3})		
P1	0.8 *(0.9)*	~ 1 *(1)*	2.3	1.9
P2	1.9 *(1.9)*	- *(2)*	2.3	1.9
P3	3.5 *(3.5)*	~ 0.2 *(0.2)*	1.0	1.9
N1	1.1 *(1.15)*	- *(0.9)*	1.1	0.6
N2	1.8 *(1.8)*	~2 *(1)*	2.2	2.0
N3	2.1 *(2.2)*	~ 1 *(1)*	1.4	0.6

Table 1. The structures of the diodes characterized as determined by secondary ion mass spectroscopy and capacitance-voltage measurements (bracketed in italics). Doping concentrations in the p and n claddings are $\geq 1x10^{18}cm^{-3}$.

A laser with wavelength of 633nm was focused on the top p (n) cladding layer to achieve pure electron (hole) injection that give rise to electron (hole) initiated multiplication, M_e (M_h), in the pin (nip) diodes. M_e was found to be higher at a given bias when thicker avalanche region, defined largely by the i-region, was used as shown in Figure 1. Useful gain exceeding 10 can be achieved at low bias below 10V in the thickest structure P3. On the other hand negligible M_h was measured in nip diodes. The slight increase in M_h was due to electron contamination in the carrier generation profile. By using a laser with a wavelength of 3.39μm it was possible to photo-generate primary carriers in all three regions of the *n-i-p* diodes. The multiplication (M_{mixed}) of this mixed primary photocurrent is also shown in figure 2. All results reported are from 200μm radii diodes. Higher multiplication could be measured on smaller P3 diodes (not shown).

Excess noise factors measured under pure electron injection are shown in Figure 3. Results from P2 and P3 clearly demonstrated the very low noise in our InAs APDs corresponding to $k = \beta/\alpha = 0$, in McIntrye's model [2]. Measurements on N2 and N3 were performed with a small fraction of light absorbed in the i-region to obtain predominant hole primary photocurrent as well as by focusing light at the edge of the mesa to generate mixed primary photocurrent. These are necessary since no measureable M_h can be obtained and hence the corresponding excess noise factor could not be extracted. Figure 4 confirms that very high excess noise, corresponding up to k = 120, was measured when predominantly hole primary photocurrent was used. When mixed injection was used the excess noise factor reduced dramatically to k = 0 to 0.3 as injection profile approached that of pure electron injection.

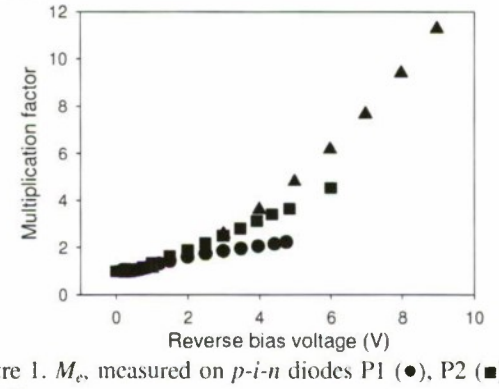

Figure 1. M_e, measured on *p-i-n* diodes P1 (●), P2 (■) and P3 (▲).

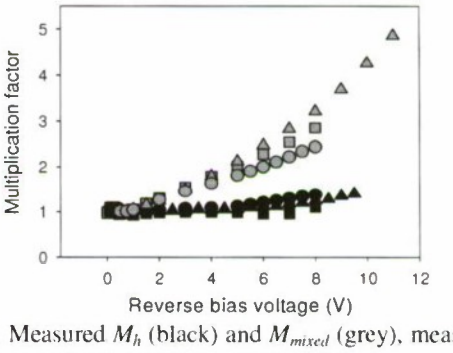

Figure 2. Measured M_h (black) and M_{mixed} (grey), measured on *n-i-p* diodes N1 (●), N2 (■), and N3 (▲).

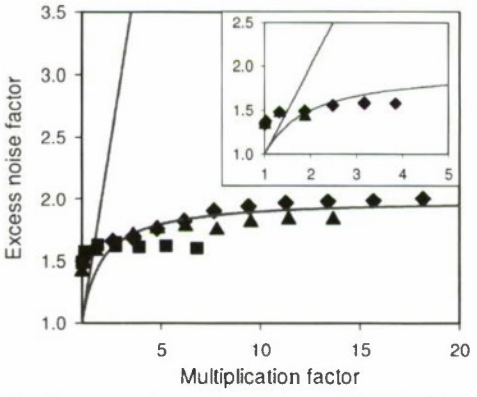

Figure 3. Excess noise measured on P3 and P2 (inset) diodes with radii of 25μm (◆), 50μm (▲), and 100μm (■). Reference lines from the local model [2] for k = 0, and 1.

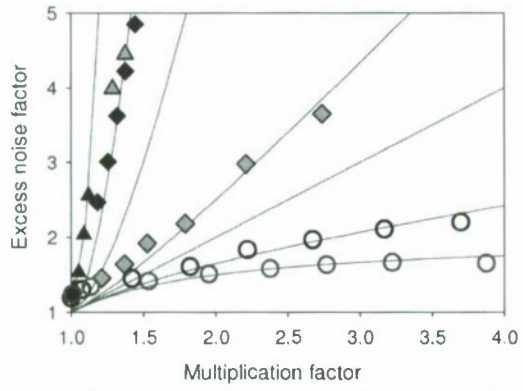

Figure 4. Excess noise characteristics measured with predominately hole primary photocurrent on N2 (grey symbols) and N3 (black symbols) diodes with radii of 25 (◆) and 50μm (▲), together with those measured with intentional mixed primary photocurrents (○) on diodes with 25μm radii. Reference lines from the local model [2] for k = 0, 0.3, 1, 2, 10, 30 and 120.

Our avalanche gain and excess noise measurements on these series of InAs pin and nip diodes, obtained under various carrier generation profiles, clearly demonstrated that hole ionisation is negligible resulting in a fully electron dominated APD (e-APD). The excess noise in our InAs e-APDs is even lower than Si APDs and is comparable to Cadmium-Mercury-Telluride (CMT) e-APDs [9].

Because of the high intrinsic carrier concentration in the relatively narrow bandgap InAs, cooling is necessary to reduce the dark current. Therefore excess noise measurements at 77K using a Janis ST-500 on-wafer probe station and a noise figure meter were performed. Since it is not possible to distinguish between dark current and photocurrent generated noise with this measurement set-up, the photocurrent was required to be at least two orders of magnitude greater than the dark current for accurate measurements to be possible. Before use the set-up was thoroughly benchmarked. Firstly using a commercial silicon pin diode to ensure that shot noise could be measured correctly. Furthermore agreement with existing room temperature noise measurements was confirmed by measuring InAlAs APDs at room temperature. To obtain the excess noise associated with electron initiated avalanche multiplication in InAs e-APDs at low temperatures, P3 was measured. Figure 5 shows dark and photocurrent results obtained on P3.

Pure electron injection initiated excess noise from P3 is shown in Figure 6. The excess noise remains very low, below the local model characteristic for k=0 confirming that β remains negligible at 77K. The new results with $k < 0$ can be attributed in part to the increased significance of the electron's deadspace (d) at this temperature. When d is comparable to the mean ionisation path length, $1/\alpha$, an increased determinism into both the spatial distribution of the impact ionisation events is achieved. An analysis similar to that performed by Saleh et al. [10] suggests that an αd value between 0.1 and 0.5 is broadly consistent with our measured data. It is also interesting to note the similar prediction of excess noise factor with $k < 0$ in CMT by Ma et al. [11].

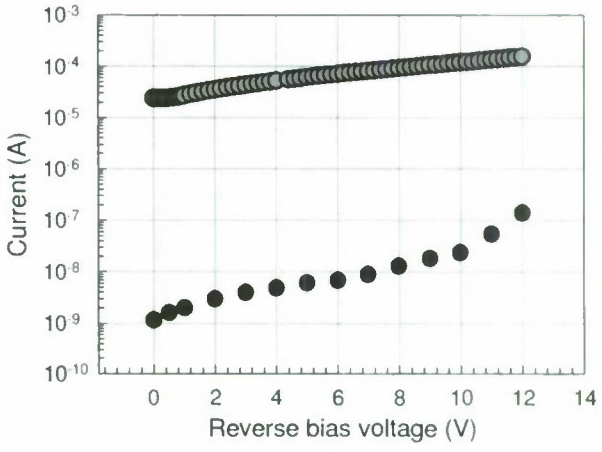

Figure 5. Dark current (•) and photocurrent (•) measurement results for a 200μm radius P3 device at 77K

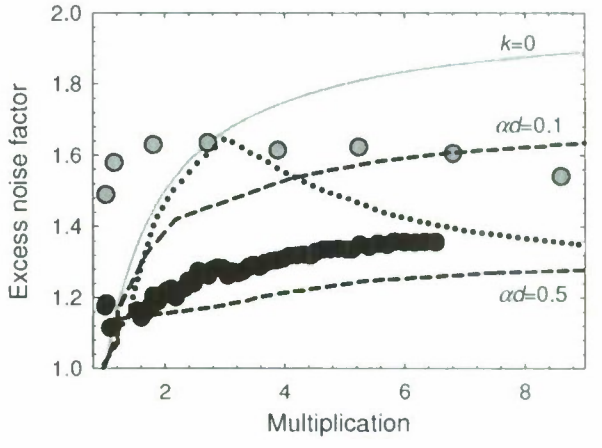

Figure 6. Excess noise factor as a function of multiplication obtained experimentally on P3 at 77K (•), shown against experimental results at 293K [7] (•) and McIntyre's theoretical result when k=0 [2] (grey line). Also shown for comparison are the excess noise characteristics modeled by Saleh *et al.* [10] for fixed values of αd (dashed lines), together with the excess noise modeled for CMT by Ma *et al.* [11] (dotted line).

III. Modelling

The low noise property of InAs e-APDs has been clearly demonstrated in previous sections. To illustrate the potential of InAs e-APDs for optical communication we employed a Random Path Length (RPL) model [1] to simulate the duration of avalanche multiplication, D_a. Figure 7 shows that for all gain values the duration of avalanche lies in the

range $\tau \leq D_a \leq 2\tau$, where τ is the carrier transit time (assuming equal velocities for electron and hole). As expected there is a large number of events with $D_a = \tau$ for primary electrons that produce unity and very low gain. For primary electrons that produce higher gain values, $D_a \leq 2\tau$ was obtained. The corresponding mean current impulse response is therefore no longer than 2τ, leading to much reduced intersymbol inference in high bit rate applications.

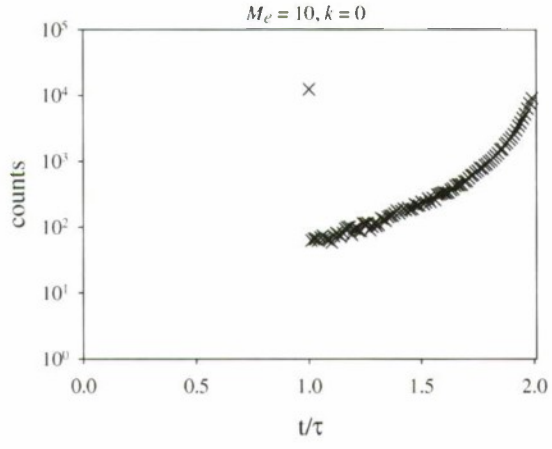

Figure 7: Simulated avalanche duration, D_a as a function of normalized time.

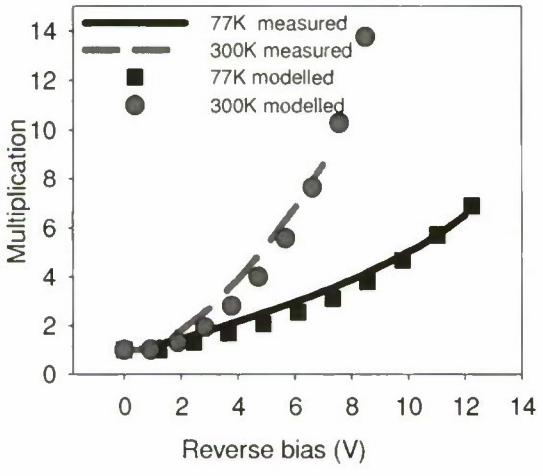

Figure 8. Temperature dependence of electron initiated multiplication in InAs, measured on P3.

To further advance the development of InAs e-APDs, we also report on the development of a 3 valley Analytical Band Monte Carlo model. Using the InAs scattering rates from Fischetti [12], the ionization rate was treated as an adjustable parameter to fit to our measured gain and excess noise both at room temperature and 77K. Using an electron ionization rate $R_i(E) = 3.2\times10^{10}(E - E_{th})^{1.85}$, where E is the electron energy and E_{th} is the ionization threshold energy, taken to be 0.35eV at room 300K and 0.40eV at 77K. Hole ionization was assumed to be negligible. Good agreement between the predicted and measured values was obtained at both temperatures as shown in Figure 8. Unlike most other well characterised semiconductors the avalanche multiplication in InAs exhibits a positive temperature dependence. For instance the electron initiated multiplication reduced from 10 at 300K to 3.6 at 77K when the diode P3 was biased at 7.6V. Our model suggests that at the low electric fields below 100kV/cm the temperature dependence of ionization rate dominates that of phonon scattering rates to produce the observed positive temperature dependence.

IV. Acknowledgments

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Patent no. GB0723858.7

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25-Gbit/s RECEIVER OPTICAL SUBASSEMBLY USING MAXIMIZED-INDUCED-CURRENT PHOTODIODE

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Abstract

We fabricated 25-Gbit/s receiver optical subassemblies (ROSAs) using a maximized-induced-current photodiode (MIC-PD). By employing a high-speed and high-responsivity MIC-PD, we achieved successful operation at 25 Gbit/s using a flexible printed circuit board and a coaxial package designed for a 10-Gbit/s ROSA.

I. Introduction

Recently, it has been reported that traffic demand on the Internet doubles for every two years. To handle the increasing traffic, new standards for 100-Gbit/s Ethernet are being prepared (1). For the 10-km transmission standard (100GBASE-LR4), four-channel 25-Gbit/s light sources and photodetectors are used in a LAN-WDM configuration. These optical devices require not only a high-frequency capability but also cost-effective packaging. To meet these requirements, some approaches have been proposed (2, 3). In the approach in Ref. 2, signal pins of the package are soldered to a flexible printed circuit board (FPC) in a straight line to reduce the electrical reflection.

In this study, we fabricated 25-Gbit/s ROSAs using a high-speed maximized-induced-current photodiode (MIC-PD) (4), 25-Gbit/s transimpedance amplifier (TIA), and 10-Gbit/s ROSA components. The MIC-PD has an intermediate structure between a conventional pin-PD and UTC-PD (5), and can provide both large bandwidth and high responsivity simultaneously. By employing a high-speed MIC-PD, a CAN-type stem and polyimide FPC can be used as they are for 25-Gbit/s ROSAs.

II. Device structure

We fabricated 25-Gbit/s ROSAs using cost-effective 10-Gbit/s ROSA technology. Figure 1 shows a schematic illustration of a fabricated module. The stem is a conventional CAN-type flat one used for a 10-Gbit/s ROSA. Its diameter is 5.2 mm and it is equipped with glass feedthrough for the electrical interface. An FPC was also designed for a 10-Gbit/s ROSA and made with polyimide film. Figure 2 shows a photograph of a fabricated ROSA. It uses an LC receptacle for optical input and complies with the XMD-MSA Type-1 structure in outer dimensions.

To compensate for the loss of 10-Gbit/s ROSA components at high frequency, we propose the use of an MIC-PD. Figure 3 shows the band diagram of the MIC-PD. It has a neutral p-type InGaAs absorption layer and a depleted non-doped InGaAs absorption layer (4). Like in the UTC-PD (5), the traveling delay time of photocarriers generated in the p-type absorption layer is dominated by the diffusion of electrons in the p-type layer, and it is not affected by the drift across the depletion layer very much. On the other hand, the traveling delay time of carriers generated in the depleted absorption layer is dominated by the drift of holes in this layer as in the case of a pin-PD. With these respective transport mechanisms, the transport of photocarriers generated in one absorption layer is not affected by the other layer very much. Therefore, by using the two absorption layers simultaneously, we can increase the total absorption layer thickness while maintaining a large bandwidth. In other words, the combined use of these two layers can yield much larger bandwidth than that possible with a single depleted absorption layer (pin-PD)

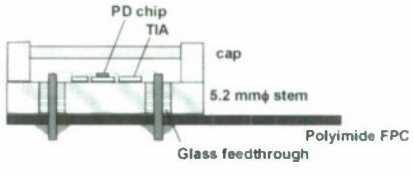

Fig. 1. Schematic illustration of the 25-Gbit/s ROSA.

Fig. 2. Photograph of a fabricated ROSA.

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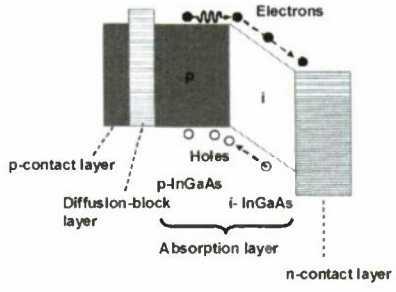

Fig. 3. Band diagram of an MIC-PD.

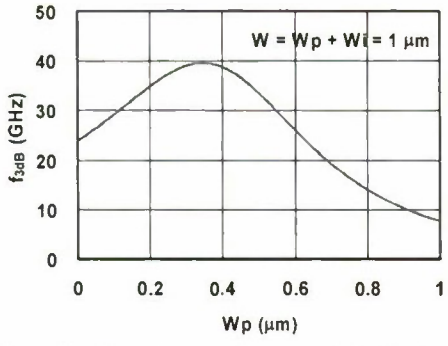

Fig. 4. Dependence of the calculated 3-dB-down bandwidth of the MIC-PD on p-type absorption layer thickness (Wp).

or p-type absorption layer (UTC-PD) with the same thickness. For example, we calculated the 3-dB-down bandwidth determined by carrier transport for an MIC-PD with a 1-μm-thick absorption layer. Figure 4 shows dependence of the 3-dB-down bandwidth on the thickness of the p-type absorption layer (Wp). When Wp is 0.35 μm, the intrinsic bandwidth has the maximum value of 40 GHz, whereas the bandwidth of the conventional pin-PD (Wp=0) is 24 GHz.

In this study, we used MIC-PDs with diameters of 12, 15, or 19 μm to fabricate ROSAs. In on-wafer measurement, a high responsivity of about 1.0 A/W was obtained for both 1.55- and 1.3-μm input light. The MIC-PD chip was mounted on a ceramic substrate by flip-chip bonding (Fig. 1). We used a commercially available TIA designed for use in 100-Gbit/s Ethernet.

III. Frequency response

Figure 5 shows small-signal frequency responses of three MIC-PDs obtained by on-wafer measurements with a lightwave component analyzer. Diameters of the PDs are 12, 15, and 19 μm. In these measurements, the light output of the analyzer (1.55 μm) was incident onto the PDs from the backside of the substrate through an antireflection coating. The measured 3-dB-down bandwidths for the 12-, 15-, and 19-μmϕ PD are 33.0, 31.7 and 25.5 GHz, respectively. Owing to the MIC-PD structure, we achieved a large

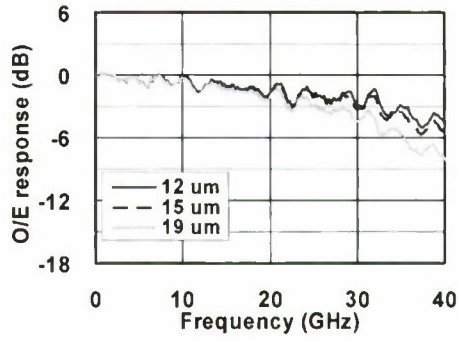

Fig. 5. Frequency response of the MIC-PD obtained by on-wafer measurements.

bandwidth exceeding 25 GHz, while keeping the responsivity above 0.9 A/W.

To investigate the influence of flip-chip bonding, small-signal frequency responses were measured for PD chips mounted on ceramic substrates. Diameters of the measured PDs are 12 and 15 μm. For both samples, O/E responses are almost flat up to 30 GHz, and the measured 3-dB-down bandwidths for a 12- and 15-μmϕ PD chip are 35.8 and 33.5 GHz, respectively. These results show that flip-chip bonding to a ceramic substrate does not degrade the high-speed capability of an MIC-PD chip.

We also measured the frequency characteristics of the stem connected to the FPC. The RF pins of the stem were connected to each other by using a 50-Ω microstrip line on the inner side of the stem and the transmission characteristics were measured between the RF pads of the FPC by using an evaluation board. From the measurement results, the transmission loss for the stem together with the FPC is estimated to be 1.5 dB at 20 GHz. Although this transmission loss for the stem and the FPC can not be ignored, we think the large bandwidth of an MIC-PD will make ROSA operation at 25 Gbit/s possible.

Figure 6 shows the O/E response of fabricated ROSAs with averaged photocurrent of 20 μA. The 3-dB-down

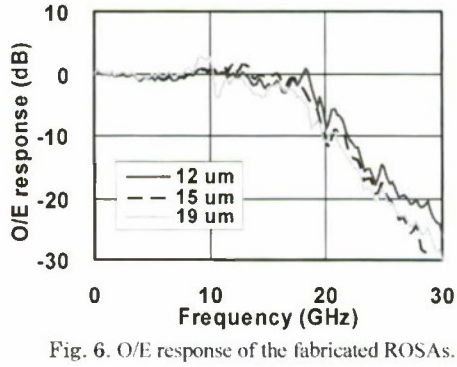

Fig. 6. O/E response of the fabricated ROSAs.

handwidth for ROSAs using 12-, 15-, and 19-μmϕ PDs is 19.0, 18.2, and 17.5 GHz, respectively. For all the three samples, bandwidths around 70% of data rate were achieved in the whole ROSA form.

IV. BER characteristics

We performed baek-to-baek bit-error-rate (BER) measurements for the fabrieated ROSAs at 1.55 μm. Figure 7 shows the experimental setup for BER measurements. In this experiment, the input optieal NRZ signal was generated using a $LiNbO_3$ Maeh-Zehnder modulator (MZM) and the extinetion ratio (ER) was 17dB. The data rate of the pseudo-random bit sequenee was 25.78 Gbit/s and the pattern length was 2^{31}-1.

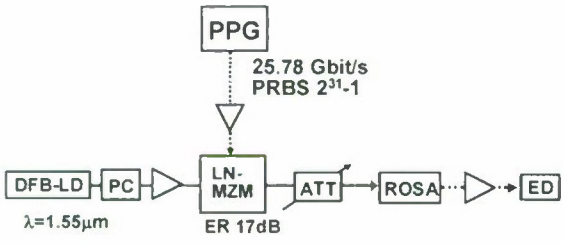

Fig. 7. Experimental setup for BER measurement of the fabricated ROSAs.

Figure 8 shows the eye patterns of the 25-Gbit/s PRBS data received by ROSAs with (a) 12-, (b) 15-, and (e) 19-μmϕ PD ehips. In this experiment, the optieal input power was fixed to -10 dBm and the output of the ROSA was direetly observed with a digitizing sampling oseilloseope. Although the signal-to-noise ratio slightly decreases as PD diameter increases, elear eye openings are ohserved for all three samples.

Figure 9 shows the BER characteristies for the ROSAs using 12-, 15-, and 19-μmϕ PD ehips. For these devices, receiver sensitivities at the BER of 10^{-12} are -14.7, -13.7, and -13 dBm in averaged power (P_{ave}), respectively. In the 100-Ghit/s Ethernet system, the required reeeiver sensitivity is -11.1 dBm in optical modulation amplitude (OMA) (1). By a simple calculation, our results eorrespond to -12.8-, -11.8-, and -11.1-dBm OMA sensitivity against a 1.3-μm-band transmitter with an 8-dB ER. Our deviee should therefore he able to satisfy the system requirements using the 10-Ghit/s ROSA components with an MIC-PD whose diameter is smaller than 19 μm. This result shows that our approaeh also has enough toleranee for optical assembly.

V. Conclusions

We fabricated 25-Ghit/s ROSAs using a high-speed and high-responsivity MIC-PD and 10-Gbit/s ROSA components (an FPC and a stem). The 3-dB-down bandwidths for ROSAs using 12-, 15-, and 19-μmϕ PDs are 19.0, 18.2, and 17.5 GHz, respeetively. From BER measurement of these deviees with a 1.55-μm transmitter at 25.78 Ghit/s, it is estimated that our ROSA should be able to satisfy system requirements. These results show that eost-effective 10-Ghit/s ROSA components can he used to build a 25-Ghit/s ROSA, owing to the use of the MIC-PD.

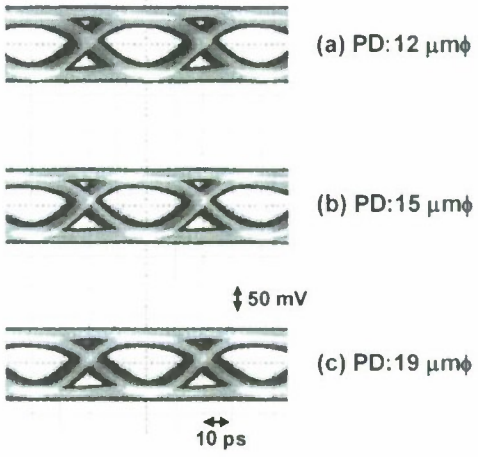

Fig. 8. Eye patterns of the 25-Gbit/s PRBS data received by fabricated ROSAs.

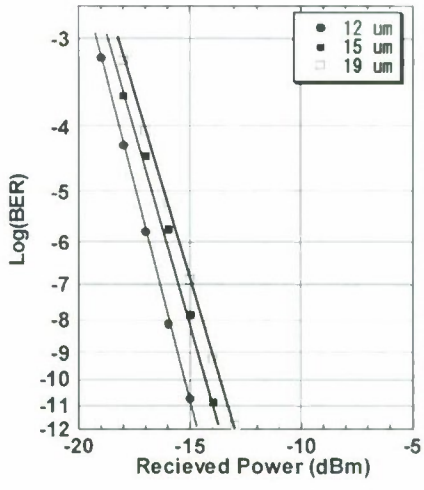

Fig. 9. Back-to-back BER characteristics for the fabricated ROSAs.

Acknowledgement

The authors thank T. Ishibashi for valuable discussions and suggestions, T. Ohyama for help in module fabrication, and T. Akeyoshi, H. Takeuchi, T. Enoki and K. Kato for their continuous encouragement.

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COMPOSITE-FIELD MIC-PDS FOR LOW-BIAS-VOLTAGE OPERATION

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Abstract

A novel maximized-induced-current-photodiode (MIC-PD) structure with a composite field depletion layer achieves high responsivity of 0.8 A/W and a wide 3-dB bandwidth of 30 GHz at a low reverse bias voltage of 2 V for optical input power of +7 dBm.

I. Introduction

Aiming toward the widespread use of high-speed and high-capacity optical communications systems, 40-Gbit/s per wavelength channel transmission technologies have already been installed in long-distance backbone networks (1). Future transmission systems with 100-Gbit/s per wavelength channels and beyond have also been investigated aggressively by using coherent detection with digital signal processing (2). In coherent receivers, high-power input light from a local oscillator can cause a space charge effect in photodiodes (PDs), which leads to reduced bandwidth, especially when the reverse bias voltages applied to the PDs is low. On the other hand, optical transceivers that can handle advanced optical modulation formats, such as DP-QPSK and QAM, will include many electrical components (a serializer/deserializer and driver amplifiers as well as A/D and DSP chips), which may lead to excessive power consumption for cooling the transceiver to its operating temperature. Thus, the components of optical transceivers (including PDs) should be operated at low power supply voltage applied from the transceiver board.

To address this issue, we propose a new composite-field PD that is suitable for low-bias and high-optical-input-power operation. Modifying the structure of a maximized induced current photodiode (MIC-PD) (3), we fabricated a PD that achieves high responsivity of 0.8 A/W and a wide 3-dB bandwidth of over 30 GHz at a PD reverse bias voltage of 2 V for optical input power of +7 dBm.

II. Design concept and fabrication of MIC-PDs

Figure 1(a) illustrates the structure of our conventional MIC-PD (4), which includes a neutral p-type absorption layer and a depleted absorption layer. The thickness ratio between the two absorption layers was determined to minimize carrier traveling delay time for a given total absorption layer thickness, which is an essential feature of our MIC-PD (3). Assuming a uniform field is applied to the depleted absorption layer, the carrier traveling time in the depletion region is mostly determined by the slow hole velocity at the depleted absorption layer. If high power light is illuminated to the PD at low bias voltages, a space charge effect is induced at the depleted absorption layer, where high-density optical carriers have a negative effect on the intensity of the electric field applied from external PD bias voltage. As a result, hole velocity at the depleted absorption layer becomes lower and the frequency response characteristics of the PD degrade unless a much higher external PD bias voltage is applied.

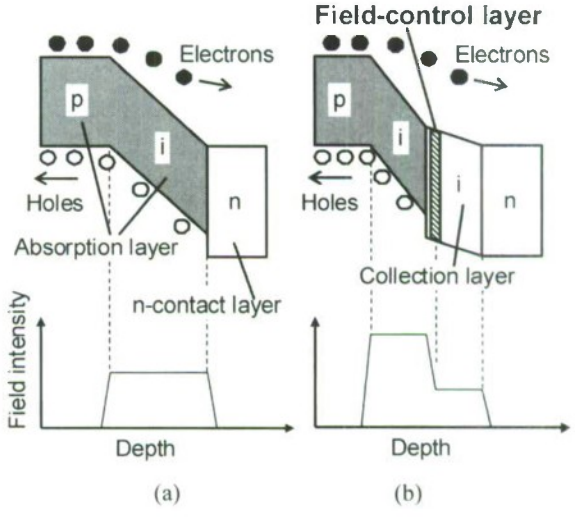

Fig. 1. Structures of the (a) conventional MIC-PD and (b) new composite-field MIC-PD.

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The new composite-field MIC-PD structure is shown in Fig. 1(b). It contains a depleted wide band-gap collection layer and a field control layer, which makes the composite field high and low in the depleted regions in the absorption and collection layers, respectively. Similar to the uni-traveling carrier photodiode (UTC-PD) (5), the effective carriers in the collection layer are only electrons. The carrier traveling time is therefore short relative to that of the depleted absorption layer. Moreover, the depleted collection layer has an effect of decreasing the junction capacitance of the PD, which leads to a smaller CR time constant. Comparing the field intensity of MIC-PDs in Figs. 1(a) and (b) at a same applied bias voltage to the PDs with the same depletion thickness, we see that the one in (b) has higher field intensity at the depleted absorption layer. Because the hole velocity of the modified MIC-PD will be higher than that of the previous one, the space charge effect can be reduced and frequency response characteristics of the PD will be maintained when high power light is illuminated to the PD.

To investigate the potential of our composite-field MIC-PD, we fabricated a conventional MIC-PD [Fig. 1(a)] and a composite-field MIC-PD [Fig. 1(b)]. Total InGaAs absorption layer thicknesses of the conventional and composite-field MIC-PDs were 1.2 and 0.8 μm, respectively. The ratio between the two absorption layers was optimized to provide the highest bandwidth for a given total thickness. Depletion thicknesses were 0.7 and 0.85 μm, respectively. The composite-field MIC-PD included an n-type InGaAsP field-control layer and undoped carrier collection layer. Mesa devices were fabricated with a conventional process comprising wet chemical etching and metal lift-off. From the viewpoint of implementation feasibility, we made the junction areas of the PDs 300 μm^2 (19-μm diameter), which is 3.3 times larger than the 90 μm^2 in our previous report (3). The devices were illuminated from the back side of the InP substrate with antireflection coating. We obtained good responsivity of about 1.0 and 0.8 A/W at a wavelength of 1.55 μm for the conventional and composite-field MIC-PDs, respectively.

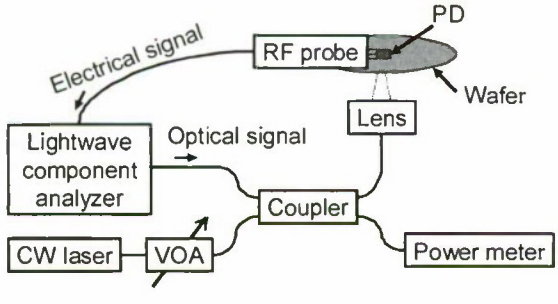

Fig. 2. On-wafer O/E measurement setup.

III. Experimental setup and results

Figure 2 shows the on-wafer O/E measurement setup. Modulated signal light and CW light (λ = 1.55 μm) were combined using an optical coupler and focused to the back-illuminated PD with a collecting lens. Note that CW light was used to assist DC photocurrent in PD; it was not intended to make for coherent detection. The $1/e^2$ beam diameter of incident beam to Φ19-μm-PD was measured with a knife-edge technique and set to be 7 ±1 μm. Assuming a Gaussian beam profile with mode-field diameter of 7 μm, the peak power density corresponds to 5.2 kW/cm^2 for an optical input power of 0 dBm.

Figure 3 shows the frequency response of the fabricated composite-field MIC-PD obtained in on-wafer measurements. Applied reverse bias voltage to PD was as low as 2.0 V. The 3-dB bandwidth (f_{3dB}) reached 30 GHz for optical the input power range from -4 to +7 dBm. As shown in Fig. 3, degradation in frequency responses due to the space charge effect under high incident light was not observed up to +7 dBm.

Figure 4 shows the PD bias voltage dependence of f_{3dB} for the fabricated composite-field MIC-PD. Optical input powers were set to -4 and +4 dBm for low and high optical input power conditions, respectively. For low and high optical input power, the required reverse bias voltages to obtain saturated f_{3dB} over 30 GHz were 0.5 and 2.0 V,

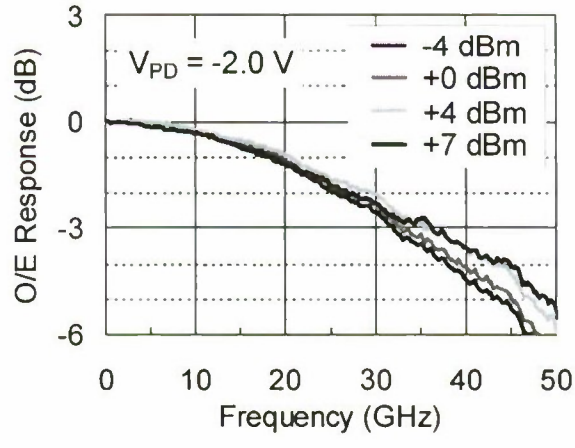

Fig. 3. Frequency response of the fabricated composite-field MIC-PD.

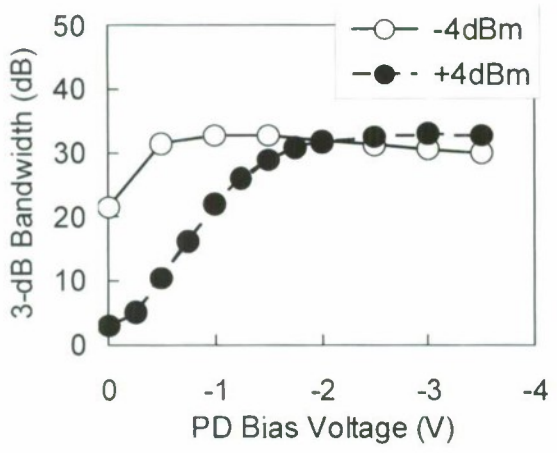

Fig. 4. Bias voltage dependence of 3-dB bandwidth of fabricated composite field MIC-PD.

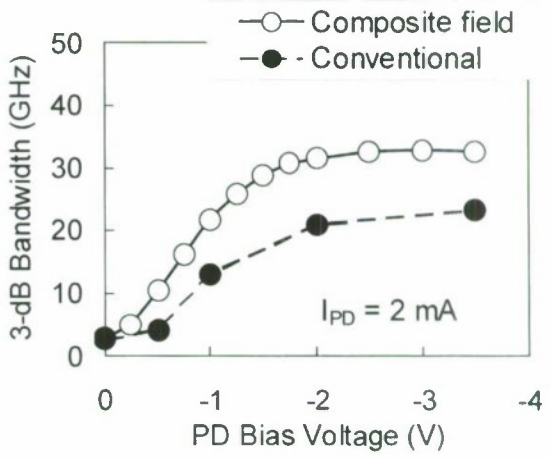

Fig. 5. 3-dB bandwidth of fabricated MIC-PDs with the same photocurrents of 2 mA.

respectively. Higher reverse bias voltage has to be applied for the high optical input power condition mainly because the field intensity at the depleted absorption layer decreases due to space charges, which cause an internal electrical field opposite to that of applied bias voltage.

To clarify the effect of the field-control layer of the composite-field MIC-PD, we compared the MIC-PDs shown in Figs. 1(a) and (b). Figure 5 shows f_{3dB} characteristics versus applied PD bias voltage. Optical input power to the PDs was set so that the photocurrents would be the same, 2 mA. The composite-field MIC-PD shows good f_{3dB} characteristics of over 30 GHz at a low reverse bias voltage of 2 V. On the other hand, the conventional one requires reverse bias voltages of 3.5 V or higher to obtain f_{3dB} of 24 GHz. From the results, with the field-control layer introduced into the depletion region, the high electric field applied to the depleted absorption layer effectively suppresses the frequency response degradation induced by the space charge effect.

To investigate the high optical power capability, we measured the optical input power dependence of f_{3dB} for the composite-field MIC-PD at an applied reverse bias voltage of 2.0 V. The results are shown in Fig. 6. Here, optical input power was varied from -4 to +9 dBm. The corresponding average photocurrent and optical peak power density ranges for optical input power range in this measurement are 0.3 to 6 mA and 2 to 41 kW/cm^2, respectively. For optical input power between -4 and +7 dBm, f_{3dB} almost stays constant at over 30 GHz. For +8 dBm and above, the frequency response degrades, and for + 9dBm, we obtained f_{3dB} of 27 GHz. From this result, it is clear that the composite-field MIC-PD can operated at a high optical input power of + 7

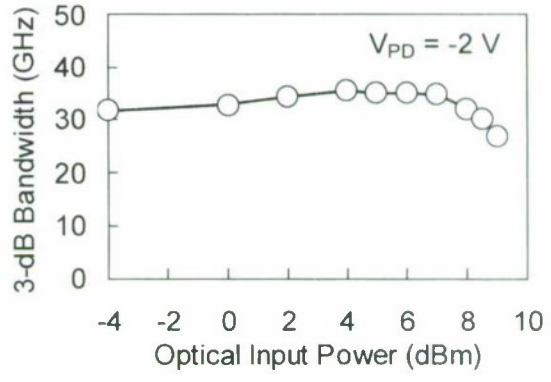

Fig. 6. 3-dB bandwidth of fabricated MIC-PDs versus optical input power.

dBm with an almost constant f_{3dB} of over 30 GHz, where the peak power density is 26 kW/cm^2 and the average photocurrent is 4 mA.

With a DP-QPSK coherent receiver assuming a 16-dBm local oscillator, 0-dBm input signal, and 10-dB loss of a dual polarization 90-degree optical hybrid (9-dB ideal loss and 1 dB excess loss), the average optical input power to PD will become +6.1 dBm. With its capability for average optical input power of +7 dBm, our fabricated composite-field MIC-PD will be applicable to such a high input power optical receivers.

V. Conclusions

We have proposed a novel photodiode structure appropriate for low-bias and high-optical-input-power operation. We achieved a high responsivity of 0.8 A/W and wide 3-dB bandwidth of 30 GHz at a low bias voltage of 2 V for optical input power of +7 dBm.

Acknowledgement

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LOW EXCESS NOISE APD WITH DETECTION CAPABILITIES ABOVE 2 MICRONS

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Abstract

In this work, we present the study on Separate Absorption, Charge and Multiplication (SACM) APDs utilising $In_{0.52}Al_{0.48}As$ as the multiplieation layer and $In_{0.53}Ga_{0.47}As/GaAs_{0.51}Sb_{0.49}$ periodie heterostructures as the absorption layer. $In_{0.52}Al_{0.48}As$ lattice matched to InP has been shown to have superior excess noise characteristies and multiplieation with relatively low temperature dependenee compared to InP. Furthermore, the type-II staggered band line-up of $In_{0.53}Ga_{0.47}As/GaAs_{0.51}Sb_{0.49}$ heterostruetures leads to a narrower effective bandgap of approximately 0.49 eV corresponding to the APD eut off wavelength of 2.4 μm. The SACM APD exhibited low dark eurrent densities near breakdown. The device also exhibited multiplieation in excess of 100 at 200 K. The excess noise of the APD was low as expected, and is comparable to that of a 1 μm $In_{0.52}Al_{0.48}As$ PIN diode.

I. Introduction

The ability for APDs operating in midwave infrared range (2-5 μm) wavelength region would be useful in many applications such as remote sensing, thermal imaging, and chemical sensing in industrial and military operations and also in medieal diagnosties. The APDs offer high sensitivity, achieved via the internal gain provided by the multiplication However the randomness in this proeess results in excess noise which degrades the signal-to-noise ratio. It is well-known that material systems with a large difference in the ionisation coefficients provide lower excess noise and higher bandwidth performanee in APDs. $In_{0.52}Al_{0.48}As$ lattice matched to InP has a larger difference in ionisation coefficients compared to InP, hence show superior APD performance compared to InP.

$In_{1-x}Ga_xAs$ (x = 0.47) and $GaAs_{1-y}Sb_y$ (y = 0.49), form a heterojunetion which exhibit unique optical properties due to its staggered type-II band configuration. In type-II periodie structures, the electron and hole potential wells are separated leading to confinement of electrons in one material and holes in another. If the layers in the periodic structures are sufficiently thin, spatially indirect photon absorption between the valence band states of $GaAs_{0.51}Sb_{0.49}$ and the conduction band states of $In_{0.53}Ga_{0.47}As$ lead to an effective band gap that is narrower than the band gap of either the constituent materials, allowing photon absorption at wavelengths beyond 2 μm, whilst erucially maintaining lattice matching to InP substrates. The type-II band line-up shows an effective band gap of 0.49 eV corresponding to photon absorption up to 2.4 μm at room temperature.

Several groups have reported on $In_{0.53}Ga_{0.47}As/GaAs_{0.51}Sb_{0.49}$ heterostructures with photoluminescence [1], [2], [3] and electro-luminescence [4] in the 2 μm wavelength region. Sidhu *et al.* [5], [6] reported a MBE-grown type-II PIN diode with 50% cut-off wavelength of 2.39 μm and a InP-based SACM APDs utilizing the type-II heterostruetures as the absorption layer with capability of detection at 2.4 μm with gains greater than 30 at room temperature.

In this work, we report the design, fabrication and characterisation of SACM APDs utilising $In_{0.52}Al_{0.48}As$ as the multiplication layer and the $In_{0.53}Ga_{0.47}As/GaAs_{0.51}Sb_{0.49}$ heterostructures as the absorbing region to detect light at wavelengths greater than 2 μm. Reverse dark current and

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avalanche multiplication characteristics as functions of temperature of these APDs are presented. A noise measurement system with a center frequency of 10MHz and a noise effective bandwidth of 4.2MHz was used to measure the avalanche multiplication associated excess noise.

II. $In_{0.53}Ga_{0.47}As/GaAs_{0.51}Sb_{0.49}$ $In_{0.52}Al_{0.48}As$/Type-II SACM APD structure

Table 1 shows the design of an electron injection SACM APD structure based on a 1 μm thick undoped $In_{0.52}Al_{0.48}As$ multiplication region and a 1.5 μm thick absorber consisting of 150 pairs of unintentionally doped $In_{0.53}Ga_{0.47}As/GaAs_{0.51}Sb_{0.49}$ superlattices with each layer 5 nm thick. The charge sheet is 0.11 μm thick with a nominal doping density of 3×10^{17} cm^{-3} to suppress the electric field across the absorption region to be below 200 $kVcm^{-1}$, to preventing ionisation events occurring in the region. The wafer was grown by MBE in The University of Sheffield.

Table 1: Device structure details of SACM APD.

Purpose	Thickness (μm)	Material
Contact	0.002	p^+-$In_{0.53}Ga_{0.47}As$
Cladding	0.500	p^+-$In_{0.53}Ga_{0.47}As$
Absorber	0.045	i-$In_{0.53}Ga_{0.47}As$
	1.500	i-5nm $In_{0.53}Ga_{0.47}As$ /5nm $GaAs_{0.51}Sb_{0.49}$
	0.005	i-$In_{0.53}Ga_{0.47}As$
Grading	0.005	i-InAlGaAs (1eV)
Charge sheet	0.110	p-$In_{0.52}Al_{0.48}As$
Multiplication	1.000	i-$In_{0.52}Al_{0.48}As$
Cladding	0.500	n^+-$In_{0.53}Ga_{0.47}As$
Substrate	---	n^+-InP

Circular and rectangular mesa devices were fabricated from the wafers using standard photolithography and a diluted HNO_3 etch solution. The devices were then passivated by spin-coating benzo-cyclobutene (BCB), which is then cured at 300 °C for 60 seconds. Finally, Cr-Ti-Au was deposited as p-metal contacts and bondpads. Ti-Au was used for n-metal contact.

III. Results

The dark current measured on 90 μm diameter circular $In_{0.52}Al_{0.48}As$/type-II SACM APD as a function of reverse voltage from room temperature (290 K) down to 100 K, is presented in Figure 1. At room temperature, the dark currents are in pA range before ~43 V, which was confirmed to be the punch-through voltage, when measurements were repeated with illumination on the devices. Beyond punch through, dark currents are ~100 nA, which translates to dark current density of approximately 5.5 $mAcm^{-2}$ at room temperature.

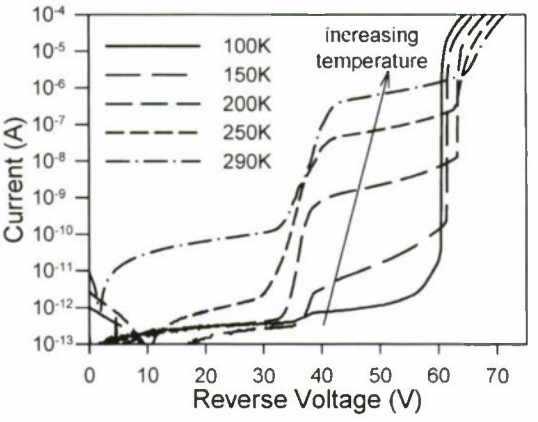

Figure 1: Temperature dependent (100 – 290K) reverse current-voltage characteristic of a 90μm diameter SACM APD device.

As the temperature is decreased down to 100 K, the dark current characteristics at the high voltage regime of interest after punch through drops drastically. The rapid decrease in dark current with decreasing temperature suggests that the dominant dark carrier mechanism is thermal generation of carriers. The temperature dependence of the dark current is demonstrated when the dark current density at a particular voltage of 46 V is plotted as a function of temperature as in Figure 2.

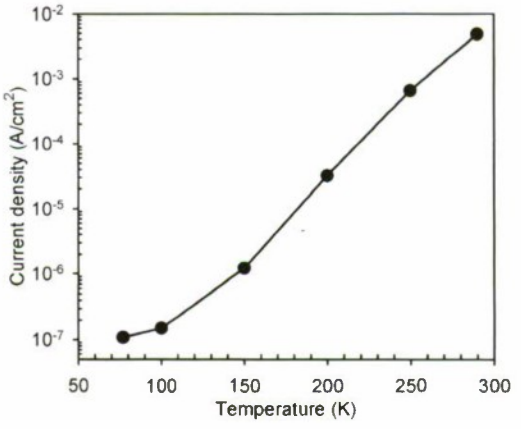

Figure 2: Dark current density at 46V at temperatures ranging from 77K to 295 K.

The breakdown voltage of the device, V_{bd} defined here as the voltage at which the current exceeds 100 μA, is found to decrease with decreasing temperature. The temperature dependence of V_{bd} characterised by the rate of change of breakdown voltage over the temperature range, is approximately 40 mVK^{-1}, which is less than half that of an InP/type-II APD with a 0.8 μm InP multiplication layer [6].

Multiplication measurements were carried out at room temperature and at 200 K. The 2.1 μm wavelength light that was focused on the optical window of the device was obtained from the output of the TRIAX550 Jobin Yvon SPEX monochromator with a tungsten lamp white light source. The measurements were carried using phase-sensitive detection to distinguish the photo-generated current from the dark leakage currents. This technique is especially useful here since the light from the monochromator output is weak and the resultant photocurrent is lower than the dark leakage currents at voltages beyond punch through.

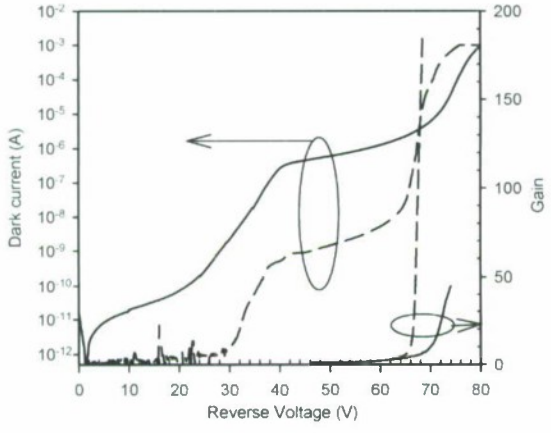

Figure 3: Gain and reverse dark current versus voltage measured for a 90 μm diameter APD at room temperature (solid lines) and at 200 K (dashed lines).

Figure 3 show the 290 K (room temperature) and cooled 200 K dark current characteristics obtained for dark and illuminated conditions respectively. The gain, M, is also plotted on the same graph but on a different axis. As there was uncertainty in determining the gain at punchthrough, since the gain may be finite (M>1) at the punch through voltage, the gain at a fixed bias of 46 V is determined experimentally by comparing photocurrent values of the APD with a type-II PIN at 5 V (fully depleted), when illuminated with identical optical power of 1.52 μm laser light. In this case, the APD is expected to give M ~ 1.2 to 1.3 at 46 V reverse bias. With this assumption and measurement technique, we were able to reliably measure large gain, in excess of 40 at 290K and 100 at 200K, despite the low optical power from the 2.1μm wavelength light. In addition, M data obtained from 1.52 μm and 2.1 μm wavelength light were in agreement, which is expected since both wavelengths of light is fully absorbed in the type-II absorber and produced pure electron injection into the $In_{0.52}Al_{0.48}As$ avalanche region.

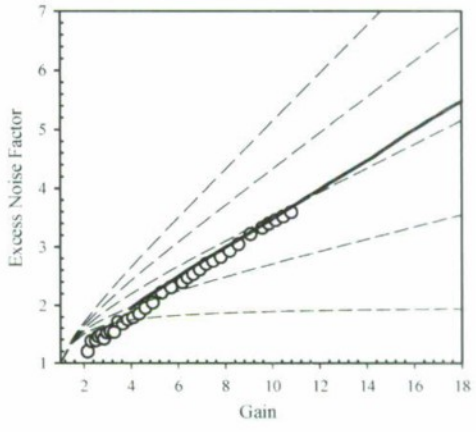

Figure 4: Excess noise factor of a 90μm diameter APD at room temperature (symbols). Excess noise factor of 1μm InAlAs bulk PIN (solid line). Dashed lines are calculations using McIntyre's local model [7] for values of k from 0 to 0.4 in steps of 0.1.

The excess noise was performed using a 1.52 μm wavelength light. For a given value of gain, the excess noise factor was calculated as the ratio of the measured noise power of the device to the noise power of a commercial silicon PIN photodiode operating below the onset of avalanche multiplication at the same photocurrent. At M=10, the excess noise factor was 3.5. The excess noise characteristics were found to be comparable to that of a 1 μm $In_{0.52}Al_{0.48}As$ homojunction PIN diode [8]. As expected, the excess noise is lower compared to that of a InP NIP diode of similar thickness.

IV. Conclusions

The design, fabrication and characterisation of a SACM APD with a $In_{0.52}Al_{0.48}As$ multiplication region and $In_{0.53}Ga_{0.47}As/GaAs_{0.51}Sb_{0.49}$ type-II heterojunction absorber has been carried out. The structure displayed a cut-off wavelength of 2.4 μm. The SACM APD exhibited dark current densities after punch through of 5.5 $mAcm^{-2}$ at room

temperature and ~70 μAcm^{-2} at 200 K. Multiplication measurements from absorption of 2.1 μm wavelength light showed gains in excess of 40 at room temperature and gains in excess of 100 at 200 K. Temperature dependence of breakdown voltage of the APD is weak and improves on prior work using InP avalanche layer. The excess noise of the APD was low as expected, and is comparable to that of a 1 μm $In_{0.52}Al_{0.48}As$ PIN diode.

Acknowledgments

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METAMORPHIC HEMT TECHNOLOGY FOR SUBMILLIMETER-WAVE MMIC APPLICATIONS

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Abstract — **Metamorphic high electron mobility transistor (mHEMT) technologies with 50 and 35 nm gate length were developed for the fabrication of submillimeter-wave monolithic integrated circuits (S-MMICs) operating at 300 GHz and beyond. Heterostructures with very high electron sheet density of 6.1×10^{12} cm^{-2} and 9800 cm^2/Vs electron mobility were grown on 4" GaAs substrates using a graded quaternary InAlGaAs buffer layer. For proper device scaling channel-gate distance and source resistance were reduced. Maximum transconductance of 2500 mS/mm and a transit frequency of 515 GHz were achieved for the 35 nm mHEMT with 2 × 10 µm gate-width. Already the 50 nm technology allows the realization of S-MMIC operation frequencies up to 320 GHz, the current limit of on-wafer probe availability. A compact four-stage H-band amplifier circuit based on a grounded coplanar waveguide (GCPW) layout is presented in 50 and 35 nm technology, respectively. The 50 nm mHEMT amplifier has a linear gain of 19.5 dB at 320 GHz and more than 15 dB between 240 and 320 GHz. The same amplifier utilizing 35 nm gate-length transistors achieves more than 20 dB gain within the entire H-band from 220 to 320 GHz.**

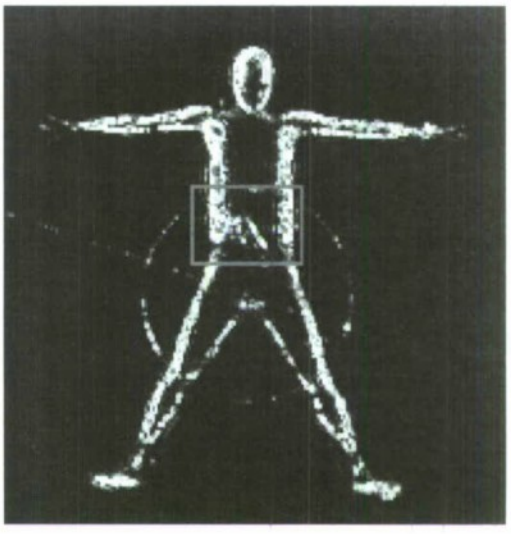

Fig. 1. 220 GHz inverse synthetic aperture radar (ISAR) image of person with gun. The distance between the person on a turn table an the radar system was 170m [1].

I. INTRODUCTION

The submillimeter-wave range of the electromagnetic spectrum which means frequencies above 300 GHz is attracting increasing interest in science and technology. The terahertz frequency regime is the transition between electronics and optics. Until recent years the electronic access to submillimeter-wave frequencies was limited to non-amplifying devices like Schottky-diodes. But now due to the progress in transistor technologies submillimeter-wave MMICs (S-MMICs) can be successfully fabricated. This opens up opportunities for new types of applications like high-resolution active and passive imaging systems (Fig.1), high data rate wireless communication links as well as ultra-wideband transmitter and receiver components, e. g. for use in explosive detection spectroscopy or measurement instrumentation. Due to the fairly high absorption of submillimeter-waves in the atmosphere, medium range applications will be limited to the atmospheric windows at 340, 480, and 670 GHz. The relative high absorption coefficient is caused by the excitation of molecular rotation modes which on the other hand enables molecule spectroscopy for many different applications. Due to the short wavelength very compact antennas can be used in high resolution imaging or detector systems. Another advantage of the submillimeter-wave is the availability of wide non-restricted frequency bands which can be used in active systems for ultra fast data transfer or radar.

Currently, the InGaAs channel high electron mobility transistor (HEMT) is the most advanced semiconductor device technology for S-MMICs [2-4]. Besides the high transistor gain at these frequencies the HEMT has the advantage of the lowest noise figures which is a very important parameter for many system applications. The high frequency performance of the HEMT was continuously improved over the years by reducing the gate length and increasing the In content in the channel layer. The advantages of the higher In concentration up to pure InAs are the higher electron mobility and the better charge confinement due to larger band offsets. InP, GaAs or even Si can be used as substrates for the epitaxial growth of

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the InGaAs/InAlAs heterostructucs. In the casc of different lattice parameters in the substrate and the active device layers (GaAs, Si) the devices are called metamorphic HEMTs (mHEMTs). Advantages of the metamorphic approach are the larger, cheaper, and less brittle substrates. Existing tools and technology modules can be used cspecially in the framework of the backside processing. The handling and packaging of thinned GaAs MMICs is a well established technology. In conclusion, this might simplify the market entry for the metamorphic HEMT approach.

The disadvantages are the costs of the additional epitaxial growth time and the lower thermal conductivity of the metamorphic buffer layer. Beyond these more or less commercial aspects in the comparison of both technologies, the mHEMT offers the higher flexibility for the heterostructure growth because of the additional degree of freedom concerning the lattice parameter. Restrictions of layer thicknesses due to the lattice mismatch of different materials can be removed by the proper adjustment of the lattice parameter by the metamorphic buffer .

Essential for the operation of S-MMICs is the confinement of the electromagnetic field and the suppression of unwanted substrate modes. These requirements are met by the grounded coplanar waveguide topology which consists of coplanar waveguides on the MMIC frondside connected to the grounded backside metallization by through-substrate vias. In addition, this topology provides low source inductance of the active devices, and compact transmission line dimensions [5].

For S-parameter measurements of S-MMICs, frequency extension modules are provided by various suppliers. With increasing frequency the dynamic range of these systems is getting lower [6]. The higher noise floor complicates system calibration and especially the measurement of single devices. For this reason, the extraction of transistor models for accurate S-MMIC design is rather difficult. Appropriate

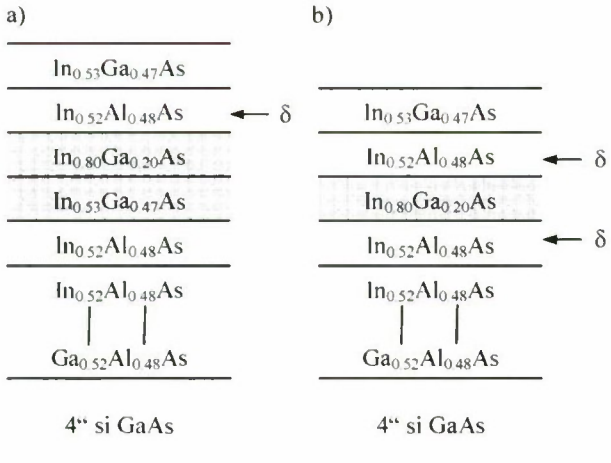

Fig. 2. Layer schematic of the 50 and 35 nm mHEMT heterostructure. The 35 nm mHEMT layer sequence includes a double-side doped single $In_{0.80}Ga_{0.2}As$ channel to avoid short channel effects.

submillimeter-wave probes for frequencies higher than 320 GHz are still under development. The progress towards higher frequencies might raise the need for micromachined probes.

Additionally, the packaging of the MMICs is getting more difficult with increasing frequency. Waveguide and MMIC dimensions are shrinking which generates higher requirements for the module fabrication and assembly. The signal transition from the MMIC into the waveguide shows higher loss. There is either the possibility to use separate microstrip to waveguide transitions or to integrate the transitions into the MMIC [5,7] with the drawback of the higher loss of the semiconductor substrate material.

II. Epitaxy and Heterostructure

Different substrate materials like GaAs, Silicon or Germanium can be used for the growth of mHEMT heterostructures [8,9]. The matching of the lattice parameter is achieved either by a graded or a non-graded buffer layer. The IAF employs for its mHEMT technology an MBE grown linear graded InGaAlAs buffer on 4" semi insulating GaAs substrates. Beginning with an $Al_{0.52}Ga_{0.48}As$ layer the group III element Ga is linearly exchanged against In within the 1 µm thick quaternary buffer layer [10]. The growth conditions were optimized with regard to surface roughness and electrical buffer isolation. Best growth temperature was found to be 460°C thermocouple temperature. Surface roughness of 1.3 nm rms measured by atomic force microscopy in combination with buffer resistivity > 10^8 Ω/sq were achieved.

For the proper scaling of the device parameters with shrinking gate length the design of the heterostructure layer sequence is essential. The RF performance of ultra short gate

TABLE I
Electrical DC- and RF-parameters of the metamorphic HEMT technologies (w_g = 2 × 10 µm)

	l_g = 50 nm	l_g = 35 nm
R_c	0.05 Ω·mm	0.03 Ω·mm
R_s	0.15 Ω·mm	0.1 Ω·mm
$I_{D,\,max}$	1200 mA/mm	1600 mA/mm
V_{th}	-0.25 V	-0.3 V
$BV_{off\text{-}state}$	2.2 V	2.0 V
$BV_{on\text{-}state}$	1.6 V	1.5 V
$g_{m,\,max}$	1800 mS/mm	2500 mS/mm
f_T	380 GHz	515 GHz
f_{max}	>600 GHz	> 900 GHz
MTTF	2.7 × 10^6 h	n.a.

length devices is often limited by parasitic gate capacitances. An increase in the parasitics is caused by the dielectric passivation layer, which is needed to attain sufficient device lifetime. To suppress the RF degradation due to the parasitic gate capacitances the intrinsic C_{gs} must be increased by reducing the distance between the two-dimensional electron gas and the gate which means reduced barrier and InGaAs channel thickness. Large conduction band offsets are needed to suppress gate leakage currents and for sufficient electron confinement. The epitaxial growth must be optimized with respect to high electron density in the channel which is required to obtain high device current density and therefore fast charging times of the speed-limiting device capacitances.

For the choice of materials in the heterostructure also the valence band offset must be considered. Because of the low band gap energy of the InGaAs channel electron-hole pair generation already starts at low gate-drain voltages. Holes accumulating outside the channel are compensated by additional electrons in the channel for reasons of charge neutrality. Therefore, the output conductivity is increased which is especially observed for InAs/AlSb heterostructures where due to the type II band alignment the valence band barrier is missing. High output conductivity in turn is making circuit design difficult.

Over the years the evolution of the InGaAs HEMT was associated with an increase in the In concentration. With employment of pure InAs the InGaAs/InAlAs material system is now coming to its limits, therefore Sb based materials are getting into focus now. Sb containing heterostructures provide large band offsets in combination with high electron mobility.

The layer structure of the IAF 50 and 35 nm mHEMT is shown in Fig. 2. In contrast to the 50 nm technology the 35 nm one uses a single $In_{0.8}Ga_{0.2}As$ channel and a double-side doping. With the optimized MBE grown layer sequences channel mobilities and channel electron densities as high as $\mu_e = 9800$ cm^2/Vs and $n_e = 6.1 \times 10^{12}$ cm^{-2} for the 35 nm and $\mu_e = 11800$ cm^2/Vs and $n_e = 4.2 \times 10^{12}$ cm^{-2} for the 50 nm mHEMT heterostructure were measured.

III. Submillimeter-wave mHEMT

For the fabrication of analog S-MMICs a transistor gain of at least 5 dB should be available at the operation frequency. Otherwise, due to matching losses within the circuit, it is hardly possible to achieve sufficient gain even in a multi-stage design. Under the assumption of a 20 dB gain drop per decade for the maximum available gain (MAG) a maximum oscillation frequency f_{max} of more than 500 GHz is needed for the design of submillimeter-wave amplifier circuits. As shown in Tab. I the IAF 50 and 35 nm mHEMTs provide sufficient high f_T and f_{max} values for submillimeter-wave applications.

The processing within both technologies starts with a wet-chemical mesa etch for device isolation. In order to avoid gate leakage currents the InGaAs channel layer is under-etched to avoid contact between the conducting InGaAs channel

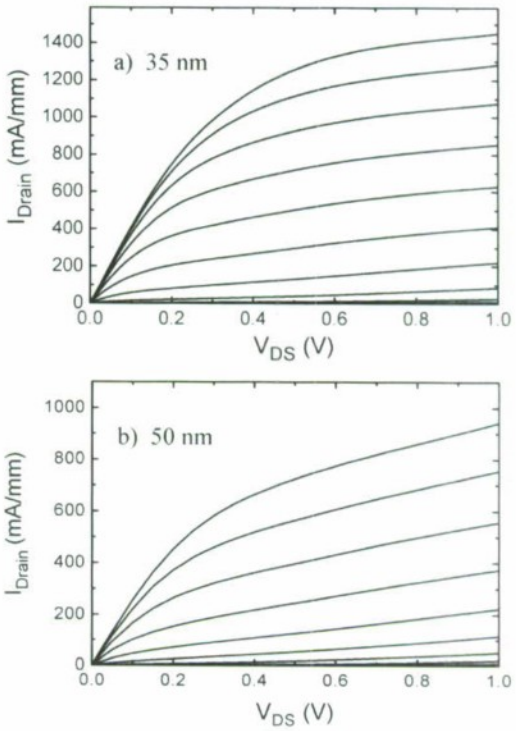

Fig. 3. Ouput characteristics of the 35 nm (a) and 50 nm (b) mHEMT. No kink effects are visible.

material and the gate metallization crossing the mesa edge. Electron beam evaporated GeAu layers are used for the ohmic contacts which are alloyed at 300°C on a nitrogen purged hot plate. Because of the very small source-drain separation of 500 nm, a new only 75 nm thick ohmic contact metallization was developed for the 35 nm mHEMT to improve device yield. The contact resistance R_C had to be reduced to satisfy the scaling requirements.

In both technologies e-beam direct writing was applied for the gate layer. This was done on a JEOL JBX 9300FS e-beam writer. For the 50 nm mHEMT the gate is defined in a four-layer PMMA resist by a single e-beam exposure. Whereas for the 35 nm the critical gate foot dimension is defined by ICP dry etching of a thin SiN layer using e-beam patterned PMMA 950K as etching mask. On top of this SiN opening a 100 nm T-gate is implemented in a three-layer resist lift-off process using the SiN opening as a shadow mask for the gate metallization after the recess etching. The disadvantage of this technology is the necessity of two e-beam writing layers whereas the process control of the critical 35 nm gate length is getting simple. An overlay accuracy of 30 nm is achieved between both exposures.

The gate recess is etched using a succinic acid based solution. Many transistor parameters are correlated with the lateral width of this recess. An undersized width would reduce the breakdown voltage of the device and cause gate leakage current, whereas an oversized lateral recess would increase the

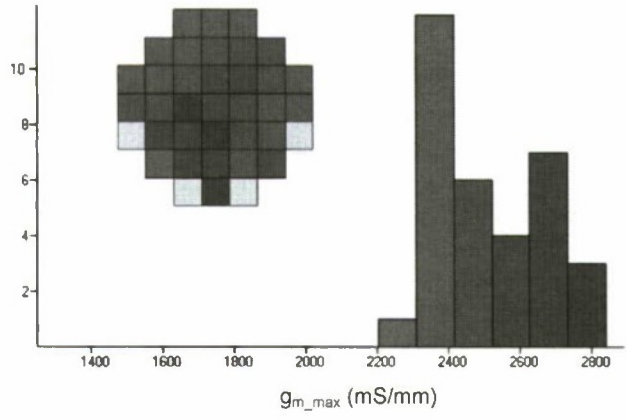

Fig. 4. Topogram of $g_{m,max}$ for a 2 × 30 µm device in 35 nm technology across the 4" wafer. The device yield is 90 % and a standard deviation of 140 mS/mm is achieved.

source resistance. Any etching delay due to surface contamination or wetting must be avoided. A Pt-Ti-Pt-Au layer sequence is used for the gate metallization. By annealing the wafer at 300°C the lower Pt-layer is alloyed into the InAlAs barrier layer. Hereby, the metal-semiconductor interface is shifted away from the surface into the semiconductor heterostructure. The reason for this approach is the improved device reliability [12] and better reproducibility of the electrical device parameters.

The mHEMTs are encapsulated in a low-k benzocyclobuten BCB (ε = 2.65) layer to keep the parasitic gate capacitances low. Vias in the BCB layer for the interconnects are opened by ICP dry etching. The mHEMTs are passivated with a 250 nm thick CVD deposited SiN layer. The output characteristics of the 50 and 35 nm mHEMT are shown in Fig. 3. Both characteristics are almost kink free and exhibit low output conductance due to the downscaled Schottky barrier and channel thickness.

A maximum transconductance $g_{m,max}$ of 1800 mS/mm for the 50 nm mHEMT and 2500 mS/mm for the 35 nm transistor was measured. To improve the source resistance R_S the ohmic contact resistance of the 35 nm mHEMT was lowered to 0.035 Ωmm and the source-gate distance was shrinked from 500 to 250 nm. The smaller device dimension makes higher demands on lithography alignment and lift-off processes for ohm and gate metallization. For the $g_{m\ max}$ of a 2 × 30 µm device in 35 nm technology a topogram across a 4" wafer is presented in Fig. 4. The device yield is 90 % and a standard deviation of 140 mS/mm is achieved. An f_T of 515 GHz for a 2 × 10 µm device was extrapolated [2]. Some electrical parameters are listed in Tab. 1. For the 50 and 35 nm mHEMT we were not able to determine f_{max} with a sufficient confidence level out of transistor measurements. The given f_{max} of 600 and 900 GHz are lower limit estimations based on measured amplifier MMIC gain. Losses in the MMIC due to the matching networks are taken into account and a 20 dB gain drop per decade is assumed.

The lifetime of HEMTs is correlated with the strength of the electric field in the device [12] and therefore also with the gate-length. A median time-to-failure of 2.7 × 10^6 h in air at 125°C channel temperature was extrapolated based on a 10% $g_{m,max}$ failure criterion for the 50 nm mHEMTs (Fig. 5). The reliability of the 35 nm mHEMT is under investigation.

Further device scaling is not limited by shrinking the gate length. As shown in Fig. 6 gates with 20 nm gate length have already been fabricated at IAF. The main challenges are the reduction of the gate-to-channel distance without increasing the gate leakage current and the necessary reduction of the source resistance R_S. Heterostructures with large band offsets

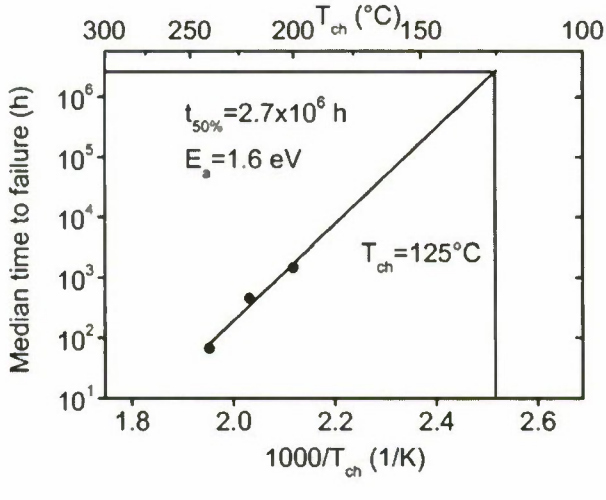

Fig. 5. A median time to failure of 2.7 × 10^6 h in air was extrapolated for the 50 nm mHEMT.

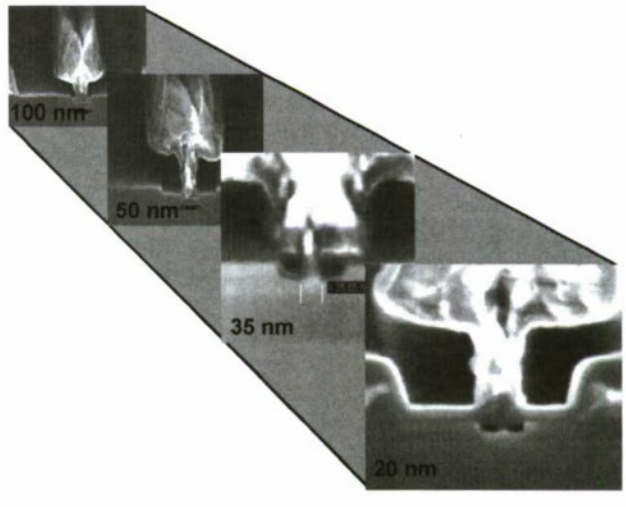

Fig. 6. Gate cross-section of the different IAF mHEMT generations. Physical gate-lengths down to 20 nm are fabricated.

and high electron sheet densities will be needed to fulfill these requirements.

III. Passive Elements and Backside Processing

In addition to the active devices, appropriate passive elements are necessary for the design of submillimeter-wave MMICs. MIM capacitors, thin film resistors, and two interconnection layers including one plated Au layer in airbridge technology are provided for circuit layout. The RF interconnects at these very high frequencies are of special importance. Because of its good isolation and small dimensions, grounded coplanar waveguides (GCPW) are used as transmission lines within the MMICs. With respect to the submillimeter wavelength the ground-to-ground spacing of the GCPW was reduced to 14 µm. The distance between adjacent through-substrate vias was also reduced to suppress unwanted substrate modes. For this reason, the via diameter was shrinked to 20 µm and a capacitor on via process was developed.

For the backside processing the wafers are glued on 4" sapphire substrates. To avoid air bubbles between the GaAs wafer and carrier the gluing is done in a vacuum chamber with the help of heated pressure plates. Subsequently, the GaAs wafers are thinned down to 50 µm thickness. Contact lithography is used for the structuring of the backside. Etching mask for the ICP etch is a 12 µm thick resist layer. After the etching of the through substrate vias the complete wafer is plated with a 3 µm thick Au layer. The dicing streets are uncovered by a second lithography and gold wet etching.

The entire 50 µm thick 4" GaAs wafer is released from the sapphire carrier by organic solvent and transferred on tape for laser dicing (Disco DFL7160) and automated picking (Royce MP300). These processes are critical for the MMIC yield due to the small thickness of the GaAs substrate.

IV. Submillimeter- Wave MMICs

A four-stage H-band amplifier was chosen to demonstrate the submillimeter-wave capability of the 50 and 35 nm mHEMT technologies. The amplifier S-MMIC was designed to achieve high gain and large bandwidth in combination with low noise figure. Therefore, a cascade configuration, consisting of a series connection of one HEMT in common source and one in common gate configuration was utilized. The transistor gate

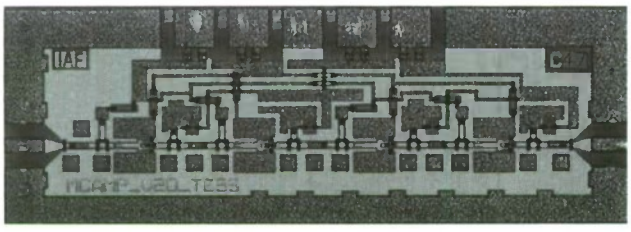

Fig. 7. Chip photograph of the four-stage H-band cascode amplifier S-MMIC. The chip size is 0.5 × 1.2 mm^2.

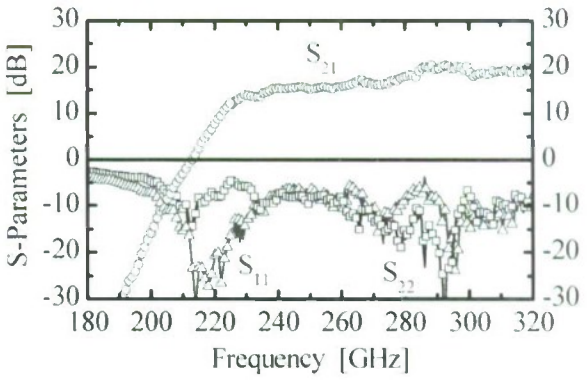

Fig. 8. On-wafer measured S-parameters of four-stage 50 nm H-band cascode S-MMIC amplifier. A linear gain of 19.5 dB at 320 GHz was measured.

width is 2 × 10 µm. Fig. 7 shows a chip photograph of the realized H-band amplifier S-MMIC. Due to the very compact grounded coplanar waveguide technology the over-all die size is only 0.5 × 1.2 mm^2. On-wafer S-parameter measurements were performed using an Agilent 8510C VNA system with an 85105A submillimeter controller, two Oleson WR-3 T/R frequency extension modules and two Picoprobe Model 325 microwave probes. For an LRL-type calibration at the probe tip, a modified CS-15 calibration substrate was chosen. Measurements at higher frequencies are presently not possible, due to the lack of suitable RF-probes.

The measured S-parameters of the 50 nm four-stage cascode amplifier circuit are presented in Fig. 8, in the frequency range from 180 to 320 GHz. A linear gain of 19.5 dB was achieved at 320 GHz, by applying a drain voltage of V_{ds} = 2 V, a second gate voltage of V_{g2} = 1.1 V and a gate voltage of V_g = 0.1 V. The total drain current at this bias point was I_d = 45 mA. Between 240 and 320 GHz, we measured a small-signal gain of more than 15 dB. Both, input return loss S_{11} and output return loss S_{22} were approximately -10 dB at 320 GHz. Due to the lack of a suitable H-band noise diode, the noise-figure of the amplifier MMIC could not be measured so far. The simulated noise-figure at room-temperature (T = 293 K) was 7.3 dB at 320 GHz.

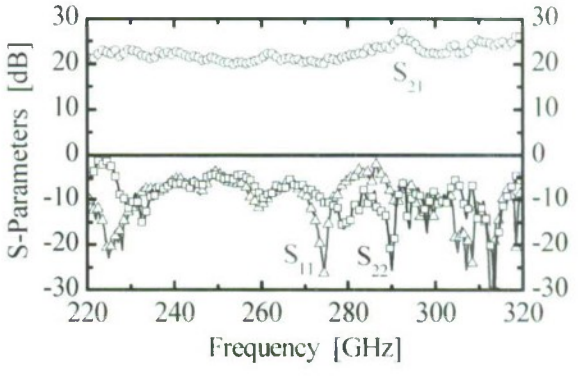

Fig. 9. On-wafer measured S-parameters of four-stage 35 nm H-band cascode S-MMIC amplifier. A linear gain of more than 20 dB over the entire H-band (220 - 320 GHz) is achieved.

In addition to the 50 nm mHEMT amplifier circuits, a 35 nm mHEMT amplifier version was fabricated demonstrating increased gain performance and larger bandwidth. As shown in Fig. 9, the 35 nm H-band amplifier S-MMIC achieved a small-signal gain of more than 20 dB in the entire H-band (220 – 325 GHz) with a maximum gain of 26.4 dB at 319 GHz. The DC-power consumption of the circuit was 49 mW with a total drain current of I_d = 35 mA.

VI. Conclusions

Metamorphic HEMT technologies with 50 nm and 35 nm gate length have been developed for operation in the submillimeter-wave frequency regime at 300 GHz and beyond. This was achieved by proper scaling of all device parameters. Of special importance were the reduced distance between the two-dimensional electron gas and the gate in combination with an extremly low source resistance of only 0.1 Ωmm for the 35 nm mHEMT. To provide sufficient suppression of submillimeter substrate modes a capacitor-on-via process was developed including through substrate vias with a diameter of only 20 µm. Grounded coplanar waveguides turned out to be a proper transmission line type for S-MMICs. Compact four-stage H-band amplifiers in 50 and 35 nm technology demonstrate more than 19 dB of linear gain at the measurement limit of 320 GHz. These results impressively demonstrate that metamorphic HEMT technology is highly suitable for the successful realization of submillimeter-wave applications.

Acknowledgement

The authors would like to thank their colleagues from the Fraunhofer IAF epitaxy, technology and high frequency departments for excellent wafer growth, processing and characterization. This work was funded by the German Federal Ministry of Defence (BMVg) and the Bundeswehr Technical Center for Information Technology and Electronics (WTD81) in the framework of the TERAMOSS program.

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SUB-50NM InGaAs/InAlAs/InP HEMT FOR SUB-MILLIMETER WAVE POWER AMPLIFIER APPLICATIONS

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Abstract— **An InGaAs/InAlAs/InP HEMT with sub-50nm EBL gate has been developed for sub-millimeter wave (SMMW) power amplifier (PA) applications. In this paper, we report the device performance including high drain current, high gain, high breakdown voltage and scalability to large gate periphery, which are essential for achieving high output power at these frequencies. Excellent yield, process uniformity and repeatability are also demonstrated, which is critical for power amplifiers employing large number of devices and gate fingers. 10mW output power is demonstrated from a fixtured 338 GHz PA module.**

Keywords- High electron mobility transisters (HEMT); InGaAs/InAlAs/InP; power amplifier; millimeter; sub-millimeter

I. INTRODUCTION

Significant improvements have been made in recent years on high frequency InP-based HEMTs which enabled low-noise and power amplifiers in the millimeter and sub-millimeter wave (>300GHz) regime. [1]-[3]This technology advancement opens up a new frontier to many unique military and commercial applications at these frequencies including radiometry, sensing, imaging, etc.

Power amplification at these extremely high frequencies is very challenging for the device technology development. Both a high output power density (per unit gate periphery) and a large total gate periphery are desirable. In order to achieve a high output power density, a high frequency gain, high maximum drain current (I_{max}) and sufficient breakdown voltage (BVgd) have to be maintained at the same time, which means the device has to be carefully optimized for this balanced performance. Having a large gate periphery requires a good scalability of the device as well as a sufficient yield and uniformity of all the gate fingers in a PA circuit.

In this paper, we present a well balanced device with our sub-50nm InP HEMT technology, which delivers a state of the art power performance at frequencies as high as 338GHz.

II. SUB-50NM INGAAS/INALAS/INP HEMT TECHNOLOGY

The epi wafers were grown in molecular beam epitaxy (MBE) on 3-inch semi-insulating InP (100) substrates. As shown in Figure 1, the layer structure consists of a n+ InGaAs/InAlAs composite cap for enhanced ohmic contacts, an un-doped InAlAs as Schottky barrier and an InGaAs/InAs composite channel for superior electron mobility. A Si doping plane is inserted in the Schottky layer to supply electrons for current conduction. The thickness and doping concentration of the cap and Schottky layers provide a trading space between the device transconductance (Gm), Imax and BVgd. The epi profile design also impacts on the device aspect ratio and the associated output conductance, especially when the gate size is aggressively scaled down. A careful optimization was done in this work to achieve high frequency power performance. Room temperature electron mobility over 15,000 $cm^2/V{\cdot}s$ has been achieved with a sheet charge of 3.3e12 cm^2.

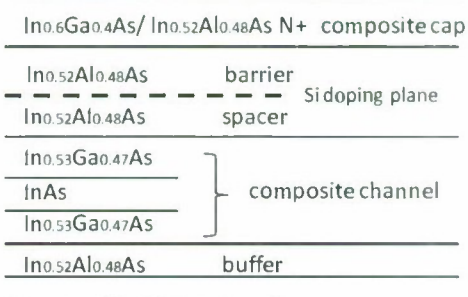

Figure 1. Layer profile of the epi wafers.

The device ohmic contact is formed with a non-alloyed metal scheme, which enables an extremely consistent low contact resistance, R_c. The typical R_c in our devices is 0.04 Ω.mm, with the on-wafer standard deviation as low as 3%. The development of a sub-50nm gate process is another critical step in realizing amplifiers with effective operation at sub-millimeter wavelengths. Scaling the size of the gate allowed for a corresponding reduction in the gate capacitance (C_{gs}), which affects gain for circuits operating at high frequencies. Sub-50nm T-gates were formed using electron beam lithography. The self-aligned gate recess is formed with wet

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chemical etching. The gate recess profile (the width and depth) were optimized for a high Gm and high BVgd at the same time. The devices are fully passivated with SiN deposited with PECVD. After the fronside process, the wafers were thinned to 50μm and processed with fully metalized ground vias.

The device dc and RF characteristics are summarized in Table 1. The device S-parameters were measured on-wafer in an extended reference plane structure from 1 to 100GHz. The current gain cutoff frequency, f_T, was calculated by extrapolating H21 to 0dB with a -20dB/decade slope. A small signal model was extracted from the S-parameters and the maximum available/stable gain (MAG/MSG) was simulated based on the model. The maximum oscillation frequency, f_{max}, was then obtained when MAG/MSG reaches 0dB. The >500GHz f_T and >1000GHz f_{max} ensure a sufficient device gain at SMMW frequencies. The combination of a high peak transconductance (Gmp), good BVgd and a high I_{max} makes this device a good candidate for high frequency power applications. Figure 2 is the on-state breakdown characteristics. The dashed line shows the device on-state breakdown locus which indicates that the drain can be biased at up to 2V at class A operation. A large output swing on the load is expected which is associated with a high output power density.

A large total gate periphery is needed in a power amplifier in order to generate a high total output power. This puts a high requirement on the device yield and uniformity within the circuit. With the device process in this work, good d.c. yield and excellent on-wafer uniformity have been achieved on the 4-finger 60μm devices, which are the typical device used in many of our PA designs. Figure 3 and 4 show the statistics of Gm and gate-drain breakdown of such devices in the recent 4 lots of a total of 10 wafers. The standard deviation of Gm is 230 mS/mm, less than 10% of the average value, which is around 2400 mS/mm. The standard deviation of the beakdown voltage is only 0.24V, which is also less than 10% of the average value. The yield is in excess of 90%. This yield number is similar to that of our production 0.1μm process.

III. POWER AMPLIFIER PERFORMANCE

SMMW power amplifiers (PA) have been fabricated with the sub-50nm HEMT technology. Typical power density of 100mW/mm has been achieved for power SMMIC's above 300GHz. [5] The four-stage MMIC SSPA [6] is a balanced power amplifier realized in coplanar waveguide. The output stage uses two 80 um transistors, while the input stages use 30, 30, and 40 um ones. The circuit chips are fixtured so that the co-planar waveguide in the circuits is directly coupled to the WR3 waveguide with the integrated transition. Output power is measured at the waveguide flange. The measured output power and power gain from a SMMW PA module are plotted in Figure 6. Psat of 10dBm (10mW) at 338 GHz [6] have been demonstrated, making it among the highest power PA's in this frequency range. This result validates the device design and fabrication for power amplification. It also opens up many potential power applications ranging from G-band to SMMW frequencies.

Device Parameters	Typical value
Gmp (mS/mm)	2400
BVgd (V) (two terminal)	2.4
BVgd (V) (on-state)	>2
I_{max} at Vd=1V (mA/mm)	900
f_T (GHz)	>500
f_{max} (GHz)	>1000

Table 1. d.c and RF performance of a sub-50nm InGaAs/InAlAs/InP HEMT with 2 fingers and 40μm total gate periphery.

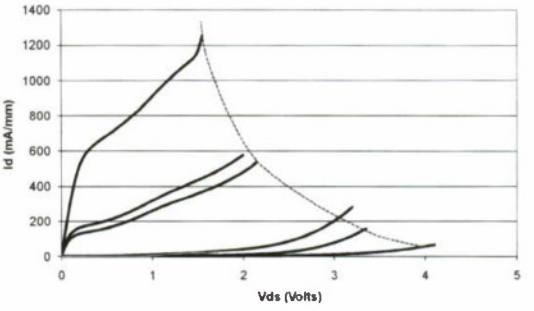

Figure 2. I-V characteristics of a 2-finger 100μm InGaAs/InAlAs/InP HEMT.

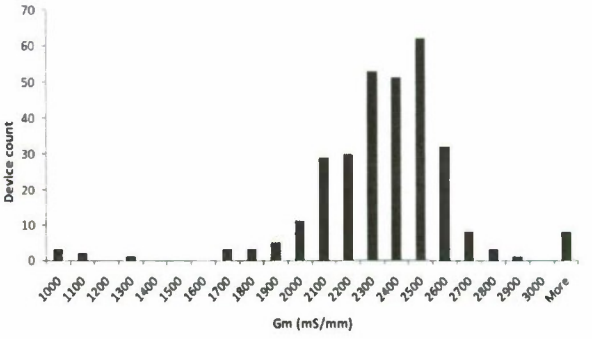

Figure 3. Histogram of Gm from 4 finger 60μm devices in recent 4 lots of a total of 10 wafers showing over 90% d.c. yield.

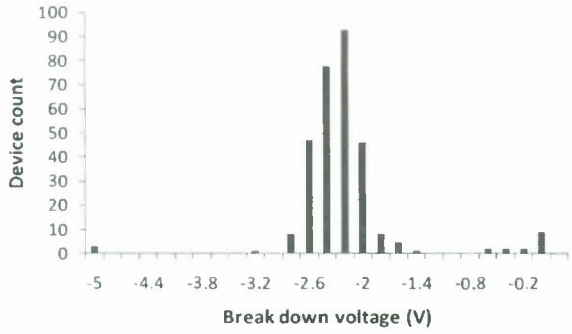

Figure 4. Histogram of gate-drain breakdown voltage from 4 finger 60μm devices in recent 4 lots of a total of 10 wafers showing over 90% d.c. yield.

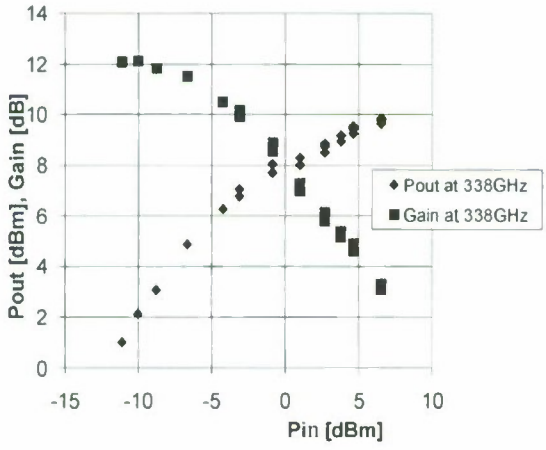

Figure 6. Measured output power and power gain of a PA module at 338GHz.

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IMPROVEMENT IN NOISE FIGURE OF WIDE-GATE-HEAD InP-BASED HEMTS WITH CAVITY STRUCTURE

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Abstract

Dependences of minimum noise figure at 94 GHz on gate-head length were studied using InP-based HEMTs. The noise figure was improved effectively by using a cavity structure even though a wide gate-head was employed. Wide gate-head InP-based HEMTs with a cavity structure are promising candidates for improving low-noise properties at millimeter-wave frequencies.

I. Introduction

InP-based high electron mobility transistors (HEMTs) have shown excellent high-frequency and low-noise characteristics. Their attractive cut-off frequency (f_t) of over 600 GHz (1, 2) and low minimum noise figure (NF_{min}) characteristics of 1.0 dB at 94 GHz (3) have been reported. To improve these high-frequency and low-noise characteristics, it was effective to reduce gate length to less than 50 nm. Furthermore, to improve f_t and NF_{min} it was also effective to increase transconductance (g_m). g_m was enhanced by thinning the carrier supply layer, reducing the horizontal dimensions in the gate recess region, increasing the sheet carrier density in the channel region, and increasing the saturation velocity (4, 5). The high performance of InP-based HEMTs makes them applicable for millimeter-wave systems, such as wireless radio communications (6) and image sensors (7). In these applications, low-noise amplifiers (LNAs) generally play the important role of amplifying the miniscule power of millimeter waves up to a practical signal level. Therefore, the noise figure should be minimized to obtain millimeter-wave signals of a higher resolution. Recently, we reported a very low NF_{min} of 0.71 dB at 94 GHz using InP-based HEMTs which had a cavity structure to eliminate any parasitic capacitance around the gate electrodes (8). Additionally, the cavity structure was effective for enhancing f_t.

In this study, we report on how a cavity structure, which reduces parasitic gate-capacitance originating from dielectric films for interconnection, was effective for improving NF_{min} even though the gate head was expanded. Reducing the gate resistance by expanding the gate-head's dimensions is a well known approach to improving NF_{min}. With conventional InP-based HEMTs, however, a wider gate head results in an increase in parasitic gate-capacitance because of the shorter gate-to-drain and gate-to-source distance. We successfully reduced the parasitic gate-capacitance in InP-based HEMTs with a wide gate-head by employing a cavity structure.

II. Device Fabrication

An InP-based HEMT structure was grown by metalorganic chemical vapor deposition (MOCVD) on a 3-inch semi-insulating InP substrate. Table I shows the epitaxial layer structure of the InP-based HEMTs we fabricated. The HEMT has a lattice-matched i-$In_{0.52}Al_{0.48}As$ buffer layer. A pseudomorphic i-$In_{0.63}Ga_{0.37}As$ channel is 15 nm thick. The $In_{0.52}Al_{0.48}As$ supply layer consists of a 3-nm-thick spacer layer, a Si-planar doping with a sheet carrier density of 3.1×10^{12} cm^{-2}, and a 5-nm-thick Schottky barrier layer. A 5-nm-thick InP etch-stopper is employed to control the depth of the recess etching. A cap layer is made of 50-nm-thick $In_{0.63}Ga_{0.37}As$ doped with Si.

Figure 1 shows cross sections of the InP-based HEMTs with a cavity structure (9). An electron-beam lithography technique was used to fabricate both a Y-shaped gate-electrode (10) and a gate recess. The Y-shaped gate structure is very effective for preventing the top gate from peeling off, resulting in a high yield during gate-electrode fabrication. In this study, the gate-head lengths (L_h) varied from 400 nm to 1200 nm, while the gate-foot length (L_g) was fixed at 75 nm. The typical gate-recess length (L_r) between the gate-electrode and

Table I Epitaxial layer structure

Material	Thickness (nm)	Carrier concentration (cm^{-3})
n^+-$In_{0.53}Ga_{0.47}As$	50	1×10^{19}
i-InP	5	Undoped
i-$In_{0.52}Al_{0.48}As$	5	Undoped
planar doping		
i-$In_{0.52}Al_{0.48}As$	3	Undoped
i-$In_{0.63}Ga_{0.37}As$	15	Undoped
i-$In_{0.52}Al_{0.48}As$	200	Undoped
S.I. InP substrate		

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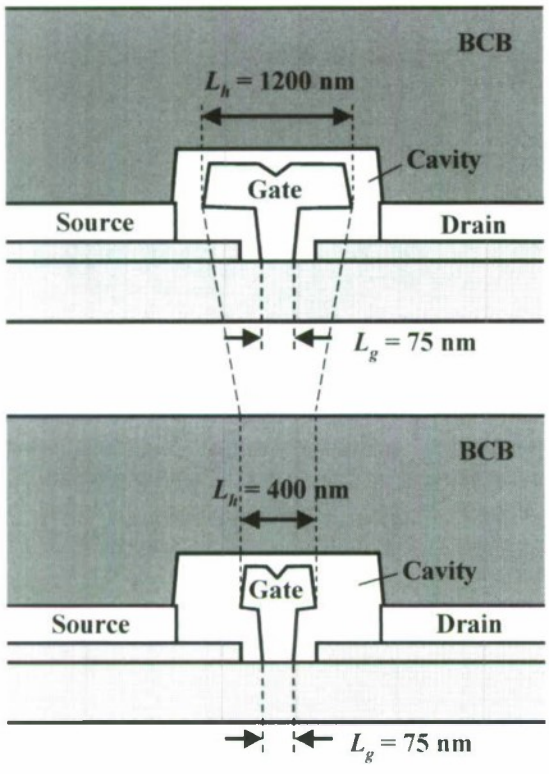

Fig. 1. Cross-sectional schematics of InP-based HEMTs with a cavity structure. The gate-head length (L_h) was varied from 400 nm to 1200 nm.

gate-recess edge, was 70 nm. The gate electrode consisting of Ti/Pt/Au was evaporated on the InP etching-stopper layer and lifted off. The transistors were fully covered with a benzocyelobutene (BCB) dielectric film. A cavity structure was formed by removing the filling material embedded in the BCB film selectively from the area that we wanted to make hollow around the gate-eleetrode. After passivating the transistors with the BCB, Au-based interconnections were ereated.

III. Device Characteristics

A. RF characteristics

RF characteristics of the fabricated InP-based HEMTs were investigated. Figure 2 shows the dependence of f_T as a funetion of gate-head length, L_h with and without a cavity structure. The gate-foot length, L_g was kept at 75 nm. The f_t decreased from 358 GHz to 301 GHz monotonically as the gate-head dimensions increased from 400 nm to 1200 nm when the gate eleetrode was fully covered with BCB and when there was no cavity, as shown in Fig. 2. Conversely, f_T stayed almost the same, about 370 GHz, for InP-based HEMTs with a cavity structure. The reason for these dependenees is considered to be that InP-based HEMTs with a eavity have a smaller dielectric constant around the gate-head regions, producing a lower parasitic capacitanee at the gate.

To estimate the parasitic eapacitance, gate-to-source eapaeitanee (C_{gs}) and gate-to-drain eapaeitance (C_{gd}) were extracted from small-signal characteristics. Dependences of C_{gs} and C_{gd} on gate-head length with and without a cavity

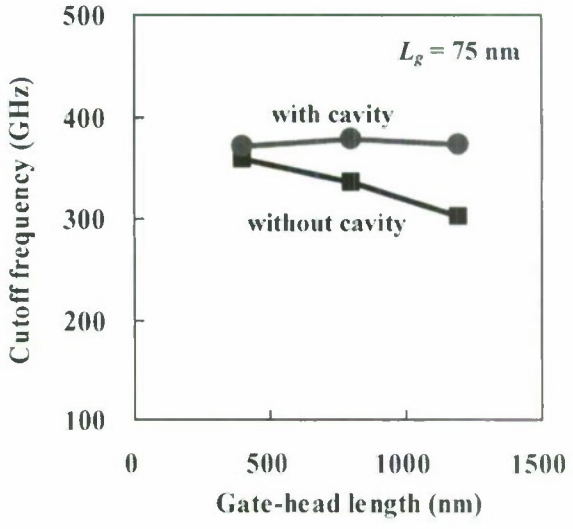

Fig. 2. Dependence of cutoff frequency on gate-head length. Gate-foot length, L_g was fixed at 75 nm.

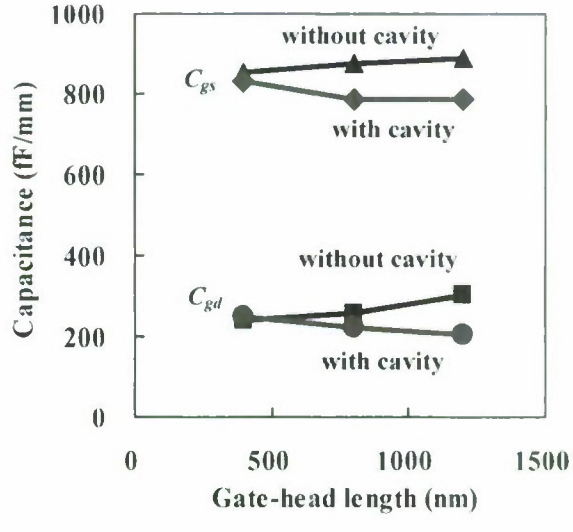

Fig. 3. Dependences of gate capacitances on gate-head length. C_{gs} and C_{gd} were extraeted from small-signal characteristics.

structure are shown in Fig. 3. In the case of HEMTs without a cavity, both C_{gs} and C_{gd} increased when the gate-head length increased. C_{gs} increased from 854 fF/mm to 889 fF/mm, and C_{gd} increased from 240 fF/mm to 303 fF/mm when the gate-head length increased from 400 nm to 1200 nm. However, each gate length was kept at 75 nm, the same as the conditions shown in Fig.1. Dependences of C_{gs} and C_{gd} on L_h, however, are small for HEMTs with a cavity structure. Moreover, the difference in g_m between HEMTs with and without a cavity structure was small even if L_h was varied. Therefore, decreasing f_t for HEMTs without a cavity structure, as shown in Fig. 1, resulted in higher values for C_{gs} and C_{gd} caused by the parasitic capacitance of BCB around the gate electrode; that is HEMTs with wide gate-head dimensions had extra parasitic capacitance. Then, f_t should be given as shown in (3.1)

$$f_T = \frac{g_m^{int}}{2\pi[(C_{gs}^f + C_{gs}^h) + (C_{gd}^f + C_{gd}^h)]}, \qquad (3.1)$$

where g_m^{int} is intrinsic transconductance, and C_{gs}^f and C_{gs}^h are gate-foot and gate-head related to gate-to-source capacitance. Similarly, C_{gd}^f and C_{gd}^h are gate-foot and gate-head related to gate-to-drain capacitance. In the equation, C_{gs}^h and C_{gd}^h indicate the parasitic capacitance caused by the gate-head. Conversely, the cavity structure effectively eliminated this parasitic capacitance of C_{gs}^h and C_{gd}^h around the gate electrode even if a wide gate-head was adopted.

B. Gate resistance

Gate resistance (R_g) under RF operation and source resistance (R_s) were extracted from DC characteristics to estimate the noise figure characteristic. Figure 4 shows R_g and R_s dependence as a function of gate-head dimensions when the gate width (W_g) was 80 μm. RF-gate resistance was calculated from a fitted curve of measured DC-gate resistance (11). A uniform R_s of 2.0 Ω, extracted from transistor parameter analysis, was employed as a function of gate-head dimensions since R_s and L_h were independent of each other. The R_g increased as L_h was reduced. R_g and R_s become similar at an L_h of 800 nm. When L_h was reduced to less than 400 nm, a rapid increase in R_g was estimated to exceed R_s.

C. Noise figure

NF_{min} was estimated as a function of gate-head dimensions. Simultaneously, the effect of a cavity structure, which would reduce parasitic capacitance, was compared. The optimum value of minimum noise figure (F_o) is expressed as Fukui's equation (12) which is given by

$$F_0 = 1 + K_f \frac{f}{f_T}\sqrt{g_m^{int}(R_g + R_s)}, \qquad (3.2)$$

where K_f is a fitting factor and f is frequency. First, a fitting factor of K_f was determined to be 0.918 using measured f_T, NF_{min} and other parameters that were obtained before (8) under a drain-to-source voltage (V_{ds}) of 0.8 V at 94 GHz. R_g and R_s were already estimated for each L_h as shown in Fig. 4. Consequently, utilizing (3.2) and estimated parameters, NF_{min} was calculated as a function of L_h at 94 GHz, as shown in Fig. 5. A remarkable improvement in NF_{min} was expected by expanding the gate-head dimensions both with and without a

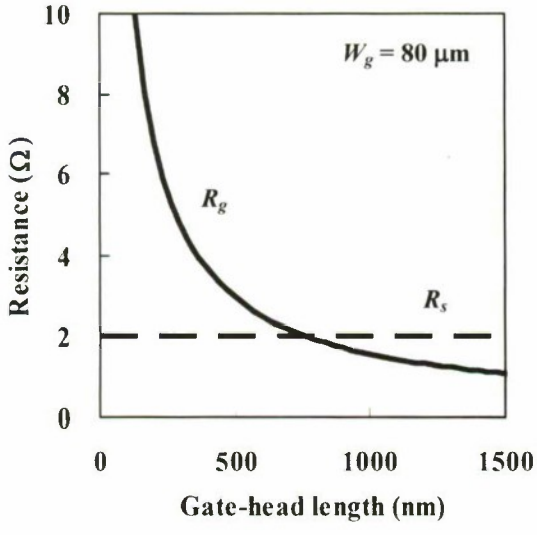

Fig. 4. Dependences of estimated gate resistance and source resistance on gate-head length.

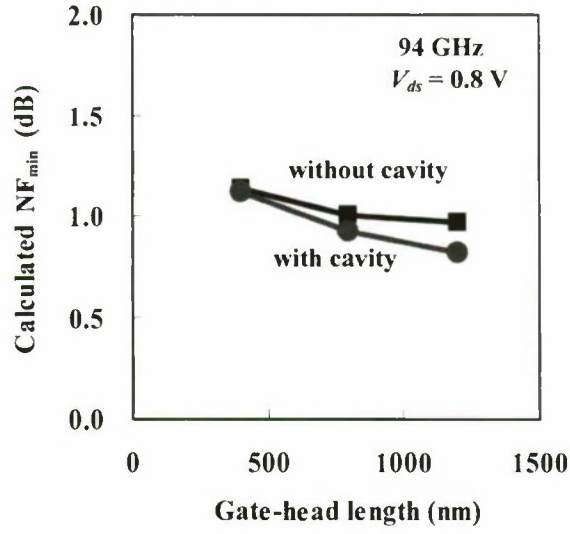

Fig. 5. Dependences of calculated NF_{min} on gate-head length at 94 GHz with and without a cavity structure.

cavity structure. In particular, the cavity structure indicated a lower NF_{min} due to the suppression of parasitic capacitance around the gate head. Moreover, a wide gate-head structure reduced R_g, resulting in a further improvement in NF_{min}. Similarly, when no cavity structure was employed, wide gate-head dimensions improved NF_{min} to the same level as that seen with a cavity structure. This result indicates that reducing R_g using a wide gate-head structure is more effective for obtaining a low NF_{min} than reducing the gate-head dimensions to suppress parasitic capacitance.

Accordingly, InP-based HEMTs with a wide gate-head indicated a superior performance for improving NF_{min}; however, f_t was degraded by increasing the gate-head dimensions because of the increased parasitic capacitance. Further improvement of NF_{min} was expected using a cavity structure which eliminated parasitic capacitance around the gate electrodes.

IV. Conclusion

In summary, dependences of NF_{min} at 94 GHz on gate-head length were studied using InP-based HEMTs. NF_{min} was improved effectively using a cavity structure even though a wide gate-head was employed. Wide gate-head InP-based HEMTs with a cavity structure are promising candidates for improving low-noise properties at millimeter-wave frequencies.

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HIGH RELIABILITY PERFORMANCE OF 0.1-μm Pt-Sunken Gate InP HEMT LOW-NOISE AMPLIFIERS ON 100 mm InP SUBSTRATES

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Abstract

Accelerated temperature lifetesting at $T_{channel}$ of 240, 255, and 270 °C was performed on 0.1-μm Pt-sunken InP HEMT low-noise amplifiers fabricated on 100 mm InP substrates. The reliability performance was evaluated based on ΔS21 < -1 dB at 35 GHz. The lifetesting results exhibit activation energy of approximately 1.8 eV and lifetime projection of 99% reliability and 90% confidence exceeds $1x10^8$ hours at $T_{channel}$ of 125 °C. The high reliability demonstration of 0.1-μm Pt-sunken gate InP HEMT low-noise amplifiers on 100 mm InP substrates is essential for advanced military/space applications requiring high reliability performance.

I. Introduction

Superior microwave and millimeter wave performance of InP high electron mobility transistor (HEMT) microwave monolithic integrated circuits (MMICs) has been demonstrated over the frequency ranges of 44 GHz (1-2), 94 GHz (3-5), 118 GHz (6-7), 155 GHz (8-9), 183-220 GHz (8, 10-12), and beyond 250 GHz (13-15). To ensure the successful insertion of InP HEMT MMICs for advanced military/space applications, it is important to demonstrate the high reliability performance of InP HEMT MMICs subjected to accelerated temperature lifetest. Since 1993, the reliability performance under accelerated temperature lifetest on either discrete InP HEMT transistors or MMICs on 75 mm substrates has been extensively investigated (16-18). Those studies resulted in the demonstration of high reliability performance on 0.07-μm (19), and 0.1-μm (20) InP HEMTs in addition to metamorphic HEMT (MHEMT) (21-22) technologies. These achievements of superior microwave performance and high reliability led to the first insertion of InP HEMT low-noise amplifiers (LNAs) operating at Q-band for phased-array applications at Northrop Grumman Corporation (NGC) [2].

With the increasing applications of high performance InP HEMT LNAs inserted into the large-aperture phased-array radar systems, system designs require several thousands to several hundreds of thousands of LNAs. To further reduce the system cost, it is essential to develop InP HEMT MMIC technology on 100 mm InP substrates. Accordingly, Northrop Grumman began to transfer 75 mm InP HEMT processes to 100 mm InP HEMT processes in 2004 (23-24).

Although the reliability investigation of InP HEMTs on 75 mm InP substrates was extensively explored, few reliability evaluations of InP HEMTs have been explored on 100 mm InP substrates. In 2007, the preliminary reliability performance of 0.1-μm InP HEMT LNAs subjected to 2-temperature lifetest was reported on 100 mm InP substrates (25). Nevertheless, it is essential to further improve reliability performance of InP HEMT LNAs on 100 mm InP substrates for advanced military/space applications requiring high reliability performance.

To improve the reliability performance of InP HEMTs, new gate metal stacks were explored recently to reduce the Ti-InAlAs reaction (26-28). It was found that the gate metal stacks in InP HEMTs are important for high reliability performance demonstration. While the Pt-sunken gate was initially introduced to fabricate high performance and enhancement-mode InP HEMTs (29-30), the reliability evaluation of 0.1-μm Pt-sunken gate InP HEMT LNAs on 100 mm InP substrates has been lacking. In this study, accelerated temperature lifetesting at $T_{channel}$ of 240, 255, and 270 °C was performed on 0.1-μm Pt-sunken InP HEMT LNAs fabricated on 100 mm InP substrates. The reliability performance was evaluated based on ΔS21 < -1 dB at 35 GHz. The lifetesting results exhibit activation energy (Ea) of approximately 1.8 eV and lifetime projection of 99% reliability and 90% confidence is over $1x10^8$ hours at $T_{channel}$ of 125 °C, which exceeds the typical bench mark of $1x10^6$ hours at $T_{channel}$ of 125 °C.

II. Lifetesting Vehicles on 100 mm InP Substrates

To evaluate the reliability performance of 0.1-μm Pt-sunken InP HEMTs on 100 mm InP substrates, a K–band balanced LNAs operating over 27- 40 GHz was designed for the standard evaluation circuitry (SEC). The material profile of Pt-sunken gate InP HEMTs is similar to that of previous InP HEMTs with conventional Ti/Pt/Au gate on 100 mm InP substrates (25). The SEC is a two-staged balanced amplifier with a total gate periphery of 160-μm on the 1st stage's devices

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Q1 & Q2 and 400-μm on the 2nd stage's devices Q3 & Q4 as shown in Fig. 1. The gate and drain resistors are also added into the gate and drain electrodes for SEC stability under radio frequency operation. As shown in Fig. 1, InP HEMT SECs with devices Q1, Q2, Q3, and Q4 were fabricated on 4-inch InP substrates for accelerated temperature lifetesting to evaluate the reliability performance of 0.1-μm Pt-sunken gate InP HEMT LNAs on 100 mm InP substrates.

Figure 2 shows the representative d.c. current-voltage (I-V) curves of discrete 0.1-μm Pt-sunken InP HEMTs. The devices exhibit excellent pinch-off characteristics and show an average peak transconductance (g_{mp}) of 1,000-1,100 mS/mm and maximum drain current (I_{MAX}) of 600-650 mA/mm. Also, Pt-sunken InP HEMTs with 0.1-μm gate length demonstrate the unity-gain-cut-off frequency (f_T) of 170-180 GHz and maximum frequency of 180-190 GHz. It was observed that the dc and radio-frequency ($r.f.$) performance in Pt-sunken InP HEMTs is comparable to that of InP HEMTs with conventional Ti/Pt/Au gate metal stacks.

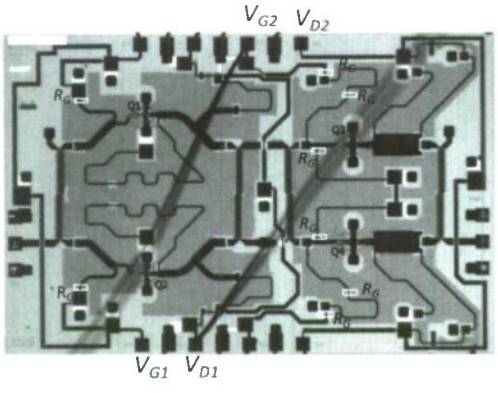

Figure 1: Optical photograph of a 0.1-μm Pt-sunken gate InP HEMT LNA as an SEC for accelerated temperature lifetesting.

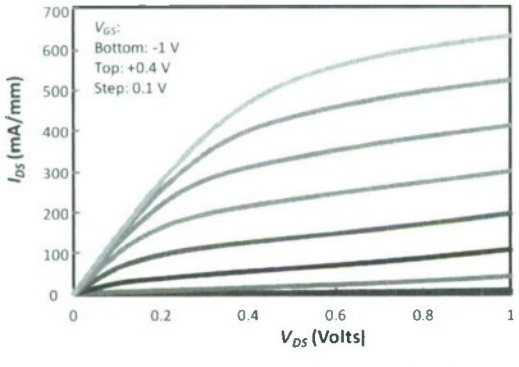

Figure 2: I-V characteristics of a 0.1-μm Pt-sunken gate InP HEMT on 100 mm InP substrates.

Additionally, scanning-transmission-electron-microscope (STEM) technique was introduced to gain insight into the Pt-sunken gate metals and semiconductor materials. The STEM micrograph of a virgin SEC without stress as shown in Fig. 3 reveals a slight Pt-sinking into the InAlAs Schottky barrier layer. The initial Pt-sinking was introduced by the front-side processes of NGC's Pt-sunken InP HEMT LNAs on 100 mm InP substrates, therefore causing a gray interface line as shown in Fig. 2. The region below the gray interface line consists of Pt-InAlAs intermetallic due to slight in-process-induced Pt diffusion into the InAlAs Schottky barrier material.

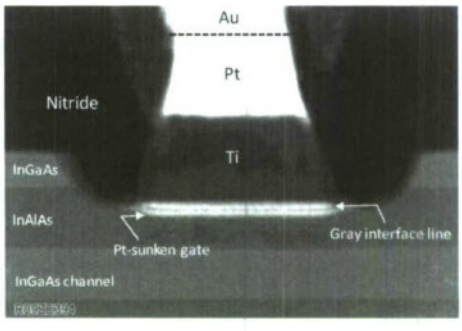

Figure 3: STEM micrograph of 0.1-μm Pt-sunken gate InP HEMTs used in the devices Q1, Q2, Q3, and Q4 as shown in Fig. 1.

III. Three-Temperature Lifetesting

Three-temperature lifetesting at $T_{channel}$ of 240, 255, and 270 °C was performed on the SECs stressed at V_{DS} = 1.5 V and I_{DS}= 150 mA/mm in an N_2 environment. During lifetesting, comprehensive characterization of d. c. and $r.f.$ parameters from 27 to 40 GHz was performed to investigate device degradation. The failure criterion was based on the ΔS_{21} of -1 dB at 35 GHz. During lifetest, the SECs were stressed until ΔS21 at 35 GHz < -1 dB as shown in Fig. 4. The ΔS21 at 35 GHz was based on test bench measurements at room temperature. The initial S_{21} increase was found to be caused by the initial nominal Pt gate sinking effect [31]. The continuing lifetesting of Pt-sunken InP HEMT SECs after reaching ΔS_{21}= -1 dB could cause more drastic S_{21} degradation. The subsequent STEM analysis reveals that the drastic S_{21} degradation is caused by the progressive diffusion of the Pt Schottky junction into the InAlAs Schottky barrier and the InGaAs channel layer (32).

Figure 5 shows the evolutions of I_{DS} and g_m characteristics versus V_{GS} on the 1st stage of an SEC subjected to lifetesting at $T_{channel}$ of 270 °C for 800 hrs. The electrical degradation consists of initial I_{DS} and g_m shifting due to the Pt-sinking into the InAlAs Schottky barrier layer, followed by I_{DS} and g_m degradation caused by progressive Schottky junction degradation together with the I_G induced debias effects on Q1, Q2, Q3, and Q4 devices as shown in Fig. 1. During the accelerated temperature lifetesting, the I_G in Q1, Q2, Q3, and Q4 devices was gradually increased. The magnitude of I_G and the resistance values of the stability R_G (as shown in Fig. 1)

could debias the devices in a low-noise amplifier (33). As shown in Fig. 6, Q3 and Q4 in the 2nd stage have higher debias voltages than those of Q1 and Q2 in the 1st stage, where the debias voltage is defined as I_G*R_G. As a result, the distinct characteristics of I_{DS} and g_m degradation and the oven's V_G evolutions between the 1st and 2nd stages in an SEC were observed.

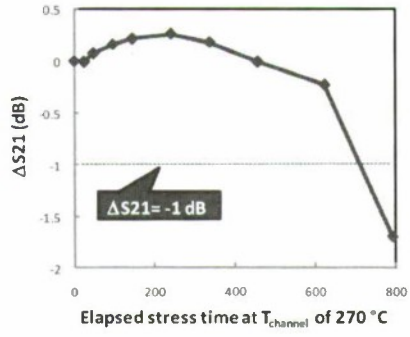

Figure 4: S21 evolution of a 0.1-μm Pt-sunken gate InP HEMT SEC lifetested at $T_{channel}$ of 270 °C.

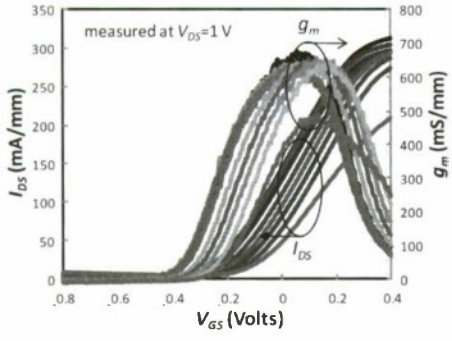

Figure 5: Evolution of I_{ds} and g_m versus V_{GS} of a 0.1-μm Pt-sunken gate InP HEM SEC (1st stage) lifetested at $T_{channel}$ of 270 °C.

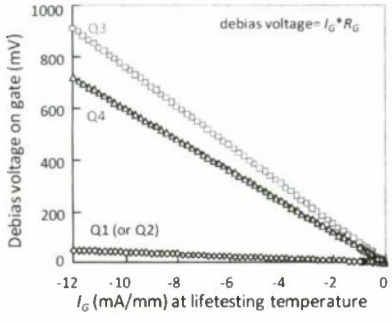

Figure 6: Debias voltage of a Pt-sunken gate InP HEMT in Q1, Q2, Q3, and Q4 versus I_G at lifetesting temperature.

IV. Reliability Performanee

The reliability performanee was evaluated based on the failure eriterion of ΔS_{21} of -1 dB at 35 GHz. Figure 7 shows the log-normal time-to-failure distribution of three-temperature lifetesting with a sigma of approximately 0.46. The Arrhenius plot shown in Fig. 8 exhibits an Ea of approximately 1.8 eV. The projected reliability performance with 99% reliability and 90% confidence exceeds $1x10^8$ hours at $T_{channel}$ of 125 °C. The high reliability demonstration of 0.1 μm Pt-sunken gate InP HEMT LNAs on 100 mm InP substrates is crucial for advaneed military/spaee applications requiring high reliability performance.

V. Conclusion

For the first time, aeeelerated temperature lifetesting at $T_{channel}$ of 240, 255, and 270 °C was performed on 0.1 μm Pt-sunken InP HEMT LNAs fabricated on 100 mm InP substrates. The lifetime projection with 99% reliability and 90% confidenee exceeds $1x10^8$ hours at $T_{channel}$ of 125 °C. The promising reliability demonstration of 0.1 μm Pt-sunken gate InP HEMT LNAs on 100 mm InP substrates is essential for advanced military/space applications requiring high reliability performance.

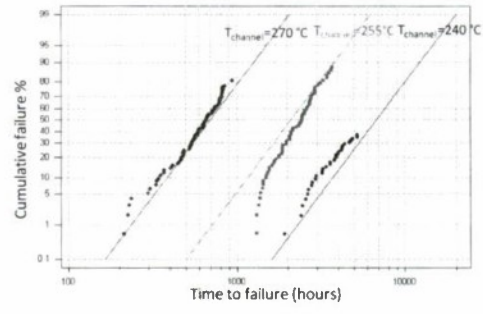

Figure 7: Log-normal time-to-failure distribution of three-temperature lifetesting at $T_{channel}$ of 240, 255, and 270 °C.

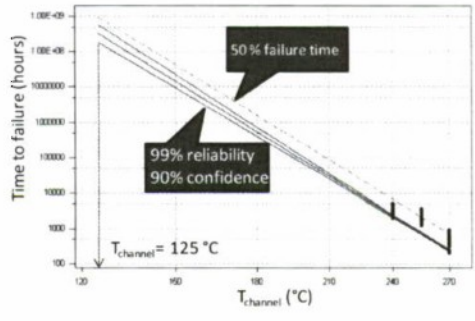

Figure 8: Arrhenius plot of three-temperature lifetesting on 0.1-μm Pt-sunken gate InP HEMT LNAs subjeeted to lifetesting at $T_{channel}$ of 240, 255, and 270 °C.

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Aluminum-Free GaInP/GaInAs pHEMTs for Low-Noise Applications with peak f_T = 256 GHz and peak f_{MAX} = 360 GHz

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Abstract

Al-free HEMTs show advantageous characteristics in terms of LF-noise, low-temperature performance, breakdown behavior, high-frequency power performance as well as reliability [1]. In the present work, we report the technology and performance of 100 nm gate length Al-free GaInP/GaInAs pseudomorphic HEMTs grown by MOVPE on semi-insulating InP substrates. The epitaxial layer structure involves an In–rich channel achieving room temperature mobilities of 8,300 cm^2/Vs. The fabrication of 100 nm T-Gate HEMTs gives rise to the highest reported f_T = 256 GHz and f_{MAX} = 360 GHz for Al-free GaInP/GaInAs InP pHEMTs. DC characterization yields shows saturation currents < 400 mA/mm and a maximum transconductance of 640 mS/mm.

I. Introduction

In the present work we re-visit the idea of AlInAs–free InP/GaInAs HEMTs in a high-performance 100 nm gate process. The concept is not new, having been explored in some depth, notably with the work of Heime and co-workers [1] who achieved promising GaInP/GaInAs/InP pHEMTs with cutoff frequencies reaching f_T = 130 GHz. Despite initial successes and indications that the Al-free structures showed favorable properties, Al-free pHEMTs did not meet with broad acceptance.

AlInAs/GaInAs High Electron Mobility Transistors (HEMTs) offer the best low-noise amplification properties available [2]. They thus play key roles in many applications ranging from telecommunication, to radio astronomy low-noise receivers, and finally in military systems. Unfortunately, the AlInAs barrier layer and its sensitivity to surface conditions are associated with device non-idealities such as the kink effect as well as to reliability problems [3]. Some of these shortcomings can be alleviated and/or solved through the insertion of InP etch-stop layers in the top barrier, but the idea of a completely Al-free transistor remains interesting.

Considering that the state-of-the-art performance of low-noise HEMTs has stagnated for nearly 15 years, we elected to re-examine Al-free GaInP/GaInAs pHEMTs at ETHZ.

II. Experimental Procedure

The MOVPE grown layers used here consist, from the bottom up, of a 1.8 µm Fe-doped InP buffer layer, a 550 nm not intentionally doped (n.i.d) InP buffer layer, a 17 nm $Ga_{0.36}In_{0.64}As$ n.i.d. channel, a 3 nm n.i.d. $Ga_{0.21}In_{0.79}P$ spacer, a 1.5 nm Si-doped (1.7×10^{19} cm^{-3}) $Ga_{0.21}In_{0.21}P$ electron supply layer, a 6.5 nm n.i.d. $Ga_{0.21}In_{0.79}P$ barrier layer followed by a 10 nm Si-doped (2×10^{19} cm^{-3}) $Ga_{0.47}In_{0.53}As$ cap layer. Hall measurements with removed cap layer revealed room temperature mobilities of 8,300 cm^2/Vs with corresponding sheet densities of 4.2×10^{11} cm^{-2}. Work is currently underway to further improve these transport properties, and we are here principally interested in providing a proof-of-concept to validate to validate the Al-free approach.

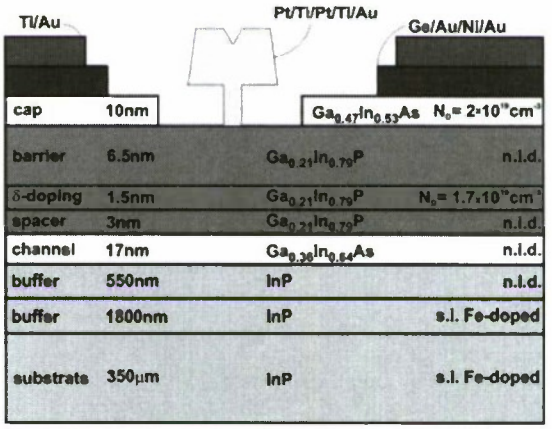

Fig. 1. Cross-sectional view of investigated Al-free $Ga_xIn_{1-x}As$ /$Ga_xIn_{1-x}P$ /InP pHEMTs.

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Device fabrication began with Ohmic contacts consisting of a Ge/Au/Ni/Au metal layer stack with subsequent annealing at 295 °C under forming gas (5% H_2 in N_2). Post-process TLM measurements revealed contact resistances of 0.13 Ω-mm on linear TLM patterns. Mesa isolation was carried out with H_3PO_4:H_2O_2:H_2O for etching GaInAs layers, H_3PO_4:HCl:H_2O for etching GaInP layers and HBr:HNO_3:H_2O for smoothing the InP buffer surface

After patterning PMMA950k with a 30 kV e-beam exposure, gate recess was carried out in succinic acid, resulting in a final recess length of L_r = 60 nm (gate metal to cap distance). Careful investigation with the SEM and AFM confirm the selectivity of succinic acid for GaInAs with respect to GaInP (GaInP < 1 nm/min). The GaInP barrier can therefore be considered not to be etched during the gate recess process.

T-gates consisting of 100 nm gate foot lengths with a 500 nm wide gate head were centered in 1, 2 and 4 µm source-drain spacings using two 30 kV exposure steps into a four layer resist stack consisting of PMGI/ZEP/PMGI/ZEP (10/200/550/270 nm). Carefully set reflow conditions in an RTA changed the negative resist flanks into positive flanks enabling e-beam evaporation of conformal gate metal films consisting of Pt/Ti/Pt/Ti/Au (5/30/20/20/325nm).

In later steps, a Ti/Au overlay metallization was e-beam evaporated followed by 2.5 µm of electroplated gold were electroplated on the device pads to enable good bonding and probing conditions.

III. Results

DC measurements carried out with an HP4156B semiconductor parameter analyzer show the output characteristics of a representative pHEMT with L_g of 100 nm and a T-shaped gate of 2 × 75 µm. As shown in Fig. 2 the device shows well-behaved current saturation over the complete V_{DS} voltage range and good pinch off characteristics up to 1.0 V. The rather low maximum output drain current of < 400 mA/mm can be attributed to the high sheet resistance in the channel due to the low sheet density of 4.2 × 10^{11} cm^{-2}.

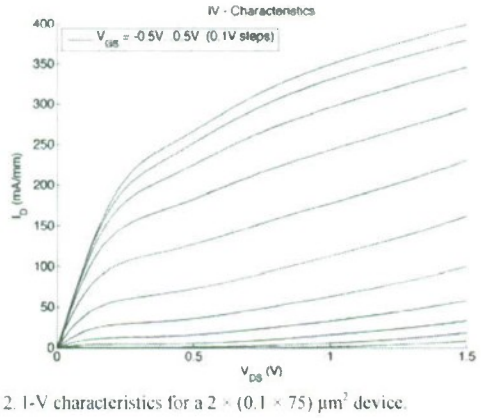

Fig. 2. I-V characteristics for a 2 × (0.1 × 75) µm² device.

The limited peak transconductance of 650 mS/mm is reached at V_{GS} = 0.1 V and V_{DS} = 1.0 V (Figs. 3) and would also profit from a higher sheet density in the channel.

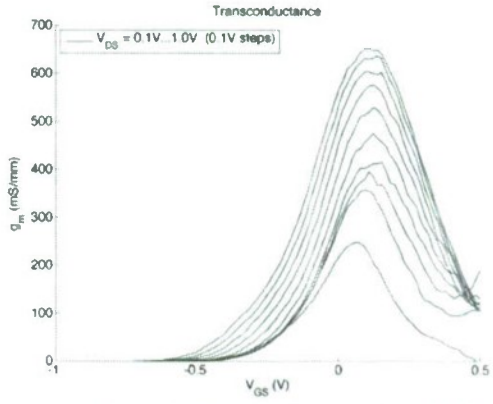

Fig. 3. Maximum transconductance of 650 mS/mm achieved at V_{GS} = 0.1 V and V_{DS} = 1.0 V.

RF measurements were performed from 0.2 to 40.2 GHz with an HP8510C vector network analyzer using a LRRM with an off-wafer calibration substrate. On-wafer open and short patterns which are geometrically identical to the devices were used to subtract pad parasitics from the measured S parameters. Fig. 4 plots the transistor microwave performance biased at V_{GS} = 0.15 V and V_{DS} = 1.05 V.

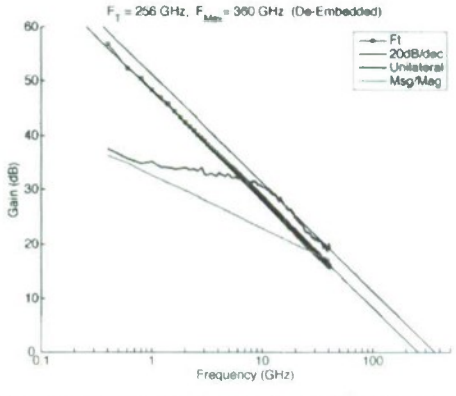

Fig. 4. RF measurements of 2 × (0.1 × 75) µm² device biased at V_{GS} = 0.15 V and V_{DS} = 1.05 V yields a peak f_T of 256 GHz with simultaneous f_{MAX} of 360 GHz.

After pad de-embedding extrapolation of $|h_{21}|^2$ and Mason's maximum unilateral gain U with a roll-off of – 20 dB/dec yield a peak f_T of 256 GHz and a peak f_{MAX} of 360 GHz at the same bias point. The f_T value was additionally verified through the Gummel's method, which yields very close agreement (deviation < 2 GHz) to the extrapolation of $|h_{21}|^2$ method.

RF measurements across a wide bias range of the device yields the overall RF behavior presented in Fig. 5 and Fig. 6. It is interesting to note that the f_T and f_{MAX} "sweet-spots" are located in close vicinity to each other with respect to the bias

point. This results in simultaneously high f_T and f_{MAX} values which a desirable feature for circuit design.

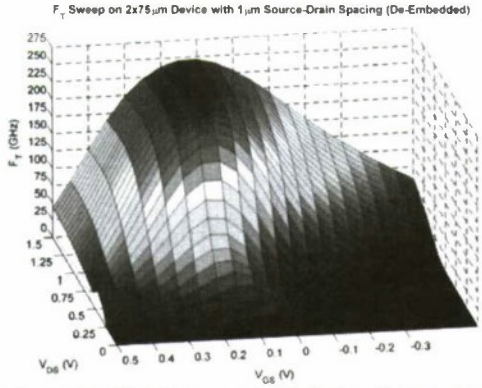

Fig. 5. A wide range bias sweep depicts the broad high f_T plateau (with only pad effects subtracted).

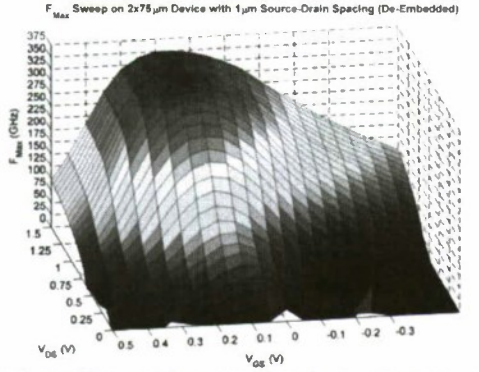

Fig. 5. A wide range bias sweep shows the f_{MAX} bias dependence (with only pad effects subtracted).

To our knowledge, these are the best results ever achieved with Al-free GaInP/GaInAs pHEMTs, and demonstrate the potential of Al-free pHEMTs for future low-noise high-speed applications.

IV. Conclusions

In this study, we reported on the fabrication of Al-free HEMTs making use of the highly-insulating InP buffer layers grown by MOCVD. The commonly used barrier material AlInAs was replaced with GaInP which only required a slight adaption in the fabrication process.

Despite a low maximum drain current can be attributed to the low sheet densities in the channel, the RF device performance is nevertheless impressive considering no channel design optimization was carried out, showing the highest simultaneous f_T and maximum f_{MAX} values ever achieved in Al-free GaInP/GaInAs pHEMTs.

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Friday
June 4, 2010

FrA1 Integrated Receivers and Related Components
FrB1 Advanced Heteroepitaxy
FrA2 Photonic Crystal Devices
FrB2 FET for Logic

2010 International Conference on Indium Phosphide and Related Materials
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Waveguide-integrated Components Based 100 Gb/s Photoreceivers: From Direct to Coherent Detection

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Abstract— **Monolithically integrated InP-based photoreceivers, either comprising pin-diodes with travelling-wave amplifiers for electrical post amplification or 90° hybrids integrated with a pair of balanced detectors forming coherent QPSK photoreceivers, are presented for 100 GbE transmission concepts.**

pinTWA RX, Optical 90° hybrid, DP-QPSK, fiber optic links

I. Introduction

100 G Ethernet is a forthcoming application to manage the ever increasing data traffic in optical communications, while improving efficiency compared to the common OSI seven layer model. Short and long-haul transmission distances are differently affected by fiber impairments, thus the OOK modulation used for short distances in ETDM systems is complemented by spectrally efficient advanced modulation formats, e.g. DP-QPSK, applied to larger distances. Monolithically integrated InP-based photoreceivers, either comprising pin-diodes with travelling-wave amplifiers for electrical post amplification or 90° hybrids integrated with a pair of balanced detectors forming coherent QPSK photoreceivers, are key components of the O/E frontends and are of great interest for 100 GbE transmission experiments.

II. Basic Receiver Concepts for 100GE

Figure 1 and Figure 2 compare basic receiver concepts applicable to 100GE, first the ETDM concept and second the DP-QPSK concept.

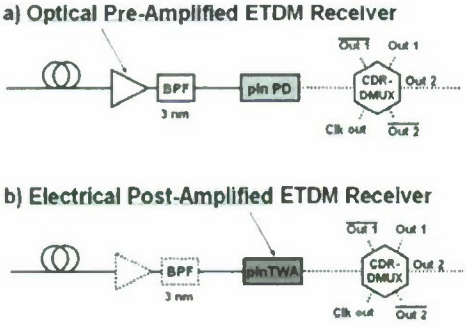

Figure 1. ETDM receiver concepts:
a) with optical pre-amplification and high-power pin photodiode, driving directly the CDR-DMUX circuit.
b) avoiding optical pre-amplification by using a pinTWA frontend.

In the ETDM concept mostly high-power pin photodiodes are used behind optical pre-amplification [1, 2], cf. to Figure 1a. For avoiding the costly optical pre-amplification, pinTWA frontends (pin photodiode with subsequent travelling-wave amplifier) can be used, which now can handle 107 Gbit/s datarates [3]. Within the ETDM concept all components in the O/E frontend and the input stage of the CDR DMUX must be capable to handle the ultra-high symbol rate of up to 112 Gbit/s. While the basic concept is simple, it will be only useable, when compact and ultra-high speed components are available. The digital electronic components (CDR-DMUX) are subjected to cost-efficient production and high integration level, using SiGe or InP technologies. Furthermore, for short range systems the fiber impairments may be negligible or easily compensated.

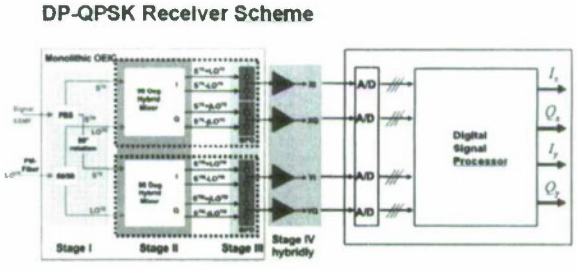

Figure 2. DP-QPSK receiver concept:
The incoming light is split-off with respect to its TE and TM polarization components, while a local oscillator (LO) enables coherent detection within two 90°-hybrid receiver subunits (dashed lines) for both polarizations, which each separate the in-phase (I) and quadrature (Q) signal informations; after linear amplification within TIAs 4 A/D converters feed their signals into a digital signal processor (DSP)

Promising techniques to re-use the available fiber base including their chain of optical amplifiers are based on (differential) quadrature phase-shift keying ((D)QPSK) modulation formats, which operate at reduced symbol rates. Therefore the polarization of the light is used for additional modulation. Thus, only 28 Gbaud/s symbol rate is sufficient to transmit a data rate of 112 Gbit/s, were a gain of factor 4 by polarization multiplexing and by QPSK modulation is achieved. The advantage of the concept is the relatively low-speed demands on the frontend components. Figure 2 shows a generic receiver concept applying a local oscillator for

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coherent detection within two 90°-hybrid receiver subunits. The polarization manipulation of the incoming light is done actually by hybrid components, like free-space optics, while their integration with the subsequent 90°-hybrid subunits is technologically challenging in view of amplitude uniformity and phase accuracy of the I, Q tributaries.
This paper focuses on the realization of the O/E converting frontends, while the subsequent electronics and complete system experiments of receivers of both kind (ETDM and DP-QPSK) are cited from preceeding work and literature.

III. PINTWA PHOTORECEIVERS

The pinTWA photoreceiver OEIC comprises a waveguide-integrated photodetector together with a travelling-wave amplifier [3], to save a 100 GHz interconnection, which otherwise is accomplished by tedious wire bonding or costly 1mm-connectors. Further more its on-chip-gain may spare an otherwise needed expensive EDFA in short range communications. The photodiode with an active area of 4 x 10 μm^2 and a InGaAsP/InGaAs heterostructure absorption layer stack is located on top of a semi-insulating ($5*10^7$ Ωcm) optical waveguide stack. The HEMTs forming the TWA are integrated by MBE over-growth after mesa-structuring the PD areas. The circuit is given in Fig. 3.

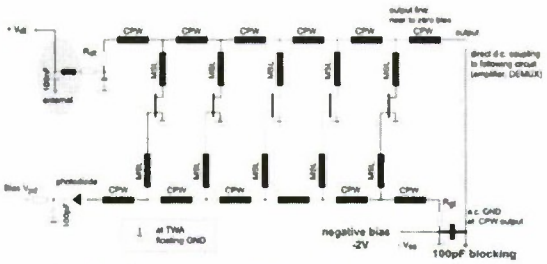

Figure 3. Circuit of the 100 Gbit/s pinTWA photoreceiver comprising a pin diode and a travelling-wave amplifier.

The bandwidth of these pinTWA receiver chips characterized by heterodyne measurements, is about 90 GHz, see Fig. 4.

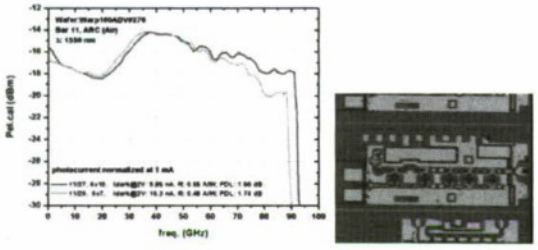

Figure 4. Electrical output power frequency response of the pinTWA OEIC measured at 1mA photocurrent (R: 0.55 A/W). TWA biasing is 1 V/30 mA; OEIC conversion gain: 29 V/W.

The advantage of applying the pinTWA concept is demonstrated in Figure 5, which exhibits a comparison of gain and bandwidth properties of single high-power photodiodes and pinTWA OEICs, comprising differently optimized travelling-wave amplifiers.

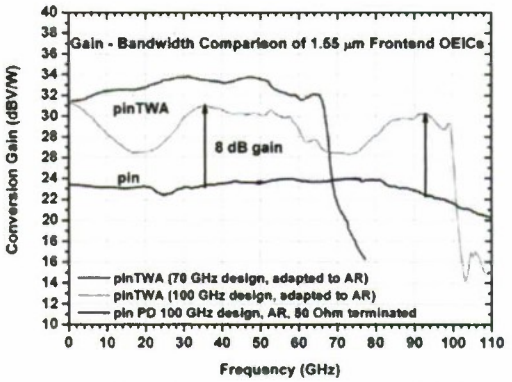

Figure 5. Conversion gain comparison between pin photodiode chips and pinTWA OEICs, designed for different bandwidths, suitable for 100GE operation.

Post-amplification gain values of more than 8 dB can be achieved, depending on bandwidth demands (70..98 GHz), thus reducing the gap between available output power of 100 Gbit/s ETDM transmitters and receiver sensitivity.

In Fig. 6 a packaged pinTWA module with fiber pigtail and 1 mm connector is shown, which is useful for system experiments, e.g. eye pattern characterization.

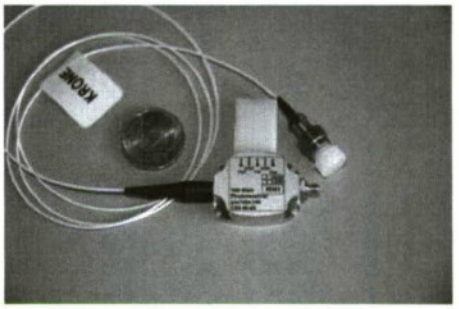

Figure 6. Packaged 107 Gbit/s pinTWA receiver module.

By using optical time domain multiplexing techniques we generated 107 Gbit/s return-to-zero (RZ) modulated data streams (PRBS) with 2^{31}-1 pattern length. In Figure 7 the

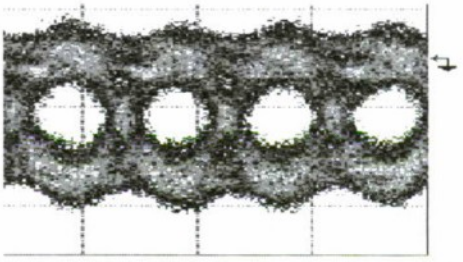

Figure 7. Received eye pattern of the module in Figure 6 at +8 dBm optical input power and 107 Gbit/s datarate; y: 100 mV/div.

optical input power to the module was adjusted to +8 dBm, resulting in a clearly opened eye at 107 Gbit/s data rate. The

output of the pinTWA OEIC was proven to drive suecessfully a DEMUXing eireuit from ATL III-V lab delivering 53.5 Gbit/s at its tributary [3, 4].

IV. Monolithic 90° Hybrid Receivers

In a coherent reeeiver, the modulated phase information is decoded by 90° optical hybrid six-port deviees, whieh are key components for DP-QPSK 100 GbE transmission coneepts, elaborated at several sites worldwide [5-7] .

Two different integrated 90° hybrid versions have been proposed, using either four 3dB splitters and a phase shifter [8] or self-imaging in a multimode interferenee strueture, in whieh the phase quadrature eondition is inherently fulfilled [9]. This eontribution foeuses on the 2x4 MMI-based version [5], monolithieally integrated now with four separate indentieal photodiodes (dual-type), whieh allow a direet ehip-to-ehip intereonneetion to transimpedanee amplifiers (TIA) with differential inputs. Comprehensive investigations on the output imbalanee dependence on MMI fabrication toleranees, the PDL, and initial investigations of the thermal behaviour of the 90° hybrid reeeiver OEICs were undertaken and deseribed.

In [5] we reported two solutions to implement optical 90°-hybrids using planar waveguide teehnologies. We showed already very good quadrature phase accuracies within 7°, applying a 2x4 MMI concept. This work is continued here, with the o/e converting balanced photodiodes replaeed by pairs of dual photodiodes. Fig. 8a shows the prineipal OEIC strueture applying tapered input aeeess waveguides, a 2x4 MMI whieh equally distributes the intensity to four output ports, a standard waveguide network with appropriate erossings of low inserlion loss and low erosstalk, and the dual photodiodes. Phase shifters are used here for test purposes.

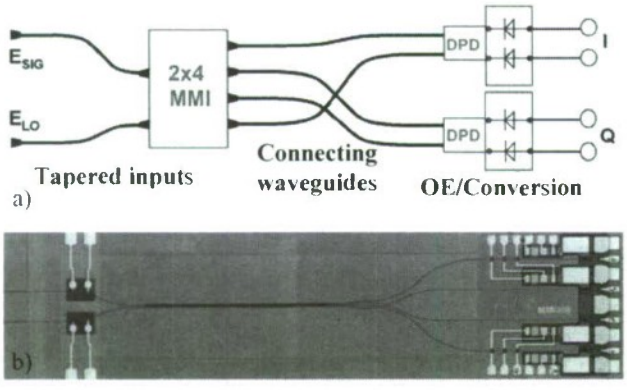

Figure 8. a) Principal design of the monolithic 90° optical hybrid receiver with one 2x4 MMI and a pair of dual photodiodes.
b) photograph of the 90°-hybrid OEIC chip.

Fig. 8b exhibits the realized AR-eoated OEIC aeeording to Fig. 8a. For toleranee studies and for eomparison between simulation and measurements, OEICs with different 2x4 MMI sizes were applied on the mask set. Insertion loss and output signal uniformity are determined as functions of different MMI widths and rib heights with fixed value for the length. The semi-insulating epitaxial sheet paekage was eompatible with earlier published ultra-high speed photodiode MOVPE-grown staek [1, 2], but with slightly inereased GaInAs absorber thickness to enhanee responsivity of the 5x30 µm² sized p-i-n diodes at 60 GHz frequeneies.

The bandwidth of the implemented photodiodes (PD) was measured using the established heterodyne method. The dual PDs and even balaneed PDs with different aetive areas showed bandwidths exeeeding 60 GHz, see Figure 9. The exploitable RF responsivity is 6 dB higher eompared to the 50 Ω terminated balaneed deteetors reported in [5].

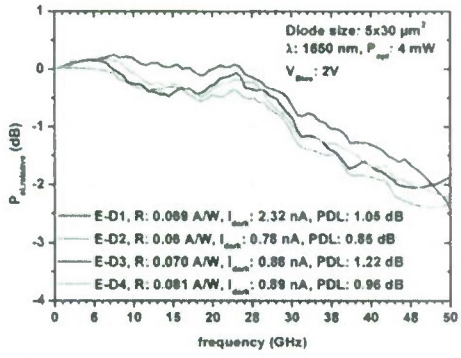

Figure 9. Conversion gain characteristics of the 4 dual pin photodiodes, measured behind the 90°-hybrid waveguide network.

One of the main challenges for the development of a suitable 90°-hybrid is the optimum design of the optical network, with a preeise eontrol of MMI width, waveguide rib height and thickness of the guiding layer. Guiding layer thickness and etching depth are well eontrolled by the epitaxy (3%) and dry etching (20nm). To investigate the impaet of the MMI width, we modified its valuc experimentally around the design eenter of the device on the wafer.

To charaeterize the performance of the 90°-hybrid, 16 photocurrent measurements are performed for each deviee at a single wavelength. We measured the eurrent of the four photodiodes for both states of polarization and for light eoupling into both input waveguides. A typical and representative data eolleetion with good uniformity is displayed in Fig. 10. Referenee detectors with identical teehnology on the same wafer show a responsivity up to 0.7 A/W.

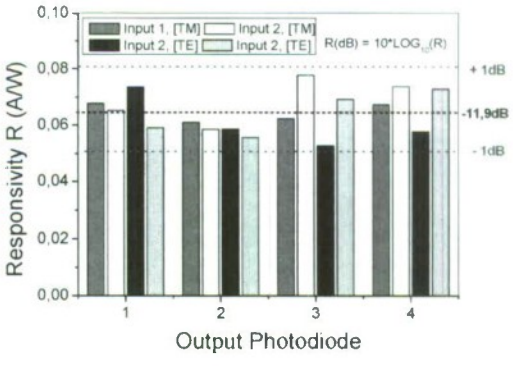

Figure 10. Responsivity at the four outputs for coupling into both inputs at TM- and TE-polarization at 1550 nm and a temperature of 20 °C.

In Fig. 11, a plot of the imbalance of the output intensities as function of the MMI-width deviation from the design value is shown. It is defined as the deviation in dB between maximum and minimum responsivity. Data are shown both for TE and for TM polarization. We observe that the imbalance increases drastically for smaller MMIs, conform with simulations. The calculated output power distribution for both input waveguides corresponds well to the measured distribution. The match between experiment and theory is best if the simulated width is 0.5µm narrower than the nominally fabricated one.

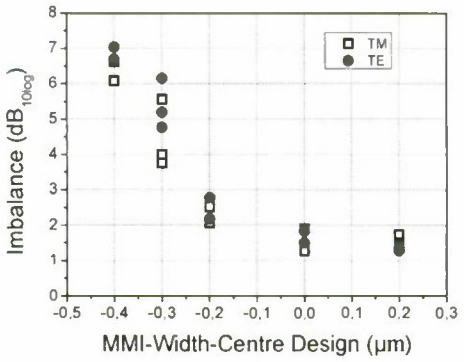

Figure 11. Imbalance of the four output signals from both inputs as function of the difference from the designed MMI width at λ=1550nm.

Finally, we investigated the temperature dependence of the responsivity over the C-band. For TM polarization we determined the mean value of the responsivity over all four outputs and the two inputs. As can be seen in Fig. 12, we nearly achieve an athermal behavior. The results for TE polarization are very similar. The temperature variation was 15° to 35°C, limited by our die level measure-ment set-up. The small changes observed indicate that the device has potential for a quite larger athermal operation range.

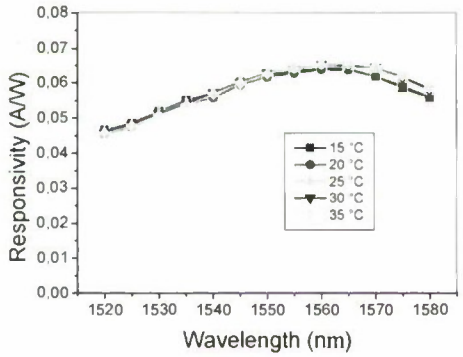

Figure 12. Responsivity as function of wavelength and temperature.

V. CONCLUSIONS

For 100GE ETDM transmission systems we showed 107 Gbit/s capable pinTWA OEICs and modules, delivering electrical post-amplification gain values up to 10 dB. For 100GE DP-QPSK transmission systems we presented a nearly athermal 2x4 MMI-based monolithically integrated InP 90° hybrid QPSK receiver OEIC operating at 50 Gbit/s for a single polarization [11], which exhibits good performance with respect to low output imbalances within ±1 dB and low PDL <1dB. These OEICs for at least 56 Gbaud/s data rates enable ultra-compact low-cost coherent receiver modules for 100 GbE applications and support even data rates of 224 Gbit/s (DP-QPSK).

ACKNOWLEDGMENT

The authors gratefully acknowledge contributions from their colleagues D. Hoffmann, A. Sigmund, W. Ebert, C. Sakkas, St. Schubert, and R. Steingrüber at the Fhl Heinrich-Hertz-Institut, Berlin. We thank colleagues from u2t for their valuable input concerning target spec., design, and characterization. This work was financed partly by the 100GET program of the German Federal Ministry of Education and Research, by the Spanish Ministerio de Ciencia e Innovacion under project ref. TSI-020400-2008-170, and supported by the EC's 100GET/CELTIC project concerning the QPSK receiver. The support from EC projects GIBON and HECTO is greatfully acknowledged with respect to the pinTWA OEICs.

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Athermal InP-Based 90°-Hybrid Rx OEICs with pin-PDs >60 GHz for Coherent DP-QPSK Photoreceivers

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Abstract **An InP-based 90° hybrid OEIC with integrated pin-photodiodes is presented. It operates unaffected in the temperature range of 15°-35° C, offering low PDL <1 dB, and stable performance in the wavelengths of 1530 nm to 1565 nm.**

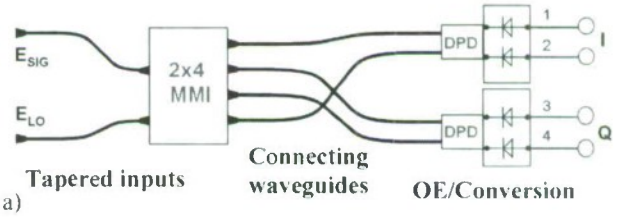
Optical 90° hybrid, monolithic QPSK receiver, waveguide-integrated photodiode, 100 GbE transmission

I. INTRODUCTION

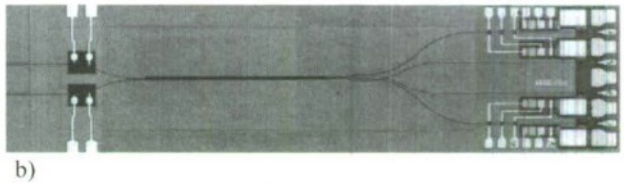
To increase the data capacity in next-generation networks, spectrally efficient data formats are essential to avoid usage of additional wavelength channels. Promising techniques are based on (differential) quadrature phase-shift keying ((D)QPSK) modulation formats. At the receiver site, the phase information is decoded by 90° optical hybrid six-port devices, which are key components for 100 GbE transmission concepts. Two different integrated 90° hybrid versions have been proposed, using either four 3dB splitters and a phase shifter [1] or self-imaging in a multimode interference structure, in which the phase quadrature condition is inherently fulfilled [2]. This contribution focuses on the 2x4 MMI-based version [3], monolithically integrated now with four separate identical photodiodes (dual-type), which allow a direct chip-to-chip interconnection to transimpedance amplifiers (TIA) with differential inputs. Comprehensive investigations on the output imbalance dependence on MMI fabrication tolerances, the PDL, the phase, photodiode characteristics, and initial investigations of the thermal behaviour of the 90° hybrid receiver OEICs were undertaken and described.

II. DESIGN AND FABRICATION

In [3] we reported two solutions to implement optical 90°-hybrids using planar waveguide technologies. We showed already very good quadrature phase accuracies within 7°, applying a 2x4 MMI concept. This work is continued here, with the o/e converting balanced photodiodes replaced by pairs of dual photodiodes. Fig. 1a shows the principal OEIC structure applying tapered input access waveguides, a 2x4 MMI which equally distributes the intensity to four output ports. It includes a standard waveguide network with appropriate crossings of low insertion loss and low crosstalk as well as dual photodiodes. The waveguide crossings are necessary to achieve the correct phase condition at the photodiodes. For the spot size transformers at the chip input an established technology is applied. The tapers are designed in the same way as for the waveguide integrated photodiodes [4,5]. These waveguides possess only a small etching depth in order to achieve a low coupling loss to the photodiodes. On the other hand the MMI, the crossings, and the curved waveguides require stronger guiding. Therefore an extra etching step is introduced in this area to enlarge the rib height of the waveguides. The resulting excess loss at the two interfaces is about 0.5 dB. The phase shifters in front of the MMI are used in this particular version only for test purposes.



a)



b)

Fig. 1: a) Principal design of the monolithic 90° optical hybrid receiver with one 2x4 MMI and a pair of dual photodiodes, b) photograph of the 90°-hybrid OEIC chip (the heating elements on the left hand side are for testing).

The semi-insulating epitaxial sheet package was compatible with earlier published ultra-high speed photodiode MOVPE-grown stack [4, 5], whereas in this paper it is with slightly increased GaInAs absorber thickness to enhance responsivity of the 5x30 μm² sized p-i-n diodes at 60 GHz.

Fig. 1b exhibits the realized anti-reflection coated OEIC according to Fig. 1a. For tolerance studies and for comparison between simulation and measurements OEICs with different 2x4 MMI sizes were applied on the mask set. Insertion loss and output signal uniformity are determined as functions of different MMI widths and rib heights with a fixed length.

III. RESULTS

One of the main challenges for the development of a suitable 90°-hybrid is the optimum design of the optical network. A precise control of MMI width, waveguide rib height and thickness of the guiding layer is essential. The guiding layer thickness can be well controlled by the epitaxial technology (3%) and is taken as constant in our design.

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All MMI performance parameters depend on the beat length of the two lowest order modes. Therefore it is important to know the dependence of this length from the design parameters. First, we show the relative MMI length as function of the rib height deviation in Fig. 2, where the optimum of the rib height and the beat length is taken as reference. Since the waveguide ribs are etched using a dry etching process that can be well controlled to about 20 nm, only a small deviation from the optimum value is expected.

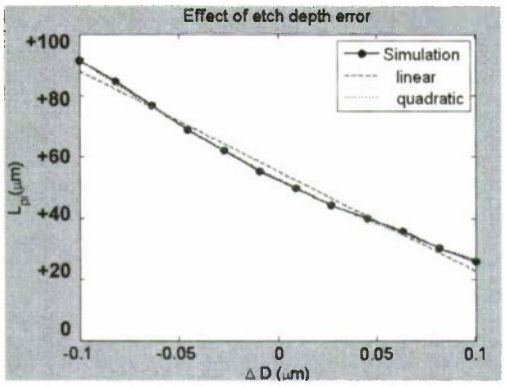

Fig. 2: Beat length sensitivity as function of the rib height deviation ΔD.

Furthermore, the impact of the MMI width variation on the beat length L_π was analyzed, which is shown in Fig. 3. Around the optimum width, a nearly linear dependence is obtained. However, each deviation from the optimum L_π will cause an excess loss.

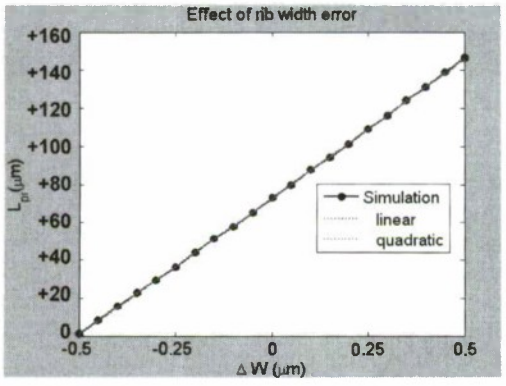

Fig. 3: Beat length sensitivity as function of MMI rib width error Δw.

This loss is not homogeneously distributed among the output ports. It also depends on the location of the inputs. Due to this result, further simulations were carried out to characterize this behavior in detail.

Fig. 4 shows the transmission loss from input 1 which is located close to the centre of the 2x4 MMI to all four outputs for both polarizations. The polarization dependency is small. Only s_{71} displays a remarkable difference. The large difference in loss for different outputs leads into a big imbalance.

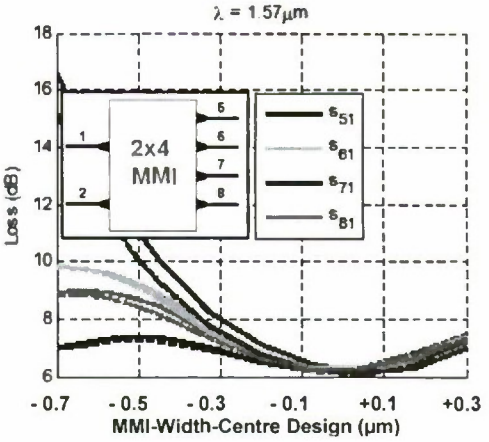

Fig. 4: Transmission loss from input 1 to all four outputs for TE- and TM-polarisation. Dashed lines correspond to TM.

The simulations show that it is essential to hit the design with an accuracy of 0.1 μm. The optimal width for minimum loss is wavelength dependent. In the present example a wavelength of 1.57 μm was chosen. As the wavelength increases, the range of acceptable widths shifts to higher values.

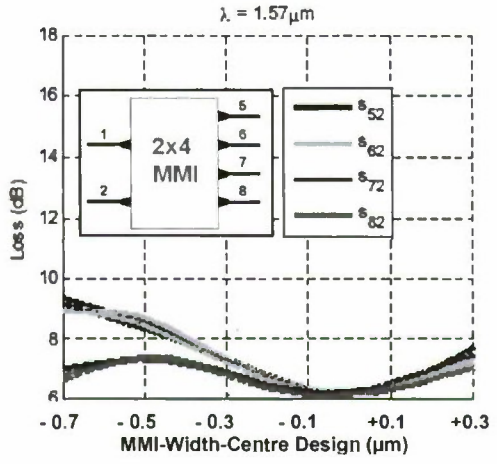

Fig. 5: Transmission loss from input 2 to all four outputs for TE- and TM-polarisation.

The dependence of loss from input 2 that is located at the edge of the MMI is less critical as can be seen in Fig. 5.

To characterize the performance of the 90°-hybrid, 16 photocurrent measurements were performed for each device at a single wavelength. We measured the current of the four photodiodes for both states of polarization and for light coupling into both input waveguides. A typical and representative data collection with good uniformity is displayed in Fig. 6. Reference detectors on the same wafer with identical technology exhibit responsivities up to 0.7 A/W.

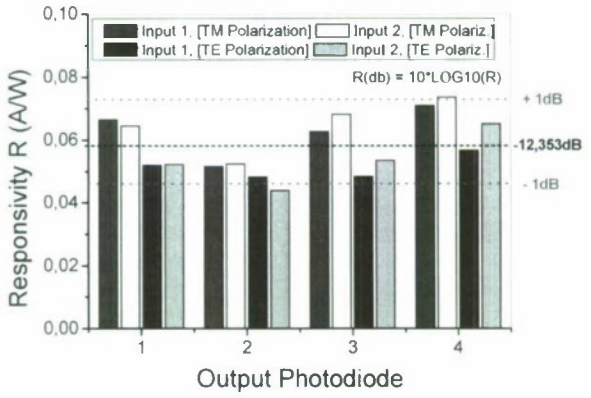

Fig.6: Responsivities at the four outputs (cf. fig. 1) for coupling into both inputs at TM- and TE-polarization at 1550 nm and a temperature of 20 °C.

In Fig. 7, a plot of the imbalance of the output intensities as function of the MMI-width deviation from the design value is shown. It is defined as the deviation in dB between maximum and minimum responsivity. Data are shown both for TE and for TM polarization. Each pair of data points corresponds to a device. Just like in the simulations we observe that the imbalance increases drastically for smaller MMIs. In simulations as well as in the experiment results, the input that is closer to the centre of the MMI displayed a larger imbalance. The match between the experimental and the theoretical work was best fitted, if the simulated width was narrower by 0.5µm than the nominally fabricated one.

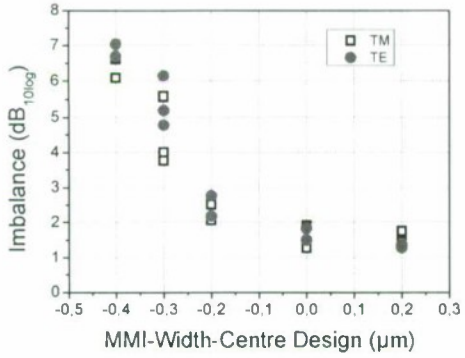

Fig. 7: Imbalance of the four output signals from both inputs as function of the difference from the designed MMI width at λ=1550nm.

From the same measured data, it was also observed that a higher average responsivity for those widths of which the imbalance is small. This is obvious since for the optimum length the image formation is best and we achieve the lowest losses.

The phase relationship between the four electrical output signals was measured with input signals that are derived from a single laser source (Fig. 8a). The optical frequency of one of the beams was shifted by 80 MHz using an acousto-optical modulator (AOM). After passing through the 2x4 MMI, the heterodyned signals are detected at the photodiodes.

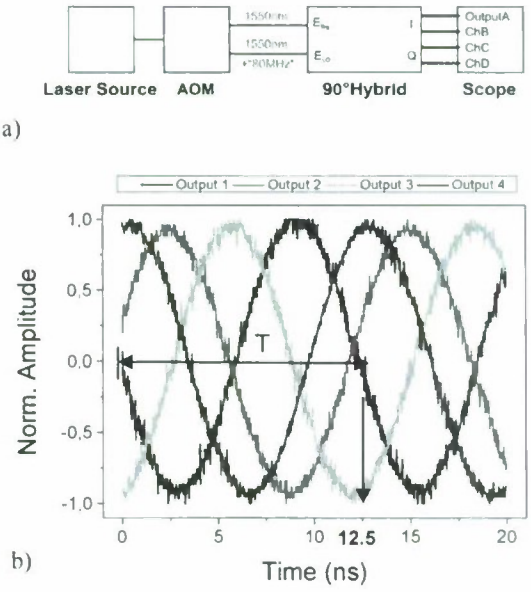

Fig. 8: a) Measurement setup with tunable laser source, AOM, device under test (90° hybrid), and oscilloscope. b) Source data of the phase measurement for the investigated 90° hybrids. The periodic length is 12.5 ns (80 MHz).

Fig. 8b shows the primary, normalized measurement result. With the modulation frequency, a periodic length of 12.5 ns is expected. Selecting output one as the reference channel, the theoretical and experimental phase difference with respect to the other channels, is exemplary 1-2: 180°/193°, 1-3: 90°/98°, and 1-4: 270°/253°.

Then, we investigated the temperature dependence of the responsivity over the C-band. For TM polarization we determined the mean value of the responsivity over all four outputs and the two inputs (average of eight measurements). As it can be seen in Fig. 9, we achieved nearly an athermal behavior. The results for TE polarization were very similar. The temperature variation was 15° to 35°C, limited by the die level measurement set-up. The small changes observed indicate that the device has potential for a quite larger athermal operation range.

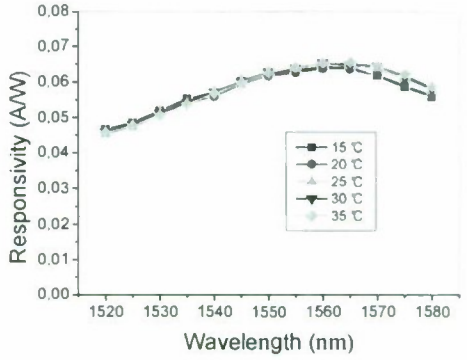

Fig. 9: Responsivity as function of wavelength and temperature.

The observed responsivity variation is about 20 % in the C-band. Deep etched, strongly guided structures have a similar performance [6].

The bandwidth of the implemented photodiodes (PD) was measured using the standard heterodyne characterization method. Fig. 10 presents the measurement of the output intensities as the function of frequency, whereas the pulse measurement is depicted in Fig. 11. The dual PDs and even balanced PDs with different active areas showed bandwidths exceeding 60 GHz. The exploitable RF responsivity is 6 dB higher compared to the 50 Ω terminated balanced detectors reported in [3].

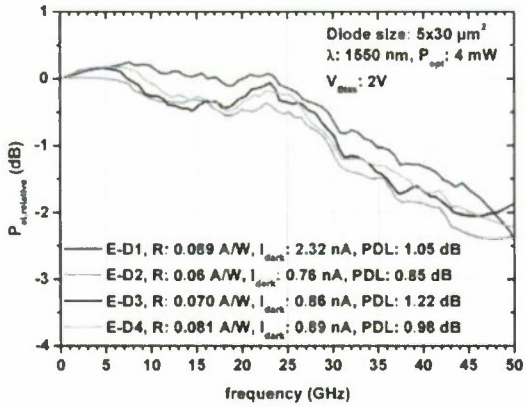

Fig. 10: Electrical power generated by OE conversion in the four output PDs of the 90° hybrid as function of frequency.

The pulse shape is quite ideal to a Gaussian shape. The post-pulse oscillation is negligibly small.

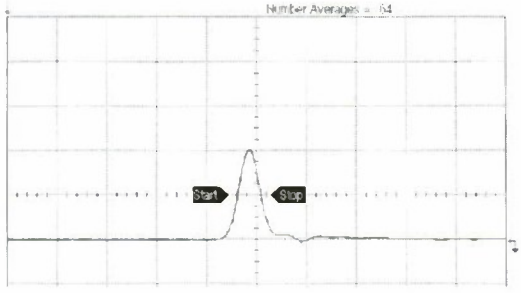

Fig. 11: Electrical voltage as function of time. A 3.5 ps wide optical pulse was applied to an input port of the 90°-hybrid. The pulsewidth is 9.14 ps, risetime 6.10 ps, and fall time 7.04 ps.

IV. Conclusions

We presented a nearly athermal 2x4 MMI-based monolithically integrated InP 90° hybrid QPSK receiver OEIC comprising spot size converters, an optical waveguide network of two etching depths, and two pairs of dual photodiodes. The good performance with respect to low output imbalances within ±1 dB and low PDL <1dB depends on the correct design of the MMI and its precise technological realization within ±100 nm width control. The output balance of the investigated 90 hybrid depends on the MMI and the outgoing s-bends which cross each other to realize a optimal electrical layout. The embedding of additional devices like a 2x2 MMI would affect the reached signal uniformity [7]. The developed OEICs for at least 56 Gbaud/s data rates enable ultra-compact low-cost coherent receiver modules for 100 GbE applications and support even data rates up to 224 Gbit/s (DP-QPSK).

Acknowledgment

The authors gratefully acknowledge contributions from their colleagues A. Sigmund, W. Ebert, C. Sakkas, St. Schubert, and R. Steingrüber at the FhI Heinrich-Hertz-Institut, Berlin. Furthermore sharing of specifications and characterizations by u2t is highly recognized. This work was financed partly by the 100GET program of the German Federal Ministry of Education and Research, by the Spanish Ministerio de Ciencia e Innovacion under project ref. TSI-020400-2008-170, and supported by the 100GET/CELTIC project of the EC.

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NOVEL *InP*-BASED OPTICAL 45° HYBRID FOR DEMODULATING 8-ARY *DPSK* SIGNAL

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Abstract—**We proposed a novel optical 45° hybrid using a 2×8 multimode interference (MMI) coupler, three phase shifters and three 2×2 MMI couplers. Since optical demodulation is achieved by using the proposed 45° hybrid with only one delayed interferometer, the 8-ary differential phase shift keyed (DPSK) demodulator has much smaller device dimensions than conventional 8-ary DPSK demodulators consisting of four pairs of delayed interferometers and optical couplers. We fabricated the proposed 45° hybrid with an InP-based deep-ridge waveguide structure, and experimentally demonstrated the octagonal phase response with a relative phase deviation of <±5° over 32-nm-wide spectral range.**

Optical waveguide device, Multimode interference coupler, Optical hybrid device, Multilevel phase modulation, 8-ary DPSK demodulator

I. INTRODUCTION

Optical transmission systems using multilevel phase shift keyed (PSK) signal have several advantages over spectral efficiency. To date, from the viewpoint of simplicity of detection scheme and superiority of cost performance, direct detection techniques using differential phase shift keyed (DPSK) signal format have been reported [1]. In an effort to enhance spectral efficiency to be more than 1 bit/s/Hz, there have been many reports on differential quadrature phase shift keyed (DQPSK) signal format [2,3]. Recently, toward even higher spectral efficiency, multilevel phase modulation formats such as 8-ary DPSK [4], and 16-ary DPSK [5] have been investigated.

Here, we report an 8-ary DPSK (8-DPSK) demodulator scheme consisting of only one delayed Mach-Zehnder interferometer (DMZI) and a novel optical 45° hybrid that does not need any waveguide intersections for balanced detection. The proposed 8-DPSK demodulator scheme has a potential to make the receiver more compact and much easier to control the phase at the DMZI. As a preliminary study, we design and fabricate the optical 45° hybrid, and experimentally demonstrate octagonal phase response with a relative phase deviation ($\Delta\phi$) of <±5° for all output channels within 32-nm-wide spectral range.

II. DEVICE STRUCTURE

Figure 1 shows schematic diagram of 8-DPSK demodulators using four pairs of DMZIs and 180° hybrids based on a 2×2 optical coupler (a) and one pair of a DMZI and the proposed 45° hybrid (b). Usually, *M*-ary (M: multiplicity of phase modulation) DPSK signal is demodulated by using as many (*M*/2) DMZIs in parallel where each DMZI normally works at the required optical phase threshold [4]. Consequently, since the number of required DMZIs typically increases in proportion to *M*/2, the receiver becomes much larger in size and much complicated in stabilizing the phase at each DMZI [see Fig. 1(a)].

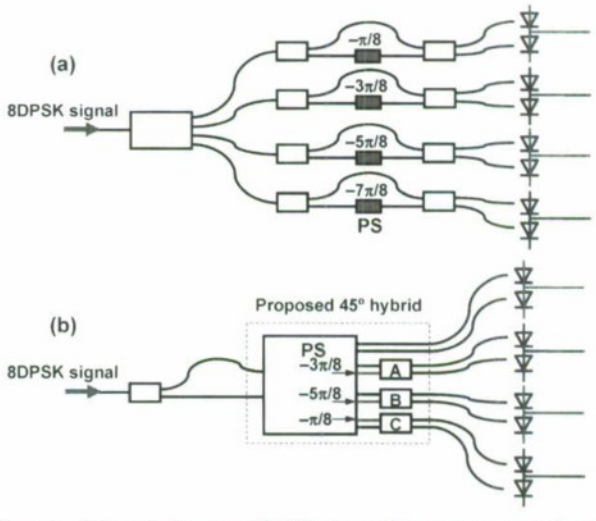

Figure 1. Schematic diagrams of 8-DPSK demodulators using a conventional scheme (a) the proposed scheme (b)

Meanwhile, as seen in Fig. 1(b), an 8-DPSK demodulator can be constructed with one pair of the DMZI and the proposed 45° hybrid. The proposed 45° hybrid is composed of three components; a paired interference (PI) based 2×8 multimode interference (MMI) coupler [6], three phase shifters (PS's) and three 2×2 MMI couplers where each coupling coefficient (κ) is set to be κ_A=0.5 for coupler A and κ_B=κ_C=0.85 both for couplers B and C.

When the 8-DPSK signal is incident on the proposed 45° hybrid, each of mutually adjacent four output pairs of the 2×8

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MMI coupler exhibit *In-phase* relation, because the 2×8 MMI coupler works as a 180° hybrid due to its centro-symmetric structure. Then only the phase relations at the output components coupled to the 2×2 MMI couplers A, B and C are rotated by 90°, 45° and 135° by means of the additional phase control at each phase shifters and the modal interference at each 2×2 MMI coupler, which makes the proposed device optical 45° hybrid. As shown in Fig. 1(b), the positions of the output channels with *In-phase* relation are mutually adjacent with each other, thus enabling to directly connect the 45° hybrid output channels to balanced photodiodes (PDs) without accompanying any waveguide intersections.

III. Simulation Results

Figure 2 shows the calculated transmission spectra of the proposed 45° hybrid as a function of the phase difference ($\Delta\theta$) between 8-DPSK signals (a) and the relative phase deviation from the octagonal phase relation ($\Delta\phi$) within C-band spectral range (b).

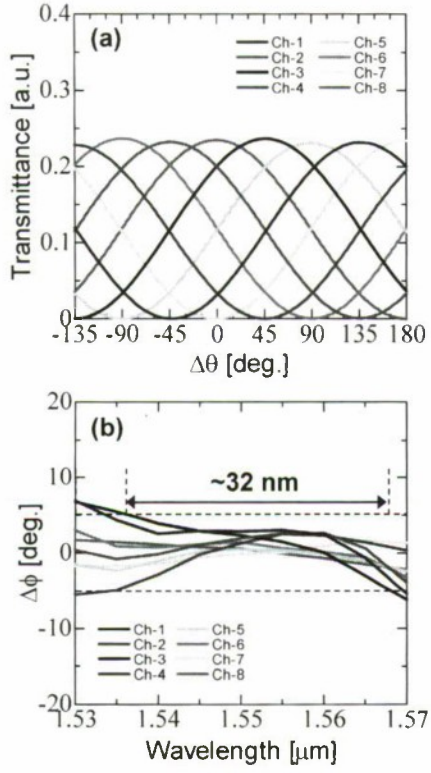

Figure 2. Calculated transmission spectra as a function of the phase difference between 8-DPSK signals ($\Delta\theta$) (a) and calculated phase deviation from the octagonal phase relation ($\Delta\phi$) (b) of the proposed 45° hybrid

In the calculation result by finite difference beam propagation method (FD-BPM), we assumed a lossless medium, a light wavelength of 1.55 μm, and a linearly polarized TE-mode. Also, the narrowest gap between the access waveguides was assumed to be 1.0 μm, and MMI coupling coefficients for three couplers were set to be κ_A=0.5 and κ_B=κ_C=0.85, respectively. Detailed coupler design can be found in Ref. [7]. It should be noted that in order to achieve octagonal phase behavior with a low excess loss and low phase deviation from perfect octagonal phase relation, it is prerequisite to make the phase matching between the 2×8 MMI coupler and three 2×2 MMI couplers. As a result of analytical calculation, we clarified that the excess loss and the phase deviation of the 8-DPSK signal can be minimized when the parameters for each phase shifter are set to be as shown in Fig. 1(b).

As seen in Fig. 2(a), each output transmittance of the proposed 45° hybrid shows octagonal phase response against $\Delta\phi$. In this case, π-phase differences are clearly shown in the output pairs of Ch-1 and 2, Ch-3 and 4, Ch-5 and 6, and Ch-7 and 8. Thus, we can directly connect the output waveguides to the balanced PDs without accompanying any waveguide intersections, as schematically shown in Fig. 1(b). Moreover, there is neither a considerable excess loss nor crosstalk at the output channels coupled to the 2×2 MMI couplers A, B and C, which is based on the phase matching by the phase shifters, thus enabling to preserve the detection efficiency for all output signal components. Furthermore, the octagonal phase relation of the proposed device can be obtained over the broad spectral range. As shown in Fig. 2(b), the available bandwidth of $|\Delta\phi|<5°$ was calculated to be ~32 nm.

IV. Exprimental Results

Based on the theoretical considerations, the proposed 8-DPSK demodulator scheme was fabricated on an InP wafer with a 0.3-μm-thick GaInAsP core layer (λ_g=1.3 μm). Using reactive ion etching technology, we formed deep-ridge waveguide with ~3.1 μm height. Subsequently, the InP substrate for the fabricated device was polished and cleaved. Finally, anti-reflection layers were coated at the input/output facets of the fabricated device. The waveguide parameters of the proposed 45° hybrid were set to be the same as those used in the calculations.

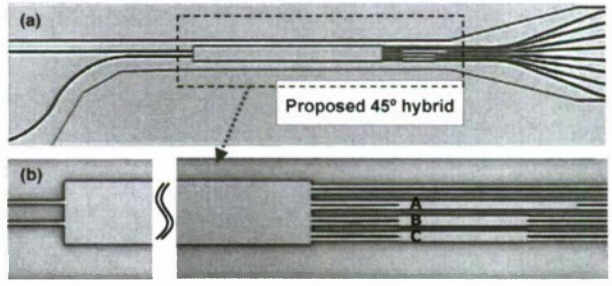

Figure 3. Top-views of the fabricated 8-DPSK demodulator scheme (a) and the proposed 45° hybrid (b)

Figure 3 shows the top-views of the fabricated 8-DPSK demodulator scheme (a) and the proposed 45° hybrid (b). As can be seen in Fig. 3(a), a DMZI is directly coupled to the 2×8 MMI coupler. A free-spectral range of the DMZI was designed to be ~520 GHz for convenience.

As seen in Fig. 3(b), the proposed 45° hybrid is composed of the PI-based 2×8 MMI coupler, three phase shifters and three 2×2 MMI couplers whose power coupling coefficient is κ_A=0.5 for coupler A and κ_B= κ_C=0.85 for couplers B and C. Also, the device length which is defined as the sum of the lengths of the 2×8 MMI coupler, the phase shifters and 2×2 MMI coupler is ~600 μm. The total chip size including fan-out regions for a fiber butt-coupling measurement was 2.2 × 0.32 mm^2.

To measure transmission spectra, we used an amplified spontaneous emission light of a semiconductor optical amplifier as a light source. The input polarization state was adjusted to be a linearly polarized TE-mode through a polarization controller. Figure 4 shows the measured transmission spectra of the fabricated 8-DPSK demodulator scheme when a CW light was incident on the device (a) and the experimentally estimated Δϕ for all output channels within the C-band spectral range (b).

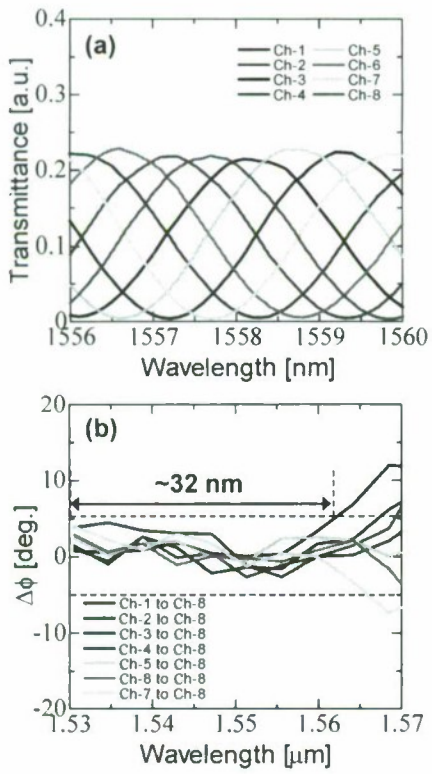

Figure 4. Measured transmission spectra of the fabricated 8-DPSK demodulator scheme (a) and the experimentally estimated phase deviation (Δϕ) for all output channels within the C-band spectral range (b).

As shown in Fig. 4(a), each output transmittance sinusoidally changed in accordance with the phase differences at the DMZI. That is, a wavelength change in Fig. 4(a) corresponds to Δ0 in Fig. 2(a). Consequently, the behavior of the measured transmittance for each output channel agrees well with that of the calculated one. Additionally, a wavelength dependent loss was measured to be <1.9dB within the C-band spectral range. Also, we were unable to observe a significant spectral asymmetry for all output channels, which originates from extremely low excess loss of the phase shifter (<0.1dB) and the 2×2 MMI coupler (<0.1dB).

As shown in Fig. 4(b), we verified that octagonal phase relation can be kept nearly constant over 32-nm-wide wavelength span, which qualitatively agrees well with the calculated result shown in Fig. 2(b).

V. Summary

We proposed, calculated and experimentally demonstrated the optical 45° hybrid consisting of a PI-based 2×8 MMI coupler, three phase shifters and three 2×2 MMI couplers. The proposed 45° hybrid has a potential to make the optical 8-DPSK demodulator scheme simpler and much easier to precisely control the phase in the device than conventional demodulator schemes. Octagonal phase behavior was numerically simulated by the FD-BPM. Based on the FD-BPM, we fabricated and characterized the proposed 45° hybrid with an InP-based deep-ridge waveguide structure. The device length was ~600 μm. The fabricated device exhibited clear octagonal phase response ($|\Delta\phi|<5°$) over 32-nm-wide spectral range.

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COMPACT *InP*-BASED 90° HYBRID USING A TAPERED 2×4 *MMI* AND A 2×2 *MMI* COUPLER

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Abstract—**We proposed a novel 90° hybrid using a paired-interference based linearly tapered 2×4 multimode interference (MMI) coupler and a 2×2 MMI coupler. We theoretically calculated and experimentally demonstrated that the proposed 90° hybrid has very short device length of ~227 μm and is never accompanied by any waveguide intersections for performing balanced detection. The proposed device exhibited quadrature phase response with a relative phase deviation of <±5° over C-band spectral range.**

Optical waveguide device, MMI coupler, optical hybrid device, QPSK demodulator, Coherent detection

I. INTRODUCTION

Recently, waveguide-based 90° hybrids based on 4×4 multimode interference (MMI) coupler and coherent detection schemes monolithically integrated with balanced photodiodes (PDs) have been reported [1-4]. Usually, a 4×4 MMI coupler inevitably requires waveguide crossings for balanced detection [2,4], which might cause excess losses and crosstalk at the cross junction area. In a previous work, to overcome this drawback, we developed the optical 90° hybrid consisting of a paired interference (PI) based 2×4 MMI coupler, a phase shifter and a 2×2 MMI coupler, and experimentally demonstrated quadrature phase response over a 94-nm-wide spectral range [5,6]. However, the length of the device reported in Refs. 5 and 6 were inherently larger than that of the 4×4 MMI coupler-based devices by a factor of ~1.3.

Here, we report a novel compact 90° hybrid without using an additional phase shifter. The proposed optical 90° hybrid is composed of a PI-based linearly tapered 2×4 MMI coupler and a 2×2 MMI coupler. Since the proposed device never requires any additional phase shifter to suppress crosstalk for the demodulated signal with a quadrature phase, the device becomes much simpler in design and more compact in size. We experimentally demonstrate quadrature phase behaviors with a low wavelength sensitive loss (<1dB), and a low phase deviation ($|\Delta\phi|$<5°) within C-band spectral range.

II. DEVICE STRUCTURE

Figure 1 shows schematic drawings of our previous 90° hybrid in Ref. 5 (a) and the proposed 90° hybrid (b). As seen in Fig. 1(a), the previous device absolutely needs an additional phase shifter to make the phase matching between the 2×4 MMI coupler and the 2×2 MMI coupler, thus enabling to minimize an excess loss and crosstalk for the signal with a quadrature phase. However, the previous device becomes inherently larger in size and somewhat complicated in design.

Meanwhile, as seen in Fig. 1(b), the proposed device consists of a linearly tapered 2×4 MMI coupler and a 2×2 MMI coupler. It should be noted that the linearly tapered 2×4 MMI coupler is based on the paired interference [7]. Noticeable difference of the proposed device to the previous device is the shape of the 2×4 MMI coupler and the absence of the phase shifter between the 2×4 MMI coupler and the 2×2 MMI coupler. Since the optical 90° hybrid inherently has the number of input channels less than that of output channels, the input MMI width (W_{MS}) can be narrower than the output MMI width (W_{MF}), thus enabling to form the linearly tapered MMI structure as schematically shown in Fig. 1(b).

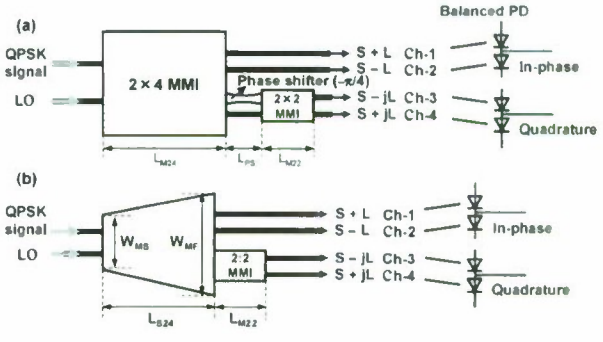

Figure 1. Schematic diagrams of the previous 90° hybrid in Ref. 5 (a) and the proposed 90° hybrid (b)

The operation principle of the devices shown in Fig. 1 is commonly explained as follows. When the quadrature phase shift keyed (QPSK) signal and the local oscillator (LO) light are incident on the devices, each of mutually adjacent two output pairs of the 2×4 MMI coupler exhibit *In-phase* relation, because the 2×4 MMI coupler works as a 180° hybrid. Then only the phase relation at the output components coupled to the 2×2 MMI coupler is rotated by 90° (*Quadrature* phase relation) through the modal interference at the 2×2 MMI coupler, which makes the device optical 90° hybrid.

Usually, the MMI length required for self-imaging can be reduced by using a tapered MMI structure [8]. Furthermore, it should be noted that the tapered shape of the 2×4 MMI coupler

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in Fig. 1(b) also contributes to the control of relative phase differences between the output channels of the 2×4 MMI coupler. Thus, when the taper angle of the 2×4 MMI coupler is optimized to provide a desired phase change, we can make the phase matching between the MMI couplers without using the phase shifter, which allows us to connect the linearly tapered 2×4 MMI coupler directly to the 2×2 MMI coupler, as schematically shown in Fig. 1(b). Therefore, compared with the previous device shown in Fig. 1(a), the proposed device can be more compact in size.

In both cases, the output phase relation of the optical 90° hybrids are given by S+L for Ch-1, S–L for Ch-2, S–jL for Ch-3 and S+jL for Ch-4, which enables us to directly connect the 90° hybrid output channels to balanced PDs without accompanying any waveguide intersections.

III. Theoretical Consideration

We numerically calculated an optimum length against the taper ratio (W_{MF}/W_{MS}) of the linearly tapered 2×4 MMI coupler. Then, we investigated the specific taper ratio that is able to omit the additional phase shifter in the optical 90° hybrid by providing an extra phase shift in the 2×4 MMI coupler.

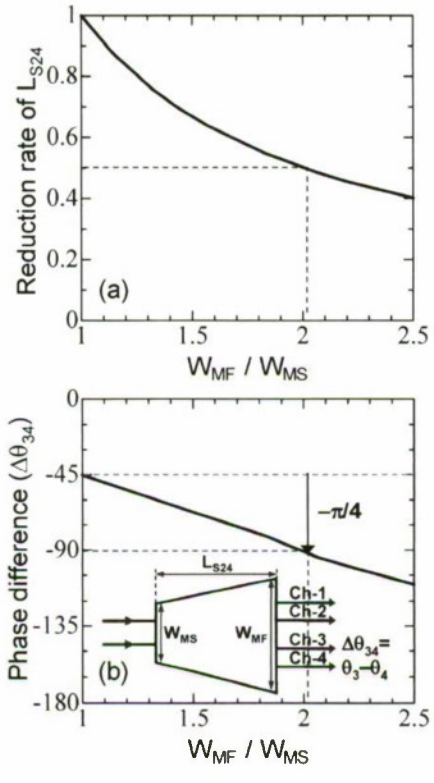

Figure 2. Calculated reduction rate of L_{S24} (a) and calculated phase difference between Ch-3 and Ch-4 ($\Delta\theta_{34}$) (b) of the linearly tapered 2×4 MMI coupler as a function of W_{MF}/W_{MS}

Figure 2 shows the calculated reduction rate of the MMI length (L_{S24}) required for 4-fold splitting (a) and the calculated phase difference between Ch-3 and Ch-4 ($\Delta\theta_{34}$) of the linearly tapered 2×4 MMI coupler (b). In Fig. 2(a), the rectangular-shaped 2×4 MMI coupler [5,6] corresponds to the case of W_{MF}/W_{MS}=1. As W_{MF}/W_{MS} increases for the fixed value of W_{MF}, the optimum L_{S24} tends to be reduced. On the other hand, in order to achieve the phase matching without using the phase shifter, $\Delta\theta_{34}$ should be $-\pi/2$ [rad.]. In this case, tapering the 2×4 MMI coupler is also responsible for the variation of $\Delta\theta_{34}$. As clearly seen in Fig. 2(b), when the value of W_{MF}/W_{MS} is set to 2.06, the extra phase change of $-\pi/4$ [rad.] is added between output Ch-3 and Ch-4 of the 2×4 MMI coupler, thus enabling to omit the phase shifter in the optical 90° hybrid as schematically shown in Fig 1(b).

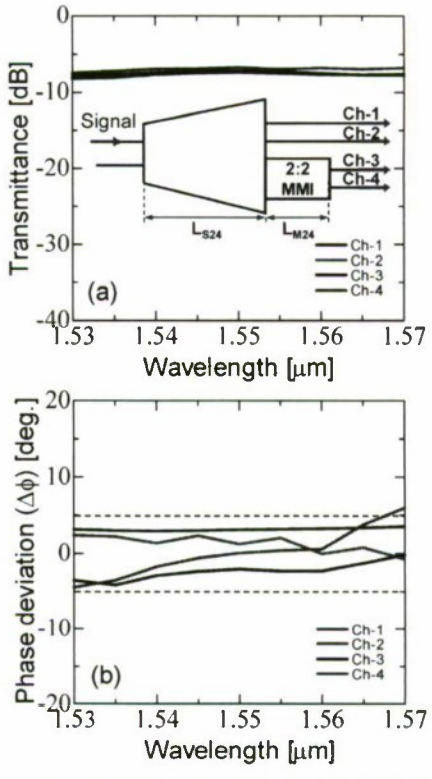

Figure 3. Calculated transmission spectra (a) and relative phase deviation ($\Delta\phi$) from the quadrature phase relation of the proposed device

Figure 3 shows the transmission spectra calculated by finite different beam propagation method (FD-BPM) when an optical signal is incident on one input port of the device (a) and the calculated phase deviation ($\Delta\phi$) from the perfect quadrature phase relation (b). In the FD-BPM simulation, we assumed an InP-based deep-ridge waveguide structure. W_{MF} was set to 18.6 μm. The narrowest gap between the output waveguide arrays (Gap) of the linearly tapered 2×4 MMI coupler was set to be 1.1 μm. As a result, W_{MS} was determined to 9.02 μm.

In order to satisfy the requirement of $\Delta\theta_{34}=-\pi/2$, L_{M24} and L_{M22} were optimized to be 116 μm and 111 μm, respectively. As can be seen in Fig. 3(a), the proposed device operates as a 4-fold power divider with an excess loss of <1.0dB. Also, as clearly seen in Fig. 3(b), the proposed device exhibits low phase deviation of $|\Delta\phi|<5°$ within the C-band spectral range, which means the proposed device works as a QPSK demodulator within 40-nm-wide wavelength span.

IV. Exprimental Results

The proposed device was fabricated on an InP wafer with a 0.3-μm-thick GaInAsP core layer (λ_g=1.3 μm). The device parameters were set to be the same as those used in the FD-BPM simulations. Figure 4 shows a top-view photograph of the proposed 90° hybrid. In this case, L_{Device} defined as the sum of L_{S24} (=116 μm) and L_{M22} (=111 μm) was 227 μm, which is ~40% shorter than the case of our previous device shown in Fig. 1(a).

Figure 4. Top-view photograph of the proposed 90° hybrid employing the linearly tapered 2×4 MMI coupler and the 2×2 MMI coupler

To experimentally evaluate the phase characteristics, we designed and fabricated a test structure in which a delayed Mach-Zehnder interferometer (DMZI) is directly coupled to the device. A free-spectral range of the DMZI was designed to be ~520 GHz for convenience. The total chip size including the DMZI and fan-out regions for a fiber butt-coupling measurement was 1.7 × 0.25 mm^2.

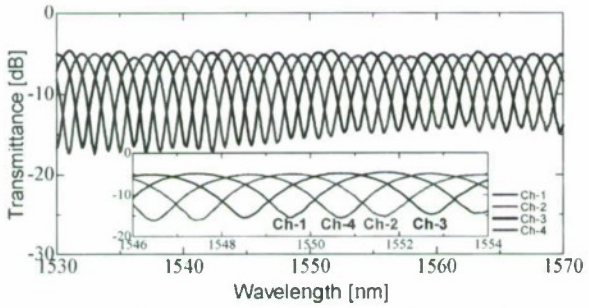

Figure 5. Measured transmission spectra of the fabricated device.

Figure 5 shows the measured transmission spectra when an optical signal (TE-mode) is incident on the DMZI integrated optical 90° hybrid. In Fig. 5, the spectra envelope corresponds to the amplitude response of the device. Similar to calculated result shown in Fig. 3(a), wavelength sensitivity was measured to be <1.0dB within the C-band spectral range. Also, as seen in the inset in Fig. 5, π-phase differences were clearly observed at the *In-phase* channels (Ch-1 and 2) and the *Quadrature* channels (Ch-3 and 4), which means that the balanced detection is never accompanied by any waveguide intersections.

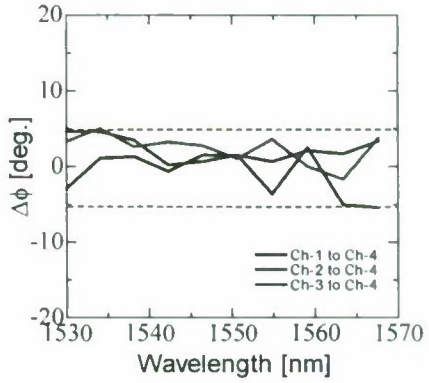

Figure 6. Experimentally estimated relative phase deviation ($\Delta\phi$) for the proposed device

Figure 6 shows the experimentally estimated relative phase deviation ($\Delta\phi$) of the proposed device. As seen in Fig. 6, $\Delta\phi$ was measured to be less than ±5° for each output channel within the C-band spectral range, which quantitatively agrees well with the calculation result shown in Fig. 3(b). .

V. Summary

We proposed a compact optical 90° hybrid using the linearly tapered 2×4 MMI coupler and the 2×4 MMI coupler, and discussed its potential for use in a coherent receiver monolithically integrated with balanced photodiodes. The proposed 90° hybrid was realized in the deep-ridge waveguide with a GaInAsP/InP material system. It has been theoretically and experimentally shown that the device length of the proposed device is ~40% shorter than that of our previous device. Furthermore, the fabricated device operated within the C-band spectral range.

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TM MODE WAVEGUIDE ISOLATOR MONOLITHICALLY INTEGRATED WITH InP ACTIVE DEVICES

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Abstract— We propose and design an integration of transverse magnetic mode waveguide optical isolator and active InP device. A semiconductor ring laser with integrated isolator is also proposed, fabricated and demonstrated. We observe the single direction continuous wave lasing.

I. INTRODUCTION

In order to avoid the optical noise reflection to semiconductor laser diodes (LDs) source or semiconductor optical amplifiers (SOAs) for stable operation, optical isolators are indispensable devices. Currently commercial isolators are, however, bulk components required collimating lenses, expensive alignment technologies when we package a laser diode. Therefore, monolithically integrated InP waveguide isolators are required for large-scale photonic integrated circuits (PICs) with numerous active devices, such as LDs and SOAs and passive optical components. For this purpose, various types of waveguide optical isolators have been proposed and developed [1-3]. Recently, we have successfully demonstrated the first monolithic integration of TE mode waveguide optical isolator with distributed feedback LDs (DFB-LDs) [4]. As a proof-of-concept, we propose and fabricate a TM mode isolator integrated with ring laser (SRL).

II. STRUCTURE OF INTEGRATED ISOLATOR

Figure 1 shows a proposed structure with integrated TM mode isolator and SOA sections. The TM-mode waveguide isolator is realized by using non-reciprocal loss mechanism. It consists of a ferromagnetic Fe/Ni layer in the upper cladding.

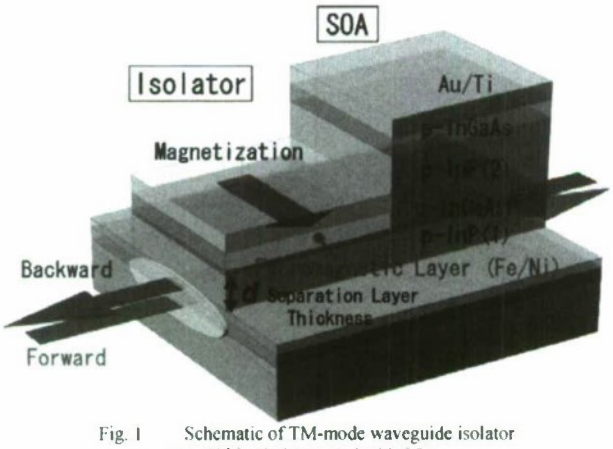

Fig. 1 Schematic of TM-mode waveguide isolator monolithically integrated with SOA.

When the ferromagnetic layer is magnetized perpendicular to the light propagation and parallel to the substrate, the propagation modes split vertically. As a result, backward-propagating light experiences larger loss compared with the forward-propagating light, thus nonreciprocal loss is induced. Under these conditions, the device can act as an optical isolator. The background loss is compensated for by injecting current to the active multiple quantum well (MQW) layer.

One important requirement to achieve sufficient nonreciprocal loss is that the separation distance between the core and Fe/Ni (d in Fig. 1) need to be less than500 nm, and is typically smaller than the thickness of conventional LDs' p-clad layer. Consequently, integration of isolator with conventional SOA requires 2 levels p-clad thickness layers on a substrate. On the other hand, there is a concern of undesirable light reflection and scattering at the boundary of the 2 level structures. We optimize the separation layer thickness by finite difference method simulation. In addition, in order to fabricate this 2 level structure, we introduce an embedded p-InGaAsP contact layer in the middle of p-InP layer as shown in Fig.1.

III. DESIGN AND SIMULATIONS OF INTEGRATED ISOLATOR

A. Nonreciprocal Loss Calculation

A large isolation ratio can be obtained at small cladding-layer thickness because a thin cladding layer easily lets light through into the ferromagnetic layer to produce a large magneto-optic interaction. Therefore, the cladding layer has to be thin as long as the amplifying gain of the SOA can compensate for the absorption loss of light in the ferromagnetic layer. Figure 2 shows the calculated optical losses for the 1550nm TM mode as a function of p-InP(1) thickness d. The nonreciprocal loss (isolation ratio) is difference between the optical absorption loss of forward propagation and the one of backward propagation. This simulation is based on the scalar wave equation including off-diagonal elements in the dielectric tensor of the ferromagnetic layer and calculated with two dimensional finite difference methods (FDM)[6]. Figure 2

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shows the nonreciprocal loss which reduces as the separation d increases because the interaction of ferromagnetic layer and light emission is small when d is large. On the other hand, when d is smaller than 200 nm, the optical loss of the isolator becomes also large. In this result, d estimates 200 to 400 nm to obtain sufficient nonreciprocal loss.

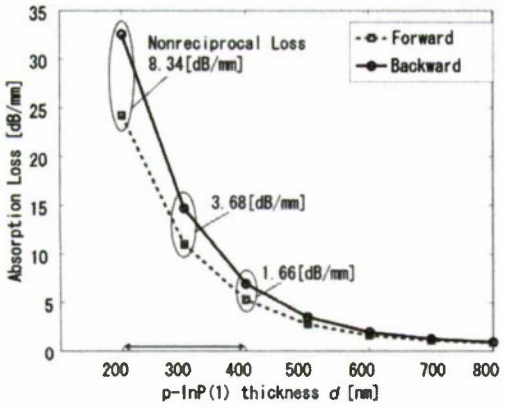

Fig.2 The simulated optical absorption loss for TM mode 1550nm of the isolator as a function of the thickness of p-InP(1) thickness d. In this simulation, the thickness of Ni and Fe is fixed to 20nm and 200nm, respectively.

B. Estimation of the Reflection and Scattering

The height difference of the 2 level p-cladding may occur undesirable light reflection and scattering. In order to estimate the reflection at the interface between SOA and isolator, we calculate the equivalent refractive indexes at SOA and isolator. The reflection is ignorable because they are almost same value. In order to estimate the scattering, we calculate the overlap integration of the mode distribution on the cross section at the isolator and SOA. In this simulation, the thickness of the p-cladding of SOA is fixed at 1450nm. The coupling efficiency η can be written as

$$\eta = \frac{\left| \iint \phi_{SOA}(x,y)\phi_{ISO}(x,y)dxdy \right|^2}{\iint \left|\phi_{SOA}(x,y)\right|dxdy \cdot \iint \left|\phi_{ISO}(x,y)\right|dxdy} \quad \cdots\cdots\cdots (3.1)$$

Figure 3 shows the calculated coupling ratio between SOA and isolator section as a function of separation d. The coupling efficiency converges to 100% as the separation d increases because isolator p-cladding profile becomes as the same as that of SOA. On the other hand, when d is smaller than 300 nm, the coupling efficiency is small. We, thus, choose d as 400nm to obtain sufficient nonreciprocal loss and high coupling ratio. The ferromagnetic layer (Ni/Fe) thickness is 20nm and 200nm [7].

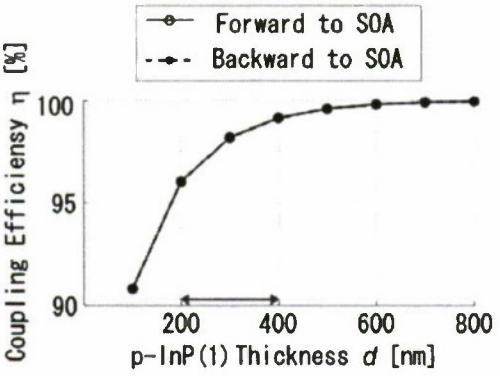

Fig.3 The calcurated mode coupling efficiency between isolator and SOA as a function of the thickness of the p-InP(1); d.

Table 1 The epitaxial layer structure in our TM mode SOA integrated with waveguide optical isolator.

Material	m	d_m (nm)
n-InP	1	-
bottom SCH	2	80
MQW	3	147
upper SCH	4	80
u-InP	5	30
u-InGaAsP	6	5
p-InP(1)	7	400
p+InGaAsP	8	50
p-InP(2)	9	800
p+InGaAs	10	200

The epitaxial layer profiles shows table 1.Diffrent from a conventional TM-mode isolator [7], a 50-nm-thick p-InGaAsP contact layer was embedded in the middle of p-InP upper cladding. Thickness of each layer shows as d_m.

IV. Fabrication of Integrated Isolator with SOA

We designed the embeded p-InGaAsP contact layer in the middle of p-InP layer and p-InP divided p-InP(1) and p-InP(2) as shown in table 1. After the reactive ion etching (RIE) for waveguide ridge structure, p-InGaAs and p-InP(2) only at the isolator section were etched. In this process, the advantage is no re-growth step requirement. We fabricated the TM mode SOA layer structure which includes isolator structure on an n-InP substrate by metal-organic vapor phase epitaxy (MOVPE). Figure 4 shows the fabrication chart. First, the ridge waveguide was formed by a standard photolithography and Cl_2/Ar reactive ion etching with SiO_2 mask. Second, SOA ridge structure was covered with photo resist to prevent followed wet etching. p+InGaAs and p-InP(2) only at the isolator section were etched with $H_2SO_4/H_2O_2/H_2O$ and HCl, respectively. The layer thickness difference can be created by this additional wet etching. Since it does not require re-growth step, the structure

is relatively fabricated easily without sacrificing the SOA performance. After that, a polyimide was spin coated and ashed to make SOA contact opening, and at only the isolator section, was partially ashed until the height of isolator surface with SiO2 mask pattern as in Fig. 4(2). Polyimide was employed for side wall passivation. Ferromagnetic Ni and Fe layers were deposited only in the isolator section with the electron-beam (EB) evaporator and their thickness were about 20nm and 200nm as mentioned above in Fig 4(4). Finally, a 100-nm-thick Ti layer and a 200-nm-thick Au layer were deposited to make top electrodes.

Figure 5 shows the scanning electron microscope (SEM) image at the intersection of both the SOA and isolator sections.

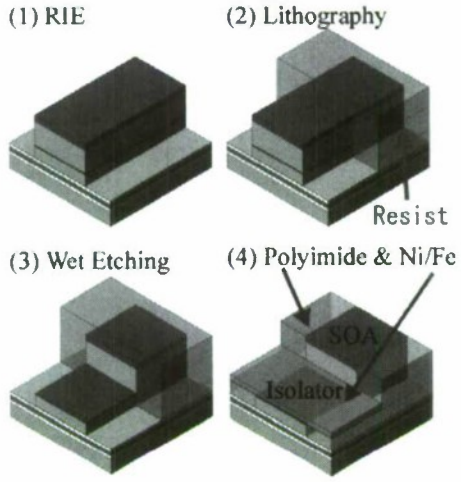

Fig.4 Fabrication images for creating 2 level p-cladding structure

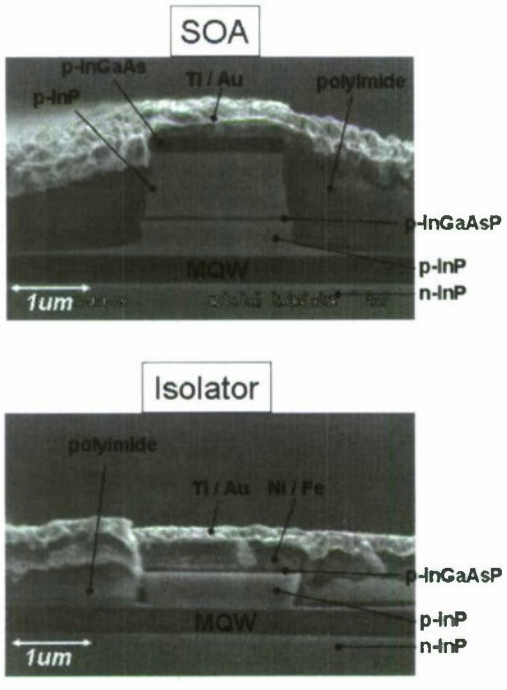

Fig.5 Cross sectional SEM image of the fabricated integrated device, SOA section and isorator section

V. Fabrication of Ring Laser with Isolator

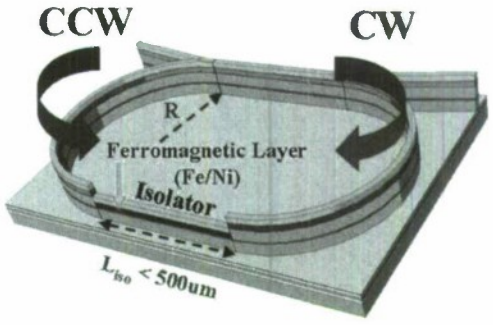

Fig.6 Schematic of TM-mode waveguide isolator monolithically integrated with SRL. Polyimide is hidden in this figure.

As a proof-of-concept, a TM-mode SRL with monolithically integrated isolator is fabricated using the fabrication method proposed above. SRL has a bistablity of the light oscillation direction. Integrated isolator brings the two different absorption loss including clockwise (CW), forward loss < counter clockwise (CCW), backward loss and suppress CCW oscillation, resulting in unidirectional operation. The relationship of the loss magnitude is defined with the external magnetic field direction and we can control the SRL oscillation direction with the magnetic field.

We prepare the device design below, ring radius is 300um and 500um, isolator length is 500um and Y-branch optical output and feedback to the cavity ratio is 50%:50%. Figure 7 shows an experimental setup for measuring the IL characteristics and spectrum. An external magnetic field of 0.15T was applied to the device by a permanent magnet. In

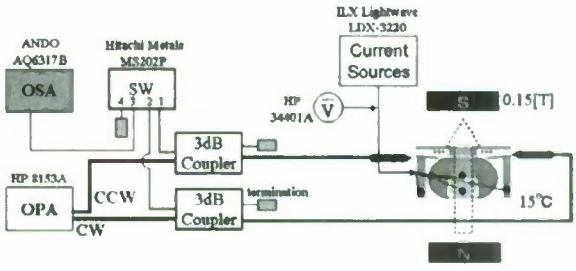

Fig. 7 Experimental setup for measuring the SRL integrated with waveguide optical isolator

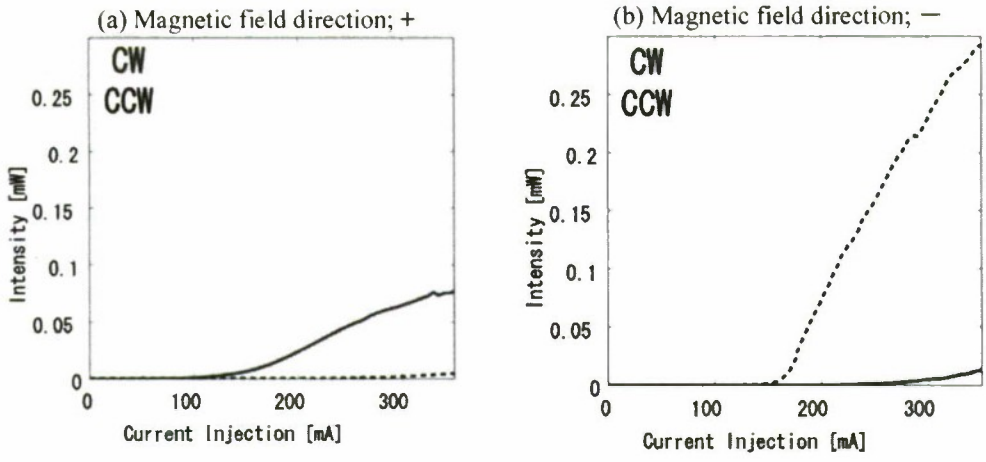

Fig. 8 IL characteristics of the integrated device with magnetic fields +0.15T and -0.15 T.

this experiment, we changed the direction (polarity) of the magnetic field. Figure 8 shows the IL characteristics of the fabricated SOA with integrated isolator output from clockwise (CW) and counter-clockwise (CCW) directions. A magnetic fields of ±0.15T is applied laterally during the measurement. The oscillation direction has a dependency of the external magnetic field direction and we observe that only one mode oscillation, corresponding to the smaller-loss direction in the waveguide isolator.

VI. Conclusion

We have proposed and demonstrated a simple structure to integrate TM-mode waveguide optical isolator with other InP active devices. By inserting a thin p-InGaAsP contact layer in the middle of p-InP upper cladding, the isolator section was integrated in a relatively simple fabrication process. As a proof-of-concept device, we have succeeded in fabricating a semiconductor ring laser with integrated isolator and demonstrated a preliminary unidirectional lasing characteristic for the first time. The proposed structure can be an effective method to control the direction of lasing mode in a micro-ring laser diode with external magnetic field direction.

Acknowledgement

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Advances in the growth of lattice-matched III-V compounds on Si for optoelectronics

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Abstract: The novel direct band gap, dilute nitride Ga(NAsP)-material system allows for the first time the monolithic integration of a III/V laser material lattice matched to Si substrate. This lattice-matched approach offers the possibility for a high-quality, low defect density integration of a III/V-laser material potentially leading to long-term stable laser devices on Si-substrate. The present paper introduces this novel integration approach and discuss the monolithically growth in line with optical properties of first laser devices grown on exactly oriented (001) Si substrates.

Introduction

The increasing miniaturisation of integrated circuits (IC) in line with the increased complexity of the chip design has been the driving force for improved micro-processor performance in the last decades. However, the shrinking IC architecture leads also inevitably to fundamental difficulties such as RC delays, signal latency and cross talk. One main challenge is the management of the heat dissipation caused by the increasing total electrical interconnection length. The application of optical interconnections and data processing could offer a solution to all these drawbacks. Therefore, Silicon Photonics has become the research focus for future optoelectronic integrated circuits (OEICs) and opens up a completely new field of device functionalities.

Optoelectronic IC building blocks such as modulators, detectors as well as light wave guides have been demonstrated with convincing performance in a down-scaleable process technology. However, a commercial solution for the monolithic integration of long term stable laser diodes has not been achieved yet, which is the key device component to finally realize OEICs and to fully profit from the concept of Silicon Photonics.

Silicon has an indirect electronic band gap and efficient light emission directly from Si has been found to be very difficult to achieve so far (1, 2, 3). However, the class of III/V compound semiconductors and related low-dimensional carrier systems is well established for optoelectronic applications particularly for laser diodes, because most of the III/V material systems reveal a direct band structure and efficient optical gain. Nevertheless, because of the large lattice mismatch between the standard III/V laser materials such as GaAs or InP to Si, the epitaxial deposition on Si substrates leads unavoidably to the formation of high densities of threading dislocations in the integrated III/V layer, preventing any long-term stable lasing operation of corresponding device structures (4).

A new approach, being introduced only very recently (5, 6) is the development of the novel III/V-dilute nitride Ga(NAsP), which reveals a direct electronic band gap and can be grown epitaxially lattice-matched to Si substrate avoiding any formation of misfit dislocations. Due to its direct band gap character this material can act as an efficient light emitter, modulator and/or detector. With the absence of any dislocation network, the main obstacle to finally realize a long-term stable laser diode monolithically integrated on Si is removed.

Result and Discussion:

The lattice constants and the corresponding band gaps of a variety of III/V-compound material systems are summarized in Fig.1. As can be clearly seen the standard direct

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band gap III/V-material such as GaAs, InP or GaN possess completely different lattice constants as the indirect semiconductor Si. GaP has a lattice-constant very similar to the one of Si, however, GaP has also an indirect band gap and therefore is a weak light emitter.

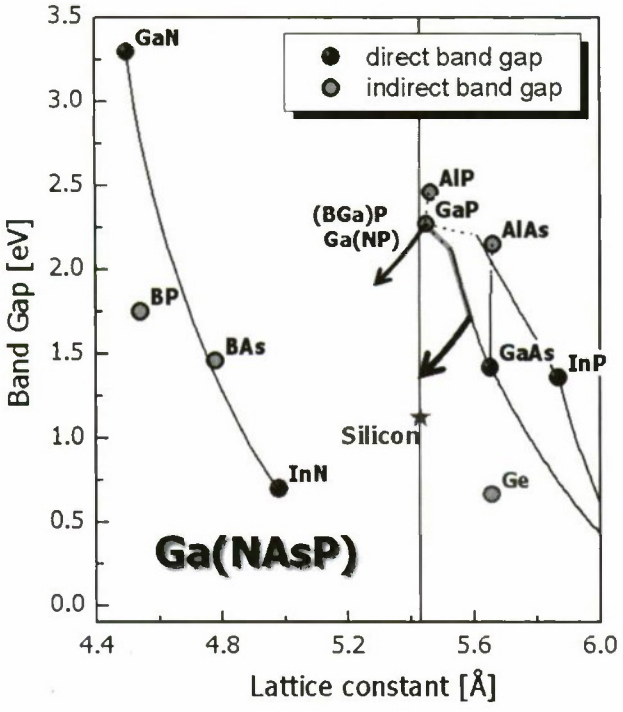

Figure 1: Energy band gap versus lattice constant for III/V-compound materials and Si

The novel GaP based dilute nitride Ga(NAsP) reveals a direct band gap due to the high As concentration of more than 75%. At the same time the lattice constant increases in relation to the one of Si with rising As content, but the incorporation of N simultaneously with As allows for a re-adjustment of the Ga(NAsP) lattice constant towards the one of Si. In addition, the presence of a few percent of N leads to a clear red-shift of the band gap due to a strong band anti-crossing coupling of the Ga(AsP)-Γ- and N-levels (7).

This lattice re-adjustment opens up the possibility of a defect-free integration scenario of a direct III/V semiconductor to Si substrate.

The epitaxial growth of the active material Ga(NAsP) on (001) Si requires the deposition of a defect-free GaP nucleation layer beforehand. In order to prevent any defect formation in this nucleation layer it is essential to guarantee charge neutrality along the III/V - Si interface and avoid unwanted cross-doping caused by atom diffusion into the respective heterolayers. In addition the exactly oriented (001) Si surface requires a specific preparation procedure to circumvent the formation of antiphase disorder in the GaP film (8). One has also to address the slightly different equilibrium lattice constants of GaP and Si, when aiming to grow films above the critical layer thickness by introducing either B or N into the III/V semiconductor to decrease its lattice constant.

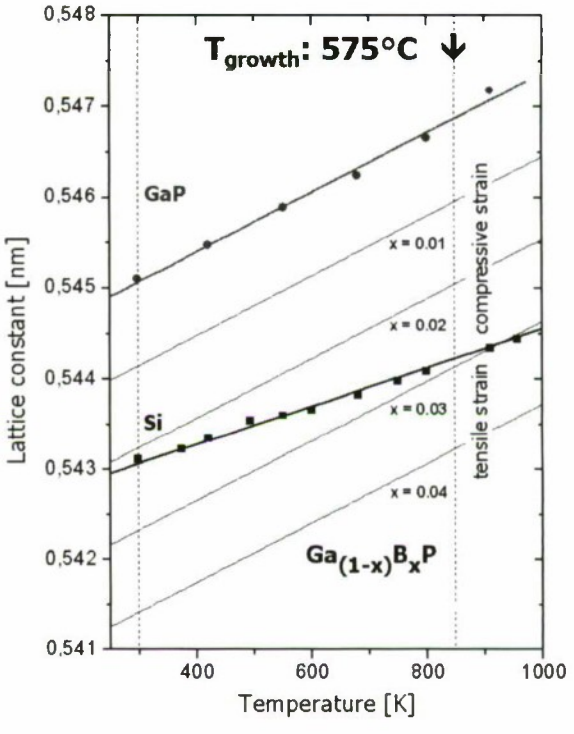

Figure 2: Lattice constant of GaP (red) and Si (black) as a function of temperature (9). Four additional thin lines represent the temperature dependence of (GaB)P with varying B concentrations, assuming the same thermal expansion coefficient as GaP.

The extent of lattice mismatch between the III/V crystal and the Si substrate significantly depends on temperature due to the differences in the thermal expansion coefficient of both classes of material

systems. This correlation beeomes obvious in Fig. 2, whcre thc temperature dependence of the lattiee eonstant of GaP and Si between room temperature and 1000 K is shown. In addition, also the temperature depcndence of the lattiee eonstant of the ternary eompound material (BGa)P is given for varying B concentrations. As misfit dislocations arc primarily nucleated during growth, it is crucial to adjust the lattice mismatch at growth temperature, which has been chosen to be 575 °C. On the other hand, if the integral strain of the entire III/V deviee structure becomes too high during cooling down, the III/V film will crack.

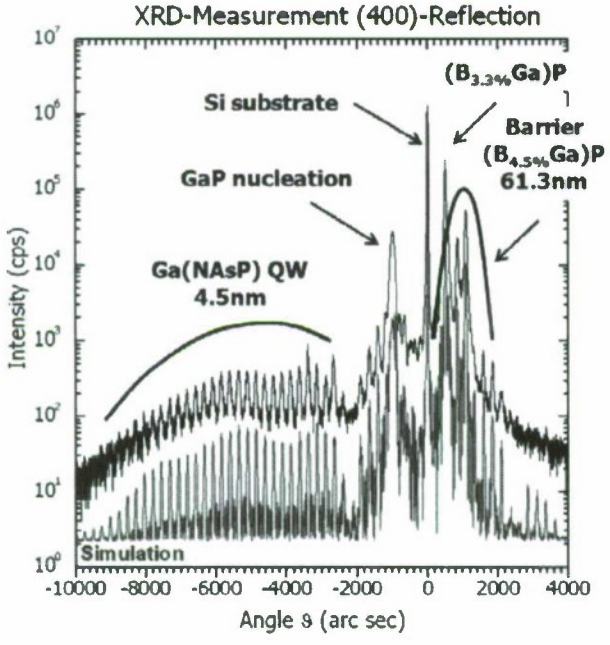

Figure 3: High-resolved XRD pattern of a 4-period Ga(NAsP)/(BGa)(AsP) MQWH inbetween (BGa)P SCH layers around the (400)-reflection of Si (upper trace-experimental, lower trace-modeling by dynamical X-ray diffraction theory). The theoretical trace has been shifted on the intensity scale for clarity.

The ineorporation of about 3% boron allows for the deposition of several micros thick (BGa)P layers on Si without craeking, which serve in the following as waveguide layers (SCH) in first laser struetures.
Compressively strained 4.5 nm thick Ga(NAsP) QWs were embedded in tensilely strained (BGa)(AsP) barrier material for strain compensation in order to grow 4-period Ga(NAsP)/(BGa)(AsP) multiple quantum well heterostructures (MQWH) on (001) Si substrates by metal organic vapour phase epitaxy (MOVPE). The epitaxial deposition is performed in a cluster consisting of a Si-vapour phase epitaxy (VPE) machine connected to a III/V-MOVPE system by a common glove box. In the Si-VPE-system the deoxidation of the chemically cleaned (001) Si-substrates, the epitaxial growth of the Si-buffer layer, the annealing step of the Si-buffer and the nucleation of thin GaP-layers takes plaee. After these proccss steps the wafer is transfered to the III/V-MOVPE-system for the overgrowth of the Ga(NAsP) based device structure. Due to the thermodynamieally metastable eharaeter of the quaternary III/V alloy system low-temperature MOVPE deposition conditions using temperatures around 575°C have beeu chosen. The effieiently decomposing MO-chemicals triethylboron (TEB), TEGa, 1,1-dimethyl-hydrazine (UDMHy), tertiarybutyl-arsine (TBAs) and tertiarybutylphosphine (TBP) have been used as preeursors for the differeut elements of the desired layer (9).
Struetural investigations have shown that a precise strain management at growth temperature allows for the epitaxial integration of these III/V multi layer stacks on Si without any indieation of misfit formation. The narrow line width of the X-ray diffraction (XRD) satellite refleetions in Fig. 3 is a clear indication for a high crystal quality and the presenee of abrupt interfaees in the MQW strueture.
Depending on the exaet composition and the quantum well width of the Ga(NAsP)/(BGa)(AsP)-MQWH system the optieal emission wavelength lies in the established data communication window in the range of 850nm to 950 nm at room temperature, as shown exemplarily for one MQWH grown lattice-matched on (001) Si substrate in Fig. 4.

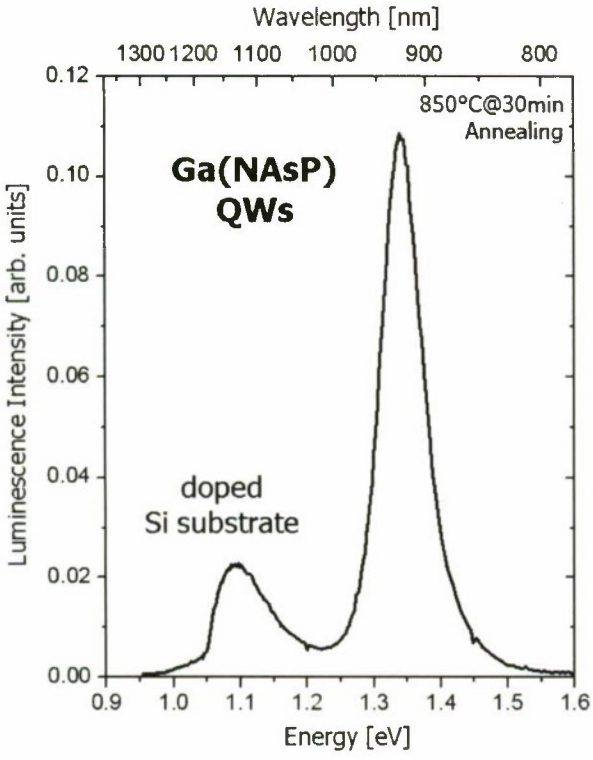

Figure 4: Photoluminescence spectra of a Ga(NAsP)/(BGa)(AsP)-MQWH system, excited at a wavelength of 514nm, grown on doped (001) Si substrate. A post-growth annealing of 30 min at 850°C has been applied to the sample.

The pronounced emission peak at 925 nm corresponds to the active III/V material Ga(NAsP) whereas the emission peak at longer wavelength belongs to the 525 µm thick doped Si substrate. In order to significantly improve the luminescence efficiency a post-growth annealing treatment has to be applied. This dependency on annealing is very typical for dilute nitrides (10).

At present detailed studies are underway to realize electrical injection lasers in this novel material system on Si-substrate by careful optimization of the MOVPE growth process, of the optoelectronic characteristics and the relevant technology steps for broad area as well as ridge waveguide laser devices. In addition, the concepts for a subsequent integration into the accepted CMOS-process flow, i.e. by appyling CMOS-compatible 300mm process tools are under development.

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Growth and characterization of TlInGaAsN/TlGaAsN triple quantum wells on GaAs substrates

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Abstract

TlInGaAsN/TlGaAsN triple quantum wells (TQWs) with different In and N eoneentration in the quantum wells (QWs) and barriers were grown by gas-souree moleeular beam epitaxy. The higher Tl ineorporation was obtained for the TlInGaAsN/TlGaAsN TQWs having higher N eoneentration in the QWs region. Temperature dependeneies of the photolumineseenee (PL) speetra for the TlInGaAsN /TlGaAsN TQWs with different Tl ineorporation in aetive region were eompared and studied. Reduetion in the temperature dependenee of the PL peak energy was observed by inereased Tl ineorporation in the aetive region.

I. Intoduction

Wavelength division multiplexing (WDM) technology is very important for optieal fiber eommunieation systems for increasing transport eapaeity and obtaining flexible network management. However, eommereially available InGaAsP/InP laser diodes (LDs) used in the WDM optieal fiber eommunication system show the lasing wavelength fluetuation with ambient temperature variation, mainly due to the temperature dependenee of the band-gap energy and refraetive index. Therefore, the LDs in the WDM system must be equipped with Peltier element to stabilize temperatures of the LDs. To solve this problem, we have proposed the TlInGaAsN quinary semieonduetor system as a promising eandidate for realizing the temperature-insensitive emission wavelength and threshold eurrent light sources operating in the wavelength range of 1.3–1.55 μm [1]. We have reported that the light emitting diodes of TlInGaAsN double quantum wells (DQWs) with TlGaAs barriers showed reduced temperature dependence of the eleetrolumineseenee wavelength [2]. In order to further deerease the temperature dependenee of the emission wavelength, it is required to inerease the incorporation of Tl into TlInGaAsN aetive layer. It is also necessary to extend emission wavelength up to 1.3 μm for optieal fiber eommunication system.

In this paper, we will investigate the influenee of In and N eoneentration in the QWs and barriers on the Tl ineorporation in the aetive region of the TlInGaAsN/TlGaAsN TQWs and the temperature dependence of their optieal properties.

II. Experiment

Figure 1 shows a sehematie illustration of sample struetures investigated in this study. The samples were grown on semi-insulating GaAs (001) substrates by gas-souree molecular-beam epitaxy. Elemental Tl (5N), In (7N) and Ga (7N) were used as group III sources, and thermally cracked AsH_3 and ion-removed eleetron eyelotron resonanee (ECR) plasma-assisted N_2 were used as group V sourees. Four types of TlInGaAsN TQWs samples A, B, C and D, were grown with different In and N eoncentration in the QWs and barriers. The growth conditions are shown in Table 1. The growth temperature for the QWs and barriers was 420°C. The buffer and eap GaAs layers were grown at 560°C. After growth, to improve the crystalline quality of the TlInGaAsN TQWs, rapid thermal annealing (RTA) for all the samples was earried out at 700°C for 1 min in N_2 ambient. In order to prevent the evaporation from the sample surface during RTA, elean GaAs wafer was plaeed faee to face on the sample. Photolumineseenee (PL) speetra were measured using a 488 nm line of an Ar-ion laser. Secondary ion mass speetroseopy (SIMS) was used to study the depth profile of Tl^{205} using oxygen as a

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primary ion. The structural properties were studied by high-resolution X-ray diffraction (HR-XRD, Cu Kα, 45KeV, 40mA, X'pert PRO, Netherlands) and cross-sectional transmission electron microscopy (TEM, JEM-3000F, 300kV, JEOL, Japan).

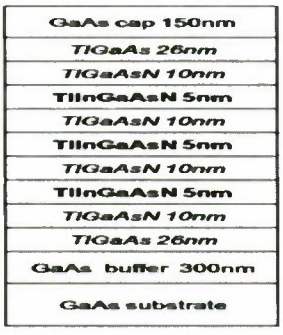

Fig. 1 Schematic illustration of TlInGaAsN/TlGaAsN TQWs sample structure.

Table. 1 Growth conditions for each samples

Sample No.	In cell temp.	ECR plasma power (QW/barrier)
A	730°C	7W/3W
B	735°C	7W/3W
C	730°C	7W/7W
D	730°C	10W/3W

III. Results and discussion

HR-XRD (004) ω-2θ scan curves for the samples A, B, C and D after RTA at 700°C for 1 min are shown in Fig. 2. The HR-XRD curves show well-defined satellite diffraction peaks that imply good periodicity of the entire TQWs region. The presence of Pendellösung fringes in all of the curves indicates the smooth interface and high uniformity of the films. These indicate that there is no obvious difference in the structural properties of these four samples.

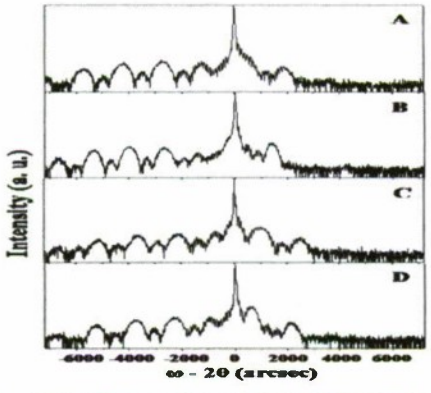

Fig. 2 XRD (004) ω-2θ scan curves for samples A, B, C and D after RTA at 700°C for 1 min.

Figure 3 shows the SIMS depth profiles of Tl^{205} around active regions in these samples. Sample B has the smallest Tl incorporation in the active region among four samples. This can be understood that under higher In flux, Tl incorporation is limited by the competition between Tl and In. Compared with the sample A, the sample C has slightly increased Tl incorporation, suggesting more Tl-N bond in the barriers which is caused by higher N flux during barrier layer growth. The sample D has the highest Tl incorporation among four samples. This indicates that Tl incorporation in the active region increased more by higher N concentration in the QWs than in the barriers.

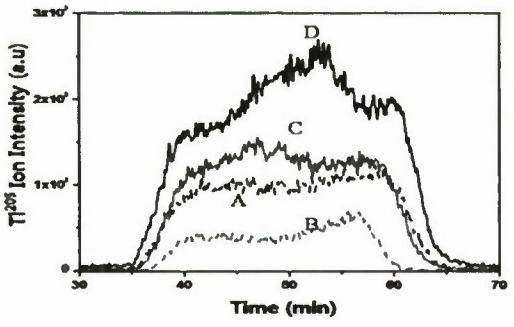

Fig. 3 SIMS depth profiles of Tl^{205} around active region for samples A, B, C and D.

Figure 4 shows room temperature (RT) PL spectra for four samples with different In and N concentrations in the QWs and barriers. RT PL peaks are located in the wavelength range from 1230 to 1300 nm. The PL wavelength at RT of sample D is extended up to 1.3 μm. Therefore, it appears advantageous to increase N concentration in the QWs, instead of increasing the N composition in the barrier layer, for extending the wavelength above 1.3 μm. The inset of Fig. 4 shows the 10 K PL spectra for the samples C and D. Compare with sample D, the PL intensity of sample C is weaker. This indicates that the optical properties of TlInGaAsN TQWs are degraded with increasing N concentration in barrier layers than in QWs. This can be understood that the high strain at the compressive/tensile strained interface will be accumulated with increasing N concentration in barrier layers in sample C, even overall strain is reduced.

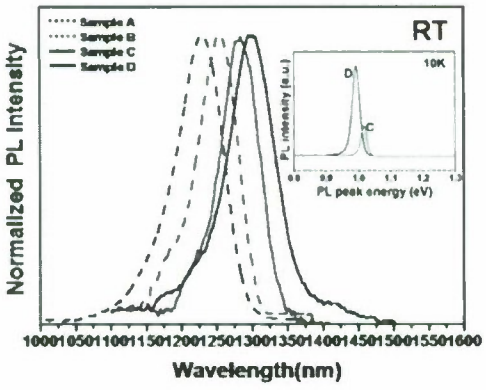

Fig. 4 Normalized RT PL spectra for samples A, B, C and D. The inset shows the PL spectra for samples C and D at 10K.

It can be well substantiated that the optical properties of QW structures are associated with their structural qualities [3-4]. However, there is a significant difference in the PL intensities between sample C and D, even though no obvious difference in the structural properties could be found in the HR-XRD data. To further clarify the effect of barrier layer N composition on the structural properties of the QW samples, (110) cross-sectional dark field (DF) TEM measurements were carried out. Fig. 5 shows the (110) cross-sectional DF TEM images obtained with diffraction vector g = (002), which is sensitive to the composition of crystals for the zinc-blende structure [5]. Fig. 5(a) reveals that the sample C has composition modulation and surface roughness at the interface between the upper side of 1st and 2nd QW layer and barrier layer. This indicates that the structural quality of TlInGaAsN TQWs at the interface dramatically deteriorated due to the high strain at the QW/barrier interface with increasing N concentration. On the contrary, the DF X-TEM image for the sample D (Fig. 5(b)) reveals perfectly two-dimensional TQWs structure without obvious surface roughness and composition modulation. These results indicate that the increase of N concentration in the barrier layers more leads to deteriorate the structural quality as compared with increased N concentration in the QW layer. DF X-TEM images in Fig. 5 show the difference of structural properties between sample C and D, which is in agreement with the PL result in Fig. 3.

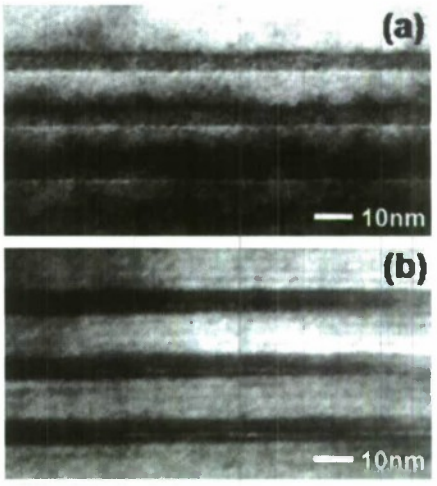

Fig. 5 (110) dark field X-TEM images obtained with diffraction vector g = (002) for the samples (a) C and (b) D.

The temperature dependence of the PL peak energy is shown in Fig. 6 for the samples C and D. The temperature dependence of PL peak energy of sample D was observed to be 0.28 meV/K, while that of the sample C was 0.30 meV/K. The reduction of the temperature dependence of the PL peak energy can be attributed to the increased Tl incorporation in the active region as shown in Fig. 3.

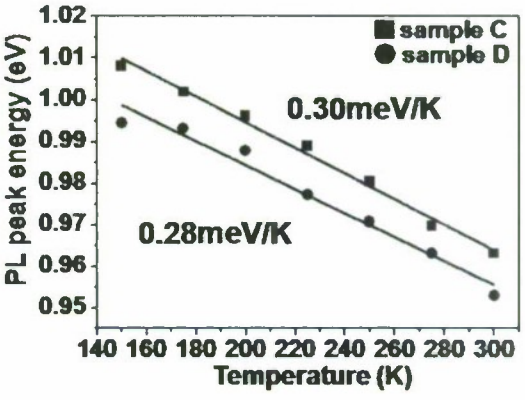

Fig. 6 Temperature dependencies of PL spectra for samples C and D.

IV. Summary

In summary, optical and structural properties for the TlInGaAsN/TlGaAsN TQWs grown by gas-source MBE with different In and N concentrations in the QWs and barriers were investigated. The TlInGaAsN TQWs sample with higher N concentration in the QWs showed increased Tl incorporation in active region and longer PL peak

wavelength. Degraded optical properties for the sample having higher N concentration in the barriers could be explained by the existing composition modulations and interface roughness. Reduced temperature dependency of 0.28 meV/K was obtained for the TlInGaAsN TQWs sample with higher N concentration in the QWs. These results are very important to realize the temperature stable wavelength TlInGaAsN/AlGaAs LDs.

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Semi-Insulating Iron-Doped InP Buffer Layers for Al-Free GaInP/GaInAs pHEMTs

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Abstract

InP buffer layers for Al-free HEMT applications were deposited by metal-organic vapor-phase epitaxy (MOVPE) on semi-insulating InP substrates. The challenge posed by the production of insulating buffers on InP substrates is a well-known problem. Different growth conditions were chosen to achieve highly insulating layers. Our experiments show that regardless of growth conditions, impurities arising from reactor parts and from the starting substrate lead to an *n*-type background doping decreasing exponentially from 1×10^{17} at the substrate to 4×10^{14} cm^{-3} for sufficiently thick layers. Highly resistive buffer layers could only be obtained doping InP with iron at a concentration of 6×10^{16} cm^{-3}. Consequently, the sheet resistance of InP could be increased from R_S = 3000 Ω/□ for undoped layers to $R_S = 9.4\times10^7$ Ω/□, resulting in InP buffer layers that are suitable for high-speed HEMTs. Non-optimized Al-free GaInP/GaInAs pHEMTs with a T-gate footprint of 100 nm achieved a cutoff frequency of $f_T = f_{MAX} \sim 250$ GHz, with a channel mobility and electron density of 10,000 cm^2/Vs and 10^{12} cm^{-2}, respectively.

I. Introduction

InP-based high electron mobility transistors (HEMTs) have recently achieved cutoff frequencies of $f_T = 628$ and $f_{MAX} = 331$ GHz [1]. Such very high cutoff frequencies make InP-HEMTs attractive for a variety of digital and millimeter-wave applications. Unfortunately, the AlInAs alloy commonly used in buffer and barrier layers is known to affect the long term reliability and stability of devices [2], [3], [4]. When this material is deposited by metal-organic vapor-phase epitaxy (MOVPE), the residual oxygen in the Al source trimethylaluminium incorporates into the crystal during growth, producing deep-levels defects. Even in molecular beam epitaxy (MBE), deep level traps have been reported at the AlInAs/GaInAs interface [5]. Such deep level defects trap electrons at low frequencies, leading to a number of transistor non-idealities. Although a passivation layer on top of the AlInAs barrier may offer some protection against oxidation, it also adds additional capacitance near the T-gate electrode. In any case, not all the AlInAs surfaces can be protected and adequately passivated by a deposited dielectric film.

The above arguments render Al-free HEMTs attractive from different viewpoints. InP is the only Al-free material for the buffer layer that can be grown lattice-matched, with a wide enough band gap, and a relatively large conduction band offset to the GaInAs channel. The use of GaInP as a strained barrier layer offers an even higher conduction band offset. Beside an improved device reliability and noise performance, InP provides also a higher thermal conductivity buffer which is advantageous in high-power dissipation applications by allowing lower junction temperatures. As a drawback, however, it is difficult to achieve highly-resistive undoped InP layers on SI InP and a poor device isolation is often observed.

In the present work, we clarify the mechanisms responsible for the low resistivity of undoped InP layers on SI InP. Capacitance-voltage (*C-V*) measurements and secondary ion mass spectroscopy (SIMS) indicate that *n*-type impurities incorporate into the InP buffer when growth is initiated. These impurities come from substrate fabrication (and/or from its packaging) as well as from reactor parts, and they are always detected near the substrate. The impurities make it practically impossible to achieve insulating InP buffer layers without introducing Fe-doping. We show that the reason for this can be understood by considering the band diagram profile in undoped InP buffer layers. Doping InP with Fe at a concentration of 6×10^{16} cm^{-3} increased the InP buffer sheet resistance from R_S = 3,000 to $R_S = 9.4\times10^7$ Ω/□. Such layers are suitable for HEMT fabrication, as demonstrated by the realization of Al-Free GaInP/GaInAs 100 nm gate HEMTs with cutoff frequencies of $f_T = f_{MAX} \sim 250$ GHz based on a still

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non-optimized channel structure featuring a mobility of 10,000 cm^2/Vs and a channel sheet density of 10^{12} cm^{-2}.

II. Experimental Procedure

The growths were performed in an horizontal MOVPE reactor at a temperature of $T_g = 630°C$ (660°C), under a 12 l/min flow of H_2 carrier gas at a total pressure of 160 mbar. All growths were performed on 2-inch (100) semi-insulating (SI) InP substrates. The group-III precursors were trimethylindium (TMIn) and trimethylgallium (TMGa). The group-V sources were arsine (AsH_3) and phosphine (PH_3). The impurity sources were silane (SiH_4) and ferrocene (Cp_2Fe).

The Al-free HEMT structure considered in this work consists of a 980 nm thick buffer layer (the first 320 nm of which are doped with Fe), a 17 nm $Ga_{0.36}In_{0.64}As$ channel, a 3 nm $In_{0.8}Ga_{0.2}P$ barrier, a 1.5 nm $In_{0.8}Ga_{0.2}P$:Si donor layer, a spacer layer of 6.5 nm $In_{0.8}Ga_{0.2}P$ and a 10 nm thick $In_{0.53}Ga_{0.47}As$:Si cap layer. The InP free-carrier concentration and the impurity density were determined by *C-V* measurements and SIMS, respectively. The sheet resistance of the buffer layer was measured through resistance measurements between pads evaporated on top of 50×50 μm^2 mesa structures, separated by 10 µm. To insure current flowing through the buffer layer, the surrounding area was etched approximately 50-100 nm into the InP.

For HEMT fabrication, Ge/Au/Ni/Au metal layers were deposited and rapid thermal annealed to form the source and drain contacts. Mesa isolation was obtained by etching the GaInAs contact layer and the GaInP barrier layer in H_3PO_4:H_2O_2:H_2O and H_3PO_4:HCl:H_2O solutions, respectively. Gate recess was carried out with succinic acid resulting in a total recess width of 220 nm. The gates were written by electron beam lithography (EBL) and centered into 2 µm source drain spacings. The HEMTs T-gate length at the foot gate was 100 nm. The gates were passivated with 75 nm of SiN_x at 120°C followed by a Ti/Au overlay metallization. Finally, 2.5 µm of gold were electroplated onto the device pads.

III. Results

Fig. 1 shows the Polaron *C-V* electron concentration versus the depth for undoped InP bulk material deposited under different conditions in order to gain insight on the origin of the impurities present at the buffer/substrate interface. The 1.5 µm thick InP buffer layers a) and c) were grown at $T_g = 630°C$, while layer b) at $T_g = 660°C$. The growth process previous to that for sample a) and b) consisted of 400 nm n.i.d. InP capped by a 10 nm GaInAs doped heavily with Si at $n = 2\times10^{19}$ cm^{-3}. The 1 µm thick buffer layer c) was deposited one day later directly on top of buffer layer b), after re-heating the substrate under PH_3 flow. The reactor was kept locked between the two growths to avoid external contamination. The electron concentration exhibits a peak at the interface between the buffer layer and the substrate, and rapidly decreases in the growth direction stabilizing at a level of $n = 4\times10^{14}$ cm^{-3}.

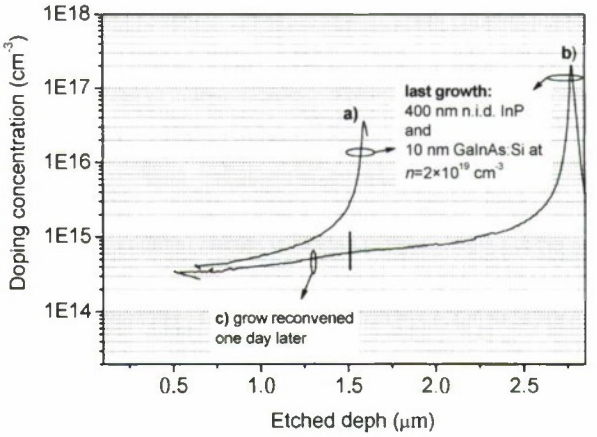

Fig. 1 Electron concentration versus depth as measured by Polaron *C-V* profiling.

SIMS measurements revealed a [Si] concentration peak at the interface with the buffer layer, as shown in Fig. 2 in the particular case of a HEMT structure with a Fe-doped InP buffer layer. Other workers also reported [Si] and [S] concentrations greater than 1×10^{15} cm^{-3} near the SI InP substrate, probably coming from the substrate fabrication and/or from the package [6], [7]. Part of the impurities at the buffer/substrate interface comes thus from the substrate.

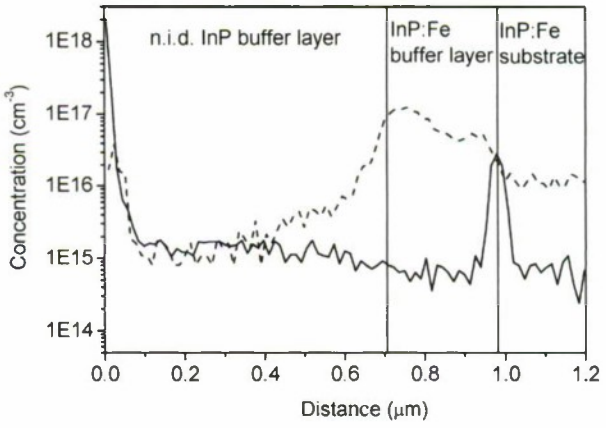

Fig. 2 SIMS concentration profiles for Fe (dashed) and Si (solid) for the HEMT structure. The vertical lines separate the 320 nm thick Fe-doped InP buffer layer from the undoped InP and the substrate.

However, the free electron concentration tail in the undoped InP buffer layer (Fig. 1) is much longer than in the [Si] SIMS profile, indicating that other impurities are also incorporated during the InP buffer layer growth. This suggests the mechanism leading to the residual doping in the InP buffer

involves impurities outgassing from the surfaces in the growth chamber, followed by their re-incorporation in the growing layers. Because outgassing increases at higher temperatures, one might expect the effect to be more pronounced at higher growth temperatures. Indeed, this idea is supported by the fact that the peak doping concentration of sample b) grown at a temperature of $T_g = 660°C$ is approximately one order of magnitude larger compared to sample a) deposited at 630°C. Because both growths had the same initial conditions (i.e. reactor coatings), the higher peak doping density can be attributed to stronger outgassing at the higher reactor temperature. Furthermore, it can be excluded that TMIn and PH_3 are the sources of contamination, since at a buffer layer thickness of 1.5 µm the residual background doping is only $n = 4\times10^{14}$ cm^{-3}. No doping peak concentration was observed at the interface between sample b) and c), since sample c) was not deposited directly on a new substrate surface. Therefore, the undoped InP of sample b) was sufficiently thick to coat the reactor parts avoiding impurity desorption during the growth of sample c).

While a thick InP layer represents an option to prevent the incorporation of dopants in subsequent epitaxial layers, the buffer layer is still useless for HEMT fabrication, because the contaminated buffer layer in the proximity of the substrate interface is still conductive. In fact, all the undoped InP buffer layers grown showed a sheet resistance $R_S < 3000\ \Omega/\square$.

To effectively suppress free carriers in the buffer, ferrocene was used to dope InP with Fe at 6×10^{16} cm^{-3}. Fe produces a mid-gap deep acceptor level 0.63 eV below the conduction band, which consequently reduces the free carrier density. Sheet resistances of $R_S > 1\times10^{8}\ \Omega/\square$ could be achieved.

However, Fe doped InP can only be an option for HEMT buffer layers if its memory effect does not impact mobility and sheet carrier density in the GaInAs channel. As shown in Fig. 2, the Fe concentration in InP shows a tail extending over 300 nm into InP after ferrocene was used to dope the first 320 nm of buffer layer. The broad shoulder is a consequence of the memory effect: Fe outgassing from the reactor parts incorporates into the layers after the ferrocene source is closed, as discussed above for the n-type dopants. To minimize the Fe concentration (memory effect) in the GaInAs channel, an additional 660 nm of undoped InP was deposited on top of the 320 nm Fe-doped buffer layer. A residual Fe concentration of 1×10^{15} cm^{-3} was still detected near the channel layer. However, the channel mobility and sheet carrier density were not affected by this amount of Fe, achieving still 10,000 cm^2/Vs and 10^{12} cm^{-2}, respectively. The sheet resistance of the 980 nm thick InP buffer layer, the first 320 nm of which were Fe-doped, was $R_S = 9.4\times10^{7}\ \Omega/\square$.

In order to gain a better understanding of the influence of Fe doping on electron density profile throughout the buffer layers, we performed numerical simulations of the HEMT band diagram for different impurity profiles. Fig. 3 shows this for the HEMT structure described above. In the growth direction, an exponentially decreasing *n*-type impurity concentration was chosen so that the simulated electron density approaches the carrier concentration extracted from sample a) in Fig. 1. This simulation should represent the conditions for the HEMT provided with an undoped InP buffer layer. The electron density decreases from the substrate in growth direction, and achieves a concentration of $n = 2\times10^{14}$ cm^{-3} at a distance of 150 nm from the surface. The conduction band (CB) shows a valley at the interface with the substrate, and is 0.1 eV above the Fermi level.

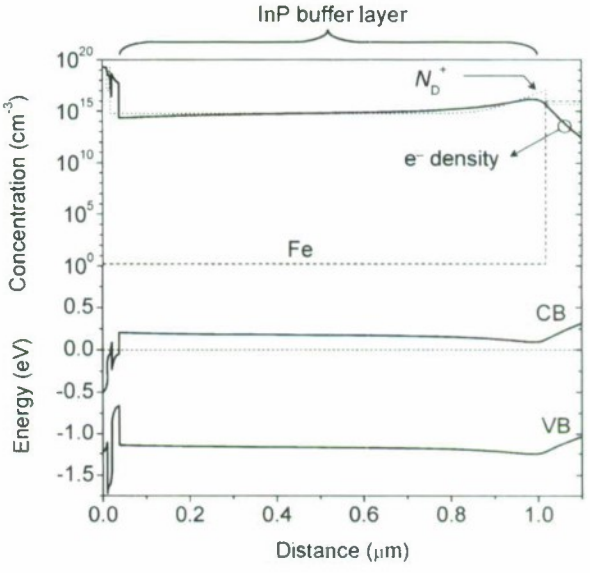

Fig. 3 Simulated conduction band (CB), valence band (CV) and electron density profiles (dotted line) in equilibrium. The n-type doping profile shown for sample a) in Fig. 1 without Fe doping was used in the calculation.

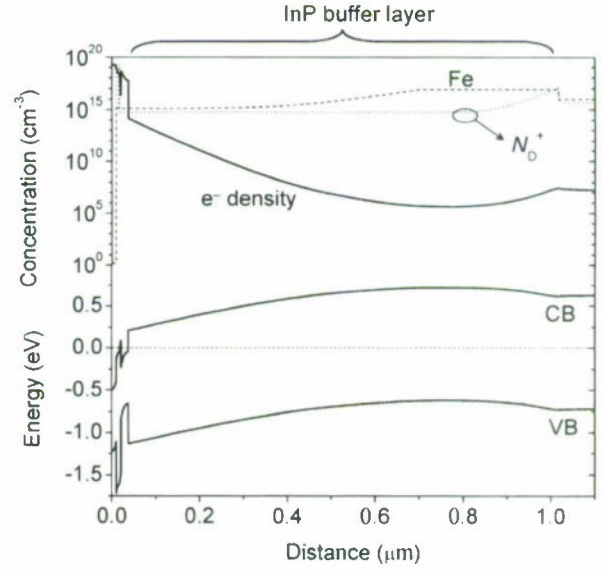

Fig. 4 Simulation of the conduction band (CB), valence band (CV) and electron density (dotted line) in equilibrium. An n-type impurity profile as that in Fig. 3, a Fe doping concentration in the first 320 nm and a Fe density tail (as shown in Fig. 2) were included for simulation.

Fig. 4 shows the band diagram and electron density for the same HEMT layer, with the single difference being the introduction of a 320 nm Fe-doped buffer directly on the SI InP substrate. The Fe profile includes the tail shown in Fig. 2. The electron density at the interface with the substrate is drastically reduced from $n = 1.5 \times 10^{16}$ cm^{-3} to $n = 1.8 \times 10^{7}$ cm^{-3} when Fe is added to InP. The electron density exhibits a minimum of $n = 4.2 \times 10^{5}$ cm^{-3} at 235 nm from the substrate, before it increases to $n = 1.5 \times 10^{14}$ cm^{-3} at the channel interface. The CB shows a convex shape with peak energy of 0.72 eV above the Fermi level. The decrease of the CB towards the GaInAs channel introduces an electric field, which confines electrons towards the channel. Interestingly, Fig. 3 and Fig. 4 show that the channel CB and electron density are not affected by the presence of Fe in the buffer layer.

Finally, the HEMT structure grown on the Fe doped InP buffer layer was processed as described in the previous section and characterized. Despite still non-optimized channel and barrier thicknesses, cutoff frequencies of $f_T = f_{MAX} \sim 250$ GHz were measured on T-gate devices with a 100 nm footprint, clearly establishing the suitability of Fe-doped InP buffer layers for Al-free pHEMTs.

IV. Conclusions

We studied the realization of highly insulating InP buffer layers for the fabrication of Al-free HEMTs. First growths showed InP buffer layers with an overall n-type doping concentration of up to 3×10^{17} cm^{-3} at the substrate interface, decreasing exponentially to reach 4×10^{14} cm^{-3} at an InP thickness of 1.5 µm. All undoped buffer layers showed sheet resistances of $R_S = 3000$ Ω/□ or less.

The origin of the n-type impurities was first investigated through *C-V* measurements and SIMS. It was shown that a source of contamination originates from reactor parts upstream with respect to the wafer. At reactor temperatures of $T_g = 630$°C, the impurities desorb into the gas phase and subsequently incorporate into the crystal, producing the *n*-type doping and leading to conductive InP buffer layers. In addition, the SI substrates also show contamination near the surface, which probably comes from fabrication and/or from the wafer packaging.

Only the incorporation of Fe at a concentration of 6×10^{16} cm^{-3} into InP could produce highly-insulating buffer layers with sheet resistances of $R_S = 9.4 \times 10^{7}$ Ω/□. However, after depositing 320 nm of InP on SI substrates, an additional 660 nm of InP had to be grown in order to reduce the Fe level in the GaInAs channel to a density of 1×10^{15} cm^{-3}. Despite this residual Fe level, mobilities and sheet carrier concentrations of 10,000 cm^2/Vs and 1×10^{12} cm^{-2} could be achieved.

Numerical calculations of the equilibrium band diagram for HEMTs grown on undoped InP buffer layers show a concave CB profile, which leads to a low-resistivity buffer layer. As Fe was introduced in the buffer layer near the substrate, the CB profile becomes convex, raising the CB edge by ~0.5 eV, and building an effective barrier layer for electrons. The processed HEMT devices with a T-gate footprint of 100 nm exhibited a cutoff frequency of $f_T = f_{MAX} \sim 250$ GHz. These results and the simulations showed that the Fe doping does not have a negative impact on device performance, although considerations of Fig. 4 shows that there is still some room for optimization in the buffer layer growth.

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HIGH-ELECTRON-MOBILITY $In_{0.53}Ga_{0.47}As/In_{0.8}Ga_{0.2}As$ COMPOSITE-CHANNEL MODULATION-DOPED STRUCTURES GROWN BY METAL-ORGANIC VAPOR-PHASE EPITAXY

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Abstract

Metal-organic vapor-phase epitaxy (MOVPE) growth of In-rich $In_xGa_{1-x}As$ on InP was investigated as a way to obtain extremely high electron mobility in modulation-doped (MD) structures. High-quality $In_{0.53}Ga_{0.47}As/In_{0.8}Ga_{0.2}As$ composite-channel (CC) MD structures were successfully grown without significant lowering of growth temperature. The room-temperature electron mobility in the CC MD reached 150,000 cm^2/Vs at the sheet carrier concentration (Ns) of $2.1x10^{12}$ cm^{-2}, which is one of the highest ever reported in MOVPE-grown InP-based InGaAs/InAlAs MD structures.

I. Introduction

Millimeter-wave frequencies of over 100 GHz are attracting much interest for use in many technical fields, such as broadband wireless communications and security. The excellent characteristics of InP-based high electron mobility transistors (HEMTs) have been demonstrated in these applications [1]. Further improvement of the high-frequency characteristics of HEMTs is required in order to advance the operation frequencies of applications toward the terahertz range. One of the basic approaches to boosting the speed of HEMTs is to enhance the electron mobility by increasing the In content in the channel layer. The use of pseudomorphic InGaAs/InAs composite-channel (CC) modulation-doped (MD) structures has demonstrated high electron mobility, where InAs has been used as a subwell layer [2]. Extremely high electron mobility of over 18,000 cm^2/Vs has been also reported by using an InGaAs/InAs CC structure at room temperature [3]. In those reports, the epitaxial layers were grown by molecular beam epitaxy (MBE). The low growth temperature in the MBE process is quite beneficial for the suppression of dislocation generation and lattice relaxation during strained-InAs growth. In contrast, metal-organic vapor-phase epitaxy (MOVPE) growth of InP-based HEMTs usually requires much higher growth temperature than MBE for precursor decomposition and the suppression of impurity incorporation. The higher growth temperature of MOVPE is not suitable for the growth of InGaAs/InAs CC MD structures because it tends to enhance three-dimensional InAs growth and affect electron-transport characteristics in the CC MD structures.

In order to obtain extremely-high-electron-mobility CC MD structures by using MOVPE at conventional high growth temperature, we investigated the potential of In-rich $In_xGa_{1-x}As$ as a subwell in CC. From the comparison of surface morphologies of In-rich $In_xGa_{1-x}As$, we chose 5-nm-thick $In_{0.8}Ga_{0.2}As$ as a subwell. The quality of epitaxial layer structures and electrical properties of $In_{0.53}Ga_{0.47}As/In_{0.8}Ga_{0.2}As$ CC MD structures were investigated. In the study of the spacer thickness dependence of mobility and sheet carrier concentration (Ns) of the CC MD structures, a room-temperature high electron mobility of 15,000 cm^2/Vs was successfully obtained at a Ns of $2.1x10^{12}$ cm^{-2}. To our knowledge, this mobility is one of the highest ever reported in MOVPE-grown InP-based InGaAs/InAlAs MD structures.

II. Experiment

CC MD structures were grown on 3-inch semi-insulating InP (001) substrates in a low-pressure horizontal flow reactor. Precursors were triethylgallium (TEG), trimethylindium (TMI), trimethylaluminum (TMA) for the group-III elements, arsine (AsH_3) and phosphine (PH_3) for the group-V elements, and disilane (Si_2H_6) for Si dopant. The growth temperature of samples was the same as that for our conventional lattice-matched (LM) InP-based HEMT wafers. Sample CC MD structures consisted of a LM InAlAs buffer, LM-InGaAs/$In_xGa_{1-x}As$ (subwell)/LM-InGaAs CC, LM InAlAs spacer and barrier, InP wet-etching stopper, and n^+-InGaAs contact layer. Delta-doped Si was inserted between the spacer and barrier. The surface morphologies of samples were evaluated by using Nomarski optical microscopy and atomic force microscopy (AFM). X-ray diffraction (XRD) and cross-sectional transmission electron microscopy (TEM) were also used for structural characterization. The van der Pauw method was used to measure the electron mobility and Ns at room temperature. In order to measure the Ns and electron mobility in CC, the contact layer of samples was selectively removed by wet etching before measurements [4].

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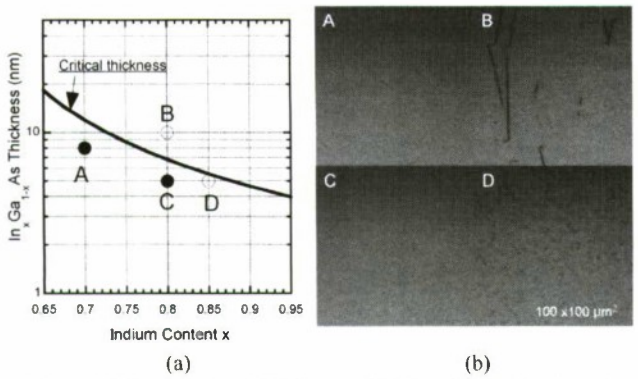

(a) (b)

Fig. 1. (a) In content and thickness of $In_xGa_{1-x}As$ samples A to D. (b) Nomarski optical micrographs of the samples.

III. Results and Discussion

A. Optimization of In content and thickness of $In_xGa_{1-x}As$

We observed the surface morphologies of several $In_xGa_{1-x}As$ samples with different In content and layer thickness in order to clarify the practical limit of In content and thickness of $In_xGa_{1-x}As$ subwell at our typical growth temperature for InP-based MD structures. Figure 1 summarizes the relationship among the In content, layer thickness, and surface morphologies of $In_xGa_{1-x}As$ samples. The samples were grown on LM InGaAs/InAlAs layers. In Fig. 1(a), the solid line is the calculated critical thickness of $In_xGa_{1-x}As$ on InP (001) using Matthews's model [5]. The position of open and filled circles denotes the In content and thickness of samples A to D. Fig. 1 (b) shows Nomarski optical micrographs of the samples. Smooth surfaces were obtained in samples A and C, where the layer thicknesses of the samples were below the critical thickness. As the layer thickness exceeded the critical thickness, a cross-hatched morphology appeared as seen in sample B. As the In content increased over 0.8, the growth mode of $In_xGa_{1-x}As$ layer seemed to change to three-dimensional. The surface morphology of sample D in Fig. 1(b) shows the formation of surface defects due to three-dimensional growth.

To obtain extremely high electron mobility in MD structures, the In content of the $In_xGa_{1-x}As$ subwell should be as high as possible. However, if the In content and layer thickness of the subwell are too close to their limits, the wafer quality will be easily affected by their fluctuations in run-to-run growth. Considering the results in Fig. 1, we chose 5-nm-thick $In_{0.8}Ga_{0.2}As$ for the subwell. To enhance electron confinement in the subwell, the subwell was sandwiched by LM $In_{0.53}Ga_{0.47}As$ layers in the CC MD structures. The total CC thickness was chosen as 9 nm, which is smaller than that of our conventional InP-based HEMTs [6] and should be favorable for the enhancement of the high-speed characteristics of the HEMTs. Figure 2 shows a typical AFM image of as-grown 5-nm-thick $In_{0.8}Ga_{0.2}As$ corresponding to the top of the subwell layer. The monolayer steps and wide atomic terraces indicate the excellent smoothness of the heterointerfaces between the LM InGaAs and $In_{0.8}Ga_{0.2}As$ subwell.

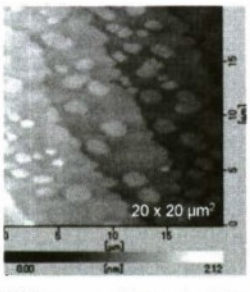

Fig. 2. Typical AFM image of 5-nm-thick $In_{0.8}Ga_{0.2}As$.

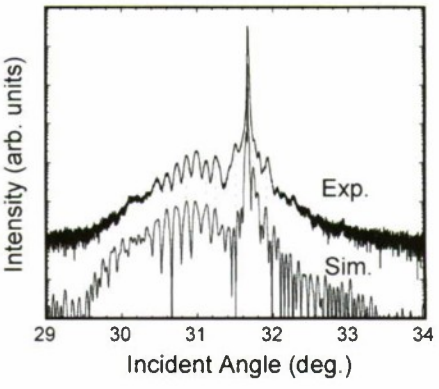

Fig. 3. Experimental and simulated XRD pattern of LM-InGaAs/$In_{0.8}Ga_{0.2}As$ CC MD structure.

B. Structural characterization of CC MD structures

Figure 3 shows typical experimental and simulated (004) XRD patterns for a LM-InGaAs/$In_{0.8}Ga_{0.2}As$ CC MD structure. The peaks in the low-angle region are due to the diffraction from the $In_{0.8}Ga_{0.2}As$ subwell and In-rich InGaAs contact layer. The pronounced Pendellösung fringes indicate the excellent abruptness and smoothness of the heterointerfaces. The experimental pattern agrees well with the simulation and indicates the precise control of the composition and layer thicknesses of the samples.

The layer structures were also examined by cross-sectional TEM. Figure 4 shows a typical TEM image

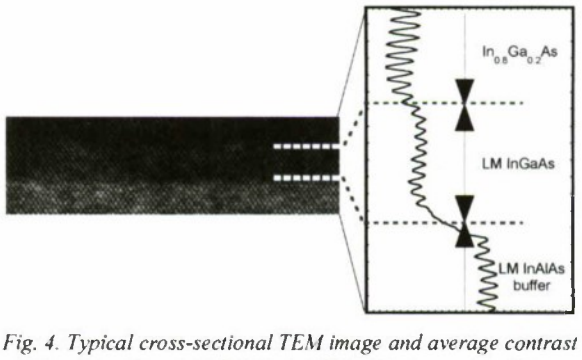

Fig. 4. Typical cross-sectional TEM image and average contrast profile of $In_{0.8}Ga_{0.2}As$/LM InGaAs/LM InAlAs heterointerfaces.

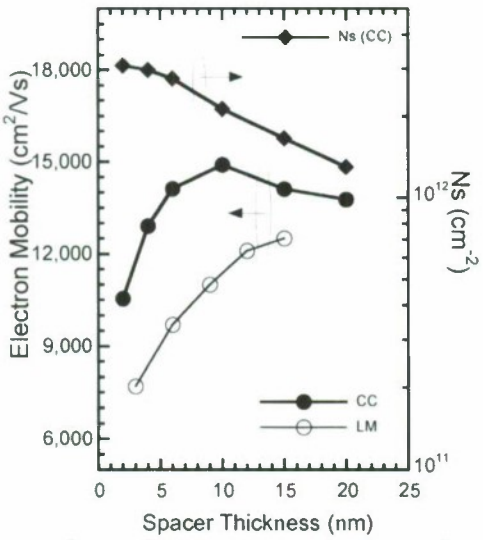

Fig. 5. Spacer thickness dependence of mobility and Ns in MD structures.

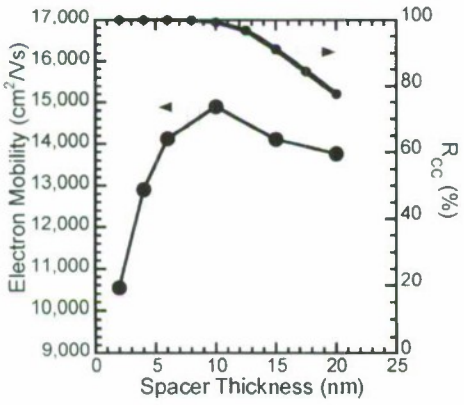

Fig. 6. Spacer thickness dependence of mobility and calculated relative electron concentration in CC (R_{cc}).

and average contrast profile of $In_{0.8}Ga_{0.2}As$/LM InGaAs/LM InAlAs heterointerfaces in a CC MD structure. The $In_{0.8}Ga_{0.2}As$ layer is observed as the darkest contrast region in the image. The abrupt heterointerfaces are clearly observed in both the TEM image and the contrast profile. This is consistent with the XRD results in Fig. 3.

C. Mobility in LM-InGaAs/$In_{0.8}Ga_{0.2}As$ CC MD structures

Figure 5 shows the spacer-thickness (t_s) dependence of mobility and Ns of LM-InGaAs/$In_{0.8}Ga_{0.2}As$ CC MD structures. Here, the delta-doping concentrations were the same among the samples. The LM-InAlAs barrier thicknesses of the samples were 15 nm. The t_s dependence of mobility in our conventional LM-channel MD structures is also shown for comparison. The higher In content of 0.8 in the CC MD structures provided much higher electron mobility than that in our conventional LM-channel MD structures. The mobility increased significantly as the t_s increased from 2 to 6 nm. Such behavior has also been reported in the literature [7]. The

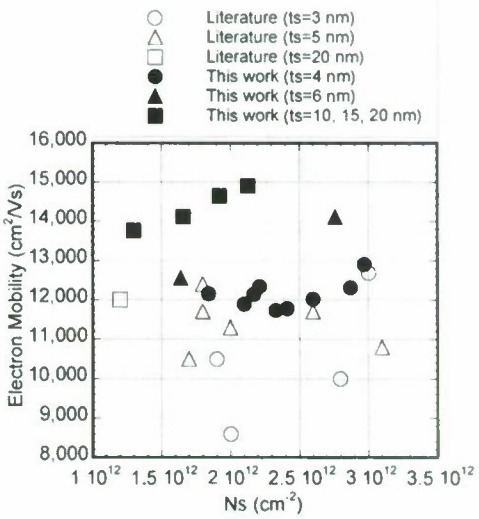

Fig. 7. Ns vs. mobility of MOVPE-grown InP-based MD structures.

increase in mobility indicates that the interaction between channel electrons and remote impurities is significantly suppressed as t_s increases from 2 to 6 nm. The monotonic decrease in Ns with increasing t_s can be explained by the change of conduction-band configuration with t_s.

The maximum mobility of 15,000 cm^2/Vs was obtained at the t_s of 10 nm. A further increase of t_s decreased mobility. The saturation and reduction of the mobility with t_s increase over 10 nm has also been reported in the literature [8, 9]. In the case of Fig. 5, one of the causes of the mobility reduction is the enhancement of parallel conduction in the delta-doped InAlAs barrier/spacer region. We estimated the electron concentration in both the CC and the barrier/spacer region of our MD structures using numerical calculation software [10]. In the calculation, the delta-doping concentration between barrier and spacer was chosen to simulate the experimental Ns obtained at the t_s of 2 to 6 nm. Figure 6 shows the t_s dependence of the experimental mobility and the calculated relative electron concentration in CC compared to the total electron concentration in the MD structures (R_{cc}). The R_{cc} is 100% below the t_s of 10 nm, which means that the carrier-supply barrier/spacer region is completely depleted. The R_{cc} decreases when the spacer thickness is over 10 nm. This indicates that the accumulation of electrons in the barrier/spacer region would become significant as t_s exceeds 10 nm, then cause the parallel conduction and affect electron mobility in CC.

We also examined the dependences of mobility and Ns on other structural parameters, such as delta-doping concentrations and total barrier thickness. Figure 7 summarizes the Ns and mobility of MOVPE-grown InP-based MD structures obtained in this work and in the literature [11-20]. The data in the literature were obtained for both LM and pseudomorphic channel structures with different spacer/barrier thickness. In almost the whole Ns range, higher

mobility was obtained in our CC MD structures. To our knowledge, the mobility of 15,000 cm^2/Vs is one of the highest ever reported in MOVPE-grown InP-based MD structures. It should be noted that we obtained high mobility of around 12,000 cm^2/Vs in the Ns range of 2 to $3x10^{12}$ cm^{-2} using our CC MD structures consisting of a comparatively thinner 4-nm spacer and 5- to 6-nm LM-InAlAs barrier. The layer structure should be favorable for practical high-speed InP-based HEMTs and enable us to boost the operation speed of HEMTs toward the terahertz range.

IV. Conclusion

The LM-InGaAs/$In_{0.8}Ga_{0.2}As$ CC MD structures were grown by MOVPE. High-quality CC MD structures were successfully obtained without lowering the growth temperature. The samples exhibited high electron mobility, which reached 15,000 cm^2/Vs at the Ns of $2.1x10^{12}$ cm^{-2}, one of the highest ever reported in MOVPE-grown InP-based MD structures. Such structures are eminently suitable for practical ultra-high-speed transistors operating in the terahertz range.

Acknowledgement

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High doping effects on *in-situ* Ohmic contacts to n-InAs

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ABSTRACT

We present the effect of active carrier concentration on the specific contact resistivity (ρ_c) of *in-situ* molybdenum (Mo) Ohmic contacts to *n*-type InAs. It is observed that, although the Fermi level pins in the conduction band for InAs, the contact resistivity decreases with the increase in InAs active carrier concentration. The lowest ρ_c obtained through transmission line model measurements was $(0.6 \pm 0.4) \times 10^{-8}$ Ω-cm^2 for samples with 8.2×10^{19} cm^{-3} active carrier concentration. The contacts were found to remain stable on annealing at 250 °C for 1 hour.

I. INTRODUCTION

Ultra-low resistance metal-semiconductor contacts are fundamental to the continued scaling of transistors towards THz bandwidths. Geometric scaling laws show that doubling transistor bandwidths requires a four-fold reduction in specific contact resistivity (ρ_c) (1, 2). $\rho_c < 1 \times 10^{-8}$ Ω-cm^2 is necessary in III-V HBTs and FETs for having simultaneous 1.5 THz f_t and f_{max} (1, 2). Moreover, high temperature operation and high current densities in modern electronic devices require the contact to be thermally stable (3).

Fabrication of Ohmic contacts using ex-situ techniques requires a significant attention to removal of semiconductor oxides and contaminants (4). Obtaining repeatable contacts through *ex-situ* techniques requires good process control; ρ_c can be highly sensitive to surface preparation and to the time interval between the surface preparation and contact metal deposition. Contacts formed through *in-situ* techniques are repeatable and result in ultra-low contact resistivities (5). *In-situ* technique involves contact metal deposition immediately after semiconductor growth without exposing the semiconductor surface to air preventing surface contamination and oxidation.

Apart from surface preparation, the interface conduction band barrier potential, determined either by Fermi level pinning or by work functions, also plays a crucial role in determining the contact resistance. For InAs, the Fermi level is pinned in the conduction band (6, 7, 8) which makes it a potential candidate to be used as the contact layer for metal-semiconductor contacts. *Ex-situ*, annealed, contacts to InAs with 2×10^{19} cm^{-3} active carrier concentration have shown to result in $\rho_c = 2 \times 10^{-8}$ Ω-cm^2 (9). Ohmic contacts to GaAs and $In_{0.53}Ga_{0.47}As$ using an InAs cap layer have been studied extensively (9, 10, 11). The contact resistance to GaAs (using an InAs cap layer) decreases on increasing the GaAs active carrier concentration because of the increased tunneling across the InAs/GaAs heterojunction (10). The active carrier concentration in InAs was kept constant in these samples. However, there have been no reports on the effect of InAs active carrier concentration on ρ_c . Here we present the dependence of ρ_c on InAs active carrier concentration. We report a ρ_c of $(0.6 \pm 0.4) \times 10^{-8}$ Ω-cm^2 for non-alloyed, in-situ, refractory molybdenum (Mo) contacts to n-type InAs with 8.2×10^{19} cm^{-3} active carrier concentration.

II. EXPERIMENTAL DETAILS

The semiconductor epilayers were grown by a Gen II solid source MBE system. A 150 nm undoped $In_{0.52}Al_{0.48}As$ layer was grown on a semi-insulating InP (100) substrate, followed by 100 nm of silicon (Si) doped InAs. The samples were grown at 400 °C substrate temperature with the Si cell temperature varying from 1190 °C to 1390 °C. After the InAs growth, the wafer was cooled and transferred under UHV to an electron beam evaporation chamber, where 20 nm of molybdenum (Mo) was deposited on half the wafer through a shadow mask (5). The active carrier concentration, mobility and sheet resistance were obtained from Hall measurements by placing indium contacts on samples taken from the half of the wafer not coated with Mo. The portion of the wafer coated with Mo was processed into transmission line model (TLM) structures for contact resistance measurement.

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To extract the specific contact resistivity, the samples were processed into TLM structures (12). For the TLM structures (Fig. 1), Ti (20 nm) /Au (500 nm) /Ni (50 nm) contact pads were patterned using optical photolithography and lifted-off after an e-beam deposition. The Au layer is 500 nm thick to reduce interconnect resistance. Mo was then dry etched in an SF_6/Ar plasma using Ni as an etch mask. The TLM structures were then isolated using mesas formed by photolithography and a subsequent wet etch. A schematic of the TLM pattern is shown in Fig. 2.

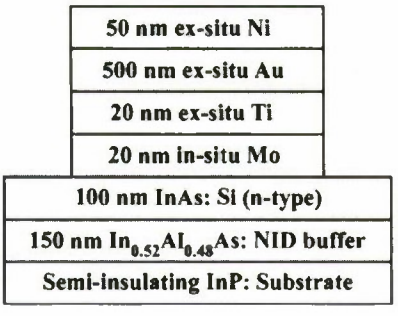

Fig. 1: Cross-section schematic of the metal-semiconductor contact layer structure used for TLM measurements.

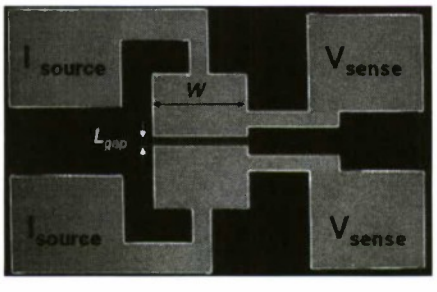

Fig. 2: Schematic of the TLM pattern used for the contact resistivity measurement. Separate pads were used for current biasing and voltage measurement

Resistances were measured using a four-point (Kelvin) probe technique on an Agilent 4155C semiconductor parameter analyzer (5). In the Kelvin probing structure (Fig. 2), the observed resistance,

$$R_{measured} = 2\rho_c / WL_T + \rho_s L_{gap} / W + R_{metal}$$

contains a small contribution R_{metal} from the sheet resistivity (ρ_m / T_m) of the contact metal. Here ρ_c is the metal-semiconductor contact resistivity, ρ_s the semiconductor sheet resistivity, $L_T = \sqrt{\rho_c / \rho_s}$ the transfer length, ρ_m the bulk metal resistivity and T_m the contact metal thickness. The dimensions W and L_{gap} are defined in Fig. 2. R_{metal} is determined from separate measurements of ρ_m / T_m and from numerical finite-element analysis of the contact geometry. For the narrow width (W=10 μm) test structures, R_{metal} changes the contact resistivity data by less than 5 %. Note that the TLM geometry used here (Fig. 2) differs from that used in (5), and the associated R_{metal} term reduced by over 4:1 for W=10 μm.

The sheet resistance of the semiconductor between the contacts does not change after being exposed to SF_6/Ar plasma etch for removing Mo (5). This validates the extraction of the contact resistivity (ρ_c) from the observed lateral access resistivity (ρ_H) and semiconductor sheet resistivity (ρ_s).

III. RESULTS AND DISCUSSION

Fig. 3 shows the variation of active carrier concentration and mobility with Si atomic concentration. For Si atomic concentration greater than 2×10^{20} cm^{-3}, the active carrier concentration was found to saturate because of the auto-compensation behavior of Si at greater atomic concentrations (13). The highest active carrier concentration obtained was 1.2×10^{20} cm^{-3} for a total Si atom concentration of 3.5×10^{20} cm^{-3}. InAs layers grown with Si atom concentration greater than 3.5×10^{20} cm^{-3} resulted in rough and hazy surfaces, probably due to excessive Si incorporation in the layers (13).

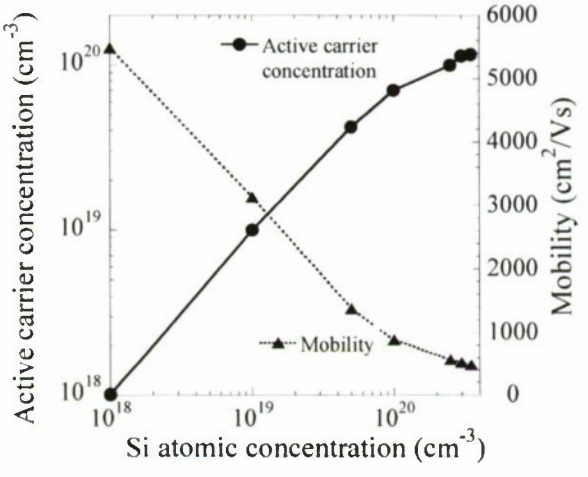

Fig. 3: Variation of active carrier concentration and mobility with Si atomic concentration.

Fig. 4 shows ρ_c as a function of active carrier concentration. For active carrier concentration below 8.2×10^{19} cm^{-3}, ρ_c decreases with increase in the active carrier concentration and saturates for an active carrier concentration greater than 8.2×10^{19} cm^{-3}. This indicates that, although the Fermi level pins in the conduction band for InAs, an active carrier concentration greater than ~ 4×10^{19} cm^{-3} is required to obtain ρ_c less than 1×10^{-8} Ω-cm^2. The lowest ρ_c extracted from the TLM measurements was $(0.6\pm0.4)\times10^{-8}$ Ω-cm^2 for the sample with an active carrier concentration of 8.2×10^{19} cm^{-3}. For this sample, the variation of TLM test structure resistance with contact separation is shown in Fig. 5. Note that after

correcting for the effect of TLM test structure interconnect resistance on measurements (5), we had earlier obtained ρ_c = (1.4±0.5)×10^{-8} Ω-cm^2 for in-situ Mo contacts to a composite layer of 5 nm of n-type InAs on 95 nm of InGaAs (14). For this sample, the active carrier concentration in the InAs layer was 3 ×10^{19} cm^{-3} (calibrated on separate samples). As shown in Fig. 4, ρ_c reported for InAs (5 nm) /InGaAs (95 nm) sample of ref. (14) is greater than expected from the current data because the observed resistivity includes Mo/InAs and InAs/InGaAs interfaces in series. Also shown in Fig. 4 is the ρ_c obtained with *ex-situ*, annealed, contacts to InAs (9), which is greater than for *in-situ* contacts.

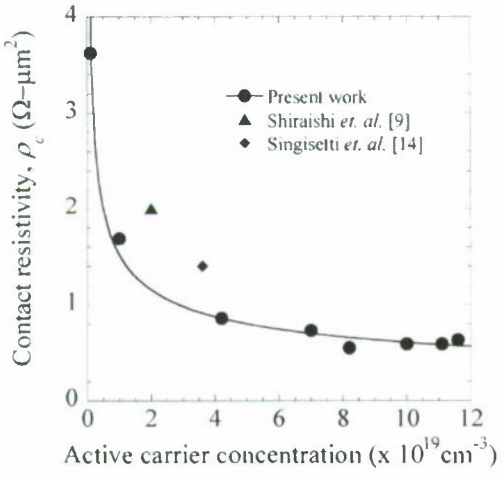

Fig. 4: Variation of specific contact resistivity with active carrier concentration.

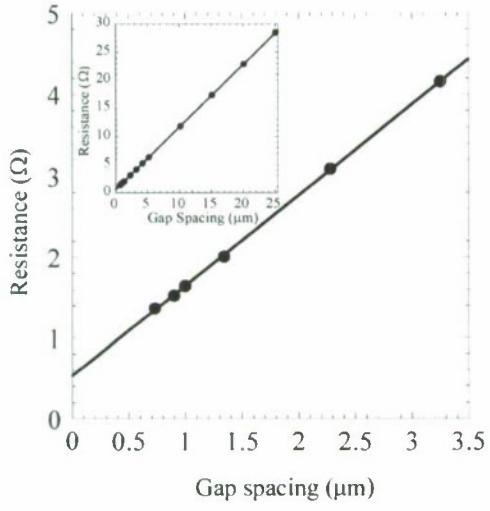

Fig. 5: Measured TLM resistance as a function of pad spacing for the sample with ρ_c = (0.6±0.4)×10^{-8} Ω-cm^2. The inset plots measured TLM resistance vs. pad spacing ranging from 0.8 μm to 25 μm.

For the sample with ρ_c = (0.6±0.4)×10^{-8} Ω-cm^2, the transfer length was 260 nm, 2.6:1 larger than the N+ layer thickness; hence resistance analysis assuming one-dimensional current flow is appropriate. Hall measurements on the same sample with lowest contact resistivity indicate 568 cm^2/Vs mobility, and 10.5 Ω sheet resistivity. The sheet resistivity determined from TLM measurements was 11 Ω, correlating closely to the sheet resistivity obtained with Hall measurements.

To study the thermal stability of the contacts, the processed samples were annealed under nitrogen atmosphere at 250 °C for 1 hour, a thermal cycle representative of the curing cycle of the benzocyclobutene (BCB) passivation and interconnect dielectric used in many III-V IC processes (15). The contacts were found to remain Ohmic and the observed variation in the contact resistivity was less than the margin of error in the measurement.

IV. CONCLUSIONS

We present the dependence of ρ_c on active carrier concentration for *in-situ*, thermally stable, Ohmic contacts to InAs. We show that, although the Fermi level pins in the conduction band for InAs, ρ_c decreases with increased active carrier concentration for active carrier concentrations below 8.2×10^{19} cm^{-3}. ρ_c was found to saturate for active carrier concentrations above 8.2×10^{19} cm^{-3} and the lowest ρ_c obtained was (0.6±0.4)×10^{-8} Ω-cm^2. Our results indicate that active carrier concentrations in excess of ~ 4×10^{19} cm^{-3} are required to obtain ρ_c less than 1×10^{-8} Ω-cm^2. These results indicate the effectiveness of InAs in forming ultra-low resistance Ohmic contacts; application in contacts to layers within III-V devices requires further characterization of the heterojunction interface resistance between InAs and the contacting layer.

ACKNOWLEDGMENTS

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Quantum and classical information processing with a single quantum dot in photonic crystal cavity

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Quantum dots (QDs) coupled to photonic crystal cavities are interesting both as a testbed for fundamental cavity quantum electrodynamics (CQED) experiments, as well as nano-scale devices for optical quantum and classical information processing. In addition to providing a scalable, robust, on-chip, semiconductor platform, this coupled system also enables very large dipole-field interaction strength, as a result of the field localization inside of sub-cubic wavelength volume (vacuum Rabi frequency is in the range of 10s of GHz). In this paper, we describe some of the recent experiments performed on this system in our group.

Interaction of QD with cavity mode happens in two different regimes: weak coupling, where the interaction strength is smaller than the energy loss from the system (cavity decay and QD spontaneous emission) and strong coupling, where the interaction strength is larger than the losses in the system. In the strong coupling regime, the QD and the cavity mode mix and result in polaritons, which is manifested as split cavity resonance at zero detuning of the QD and the cavity mode. Thus in a strongly coupled QD-cavity system, one can probe light-matter interaction at the most fundamental level.

The InAs QD sample is grown by molecular beam epitaxy. Photonic crystal cavities are then made by e-beam lithography, followed by reactive ion etching and removal of AlGaAs sacrificial layer by HF. The chip is kept at cryogenic temperatures (4K to 50K) in a helium-flow cryostat. All the optical experiments are performed in a cross-polarized reflectivity setup. The setup along with SEM picture of a fabricated cavity and electric field profile of the cavity mode is shown in Fig. 1.

We have resonantly probed a strongly coupled QD-cavity system (1) and observed the split resonance (as shown in Fig. 2). The enhanced light-matter interaction in this system enables ultra-low control power electro-optic modulation as a coupled single QD can modify the cavity transmission spectrum. The QD resonance frequency was modulated by a lateral electric field via quantum confined Stark effect (2), and thus the optical transmission through the cavity was changed. Fig. 3(a) shows the different cavity transmission spectra for different lateral bias applied and Fig. 3(b) shows the temporal modulation of the optical signal by an electrical signal. A modulation speed of 150MHz was

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demonstrated with estimated control energy of 1fJ/bit. Currently the modulation speed is limited by the RC constant of the transmission line and the cryostat, while the device-limited speed is in tens of GHz (3).

We have also investigated the quantum nature of this system by probing the photon blockade (4). The presence of the QD makes the otherwise linear cavity, nonlinear, and coupling of one photon to the system hinders the coupling of the second photon. This phenomenon is called photon blockade and can be used to produce deterministic single photons at the output of the cavity QED system (5).

One of the puzzling aspects of the solid state cavity quantum electro-dynamics experiments with QD is off-resonant QD-cavity coupling. Unlike atomic systems, the QD couples to the cavity even when they are far-detuned. We have studied this effect by resonant excitation of the QD (6). We have shown that this coupling can be used for resonant QD spectroscopy. We have also shown that when the cavity is resonantly excited, emission from the QD is observed. Fig. 4 shows experimental results on the off-resonant coupling between the QD and the cavity. By observing the cavity and QD emission one can estimate the QD and the cavity linewidth respectively [Fig. 4 (c)]. We have performed similar experiments on several QD-cavity systems with different detunings between them and have measured the QD linewidth as a function of the excitation laser power. We found that the QD linewidth has a constant power-independent broadening, which is larger than the theoretical prediction (7). This indicates that the additional broadening has to be a result of the mechanism that facilitates off-resonant interaction between the QD and the cavity.

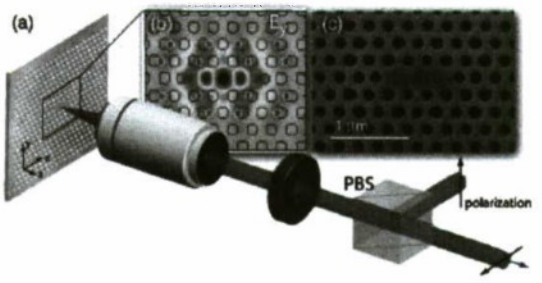

Fig. 1: (a) Cross-polarized reflectivity setup; (b) The FDTD simulation of the electric field profile of the cavity mode; (c) SEM image of the fabricated cavity.

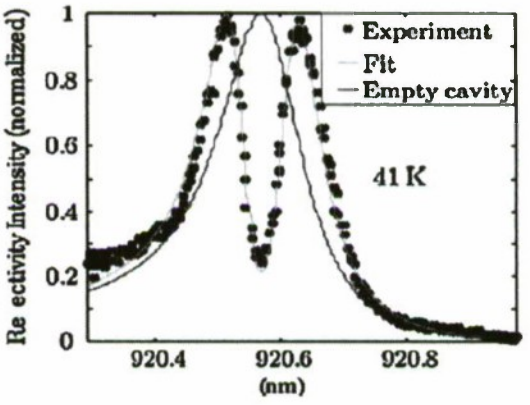

Fig. 2: Transmission spectrum of a strongly coupled QD-cavity system.

In conclusion, the experiments show that the coupled QD-cavity system is a promising candidate for probing CQED as well as for optical information processing. Our present work includes building of a three level system in a QD coupled to cavity, which is essential for construction of any quantum information processing devices.

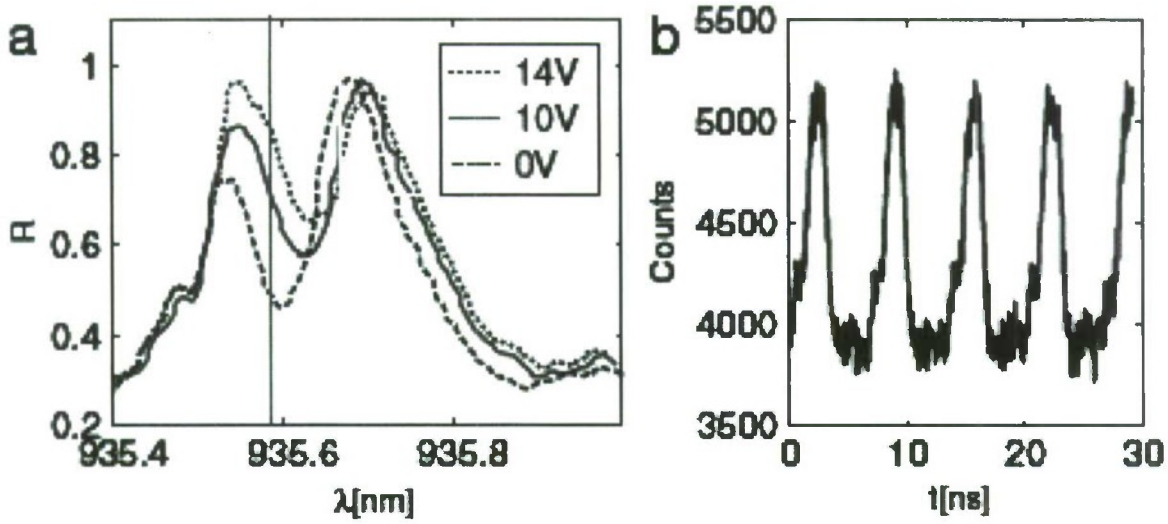

Fig. 3: (a) Transmission spectra of the cavity with different lateral bias voltage across the QD. (b) The modulated optical signal with time. A modulation speed of 150MHz is experimentally achieved.

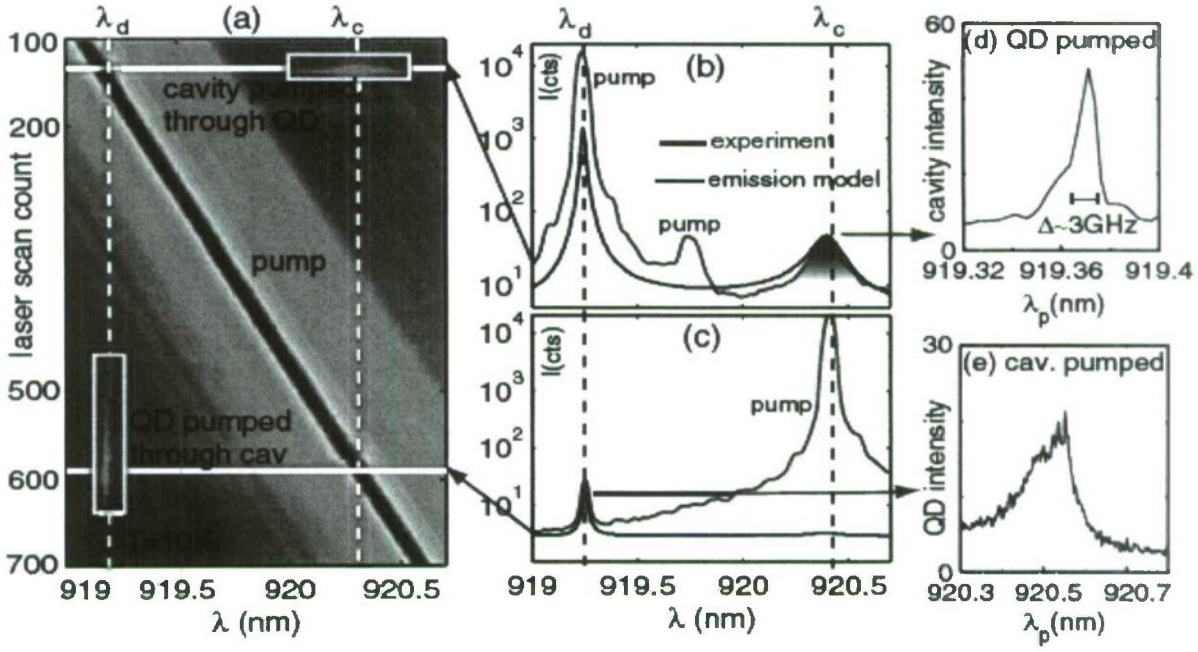

Fig. 4: (a) Two-dimensional plot of the laser scanning the coupled QD-cavity system in time (laser scan count is proportional to time). (b) Spectra showing the off-resonant coupling between the QD and the cavity mode. When the laser is resonant with the QD, we observe emission from the cavity mode. Similarly, laser resonant with the cavity mode causes QD emission. (c) The estimation of QD and cavity line-width by observing the cavity and QD emission respectively. This shows that this coupling can be used for resonant QD spectroscopy.

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Hybrid III-V Laser on Silicon Wire

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Efficient Grating Couplers on InP with Suspended Membrane

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Single quantum dot laser using photonic crystal nanocavity

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We demonstrate laser oscillation in InAs/GaAs single quantum dot (SQD) and photonic crystal nanocavity coupled systems. The coupling SQD provides most of the gain and distinct SQD feature is observed in the photon statistics. Depending on the light-matter coupling strength, laser oscillation starts in the weak- or strong-coupling regime. It is significant that the polariton doublet is still observed at the threshold pump power in the strongly coupled system. This fact indicates that the coherent exchange of quanta between the SQD and the cavity is still sustained under laser oscillation in the intermediate state.

1. Introduction

Development of nanotechnology enables laser oscillation with a small number of emitters, such as a one-atom laser [1]. The system generally includes an isolated gas atom trapped in a vacant large cavity. Such a laser is, in principle, implementable in also solid-state materials by using a semiconductor nanocavity and single quantum dot (SQD). Recent progress in nanostructure fabrication technology enables us to study cavity quantum electrodynamics and achieve lasing using microdisks, micropillars, and photonic crystal (PhC) nanocavities using QD ensembles. However, it has been difficult to implement the complete analogue of a single atom laser in solid; SQD nature is masked by inherent feature of self-tuned gain [2] and by gencrally dense distribution of QDs, which causes multiple QD interference. Here, we demonstrate lasers using a SQD gain with PhC nanocavity. The PhC nanocavity contains only ~1 QD on average and results in high SQD purity of the system.

2. Crystal growth and sample structure

Figure 1(a) shows a scanning electron micrograph of the PhC structure. The sample was grown on an undoped (100)-oriented GaAs substrate by molecular beam epitaxy. A 700-nm-thick $Al_{0.6}Ga_{0.4}As$ sacrificial layer was grown and then, a 165-nm-thick GaAs slab layer was grown including single self-assembled InAs QD layer as the gain material. The areal QD density is 1-4x10^8 cm^{-2}; a nanocavity contains only ~1 QD. The PhC was fabricated by using electron beam lithography, an inductive coupled plasma reactive ion etching process, and wet etching process. The detailed fabrication method has been reported in our previous paper [3]. The nanocavity, which consists of three missing air holes at the center of the PhC pattern, confines photons [4]. The mode-volume is ~0.02 μm^3 and cavity quality factor Q is larger than 14,000. An example of the photoluminescence (PL) spectrum below laser threshold is shown in Fig. 1(b). The target exciton peak can bc spectrally tuned to longer wavelength side and can be coupled to the cavity mode.

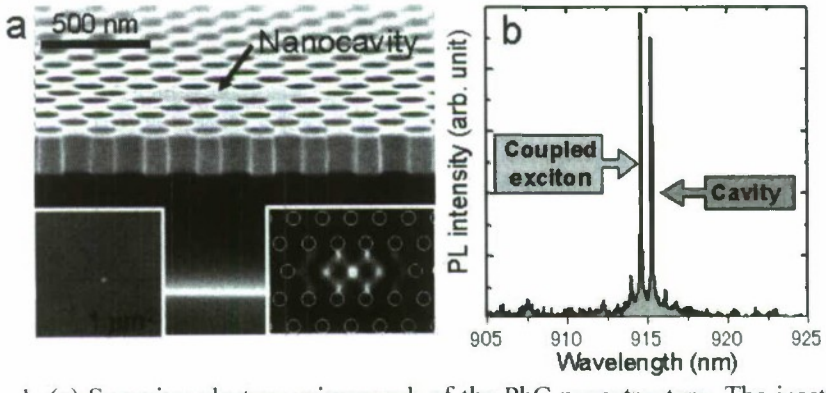

Fig. 1. (a) Scanning electron micrograph of the PhC nanostructure. The insets are an atomic force micrograph of an equivalent uncapped QD sample (left) and simulated electric field distribution. (b) PL spectrum below the threshold. The gain of the system can be controlled by tuning the spectral position of the exciton

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3. Experimental results

3.1. Lasing in a weakly coupled system

The exciton-mode spectral coupling in our system was finely controlled using a temperature-tuning technique. This technique tunes the relative spectral positions of a target QD and the fundamental cavity mode, based on the different temperature dependence of the bandgap and of the refractive index. The contribution of the coupled, SQD gain to the laser oscillation was quantitatively investigated by measuring the laser threshold at various detunings. Figure 2(a) shows PL spectra measured under resonant (red) and far-detuning (blue) conditions. The coupling of a single QD drastically enhances the intensity of the cavity mode. Figure 2(b) shows light-in versus light-out (L-L) plot collected at $\Delta\lambda = 0$ nm. At zero detuning, the threshold was estimated to be ~42 nW, while sufficiently detuned cases required ~145 nW on average (Fig. 2(c)). Thus, the coupling of the single exciton significantly increases the material gain of the system, and results in a significant reduction of the threshold pump power compared with the far-detuning condition. We can estimate that the dominant gain (~71%) is supplied by the coupling SQD. Lasing was observed even under the far-detuning condition. We investigated the gain source of the cavity mode by carrying out cross-correlation measurement under a far-detuning condition of $\Delta\lambda \sim -3.7$ nm. The observed cavity-exciton anti-correlation indicates the occurrence of non-resonant coupling between the SQD and the cavity mode and subsequent non-resonant lasing. This unidentified channelling mechanism is caused by several factors including phonon mediated processes. This channelling mechanism enables the single QD to provide the gain in the far-detuning conditions; a net SQD gain may be larger than 71%. The detailed discussion can be found in ref. 5.

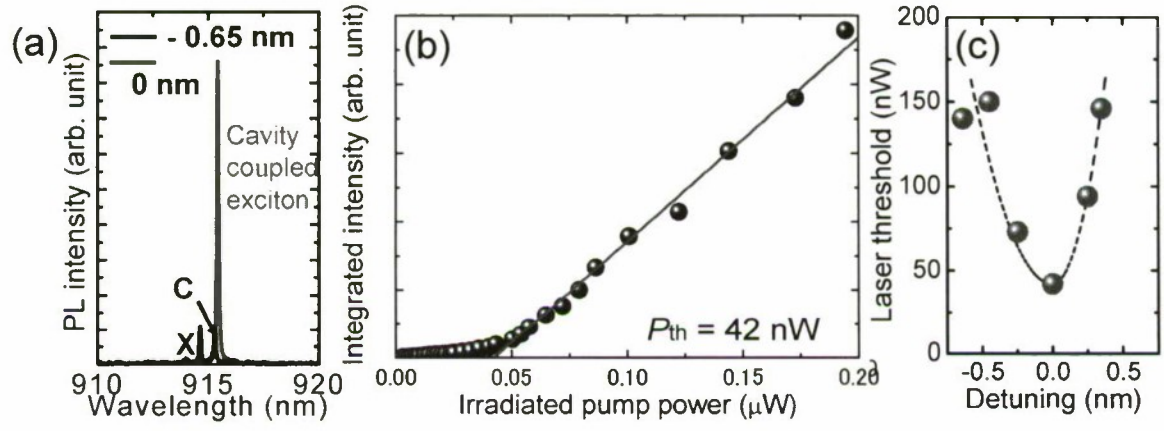

Fig. 2 (a) PL spectra measured under far-detuning (-0.65 nm, blue) and resonant (red) conditions at the excitation power of ~15 nW. (b) L-L plots of the cavity mode under coupled condition. (c) Spectral detuning dependence of laser threshold. Lasing begins at a pump power of 42 nW under resonant condition, while the far-detuning conditions require ~145 nW for lasing. The spectral detuning dependence of the laser threshold indicates that more than 70% of the gain is provided by the coupling single QD. The detuning of the single QD to the cavity mode was carried out by changing the temperature.

3.2 Lasing in a strongly coupled system

In this experiment, we prepared another sample with a stronger light-matter coupling. Fig. 3(a) shows PL spectrum measured at 6 K at sufficiently high detuning of the QD from the cavity mode. The exciton-mode coupling in our system was finely controlled using a temperature-tuning technique as shown in Fig. 3(b) PL spectra were recorded at an irradiated pump power (defined as the power at the sample surface) of ~3 nW as a function of the temperature. In the temperature tuning measurement, typical phenomena in the strong-coupling regime, such as anti-crossing and energy mixing between the two modes, were observed. The spectra measured in the vicinity of zero detuning of the exciton and cavity mode exhibited an exciton-polariton doublet with approximately identical intensity and linewidth (Fig. 3(c)). The estimated exciton-mode coupling strength g was 68 μeV.

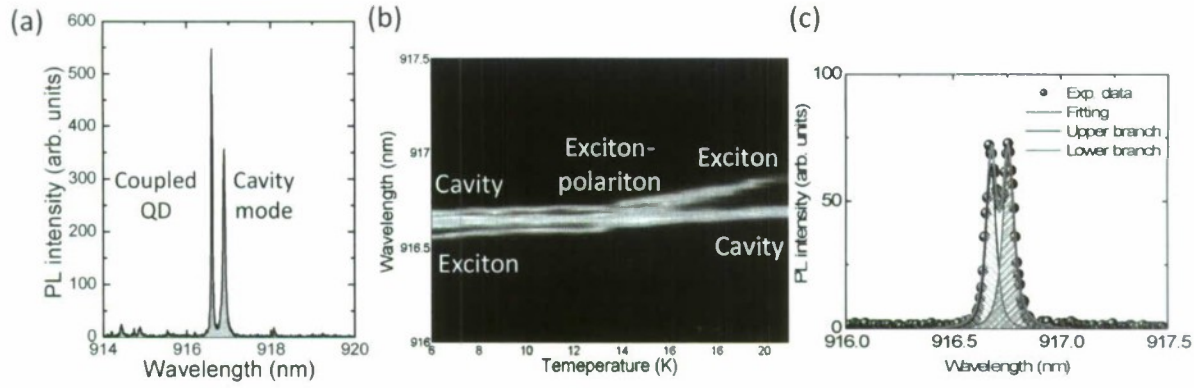

Fig. 3 (a) PL spectrum of the target exciton and the cavity mode at sufficiently high detuning. (b) PL spectra recorded at various detunings, controlled by temperature detuning method, for a pump power of 3 nW shows vacuum Rabi splitting. (c) PL spectrum at zero detuning; clear intensity mixing is observed.

Figs. 4(a), 4(b), and 4(c) show experimental results for an SQD laser originally in the strong-coupling regime. Fig. 4(a) shows the recorded PL spectra between pump powers of ~25 and 500 nW. We found the laser threshold, which is defined by the inflection point, to be ~90 nW by analyzing the light-in versus light-out (L-L) data (Fig. 4(b)). It is noteworthy that the polariton doublet is still observable at the threshold. As the pump power was increased, the polariton doublet merged into a single lasing mode located at the bare cavity resonant wavelength and entered a complete lasing regime, where a drastic linewidth narrowing was observed (not shown). The asymmetry in the PL spectra in the weak pumping regime was due to the unintentional detuning $\Delta\lambda = 0.02$ nm of the excitonic mode and cavity mode. The analysed L-L plots of the two modes are shown in Fig. 4(b). The cavity-like mode (red circle) showed a gentle s-shaped L-L plot. Such a soft turn-on lasing is typically observed in microcavity lasers in which spontaneous emission efficiently couples to the lasing mode. The vacuum Rabi splitting was sustained at the laser threshold, which is defined as the inflection point in the L-L plot. This fact indicates the coexistence of the lasing and coherent exchange of quanta in the system. The photon statistics was also measured by photon correlation measurements. The single QD feature (anti-bunching) and coherent light generation were observed with the photon bunching feature around the laser threshold.

The quantum-statistical characteristics of the photon emission from the system are an important parameter for describing the system. We also calculated the mean cavity photon number N_{ph} and $g^{(2)}(0)$ in the steady state for the SQD purity of 80% (Fig. 3(c)). The computed pump rate dependence of $g^{(2)}(0)$ for each SQD purity was normalized by the corresponding threshold pump rate in order to compare the general behaviour of $g^{(2)}(0)$ around the threshold. The general behaviour of the measured $g^{(2)}(0)$, such as the SQD feature, photon bunching, and coherent light generation, can be explained on the basis of a computed $g^{(2)}(0)$ with an SQD purity of 80% using the relatively simplified simulation model. It is significant that slight photon bunching signature is observed around the laser threshold, which is a hallmark of the transition to laser oscillation.

It has been reported that the strong-coupling state is unexpectedly resistant to dephasing and often appears 'in the disguise' of a single peak [7]. Now, we examine whether the coherent exchange dynamics survives at the laser threshold or not. We have calculated the estimated the threshold pumping rate and the strong-coupling limit and obtained ~590 GHz and 800 GHz, respectively. The analyses of experimental results by numerical simulations brought us to the conclusion that laser oscillation, while partly maintaining a coherent exchange of a quantum between the SQD and cavity, occurred between the pump rates of 590 and 800 GHz. This result indicates the coexistence of vacuum Rabi oscillation and laser oscillation in the cavity in this pumping regime. The details about photon correlation measurements and simulations can be found in ref. 6.

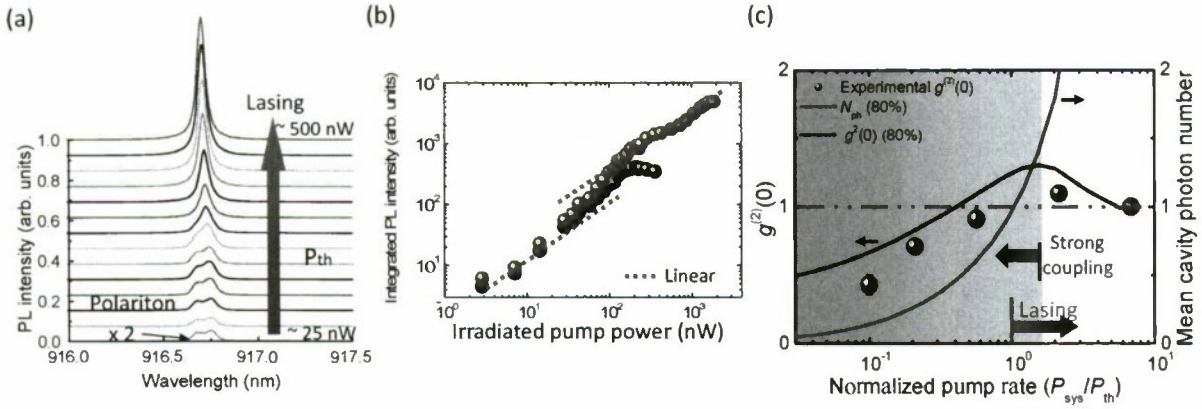

Fig. 4 (a) Pump power dependence of the PL spectrum of a strong-coupling SQD laser. The spectral transition from the exciton-polariton state to lasing is observed. (b) L-L plots of two polariton branches analyzed by two Voigt functions. A slight detuning resulted in lasing in cavity-like branch (red ball), which is observed as the lower exciton-polariton branch in Fig. 4(a). (c) Calculated mean cavity photon number and $g^{(2)}(0)$s for SQD purity of 80% as a function of pump power, and experimental $g^{(2)}(0)$ values (purple circle). Laser oscillation begins ($N_{ph} > 1$) in the strong-coupling regime (light-blue region). The general behaviour of the measured $g^{(2)}(0)$ can be explained on the basis of a computed $g^{(2)}(0)$ with an SQD purity of 80%. Slight photon bunching is experimentally observed at $2.1P_{th}$.

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High speed III-V devices for low power logic application

M. Radosavljevic, *Intel, USA*

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Logic Characteristics of 40 nm thin-channel InAs HEMTs

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Abstract

We have experimentally investigated the trade-offs involved in thinning down the channel of III-V FETs with the ultimate goal of enhancing the electrostatic integrity and scalability of these devices. To do so, we have fabricated InAs HEMTs with a channel thickness of t_{ch} = 5 nm and we have compared them against, InAs HEMTs with t_{ch} = 10 nm. The fabricated thin-channel devices exhibit outstanding logic performance and scalability down to 40 nm in gate length. L_g = 40 nm devices exhibit S = 72 mV/dec, DIBL = 72 mV/V, and I_{ON}/I_{OFF} = 2.5 x 10^4, all at V_{DS} = 0.5 V. However, there are trade-offs of using a thin channel which manifest themselves in a higher source resistance, lower transconductance, and lower f_T when compared with InAs HEMTs with t_{ch} = 10 nm.

INTRODUCTION

As conventional Si CMOS scaling approaches the end of the roadmap, III-V based MOSFETs are being considered as an alternative technology to continue transistor size scaling [1-2]. In the quest to map the potential of III-Vs for future CMOS applications, the High Electron Mobility Transistor (HEMT) has emerged as a valuable model system to understand fundamental physical and technological issues. In fact, recently, excellent logic characteristics have been demonstrated in InAs HEMTs with gate length as small as 30 nm [3-4]. This is mainly a result of the outstanding electron transport properties of InAs and the use of a thin quantum well channel. Further scalability to L_g = 10 nm dimension characteristic of a future III-V CMOS technology will require harmonious scaling of all relevant device dimensions including the channel thickness. A consequence of very thin channel is that carrier transport deteriorates, mainly as a result of increased carrier scattering [5]. This can detract from performance.

In order to understand the trade-offs involved in thinning the channel in sub-100 nm III-V FETs, we have experimentally investigated the characteristics of InAs HEMTs with a 5 nm thick channel. This is half the value of earlier device demonstrations from our group [4]. We show that a very thin channel design substantially improves short channel effects (SCEs) and output conductance (g_o) characteristics but deteriorates its transport properties and access resistance. Future self-aligned gate (SAG) device architectures should be able to mitigate these problems.

PROCESS TECHNOLOGY

Fig. 1 shows a schematic cross sectional view of the device giving the details of the epitaxial layer structure. This heterostructure is essentially identical to that of our previous InAs HEMT designs [4] except that the channel consists of a multilayer structure with a 2 nm thick pure InAs core surrounded by a 1 nm $In_{0.7}Ga_{0.3}As$ top cladding and a 2 nm nm $In_{0.7}Ga_{0.3}As$ bottom cladding layer. In an epi wafer with an identical heterostructure except for a simpler 10 nm InGaAs capping layer with 1 x 10^{18} /cm^3 Si doping, the Hall mobility ($\mu_{n,Hall}$) and carrier density (n_s) were 9,950 cm^2/V-s and 2.5 x 10^{12} /cm^3. This is about 30 % lower than the value obtained in a 10 nm thick channel InAs HEMT heterostructure with a 5 nm InAs core [6] and reveals the increased carrier scattering that comes with channel thickness scaling.

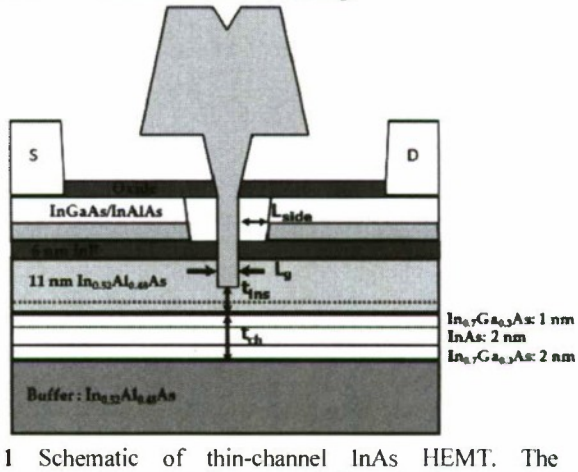

Fig. 1 Schematic of thin-channel InAs HEMT. The heterostructure features a 5 nm total channel thickness that includes a 2 nm InAs core channel layer.

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Device fabrication closely follows our previous device demonstrations [6]. We used a three-step gate recess process that yielded an InAlAs barrier thickness in the intrinsic region, t_{ins}, of about 4 nm and a Ti/Pt/Au (20/20/300 nm) T-gate with gate-cap edge distance L_{side} = 80 nm. We have fabricated devices with L_g values in the range of 40 to 200 nm.

For reference, we simultaneously fabricated devices on an InAs HEMT heterostructure with t_{ch} = 10 nm that it is very similar to an epi wafer structure that we have processed earlier [6]. These devices have gone through an identical process and should therefore have closely matched dimensions.

DC AND LOGIC CHARACTERISTICS

Fig. 2 shows the output characteristics of 40 nm gate length InAs HEMTs on both heterostructures. Both devices exhibit excellent pinch-off and saturation characteristics up to V_{DS} = 0.7 V. The threshold voltages of both devices are -0.22 V at 1 mA/mm of I_D and V_{DS} = 0.5 V. Interestingly, the thin channel device show much better output conductance. This is expected as a result of reduced impact ionization and V_T dependence on V_{DS} (DIBL, discussed below). These are both a product of a thin highly quantized channel. However, the thin-channel HEMTs exhibit slightly higher R_{ON}.

Fig. 3 shows subthreshold and gate current characteristics of both 40 nm InAs HEMTs at V_{DS} = 50 mV and 0.5 V. The thin-channel (t_{ch} = 5 nm) device shows much shaper subthreshold swing and much less threshold voltage shift with V_{DS} (DIBL) than the thick-channel (t_{ch} = 10 nm) device. For the t_{ch} = 5nm device, the subthreshold swing (S) is 72 mV/dec, the drain-induced-barrier-lowering (DIBL) is 72 mV/V, and the I_{ON}/I_{OFF} ratio is 2.5 x 10^4. These results compare favorably with those obtained on the t_{ch} = 10 nm device which are 79 mV/dec, 84 mV/V, and 9 x 10^3, respectively.

Fig. 4 shows typical transconductance characteristics of both InAs HEMTs at V_{DS} = 0.5 V. The 5 nm thick channel device exhibits a maximum transconductance of 1.65 S/mm, while the 10 nm channel HEMT shows 1.75 S/mm.

Fig. 5 shows the subthreshold and gate leakage current characteristics of thin channel InAs HEMTs from L_g = 200 nm to 40 nm at V_{DS} = 0.5 V. There is a very small V_T shift of less than 34 mV as the gate length scales down from 200 to 40 nm. In contrast, the V_T shift of the 10 nm thick devices over the same gate length rage is 55 mV.

The superior scalability of the 5 nm devices is also manifested in the evolution of S and DIBL with L_g (**Fig. 6** and **Fig. 7**). These figures also include result from an earlier set of devices with a 13 nm InGaAs channel, and similar value of L_{side} and t_{ins} [3]. It is clear that thinning down the channel brings significant benefits in terms of improved electrostatic integrity and scalability.

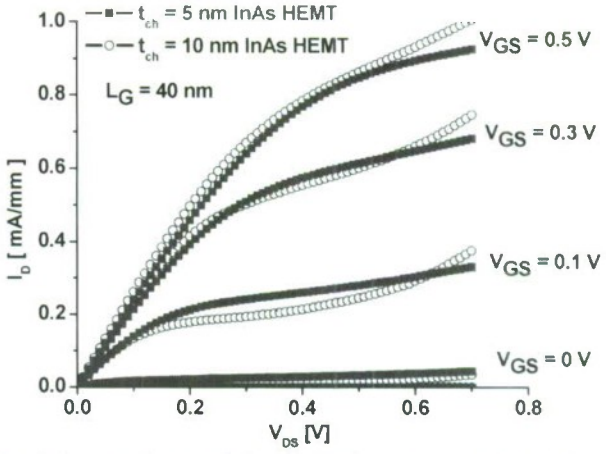

Fig. 2 Output characteristics for both 40 nm gate length InAs HEMTs.

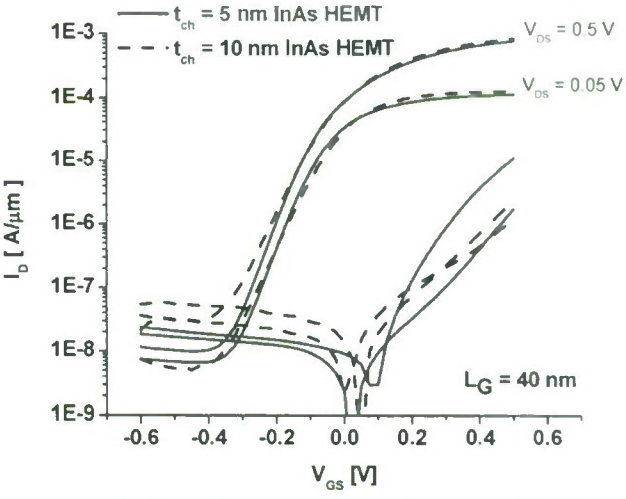

Fig. 3 Subthreshold and gate leakage characteristics for both 40 nm gate length InAs HEMTs.

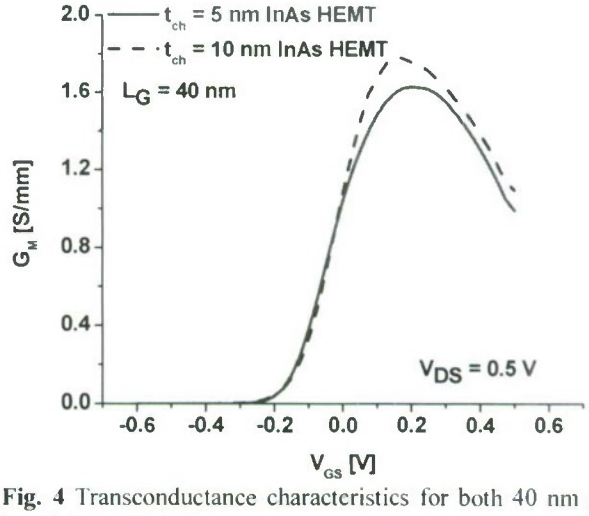

Fig. 4 Transconductance characteristics for both 40 nm gate length InAs HEMTs.

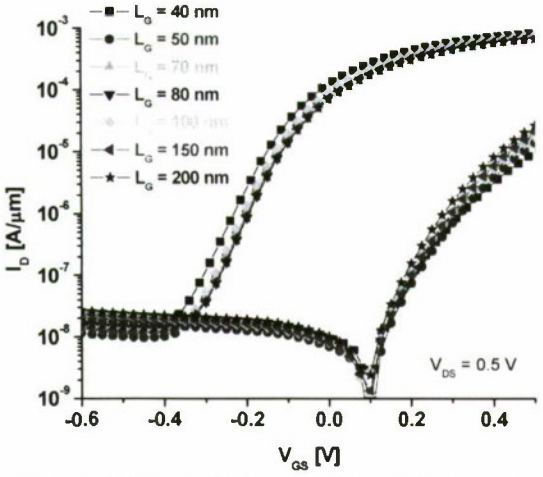

Fig. 5 Subthreshold and I_G characteristics for 5 nm thick channel InAs HEMTs with different values of L_g at V_{DS} = 0.5 V.

The increased R_{ON} observed in **Fig. 2** and the decreased transconductance observed in **Fig. 4** for the thin channel device also points out the trade-offs of the present approach. They essentially arise from enhanced scattering which translates into lower channel electron mobility. **Fig. 8** shows the evolution of the transconductance as a function of gate length at V_{DD} = 0.5 V for the three types of devices. At all gate lengths, the present devices exhibit a lower extrinsic transconductance than the 10 nm thick channel InAs HEMTs but better than the 13 nm thick channel InGaAs HEMTs which show poor scalability.

To understand this result better, we have carried out measurements of the effective source resistance, R_S^*, using the gate current injection method [7]. As shown in **Fig. 9**, R_S can be extracted by linear extrapolation to zero L_g. The extracted R_S^* for thin channel devices is 0.255 Ohm•mm, in contrast with 0.24 Ohm•mm for the 10 nm thick channel devices and 0.25 Ohm•mm for the 13 nm thick channel devices. In addition, we found that devices with the 5 nm thick channel exhibit a higher sheet resistance (320 Ohm/sq) in the channel region when compared with 240 Ohm/sq for the 10 nm InAs HEMTs and 280 Ohm/sq of the 13 nm InGaAs HEMTs. Self-aligned gate (SAG) device architectures should be able to partially mitigate this problem.

Using these measurements, we have extracted the intrinsic transconductance of our transistors. Our extraction accounts for the effects of output conductance (g_o), R_S, and R_D. **Fig. 8** shows a reduced value of g_{mi} for the thin channel when compared with the 10 nm thick channel devices but better scalability. In fact, at L_g = 40 nm, the intrinsic transconductance is about the same in both transistors. It seems reasonable to expect that for shorter gate lengths, the thin channel device will surpass the thicker designs in terms of intrinsic transconductance as it should continue to scale much better.

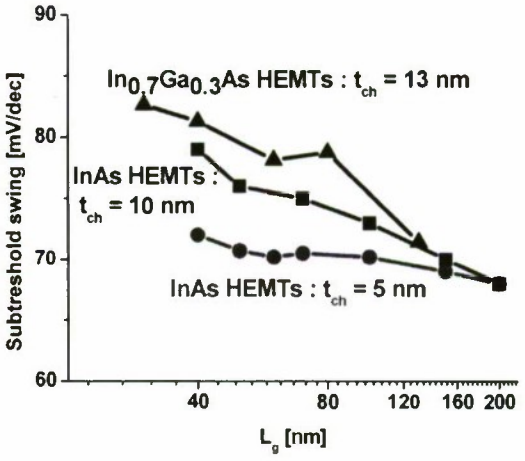

Fig. 6 Subthreshold swing of InAs HEMTs with t_{ch} = 5 nm and 10 nm as well as $In_{0.7}Ga_{0.3}As$ HEMTs with t_{ch} = 13 nm as a function of L_g.

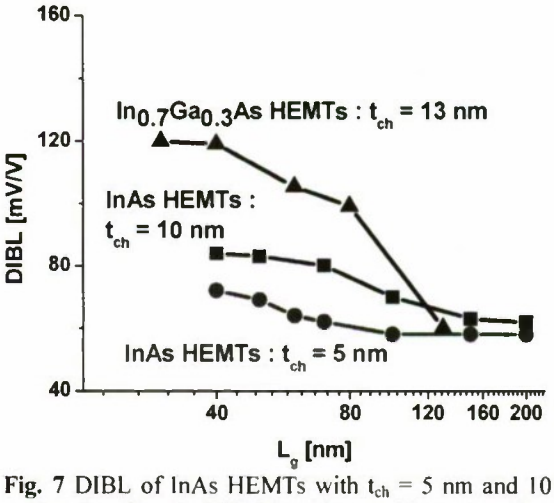

Fig. 7 DIBL of InAs HEMTs with t_{ch} = 5 nm and 10 nm as well as $In_{0.7}Ga_{0.3}As$ HEMTs with t_{ch} = 13 nm as a function of L_g.

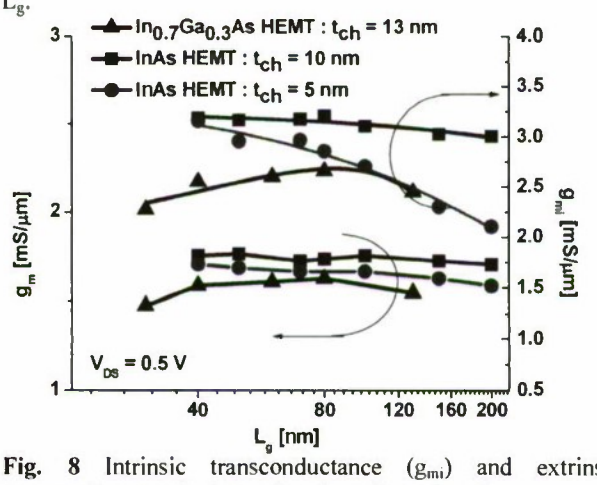

Fig. 8 Intrinsic transconductance (g_{mi}) and extrinsic transconductance (g_m) as a function of gate length.

MICROWAVE CHARACTERISTICS

Small-signal microwave performance was characterized from 0.5 to 40 GHz. On-wafer open and short patterns were used to subtract pad capacitances and inductances from the measured device S-parameters. **Fig. 10** plots current gain (H_{21}) and unilateral gain (U_g) as a function of frequency for the best bias conditions at V_{GS} = 0.2 V and V_{DS} = 0.6 V for L_g = 40 nm thin and thick channel InAs HEMTs. Values of f_T = 445 GHz and f_{max} = 395 GHz have been obtained for the t_{ch} = 5 nm device while values of f_T = 520 GHz and f_{max} = 337 GHz have been obtained for the t_{ch} = 10 nm device. For the 5 nm channel device, f_T is lower but f_{max} is higher. Low f_T mainly comes from a high source resistance and a higher gate capacitance without any higher intrinsic transconductance which reflects a lower velocity. The higher f_{max} is due to the improved output conductance (g_o) characteristics which arise from the reduced impact ionization and strong electron confinement. This is shown in **Fig. 11** which graphs the output conductance (g_o) as a function of I_D for three difference devices with L_g = 40 nm. As I_D increases, 5 nm thick channel InAs HEMTs exhibit much better output conductance (g_o) than the 10 nm thick InAs HEMTs.

CONCLUSION

We have demonstrated 40 nm InAs HEMTs with a 5 nm thick channel. The devices show excellent short-channel effects and scalability although their performance suffers from an increased source resistance. In particular, 40 nm devices exhibits S = 72 mV/dec, DIBL = 72 mV/V, and I_{ON}/I_{OFF} = 2.5 x 10^4. These encouraging results stem from the combination of the outstanding transport properties of InAs and the tight electron confinement afforded by the thin channel. But there are trade-offs in the thin channel approaches which are related to degraded transport properties and access resistance. However, future self-aligned gate (SAG) device architectures should be able to mitigate these problems. This work suggests that future thin InAs channel MOSFETs have the potential for scaling to very small dimensions.

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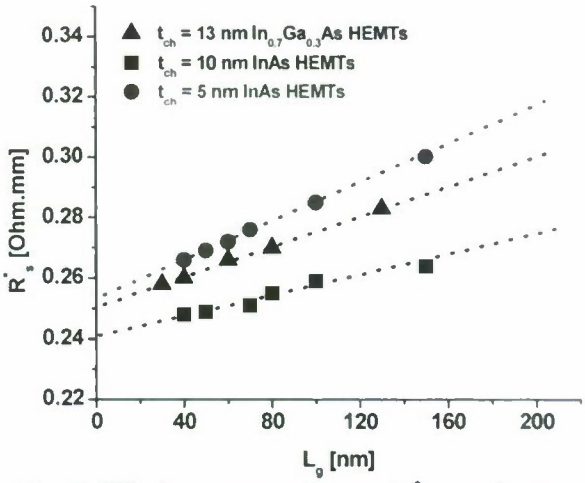

Fig. 9 Effective source resistance R_s^* as a function of L_g obtained through the gate current injection technique.

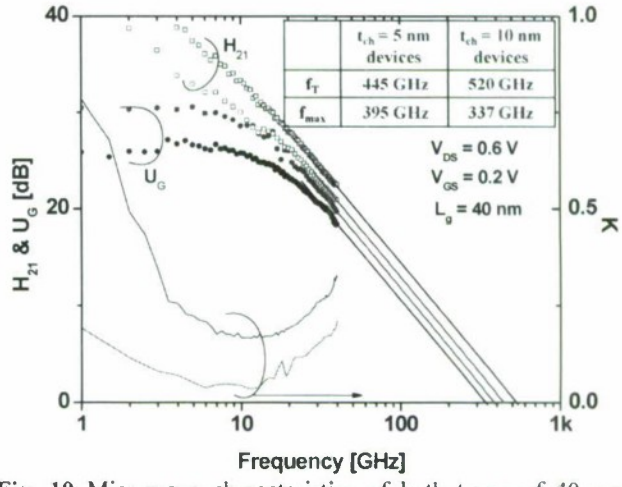

Fig. 10 Microwave characteristics of both types of 40 nm InAs HEMTs with t_{ch} = 5 nm and t_{ch} = 10 nm.

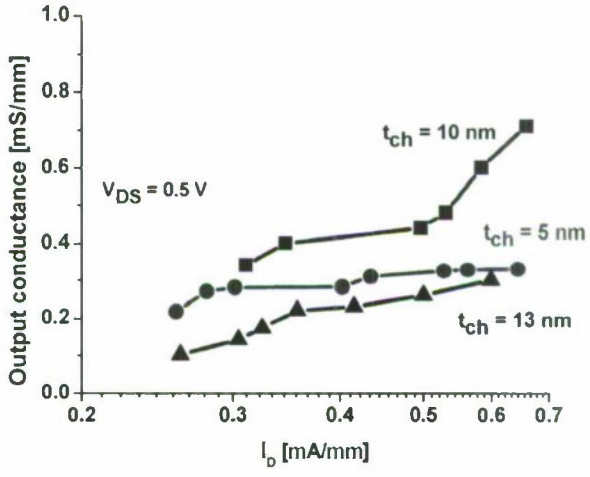

Fig. 11 Output conductance (g_o) characteristics as a function of I_D for three different L_g = 40 nm devices at V_{DS} = 0.5 V.

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III-V-SEMICONDUCTOR-ON-INSULATOR MISFETs ON Si WITH BURIED SiO_2 AND Al_2O_3 LAYERs BY DIRECT WAFER BONDING

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Abstract

We have developed III-V-OI MISFETs on Si with buried SiO_2 and Al_2O_3 layers fabricated by low damage and low temperature direct wafer bonding processes. The III-V-OI MISFETs with both buried SiO_2 and Al_2O_3 layers have demonstrated the high electron mobility of 1200 cm^2/Vs. In addition, we found that the buried Al_2O_3 layers can improve the interface condition between III-V and the buried oxide layers, leading to the higher electron mobility of III-V-OI MISFETs even in the high electric field than that of Si MOSFETs. These high performance transistors will open up the way to the future high performance logic LSI systems.

I. Introduction

III-V metal-insulator-semiconductor field-effect transistors (MISFETs) have intensely been investigated because of the scaling limit of the Si metal-oxide-semiconductor field-effect transistors (MOSFETs) [1]. Integration of high mobility materials as a channel material is expected to be a technology booster in the near future. High-performance bulk InP and InGaAs channel MISFETs on III-V-semiconductor wafers have been demonstrated due to the recent progress of atomic-layer-deposition (ALD) technology for the gate dielectric formation on III-V [2]-[4]. However, integrating III-V MISFETs on the Si platform is still challenging. It is difficult to obtain the high crystal quality thin body III-V semiconductor layers on Si substrates by directly epitaxial growth because of the large lattice mismatch between III-Vs and Si. Instead, a direct wafer bonding (DWB) process is promising for the integration III-V MISFETs on the Si platform [5] [6]. As a result, the DWB process is anticipated to offer an excellent integration way of high mobility materials with the Si platform, and thus III-V-semiconductor-on-insulator (III-V-OI) MISFETs on Si can offer the ultimate CMOS transistors [1].

In this paper, we demonstrate metal source/drain (S/D) thin body InGaAs-OI MISFETs on Si with both SiO_2 and Al_2O_3 buried oxide (BOX) layers. They demonstrate the high electron mobility of 1200 cm^2/Vs. Moreover, we find that the Al_2O_3 BOX layers can offer the smoother InGaAs/Al_2O_3 interface roughness, compared to the InGaAs/SiO_2 ones, which results in the higher electron mobility than Si even in the high electric field.

II. Fabrication of III-V-OI-on-Si wafer

A. Fabrication of III-V-OI-on-Si with SiO_2 BOX

Thin body III-V-OI-on-Si wafers were fabricated by low damage and low temperature DWB processes. Figure 1(a) shows a schematic illustration of a process flow of the III-V-OI wafers with SiO_2 BOX layers using a low damage and low temperature electron-cyclotron-resonance (ECR) plasma assisted DWB process [5] [6]. First, a 100-nm-thick $In_{0.53}Ga_{0.47}As$ channel layer was grown on InP(001) wafers by metal-organic vapor phase epitaxiy (MOVPE). Then, a SiO_2 layer was deposited on the $In_{0.53}Ga_{0.47}As$/InP(001) wafer by ECR sputtering. The ECR O_2 plasma was irradiated with both III-V and Si wafers. Next, the III-V wafer was bonded to a Si wafer, followed by annealing to enhance the bonding energy. Finally, InP was removed by HCl solution, and then the InGaAs-OI on Si wafer completed. Figure 1(b) shows a transmission infrared (IR) image of a III-V-OI-on-Si wafer (InP/InGaAs/SiO_2-Si), indicating the successful bonding in the 2-inch wafers fabricated with an ECR-SiO_2 BOX layer.

B. Fabrication of III-V-OI-on-Si with Al_2O_3 BOX

The III-V-OI wafers with Al_2O_3 BOX layers were fabricated by a surface activated bonding (SAB) process using

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Ar beam irradiation, which is suitable for bonding high-k materials with Si wafers [7] [8]. Figure 1(c) shows a process flow of III-V-OI-on-Si wafers using the SAB process. First, a 100-nm-thick $In_{0.53}Ga_{0.47}As$ channel layer was grown on InP(001) wafers by MOVPE. An Al_2O_3 layer was deposited on the $In_{0.53}Ga_{0.47}As$/InP(001) wafer by ALD. After an Ar beam was irradiated with both III-V and Si wafers in a SAB vacuum chamber, the III-V wafer was bonded to a Si wafer. Finally, InP was removed by HCl solution, and then the InGaAs-OI on Si wafer completed. Compared to the plasma assisted DWB process, the SAB process can offer us the strong bonding without thermal treatment after bonding wafers.

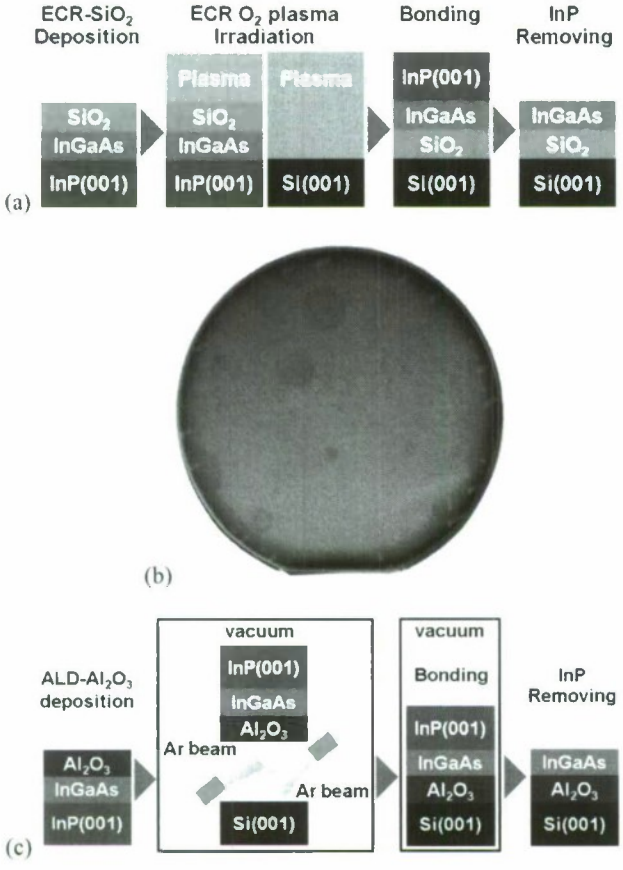

Fig. 1 (a) Process flow of the III-V-OI-on-Si wafers with ECR-SiO_2 BOX layers using the ECR O_2 plasma assisted DWB process. (b) Transmission IR image of a III-V-OI-on-Si wafer The wafer size is 2 inch in diameter. (c) Process flow of the III-V-OI-on-Si wafers with ALD-Al_2O_3 BOX layers using the SAB process.

C. Feature of our DWB processes (TEM observation)

Both BOX layers can protect the III-V-OI channels from plasma, Ar beam and bonding damage. Additionally, the high selectivity between InP and InGaAs (InP:InGaAs>1000:1) can enable us to fabricate thin body III-V-OI channels without serious damage during removing an InP substrate. Figures 2(a) and 2(b) show cross-sectional transmission electron microscope (TEM) images of InGaAs-OI-on-Si wafers with SiO_2 and Al_2O_3 BOX layers. Both InGaAs/BOX and bonding interfaces are abrupt and smooth, indicating that the bonding processes were employed without serious damage.

D. Fabrication of III-V-OI MISFETs

Using both fabricated III-V-OI-on-Si wafers, metal S/D III-V-OI MISFETs with back-gate configuration were fabricated as shown in Fig. 3. First, a Au-Ge alloy was formed by a standard lift-off method, as metal S/D. Secondary, the device isolation was done by etching InGaAs using H_3PO_4:H_2O_2:H_2O solution, and a back-gate Al electrode was deposited on the back side of the Si substrate. Here, we investigated the electric transport properties of III-V-OI MISFETs in accumulation-mode.

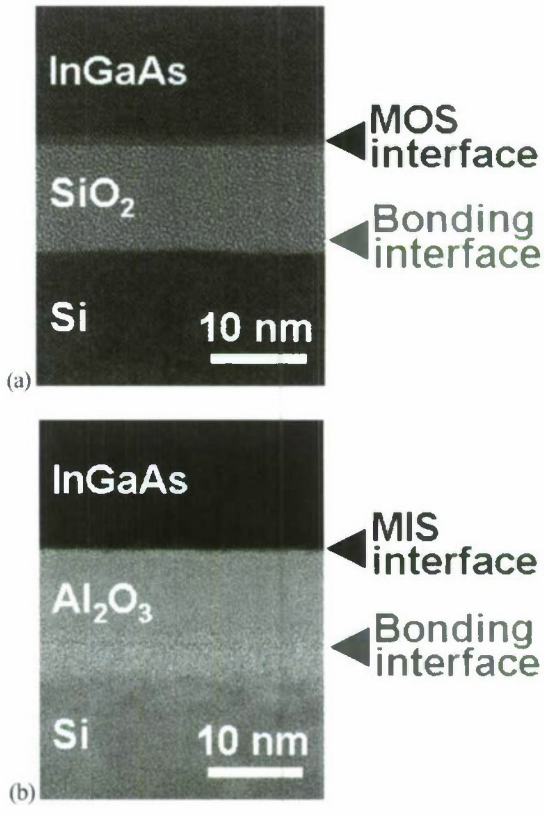

Fig. 2 Cross-sectional TEM images of III-V-OI-on-Si with (a) a SiO_2 and (b) an Al_2O_3 BOX layer. Both InGaAs/BOX and bonding interfaces are smooth and abrupt.

III. Transistor performances

A. III-V-OI MISFET on Si with SiO_2 BOX

Figure 4 shows the transistor characteristics of the metal S/D thin body III-V-OI MISFETs with a SiO_2 BOX layer. Figures 4(a) and 4(b) show the drain current *versus* drain voltage ($I_D - V_D$) and the drain current *versus* gate voltage ($I_D - V_G$) characteristics, respectively. The transistors exhibited excellent saturation and pinch-off characteristics. The on-current to off-current (I_{on}/I_{off}) ratio and the S factor were $\sim 10^5$ and 98 mV/dcc. Considering the narrow band gap of 0.74 eV, the amount of the leak current (<10 pA/μm) is quite low. The interface state density D_{it} estimated from the S factor was $\sim 1 \times 10^{12}$ $cm^{-2}eV^{-1}$.

B. III-V-OI MISFET on Si with Al_2O_3 BOX

Figure 5 shows the transistor characteristics of the metal S/D thin body III-V-OI MISFETs with an Al_2O_3 BOX layer. Figures 5(a) and 5(b) show the $I_D - V_D$ and $I_D - V_G$ characteristics, respectively. The transistors showed excellent saturation and pinch-off characteristics. The I_{on}/I_{off} ratio and the S factor were $\sim 10^5$ and 170 mV/dec. Considering the narrow band gap of 0.74 eV, the amount of the leak current (<10 pA/μm) is quite low. The interface state density D_{it} estimated from the S factor was $\sim 3 \times 10^{12}$ cm^{-2} eV^{-1}. The InGaAs-OI MISFETs with an Al_2O_3 BOX layer also demonstrated high transistor performances, as similar to the InGaAs-OI MISFETs with a SiO_2 BOX layer. This is the first demonstration of a channel-on-insulator structure with a high-k material BOX layer.

C. Mobility of III-V-OI MISFET on Si

Figure 6 shows the effective mobility *versus* effective electric field ($\mu_{eff} - E_{eff}$) characteristics of InGaAs-OI with a SiO_2 and an Al_2O_3 BOX layer and of Si MOSFETs ($N_{sub}=4\times10^{15}$ cm^{-3}), respectively. Both InGaAs-OI MISFETs demonstrated the high peak μ_{eff} of 1200 cm^2/Vs. Here, we assumed a constant capacitance value, independent of V_G, meaning that the measured μ_{eff} values could be lower than the real values, particularly in the low E_{eff} range. Nevertheless, this electron mobility was almost comparable to that of the bulk III-V MISFETs with the $In_{0.53}Ga_{0.47}As$ channel. Furthermore, the mobility of the InGaAs-OI MISFET with an Al_2O_3 BOX layer retained higher than that of Si MOSFET even in the high E_{eff} range. These results indicate that both DWB processes are applicable to fabricating the ultrathin body III-V-OI structure with a superior III-V MIS interface. According to the TEM observation, the mobility reduction of III-V-OI MISFETs with SiO_2 BOX in the high E_{eff} range could be attributable partly to existence of III-V oxide at the InGaAs/SiO_2 interface. On the other hand, the mobility improvement of III-V-OI MISFETs with Al_2O_3 BOX in the high E_{eff} range can be attributable partly to reduction in carrier scattering at the InGaAs/Al_2O_3 BOX interface due to the smoother III-V-OI interface flatness.

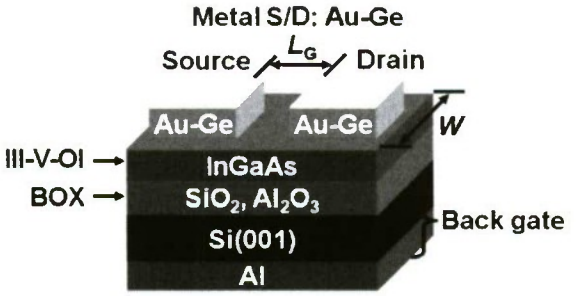

Fig. 3 Schematic illustration of a metal S/D III-V-OI MISFET on Si with a SiO_2 or Al_2O_3 BOX layer in back-gate configuration.

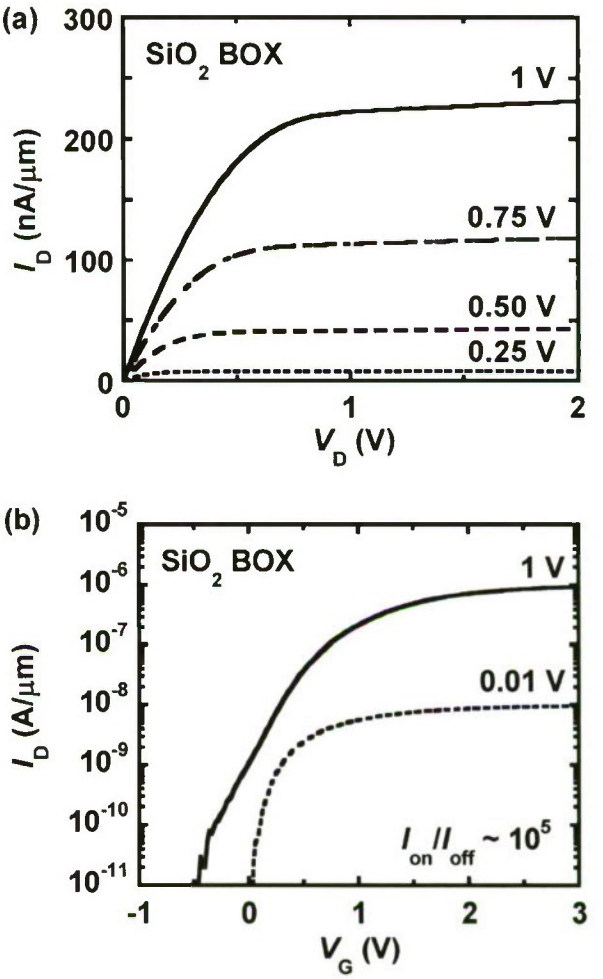

Fig. 4 (a) $I_D - V_D$ and (b) $I_D - V_G$ characteristics of metal S/D thin body InGaAs-OI MISFETs with a SiO_2 BOX layer.

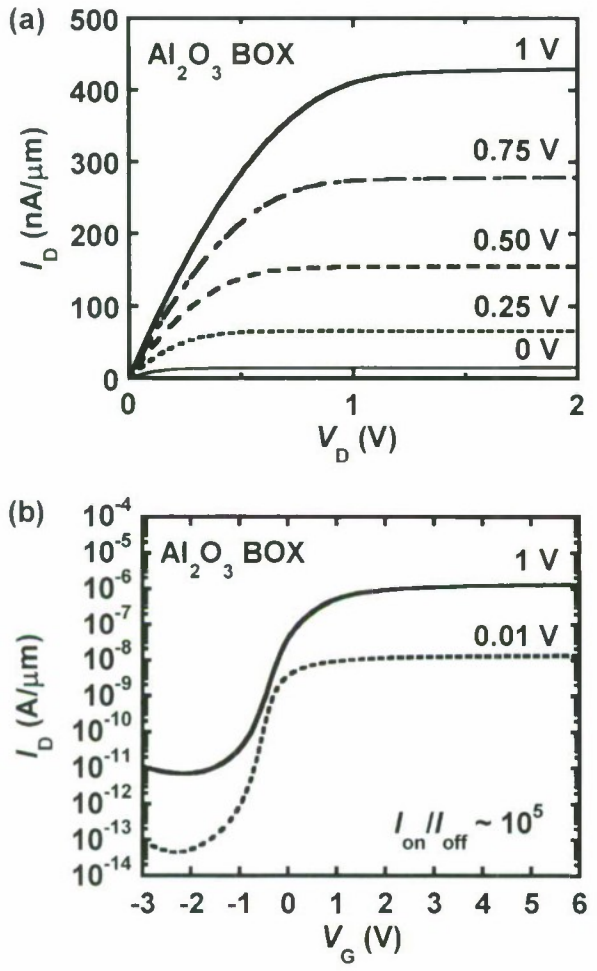

Fig. 5 (a) $I_D - V_D$ and (b) $I_D - V_G$ characteristics of metal S/D thin body InGaAs-OI MISFETs with an Al_2O_3 BOX layer.

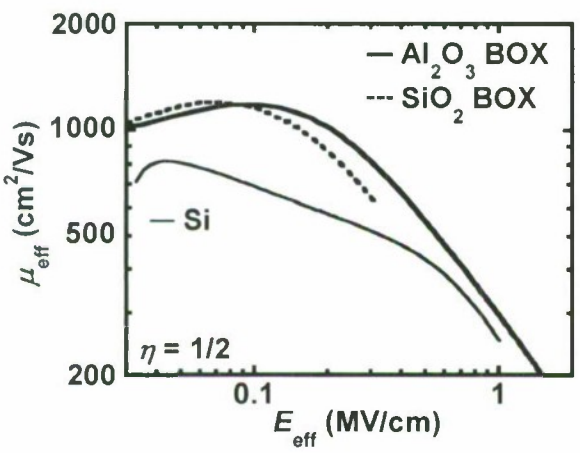

Fig. 6 $\mu_{eff} - E_{eff}$ characteristics of metal S/D thin body InGaAs-OI MISFETs with a SiO_2 and an Al_2O_3 BOX layer.

IV. Conclusions

We have developed metal S/D thin body III-V-OI MISFETs on Si wafers using the low damage and low temperature DWB processes, whose performances are comparable to those of the bulk III-V MISFETs. The present III-V-OI MISFETs and DWB techniques are promising for integrating ultrathin body or multi gate III-V-OI MISFETs on the Si CMOS platform as the ultimate CMOS transistors.

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Mobility Enhancement in Indium-rich N-channel $In_xGa_{1-x}As$ HEMTs by Application of <110> Uniaxial Strain

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Abstract— As in Si CMOS, the incorporation of mechanical strain offers the possibility of improving the performance of III-V field effect transistors (FETs). Quantifying its potential and providing fundamental understanding of the impact of strain are the goals of this study. This paper reports an investigation of the impact of <110> uniaxial strain on n-type InAlAs/InGaAs HEMTs with a 70% InAs channel core. The main impact of strain is found to be a modification of the electron effective mass and mobility. A comparison between the effect of <110> strain in Si and InGaAs suggests that strain engineering can indeed be leveraged to improve transport properties in deeply scaled InGaAs FETs.

I. Introduction

The incorporation of mechanical strain in the channel has greatly enhanced the carrier velocity and performance of both n- and p-type Si MOSFETs (1). As scaling approaches the end of the roadmap, InGaAs-based FETs are receiving a great deal of attention as a potential post-Si CMOS logic technology. (2-3) Just as with Si, in an effort to explore the ultimate potential of InGaAs for logic, strain is being investigated as a path to improve the performance of InGaAs FETs. (4-5)

In the literature, only a handful of experiments involving strain on actual FETs have been described. (6-7) In these studies, it is hard to attribute the observed changes entirely to strain-induced effects such as mobility enhancement, because the effects of strain and channel material composition were not separated (6), or the analysis was not detailed enough (7).

Our previous study showed that uniaxial strain can be used to improve the electrostatic control of n-type AlGaAs/InGaAs Pseudomorphic High Electron Mobility Transistors (PHEMT) with a low InAs mole fraction (15%) channel through the piezoelectric effect but offered little in terms of improved transport. (8) In the present work, we carry out a detailed experimental study of uniaxial strain effects on InAlAs/InGaAs HEMTs with a 70% InAs channel core and a scaled InAlAs barrier. In these devices we found that mobility change dominates the impact on the device characteristics that result from the application of uniaxial strain.

II. Experiments

To introduce controlled uniaxial strain in HEMTs, we designed and fabricated a mechanical apparatus to bend small chips (Fig. 1(*a*)). This apparatus allows the application of uniaxial strain up to ±0.3% to III-V chips with a size down to 2 mm x 4 mm. Four metal ridges at the center of the apparatus are used to apply force to the chip. Alternating the relative horizontal positions of the two pairs of ridges changes the type of strain (compressive or tensile) on the top surface of the chip. Due to their fragility, the III-V chips are mounted on a Ti plate together with a strain gauge (Fig. 1 (b)). The devices are wire-bonded to connection pads that connect them to a semiconductor parameter analyzer. The strain level has been calibrated through: 1) *in-situ* strain gauge measurements and 2) *ex-situ* curvature measurements by surface laser reflection.

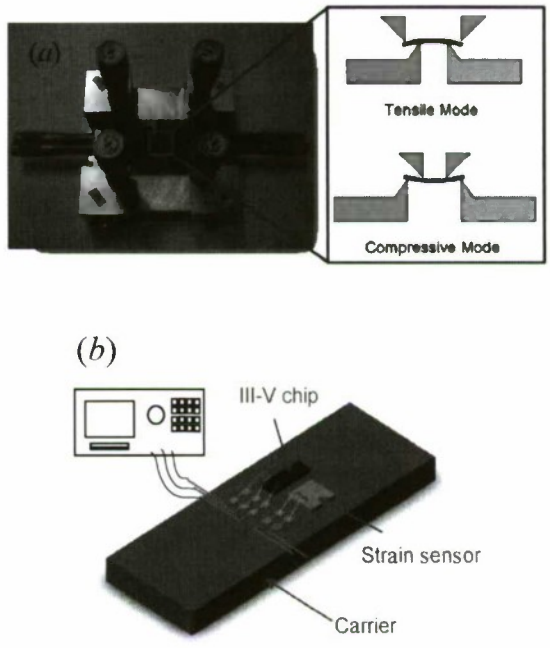

Fig. 1. (*a*) Chip-bending apparatus. (*b*) Experimental setup to characterize devices under uniaxial strain.

The devices used in this study are HEMTs with a thin indium-rich $In_{0.70}Ga_{0.30}As$-channel core. Fig. 2 sketches a cross section of these devices. Devices made on the same heterostructure have shown excellent logic scaling behavior down to gate lengths (L_g) of 30 nm. (9) In this study, in order to

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avoid short-channel effects, devices with L_g = 2 μm were fabricated. The gate was driven into the InAlAs barrier by a platinum-sinking technique (2). The final InAlAs barrier thickness is estimated to be 10 nm. Fig. 3 shows typical transfer characteristics of a representative device.

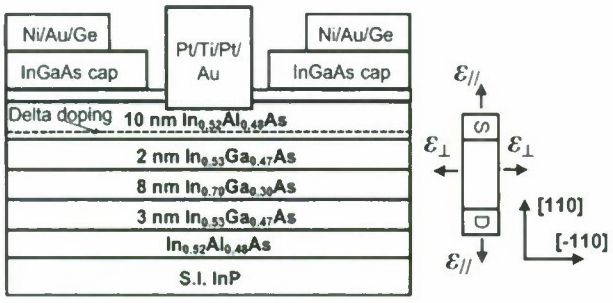

Fig. 2. (Left) Cross section of HEMTs used in this study. L_g = 2 μm. (Right) The configuration of applied strain.

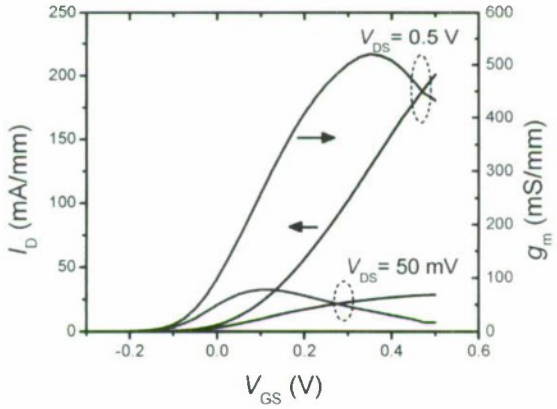

Fig. 3. Transfer characteristics of the device under study.

We performed bending experiments on devices with the channel oriented along the [110] direction. We sequentially applied tensile and compressive strain, both parallel ($\varepsilon_{//}$) and perpendicular ($\varepsilon_{\perp}$) to the channel direction, as indicated in Fig. 2. A set of electrical parameters were extracted by a benign characterization suite during bending experiments. We studied the strain dependence of V_T, defined at I_D=1 mA/mm, as a proxy for the device electrostatics, and the linear-regime drain current (I_{Dlin}) as a proxy for low-field transport. Both V_T and I_{Dlin} are determined at V_{DS}=50 mV to minimize heating effects and parasitic ohmic drops.

III. Results and Discussion

Fig. 4 shows the sequential change of V_T with $\varepsilon_{//}$. The fact that V_T tightly follows the loading and unloading of strain indicates that strain was successfully applied to the device and that no relaxation took place in the course of the experiment. Similar results were obtained with strain applied normal to the channel.

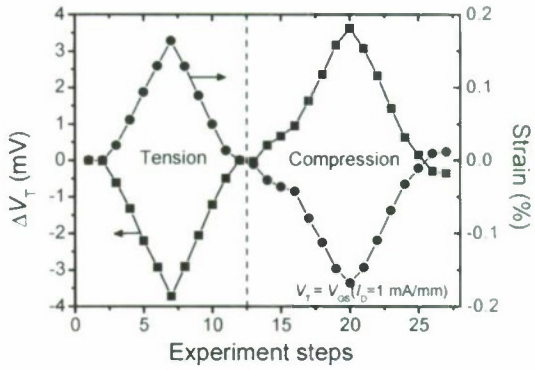

Fig. 4.Threshold voltage shift under $\varepsilon_{//}$.

Fig. 5 shows the change of threshold voltage (ΔV_T) for both strain along [110] ($\varepsilon_{//}$) and [-110] ($\varepsilon_{\perp}$). ΔV_T for the two <110> directions shows exactly the same dependence on strain. To avoid any interference from mobility change when using the constant current V_T definition, we also extracted V_T defined as the value of V_{GS} that corresponds to the extrapolation of the linear-regime drain current to zero. The conclusion that ΔV_T is independent of the strain orientation does not change.

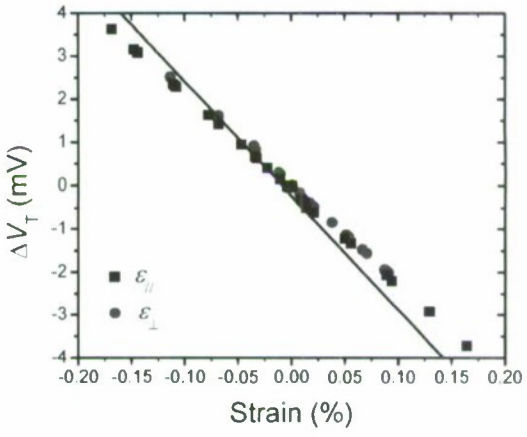

Fig. 5. Change of V_T as a function of <110> strain. The line corresponds to a model accounting for strain-induced $\Delta\phi_B$.

Fig. 6 shows the change in the Schottky barrier height ($\Delta\phi_B$) extracted from a thermionic-emission model for the forward I-V characteristics of the gate-source diode as a function of the change in V_T. The linear regression of $\Delta\phi_B$ to ΔV_T reveals that the dependence of ΔV_T on strain can be almost fully attributed to the strain-induced change in ϕ_B, which is due to the hydrostatic component of the applied strain and is orientation independent (8). The coefficient that determines the change in ϕ_B with strain is the conduction band deformation potential (a_c). a_c extracted from our experiment is -13 eV, which is within the range of -3.4 eV to -21 eV that is reported in the literature (13).

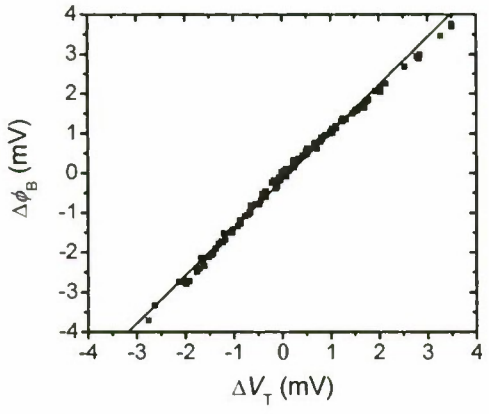

Fig. 6. Linear regression of $\Delta\ \phi_B$ to ΔV_T.

The orientation-independent ΔV_T behaviour observed in these InAlAs/InGaAs devices is different from our earlier report on AlGaAs/InGaAs PHEMTs (8). In the devices in (8), the sign of ΔV_T changes as one alters the strain direction from [110] to [-110]. This was attributed to the piezoelectric effect. The orientation-independent ΔV_T in the present InAs-rich devices indicates that the piezoelectric effect is negligible. The reason for this is the much reduced barrier and channel thicknesses in the present devices and the small piezoelectric constants of the InAs-rich alloys in the barrier and the channel. (10) The orientation-independent ΔV_T also implies that the change of the centroid capacitance, which is the primary mechanism behind the gate capacitance (C_G) shift in the AlGaAs/InGaAs PHEMTs (8), becomes insignificant in the present devices.

To investigate the impact of strain on transport in our InGaAs HEMTs, we have extracted the linear-regime drain current (I_{Dlin}) defined at a constant gate overdrive (V_{GS}-V_T=0.2 V) and V_{DS}=50 mV. Similar to strained Si MOSFETs, if C_G stays constant with strain, I_{Dlin} can be used as an indicator of mobility shift (11).

Fig. 7 shows the relative change of I_{Dlin} for strain along the two <110> directions. It is clearly seen that tensile $\varepsilon_{//}$ increases I_{Dlin}, and tensile $\varepsilon_{\perp}$ decreases I_{Dlin}. Compressive strain has the contrary effect.

Monte Carlo simulations of biaxial strain effects on $In_xGa_{1-x}As$ (12) show that strain changes the electron effective mass (m_e^*) and, as a consequence, the electron mobility (μ_e). To facilitate understanding of the essential physics, we have carried out 8x8 *k.p* simulations and calculated the band structure of InGaAs as affected by uniaxial strain. Band parameters from (13) were used. A Poisson ratio of 0.33 was used, which corresponds to the Ti plate as the mounted chip deforms with it.

Fig. 8 shows constant energy contours of the conduction band on the 2DEG plane. The constant energy contours elongate along the direction of compressive strain (left) and contract along the direction of applied tensile strain (right). The contrary happens along the normal direction. The elongation and contraction of the energy contours respectively correspond to the increase and decrease of m_e^*.

Values of m_e^* were extracted from the curvature of *E-k* curves along <110>. A pronounced anisotropy of m_e^* change is seen with <110> uniaxial strain. The relative change for the in-plane effective mass parallel to strain ($m_{//}^*$) is -7% per 1% strain, and +7% per 1% strain for the in-plane effective mass perpendicular to strain ($m_{\perp}^*$).

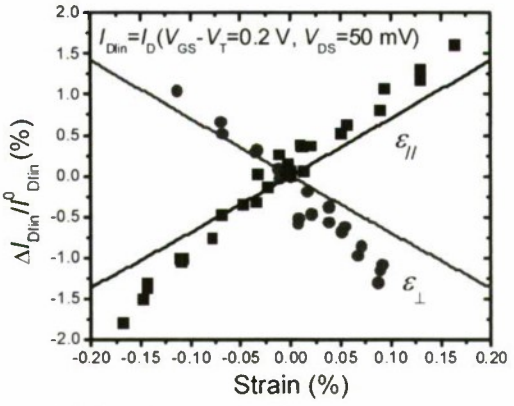

Fig. 7. Relative change of drain current in linear regime under <110> strain. The lines are results from *k.p* simulations.

In theory, the change in mobility ($\Delta\mu_e$) is a combination of changes in the conductivity effective mass (m_c^*) and scattering time (τ). However, in our present devices, little change is expected in τ. To the first order, the value of τ is determined by m_{DOS}^* ($=\sqrt{m_{//}^* m_{\perp}^*}$). Under <110> uniaxial strain, our k.p simulation results suggest that changes in $m_{\perp}^*$ and $m_{//}^*$ almost precisely cancel out. Hence, $\Delta\mu_e$ is mainly determined by changes in $1/m_c^*$. m_c^* is equal to $m_{//}^*$ when $\varepsilon_{//}$ is applied and to $m_{\perp}^*$ when $\varepsilon_{\perp}$ is applied. The solid lines in Fig. 7 represent the relative change in μ_e considering the change in $1/m_c^*$ due to <110> uniaxial strain as obtained from our *k.p* simulations. The μ_e reduction/enhancement factors predicted by $1/m_c^*$ are +7% and -7% per 1% strain, close to those experimentally measured in I_{Dlin} (+9.9% and -11.0% per 1% strain).

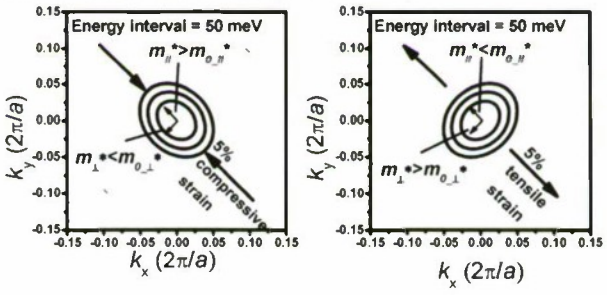

Fig. 8. Constant energy contour on the 2DEG conduction plane of InGaAs, under 5% <110> uniaxial compression (left) and tension (right).

To benchmark the <110> uniaxial strain effect on the InGaAs mobility, we compare it with that of Si (14-17). As shown in Fig. 9, similar to InGaAs, the <110> m_e^* of the 2-fold valleys in Si obtained by empirical non-local pseudopotential simulations changes anisotropically with applied <110> uniaxial strain. (14, 16-17) The <110> experimental μ_e data obtained from ultrathin-body Si FETs manifests this anisotropic change of m_e^*. (14) The mobility enhancement in Si, in addition

to the change in m_e^*, might arise from reduced inter-valley scattering. It can be seen that the experimental mobility enhancement (14-15) as a result of 1% $\varepsilon_{//}$ is almost 4x higher in Si than in $In_{0.7}Ga_{0.3}As$.

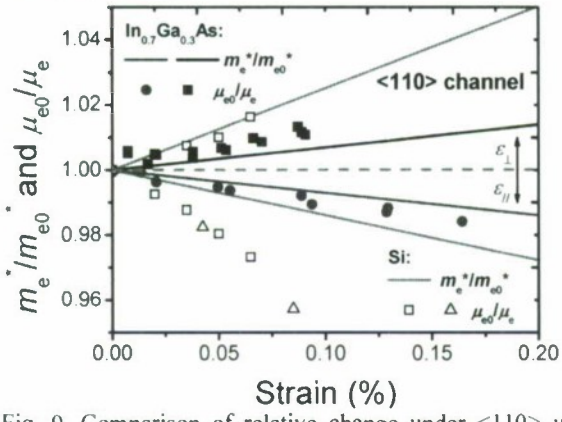

Fig. 9. Comparison of relative change under <110> uniaxial tensile strain in m_e^* and μ_e between Si (14-16) and $In_{0.7}Ga_{0.3}As$. The ratio of unstrained over strained μ_e is plotted, to compare with the effect in m_e^* reduction/enhancement. Continuous lines are simulations and symbols are experimental data.

In very short devices, the most important transport parameter is the high-field electron velocity and not the low-field mobility. (18-19) The effective electron velocity is a portion of the thermal velocity which is itself propotional to $(m_e^*)^{-1/2}$. (18) In fact, HEMTs with InAs channel cores have already demonstrated >2x higher electron injection velocity than strained Si MOSFETs thanks to the much smaller m_e^* in InAs. (20) Fig. 10 shows the simulated m_e^* reduction under 1 GPa <110> tensile stress for $In_xGa_{1-x}As$ with x ranging from 53% to 100% on an InP substrate or fully relaxed as on a suitable metamorphic substrate. For reference, the simulated reduction in m_e^* of the 2-fold valleys in Si (14, 16) under the same level of tensile stress is also indicated. The choice of the same stress level (as opposed to strain level) for the comparison is reasonable since stress more closely reflects the technological effort involved.

As more InAs is incorporated into the channel, the m_e^* reduction becomes more pronounced. A pure InAs channel on an InP substrate shows the same level of m_e^* reduction as Si does. Furthermore, if the lattice-mismatch induced biaxial compressive strain in the channel could be relieved, the m_e^* reduction factor can be further enlarged, exceeding that of Si.

One concern of further m_e^* reduction in materials with small m_e^* is that the current drivability of the device suffers as a result of a reduction in gate capacitance that is dominated by the quantum capacitance. (21) However, the quantum capacitance is set by the m_{DOS}^* and, as discussed before, this is little affected by uniaxial strain.

IV. Conclusion

We have investigated <110> uniaxial strain effects on InAlAs/InGaAs HEMTs with an InAs-rich channel by chip-bending experiments. We have found that uniaxial strain changes the electron mobility through a change in the effective mass. *k.p* simulations suggest that the effective mass reduction factor can exceed that of Si by incorporating more InAs in the channel and relieving the lattice-mismatch biaxial strain. This result indicates that strain engineering can be leveraged to improve the transport properties of InGaAs FETs, especially in deeply scaled devices.

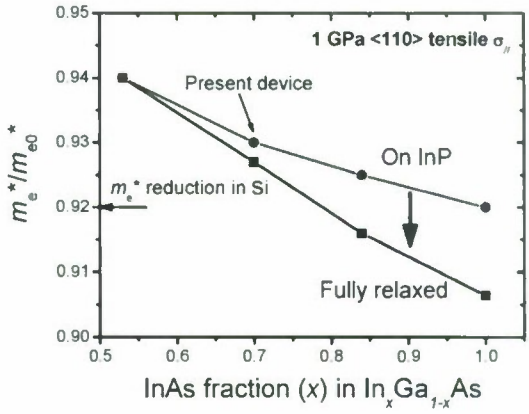

Fig. 10. Effective mass reduction factors obtained from *k.p* simulations for $In_xGa_{1-x}As$ with various InAs fraction. Incorporation of high InAs composition and relief of the lattice-mismatch strain enlarge the m_e^* reduction factor.

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DC and RF Characteristics of InAs-Channel MOS-MODFETs Using PECVD SiO_2 as Gate Dielectrics

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Abstract

Small-bandgap InAs channel materials are potential candidates for high-speed and low-power applications and have been demonstrated in AlSb/InAs/AlSb QWFETs. Taking advantage of their excellent transport properties, we successfully develop an InAs-channel metal-oxide-semiconductor modulation-doped field-effect transistor (MOS-MODFET) using 100-nm PECVD-deposited SiO_2 dielectrics for gate dielectrics. A 2μm-gate-length depletion-mode InAs n-channel MOS-MODFET shows a maximum drain current of 270 mA/mm, a peak transconductance of 189 mS/mm, and a low output conductance of 18 mS/mm in dc characteristics, and a maximum current-gain cut-off frequency of 14.5 GHz and a maximum oscillation frequency of 24.0 GHz in rf performances. The InAs-channel MOS-MODFET presents potentials for further developing complementary circuit devices.

Keywords- InAs, metal-oxide-semiconductor modulation-doped field-effect transistor (MOS-MODFET)

I. Introduction

In the continuing pursuit of Moore's Law, the Si integrated circuit industry is expected to reach the scaling limit beyond 22-nm technology generation. As such, increased interests focus on alternative materials for use in future-generation transistor circuitry. High transport properties of III-V materials are currently under intensive investigation to further improve the device performance. InAs is one of the important candidates for the channel materials due to a high electron mobility of 33,000 $cm^2/V\text{-}s$ and a large Γ-L valley separation of ~0.9 eV that enable a very high peak velocity of $>3.5\times10^7$ cm/s [1][2]. Because the primary difficulty for developing III-V MOSFETs is the lack of high-quality insulator-semiconductor interface, a lot of research efforts have been made on the developments of gate dielectrics deposited on the III-V compounds, which include Ga_2O_3, Gd_2O_3, Al_2O_3, SiN_x, and HfO_2...etc [3]. The InAs MOS capacitors fabricated by composite oxides [4] and SiO_2 [5] in early studies suffered negative flat-band shift and large hysteresis, indicating high densities of both interface states and bulk fixed charges. Recently, Ning et al. [6] reported the results of InAs MOS capacitors and FETs, which were fabricated on a bulk InAs material using ALD-deposited Al_2O_3 dielectrics. The FETs had an issue of incomplete pinch-off while low leakages were demonstrated in the MOS capacitors.

A layer structure of the InAs channel layer atop of lattice-matched Al(Ga)Sb buffer materials grown by MBE on a semi-insulating GaAs substrate was proposed in this work. The epitaxy materials were fabricated into depletion-mode InAs n-channel MOS-MODFETs using the SiO_2 gate dielectrics that were deposited by plasma-enhanced chemical vapor deposition (PECVD). Epitaxy growth, device development, and electric characterization will be introduced in the following.

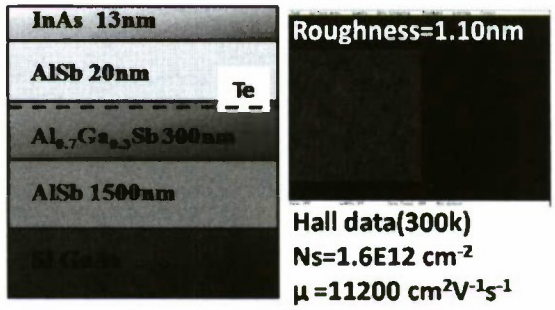

Fig. 1 Layer structure, AFM, and Hall data of as-grown epitaxy materials.

II. Growth and Device Fabrication

The InAs MOS-MODFETs epiyaxy materials were grown

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by solid-source molecular beam epitaxy (MBE) on a semi-insulating (001) GaAs substrate. Growth was initiated with a 0.1μm-thick smoothing layer of GaAs and a 10nm-thick transition layer of AlAs just before the nucleation of a 7% mismatched AlSb buffer layer. The AlSb buffer layer, grown at 540 °C, was 1.5μm thick and served primarily to reduce the high density of threading dislocations to be below 10^8 cm^{-2}. A 0.3 μm-thick $Al_{0.75}Ga_{0.25}Sb$ layer was inserted prior to the growth of the InAs-channel MOS-MODFETs active layers. The $Al_{0.75}Ga_{0.25}Sb$ layer, grown at 500 ℃, provided a stable surface at the step of device mesa isolation. The MOS-MODFETs active layers were grown at 430 ℃ and consisted of a 20nm AlSb bottom barrier layer and a 13nm InAs channel layer. A planer tellurium (Tc) modulation doping sheet of 2×10^{12} cm^{-2} was applied 25nm below the channel layer. During the period of cooling the epitaxy wafers, an arsenic flux of 1.4×10^{-7} torr was applied to the wafer surface until a substrate temperature of 200 ℃ was reached. The As-capped surface could help prevent the beneath epitaxy materials from direct exposure to the atmosphere and consequent formation of native oxides when the as-grown epitaxy wafers was transferred from a MBE to a PECVD system for depositing SiO_2 gate dielectrics. The native oxides would be difficult to be removed completely and further degrade the semiconductor-dielectric interface quality. Figure 1 shows the layer structure, AFM picture, and 300K Hall data of the as-grown epitaxy materials. A roughness of 1.10 nm, a carrier density of 1.6×10^{12} cm^{-2}, and a mobility of 11,200 cm^2/V-s were obtained.

The as-grown epitaxy wafer that were loaded into the PECVD system was first performed an As-desorption baking at 300℃ for 30 seconds to remove the excess As atoms at the surface, and was immediately deposited a 10nm SiO_2 gate dielectric layer at the same temperature. Following a SiO_2 removal by a dry etch and a subsequent surface pretreatment by a standard HCl solution at source and drain contact areas, Pd/Ti/Pt/Au ohmic metals were deposited on the InAs channel layer and alloyed at 300 ℃ for 10 s by rapid thermal annealing (RTA). Device mesas were then defined by a dry etch, which stopped in the $Al_{0.7}Ga_{0.3}Sb$ layer. After Ti/Pt/Au gates were fabricated on the SiO_2 dielectrics, metallic probing pads of Ti/Au were made in the final. Device gate length and width are 2 and 50×2 μm respectively. Transmission-line measurement showed a contact resistance of 0.26 ohm-mm and a sheet resistance of 350 ohms/square, which was slightly higher than the 339 ohms/square value determined by the Hall measurement on the SiO_2-capped epitaxy materials. Figure 2 shows the energy band diagram of the device structure that was simulated using a vacuum work function of titanium in a self-consistent one-dimensional (1-D) Poisson-Schrödinger solver [7]. A cross-sectional schematic of the InAs-channel MOS-MODFET is shown in Fig. 3.

III. Results and Discussions

Figure 4 and 5 present the drain and transfer characteristics of a MOS-MODFET with 2μm gate length. Drain-source saturation currents (I_{DSS}) and output conductances (g_{DS}) at V_{DS} = 2.0 V and V_{GS} = 0 V are 154 mA/mm and 18 mS/mm, respectively. Peak transconductance ($g_{m,peak}$) is 189 mS/mm

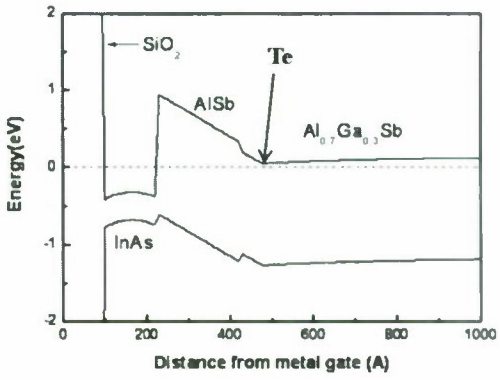

Fig. 2 Calculated energy band diagram of an InAs-channel MOS-MODFET.

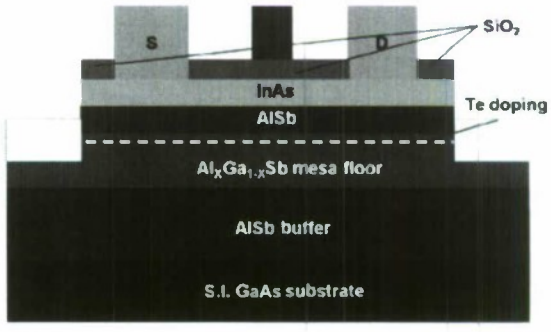

Fig. 3 Cross-sectional schematic of an InAs-channel MOS-MODFET.

obtained at V_{ds}=2.0V and V_{GS} = -0.3 V. In addition, the output conductances of InAs-channel MOS-MODFETs are much lower than those of conventional InAs/AlSb HEMTs [8][9][10], which are primarily generated by the accumulation of impact-ionized holes in the buffer. Assisted by the enhanced hole confinement in the InAs channel using the wide-bandgap SiO_2 gate dielectric and the n-type Te modulation sheet in the buffer, the output conductances of the MOS-MODFETs are remarkably reduced. For example, the out conductance obtained at V_{DS} = 2.0 V is at least ten times smaller than that of the conventional InAs/AlSb HEMTs obtained at V_{DS} = 0.5 V.

Figure 6 shows sub-threshold gate and drain characteristics. The drain I_{on}-I_{off} ratio is 256 and subthreshold swing is 324 mV/dec at V_{ds} = 1.0V. Gate leakage is as low as 0.158 mA/mm at V_{gs}= -1.5 V and V_{ds}=1.0 V. A weak dependence of gate currents on gate biases and inconsistency of gate and drain currents in the deep subthreshold region may indicate a leakage path at device surface. The poor interface between the SiO_2 dielectric and the InAs channel layer is suspected to provide the leakage path. More works are needed to improve the semiconductor-dielectric interface quality.

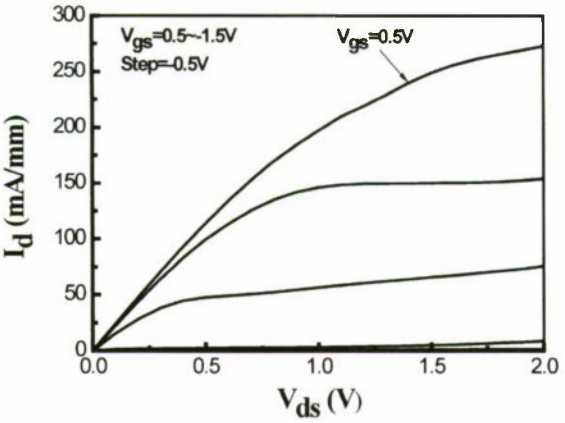

Fig. 4 Drain I-V characteristics

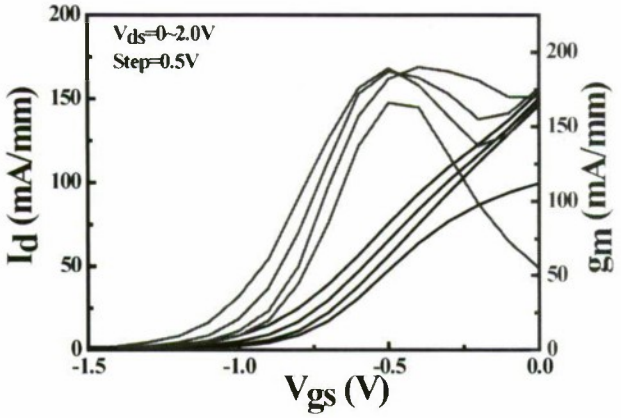

Fig. 5 Drain current and transconductance against gate bias

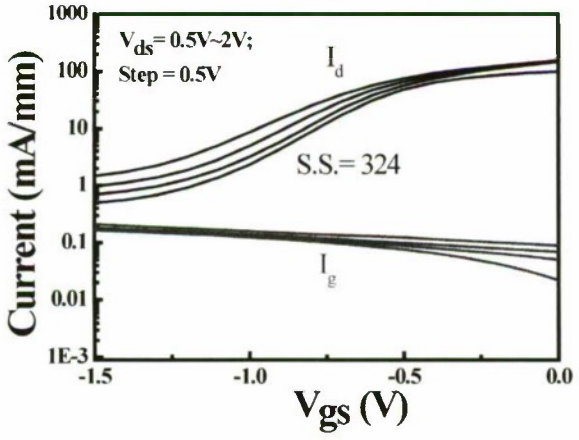

Fig. 6 Gate and drain subthreshold behaviors as function of gate bias

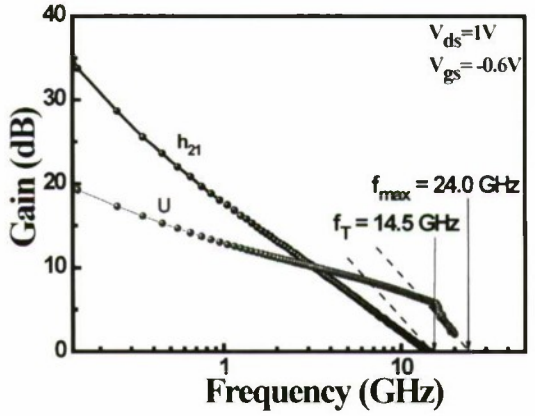

Fig. 7 Current and power gains as function of frequency

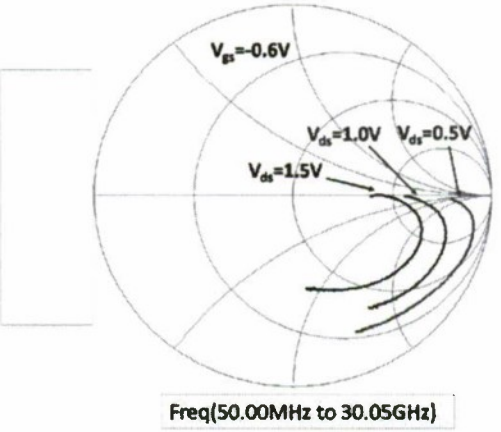

Fig. 8 Smith chart showing S_{22} at drain voltages of 0.5, 1.0, and 1.5 V, respectively. V_{GS} is -0.6V.

S-parameters of the InAs-channel MOS-MODFET were measured from 1 to 20 GHz using a Cascade Microtech on-wafer probing system along with a HP8510C network analyzer. The short-circuit current-gain cut-off frequency (f_T) and the maximum oscillation frequency (f_{MAX}) were determined by extrapolating the current gain (h_{21}) and the unilateral power gain (U) curves to 0 dB, respectively, using -20 dB/decade slopes. The MOS-MODFET with 2 μm gate length yielded an f_T = 14.5 GHz and an f_{MAX} = 24.0 GHz at V_{DS} = 1.0 V and V_{GS} = -0.6 V (Fig. 7). Figure 8 shows three S_{22} parameters swept from 50 MHz to 30.05 GHz in a Smith chart at V_{gs} = -0.6 and V_{ds} = 0.5, 1.0, and 1.5V, respectively. Inductance characteristics, which are characterized as the sign for the impact ionization effect [11], are not observed at a drain bias as high as 1.5 V. The lack of inductances in the Smith chart provides another evidence of suppressing the impact ionization effects in the MOS-MODFET devices and is consistent with the low output conductances observed in the I-V characteristics.

IV. CONCLUSIONS

This work demonstrated for the first time the dc and rf characteristics of InAs-channel MOS-MODFETs using PECVD-deposited SiO_2 for gate dielectrics. A 2-μm gate-length MOS-MODFET exhibited a low output conductance of 18 mS/mm, an f_T of 14.5 GHz, and an f_{MAX} of 24.0 GHz. Non-ideal gate leakage and subthreshold behaviors were attributed to an additional leakage path at device surface which were generated by poor dielectric-semiconductor interfaces. The InAs-channel materials promise further studies in MOSFET development for future complementary circuit device applications.

V. ACKNOWLEDGMENT

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