A Preamplifier-Shaper-Stretcher Integrated Circuit System for Use with Germanium Strip Detectors

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Abstract

A 16-channel Integrated Circuit readout electronics chip is being developed for use with a germanium strip detector. Such a system will provide superior energy resolution with 2-dimensional imaging in a single instrument that can be used for X-ray imaging and nuclear line gamma-ray spectroscopy. As part of the total ASIC development, prototype ICs of a typical channel have been designed, fabricated and tested. These integrated circuits include a low-noise, variable gain, preamplifier circuit that can detect both positive and negative going input charges, a 4-pole pulse shaper with variable peaking times and a stretcher circuit that can do a peak detect and hold for the different peaking times. The integrated circuits are fabricated in a 1.2 micron n-well CMOS process. The noise performance for this system was measured to be 185erms +14e/pF for a 2μs peaking time and gain at ~200mV/fC. Linearity measurements in both inverting and non-inverting modes of operation were approximately +/-1%. Peaking times from 0.5 microseconds to 8 microseconds and gain adjustments to get up to 400mV/fC per channel were done through digital switching.

I. Introduction

Solid-state strip detectors based on germanium or CdZnTe are gaining importance in a variety of x-ray detection applications that require both good spatial resolution and excellent energy resolution. These detectors require compact, low-noise electronics with a high number of channels and the capability to measure both signal polarities over a wide dynamic range [1-4]. The preamplifier-shaper-stretcher system described in this paper is part of a typical channel in the final version of the chip that will include discriminators and other capabilities for remote setup and reading of data. Each part of the system under discussion is fabricated as a separate 4-channel chip in standard 1.2μm n-well CMOS process. The preamplifier chip consists of three components – a basic charge to voltage converter, an inverter section to invert opposite polarity charges and a switchable gain stage. This is followed by a shaper chip based on a 4-pole Sallen-Key design with switchable shaping times of 0.5 microsecond to 8 microseconds peaking. A stretcher circuit follows the shaper circuit. The stretcher chip itself is comprised of three sections, the peak-detect circuit, the hold circuit and the logic control to generate and adjust the hold and associated signals. A block diagram of a single channel of preamplifier-shaper-stretcher system is given in Fig. 1. In the following sections, we describe the design and test results of each of the blocks.

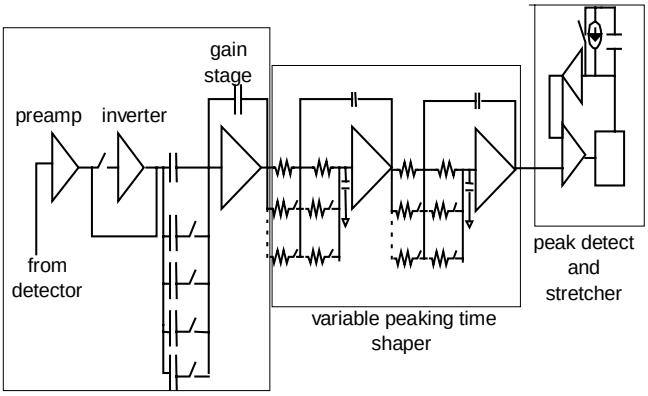

Figure 1: Single channel block diagram.

II. Charge Sensitive Preamp Design

The preamp section consists of three stages. The first stage is a charge to voltage amp with a gain of -10mV/fC. The second stage is a unity gain inverting amplifier stage that is switched on only for positive going pulses. The third stage is a voltage amp with a gain of –1V/V to –20V/V. This gives an adjustable gain of up to 200mV/fC across the preamplifier–inverter-gain stage. The preamplifier circuit is a low noise, dual-polarity charge amplifier circuit with a novel adjustable feedback. The design is based on the low noise preamp topology given by Britton [5].

It is composed of an inverting, single gain stage, cascode amplifier followed by a non-inverting, level shifting buffer stage with a combined 0.1pF poly-poly feedback capacitor. The feedback capacitor is split between the output of the cascode amp and the output of the common drain, level shifting buffer that is designed using fet devices available in the CMOS process. This first stage input is referenced to an adjustable reference voltage. The reference voltage is set closer to the positive rail so that its output swings towards the negative rail for positive input charges. For negative input charges the reference voltage is set closer to the negative rail so that its output swings towards the positive rail.

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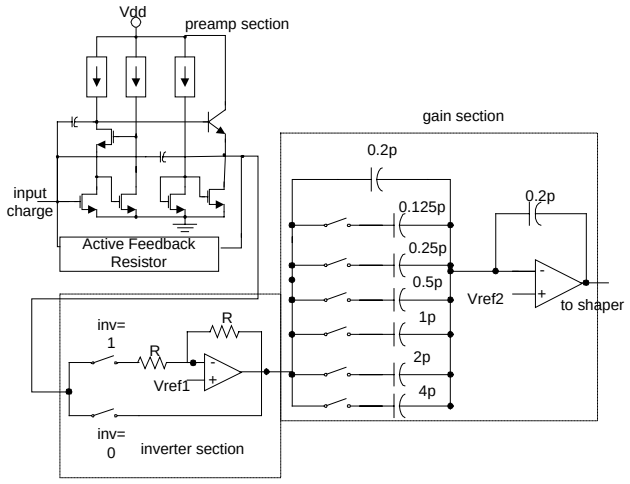

Figure 2: Preamplifier, Inverter and Gain Sections.

The inverter section is switched on only for positive going input charges so that all signals (for positive or negative going input charges) that reach the input of the gain stage swing towards the positive rail. The gain stage is an inverting voltage amp that is referenced to a voltage of 3.5V. Its output swings towards the negative supply for all input charges. It has switchable gain stages with various gains realized by input capacitor switching as shown in the block diagram of the preamplifier section of Figure 2.

III. Shaper Design

A gaussian pulse shaping method gives a signal to noise ratio closest to the maximum that is theoretically possible.

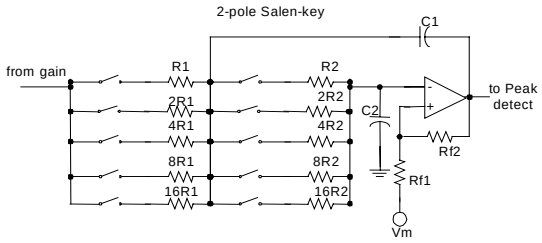

Figure 3: LPF unit used in the Shaper Section.

Therefore, a pulse shaping method was chosen so that it was possible to get an approximate gaussian shape for the spectroscopy in order to get the best signal to noise ratio [6]. This was done using a combination of the CR from the preamplifier section followed by two 2-pole Sallen-Key low pass filters (as shown in Figure 3) placed end to end to give a total CR-RC^4 semi-gaussian shaping method. The 2-pole LPFs are designed so that they could realize a gain greater than one each and are also designed so that both the poles of each filter are at the same location.

A gain of two is realized across both the LPF sections together. The peaking times of both the stages can be switched by switching in respective input resistances as shown in Figure 3 to give individual, selectable peaking times of 0.5, 1, 2, 4 and 8 microseconds. Since the shaper stage has an additional gain of 2, this gives a total gain range of up to 400mV/fC across the entire channel.

IV. Peak Detect Circuit and Stretcher

This section consists of the circuitry needed for peak detect, track and hold of the peak signal out of the shaper. The design is a modification of the CMOS peak detect and hold circuit based on the topology introduced by Kruikamp and Leenaerts [7].

A simplified block diagram of the Peak Detect and Hold (PDH) circuit is given in Figure 4. It is designed to detect and hold negative going pulses referenced to 3.5V. A linear gate architecture that consists of 2 differential input stages is used to prevent pileup of incoming signals. In the track mode, the input from the shaper is tracked. But once the peak is detected, the hold loop is tied to the Vref signal of 3.5V. This prevents a second input signal from further charging the capacitors. Only one of these two complementary differential input stages is ON at any time. A detailed description of this modified stretcher topology is given in reference [8].

The Control signal generator implements the linear gate controls referenced to as lgate and lgateb in the figure below. This control generator can also be reset, enabled or disabled by external signals. The stretcher hold time for holding the peak value of the shaper output is thus adjustable.

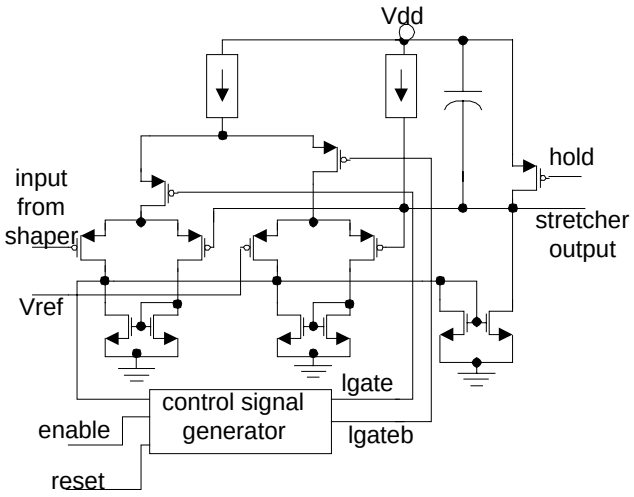

Figure 4: Peak detect Circuit and Stretcher.

V. TEST RESULTS

The test setup was designed to test the chips as a typical channel. Each block of the system was designed as a tiny-size (2.2 mm. x 2.2 mm.) chip in a 1.2 micron process. The input charge pulses were given to the preamplifier chip, whose output was connected to the shaper chip and whose output in turn was connected to the peak-detect and stretcher chip. Tests were done for different peaking times. The shaper outputs for the 1 and 4 microsecond cases are shown in Figures 5 and 6 respectively.

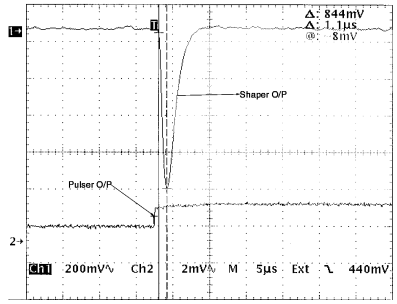

Figure 5: Shaper output for 1 microsecond peaking.

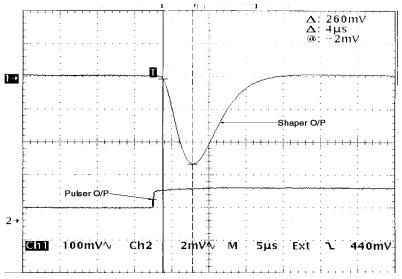

Figure 6: Shaper output for 4 microsecond peaking.

The noise measurements were done using an analog oscilloscope in which the rms noise value is 1/5 the peak-to-peak envelope. All relevant measurements were taken at the stretcher output when the stretcher was in tracking mode. Hence all graphs pertain to an entire channel system. Noise measurements were done for the same input charge, for different peaking times for both inverting and non-inverting modes of operation with an equivalent input capacitance of about 6pF. Gain adjustments were done to get the best shaping for each peaking time. Figure 7 and Figure 8 give the noise measurements across the system for the non-inverting and inverting modes of operation respectively. Noise measurements done for absolute 0pf (with the bond trace disconnected) was measured at 185erms for a 2µs peaking time (5.6µs FWHM), and gain at ~200mV/fC. The noise measured for an input capacitance of 50.5pF for the same settings was 964 erms. The total electron noise of the preamplifier-shaper is given by 185erms +14e/pF.

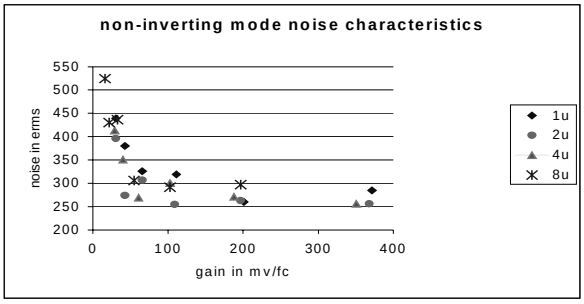

Figure 7: Noise characteristics for the non-inverting mode.

The noise in electron rms value versus the total gain of the system shows a break in characteristics at approximately 45mV/fC. At gains less than this, the noise contribution from the stages after the preamplifier, become a larger fraction of the input signal itself.

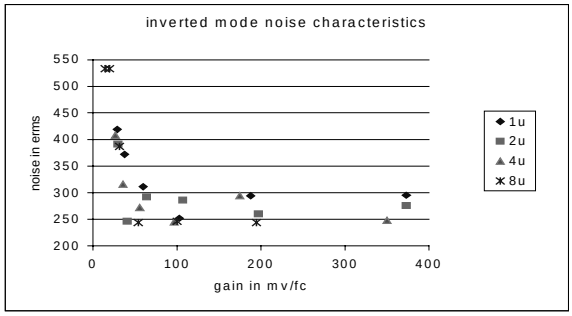

Figure 8: Noise characteristics for the inverting mode.

Power consumption was approximately 10mW per channel for this test setup. Linearity measurements were done for all peaking times at a gain of 100mV/fC. These results are given in Figure 9. Linearity numbers remained virtually unaffected by the two different modes of operation. They remain about +/-1 % in most cases.

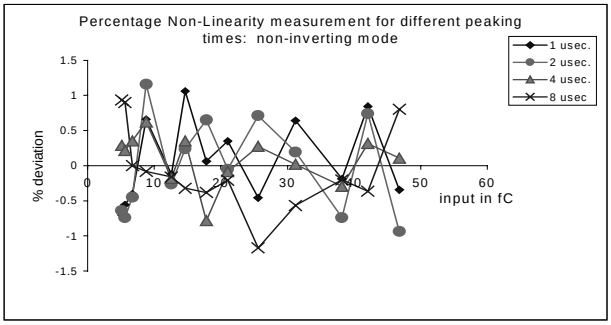

Figure 9: Non-Linearity in % for the different peaking times.

VI. Conclusions

A preamplifier-shaper-stretcher system has been designed and tested as part of the development of a 16-channel ASIC readout chip. Based on the results of the chips just discussed an integrated ASIC was designed with discriminator, serial control and other novel features for a one-chip solution for gamma ray spectroscopy and other like applications. A prototype of the multi-channel integrated ASIC that combines the three components of the described test system in one chip is currently being fabricated in a 1.2 micron process.

VII. Acknowledgements

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